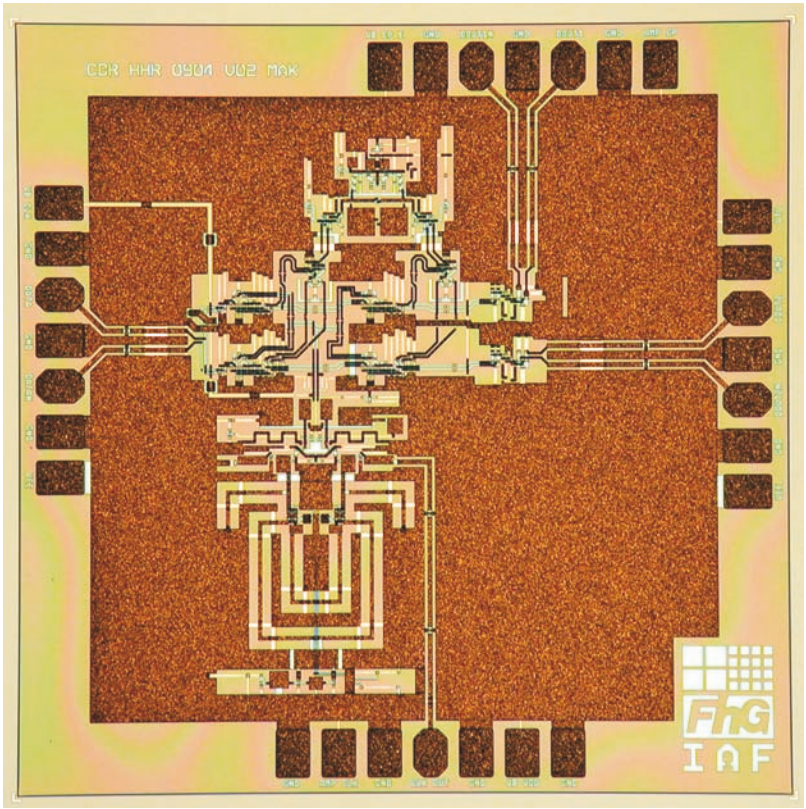
Robert Elvis Makon

InP DHBT-based Clock and Data Recovery Circuits for Ultra-High-Speed Optical Data Links



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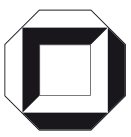

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Contents

Abstract

In today's optical access telecommunication networks, 10 Gbit/s transmission systems are well established. In order to accommodate the steadily increasing demand for larger transmission capacity, 40 Gbit/s transmission systems are being evaluated and are getting close to commercial deployment. Next generation optical data networks will be operated at a data speed of 80 Gbit/s. In the receiver part of such networks, the clock and data recovery (CDR) circuit is among, if not, the most critical key component.

In this work, up to 80 Gbit/s CDR circuits with 1:2 demultiplexer are developed. The integrated circuits are manufactured using an (in-house) InP double heterojunction bipolar transistor (DHBT) technology, featuring cut-off frequency values of more than 250 GHz for both f_T and f_{max}. The used CDR concept is based on a phase-locked loop (PLL) topology including a half-rate linear phase detector, a loop filter, and a voltage controlled oscillator (VCO) as the main circuit components.

The implementation of the fully integrated CDR circuits is preceded by the development of the corresponding main components as stand-alone circuits. Thus, differential LC VCOs were designed and realized, which are capable of delivering frequency signals for half- and full-rate data sampling at data rates beyond 80 Gbit/s. A first VCO version targeting the 43 GHz operation range features a tuning bandwidth of 7 GHz. Within this tuning bandwidth, very low phase noise values down to -109 dBc/Hz at 1 MHz offset are achieved, while a single-ended output power up to 3 dBm is obtained.

A second VCO version aiming the 86 GHz operation range features a tuning range of 6 GHz. Within this tuning range, very low phase noise values down to -102 dBc/Hz are obtained at 1 MHz offset, while a single-ended output power up to 5 dBm is achieved. Regarding both VCO versions, the overall achieved performance is comparable, if not, better than the state-of-the-art, independently of the considered device technology.

As a further CDR main component, a half-rate linear phase detector (PD) including an 1:2 demultiplexer was also developed. This phase detector is monolithically integrated with the CDR loop filter, thus allowing a clear interpretation of the operation of the PD component. The data recovery is performed within the phase detector in form of two demultiplexed output data channels. Proper data regeneration is obtained at data rates exceeding 80 Gbit/s.

Based on the achievements regarding the single CDR components, fully integrated CDR circuits showing proper operation at data speed up to 80 Gbit/s were developed. Concerning the 80 Gbit/s CDR circuit, the recovered and demultiplexed 40 Gbit/s data

feature clear eye opening with a voltage swing as high as 600 mV_{pp}. The extracted 40 GHz clock signal from the input data shows an excellent phase noise value of -98 dBc/Hz at 100 KHz offset. The corresponding rms jitter is as low as 0.365 ps, while the peak-to-peak jitter amounts to 1.66 ps. The tracking range of the CDR circuit is measured to be 100 MHz. The proper operation at 80 Gbit/s illustrates the highest data rate published to date for a CDR circuit, regardless of all competing semiconductor technologies.

Aiming the characterization of the realized CDR circuits up to their operation speed limit, multiplexing components acting as high-speed data source were developed. A 2:1 selector circuit, as a first version of the implemented multiplexing components, features proper operation at data rates up to 105 Gbit/s. A signal swing of 600 mV_{pp} is available at the two complementary outputs of the selector circuit. Very low power operation is achieved at data rates up to 90 Gbit/s.

A 2:1 full multiplexer, as a second circuit version intended for the generation of high-speed data, was also developed. This full multiplexer features proper operation at data rates up to 80 Gbit/s. A signal swing as high as 600 mV_{pp} is obtained at the corresponding single-ended output.

Summarizing, the outstanding and (to some extent) record achievements in this work make an essential contribution to the development of future optical telecommunication networks operating at 80 Gbit/s.

Zusammenfassung

In den heutigen Telekommunikationsnetzen mit optisch basiertem Zugang sind 10 Gbit/s Übertragungssysteme Standard. Um der stetig wachsenden Nachfrage nach mehr Übertragungsbandbreite entgegenzukommen, werden 40 Gbit/s Übertragungssysteme herangezogen, welche in den Startlöchern eines kommerziellen Einsatzes stehen. Datenübertragungssysteme der nächsten Generation sind für den Betrieb bei einer Datenrate von 80 Gbit/s bestimmt. Auf der Empfängerseite von solchen Übertragungssystemen ist die Takt- und Datenrückgewinnungsschaltung (CDR) eine der entscheidenden Komponenten mit dem komplexesten Aufbau.

In dieser Arbeit werden CDR-Schaltungen mit eingebautem 1:2 Demultiplexer entwickelt, die Arbeitsgeschwindigkeiten von bis zu 80 Gbit/s aufweisen. Die für die Entwicklung dieser integrierten Schaltungen zugrundeliegende Halbleitertechnologie ist eine hauseigene InP-basierende Doppelheterostruktur-Bipolar-Transistor-(DHBT)-Technologie. Diese Technologie zeichnet sich durch Grenzfrequenzen f_T und f_{max} aus, die oberhalb von 250 GHz liegen. Das verwendete CDR-Konzept beruht auf der Topologie einer Phasenregelschleife (PLL). Zu den Hauptkomponenten der CDR-Schaltung zählen ein linearer Half-Rate-Phasendetektor, ein Schleifenfilter und ein spannungsgesteuerter Oszillator (VCO).

Als Vorstufe zur Realisierung der monolithisch integrierten CDR-Schaltungen sind die einzelnen zugehörigen Hauptschaltungskomponenten als eigenständige Schaltungen entwickelt worden. Diesbezüglich sind LC-VCOs in differentieller Topologie realisiert worden, die sich sehr gut als Frequenzquellen für Half- und Full-Rate-Anwendungen bei Datenraten über 80 Gbit/s eignen. Eine erste VCO-Ausführung mit Arbeitsfrequenzen um 43 GHz zeichnet sich durch eine Abstimmungsbandbreite von 7 GHz aus. Innerhalb dieser Abstimmungsbandbreite weist der VCO sehr niedrige Phasenrauschenwerte mit einem Minimum von -109 dBc/Hz bei 1 MHz Offsetfrequenz auf, während eine auf einen Ausgang bezogene Ausgangsleistung von bis zu 3 dBm erzielt wird.

Eine zweite VCO-Ausführung mit Arbeitsfrequenzen um 86 GHz zeichnet sich durch eine Abstimmungsbandbreite von 6 GHz aus. Innerhalb dieser Abstimmungsbandbreite werden sehr niedrige Phasenrauschenwerte mit einem Minimum von -102 dBc/Hz bei 1 MHz Offsetfrequenz erzielt, während eine auf einen Ausgang bezogene Ausgangsleistung von bis zu 5 dBm erreicht wird. Mit Bezug auf beide VCO-Ausführungen sind die insgesamt erzielten Schaltungsergebnisse vergleichbar und zum Teil besser als der Stand der Technik, wobei die Aussage unabhängig von der betrachteten Halbleitertechnologie

gilt.

Als eine weitere Hauptkomponente der CDR-Schaltung ist ein linearer Half-Rate-Phasendetektor (PD) mit eingebautem 1:2 Demultiplexer realisiert worden. Die Schaltung des Phasendetektors beinhaltet ebenfalls das CDR-Schleifenfilter, um eine eindeutige Interpretation der vom Phasendetektor erzeugten Steuersignale zu ermöglichen. Die Datenrückgewinnung erfolgt innerhalb des Phasendetektors in Form von zwei demultiplexten Ausgangsdatenkanälen. Es wird eine einwandfreie Datenregenerierung bei Datenraten über 80 Gbit/s erzielt.

Basierend auf den gewonnenen Erkenntnissen aus der Entwicklung der einzelnen CDR-Hauptschaltungskomponenten sind monolithisch integrierte CDR-Schaltungen realisiert worden, die bei Datenraten von bis zu 80 Gbit/s einwandfrei arbeiten. Mit Bezug auf die realisierte 80 Gbit/s CDR-Schaltung zeichnen sich die regenerierten und demultiplexten 40 Gbit/s Ausgangsdaten durch weit geöffnete Augendiagramme mit einem Ausgangsspannungshub von 600 mV_{pp} aus. Das extrahierte 40 GHz Taktsignal aus den Eingangsdaten zeigt ein exzellentes Rauschverhalten mit einem Phasenrauschenwert von -98 dBc/Hz bei 100 KHz Offsetfrequenz. Der entsprechende rms-Jitter beträgt 0.365 ps, während der Peak-to-peak-Jitter einen relativ kleinen Wert von 1.66 ps aufweist. Der Ausrastbereich der CDR-Schaltung liegt bei 100 MHz. Unabhängig von der betrachteten Schaltungstechnologie stellt der erzielte (einwandfeie) CDR-Betrieb bei der Datenrate von 80 Gbit/s einen Weltrekord mit Bezug auf alle bisher veröffentlichten Arbeiten über CDR-Schaltungen dar.

Hinsichtlich der messtechnischen Charakterisierung von CDR-Schaltungen bis zu dem zugehörigen Geschwindigkeitslimit sind Multiplexer-Schaltungskomponenten realisiert worden, die sich sehr gut als Hochgeschwindigkeitsdatenquellen eignen. Eine als erste Ausführung zur Realisierung von Hochgeschwindigkeitsdatenquellen einsetzbare 2:1 Selektor-Schaltung zeichnet sich durch einen einwandfreien Betrieb bei Datenraten von bis zu 105 Gbit/s aus. Der jeweilige Ausgangsspannungshub an den zwei komplementären Datenausgängen beträgt 600 mV_{pp}. Ein äußerst verlustarmer Betrieb wird bei Datenraten von bis zu 90 Gbit/s erreicht.

Als zweite Ausführung zur Realisierung von Hochgeschwindigkeitsdatenquellen ist eine vollständige 2:1 Multiplexer-Schaltung entwickelt worden. Diese Multiplexer-Schaltung zeichnet sich durch einen einwandfreien Betrieb bei Datenraten von bis zu 80 Gbit/s aus. Ein Ausgangsspannungshub von 600 mV_{pp} wird an jedem komplementären Datenausgang erzielt.

Zusammenfassend leisten die ausgezeichneten und teilweise Rekord-Ergebnisse dieser Arbeit einen wesentlichen Beitrag zur Entwicklung von zukünftigen 80 Gbit/s optischen Telekommunikationsnetzen.

Chapter 1

Introduction

The establishment of the information and telecommunication (IT) technologies in our society illustrates one of the most impressive success story observed over the past decade. IT technologies such as internet or mobile communication find broad approval especially in the professional world, where these technologies are used for maintaining or improving the working processes. Furthermore, more and more private users and households take advantage of the possibilities of the IT technologies for managing their daily life activities as well as for entertainment purposes. Current trends predict the continuing growth of the amount of IT end-users as well as the emergence of novel IT services requiring higher transmission bandwidth. These development tendencies set new requirements on the data transport networks regarding the transport capacity as well as the associated cost efficiency.

Transport network standards such as Ethernet or SDH/SONET [1] have been introduced in order to account for the steadily rising demand for new IT services as well as higher user-end bandwidth. These standards are optical access networks, thereby relying on the low-cost electrical time domain multiplexing (ETDM) data transmission technique. Figure 1.1 illustrates the block diagram of an ETDM optical link, showing the corresponding electronic, optoelectronic, and optical components.

10 Gbit/s Ethernet standard activity was completed before the end of 2002, thus allowing the commercial deployment of the corresponding transmission systems for the broadband local area network (LAN) and metro network applications. For telecommunication applications, a well-established standard for 10 Gbit/s optical link has also been defined by SDH STM-64 or SONET OC-192 and is now in a large commercial market. Telecommunication equipment for higher data rate standards at 40 Gbit/s (SDH STM-256 or SONET OC-768) is currently being commercialized.

[1] SDH (Synchronous Digital Hierarchy) is the European standard published by the International Telecommunication Union (ITU). SONET (Synchronous Optical NETwork) is the United States version of the standards published by the American National Standard Institute (ANSI).

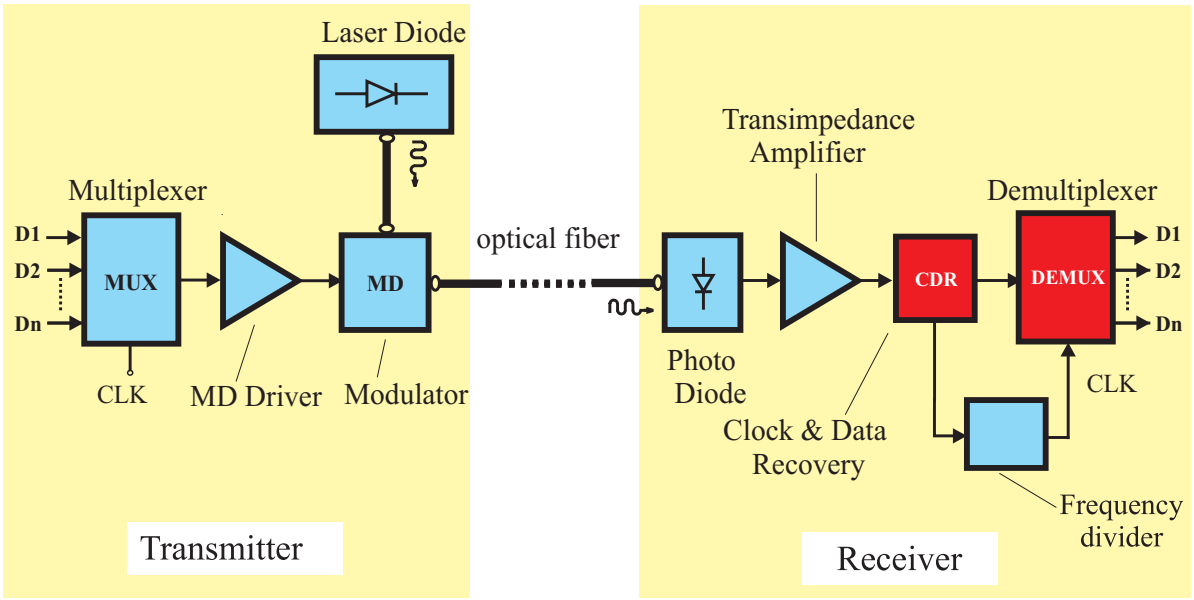


Figure 1.1: Optical data link based on the electrical time domain multiplexing (ETDM) transmission technique.

1.1 Motivation

At the beginning of this work in the year 2002, the feasibility of 40 Gbit/s electronic components for use in ETDM-based transport networks was largely demonstrated in laboratory environments. Development efforts were then concentrated on making these electronic components mature for commercial deployment, regarding the market demand for low-cost integrated solutions ([8], [13], [29], [53]). In order to prepare the post 40 Gbit/s transmission systems, research activities, at that time, were launched for developing electronic components targeting next generation 80 Gbit/s ETDM-based optical link. Furthermore, research achievements for telecommunication networks at this data rate would build an important knowledge basis for the development of future Ethernet data networks featuring an operating speed of 100 Gbit/s.

Following the aforementioned development trend, the Fraunhofer IAF started in 2002 a project aiming the realization of electronic components included in the transmitter and receiver part of 80 Gbit/s ETDM-based serial links. The project comprised the complete development of an InP double heterojunction bipolar transistor (DHBT) technology, on the basis of which the electronic circuits were designed and realized. A fundament for the successful carrying out of this undertaking was the long standing and established experience of the Fraunhofer IAF in terms of high-speed electronic components for optical communication ([34], [35], [77]). As a matter of fact, Figure 1.2 shows the 40 Gbit/s electronic components which have been developed and manufactured at Fraunhofer IAF by the year 2002.

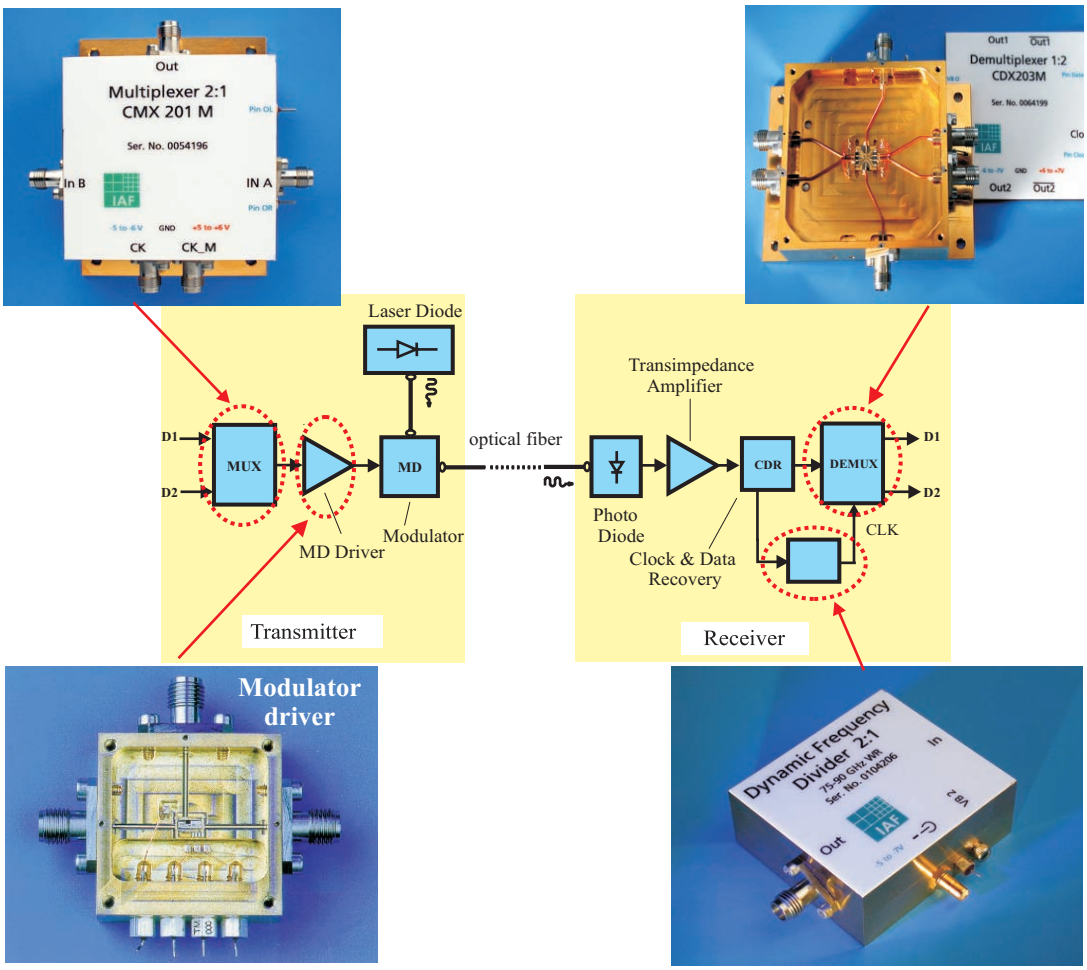


Figure 1.2: Critical electronic components of a 40 Gbit/s ETDM-based optical data link. These components are developed and packaged into module at Fraunhofer IAF.

The underlying InP-DHBT technology is a very good candidate for implementing high-performance mixed-signal circuits at the aimed high-speed application. In fact, InP-based DHBTs offer very high operation frequencies combined with high breakdown voltage, low offset voltage, high current gain, as well as low 1/f noise performance. The unique combination of these properties make the superiority of the InP-DHBT technology regarding the competing high-speed technologies (e.g.: SiGe HBT, GaAs HBT, InP HEMT).

The scope of this thesis is the successful development and realization of monolithically integrated clock and data recovery (CDR) circuits including an 1:2 demultiplexer (DEMUX) circuit. These circuits are intended for deployment in ultra-high-speed optical data links, especially in next generation ETDM-based 80 Gbit/s telecommunication networks. The reasons motivating the choice of the CDR circuit as working theme are addressed in the following:

- The CDR circuit is a key component regarding data processing in the receiver part

of ETDM transmission link.

- The CDR circuit includes several circuit functions (e.g.: data retiming, clock recovery, and data demultiplexing) on a single chip, thus making it one of the most challenging components among the electronic circuit components included in an optical link.
- The fully integrated CDR circuit allows to validate the ability of the developed technology for performing medium scale integration of complex mixed-signal circuits.
- A monolithically integrated CDR circuit targeting 80 Gbit/s operation speed was not yet demonstrated at the beginning of this work.

1.2 State-of-the-art

Table 1.1 shows state-of-the-art works on CDR circuits at the beginning of the thesis (in the year 2002) as well as within the period accompanying this thesis. According to this table, CDR circuits have been demonstrated at data rates up to 43 Gbit/s not only by using the high-speed technologies SiGe HBT and InP HBT/HEMT, but also by using the "slower" technologies Si BJT and CMOS. Regarding the single function of clock extraction, a clock recovery circuit implementing this function has been reported in [72], showing an operation speed of 56 Gbit/s.

Most of the CDR circuits presented in the different publications extracts a clock signal with a frequency corresponding to the full rate or half the rate of the input data. A smaller ratio between the CDR input data and the extracted clock signal has been also demonstrated in [37].

Earlier CDR works presented in Table 1.1 feature a hybrid integration of the CDR main circuit components ([20], [84]). However, the obvious trend consists in the monolithic integration of all CDR components, thereby implementing the data demultiplexing function at the same time. The amount of active devices included in the different CDR circuits reveals the challenge of performing medium or large scale integration for a successful realization of these circuits.

1.3 Organization

The development steps illustrating the course of this thesis are presented in this section. As already mentioned, the final intention is the successful realization of up to 80 Gbit/s monolithically integrated CDR circuits with 1:2 DEMUX, thereby using an InP-DHBT technology.

As an introduction to the working theme, **Chapter 2** addresses the theory of clock and data recovery in the context of ETDM-based optical data link. Among the competing CDR concepts, a PLL-type CDR architecture including a (digital) half-rate linear phase detector is chosen on the basis of defined selection criteria for high-performance CDR.

Reference	Data Rate [Gbit/s]	Clock frequency [GHz]	Technology	f_T/f_{max} [GHz]	Transistor Count	Remarks
[20] ('96)	10	5	Si BJT	16/-	> 200	Hybrid CDR with 1:4 DEMUX
[84] ('99)	40	20	Si BJT	50/-	≈ 100	Hybrid CDR with 1:2 DEMUX
[15] ('00)	10	10	SiGe BiCMOS	n.a.	n.a.	Monolithically integrated CDR
[68] ('01)	10	5	CMOS	n.a.	n.a.	Fully integrated CDR with 1:2 DEMUX
[54] ('01)	43	43	InP HEMT	173/-	370	Monolithically integrated CDR
[64] ('01)	40	20	SiGe HBT	72/74	> 200	Fully integrated CDR with 1:4 DEMUX
[72] ('01)	56	56	InP HBT	130/220	100	Clock recovery circuit
[25] ('02)	10	10	InP HBT	98/160	460	Fully integrated CDR with 1:4 DEMUX
[56] ('02)	40	40	InP HBT	140/200	> 500	Monolithically integrated CDR
[29] ('03)	40	20	InP HBT	140/160	n.a.	Fully integrated CDR with 1:4 DEMUX
[55] ('03)	43.2	21.6	InP HBT	150/170	2200	Fully integrated CDR with 1:4 DEMUX
[37] ('03)	40	10	CMOS	n.a.	n.a.	Quarter-rate CDR with 1:4 DEMUX
[50] ('03)	43	21.5	SiGe BiCMOS	120/100	n.a.	Fully integrated CDR with 1:4 DEMUX

Table 1.1: State-of-the-art works on clock and data recovery circuits. The indicated data rate corresponds to the data speed at the CDR input. The clock frequency is the frequency of the extracted clock signal by the CDR circuit. The transistor count is assumed from references and estimations in [73].

System level considerations of the CDR circuit are performed to derive figures of merit, which serve as guidelines during the circuit design.

The design of the CDR circuit is mainly performed on a transistor level. Therefore, in-depth knowledge regarding the basic device and its underlying technology is necessary for achieving high-performance CDR circuits. Thus, **Chapter 3** introduces the InP-DHBT technology providing the devices used in each CDR circuit components. The basic epitaxial and technological aspects as well as the achieved dc and high-frequency performance by

the processed DHBTs are discussed. The transistor models involved in the circuit design are also presented.

A separate consideration of the CDR main circuit components is performed, thus allowing to gain deep understanding of the corresponding operation mechanisms. In this way, the maximum performance by these components can be achieved, consequently resulting in high-performance CDR circuits. Thus, **Chapter 4** deals with the design and realization of voltage controlled oscillators (VCOs), which are suitable for over 80 Gbit/s applications. The applied negative resistance LC VCO concept is introduced. Design considerations for achieving very low phase noise performance are addressed. The measurement technique for characterizing the realized VCOs at such high operation frequencies is discussed.

Chapter 5 deals with the design and realization of a half-rate linear phase detector, as a further main component of the CDR circuit. The design of each circuit block forming the phase detector is explicitly addressed, thereby following afore defined design considerations for achieving at least 80 Gbit/s operation speed. The design of the low-pass filter is performed in this chapter, since it allows a better understanding of the phase detector operation. As in Chapter 4, the measurement technique for characterizing the high-speed phase detector is described.

Based on the developments of the CDR main components, as described in Chapter 4 and Chapter 5, **Chapter 6** addresses the design and realization of fully integrated CDR circuits operating up to 80 Gbit/s. The design of the circuit interfaces for connecting the CDR components is discussed.

The successful characterization of the aimed high-speed CDR circuits requires the availability of a data source at such high operation speed. Multiplexing components are essential in the generation of such high-speed data. In this regard, **Chapter 7** addresses the design and realization of multiplexing components capable of delivering over 80 Gbit/s data. The 2:1 selector and the 2:1 full multiplexer, as two versions realizing the multiplexing components, are introduced. The corresponding design aspects are extensively discussed.

Chapter 8 resumes the achieved results throughout the work. Furthermore, an outlook discusses measures intending further improvements of the realized CDR circuit, regarding upcoming development challenges.

Chapter 2

Introduction to Clock and Data Recovery

In optical fiber link, the processing of the data underlies synchronous operation. However, the processed data in the transmitter part of the link are transferred to the receiver without timing information. As a consequence, the received data are asynchronous. Moreover, these data are severely distorted by dispersion, damping and noise encountered during the transmission over the link. Thus, for a proper synchronous data processing in the receiver part, the synchronization (or clock) signal must be generated in the latter receiver. Furthermore, the distorted data during the transport have to be reshaped or recovered. These tasks are referred to as clock and data recovery (CDR) and performed by a CDR circuit.

This chapter deals with the theory of clock and data recovery. Beginning with the basic principle of CDR, the (popular) competing concepts for realizing CDR circuits are then presented. Weighing up the advantages and disadvantages of these concepts, a CDR concept for realization in this work is selected in the third part of the chapter. Subsequently, the selected CDR concept is briefly considered on a system level. The fourth part of the chapter deals with figures of merit which will accompany the CDR implementation in the following chapters. Finally, the chapter is closed by a summary.

2.1 Principle of Clock and Data Recovery

2.1.1 General Description

The operation principle of a CDR circuit is illustrated in Figure 2.1. Thus, the received noisy data are simultaneously transferred to a data recovery (DR) and to a clock recovery (CR) circuit. The clock recovery circuit senses the incoming data and generates a periodic clock signal. The latter clock signal is used by the data recovery circuit for retiming the incoming data. Moreover, the clock signal extracted from the incoming data can also be used in the receiver part of the link for further synchronous data processing, e.g., data

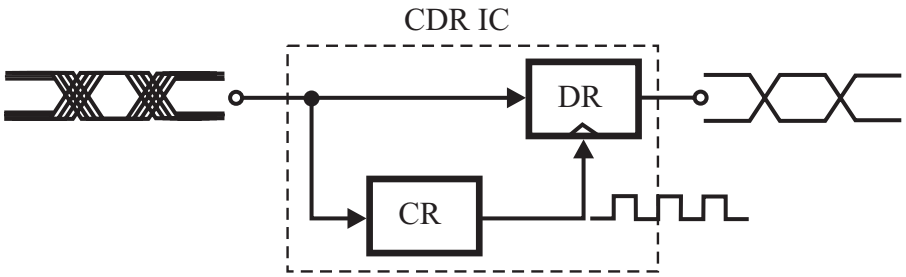


Figure 2.1: Operation principle of the CDR circuit. DR denotes the data recovery circuit while CR is the clock recovery circuit.

demultiplexing.

In general, the data recovery is performed using a digital circuit, e.g., decision circuit or D-flipflop (D-FF). Within this D-FF, the extracted clock signal samples the incoming data, thus resulting in the recovered data at the D-FF output. For a proper data recovery, three important conditions must be satisfied by the clock signal:

- The clock signal frequency must be consistent with the input data rate. As an example, an input data rate of 80 Gbit/s results in an 80 GHz clock signal for a full-rate CDR. For a half-rate CDR, the aforementioned data rate translates to a clock frequency of 40 GHz.
- A certain phase relationship must exist between data and clock signal for optimum data sampling. In general, an optimum data sensing is achieved by sampling the data in the middle of the bit (see Figure 2.2).
- The regenerated clock signal must feature low jitter performance, thus allowing to minimize the jitter of the regenerated data.

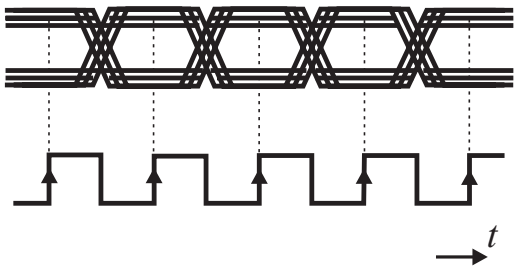


Figure 2.2: Optimum data sampling by the extracted clock signal.

2.1.2 Basic Problem of Clock Recovery

The transmitted data through the optical link are of random nature, as is generally known. Usually, these data are coded in the so-called Non-Return to Zero (NRZ) format. This data format is especially well-suited for high-speed communication systems, unlike its Return to Zero (RZ) counterpart [60]. However, an extraction of the clock signal directly from the NRZ data is impossible. This is explained by considering the power spectrum S_{xNRZ} of NRZ data. Namely, this power spectrum is described by the following equation [60]:

$$S_{xNRZ}(f) = T_B \left[\frac{sin(\pi f T_B)}{\pi f T_B} \right]^2 \tag{2.1}$$

where T_B represents the bit width of the data. The corresponding variation of S_{xNRZ} as a function of frequency is shown in Figure 2.3. Thus, the spectrum exhibits no power line at the frequency equal to the bit rate. That is, no direct information is provided for clock extraction. In other words, the clock recovery circuit needs special measures in order to extract the clock signal from the incoming NRZ data.

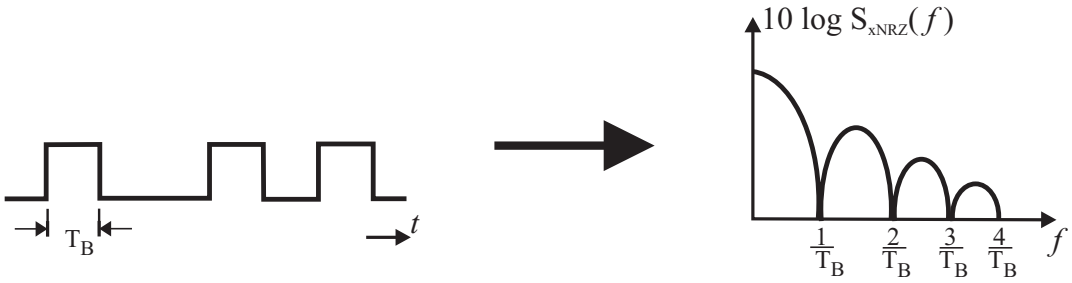


Figure 2.3: Bit sequence of NRZ data and the corresponding spectrum.

2.1.3 Solution for Clock Recovery

From the previous section, it becomes obvious that a preprocessing of the NRZ data is necessary for a possible extraction of the clock signal. Therefore, a nonlinear operation has to be performed on the NRZ data, thus inducing a power line at the frequency corresponding to the data rate. This nonlinear operation is referred to as the edge detection method. The proceeding using this method is depicted in Figure 2.4. First, the NRZ data are differentiated with respect to time, thus creating positive and negative pulses at each edge of the data waveform. Second, the differentiated data are rectified, thus generating only positive pulses at each edge of the data waveform. The resulting spectrum exhibits a power line at the frequency corresponding to the bit rate. This frequency component can be extracted using a narrow-band filter, thus resulting in an almost sinusoidal signal with the frequency corresponding to the data rate.

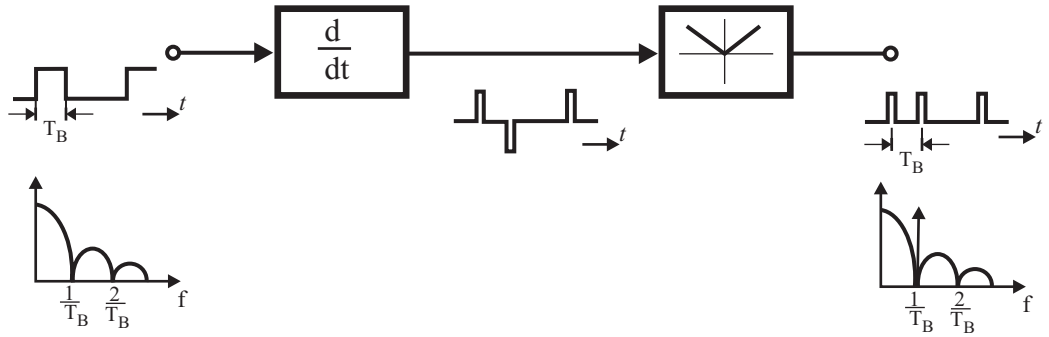


Figure 2.4: Edge detection method aiming the generation of a power line at a frequency corresponding to the data rate of NRZ data.

Using the edge detection method, a CDR circuit according to the block diagram of Figure 2.5 can be realized. The phase shifter in the clock feeding path of the data recovery circuit is used to guarantee an optimum phase setting of the clock with respect to the incoming data. Thus, the bit error rate (BER) during data recovery is minimized.

2.2 Concepts for Clock and Data Recovery Circuits

In all CDR circuits known from the literature, the data recovery (DR) is performed on the basis of digital data processing, as already mentioned. Decision circuits such as D-FF are used for performing this task. However, the concepts for implementing CDR circuits differ in the proceeding for clock recovery (CR). Thus, one may differentiate between the analog clock recovery concept and the digital clock recovery concept. These concepts are

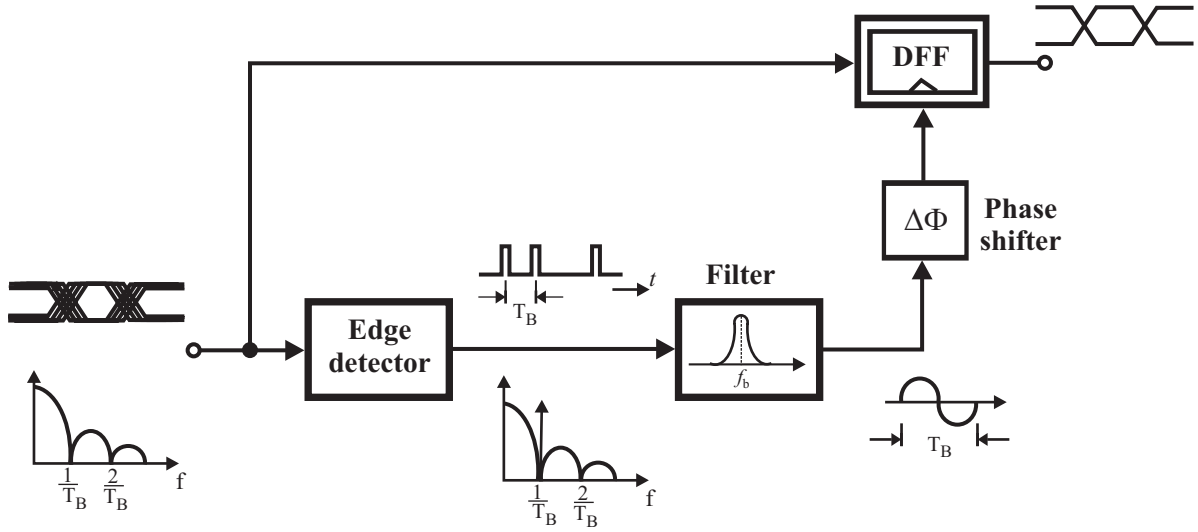


Figure 2.5: General block diagram of a clock and data recovery circuit.

discussed in this section, considering them in the context of a whole CDR circuit.

2.2.1 Concepts for Analog Clock Recovery

The system architecture for CDR circuits performing analog CR is fully conform with the block diagram illustrated in Figure 2.5. The edge detector is realized using analog circuit design technique. That is, the differentiation of the incoming data is achieved using high-pass filtering, while the rectification is performed by a squaring device such as a four-quadrant multiplier. A compact realization of the differentiator with the rectifier is achieved using a Gilbert Cell-type circuit configuration, but with capacitive degeneration added in the lower differential amplifier [60]. For the extraction of the power line at the frequency f_b ($f_b = \frac{1}{T_b}$) corresponding to the data rate, a narrow-band filter with high Q is needed. In fact, a high Q allows to maintain the clock signal available, even if the incoming data stream includes (relatively) long sequences of identical bits. Different options for implementing high-Q filter are known from the literature:

- **Passive filter** [85]: Surface acoustic wave (SAW) filter or dielectric resonator represent this type of filter. They feature very high Q values (e.g.: > 800). However, they are suited for relatively low data rates. Furthermore, a monolithic integration within the CDR circuit is impossible, since the high Q value can not be achieved with passive components in integrated circuit technologies.

- **Regenerative frequency divider**: It operates at half the frequency f_b. This frequency divider type includes a resonator, which has to feature high Q values. In this way, the effective Q of the frequency divider is correspondingly high. Hence, external resonator components with high Q are used, as shown in [52]. Regenerative frequency divider with integrated LC resonator are also presented in [81].

- **Injection locked VCO** [82]: This type of VCO can be considered as a narrow-band filter at the VCO center frequency. A high effective Q can be achieved without using high-Q passive components within the VCO resonator [58]. Thus, a monolithic integration of the CDR circuit including a high-Q filter is possible.

- **Phase-locked loop (PLL)** [73]: As for the injection locked VCO, the PLL can be regarded as a narrow-band filter at the center frequency of the included VCO. Furthermore, an on-chip implementation of this PLL-type filter at high effective Q can be obtained without using high-Q passive components. Unlike the aforementioned filter types, the properties of the filter realized by the PLL are adjustable by varying the value of the PLL system parameters. Thus, these filter properties can be adapted to system standards during the characterization of the CDR.

Figure 2.6 illustrates the block diagram of a CDR including a PLL as narrow-band filter, as an example. The PLL is composed of an analog phase detector (PD) [73], a low-pass filter (LPF), and a VCO, as is generally known. In the case of phase misalignment

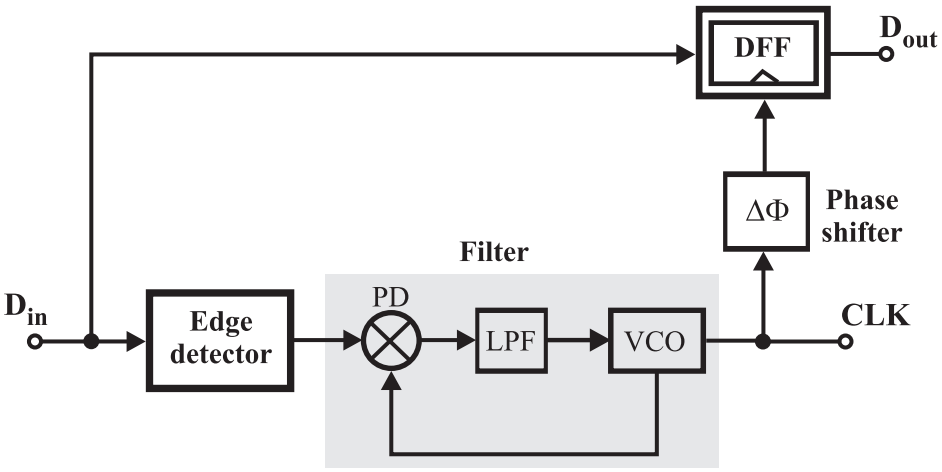


Figure 2.6: CDR circuit including a PLL as narrow-band filter.

between the preprocessed NRZ data and the frequency signal generated by the VCO, the PD generates an output signal which carries information about this phase misalignment or (in other terms) about the resulting phase difference. The latter PD output signal is low-pass filtered by LPF, thereby extracting a dc voltage signal. This voltage signal is then fed to the frequency tuning input of the VCO. Thus, an iterative adjustment of the VCO operation frequency is performed by the loop until the phase of the frequency signal features an optimum alignment with respect to the PD input signal. This phase alignment operation assumes that the VCO center frequency is close to f_b. The basic theory of PLL operation is extensively addressed in [10], [59], [60], and [61].

The PLL in Figure 2.6 optimally aligns the phase of the extracted clock signal with the preprocessed NRZ data. However, since the edge detector induces an unknown phase delay between the incoming and the preprocessed data, the frequency signal generated by the VCO shows a static phase error regarding these incoming NRZ data. That is, the data at the CDR input are not optimally aligned with the frequency signal. Hence, an adjustable phase shifter in the clock feeding path of the decision circuit is inevitable for aligning the phase of the extracted clock signal with respect to the incoming NRZ data. In this way, an optimum sampling of the NRZ data in the D-FF can be achieved.

2.2.2 Concepts for Digital Clock Recovery

Figure 2.7 illustrates the general block diagram of a CDR including a CR on the basis of digital data processing. In this context, the proceeding for clock recovery underlies the PLL-system topology, as for the analog CR including a PLL as filter. According to Figure 2.7, the CDR is composed of a digital phase detector (PD), a low-pass filter or loop filter (LPF), and a VCO. A preprocessing stage for the NRZ data is not needed in this case since the function of edge detection is performed within the PD. The system operation of the digital CR is similar to that of the analog CR including a PLL as filter. Actually, the

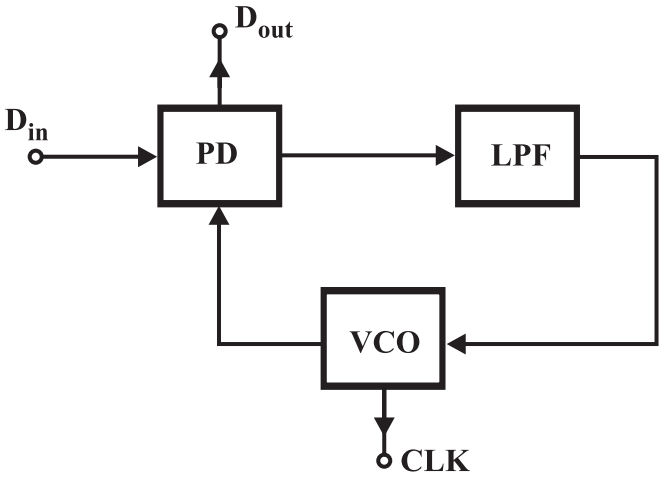


Figure 2.7: Block diagram of a CDR circuit including a CR on the basis of digital data processing.

difference between either CR types consists in the implementation technique used for the edge detector and the PD.

The data recovery in the block diagram of Figure 2.7 is inherently performed within the PD. Different concepts addressing the implementation of digital phase detectors are known from the literature. These concepts feature, on the one hand, phase detectors capable of operating at half the frequency f_b corresponding to the data rate (e.g.: [8], [68], and [84]). On the other hand, PD concepts are presented in the literature, which feature an operation at the full frequency f_b (e.g.: [11], [19], [22], and [38]). In the case of the PD operation at $\frac{f_b}{2}$, the corresponding concept is referred to as half-rate phase detector and the whole CDR circuit correspondingly half-rate CDR. For the PD operating at f_b, the corresponding concept is called full-rate phase detector and the whole CDR circuit full-rate CDR. Both phase detector types may feature either a linear output characteristic [68] or a binary (bang-bang) one [84].

The PD with linear output characteristic, also called linear PD, generates an output voltage signal, the mean value of which is linearly proportional to the phase difference between input data and clock signal. Figure 2.8(a) illustrates the transfer characteristic of a linear PD. Regarding the PD with a binary output characteristic, also called bang-bang PD, the PD output signal features two voltage levels, depending on whether the phase of the input data leads or lags that of the clock signal. Figure 2.8(b) illustrates the transfer characteristic of a bang-bang PD.

2.3 Choice of a CDR Concept

In this work, an essential criterion for the selection of a CDR concept is the possibility of a monolithic integration of the whole CDR circuit. Regarding the CDR concepts including an analog clock recovery, the options with PLL and injection locked VCO as filter satisfy the aforementioned essential criterion. However, the PLL-type filter is more suited for

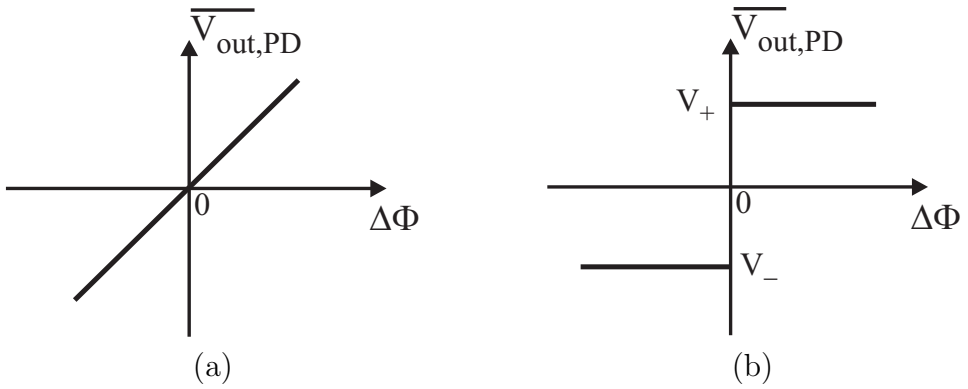


Figure 2.8: Transfer characteristic of (a) linear phase detector, (b) bang-bang phase detector.

field applications due to the adjustable filter characteristics. Regarding the CDR concepts including digital clock recovery, all discussed concept options offer the possibility of monolithic integration. Thus, the CDR concepts with full-rate as well as half-rate phase detector, thereby featuring either a linear or a bang-bang transfer characteristic, are considered.

For an effective selection of a suitable CDR concept, the advantages and disadvantages of the discussed CDR concepts including analog and digital CR are listed. Thus, the CDR including a CR topology according to Figure 2.6 features the following advantages (+) and disadvantages (-) [73]:

+ Relatively low jitter performance is achieved since the included PLL-type filter features a narrow bandwidth.

+ The static and dynamic characteristics of the CDR circuit are influenceable through the parameters of the PLL-type filter. Thus, these characteristics can be adjusted for conforming with system standards, independently of the circuit technology.

+ The clock recovery circuit features a relatively low device count, thus having a positive impact on the power dissipation as well as the probability of successful technological circuit processing.

- The proceeding of data recovery is separated from the clock recovery, thus resulting in an additional decision circuit for performing the former (DR) task.

- For field applications, the phase shifter (in the clock feeding path of the decision circuit) has to automatically align the phase of the extracted clock signal with the input NRZ data. This results in the use of an additional PLL at this place, thus leading to a much higher circuit complexity.

The CDR concept including a CR topology according to Figure 2.7 features the following advantages and disadvantages:

+ The edge detector merges with the phase detector. As a consequence, the clock signal extracted by the PLL loop is inherently phase aligned with the input data. Thus, unlike the CDR including an analog CR, the phase shifter in the clock feeding path of the decision circuit is dispensable.

+ The data recovery is inherently performed within the phase detector. This minimizes possible phase misalignment between input data and extracted clock signal within the decision circuit [60].

+ The VCO included in the PLL loop can be operated at half the bit rate, thus relaxing the requirements on the VCO performance (e.g.: oscillation frequency, phase noise).

+ Relatively low jitter performance is achieved since the included PLL-type filter features a narrow bandwidth.

+ The static and dynamic characteristics of the CDR circuit are influenceable through the PLL filter parameters.

- The CDR based on a bang-bang phase detector features a comparable higher jitter due to the nonlinear transfer characteristic [56].

- The CDR including a half-rate bang-bang phase detector sets higher requirements on the circuit and layout design. Namely, a quadrature clock signal is needed for a proper operation of the latter phase detector [84].

- CDR circuits in half-rate architecture are very sensitive to clock duty cycle distortion, since both edges of the half-rate clock are used to sample the data. This results in more stringent requirements in the signal quality delivered by the VCO.

- The circuit complexity is relatively high, especially for a CDR including a bang-bang phase detector (complexity beyond 200 active devices).

The listed advantages and disadvantages of the discussed CDR concepts reveal that CDR circuits including digital CR feature a considerable edge over their counterpart including analog CR. This is especially obvious by considering the phase alignment of the extracted clock signal with respect to the input data. As a result, the CDR concept including digital CR is more adequate and robust for field applications. Otherwise, both CDR concepts present the same advantages, regarding the performance of the included PLL-type filter for clock recovery. Therefore, CDR circuits including digital PD are selected for further consideration in this work.

Considering the different digital phase detector types, the linear PD is preferred to its bang-bang counterpart. In fact, the main disadvantages of the CDR including digital CR arise from the characteristics of the bang-bang PD, as listed before. The linear PD is chosen to operate in a half-rate mode, thus easing the circuit and layout design requirements, especially in the speed range of interest.

The discussed CDR concepts actually lock the phase of the VCO output signal to the input NRZ data. For some field applications, an additional circuit is used for automatically tuning the VCO frequency to the frequency $\frac{f_b}{2}$ (or f_b for full-rate operation mode), assuming a considerable deviation of the VCO frequency from $\frac{f_b}{2}$. This additional circuit is also referred to as frequency-locked loop (FLL). However, this FLL is not considered in the development of the CDR in this work. Namely, the FLL considerably increases the complexity of the circuit (e.g.: > 300 active devices). As a consequence, the successful processing of the implemented circuit might be seriously compromised. As shown in Chapter 5, a measure providing manual frequency tuning is intended in the CDR circuit, thus allowing to counteract the case of a strong deviation of the VCO center frequency from $\frac{f_b}{2}$.

2.4 System Level Considerations

The circuit components included in the CDR configuration according to Figure 2.7 are resumed in a feedback system, thereby forming the already mentioned phase-locked loop. Investigations regarding the dynamic behavior of this loop require the consideration of the CDR in a system level, which is independent of the used circuit technology. In this section, the system level consideration of the CDR is essentially limited to the system parameters necessary for ensuring a stable operation of the feedback system. On the basis of this stable feedback system, the design of the individual CDR components and then the design of the whole CDR on circuit or device level can be attempted. These design tasks on circuit level actually constitute the main focus of this work.

2.4.1 Linear Model of the CDR Loop

The development of a linear model characterizing a PLL-type CDR is a prerequisite for quantifying the dynamic behavior of the corresponding feedback system. This linear model is only valid for the CDR loop locking to the input data. Figure 2.9 illustrates the considered linear model of the CDR loop. In this figure, the input and output variable of the system are represented by the phase of the input data φ_i and that of the extracted clock signal φ_o, respectively. Thus, the selected linear PD is modeled by a subtractor whose output is amplified by the PD gain K_{PD}. The output voltage of the PD is consequently given by the following equation:

$$V_{PD}(s) = K_{PD}\,\varphi_e(s) = K_{PD}\,(\varphi_i(s) - \varphi_o(s)) \tag{2.2}$$

The low-pass filter LPF is represented in Figure 2.9 by the corresponding transfer function H_{LPF}. Actually, LPF can be implemented either as active or as passive filter. The former filter generally includes an amplifier featuring high gain, from which the dynamic properties of the CDR loop benefit. However, the implementation of the passive filter is quite simple and its performance is often satisfactory for most applications of the CDR

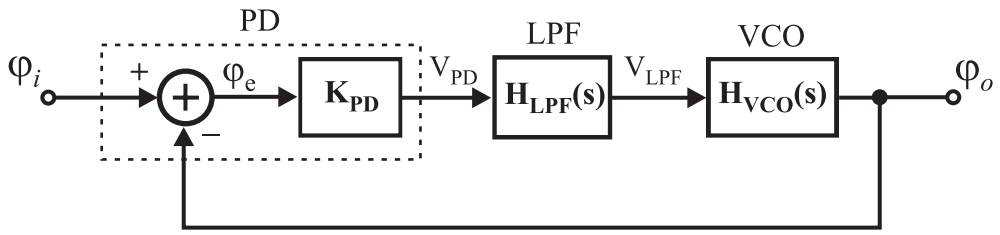


Figure 2.9: Linear model of the CDR loop.

loop ([9], [10]). Thus, the passive filter is considered for use in the CDR loop. The corresponding transfer function is given by the relation:

$$H_{LPF}(s) = \frac{1 + s\tau_2}{1 + s\tau_1},\ \tau_2 < \tau_1 \tag{2.3}$$

Thus, the output voltage V_{PD} is low-pass filtered by LPF and the resulting voltage signal V_{LPF} is defined as follows:

$$V_{LPF}(s) = H_{LPF}(s)\, V_{PD}(s) \tag{2.4}$$

The VCO is represented in Figure 2.9 by the corresponding transfer function H_{VCO}. In the frequency domain, the VCO behaves as a perfect integrator regarding the input voltage signal V_{LPF} and the output phase signal φ_o. Thus, the transfer function H_{VCO} is defined as:

$$H_{VCO}(s) = \frac{\varphi_o(s)}{V_{LPF}(s)} = \frac{K_{VCO}}{s} \tag{2.5}$$

where K_{VCO} represents the gain of the VCO. Actually, V_{LPF} represents the tuning voltage at the corresponding input of the VCO.

Before addressing the closed loop transfer function, the following system parameters are defined:

$$\omega_n = \sqrt{\frac{K}{\tau_1}} \tag{2.6}$$

and

$$\zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{K}\right) \tag{2.7}$$

In equation (2.6), ω_n is referred to as the natural frequency of the loop. K denotes the dc loop gain and is defined as follows:

$$K = 2\pi K_{PD} K_{VCO} \tag{2.8}$$

In equation (2.7), ζ is referred to as the damping factor of the loop.

By considering the system parameters ω_n and ζ and assuming that $K >> \omega_n$, which is the case for PLL-type CDR with relatively narrow bandwidth, the closed loop transfer function H is described by the following equation:

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.9}$$

Equation (2.9) shows that the transfer function $H(s)$ is influenceable using the loop system parameters ζ and ω_n. Generally, the loop is stable for a ζ value of at least 0.7 [10]. As shown by equation (2.7), the damping factor can be adjusted by the loop filter parameter τ_2, thereby considering ω_n as a constant and the dc loop gain as very high.

2.4.2 Static and Dynamic Loop Properties

Using the linear model of the CDR as well as the resulting system parameters, the investigation and optimization of static and dynamic properties of the corresponding loop can be performed [10]. The latter properties, which are considered during the CDR development, are defined in the following:

Static Phase Error: It depicts the phase error $\Delta\varphi_s$, which results from a frequency mismatch $\Delta\omega$ between the input data and the free running VCO. This phase error is defined as follows:

$$\Delta\varphi_s = \frac{\Delta\omega}{K \cdot H_{LPF}(0)} = \frac{\Delta\omega}{K} \tag{2.10}$$

The target is the minimization of $\Delta\varphi_s$, thus ensuring an optimum sampling of the data by the extracted clock signal. Therefore, a high dc loop gain proves to have a positive impact regarding a minimum $\Delta\varphi_s$.

Tracking range: It denotes the frequency range $\Delta\omega_T$, across which a locked CDR loop can track data rate variations at the CDR input. The tracking range features the following proportionality:

$$\Delta\omega_T \propto K \tag{2.11}$$

As for the static phase error, a high dc loop gain has a positive impact on the tracking range.

2.5 CDR Figures of Merit

The performance expected from the electronic components included in optical links is usually defined in form of standards recommended by the *International Telecommunication Union* (ITU). In Europe, the standard for ETDM systems is called *Synchronous*

Transfer Mode (STM) in the *Synchronous Digital Hierarchy* (SDH). However, no standard is defined so far for 80 Gbit/s ETDM systems, not to mention for 80 Gbit/s CDR circuits. Therefore, the performance expected from these CDR circuits, especially regarding the clock recovery processing, is extrapolated from already defined standards at lower data rates, e.g., 40 Gbit/s (STM-256), 10 Gbit/s (STM-64). Figures of merit with respect to data processing are based on typical requirements of circuits following the CDR in the receiver part of optical links.

High Operation Speed

The decision circuit within the phase detector must be able to process or retime the incoming high-speed NRZ data. For 80 Gbit/s systems, the data rate is actually set to 86 Gbit/s. The 7.5% bit overhead is dedicated to the so-called forward-error correction (FEC). This FEC is used for detecting and correcting data bits corrupted by transmission errors. However, due to in-house (laboratory) limitations regarding the generation of >80 Gbit/s data for circuit characterization, the aimed operation speed of the CDR circuit is fixed to maximum 80 Gbit/s.

Output Voltage Swing

The regenerated data by the decision circuit within the phase detector must feature a voltage swing which is able to drive the circuits following the CDR, e.g., demultiplexer. With an output swing of at least 300 mV, the CDR circuits will be able to drive circuits underlying the known high-speed technologies (HBT, HEMT).

Jitter Generation

Jitter generation refers to the clock signal jitter produced by the CDR circuit itself when the input NRZ data contains no jitter. Recalling the general definition of jitter, it represents the deviation of the zero crossings of the clock signal from their ideal points on the time axis (see Figure 2.10(a)). For noise as a source of jitter, the time differences in Figure 2.10(a) are often plotted as a histogram, as shown in Figure 2.10(b). This histogram features a maximum value at $\Delta t_j = 0$, representing the ideal zero crossing time. Furthermore, a standard deviation σ_T denoting the root mean square (rms) value of timing jitter can be read from this histogram. Under the assumption of a Gaussian distribution of the jitter, the peak-to-peak timing jitter σ_x is related to the rms counterpart as $\sigma_x \approx 6\sigma_T$ [73].

The values characterizing the jitter generation are defined according to the so-called Type-A group in STM standards. These values are often expressed in terms of the bit period, also called the unit interval (UI). Thus, the jitter of the clock signal should feature a value σ_T not exceeding 0.05 UI_{rms}. This results in an absolute value of 0.625 ps_{rms}. The corresponding maximum peak-to-peak jitter amounts to 0.3 UI_{pp}, resulting in an absolute value of 3.75 ps_{pp}.

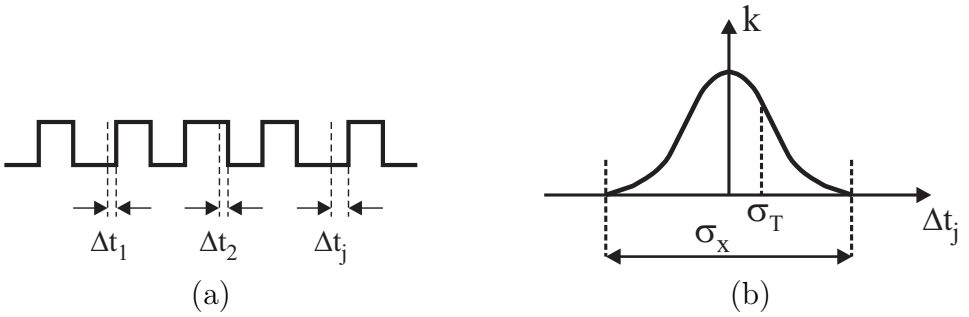


Figure 2.10: (a) Definition of time jitter. (b) Histogram of noise as jitter.

VCO Phase Noise

The VCO phase noise represents the main noise contributor resulting in jitter generation at the clock output of the CDR circuit. Therefore, a minimization of the latter phase noise is crucial and this task is particularly addressed in Chapter 4. The maximum allowable phase noise can be derived from the rms jitter defined in the previous paragraph. In [60], the following equation is used for relating both quantities:

$$\sigma_T \approx \frac{1}{\sqrt{2\pi f_u}} \sqrt{\pounds(f_m)} \, \frac{f_m}{f_0} \tag{2.12}$$

where f_u represents the 3dB bandwidth of $H(s)$ in equation (2.9), $\pounds(f_m)$ is the VCO phase noise at an offset frequency f_m, and f_0 is the operation frequency of the VCO. Based on the specifications for the standard STM-256, the extrapolated loop bandwidth for an 80 Gbit/s system amounts to 64 MHz. Since the selected phase detector operates at half the bit rate, f_0 amounts to 40 GHz. Thus, the maximum allowable VCO phase noise amounts to -66 dBc/Hz at 1 MHz frequency offset.

2.6 Summary

In this chapter, the basic theory of clock and data recovery with respect to NRZ data has been introduced. Different CDR concepts known from the literature have been discussed, thereby showing the advantages and disadvantages of each concept. Aiming at the realization of a monolithically integrated CDR circuit, a CDR architecture including a PLL as narrow-band filter has been chosen as the basic topology. The phase detector included in the PLL-type CDR circuit was chosen to be implemented as a digital one, thereby featuring a linear transfer characteristic and a half-rate operation mode. Using this phase detector type, the realization of a CDR circuit with relatively low complexity (< 200 active devices) can be achieved, thus promising a successful processing of the circuit by the in-house technology. Furthermore, the linear transfer characteristic is advantageous with respect to the jitter performance of the CDR, while the half-rate operation mode eases the requirements on circuit and layout design.

Based on the selected CDR concept, system level considerations have been briefly performed, thereby allowing to survey the stability of the CDR loop. Furthermore, static and dynamic properties accompanying the CDR design could be defined, as a result of the CDR consideration on system level. Figures of merit of the targeted CDR circuit have been addressed. Since no standards are defined for the aimed 80 Gbit/s data rate, these figures of merit were extrapolated, to some extent, from defined standards at lower data rates.

Chapter 3

InP-DHBT Technology

The analog and digital integrated circuits realized within this work rely on an in-house InP double heterojunction bipolar transistor (InP-DHBT) technology. In general, this technology features several edges over other III-V semiconductor technologies (e.g.: GaAs HBT) as well as Si-based bipolar technologies. In fact, InP-DHBTs provide superior carrier mobility resulting in high operation frequencies at moderate transistor dimensions. The wide bandgap of the InP material allows to achieve high breakdown voltage at the aforementioned high operation frequencies. Furthermore, the relatively low turn-on as well as low saturation voltage of the DHBTs result in low-power analog and digital circuits. Additionally, the inherent low 1/f noise as well as the high dc current gain of InP-DHBTs make them very attractive for realizing low phase noise and low power oscillators.

This chapter presents the underlying InP-DHBT technology regarding the intended design and realization of analog and digital integrated circuits. Beginning with a brief description of the basic operation of the (D)HBT, the structure of each layer forming the different parts of the used DHBTs is presented. The third part of this chapter deals with the device geometrical layout. Subsequently, the fabrication process of the DHBTs is addressed. The resulting dc and high-frequency performance of the devices is then discussed. In the sixth part of this chapter, transistor models describing the small-signal and large-signal behavior of the processed DHBTs are introduced. On the basis of the introduced models, the analog and digital circuits presented from Chapter 4 to Chapter 7 are designed and optimized. The present chapter is finally closed by a summary.

3.1 Basic (D)HBT Operation

The processed DHBTs are exclusively of npn type. That is, regarding the three main layers forming the DHBTs, the emitter and the collector region are doped to the same n-type, while the base region is doped p-type. As generally known from bipolar transistors, electrons and holes respectively represent the primary and secondary conducting carriers involved in the generation of the operation currents. The flow of these carriers through the DHBT layers is illustrated in Figure 3.1. In this figure, the considered operation mode of

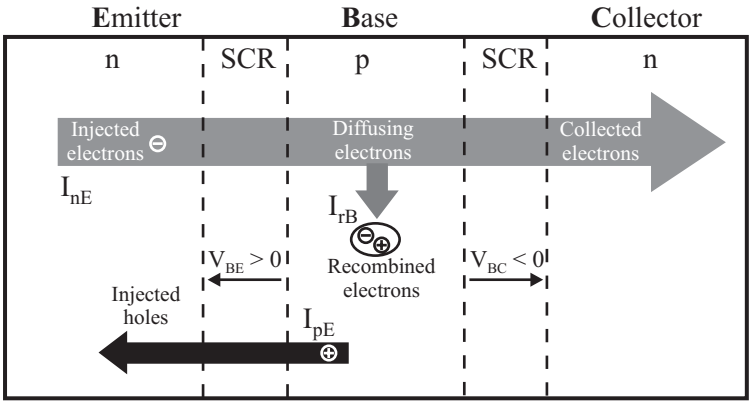


Figure 3.1: Current flow in a bipolar transistor operating in forward active mode. In a first order of approximation, the generation and recombination of carriers in the space charge regions (SCR) can be neglected.

the DHBT corresponds to the forward-active mode of operation. That is, the base-emitter junction is forward-biased at a voltage V_{BE} ($V_{BE} > 0$), while the base-collector junction is reverse-biased at a voltage V_{BC} ($V_{BC} < 0$).

The forward bias on the base-emitter junction results in current flowing across this junction. In a first order of approximation, this current consists of two components: a diffusion current (I_{nE}) caused by the electrons injected from the emitter into the base, and a diffusion current (I_{pE}) caused by the holes injected from the base into the emitter. Both currents constitute the emitter current I_E, as indicated in Figure 3.1. Thus, I_E is defined as follows:

$$I_E = I_{nE} + I_{pE}$$

The injected electrons from the emitter into the base are minority carriers in the p-type base region. These minority carriers diffuse through the base region toward the base-collector junction. During this diffusion, some electrons recombine with holes, thereby creating a recombination current I_{rB}. However, since the base thickness X_B is chosen to be much thinner than the diffusion length L_n of the electron, the percentage of electrons recombining with the holes before reaching the base-collector space charge region is quite small. The base current I_B is defined as follows:

$$I_B = I_{pE} + I_{rB} \approx I_{pE}$$

The electric field in the base-collector space charge region draws the diffusing electrons (in the base region) into the collector region. These electrons are then collected to constitute the collector current I_C. Since the majority of the electrons injected from the emitter in the base reach the collector, the current I_C is defined as follows:

$$I_C \approx I_{nE}$$

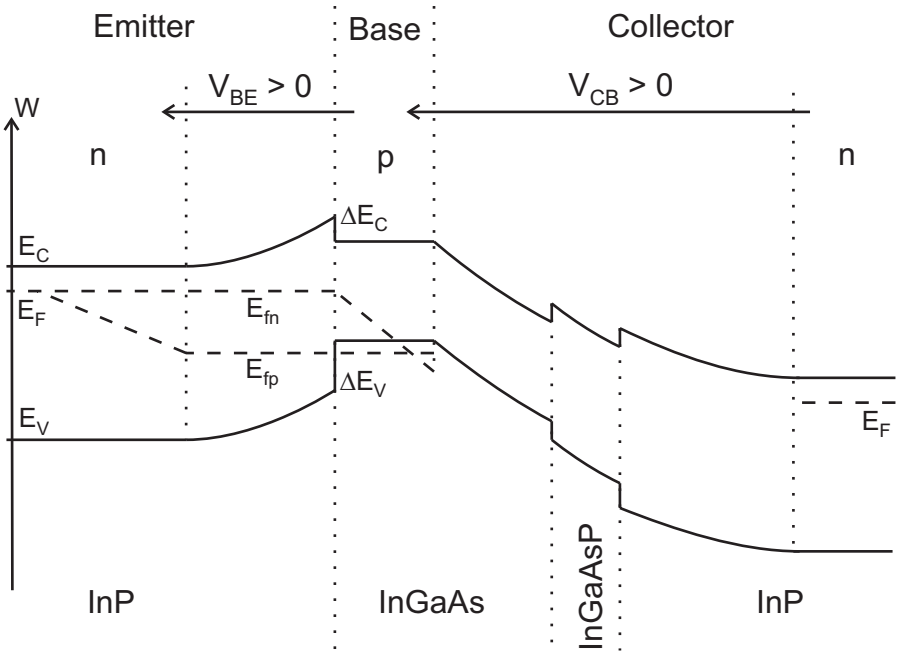


Figure 3.2: Schematic band diagram of a DHBT in forward active mode. The InP and InGaAs material features a bandgap E_G of 1.34 eV and 0.75 eV, respectively. The wideband emitter has a conduction band offset $\Delta E_C = 0.23$ eV and valence band offset $\Delta E_V = 0.37$ eV.

The typical band diagram of the used DHBTs is shown in Figure 3.2. The particularity of the HBTs, compared to their bipolar contenders (e.g.: bipolar junction transistor, BJT), consists in the base-emitter junction, which is a heterojunction. This is illustrated in Figure 3.2 by the conducting band discontinuity in the base-emitter junction. The latter discontinuity is achieved by an emitter material, which features a larger energy gap E_G than the base material.

Considering the geometric and technologic parameters of a HBT, the collector current I_C and the base current I_B are given by the expressions defined in equation (3.1) and equation (3.2), respectively [46]:

$$I_C \approx I_{nE} = \frac{qA_{BE}D_{nB}}{X_B}\frac{n_{iB}^2}{N_B}\left(e^{\frac{qV_{BE}}{k_BT}} - 1\right) \tag{3.1}$$

$$I_B \approx I_{pE} = \frac{qA_{BE}D_{pE}}{L_p}\frac{n_{iE}^2}{N_E}\left(e^{\frac{qV_{BE}}{k_BT}} - 1\right) \tag{3.2}$$

In equation (3.1) and equation (3.2), q is the electric charge, A_{BE} is the base-emitter junction area, D_{nE} is the minority electron diffusion coefficient, n_{iB} is the minority carrier concentration in the base, N_B is the base doping level, k_B is the Boltzmann constant, T is the operation temperature, D_{pE} is the minority hole diffusion coefficient, n_{iE} is the minority carrier concentration in the emitter, L_p is the hole diffusion length in the emitter, and N_E is the emitter doping level. For a HBT, if we assume that the density of states

in the emitter and base region is the same, n_{iB} and n_{iE} are exclusively related to each other by the band gap difference ΔE_G between emitter and base material [46]. Thus, the following relation between n_{iB} and n_{iE} is valid:

$$n_{iB} = n_{iE} e^{\frac{\Delta E_G}{k_B T}} \tag{3.3}$$

The direct current (dc) gain β_{DC} of a HBT is given as follows [46]

$$\beta_{DC} = \frac{I_C}{I_B} \approx \frac{D_{nB} L_p N_E}{D_{pE} X_B N_B} e^{\frac{\Delta E_G}{k_B T}} \tag{3.4}$$

Equation (3.4) reveals the major edge of HBTs over BJTs. In fact, because of the exponential factor including ΔE_G ($\Delta E_G \gg k_B T$), the base and emitter doping level can be determined independently of each other, thereby keeping high the current gain (emitter efficiency almost equal to unity). Thus, on the one hand, the base doping level is chosen to be high in order to minimize the base resistance. The reduced base resistance allows a reduction of the base thickness X_B, thus leading to a much higher current gain. On the other hand, the emitter doping level is chosen to be relatively low ($N_E \ll N_B$), thus allowing to minimize the base-emitter junction capacitance. The latter measures have a positive impact on the high-frequency properties of the processed devices. Regarding BJTs, $\Delta E_G = 0$ and the exponential factor in equation (3.4) is unity. As a consequence, tradeoffs have to be made (e.g. between N_E and N_B) either for the benefit of the current gain or that of high-frequency properties of the device [46].

In the band diagram of Figure 3.2, the step graded collector is specific to the DHBTs used for the development of the integrated circuits. The benefit of this structure type is discussed in the next section.

3.2 Device Layer Structure

The DHBT layer structure is grown on 3-inch InP substrates using a solid phosphorus molecular beam epitaxy (MBE). This MBE allows to achieve good composition control, accurate doping profiles, and high doping levels, the benefit of which is shown in this section. A careful design of the epitaxial layers composing the DHBTs is crucial for achieving outstanding dc and high-frequency performance. Accompanying the development of the InP DHBT technology, substantial investigations have been performed in [70] for optimizing the device layer structure. The current gain β_{DC} and the turn-on voltage, as well as the cut-off frequencies f_T (transit frequency) and f_{max} (maximum oscillation frequency) are used as the figures of merit. These cut-off frequencies are defined as follows ([32], [46]):

$$f_T = \frac{1}{2\pi\tau_{ec}} \; ; \; \tau_{ec} = \underbrace{R_{je}(C_{je} + C_{bc})}_{\tau_e} + \tau_b + \tau_c + \underbrace{C_{bc}(R_E + R_C)}_{\tau_{sc}} \tag{3.5}$$

$$f_{max} = \sqrt{\frac{f_T}{8\pi(R_{bb} + R_B)C_{jc}}} \tag{3.6}$$

In equation (3.5), τ_{ec} represents the emitter-collector transit time. This transit time is composed of the emitter charging time τ_e, the base transit delay τ_b, the collector transit time τ_c, and the collector space charge delay τ_{sc}. τ_e is determined by the base-emitter junction resistance R_{je}, the base-emitter junction capacitance C_{je}, and the total base-collector junction capacitance C_{bc}. τ_{sc} is given by the emitter and collector path resistances R_E and R_C, respectively, as well as C_{bc}. In equation (3.6), the resistances R_{bb} and R_B represent the intrinsic and extrinsic base resistance, respectively, while C_{jc} is the intrinsic base-collector junction capacitance.

In addition to the dc and high-frequency performance, the power performance of the DHBT may benefit from a careful design of the device layer structure. The underlying (vertical) layer structure for the processing of the used DHBTs is illustrated in Table 3.1.

Layer	Thickness (nm)	Material	Doping (cm^{-3})
Emitter	40	InP:Si	6.0×10^{17}
Base	30	$In_{0.53...0.45}Ga_{0.47...0.55}As$:C	5.0×10^{19}
Collector spacer	50	$In_{0.53}Ga_{0.47}As$	
Collector	20	$In_{0.75}Ga_{0.25}As_{0.54}P_{0.46}$	
Collector	20	InP:Si	2.0×10^{17}
Collector	70	InP:Si	2.0×10^{16}

Table 3.1: Layer structure of the used InP/InGaAs DHBT.

Emitter Layer

As shown in Table 3.1, the emitter layer is composed of Si-doped InP ($E_G = 1.35$ eV). The design of this layer has a direct impact not only on the emitter charging time τ_e, but also on the base-emitter turn-on voltage. In fact, a high emitter doping level is needed for obtaining low turn-on voltage, while a lightly doped emitter results in a low base-emitter junction capacitance, thus benefiting τ_e and consequently f_T (see equation (3.5)). Thus, as a trade-off, the emitter doping level N_E is set to a value of 6×10^{17} cm^{-3}. A relatively thin emitter ($X_E = 40$ nm) further contributes to shift the turn-on voltage to lower values [70].

Base Layer

The base layer is initially composed of C-doped InGaAs ($E_G = 0.75$ eV). Thus, with respect to the InP material in the emitter region, a heterostructure is generated at the base-emitter junction. The design of the base layer allows to influence the base transit delay τ_b in equation (3.5) as well as the intrinsic base resistance R_{bb} in equation (3.6). Moreover, the dc current gain β_{DC} is also influenced by adjusting the base layer. Thus, a thin base ($X_B = 30$ nm) helps minimizing τ_b, thereby maximizing f_T as well as β_{DC}. Furthermore, a high base doping level ($N_B = 5 \times 10^{19}$ cm^{-3}) proves to be effective for an essential reduction of R_{bb}, thereby moving f_{max} to higher values. As described in Table 3.1, an InGaAs grading ($In_{0.53...0.45}Ga_{0.47...0.55}As$) is subsequently introduced in the base region,

thus allowing to gradually increase the bandgap (in the base) from the collector side to the emitter side. The latter measure generates an additional electric field which further reduces τ_b and consequently further increases β_{DC} and f_T [70].

Collector Layer

According to Table 3.1, the collector layer incorporates a step grading composed of an InGaAs spacer followed by a quaternary layer of InGaAsP. This step grading is adjacent to a thin n-doped InP layer. The collector layer in this form is particularly effective for minimizing the undesired current blocking effect [70]. The latter effect would be strongly present if the InGaAs base were directly adjacent to the InP layers in the collector, thus forming a strong conduction band discontinuity at the base-collector junction. Negative consequences would be higher values of τ_{sc} in equation (3.5), lower β_{DC}, and higher saturation voltage.

The total collector thickness is chosen to be 160 nm. This thickness is a trade-off between the transit time τ_{sc}, which is proportional to the collector length, and the junction capacitance C_{jc}. The latter capacitance is inversely proportional to the collector thickness. Furthermore, a thinner collector would support higher collector current densities ([28], [83]).

3.3 Device Geometrical Layout

The underlying layout for the used DHBTs is illustrated in Figure 3.3. Extensive experimental investigations have been performed in [70] for determining the optimum lateral dimensions of the DHBTs. Namely, beside a good epitaxial layer design, the geometrical layout design of the transistor is also essential for obtaining outstanding high-frequency performance. Table 3.2 shows the resulting lateral dimensions of the used DHBTs, considering the emitter, base, and collector regions.

	W_E [μm]	L_E [μm]	W_B [μm]	S_{BE} [μm]	L_B [μm]	W_C [μm]	S_{BC} [μm]	L_C [μm]
Dimension	1	2 - 16	0.75	1.5	2	2	1	2 - 16

Table 3.2: Lateral dimensions of the used DHBTs with respect to Figure 3.3.

Emitter dimensions

The emitter width W_E is set to be 1 μm, as shown in Table 3.2. In general, W_E should be as small as possible in order to minimize the resistance R_{bb} and the capacitance C_{jc} of the HBT, thus maximizing f_{max} (cf. equation (3.6)). Furthermore, a small W_E results in a concentrated base current flow through the base-emitter junction, thus minimizing the current crowding effect and consequently the effective base-emitter junction capacitance

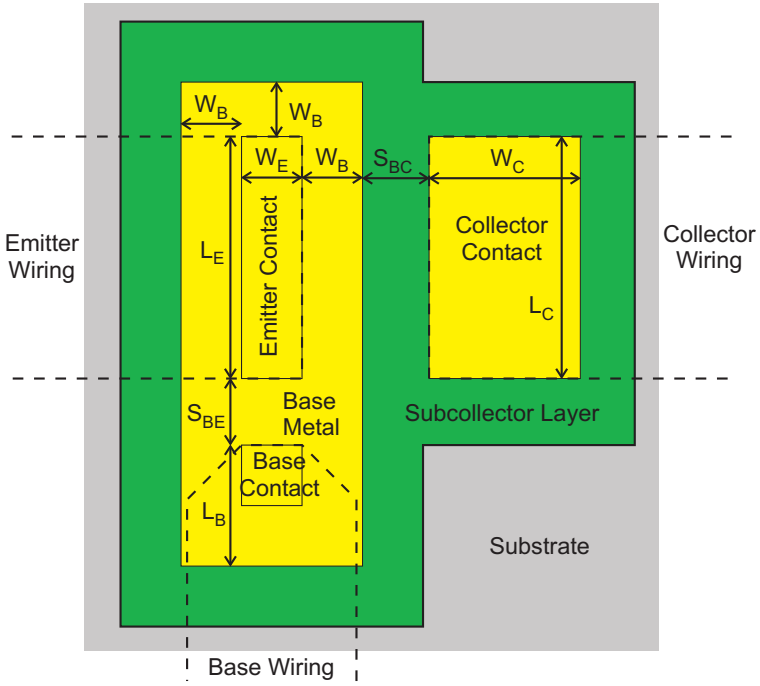


Figure 3.3: Top view of the underlying DHBT layout.

C_{je}. This results in higher f_T values, regarding equation (3.5). From a technological point of view, W_E can be reduced down to 0.7 μm as shown in [70]. However, within this work, W_E of the used DHBTs is chosen to be 1 μm, to ensure high circuit yield.

The emitter length L_E features values ranging between 2 μm and 16 μm. Thus, during the circuit design, L_E is used as setting variable for varying the device size according to the circuit requests, e.g.: operation current, junction capacitances (for transistor varactor in Chapter 4), minimal gate delay. In the present technology, a too short L_E results in a strong decrease of f_T and f_{max} (cf. sec. 3.5.2) due to an increase of the influence of the extrinsic base-collector capacitance with respect to the small active device size. Furthermore, a too long L_E induces a drop of f_{max}, which might be due to resistive and inductive effects in the base contact [70].

Base dimensions

The base width W_B is set to be 0.75 μm. Commonly, W_B should be as small as possible in order to minimize the total base-collector capacitance, thus essentially reducing f_T and f_{max}. The in-house process technology is capable of processing DHBTs featuring W_B values down to 0.5 μm [70]. However, device processing with high yield and good reliability is only available for base width values of at least 0.75 μm.

The area determined by the lengths L_B and S_{BE} in Figure 3.3 contributes to the base-collector junction capacitance of the device. Therefore, the corresponding dimensions should be as small as possible. The lower limit of the latter dimensions is determined by

the process technology with respect to high device yield and process reliability. Thus, L_B and S_{BE} amount to 2 μm and 1 μm, respectively.

Collector dimensions

The collector dimensions S_{BC}, W_C, and L_C are set in such a way that the corresponding extrinsic collector resistance R_C is minimized. A small R_C minimizes the collector charging time τ_{sc}, thus resulting in high f_T values (cf. equation (3.6)). Thus, with respect to device yield and process reliability, the spacing S_{BC} is set to 1 μm. In order to guarantee low resistance value as well as compact device layout, the collector width W_C is twice as wide as the emitter width. That is, W_C amounts to 2 μm. A collector length L_C, which is equal to the emitter length, proves to be advantageous for an uniform current distribution in the collector. Therefore, L_C features values ranging between 2 μm and 16 μm.

3.4 Process Technology

Device and Circuit Process

The fabrication process of the used InP/InGaAs DHBTs as well as that of the integrated circuits (ICs) relies on a standard triple mesa technology [26]. This technology features self-aligned base-emitter contacts and selective wet chemical etching for forming the triple mesa structure. Furthermore, a benzocyclobutene (BCB) polymer film is used for device passivation and planarization. The collector and the base are connected using via holes in the BCB. Figure 3.5 and Figure 3.4 show the SEM (scanning electron microscopy) photographs of processed DHBTs from a side and top view, respectively.

The backend process of the DHBT technology conforms with a well-established in-house metamorphic HEMT-based IC process. This process features NiCr resistors (50 $\Omega/\square$), thin film MIM capacitors (23 fF/μm^2), and three levels of gold-based interconnect metals.

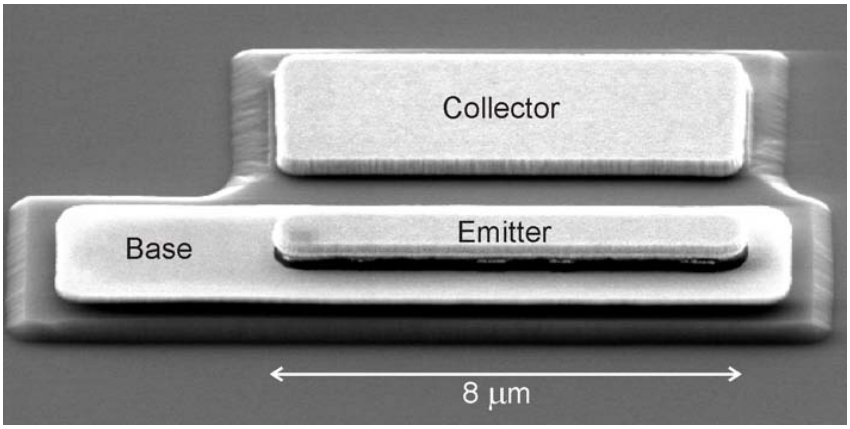


Figure 3.4: SEM photograph illustrating the top view of processed DHBTs. The photograph is consistent with the transistor layout illustrated in Figure 3.3.

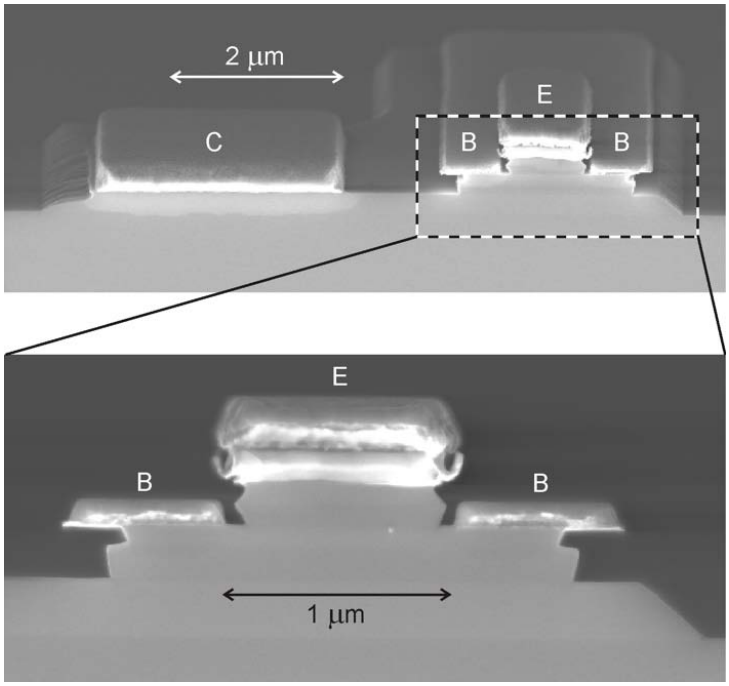


Figure 3.5: SEM photograph showing the typical cross-section of processed DHBTs.

Figure 3.6 illustrates the schematic cross-section of the DHBT process, thereby showing all the elements available for the ICs design. The NiCr resistors are below the BCB. They are connected using the metal layer MET1. For the implementation of the MIM capacitors, the layer MET2 and the galvanic metal are used. A thin layer of silicon nitride acts as dielectric. Air bridges are implemented using the galvanic metal layer.

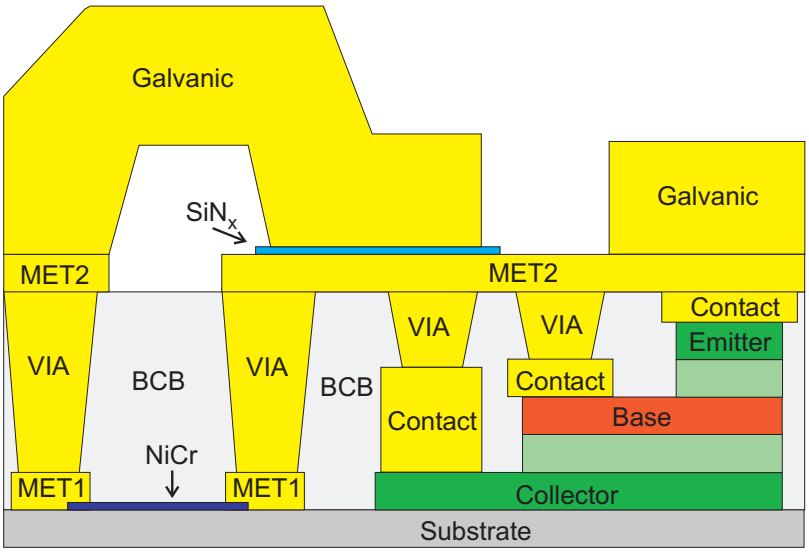


Figure 3.6: Schematic cross-section of the DHBT process.

Circuit Interconnects

By exploiting the metal layers offered by the IC process, transmission lines in form of simple metal connection lines and coplanar waveguides (CPW) are implemented for signal guiding outside and inside of the ICs. The former transmission line type is realized using the galvanic metal layer with a width of 4 μm, thereby displaying a resistance and inductance per unit length of 2 mΩ/μm and 1 pH/μm, respectively.

Regarding the coplanar lines, the corresponding ground and signal conductors are realized using the two upper metal layers MET2 and galvanic. The line impedance is determined by adjusting the ratio between the ground-to-ground spacing (S) and the signal conductor width (W) ([21], [80]). Thus, the developed mixed-signal ICs include CPW lines with a line impedance of 70 Ω (S = 50 μm, W = 7 μm) and 50 Ω (S = 25 μm, W = 8.5 μm).

3.5 Device Characteristics

In this section, figures of merit representing the dc and high-frequency performance of the processed DHBTs are briefly discussed. These characteristics result from the optimum vertical and horizontal device structure, as presented in the previous sections. Among the dc performance, the current gain β_{DC}, the turn-on voltage, the saturation voltage, and the breakdown voltage are treated. Regarding the high-frequency performance, the cut-off frequencies f_T and f_{max} are addressed.

3.5.1 DC Characteristics

Figure 3.7 illustrates the measured Gummel plot for an 1 $\times$ 8 μm^2 DHBT. The displayed variation of I_C and I_B as a function of V_{BE} is typical for the processed DHBTs. Thus, leakage currents below 1 nA are stated. Furthermore, the ideality factors for base and collector currents extracted at a current of 1 μA amount to 1.4 and 1.1, respectively. From Figure 3.7, a maximum current gain β_{DC} of 85 is extracted. No current blocking effect can be observed by varying V_{BE} up to 1 V.

Figure 3.8 shows the measured output characteristic for an 1 $\times$ 8 μm^2 DHBT. From this characteristic, a relatively low turn-on voltage of 0.12 V can be read. Furthermore, the saturation voltage amounts to 0.7 V, while the breakdown voltage is measured to be 5 V. All these characteristics are typical for the different device sizes available in the technology.

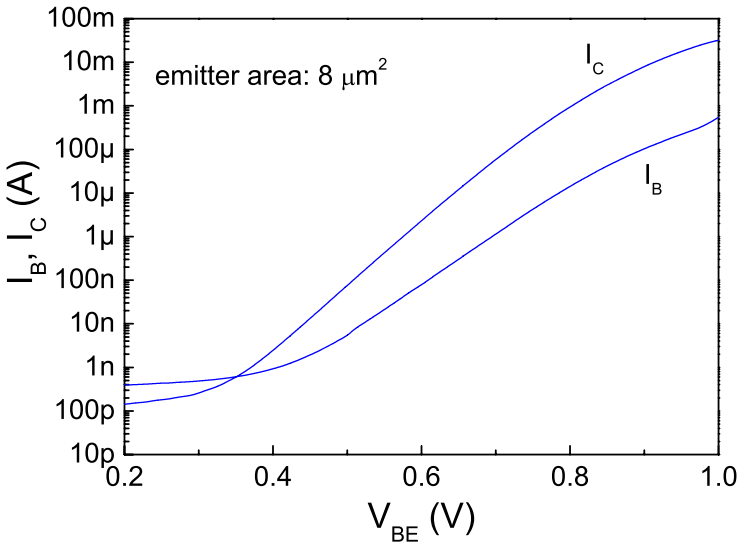


Figure 3.7: Typical Gummel plot of the processed InP/InGaAs DHBTs.

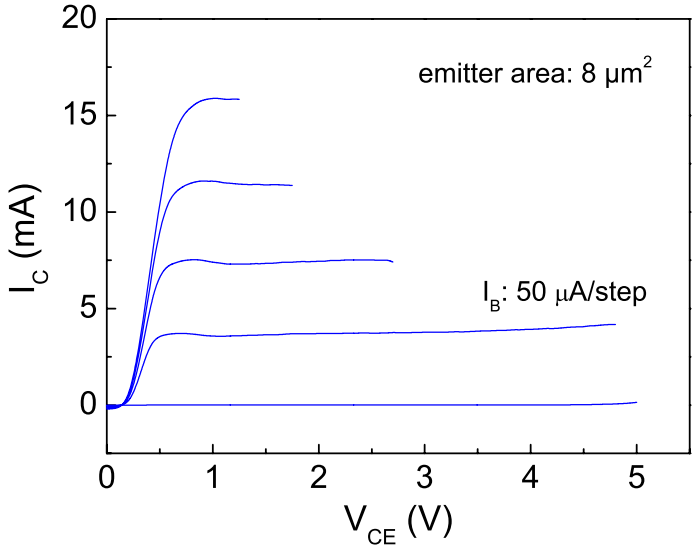


Figure 3.8: Output characteristic of an 1 × 8 μm^2 DHBT.

3.5.2 High-frequency Characteristics

Figure 3.9 and Figure 3.10 respectively show the variation of the cut-off frequencies f_T and f_{max} as a function of the collector current density J_C, for different collector-emitter voltages V_{CE}. The device size amounts to 1×8 μm^2. Thus, a non-negligible bias dependence of these cut-off frequencies can be stated. This bias dependence is due to the so-called velocity modulation effect. This effect describes the non-monotonic dependence of the electron velocity on the electric field in the InP layers of the HBTs [24].

Considering Figure 3.9, f_T features a maximum value of 240 GHz at a current density J_C of 3.0 mA/μm^2 and a voltage V_{CE} of 1.75 V. Regarding Figure 3.10, f_{max} features a maximum value of 250 GHz at a current density J_C of 3.0 mA/μm^2 and a voltage V_{CE} of 2 V. Thus, with respect to highest cut-off frequencies, an optimum operation of the device is achieved at a current density J_C of approximately 3.0 mA/μm^2 and voltages V_{CE} between 1.5 V and 2 V. The latter statement remains valid for the other device sizes available in the technology. Relying on this, Figure 3.11 depicts the variation of the cut-off frequencies f_T and f_{max} as a function of the emitter length L_E at the optimum operation point: $V_{CE} = 1.75$ V and $J_C = 3.0$ mA/μm^2. According to this figure, the frequency f_T increases with emitter length up to 250 GHz for long emitters. Moreover, the frequency f_{max} features a maximum value well above 270 GHz at an emitter length of 6 μm. The sharp drop of f_T and f_{max} for short L_E as well as the moderate drop of f_{max} for long L_E is explained in sec. 3.3.

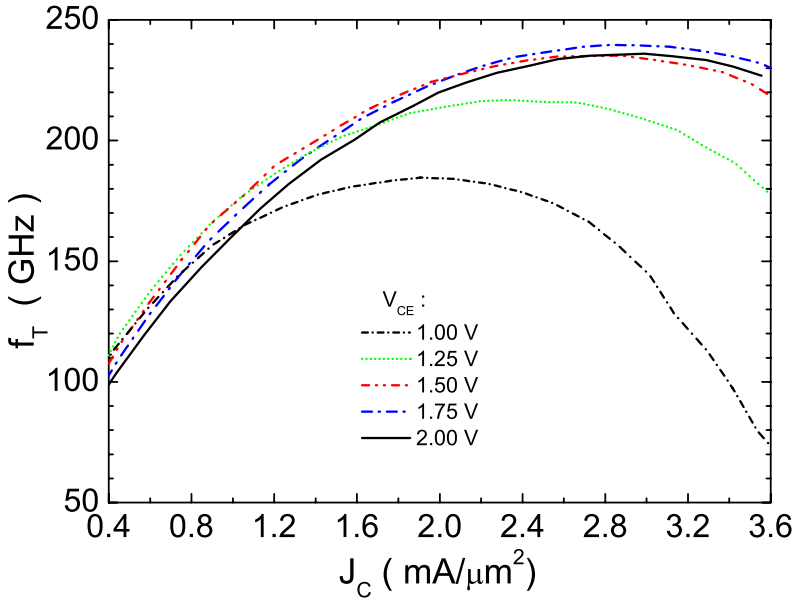


Figure 3.9: Variation of the transit frequency f_T as a function of the collector current density J_C for different collector-emitter voltages V_{CE}. The considered device features a size of 1×8 μm^2.

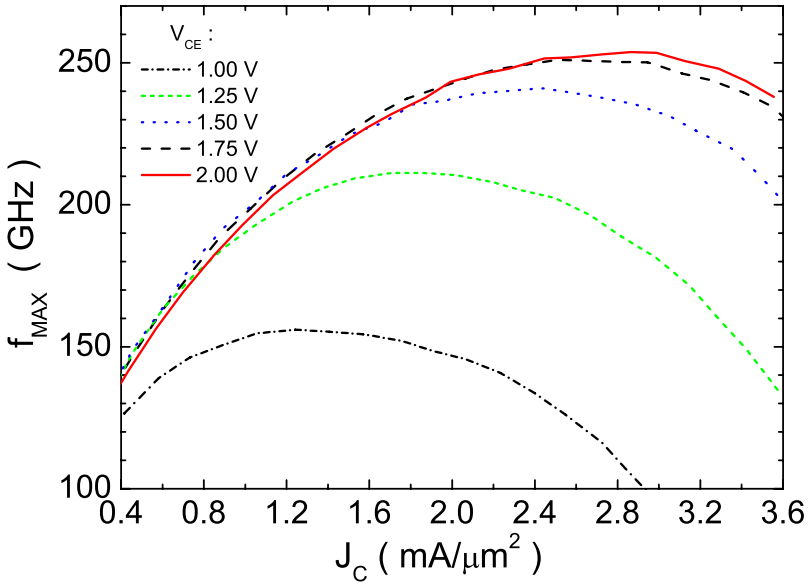


Figure 3.10: Variation of the maximum oscillation frequency f_{max} as a function of the collector current density J_C for different collector-emitter voltages V_{CE}. The considered device features a size of 1×8 μm^2.

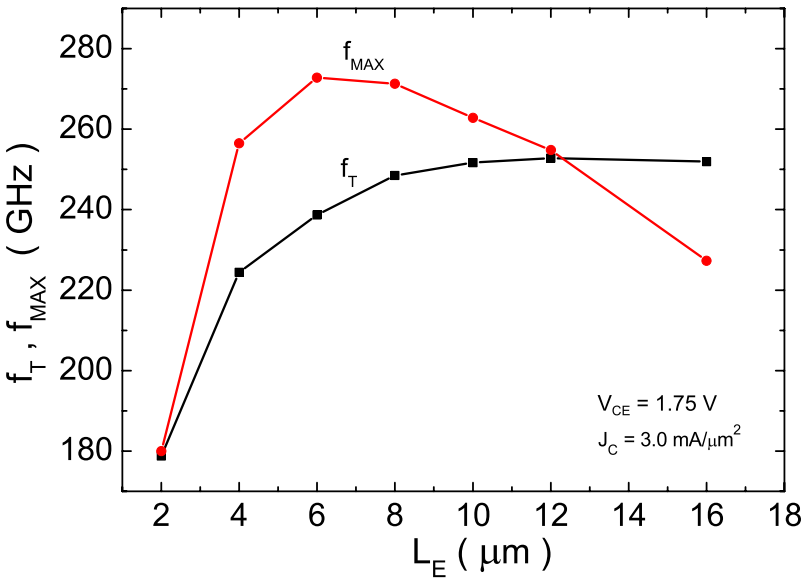


Figure 3.11: Variation of the cut-off frequencies f_T and f_{max} as a function of the emitter length L_E at the device operation point: $V_{CE} = 1.75$ V, $J_C = 3.0$ mA/μm^2.

3.6 Device Models

The analog and digital integrated circuits presented from Chapter 4 to Chapter 7 feature a steady operation state, which drives the included DHBTs in a nonlinear operation mode. Because of this fact, a large-signal model of the DHBTs with sufficiently high accuracy is needed for reliable design, investigation, and optimisation of these integrated circuits. In addition to this large-signal model, an accurate small-signal model is further needed. Namely, the starting operation state of targeted analog circuits such as voltage controlled oscillators is well described by its (linear) small-signal behavior, thus allowing a starting dimensioning of the circuit. Furthermore, a small-signal model is needed for frequency bandwidth investigations of the buffer amplifiers included in the digital circuits. Thus, this section introduces the underlying large-signal model of the DHBTs included in the integrated circuits. Moreover, the small-signal model accompanying the design and analysis of the targeted analog circuits is addressed.

3.6.1 Large-Signal Model

The underlying large-signal model of the used DHBTs originates from the University of California, San Diego and is therefore referred to as UCSD-model. This model is specific to DHBTs, thus allowing a better description of the corresponding large-signal behavior, unlike its contenders such as the Gummel-Poon-Model [17]. In fact, the UCSD-model shows the following attractive features for modeling accurately the large-signal behavior of DHBTs:

- A variety of transit time parameters is available for taking into account the velocity modulation effect, which is responsible for the bias dependence of the cut-off frequencies f_T and f_{max}.
- The impact of potential spike, appearing at the heterojunctions, on the collector current is considered, thus allowing to take into account the variation of the current gain β_{DC} with the collector current density J_C.
- The modeling of thermal effects including self-heating of the DHBTs is possible.
- The Kirk effect, which induces the drop of the cut-off frequencies f_T and f_{max} at high current densities, can be modeled.

Figure 3.12 illustrates the large-signal equivalent circuit of the DHBTs, according to the UCSD-model. In this figure, only the components needed for large-signal modeling of the used DHBTs are represented. In fact, the UCSD-model provides much more components for HBT modeling, as discussed in [78]. Thus, in Figure 3.12, the intrinsic and extrinsic path resistances in the emitter (R_e), base (R_{bi}, R_{bx}), and collector (R_{ci}, R_{cx}) region are considered. Furthermore, the pn diodes built by the base-emitter and base-collector junction with the respective currents (I_{bci}, I_{bcx}, I_{be}) are addressed. The corresponding junction

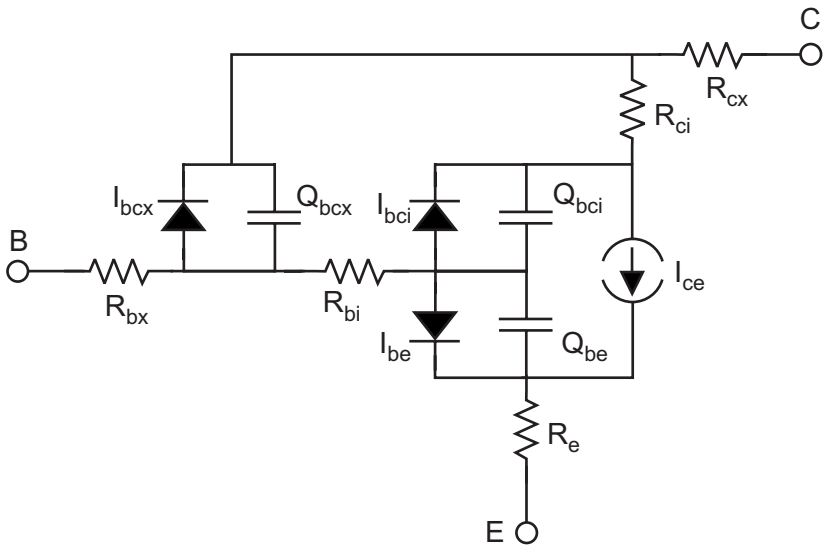


Figure 3.12: DHBT large-signal equivalent circuit according to the UCSD-model. Only the components needed for the device modeling are represented.

and diffusion capacitances are also included (Q_{bci}, Q_{bcx}, Q_{be}). Finally, the electron flow from the emitter to the collector is taken into account with the current source I_{ce}. A list of the used model parameters as well as their corresponding values are given in appendix A.1. The extraction method for obtaining the latter model parameters is presented in details in [70].

3.6.2 Small-Signal Model

For small-signal analysis and simulation of the developed integrated circuits, the small-signal equivalent circuit according to Figure 3.13 is valid. The actual transistor equivalent model is within the boundary. The components out of the boundary represent the parasitic capacitances between the transistor ports, the parasitic inductances and the contact resistances at the transistor ports.

The small-signal equivalent circuit uses a T-topology. An advantage of this topology is its direct correlation with the physic architecture of the device. A list of the used model parameters as well as their corresponding values are given in appendix A.2. As for the large-signal model presented before, the extraction methods of the small-signal parameters are discussed in details in [70]. In addition to the T-topology, the so-called Π-topology is also applied for analytical (small-signal) analysis of the targeted circuits (e.g.: VCOs), as shown in Chapter 4. An one-to-one transformation between the Π-model and the T-model is available [67].

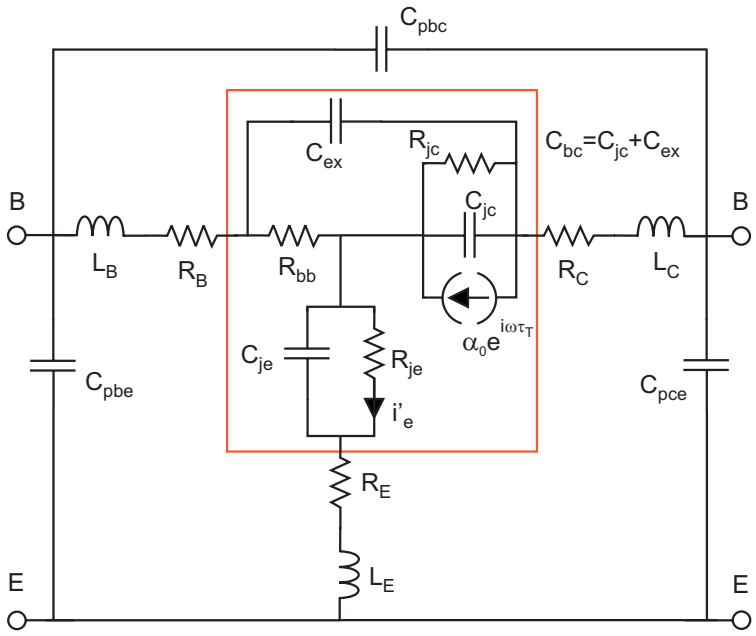


Figure 3.13: Small-signal equivalent circuit of the used DHBTs. The internal device is within the boundary.

3.7 Summary

In this chapter, the underlying InP-DHBT technology for the ICs development has been discussed. Thus, the epitaxial structure of the layers forming the used DHBTs has been presented. The crucial importance of a careful layer design for obtaining outstanding device performance has been emphasized. In fact, the choice of the device layer structure has a considerable impact on the corresponding dc performance (current gain β_{DC}, turn-on voltage, saturation voltage) and on the high-frequency performance (f_T, f_{max}).

In addition to the device layer structure, the corresponding geometrical layout has been presented. Its critical importance for further improving the high-frequency performance of the device has been pointed out. Thus, among the geometric layout parameters, the emitter length L_E of the device has been set variable, thus allowing the variation of the device size according to the requirements of the designed circuit. The other geometric layout parameters are set to (optimum) fix value with respect to high-frequency performance as well as high device yield and reliability.

The process technology has been briefly discussed, thereby pointing out the different components contributing to the processing of the device, the passive components, and the integrated circuits. The resulting performance of the devices, regarding the available (different) emitter lengths, was then presented. Thus, the devices feature a maximum current gain β_{DC} of 85, a turn-on voltage of 0.12 V, a saturation voltage under 1 V and a breakdown voltage of > 4 V. Moreover, cut-off frequency values of more than 250 GHz

for both f_T and f_{max} have been achieved at a collector current density of approximately 3.0 mA/μm^2.

The high current gain featured by the DHBTs combined with the high cut-off frequency f_{max} are essential properties for realizing high-frequency low-noise VCOs with relatively low power consumption, as is shown in Chapter 4. Furthermore, the relatively high breakdown voltage offers enough margin for achieving high signal power at the intended high operation frequencies.

Thanks to the low turn-on and saturation voltage in association with the high cut-off frequencies (f_T, f_{max}) and the (relatively) high current densities, the fundament for developing high-speed digital circuits, to some extent with low power consumption, are set. The next chapters deal with all these mentioned circuits.

Chapter 4

Voltage Controlled Oscillators for > 80 Gbit/s Applications

Voltage controlled oscillators (VCOs) are important building blocks in clock and data recovery (CDR) circuits, as described in sec. 2.1. For the implementation of VCOs intending high data rate applications, so called LC-type oscillators are a better candidate compared to their counterparts (ring and relaxation oscillators), since they combine high-frequency operation capabilities with low phase noise performance as well as large output signal swings [18], [69], [73].

This chapter deals with the design, implementation, and characterization of LC-type VCOs, suitable for use as a frequency source for half- and full-rate data clocking at data rates over 80 Gbit/s. Beginning with a general description of oscillators, we then introduce the so-called negative resistance (NR) LC-type oscillator and its existing design and analysis approaches. The phase noise, as an important quality factor for the purity of the frequency source signal, is discussed in the third part of this chapter. Based on the selected design and analysis method, low-noise VCO circuit concepts and their implementations for operation frequencies around 43 GHz and 86 GHz are presented in the fourth part of this chapter. Finally, measurement technique issues as well as the achieved IC performance are discussed. The organization structure of this essential chapter is further illustrated in the block diagram of Figure 4.1. The logical links between the development steps accompanying the VCO realization are pointed out.

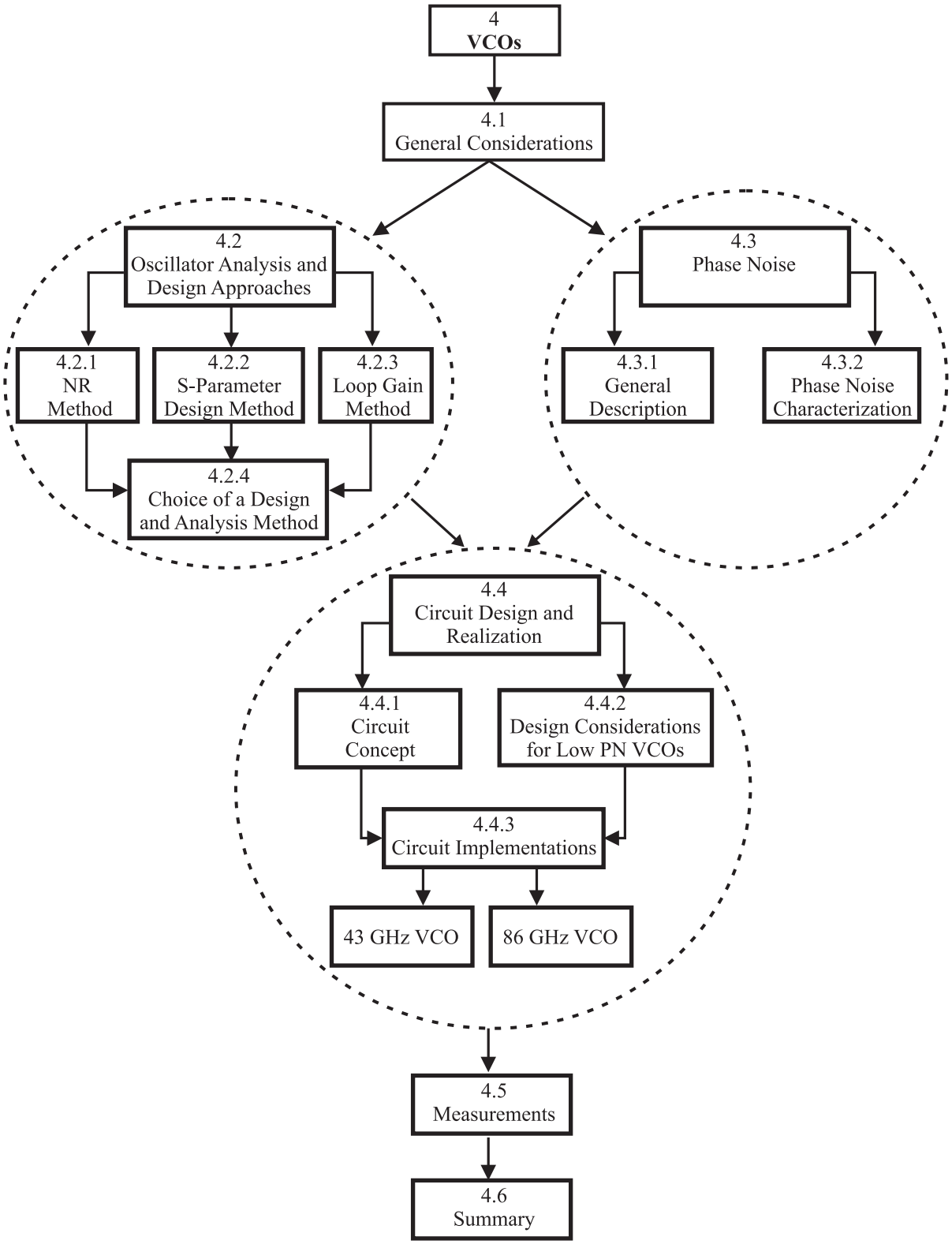


Figure 4.1: Block diagram showing the organization structure of this chapter. The block sequence illustrates the logical development step applied towards the realization of the VCOs. Abbreviations: NR = Negative Resistance, PN = Phase Noise.

4.1 General Considerations

An oscillator can be considered as an amplifier system, which produces a harmonical signal at its output. In the time domain, this signal is ideally expressed by the following mathematical expression:

$$v_{out}(t) = V_0 \, cos(\omega_0 t + \varphi_0) \tag{4.1}$$

According to equation (4.1), the oscillator ideally generates a sinusoidal output signal with constant amplitude V_0, frequency ω_0, and phase φ_0. In the frequency domain, the output signal corresponds to an ideal pulse at frequency ω_0, as shown in Figure 4.2.

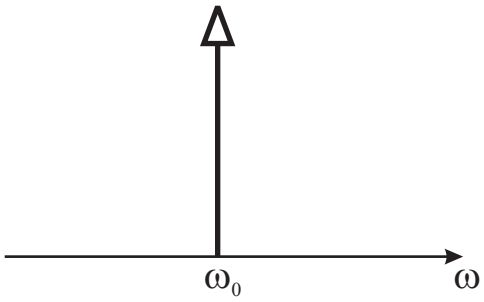


Figure 4.2: Spectrum of an ideal oscillator output signal.

In general, the oscillator is described as an amplifier whose output is fed back to its input through a feedback network, as illustrated in Figure 4.3. At the summation point, either negative or positive feedback can occur. Negative feedback is available, if the phase shift between the fed back signal v_f and the input signal v_{in} is $n \cdot 180°$ (with n = 1,3,5,...), whereas the phase of v_f is determined by the closed loop circuit. Positive feedback occurs, if the phase shift between v_f and v_{in} is $n \cdot 360°$ (with n = 0,1,2,...). As shown in Figure 4.3, v_f is added to v_{in} at the summing network, thus resulting in a positive feedback, which is essential for oscillations to occur. The feedback network, also called resonator, is a frequency selective network, where the operation frequency of the oscillator output signal is adjusted.

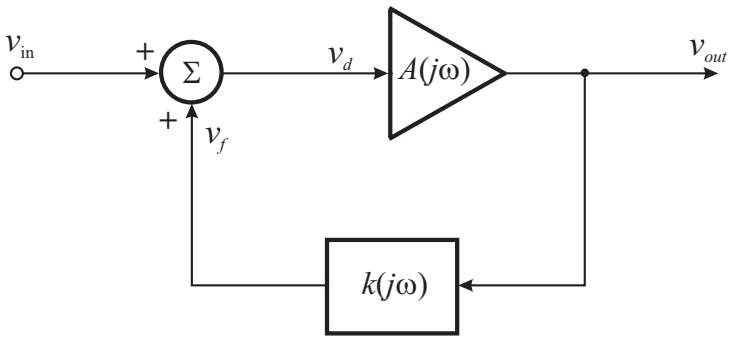


Figure 4.3: Classical oscillator description by means of a feedback topology.

Considering the gain $A(j\omega)$ of the amplifier and the transfer function $k(j\omega)$ of the feedback network (see Figure 4.3), we can write:

$$v_{out} = A(j\omega)v_d \tag{4.2}$$

$$v_f = k(j\omega)v_{out} \tag{4.3}$$

and

$$v_d = v_{in} + v_f. \tag{4.4}$$

From equation (4.2) to (4.4), the transfer function $H(j\omega)$ of the oscillator system results in:

$$H(j\omega) = \frac{v_{out}}{v_{in}} = \frac{A(j\omega)}{1 - k(j\omega)A(j\omega)} \tag{4.5}$$

The basic condition for oscillations start up is given if the oscillator system becomes unstable. In this case, an output signal is generated even in the absence of an input signal. Expressing this by means of equation (4.5), with $v_{in} = 0$, a finite output signal v_{out} is available only when:

$$1 - k(j\omega)A(j\omega) = 0$$

or

$$k(j\omega)A(j\omega) = 1 \tag{4.6}$$

The expression $k(j\omega)A(j\omega)$ is referred to as the loop gain of the oscillator system. Equation (4.6) is known as the Barkhausen criterion. According to this criterion, oscillations occur if the loop gain is equal to unity. Equation (4.6) can also be expressed in polar form, as described by the following expressions:

$$\mid k(j\omega)A(j\omega) \mid = 1 \tag{4.7}$$

and

$$arg[k(j\omega)A(j\omega)] = n \cdot 360^\circ \; with \; n \; = \; 0, 1, 2... \tag{4.8}$$

Equation (4.7) and (4.8) are respectively known as the amplitude and phase condition for oscillations to occur. The frequency of oscillation can be derived from equation (4.8) as the frequency at which the phase shift around the closed loop is 0° or a multiple of 360°.

For oscillators addressing the millimeter-wave frequency domain, a compact circuit topology is required in order to minimize the influence of parasitic elements on the circuit core. Unlike oscillators with obvious feedback circuit (e.g. Colpitts oscillator, Hartley oscillator), so-called negative resistance (NR) oscillators prove to be an adequate candidate for fulfilling the aforementioned requirement. The basic configuration of NR oscillators features an active device, commonly a transistor, whose ports are connected with frequency dependent networks in such a way that a negative resistance is generated at one of these ports. These networks are realized either by means of inductances, or capacitances, or a combination of both. A general small-signal schematic diagram of the NR oscillator

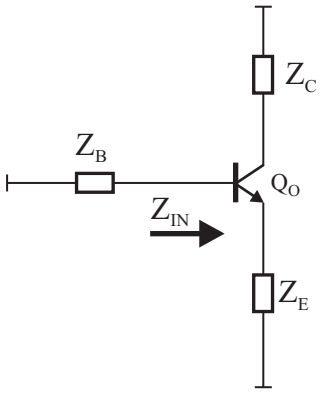


Figure 4.4: Small-signal schematic diagram of a negative resistance oscillator.

is shown in Figure 4.4, where the elements Z_C, Z_B and Z_E represent the corresponding impedance of the frequency dependent networks. The negative resistance is assumed to be generated at the base of the transistor, which therefore features an unstable behavior. That is, the input impedance Z_{in} features a negative real part.

Since the negative resistance oscillator corresponding to Figure 4.4 does not feature an explicit separation between the amplifier (or transistor) and the feedback network, a NR oscillator analysis based on the discussed (classical) feedback model is a priori not suitable. General applicable methods for small-signal considerations are presented in the following section.

4.2 Oscillator Analysis and Design Approaches

4.2.1 Negative Resistance Method

The negative resistance method implies the description of the NR oscillator as an one-port system, as shown in Figure 4.5. On the one hand, this system is composed of the amplitude and frequency-dependent impedance Z_{IN}, representing the active element. Z_{IN} is described by the following expression:

$$Z_{IN} = R_{IN}(A, \omega) + jX_{IN}(A, \omega) \tag{4.9}$$

where A is the amplitude of $i(t)$ and $R_{IN}(A, \omega) < 0$.

On the other hand, the one-port system is completed by the connection of the active element to the load impedance Z_L, which is given by the expression:

$$Z_L = R_L(\omega) + jX_L(\omega) \tag{4.10}$$

Referring to Figure 4.4, Z_L represents the impedance Z_B, while Z_{IN} represents the transistor input impedance at the base port.

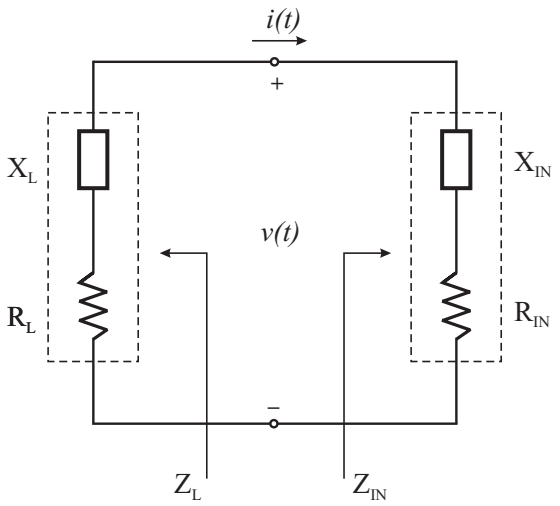


Figure 4.5: One-port description of a negative resistance oscillator.

For oscillations to build up, the active device has to overcompensate the losses in the one-port network. This means that the net resistance of the network should be negative, thus corresponding to the mathematical expression:

$$R_{IN}(A,\omega) + R_L(\omega) < 0 \tag{4.11}$$

At the start of oscillations, the amplitude A of the sinusoidal current $i(t)$ through the loop is very small and given by the noise within the network. In order to ensure the growing up of $i(t)$ or the corresponding amplitude A, equation (4.11) must be even satisfied for $A \approx 0$. This is expressed in the form:

$$R_{IN}(0,\omega) + R_L(\omega) < 0 \tag{4.12}$$

which is related to as the starting oscillation condition.

The oscillations will continue to build up as long as the net resistance of the network is negative, according to equation (4.11). The amplitude of the current will eventually reach a steady-state value ($A = A_0$ at $\omega = \omega_0$), which is the case when the net resistance of the network is zero. In other words, steady-state oscillations at the frequency ω_0 and the amplitude A_0 are sustained if the following oscillation condition is satisfied:

$$Z_{IN}(A_0,\omega_0) + Z_L(\omega_0) = 0 \tag{4.13}$$

Substituting equation (4.9) and (4.10) into (4.13) and equating the real and imaginary parts, the steady-state oscillation condition can be expressed as

$$R_{IN}(A_0,\omega_0) + R_L(\omega_0) = 0 \tag{4.14}$$

and

$$X_{IN}(A_0,\omega_0) + X_L(\omega_0) = 0 \tag{4.15}$$

The oscillation frequency is uniquely determined by the oscillation condition defined in equation (4.14) and (4.15). However, due to the amplitude and frequency dependence of $Z_{IN}(A,\omega)$, the oscillation frequency might not be stable. Therefore, a completing condition for ensuring a stable oscillation has been introduced by Kurokawa [33]. This condition is expressed in the form

$$\left.\frac{\partial R_{IN}(A)}{\partial A}\right|_{A=A_0} \left.\frac{\partial X_L(\omega)}{\partial \omega}\right|_{\omega=\omega_0} - \left.\frac{\partial X_{IN}(A)}{\partial A}\right|_{A=A_0} \left.\frac{\partial R_L(\omega)}{\partial \omega}\right|_{\omega=\omega_0} > 0 \tag{4.16}$$

and is valid if the frequency dependence of $Z_{IN}(A,\omega)$ is negligible for small variations around ω_0.

4.2.2 S-Parameter Design Method

The S-Parameter design approach requires the description of the oscillator system by means of a two-port network, as shown by the corresponding block diagram in Figure 4.6. In this case, the transistor amplifier behavior is described by its small-signal scattering parameters (S-parameters). The oscillator network is eventually completed by the terminating network impedance Z_T and load impedance Z_L. Additionally, the input and output of the transistor amplifier as well as the load and terminating network are characterized by their respective reflection coefficient, which is defined by the general expression:

$$\Gamma_X = \frac{Z_X - Z_0}{Z_X + Z_0} \tag{4.17}$$

whereas Z_0 is the reference impedance value of the system.

Considering the loop related to the input of the transistor, oscillations are able to occur at this port if the following condition is satisfied:

$$\Gamma_{IN}\Gamma_L = 1 \tag{4.18}$$

The fulfillment of equation (4.18) gives rise to oscillations at the second port of the oscillator system. This can be proved as follows.

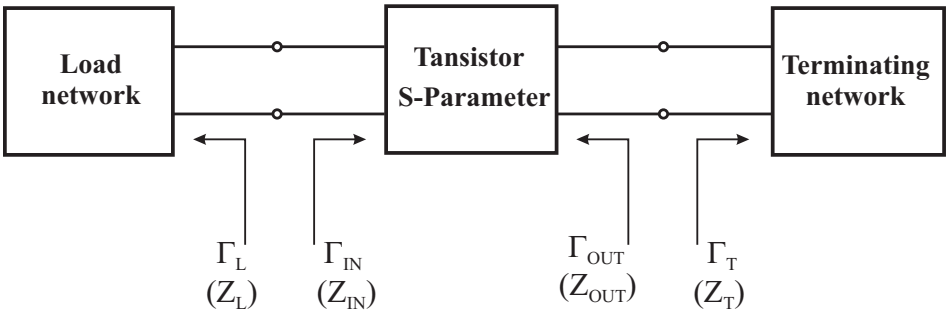


Figure 4.6: S-parameter description of a negative resistance oscillator.

The input and output reflection coefficient of the transistor network related to its S-parameters and the corresponding termination impedances are given by [14]:

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_T}{1 - S_{22}\Gamma_T} \tag{4.19}$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{11}\Gamma_L} \tag{4.20}$$

Substituting equation (4.19) into (4.18) and with $\Delta S = S_{11}S_{22} - S_{12}S_{21}$, Γ_T can be expressed as:

$$\Gamma_T = \frac{1 - S_{11}\Gamma_L}{S_{22} - \Delta S\,\Gamma_L} \tag{4.21}$$

Furthermore, equation (4.20) can be rewritten as follows:

$$\Gamma_{OUT} = \frac{S_{22} - \Delta S\Gamma_L}{1 - S_{11}\Gamma_L} \tag{4.22}$$

The multiplication of equation (4.21) and (4.22) results in

$$\Gamma_{OUT}\Gamma_T = 1 \tag{4.23}$$

which confirms the fulfillment of the oscillation condition at the second port of the oscillator system.

4.2.3 Loop Gain Method

The loop gain method, as indicated by its name, is based on the definition of a loop gain G_L for NR oscillators. As already mentioned in sec. 4.1, amplifier and feedback network in NR oscillators merge to a unique circuit, thus making impossible the derivation of a loop gain according to the classical oscillator concept. Nevertheless, by applying the so called virtual ground principle (cf. [1], [2], [3], and [4]), it is possible to reshape the NR oscillator architecture in such a way that a loop gain can be defined.

The virtual ground principle attests that, in an oscillator circuit considered in its small-signal operation mode, a virtual ac-ground can be placed in any point in the circuit without affecting its electrical behavior. The virtual ground point is independent of the physical ground position. Referring to the NR oscillator in Figure 4.4, it is preferable to set the virtual ground at the emitter of the amplifier transistor, thus allowing a clear distinction of the resonator in the oscillator circuit. In this way, a suitable transmission model for analysis is defined.

The application of the aforementioned virtual ground method to the NR oscillator according to Figure 4.4 results in the oscillator configuration presented in Figure 4.7. Latter shows an amplifier or a transistor in emitter-grounded configuration, whereas its collector output is fed back to its base input through a feedback network composed of the load impedances Z_C, Z_E, and Z_B. In this way, the loop gain G_L can be defined as the

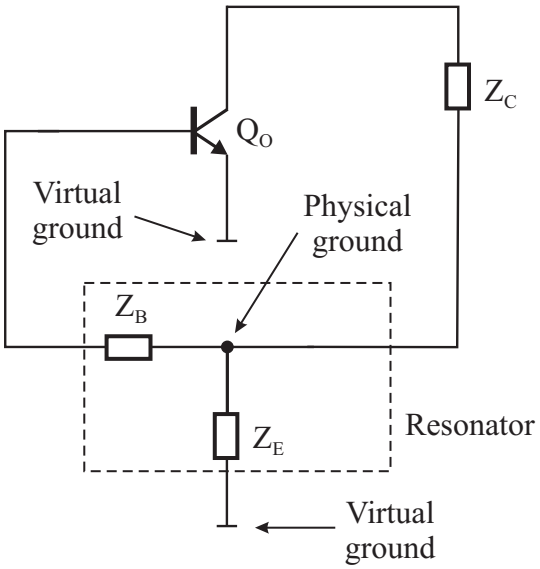


Figure 4.7: Description of the NR oscillator in a feedback topology using the virtual ground method.

product of the transistor transfer function g_m and the transfer function of the feedback network $k(j\omega)$:

$$G_L(j\omega) = g_m \cdot k(j\omega) \tag{4.24}$$

Since the input quantity of the amplifier transistor is the base emitter voltage U_{BE} and its output quantity the collector current I_C, the corresponding transfer function g_m is uniquely defined by the transconductance of the transistor. Furthermore, the transfer function of the feedback network can be expressed as:

$$k(j\omega) = \frac{U_{BE}}{I_C} \tag{4.25}$$

Similar to equation (4.7) and (4.8), the conditions for steady state oscillations are:

$$\mid G_L(j\omega) \mid = 1 \tag{4.26}$$

and

$$\varphi(G_L) = arg[G_L] = n \cdot 360^\circ \; with \; n \; = \; 0, 1, 2... \tag{4.27}$$

For oscillations to start, the magnitude of the loop gain $\mid G_L \mid$ has to be greater than 1. In this case, the output signal amplitude of the oscillator shows an exponential rising up to the overdriving of the amplifier. In this state, $\mid G_L \mid$ drops to a value of 1, thus resulting in a constant output signal amplitude.

From the phase $\varphi(G_L)$ of the loop gain, the so-called loaded quality factor Q_L of the oscillator, for small-signal consideration, can be derived to:

$$Q_L = \frac{\omega_0}{2} \left. \frac{d\varphi(G_L)}{d\omega} \right|_{\varphi=0} \tag{4.28}$$

whereas $\varphi(G_L)$ has the unity radian.

Q_L is a measure for the purity of the oscillator output signal. In other words, it is part of the determination quantities of the oscillator phase noise.

4.2.4 Choice of a Design and Analysis Method

The afore presented design and analysis methods (sec. 4.2.1 - sec. 4.2.3) proved their suitability for determining the oscillation tendencies of NR oscillator circuits. Therefore, explicit oscillation conditions are defined for each approach, thus allowing to obtain the resulting frequency of oscillation, as far as the oscillation conditions are satisfied. However, the loop gain method gives a better insight into the oscillator operation, since it enables a clear separation between the amplifier and the resonator of the oscillator circuit. Thus, the influence of each of these components on the overall circuit behavior can be studied separately. Furthermore, the possibility of determining the loaded quality factor Q_L points out the suitability for a deep oscillator analysis. Therefore, the loop gain method is the approach of choice for small-signal considerations of the NR oscillator.

Small-signal simulations are performed by using the Agilent simulator ADS. In this simulator, a special tool is available for the simulation of the frequency dependent loop gain of NR oscillators. In this way, a reshaping of the whole oscillator circuit only for loop gain simulations, as required by the virtual ground method, is avoided. In this work, the latter method is however applied for analytical calculations and considerations of the NR oscillator, reshaped in a feedback topology.

As already mentioned, the conditions for oscillation start-up are fully taken into account by small-signal considerations. For an accurate characterization of steady state oscillations, i.e., precise determination of the oscillation frequency as well as the output signal amplitude, the small-signal simulations must be completed by their large-signal counterpart. Namely, the behavior of oscillators in their steady state is mainly defined by their large-signal performance. The large-signal characterization is performed in form of transient and harmonic balance simulations. As for the small-signal simulations, the used simulator is further on ADS.

4.3 Phase Noise

4.3.1 General Description

The output signal of an ideal oscillator has been expressed by equation (4.1). However, due to the circuit and system noise in practical oscillators, the amplitude and phase of the output signal are no more constant, but time dependent. Therefore, equation (4.1) must be rewritten as in the following:

$$v_{out}(t) = V(t) \cdot cos(\omega_0 t + \varphi(t)) \tag{4.29}$$

$V(t)$ and $\varphi(t)$ are stochastical quantities with the respective expected value $\mathrm{E}V(t) = V_0$ and $\mathrm{E}\varphi(t) = \varphi_0$, whereas V_0 and φ_0 are the amplitude and the phase of the noiseless signal, respectively. $V(t)$ is referred to as amplitude noise, while $\varphi(t)$ is called phase noise. Thus, the period (or the frequency) of $v_{out}(t)$ is modulated by the random phase noise component $\varphi(t)$.

In well-designed and stable oscillator circuits, since the corresponding amplifier operates in a limiting mode, amplitude fluctuations of the oscillator output signal are held very low. As a consequence, the amplitude $V(t)$ can be considered as time independent, i.e., $V(t) = V_0$. Furthermore, the phase noise component $\varphi(t)$ is assumed to be a sinusoidal frequency modulation of the oscillator signal, with ω_m as the modulation frequency. Thus, equation (4.29) can be rewritten as:

$$v_{out}(t) = V_0 \cdot cos\left(\omega_0 t + \frac{\Delta\omega}{\omega_m} sin(\omega_m t)\right) \tag{4.30}$$

where $\Delta\omega$ is the peak frequency deviation and $\theta_p = \frac{\Delta\omega}{\omega_m}$ is the peak phase deviation, also referred to as the modulation index β. Equation (4.30) can be expanded as:

$$v_{out}(t) = V_0 \left[cos(\omega_0 t)\, cos(\theta_p\, sin\, \omega_m t) - sin(\omega_0 t)\, sin(\theta_p\, sin\, \omega_m t)\right] \tag{4.31}$$

Assuming a very small peak phase deviation, i.e., $\theta_p \ll 1$, the following expressions are valid:

$$cos(\theta_p\, sin\, \omega_m t) \approx 1$$

and

$$sin(\theta_p\, sin\, \omega_m t) \approx \theta_p\, sin\, \omega_m t$$

Thus, for $\theta_p \ll 1$, equation (4.31) can be simplified to the expression:

$$\begin{aligned} v_{out}(t) &= V_0 \left[cos(\omega_0 t) - \theta_p\, sin(\omega_0 t)\, sin\, \omega_m t)\right] \\ &= V_0 \left\{cos(\omega_0 t) - \frac{\theta_p}{2}[cos(\omega_0 + \omega_m)t - cos(\omega_0 - \omega_m)t]\right\} \end{aligned} \tag{4.32}$$

Interpreting equation (4.32), the output spectrum of a practical oscillator is composed of an impulse at the carrier frequency ω_0, which is symmetrically broadened around ω_0 due to additional frequency components induced by the phase noise component $\varphi(t)$. The amplitude of these frequency components is given by $\frac{\theta_p}{2}$. These interpretations are illustrated in Figure 4.8.

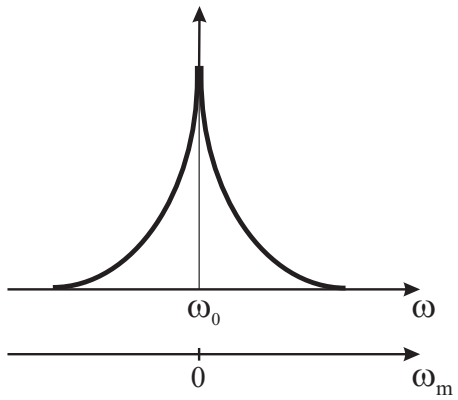


Figure 4.8: Output spectrum of a practical oscillator.

4.3.2 Phase Noise Characterization

As revealed in the previous section, the phase noise of an oscillator output signal results in symmetrical sidebands around the original impulse at the frequency ω_0, considering the output spectrum. That is, the output signal features a finite energy at frequencies ($\omega_0 \pm \omega_m$) relatively close to the carrier. Thus, at a specified frequency interval ω_m away from ω_0, the measured energy or the corresponding determined power in a 1 Hz bandwidth gives the power spectral density of the phase noise (Figure 4.9). The frequency ω_m is also referred to as the offset frequency. An universal statement of the power spectral density of the phase noise, regarding different oscillators in their performance, is achieved by normalizing the measured power (in 1 Hz at ω_m) to the carrier power at ω_0. Thus, measuring the carrier signal amplitude V_0 as well as the noise amplitude V_n at the offset frequency ω_m, the ratio of noise power to carrier power referred to 1 Hz bandwidth gives the single sideband phase noise:

$$\pounds(\omega_m) = \left(\frac{V_n}{V_0}\right)^2 \tag{4.33}$$

According to equation (4.32), equation (4.33) can be rewritten as:

$$\pounds(\omega_m) = \frac{\theta_p^2}{4} = \frac{\theta_{rms}^2}{2} \tag{4.34}$$

The normalization of the power spectral density of the phase noise with respect to the carrier is usually emphasized by using the unit [dBc/Hz], resulting from the formula:

$$\pounds(\omega_m) = 10\, log(\pounds(\omega_m))\ [dBc/Hz] \tag{4.35}$$

where the unit [dBc/Hz] denotes decibels related to the carrier in a 1 Hz bandwidth.

The total phase noise is determined by the phase noise in both sidebands as follows:

$$S_\varphi(\omega_m) = 2\pounds(\omega_m) \tag{4.36}$$

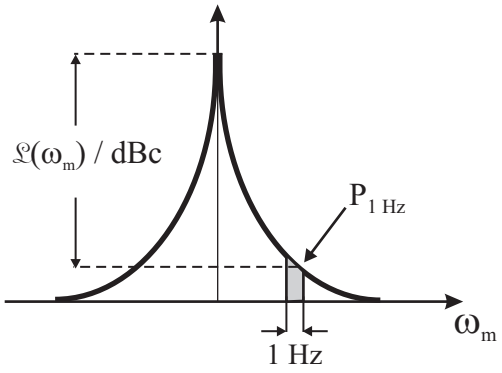


Figure 4.9: Phase noise characterization of the oscillator output spectrum.

Since the power spectrum of the phase noise features symmetrical sidebands around ω_0, the characterization of the corresponding phase noise is uniquely achieved by considering one sideband.

A deep insight into the generation mechanisms of the phase noise in oscillators is given by the extended Leesons formula [39], [65]. Its expression is given as follows:

$$\mathcal{L}(\omega_m) = 10\,log\left[\frac{1}{2}\left(1+\frac{1}{\omega_m^2}\left(\frac{\omega_0}{2Q_L}\right)^2\right)\left(1+\frac{\omega_c}{\omega_m}\right)\frac{Fk_BT}{P_{sav}}\right] \tag{4.37}$$

Interpreting equation 4.37, two types of noise originating from the oscillator amplifier are mainly responsible for the phase noise generation in the oscillator system: the white noise and the flicker noise. These noise components are translated to the sidebands of the oscillator output spectrum through mixing and modulation processes as well as additive superposition with the carrier signal. Their form of appearance in the oscillator circuit is shortly discussed in the following.

White noise

The contribution of the white noise on the oscillator phase noise performance is expressed in equation (4.37) by the term

$$S_\varphi(\omega_m) = \frac{Fk_BT}{P_{sav}} \tag{4.38}$$

which represents the spectral power density of the induced phase perturbation, due to this white noise. In other words, the white noise contribution is given by the ratio of noise power per unit bandwidth (Fk_BT) to signal power at the resonator output (P_{sav}). The factor F represents the noise figure of the oscillator amplifier, while k_B is the Boltzmann constant and T the temperature in the unit Kelvin.

The white noise in the oscillator amplifier originates from two components: on the one hand, it is due to the thermal noise of the corresponding path resistances within the amplifier. On the other hand, the white noise results from the shot noise due to the charge carrier pass through the semiconductor junctions. The spectral power density of

the thermal noise and that of the shot noise are given by equation (4.39) and (4.40), respectively.

$$S_{th}(\omega_m) = 4k_B T R \tag{4.39}$$

$$S_s(\omega_m) = 2qI \tag{4.40}$$

In equation (4.40), the factor q represents the electron charge, while I is the current through the semicondutor junction.

According to the equations (4.38), (4.39), and (4.40), the white and high-frequency noise originating from the oscillator amplifier results similarly in an uniformly distributed high-frequency phase noise at the oscillator output.

Flicker noise

An allowance for the flicker noise impact on the oscillator phase noise performance is considered in equation (4.37) with the term

$$\left(1 + \frac{\omega_c}{\omega_m}\right)$$

which represents the dependence of the flicker noise on the offset frequency ω_m. The frequency ω_c stands for the so called flicker corner frequency, over which the flicker noise exerts no more influence on the overall oscillator phase noise performance.

The flicker noise is due to the low-frequency noise of the active semiconductor device in the oscillator amplifier. Within this semiconductor device, so called surface and bulk effects are responsible for the low-frequency noise generation. While surface effects are caused by the interaction between the charge carriers and the semiconductor surface traps, thus resulting in a generation-recombination noise, bulk effects are due to the fluctuation of the charge carrier mobility.

Generally, the spectral power density of the flicker noise can be expressed as

$$S_{1/f}(f) = \frac{C}{f^\gamma} \tag{4.41}$$

where f is the frequency of measurement. The parameter C depends on material, scattering mechanism, and device operation conditions. Since the exponent γ is close to unity ($0.8 < \gamma < 1.2$), the flicker noise is also referred to as the 1/f-noise.

The white and flicker noise signal at the oscillator output, originating from the oscillator amplifier, are fed back to the input of this amplifier through the resonator. Therefore, the transfer function of the resonator has to be considered in the definition of the oscillator phase noise. This is achieved in equation (4.37) with the term

$$|k(\omega_m)|^2 = 1 + \frac{1}{\omega_m^2}\left(\frac{\omega_0}{2Q_L}\right)^2 \tag{4.42}$$

where $k(\omega_m)$ represents the resonator transfer function related to the offset frequency.

The parameter Q_L represents the loaded quality factor (loaded Q) of the resonator, as already introduced in sec. 4.2.3. In small-signal considerations of the oscillator circuit, the loaded quality factor of the resonator describes, according to equation (4.28), the slope of the phase of the loop gain at frequencies close to ω_0. Thus, the higher this slope, the higher the frequency stability of the oscillator circuit with respect to arising phase fluctuations. This is for the benefit of a good oscillator phase noise performance.

Since the steady state operation of the oscillator is mainly described by its large-signal behavior, a definition of the loaded quality factor using large-signal parameters proves to be meaningful. Thus, similar to [65], the loaded Q of the resonator can be defined as follows:

$$Q_L = \frac{Reactive\ power\ in\ the\ resonator}{Total\ dissipated\ power\ in\ the\ resonator} = \frac{\omega_0 W_e}{P_{in} + P_{res} + P_s} \tag{4.43}$$

where W_e is the reactive energy stored in the LC resonator. P_{in}, P_s, and P_{res} represent the input and output power of the amplifier as well as the power dissipated in the resonator, respectively. The following equations are valid:

$$W_e = \frac{1}{2} CV^2 \tag{4.44}$$

$$P_{res} = \frac{\omega_0 W_e}{Q_{unloaded}} \tag{4.45}$$

where the parameter V in equation (4.44) represents the signal amplitude in the resonator, while $Q_{unloaded}$ in equation (4.45) is the quality factor for an unloaded resonator.

The typical impact of the aforementioned noise sources on the power spectrum of the oscillator circuit is illustrated in Figure 4.10 ([18], [30]). The observed roll off is consistent with the phase noise behavior described in equation (4.37).

Phase noise simulations are performed using the simulator ADS. The underlying noise model is derived by this simulator using the afore mentioned noise sources, which are considered in the UCSD device model.

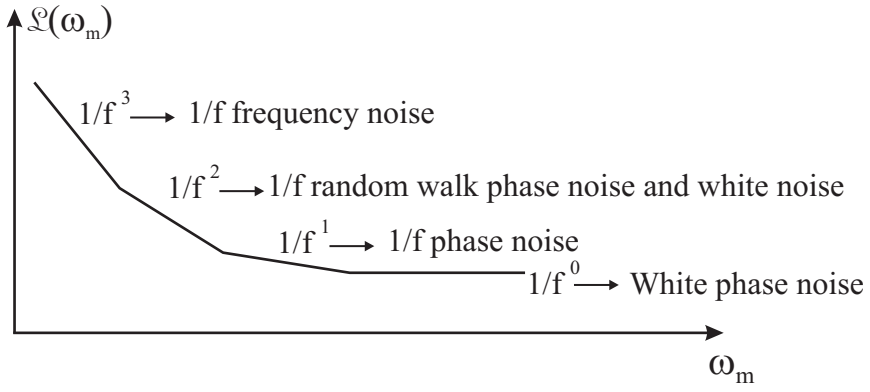


Figure 4.10: Typical run of an oscillator single sideband phase noise.

4.4 Circuit Design and Realization

4.4.1 Circuit Concept

LC oscillators of negative resistance type represent the underlying concept for the designed oscillator circuits, as already mentioned in sec. 4.1. Based on the schematic circuit diagram of Figure 4.4, a NR oscillator is realized by implementing the impedance Z_B as an inductance L_B, while the impedance Z_E is realized as a capacitor C_{VAR} (Figure 4.11). This capacitor acts as the destabilizing element of the oscillator system. In other words, C_{VAR} helps generating the negative resistance at the base of the oscillation transistor Q_O.

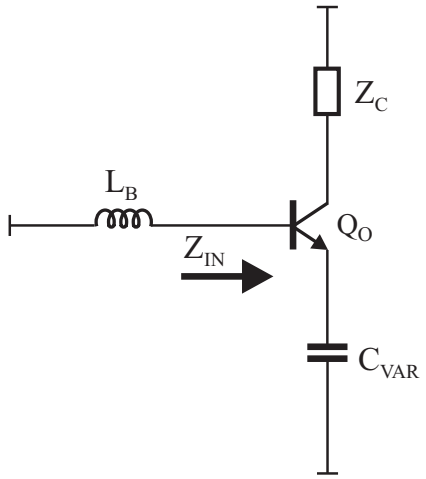


Figure 4.11: Circuit concept of a NR oscillator.

The analytical determination of the oscillation conditions using the loop gain method described in sec. 4.2.3 requires the reshaping of the circuit in Figure 4.11 according to the virtual ground principle. At the same time, the oscillation transistor Q_O has to be replaced by its small-signal equivalent circuit, thus allowing to obtain the oscillation conditions in relation with the transistor electrical parameters. For this small-signal equivalent circuit, the so called Π-configuration is preferred to its T-configuration counterpart, since it features parameters commonly used for the transistor characterization in common emitter operation mode (e.g.: common emitter current gain β). The corresponding small-signal schematic diagram is shown in Figure 4.12(a) [67]. The extrinsic and intrinsic collector-base capacitance are resumed to a single capacitance C_{CB}. The same is performed for the corresponding base, emitter and collector resistance to obtain the single resistances r_B, r_E, and r_C, respectively. Furthermore, the resistances r_{be}, r_{bc}, and r_{ce} are neglected because of their high values compared to the resistance value of the corresponding parallel capacitance.

In a first order of approximation, the analytical expressions for the oscillation conditions are calculated by neglecting the transistor internal feedback from the collector output to the base input. That is, the capacitance C_{CB} is out of consideration (Figure 4.12(b)).

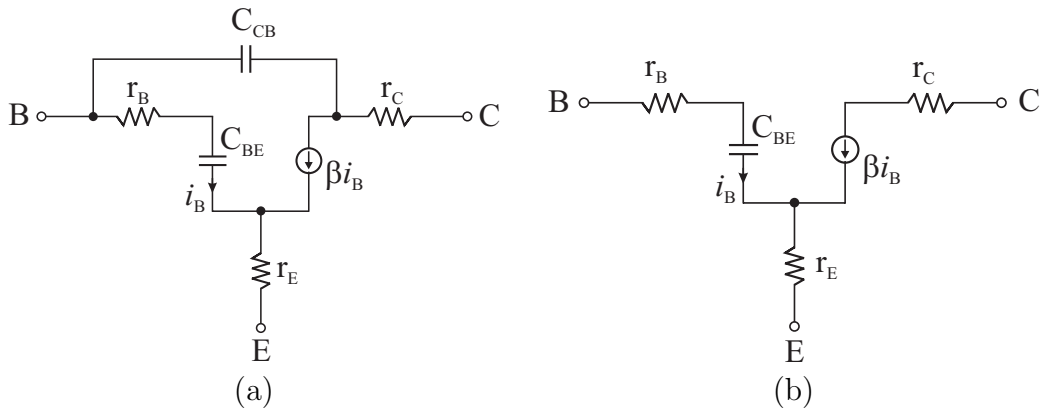


Figure 4.12: Π-type transistor small-signal equivalent circuit used for analytical investigations of the VCO: (a) Consideration of the collector-base capacitance C_{CB}, (b) Neglect of C_{CB} for the sake of calculation simplicity.

By applying the small-signal equivalent circuit of Figure 4.12(b) in the oscillator circuit of Figure 4.11, and then reshaping the circuit according to the virtual ground principle, the oscillator circuit of Figure 4.13 is obtained.

The (frequency dependent) transistor current gain β features a low-pass behavior ([63], [71]) and can be expressed as

$$\beta(j\omega) = \frac{\beta_{DC}}{1 + j\frac{\omega}{\omega_\beta}} \tag{4.46}$$

where β_{DC} is the dc current gain and ω_β the 3dB cut-off frequency of $\beta(j\omega)$.

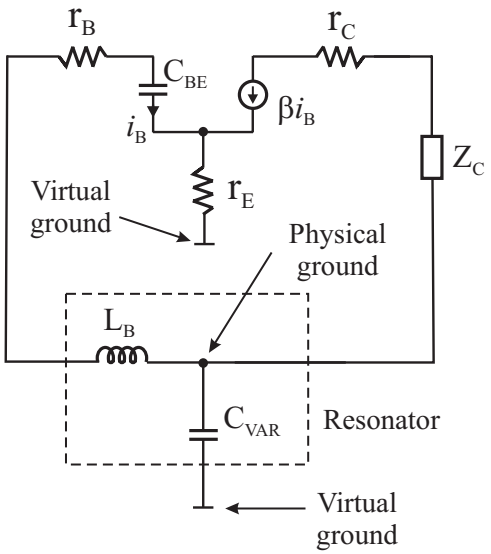


Figure 4.13: Reshaped NR oscillator using the virtual ground method. The transistor is replaced by its simplified small-signal equivalent circuit according to Figure 4.12(b).

At the considered millimeterwave operation frequencies, the expression

$$\frac{\omega}{\omega_\beta} \gg 1$$

is valid and with the transistor cut-off frequency ω_T given by the term

$$\omega_T = \beta_{DC}\,\omega_\beta = \frac{g_m}{C_{BE}}, \tag{4.47}$$

the current gain arises to:

$$\beta(j\omega) \approx \frac{\omega_T}{j\omega} = \frac{g_m}{j\omega C_{BE}} \tag{4.48}$$

Referring to equation (4.25), the transfer function $k(j\omega)$ of the resonator can be found to be:

$$k(j\omega) = \frac{-\frac{1}{j\omega C_{BE}}}{(1-\omega^2 L_B C_{VAR} + \frac{C_{VAR}}{C_{BE}}(1+g_m r_E)) + j\omega C_{VAR}(r_B + r_E)} \tag{4.49}$$

Thus, the loop gain $G_L(j\omega)$ arises to:

$$G_L(j\omega) = \frac{g_m\,(-\frac{1}{j\omega C_{BE}})}{(1-\omega^2 L_B C_{VAR} + \frac{C_{VAR}}{C_{BE}}(1+g_m r_E)) + j\omega C_{VAR}(r_B + r_E)} \tag{4.50}$$

The fulfillment of the phase condition for oscillation startup, as defined in equation (4.27), is ensured if the denominator of G_L in equation (4.50) shows a phase of $\frac{\pi}{2}$ as in the numerator. That is, the real part in the denominator of G_L must vanish:

$$(1-\omega^2 L_B C_{VAR} + \frac{C_{VAR}}{C_{BE}}(1+g_m r_E)) = 0 \tag{4.51}$$

From equation (4.51), the oscillation frequency ω_0 can be found to be:

$$\omega_0 = \sqrt{\frac{1}{L_B}\left(\frac{1}{C_{VAR}} + \frac{1}{C_{BE}} + \omega_T r_E\right)} \tag{4.52}$$

Since $\omega_T r_E \ll \frac{1}{C_{VAR}} + \frac{1}{C_{BE}}$, ω_0 can be approximated as

$$\omega_0 \approx \sqrt{\frac{1}{L_B}\left(\frac{1}{C_{VAR}} + \frac{1}{C_{BE}}\right)} \tag{4.53}$$

At the oscillation frequency, the amplitude condition according to equation (4.26) must be satisfied. By applying this condition in the expression of equation (4.50), the following equation is obtained:

$$\mid G_L(\omega) \mid = \frac{g_m}{\omega^2 C_{BE} C_{VAR}(r_B + r_E)} = \frac{\omega_T}{\omega^2 C_{VAR}(r_B + r_E)} = 1 \tag{4.54}$$

From equation (4.54), the amplitude condition for steady-state oscillation is given by the relation

$$r_B + r_E - \frac{\omega_T}{\omega^2 C_{VAR}} = 0 \tag{4.55}$$

which means that the net resistance in the oscillator system is zero.

The term on the left of equation (4.55) represents the real part of the input impedance Z_{IN} of the transistor amplifier, which can be found using the negative resistance method.

The impact of the capacitance C_{CB} of the oscillation transistor is considered during numerical simulations. As demonstrated in Figure 4.14, this capacitance can be seen as part of the oscillator feedback circuit and therefore influences the oscillation performance. Furthermore, as a result of the consideration of C_{CB}, the load impedance Z_C is also transferred to the resonator of the oscillator circuit.

The inductance L_B is realized using a shorted coplanar transmission line. Unlike its counterpart in form of a microstrip line, the coplanar transmission line for inductance implementation in the used InP technology features the following advantages:

- The characteristic impedance shows a negligible sensitivity related to the variation of the thickness of the planarization element BCB as well as the substrate thickness. Therefore, the aimed inductance value is achieved with high precision, which is essential for meeting the targeted oscillation frequency.
- The electromagnetic coupling between proximate lines is very weak, due to the ground planes between these signal lines.
- On a same transmission path, the width of the signal line can be adjusted without modifying the characteristic impedance, by just readjusting the space between the ground planes.

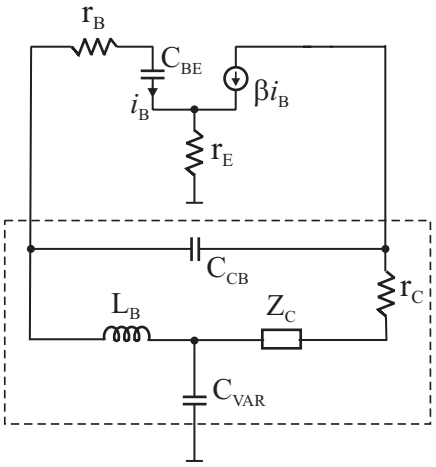


Figure 4.14: Reshaped NR oscillator using the virtual ground method. The transistor is replaced by its simplified small-signal equivalent circuit according to Figure 4.12(a).

For a shorted transmission line, the corresponding input impedance Z_{IN} is given by the relation

$$Z_{IN} = jZ_0 tan\left(2\pi\frac{l}{\lambda}\right) \tag{4.56}$$

where Z_0 is the characteristic impedance of the line, while l is the corresponding length and λ the wavelength. The line acts as an inductance as long as the correlation

$$l < \frac{\lambda}{4}$$

is valid. As a good compromise between the quality factor and the needed layout size of the transmission line, 70 Ω coplanar transmission lines are applied in the oscillator circuit.

Since the operation frequencies in the oscillator circuit have to be voltage controlled (therefore voltage controlled oscillator), the capacitor C_{VAR} is replaced by a so-called transistor varactor. In the latter component, the collector-base and base-emitter depletion capacitances of the corresponding transistor are shunted (Figure 4.15). Thus, the voltage dependence of the resulting total capacitance is used to tune the operation frequency of the oscillator.

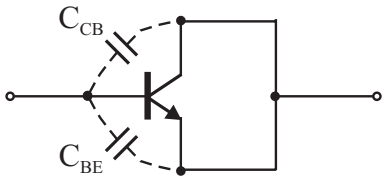


Figure 4.15: Varactor implementation by exploiting the voltage dependence of the transistor collector-base and base-emitter depletion capacitances.

4.4.2 Design Considerations for Low Phase Noise VCOs

In sec. 4.3.2, the generation mechanisms of phase noise in oscillator circuit have been described. Based on these acquired insights and referring to the oscillator concept of Figure 4.11, design considerations for minimizing the contribution of each noise source (or type) to the total oscillator phase noise are developed. Therefore, the circuit of Figure 4.11 is extended by ideal bias sources, except for the corresponding internal resistance and potentially parasitic capacitance. The resulting circuit is shown in Figure 4.16. Thus, the following actions are essential to get an oscillator with low phase noise behavior:

1. **Minimization of the flicker noise**: The amount of flicker noise, originating from the oscillation transistor Q_O, is given by the technology, on which the oscillator design is based. Therefore, the used InP-DHBTs prove to be suitable due to their inherent low flicker noise originating from their vertical transport characteristics [23].

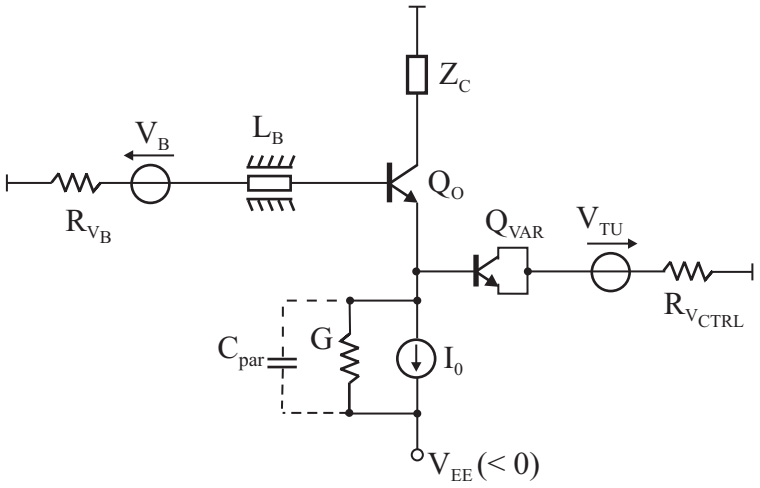


Figure 4.16: NR oscillator with ideal bias sources, except for the corresponding internal resistance and potentially parasitic capacitance.

2. **Maximization of the loaded quality factor** Q_L: According to the extended Leeson's relation in equation (4.37), Q_L of the resonator has a considerable influence on the oscillator phase noise performance, due to its exponent in the considered formula. Based on the definition of Q_L in equation (4.43), its maximization is achieved by the implementation of the following actions:

   - Maximization of the reactive energy within the resonator: The signal amplitude over the transmission line L_B or the varactor Q_{VAR} can be considered as a measure of the energy stored in the LC resonator. Thus, the maximization of the reactive energy in the resonator results in the maximization of the signal amplitude within the resonator. The limitation in this action arises, on the one hand, from the breakdown voltage level of the amplifier as well as the varactor transistor. On the other hand, the limitation results from the saturation voltage level of the amplifier transistor.
   - Minimization of the power dissipation within the resonator: Essential for this purpose is the use of a coplanar line as well as a transistor varactor with smallest possible losses. Thus, in this way, the quality factor of the latter elements is maximized. Considering the varactor, since the base resistance of the corresponding transistor mainly represents the losses, relatively high emitter length with respect to the aimed operation frequency (due to the resulting higher varactor capacitance) is advantageous.
   - Minimization of the power dissipation at the resonator entry: This quantity is mainly given by the voltage signal generated over the load Z_C of the transistor amplifier. Thus, a load with minimal losses is required. An inductive acting element such as a transmission line might be adequate.

3. **Minimization of the high-frequency noise**: The high-frequency noise results from the thermal noise and the shot noise, both originating from the transistor amplifier, as already mentioned in sec. 4.3.2. Thus, a minimization of the high-frequency noise results in the following measures:

   - Minimization of the thermal noise within the amplifier: This noise is mainly given by the equivalent path resistances within the active semiconductor device. Especially, the base path resistance features an essential weight in the thermal noise generation. Therefore, a relatively high emitter length with respect to the aimed operation frequency might be advantageous.
   - Minimization of the shot noise: As described by the shot noise spectrum in equation (4.40), the current through the amplifier transistor is a cause of the generated shot noise. Thus, the reduction of this noise results in the minimization of the operation current of the amplifier transistor. Limitations in this action arise from the fulfillment of the amplitude condition and the maintenance of a high loaded Q. Namely, a reduction of the operation current results in a smaller loop gain magnitude as well as smaller signal amplitude within the resonator. However, since the loop gain is proportional to the transit frequency ω_T, a much higher ω_T compared to the operation frequency offers a wider operation margin, in which the operation current can be reduced. Thus, for a constant corner frequency ω_β of the current gain β, a high DC current gain is advantageous (cf. equation (4.47)).

4. **Minimization of frequency modulation effects**: The extended Leeson's formula does not account for the case of a voltage controlled oscillator. That is, there is no allowance for the operation frequency modulation due to the influence of the noise voltages on the voltage dependent capacitances in the oscillator circuit. These capacitances are represented by the equivalent varactor capacitor C_{VAR}, the collector-base capacitance of the amplifier transistor Q_O, and potentially, the parasitic capacitance C_{par} of the current source I_0. Thus, the frequency modulation can be minimized by the following actions:

   - Reduction of the noise voltage due to the thermal noise sources in the oscillator circuit: This measure results in the minimization of the path resistances within the transistor amplifier and the varactor, especially the base path resistance. Furthermore, the equivalent internal resistance of the bias voltage sources as well as the transmission line losses have to be kept small.
   - Minimization of the tuning range of the voltage dependent capacitances: A relatively high dc voltage across the collector-emitter junction of the amplifier transistor keeps the corresponding collector-base capacitance at a relatively small value. Thus, the capacitance tuning due to noise voltages is kept small. However, special caution is necessary concerning the breakdown voltage level

of the transistor. Concerning the varactor, keeping the total capacitance small helps limiting the tuning effect of the noise voltages on this element.

4.4.3 Circuit Implementations

Based on the introduced oscillator concepts, the implementation of VCOs in the 43 GHz and 86 GHz frequency range is discussed in this section. The underlying circuit architecture is the so called differential topology. Unlike its single-ended counterpart, the differential topology features the following advantages:

- The supply of the clock signal is simplified due to the differential clock input of the driven circuits.
- The points in the symmetrical plane of a differential topology behave, for ac-signals, as a virtual ground. Thus, push-pull transmission lines can be grounded just by connecting their respective ends together. As a consequence, parasitic lines for grounding in the ground plane are avoided.
- The virtual ground eases the on- and off-chip decoupling of supply and bias voltage sources. Furthermore, these sources behave ideally, since their respective internal resistance vanishes into the virtual ground.
- On-chip noise generation, such as common mode noise, is substantially reduced.

The schematic circuit diagram of the differential VCO with ideal bias sources is shown in Figure 4.17. Due to the virtual ground in the symmetrical plane, the circuit part on the left and the right of the latter plane can be considered separately. Thus, the oscillation conditions defined in equations (4.26) and (4.27) are applicable to each circuit part. Analog oscillation conditions can be defined for the differential topology.

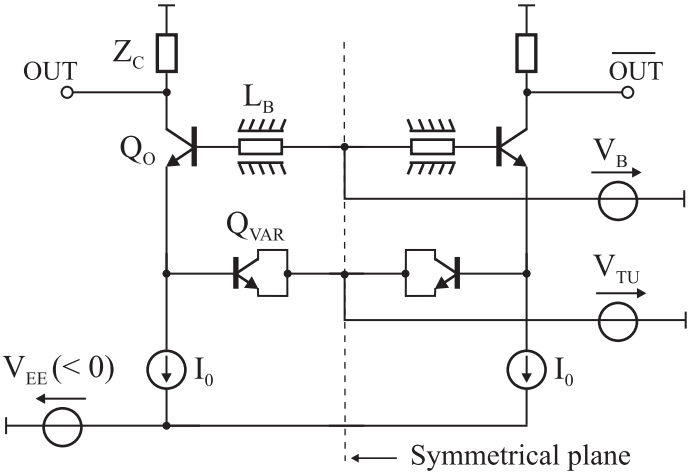


Figure 4.17: Schematic circuit diagram of the differential NR VCO with ideal bias sources.

Up to now, the current and voltage bias sources in the oscillator circuit have been considered, more or less, as ideal sources. Therefore, the next paragraphs describe the implementation of the actual bias sources, considering the different possibilities of realization.

Current Source

Two options for the realization of the current bias source are considered, as shown in Figure 4.18. On the one hand, the current source can be realized using a transistor current source in the so-called current mirror configuration (Figure 4.18(a)). With this configuration, a robust and stable current source is available. In fact, the magnitude of the current generated by the current source is almost independent of the load connected at its output. Furthermore, the current mirror topology offers the possibility of adjusting the bias current without modifying the voltage operation points in the circuit. This is done by connecting an external voltage source at the pad in Figure 4.18(a).

The output impedance of the transistor current source is mainly determined by the corresponding collector-base capacitance at its output. The latter capacitance might degrade the phase noise performance due to frequency modulation effects. Furthermore, a limitation of the frequency tuning range of the VCO is inevitable, since the varactor and the output capacitance of the current source are shunted, considering ac signals.

Beside the transistor current source, the second option for realizing the current source is shown to be a resistor current source (Figure 4.18(b)). Unlike its transistor counterpart, the resistor current source does not feature a capacitive output with the known disadvantages. However, since the current source resistance and the corresponding varactor capacitance are shunted, the loaded Q of the resonator is severely affected. Furthermore, the magnitude of the current delivered by the resistance current source depends on the dc potential induced by the source load.

Measuring the respective advantages and disadvantages of both mentioned current sources, the transistor current source proves to be more adequate for use and is consequently the applied type of current source. The mentioned negative influence of the

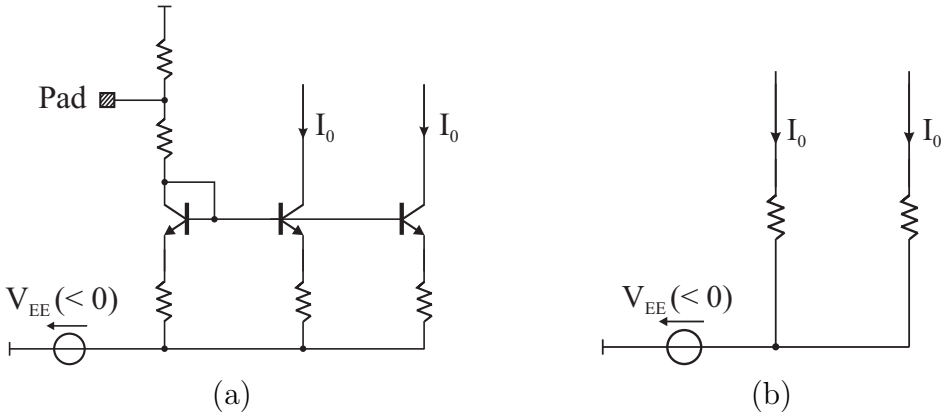


Figure 4.18: Circuit concepts for the implementation of a current source.

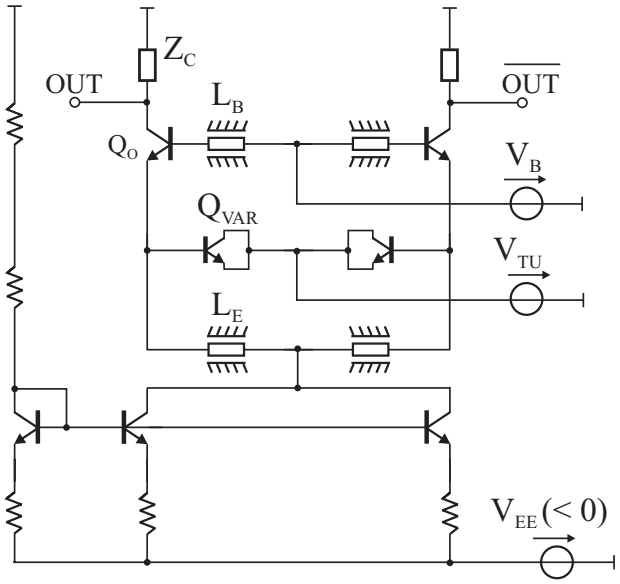


Figure 4.19: Schematic circuit diagram of the differential NR VCO. An additional transmission line L_E is set at the emitter of Q_0 to generate a virtual ground node at the bias current feed point.

collector-base capacitance on the oscillator performance can be eliminated by generating a virtual ground node at the current feed point of the VCO. Therefore, an additional transmission line and its complementary counterpart are added at the emitter of the oscillation transistors, whereas the end of these lines are connected together. This common point represents the current feed point and behaves at the same time as a virtual ground for ac-signals. The oscillator circuit arising from this measure is presented in Figure 4.19. The corresponding inductance of the transmission line L_E is designed to have an impedance much higher than the impedance of the equivalent varactor capacitance C_{VAR}. Thus, the influence of L_E on the resonator performance is very small, since L_E and C_{VAR} are shunted for small-signal considerations.

Voltage Source

Similar to the afore discussed realization of the current source, two options are considered for the implementation of the voltage sources in the oscillator circuit, as shown in Figure 4.20. The first option envisages a voltage source realization using the current mirror configuration (Figure 4.20(a)). Analog to the current source implemented in the latter configuration, the considered voltage source type features a robust and stable behavior. However, the relatively high output impedance of such a voltage source degrades the phase noise performance due to the induced high-frequency noise. Furthermore, as a result of the multiple voltage sources required in the oscillator circuit, the complexity of the VCO (related to the number of active devices) increases.

The second option, considered for the implementation of the voltage sources, is shown to

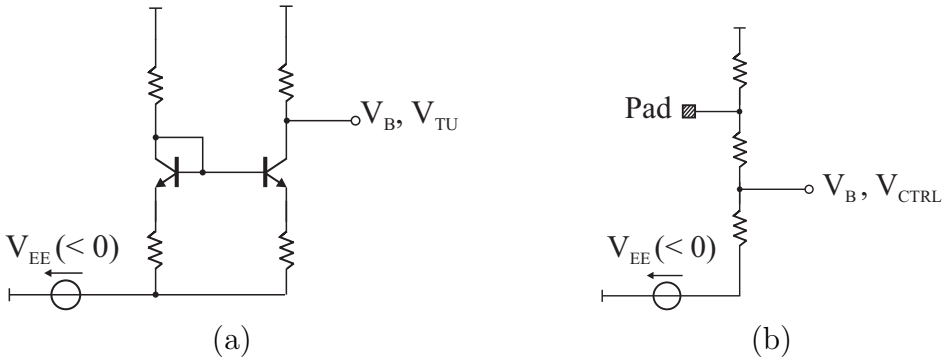


Figure 4.20: Circuit concepts for the implementation of a voltage source.

be a resistive voltage divider (Figure 4.20(b)). Using this voltage divider, the possibility of realizing of a voltage source with relatively small internal resistance is given. Furthermore, since no active device is used in the source, the complexity of the circuit is not affected. The generated bias voltage can be adjusted by connecting an external potentiometer at the represented pad.

By comparing the mentioned properties of both considered voltage source types, the resistive voltage divider proves to be more suitable for use as a voltage source in oscillator circuits.

The supply voltage V_{EE} in Figure 4.17 is connected off-chip. Therefore, no allowance for its implementation is required at this place.

Up to now, the implementation of the impedance Z_C has not been discussed. This impedance actually takes into account the collector load of the oscillation transistor, through which the output signal is generated. In addition, since the realized VCOs are measured as stand-alone circuits, the external load defined by the measurement environment is also included in Z_C. The latter load could induce negative impacts on the VCO circuit performance such as frequency discontinuities within the tuning range. Therefore, a decoupling stage between the VCO core and the external load is introduced in the oscillator circuit. Since the intended VCOs aim at different frequency ranges, different approaches are developped to realize the decoupling stage. The arising VCO circuits are discussed in the following.

43 GHz Voltage Controlled Oscillator

The implemented oscillator circuit for the 43 GHz operation range is shown in Figure 4.21. Unlike the VCO core represented in Figure 4.17, a fixed capacitor C_E is added in parallel to the base-emitter junction of the oscillation transistors (Q_O), respectively. As an additional energy storage element (regarding L_B and Q_{VAR}), C_E allows maximizing the total voltage swing across the resonator, thus minimizing the phase noise of the VCO.

The oscillation transistors are followed by a differential cascode stage, which acts as an output buffer. In fact, the characteristic small input impedance as well as the high output

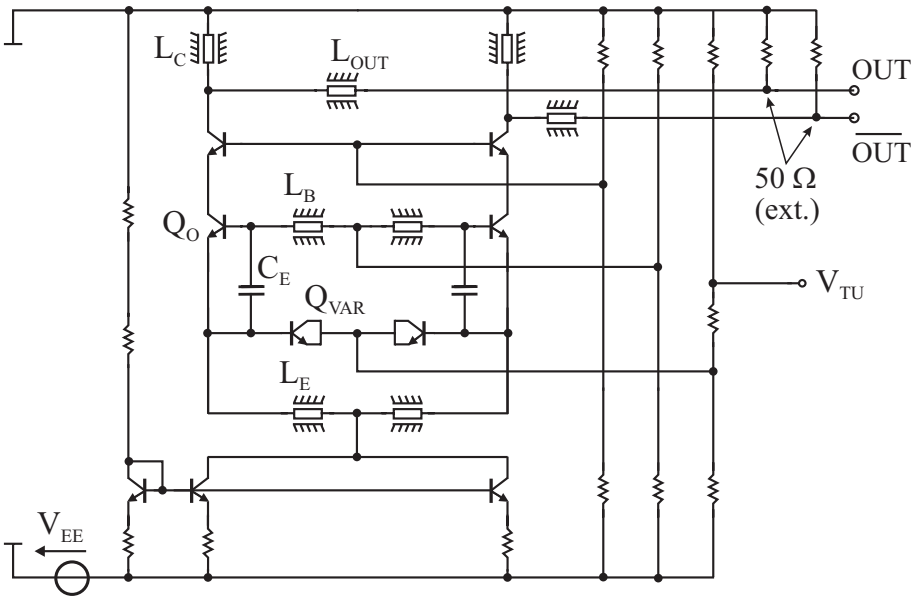


Figure 4.21: Schematic circuit diagram of the NR VCO targeting the 43 GHz operation range.

impedance of this cascode stage allow to restrain the external load pulling effect on the performance of the VCO core. The collector of the cascode stage transistors is respectively loaded by an inductive acting transmission line L_C. Unlike a resistive load at this place, the inductive load allows to realize a narrow band power matching, in collaboration with the output capacitance of the cascode transistors. Thus, for the same bias current, a relatively higher output power is obtained in the case of an inductive loading compared to the resistive loading counterpart.

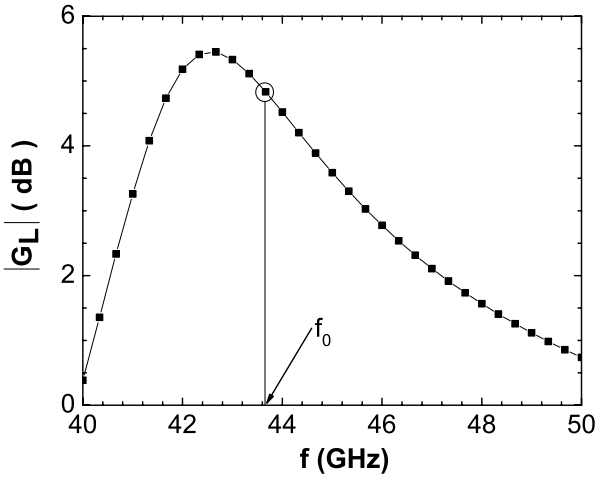
The transmission line L_{out} accounts for the connection line from the oscillator output to the output pads, where the 50 Ω load arising from the measurement system is connected. This external load is considered in the design by the connection of a 50 Ω resistor at the end of L_{out}.

The set bias current of the VCO core amounts to 14 mA. This is the result of a trade-off between relatively low bias current for smallest possible shot noise and relatively high bias current for maximal signal amplitude within the resonator as well as sufficiently high output power. For the oscillation and cascode transistors, HBTs with a total emitter size of $1 \times 16\,\mu\text{m}^2$ are used. The use of transistors with the maximal available emitter length allows to reduce the base resistance to a minimum, thus inducing a positive impact on the phase noise performance. The reverse voltage V_{VAR} across the used transistor varactor with a total emitter size of $1 \times 16\,\mu\text{m}^2$ can be varied between 0 V and 4 V. The arising capacitance ratio $C_{VAR}(V_{VAR} = 0V)/C_{VAR}(V_{VAR} = 4V)$ amounts to 2.

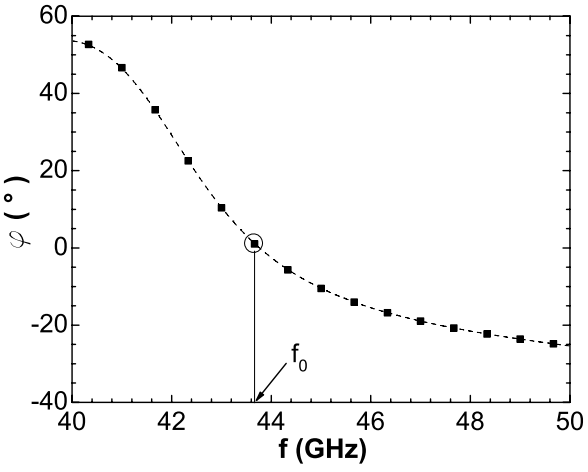
A typical run of the simulated loop gain magnitude and the corresponding phase as a function of frequency is shown in Figure 4.22(a) and Figure 4.22(b), respectively. At the oscillation frequency f_0, the magnitude of the loop gain $|G_L|$ is 5 dB. Thus, $|G_L|$ is high enough for oscillation to start, even under worst case conditions. Derived from the phase

$\varphi(G_L)$ of the loop gain, the run of the small-signal loaded Q vs. frequency is plotted in Figure 4.23. At the frequency f_0, a value of approximately 4 is obtained, which represents the loaded quality factor at the oscillation start-up.

Considering the saturation voltage of the oscillation transistors at the set bias current, the maximal adjustable signal amplitude over the transmission line L_B amounts to about 1 V. As already mentioned, the latter quantity serves as a measure of the energy stored in the resonator and is at the same time an indicator for the loaded quality factor under large-signal VCO operation. The amplitude over L_B can be adjusted by varying the corresponding length, whereas the resulting frequency variation is intercepted by a



(a)



(b)

Figure 4.22: Typical run of the simulated loop gain (a) and the corresponding phase (b) as a function of the frequency.

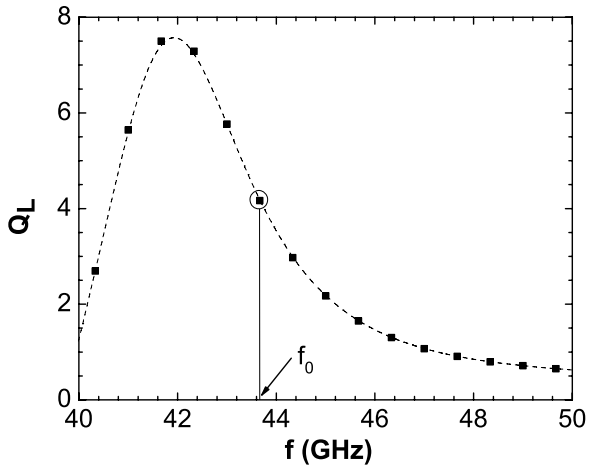


Figure 4.23: Frequency variation of the the small-signal loaded Q derived from the phase $\varphi(G_L)$ of the loop gain in Figure 4.22.

corresponding adjustment of the capacitance C_E, for a constant size of the varactor Q_{VAR}.

The chip photograph of the realized 43 GHz VCO is shown in Figure 4.24. The total chip size is 1.25×1.25 mm^2, while most of the area results from the bias and high-frequency measurement pads. The circuit features a complexity of 15 active elements.

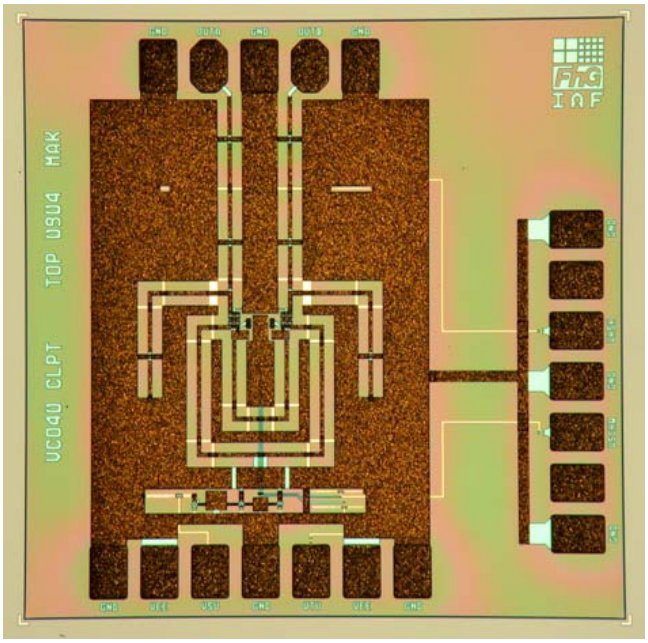


Figure 4.24: Chip photograph of the realized VCO targeting the 43 GHz operation range. The chip size is 1.25×1.25 mm^2.

86 GHz Voltage Controlled Oscillator

For the implementation of VCOs operating at W-band frequencies, an output buffer corresponding to the cascode stage applied in Figure 4.21 is not suited for use as isolation stage ([43], [45]). In fact, at such high frequencies, the decoupling effect ensured by the cascode stage between the VCO core and the external load is severely weak due to the more effective capacitive feedback from the collector output to the emitter input. This fact becomes more obvious by interpreting the small-signal equivalent circuit of the cascode transistor with the corresponding load. This small-signal equivalent circuit is shown in Figure 4.25, where the distributed form of the base-collector capacitance as well as the base path resistance is considered. Thus, the higher the operation frequency, the smaller the impedance value of the collector-base capacitances, which results in a stronger feedback.

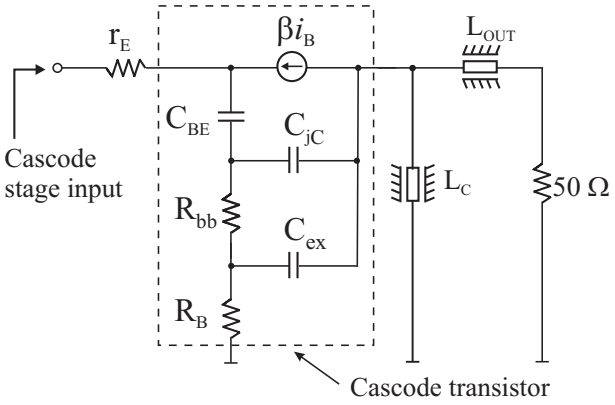


Figure 4.25: Small-signal equivalent circuit of the cascode stage with the corresponding load, according to the 43 GHz VCO circuit in Figure 4.21. The transistor small-signal equivalent circuit conforms to a Π-topology.

Figure 4.26 shows the schematic circuit diagram used for the VCO in the 86 GHz operation range. Unlike the resonator of the VCO core shown in Figure 4.21, the capacitance C_E, in this case, is not considered in order to boost the operation frequencies to the W-band. Furthermore, the emitter size of the oscillation transistors is reduced to $1 \times 8\,\mu m^2$, while the transistor varactor features a size of $1 \times 4\,\mu m^2$.

Similar to the oscillator circuit for the 43 GHz operation range, inductive loading (L_C) is applied at the collector side of the oscillation transistors in order to keep high the loop gain, as well as the loaded Q, and the signal swing within the resonator. As a consequence, a relatively high signal amplitude is available at the collector of Q_O. The saturation of the first stage of the output buffer is then avoided by an appropriate tapping of L_C, thus generating an inductive voltage divider (L_{C11}, L_{C12}). This voltage divider also allows alleviating the loading of the VCO core by the buffer input.

The ac-coupled output buffer in the topology of Figure 4.26 is composed, in the first stage, of an emitter follower pair. This emitter follower, with its characteristical high input as well low output impedance, represents the first decoupling unit of the output buffer. In a second stage, the output buffer consists of a differential, emitter-coupled transadmittance

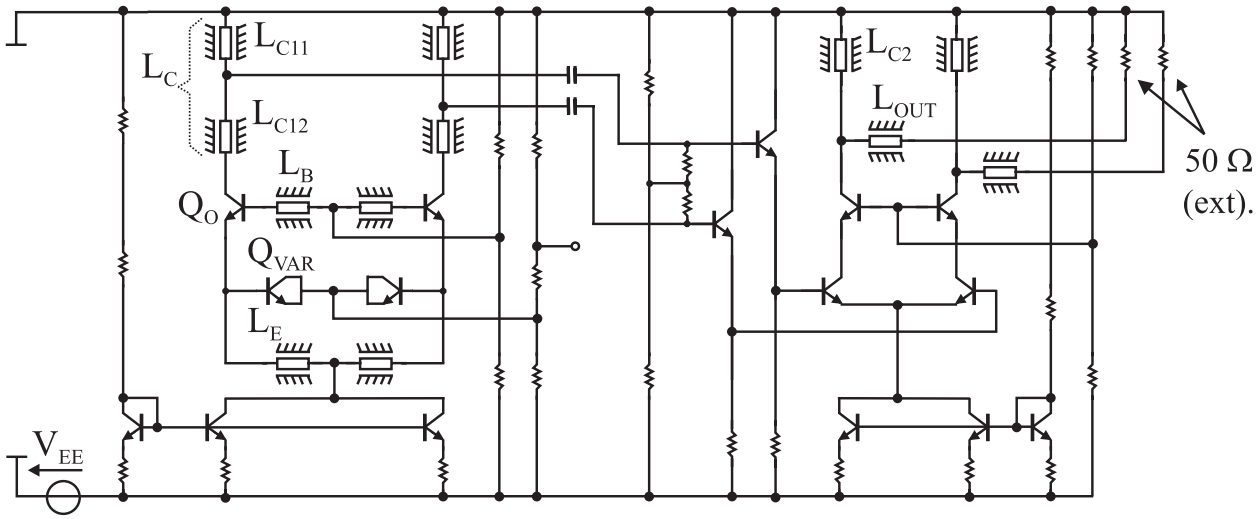
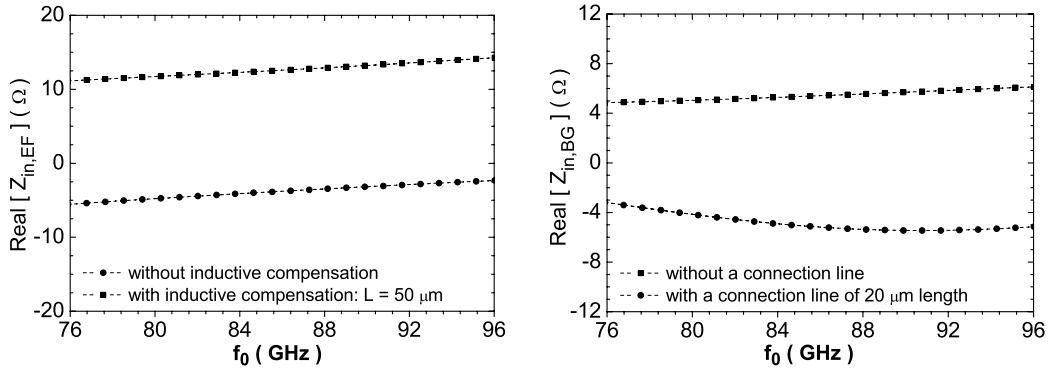


Figure 4.26: Schematic circuit diagram of the NR VCO targeting the 86 GHz operation range.

stage (TAS), which is then loaded by a base-grounded stage. The latter stage enforces the decoupling effect as well as the amount of achievable output signal amplitude, i.e. higher output power. Inductive loading (L_{C2}) is applied to further boost the output power by better output load matching at the frequency range of interest. The load at this point is completed by the transmission line L_{out} and the external 50 Ω load.

The total bias current through the oscillation transistors is adjusted to a minimal value of 10 mA, whereas the signal amplitude over L_B amounts to 0.8 V. Unlike the case encountered with the 43 GHz VCO, such a small bias current value is possible since the output power at the buffer output is not very critical for the setting of the current in the VCO core. In fact, the output buffer in the configuration of Figure 4.26 allows an adjustment of the output power without any consideration of the VCO core characteristics. That is, there is one parameter less for the minimization of the bias current through the transistor Q_O. However, the output buffer generates a current consumption, which is the triple of the VCO core consumption. Actually, in contrast to a stand-alone application of the VCO, the output buffer can be omitted if the VCO is part of a monolithically integrated circuit, thus avoiding the additional power consumption induced by the output buffer.

During the layout design of the output buffer, special attention is devoted to possible parasitic oscillations. Due to the inevitable parasitic inductances and capacitances in this output buffer, impedances with negative real part may be generated at several nodes. For instance, a parasitic inductance at the base of the base-grounded stage may cause a negative resistance at the emitter input. As another example, a negative resistance may occur at the base input of the emitter followers in the first stage, which are capacitively loaded by the differential amplifier input. Moreover, since the emitter followers are driven by an inductive source, a negative resistance can appear at the emitter output.



(a) (b)

Figure 4.27: Detection of possible parasitic oscillation in the output buffer by determining the real part of the input impedance $Z_{IN,EF}$ and $Z_{IN,BG}$ of the emitter follower and base-grounded stage, respectively.

Possible parasitic oscillations are detected by small-signal simulations of the impedance at the critical nodes, and then applying the negative resistance method according to sec. 4.2.1. Figure 4.27(a) shows the real part of the input impedance $Z_{IN,EF}$ of the emitter followers in the frequency range of interest. Negative values can be stated if no action is taken to suppress the effect of capacitive loading at the emitter output. An effective measure for the minimization of the capacitive loading effect is the connection of an inductively acting transmission line between the emitter follower output and the input of the differential amplifier stage. In this way, the amount of capacitance seen at the output of the emitter follower is reduced, thus shifting the real part of $Z_{IN,EF}$ to positive values. The latter effect is also shown in Figure 4.27(a), where a transmission line of 50 μm length is used.

Figure 4.27(b) shows the real part of the input impedance $Z_{IN,BG}$ of the base-grounded stage as a function of frequency. On the one hand, positive values are stated if no (transmission) line is set at the corresponding critical base node, which is valid only for an ideal output stage. On the other hand, the connection of a transmission line greater than 20 μm already induces negative resistance values at the emitter input. That is, tendencies to parasitic oscillations at this place are avoided by keeping the length of the base connection line as small as possible.

In the time domain, parasitic oscillations modulate the oscillator signal, thus making it useless for application. Therefore, a suppression of the latter oscillations is essential for a proper operation of the oscillator circuit. That is, all parasitics arising from the layout have to be considered during the circuit design process.

Figure 4.28 shows the chip photograph of the realized VCO aiming the 86 GHz frequency range. The total chip size is 1.25×1.25 mm^2, including the bias and high-frequency measurement pads. The circuit features a complexity of 21 active elements.

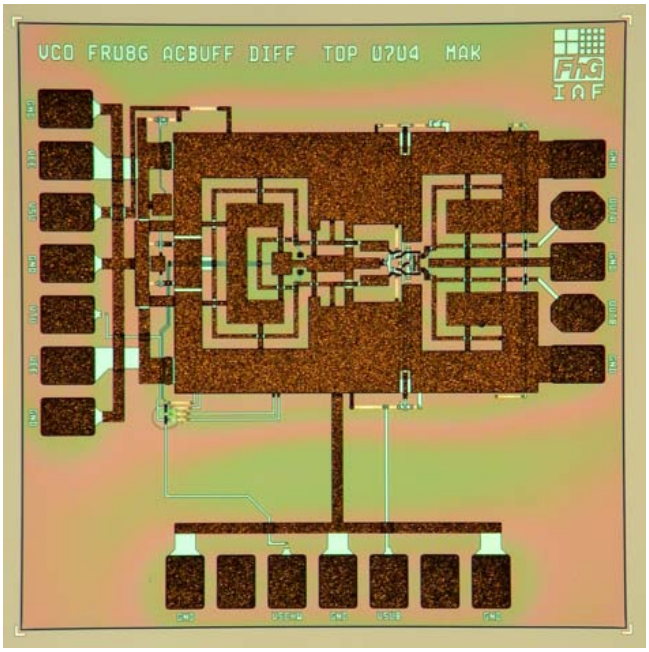


Figure 4.28: Chip photograph of the realized VCO targeting the 86 GHz operation range. The chip size is 1.25×1.25 mm^2.

4.5 Measurements

4.5.1 Measurement Setup

The measurements of the realized VCOs are performed on-wafer. Since both VCO types aim at different frequency bands, the measurement setups used for their respective characterization differ in high-frequency measurement components. For the 43 GHz VCO, the output signal is probed with cascade ACP65-D 50 Ω coplanar probes. Through a 2.4 mm coaxial cable, the tapped oscillator signal is led to a directional coupler, where it is split up for spectral measurements on the one side, and power measurement on the other side. Spectral measurements are performed using a spectrum analyzer (Agilent E448A) extended in frequency with a waveguide down mixer (HP 11970). This waveguide down mixer is connected to the coupler via a coaxial-to-waveguide adapter (HP Q281A), whereas the attenuated part of the high-frequency signal in the coupler is delivered to the mixer. Power measurements are performed by means of a calibrated power meter (HP 438A). The latter element is supplied with the undamped high-frequency signal through the coupler. Figure 4.29 illustrates the measurement setup used for characterizing the 43 GHz VCO.

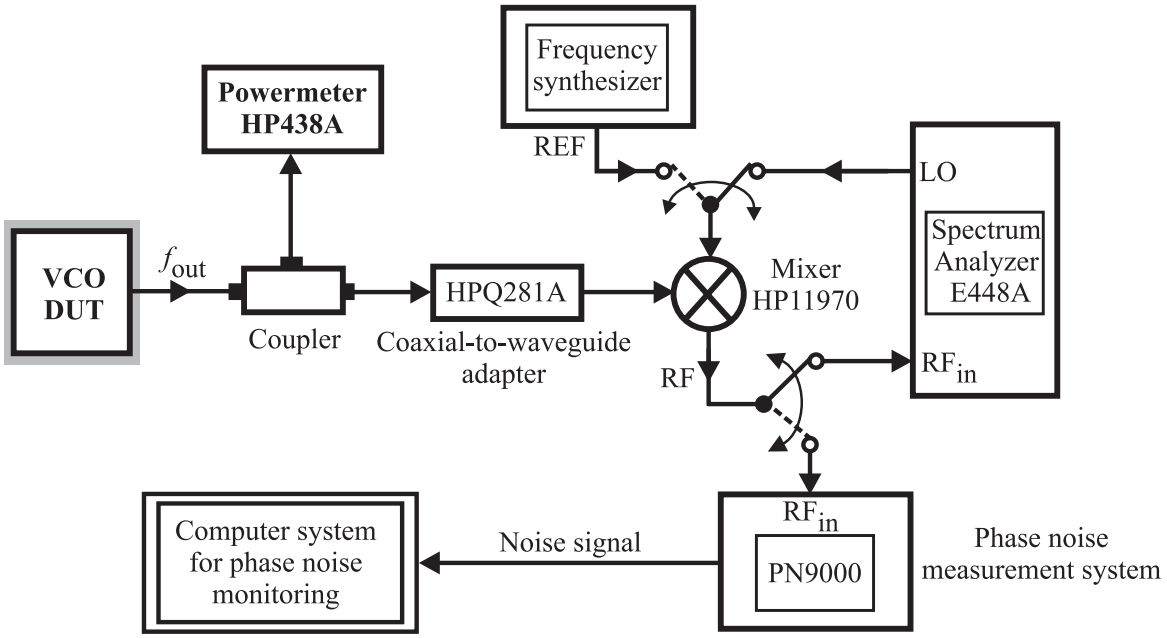


Figure 4.29: Measurement setup for characterizing the realized voltage controlled oscillators.

For the VCO aiming the 86 GHz operation range, Picoprobe W-band waveguide probes are used for probing the output signal. This signal is led, via the attenuated path of a waveguide coupler (HP W752C), to the aforementioned spectrum analyzer, which is extended in frequency by a waveguide down mixer (HP 11970W). Power measurements are performed using a calibrated waveguide power meter (HP W8486A). The high-frequency measurement signal is delivered by the undamped path of the coupler. The measurement setup used for characterizing the 86 GHz VCO is consistent with Figure 4.29, except for the components coupler, HP Q281A, HP 438A, and HP 11970. The latter components are replaced by the corresponding W-band counterparts, which are mentioned above.

Phase noise measurements, for both VCO types, are performed using a special measurement setup based on the delay line method [57]. This method allows accurate phase noise measurements on free running oscillators, unlike measurements directly performed with a spectrum analyzer. The measurement system used for the phase noise characterization is the Europtest PN9000 (see Figure 4.29). The reference signal (REF) necessary for performing the phase noise measurements is supplied by a frequency synthesizer.

4.5.2 Discussion of the Simulation and Measurement Results of the 43 GHz VCO

Figure 4.30(a) shows the simulated and measured operation frequencies as well as the corresponding output power of the 43 GHz VCO as a function of the tuning voltage V_{TU}. Thus, the measurements reveal that the VCO can be continuously swept from 39.65 GHz to 47 GHz by varying V_{TU} over 3 V (against V_{EE}). This corresponds to a VCO gain K_{VCO}

of 2.45 GHz/V. As shown in Figure 4.30(a), the simulated frequency tuning range agrees well with the measured one. The observed frequency deviation between simulation and measurement at the upper operation frequencies is less than 3% and is therefore negligible.

Within the tuning range, a measured output power up to 3 dBm is achieved for each of the two complementary outputs, resulting in a total signal power of 6 dBm. As for the frequency tuning, a good agreement between simulation and measurement results is also achieved regarding the output power.

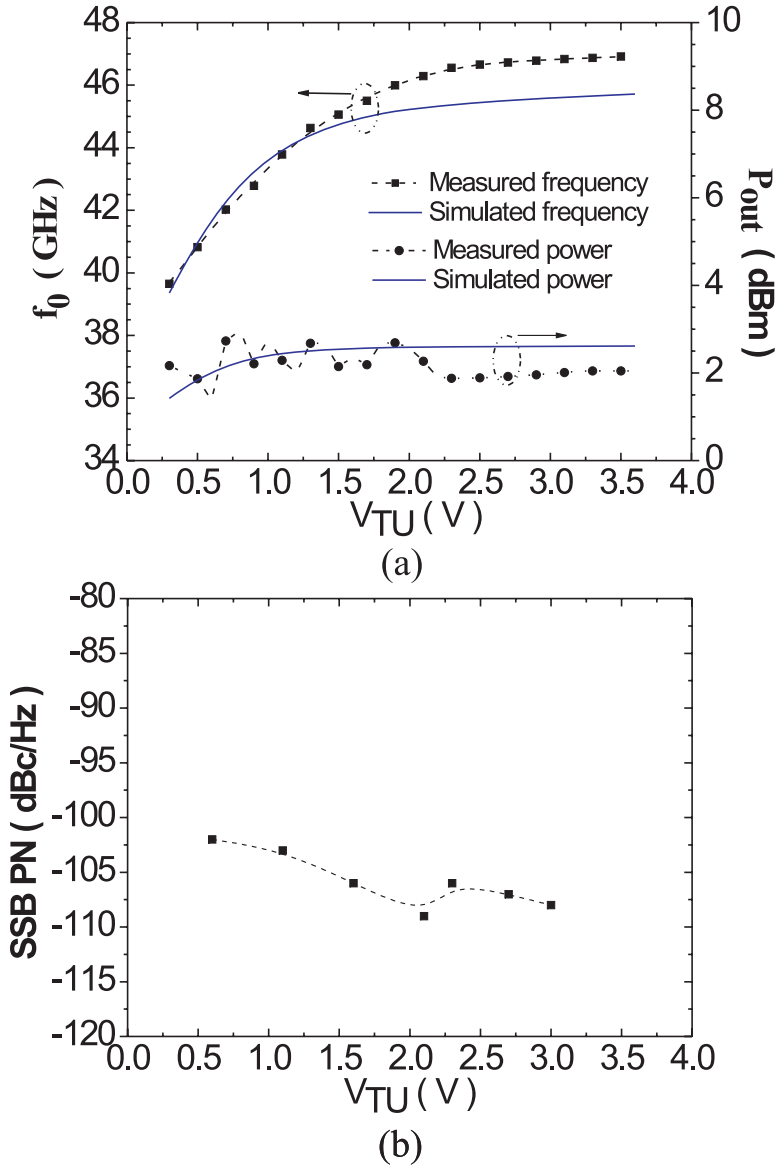


Figure 4.30: Measured and simulated performance of the 43 GHz VCO: (a) Operation frequency f_0 and signal output power P_{out} vs. tuning voltage V_{TU}; (b) Single-sideband phase noise SSB PN vs. V_{TU} at 1 MHz offset frequency.

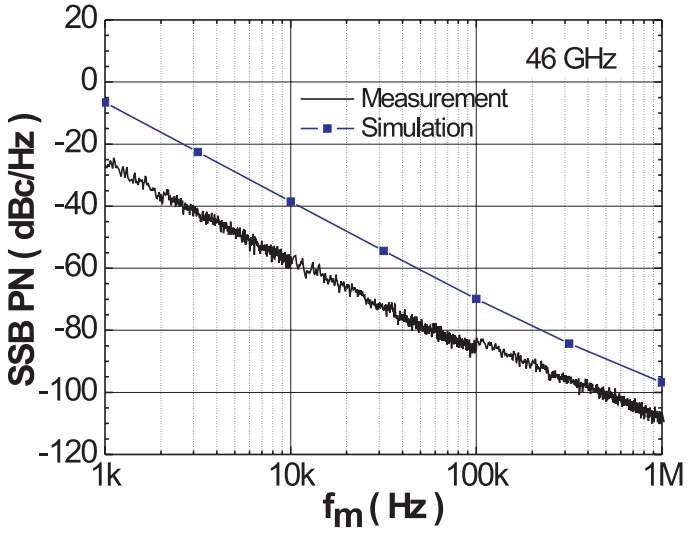


Figure 4.31: Measured and simulated SSB PN vs. offset frequency f_m at $f_0 = 46$ GHz.

Within the operation range of the VCO, the variation of the measured single-sideband phase noise (SSB PN) is shown in Figure 4.30(b). The frequency offset from the carrier amounts to 1 MHz. At 46 GHz, the VCO features a minimal phase noise of -109 dBc/Hz. The corresponding measured and simulated roll-off as a function of the offset frequency is shown in Figure 4.31. According to this figure, the simulated phase noise is higher than the measured one by 10 dBc/Hz. Thus, the phase noise simulation strongly underestimates the noise behavior of the VCO. A possible explanation for this deviation might be the erroneous consideration of the high-frequency noise components (of the VCO circuit) by the simulator. This fact would be due to inaccuracies of the noise model derived by this simulator. Thus, the systematic development of a device noise model appears to be indispensable for obtaining accurate phase noise simulations.

The VCO circuit is operated at a supply voltage of $V_{EE} = -4$ V. The resulting power consumption amounts to $P_{DC} = 136$ mW.

4.5.3 Discussion of the Simulation and Measurement Results of the 86 GHz VCO

Figure 4.32(a) shows the simulated and measured operating frequency range as well as the corresponding output power of the 86 GHz VCO as a function of the tuning voltage. By varying the tuning voltage over 3 V, the measured oscillation frequencies continuously range from 83 GHz to 89 GHz, corresponding to a VCO gain K_{VCO} of 2 GHz/V. The simulated frequency tuning range agrees well with the simulated one, except for a deviation far less than 2%.

Within the frequency tuning range, a measured single-ended output power up to 5 dBm is achieved, i.e. a total available signal power of 8 dBm. The simulated output power shows

good agreement with the corresponding measurements at the upper operation frequencies, but a decreasing accord towards the lower frequency tuning limit. The maximum deviation amounts to 2 dBm. The decrease of the measured output power towards lower operation frequencies can be explained by the inferior power matching realized at the buffer output. Simulation inaccuracy however prevents the consistence between the simulated and measured output power in this lower frequency range.

Figure 4.32(b) presents the variation of the measured phase noise as a function of

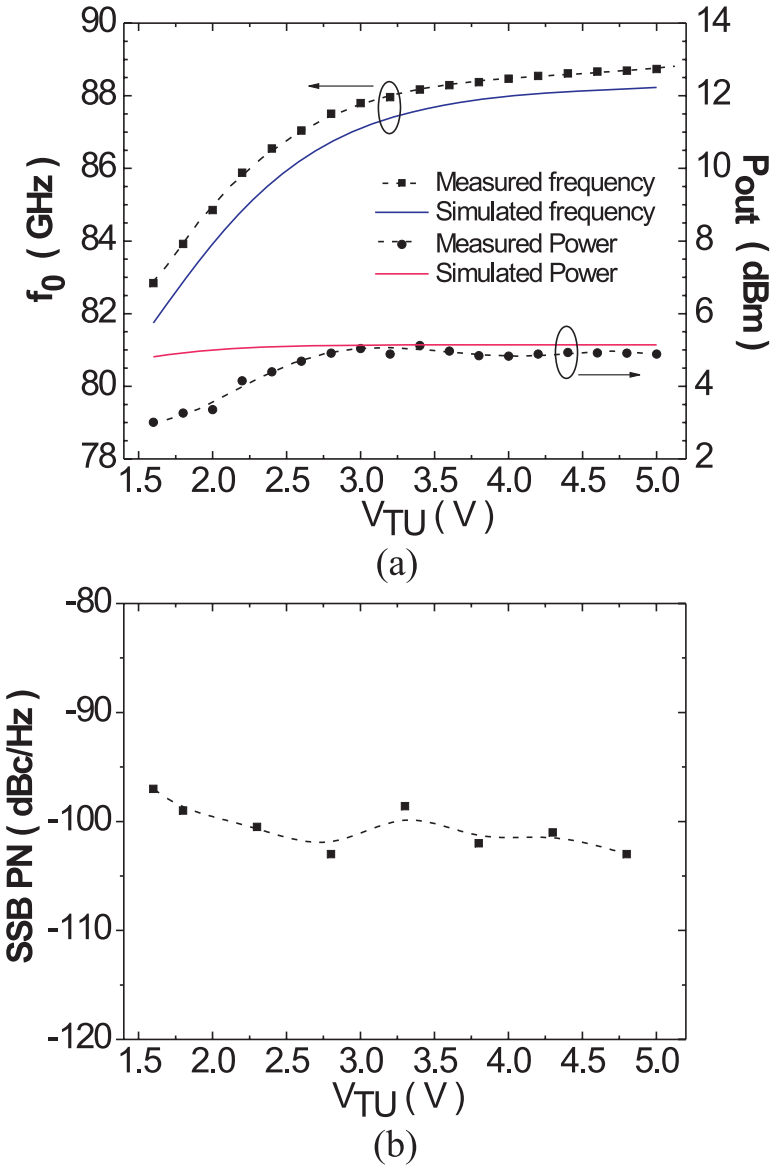


Figure 4.32: Measured and simulated performance of the 86 GHz VCO: (a) Operation frequency f_0 and signal output power P_{out} vs. tuning voltage V_{TU}; (b) Single-sideband phase noise SSB PN vs. V_{TU} at 1 MHz offset frequency.

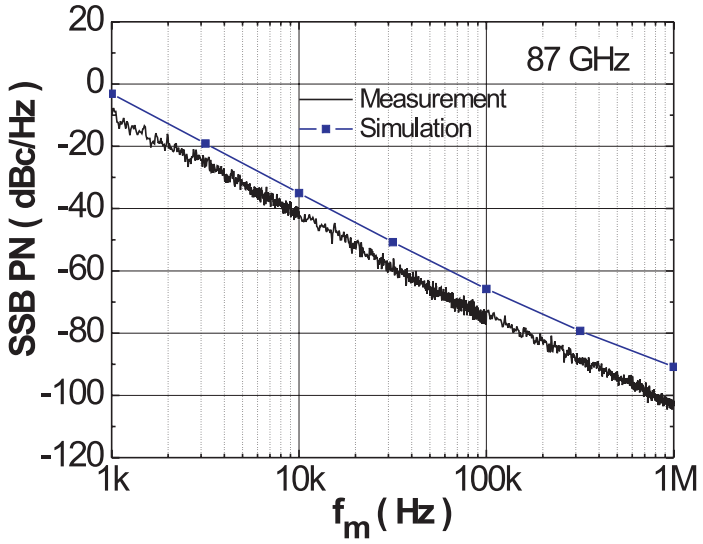


Figure 4.33: Measured and simulated SSB PN vs. offset frequency f_m at $f_0 = 87$ GHz.

the tuning voltage. At 87 GHz a minimum phase noise value of -102 dBc/Hz at 1 MHz offset from the carrier is achieved. The latter phase noise value is consistent with the phase noise measured at 43 GHz in sec. 4.5.2. In fact, as a rule of thumb and according to Equation (4.37), the phase noise features an increase of approximately 6 dB as the operation frequency of the VCO is doubled, thereby considering Q_L as constant. The roll-off of the simulated and measured phase noise at 87 GHz as a function of the offset frequency is shown in Figure 4.33. Similar to Figure 4.31, a deviation of 10 dBc/Hz between simulation and measurement can be observed. The possible cause for this deviation is given in the previous section.

The 86 GHz VCO is operated at a supply voltage of $V_{EE} = -5$ V. The resulting power consumption amounts to $P_{DC} = 550$ mW, while the output buffer consumes more than two-thirds of these power losses.

4.6 Summary

In this chapter, the design and realization of fully integrated differential VCOs for the 43 GHz and 86 GHz operation range have been discussed. These VCOs are intended for use as frequency source for data clocking in half- and full-rate CDR circuits at data rate over 80 Gbit/s. In order to achieve the intended high operation frequencies as well as low phase noise performance, the so-called LC negative resistance oscillator concept has been applied. Beside the loop gain method for the consideration of oscillation start up, the circuit design is further based on harmonic balanced simulations, by means of which the behavior of the oscillator circuits in their steady-state has been considered. Since the phase noise represents an essential property of oscillators, design considerations for smallest

possible phase noise performance have been developed.

The achieved performance of the realized VCOs (in terms of output power, phase noise, and tuning range) at 43 GHz and 86 GHz, respectively, makes them well suited for the intended application. Furthermore, the overall achieved performance is absolutely comparable, if not, better than state-of-the-art VCOs in all competing technologies. This is proven by Table 4.1 and Table 4.2, where state-of-art publications at the time of this work are listed, considering our operation frequencies of interest.

Reference	Technology	f_0 [GHz]	P_{out} [dBm]	SSB PN [dBc/Hz]	Δf [GHz]	P_c [mW]
[42] ('02)	SiGe HBT	41.5	3.5	-108.5	10	280
[79] ('04)	CMOS	43	-23	-90	1.8	14
[31] ('02)	InP HBT	44	1	-100	4.5	600
This work [6]	**InP HBT**	**43**	**2**	**-108**	**7.35**	**136**

Table 4.1: State-of-the-art publications on VCOs operating in the 43 GHz frequency range. The phase noise is measured at 1 MHz offset frequency.

Reference	Technology	f_0 [GHz]	P_{out} [dBm]	SSB PN [dBc/Hz]	Δf [GHz]	P_c [mW]
[44] ('02)	SiGe HBT	86	7	-91	4	930
[36] ('04)	InP HBT	80	-2	-118	4	95
[40] ('03)	GaAs HBT	77	-2.3	-92	1.2	486
This work [48]	**InP HBT**	**86**	**5**	**-102**	**6**	**550**

Table 4.2: State-of-the-art publications on VCOs operating in the 86 GHz frequency range. The phase noise is measured at 1 MHz offset frequency. The VCO in [36] does not include any output buffer, the consequence of which is the observed low power consumption.

Chapter 5

Phase Detector for > 80 Gbit/s Clock and Data Recovery Applications

The phase detector is, beside the voltage controlled oscillator, a further crucial component in the composition of digital clock and data recovery circuits. As already discussed in sec. 2.2, the digital phase detector is responsible for the detection of the input data transitions as well as the detection of the phase difference between the input data and the VCO signal. As a result of these, a dc voltage signal for the frequency control input of the VCO is generated over the low-pass filter. Due to the presence of flip-flops within the phase detector, the latter component further inherently provides the function of data recovery. As mentioned in sec. 2.3, the so-called linear half-rate phase detector represents the concept of choice for the realisation of the CDR circuit.

This chapter deals with the design and implementation of a linear half-rate phase detector including an 1:2 DEMUX. This phase detector is intended for applications in > 80 Gbit/s monolithically integrated CDR circuits. In the first part of this chapter, the operation principle of the aforementioned phase detector type is discussed. Then, design considerations as well as concepts for the implementation of the digital components included in the phase detector are introduced. The third part of this chapter deals with the processing of the phase detector output signal by the loop filter, discussing the operation principle and the implementation of the latter component. In the fourth part, the results of measurements performed on the implemented phase detector are presented. Finally, a summary resumes the developments and results achieved. Similar to Chapter 4, a detailed block diagram (see Figure 5.1) is used for further illustrating the organization structure of this essential chapter as well as the links between the different development steps.

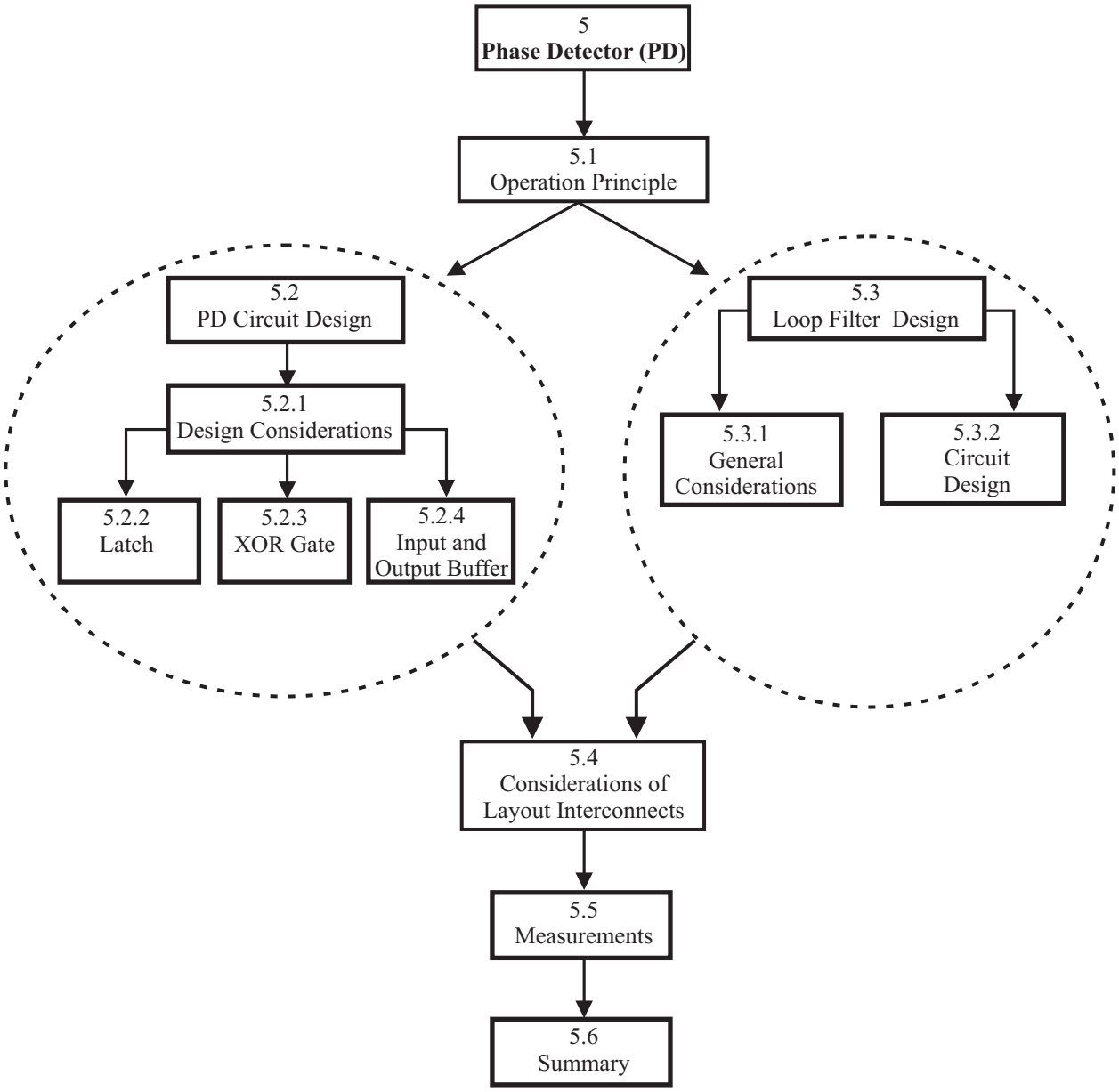


Figure 5.1: Block diagram showing the organization structure of this chapter. The block sequence illustrates the logical development step applied towards the realization of the phase detector along with the loop filter.

5.1 Operation Principle

The concept applied for the half-rate linear phase detector is illustrated in the block diagram of Figure 5.2. This concept was reported for the first time by Savoj et al. [68], relating to a 10 Gbit/s CMOS-based CDR circuit. The phase detector is composed of four latches (L_1-L_4) in the topology of a demultiplexer, with the corresponding distribution

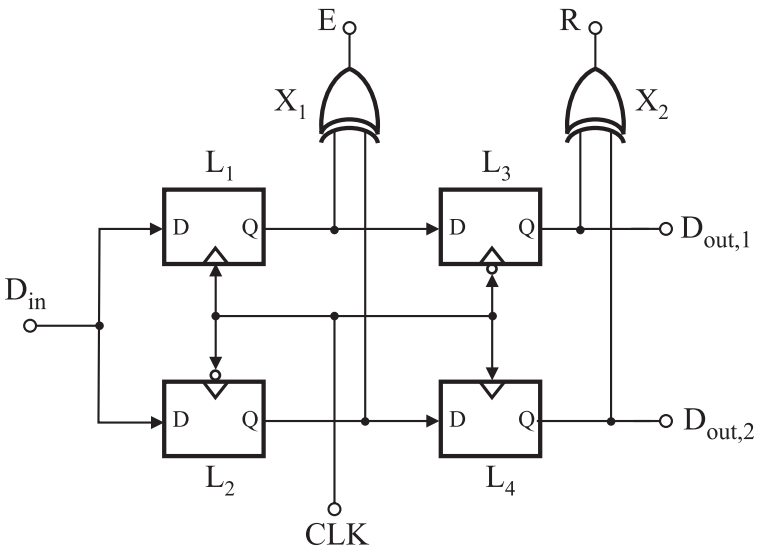


Figure 5.2: Block diagram of the half-rate linear phase detector.

of the clock signal. The respective output data signal of the latches L_1-L_2 is fed to the inputs of the XOR gate X_1, while the respective output of the latches L_3-L_4 is connected to the inputs of the XOR gate X_2. The detection of data edges as well as the detection of the phase difference between data and clock signal are performed by the latches L_1-L_2 in cooperation with the XOR gate X_1. That is, a pulse signal appears at the output of X_1 as soon as a data transition occurs at the input of the phase detector. Furthermore, the width of this pulse signal is proportional to the phase difference between data and clock signal. Due to its representation of the phase error, the aforementioned proportional pulse signal is related to as error (E) signal. However, the average value of the latter signal is a function of the data transition density, thus failing to uniquely represent the phase error for different data patterns. In effect, two different phase errors may result in the same dc output for the control voltage of the VCO, leading to an erroneous lock behavior of the CDR circuit. A remedy of this ambiguity is found by relating the error signal to a reference pulse signal, the width of which is constant for any phase difference. This is achieved with the pulse signal R at the output of the XOR gate X_2, generated in cooperation with the respective output of the latches L_3-L_4. The signal R features a constant pulse width corresponding to half the period of the clock signal.

The operation of the phase detector is further illustrated by the time signal diagrams of Figure 5.3, showing the resulting signals E and R for various phase differences between data and clock signal. The phase difference is considered to be zero, as the rising edge of the clock signal samples the input data in the midpoint of each bit. Thus, Figure 5.3(a) shows the time signal constellation within the phase detector when the CDR loop locks to the random input data. In this state, the error signal features a pulse width equal to half the pulse width of the reference signal. A neat integration or subtraction of both signals (E and R), as discussed in sec. 5.3, results in a constant and negligible dc voltage signal

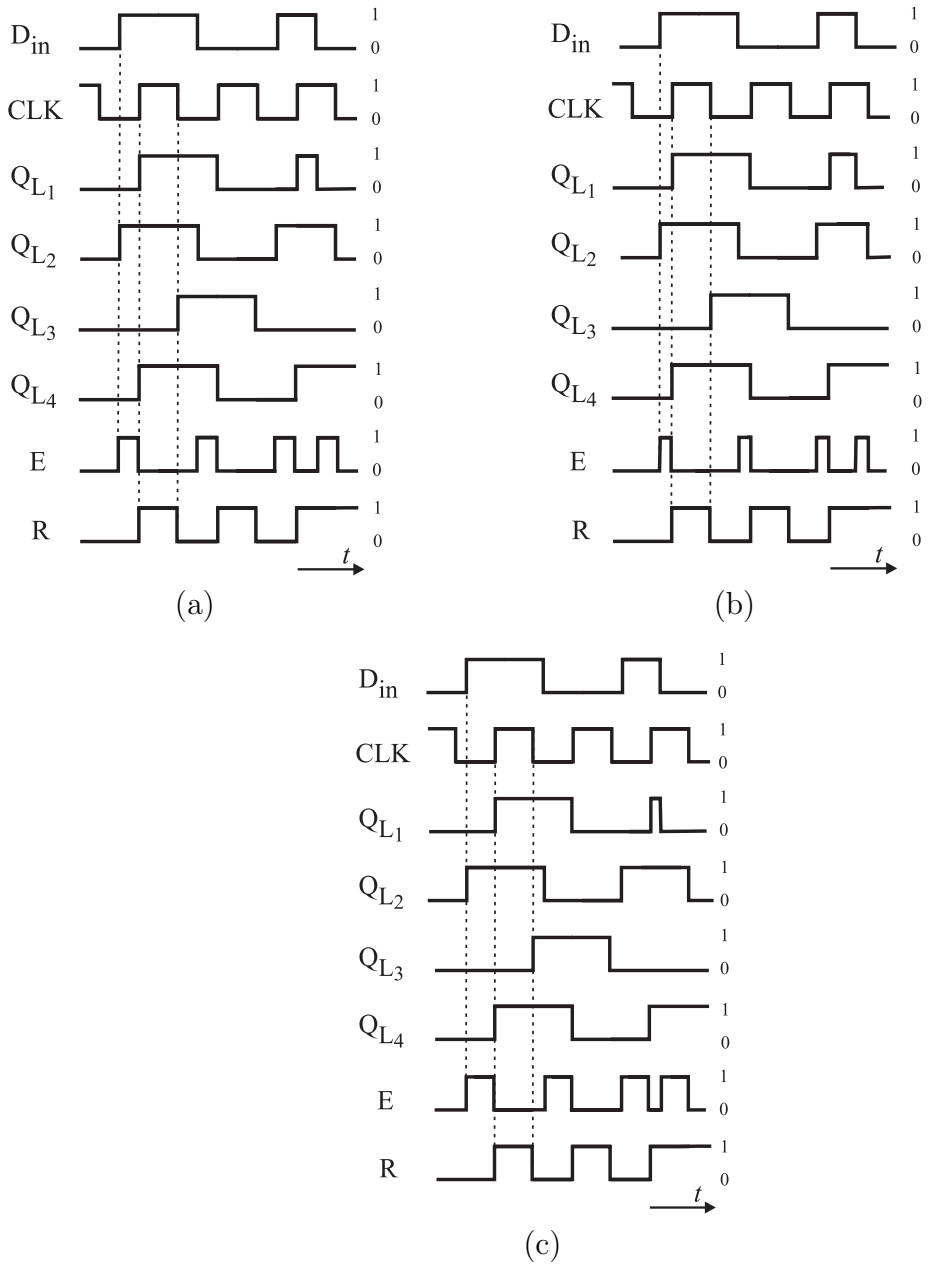


Figure 5.3: Time diagrams of the signals within the phase detector for different clock phase states related to the input data: (a) lock state, (b) clock early, (c) clock late.

for the frequency control of the VCO.

Figure 5.3(b) illustrates the operation of the phase detector when the rising edge of the clock signal is early with respect to the midpoint of the bit. This state is also referred to as the early state. In the latter state, the pulse width of the error signal E is smaller than the corresponding width in the lock state. The appearance of the resulting VCO control voltage is discussed in sec. 5.3. Figure 5.3(c) shows, on the other hand, the behavior of the phase detector when the clock lags. The latter state is called late state, with the pulse width of the signal E greater than the corresponding width in the lock state.

The data regeneration occurs at the respective output of the latches L_3 and L_4. Since the architecture of the phase detector latches corresponds to a demultiplexer, the regenerated data are produced in form of two parallel streams with the corresponding bit rate equal to half the input data rate.

5.2 Circuit Design

5.2.1 Design Considerations

The implementation of the digital circuit components included in the phase detector underlies some basic design principles, which allow the achievement of highest operation speed. These basic design techniques have been introduced in [62] for Si-based bipolar digital circuits at data rates up to 50 Gbit/s, but are found to remain applicable in the used InP-DHBT technology, even at the much higher data rate of interest.

Differential Topology

The differential operation of digital circuits is a well-established design technique because of the following well-known advantages with respect to the single-ended contender:

- The maximum achievable data rate is higher due to a lower time jitter as well as steeper pulse edges.
- The crosstalk is minimized because of the complementary nature of the high-frequency signals.
- The power consumption is lower due to the smaller voltage swing necessary for signal switching.

Current Switch Technique

The current switch technique forms the basis of the so-called current mode logic (CML) with its two counterparts: emitter-coupled logic (ECL) and emitter-emitter-coupled logic (E^2CL) (Figure 5.4). This design technique allows to implement complex logic functions at high data speed, with outstanding driving capability of terminated lines. However, the E^2CL logic achieves higher data rate with respect to the ECL logic, while the latter logic shows higher operation speed regarding the CML technique. The speed advantage of the

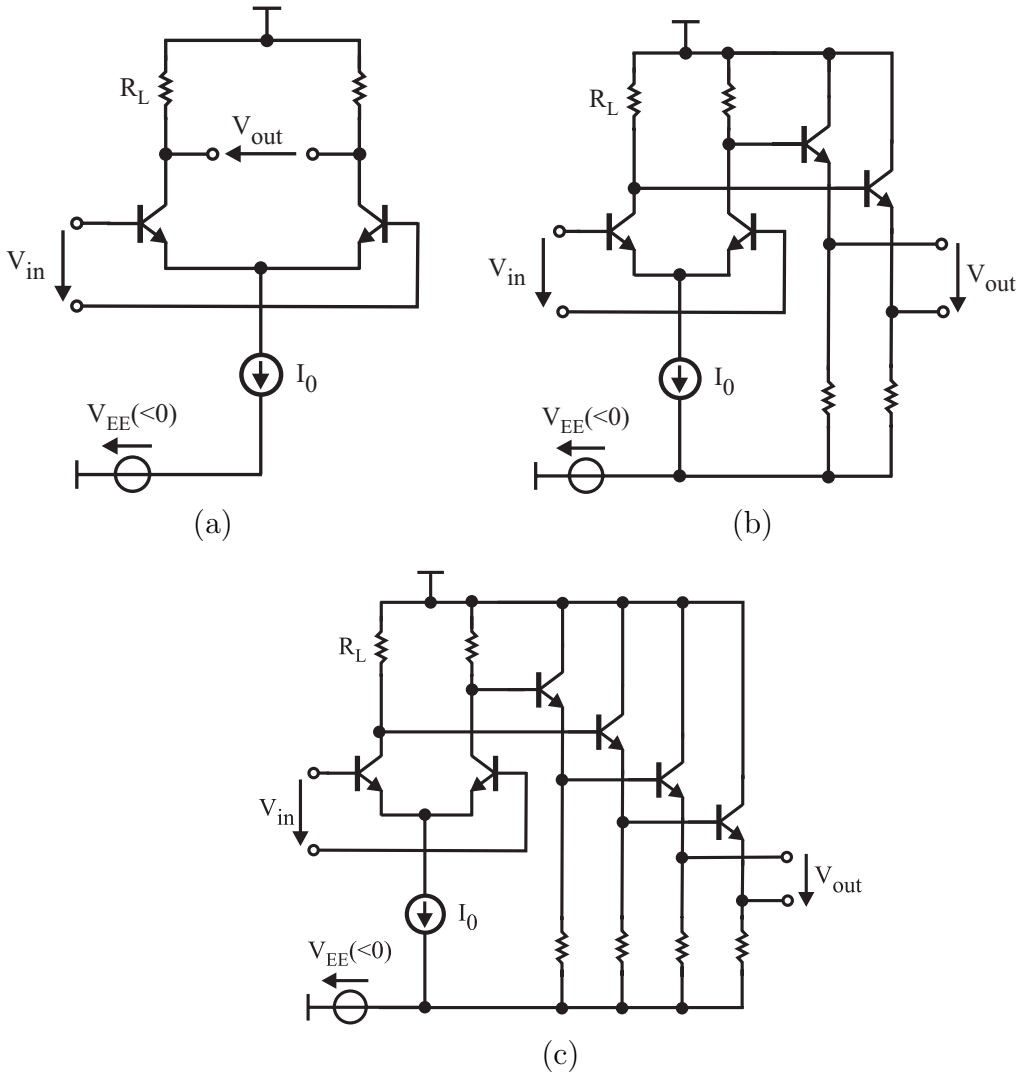


Figure 5.4: Different realisations of logic gates based on the current switch technique: (a) CML gate, (b) ECL gate, (c) E^2CL gate.

ECL and E^2CL logics originates from the very low output impedance of the included one- and two-stage emitter follower, respectively, but at the cost of a higher power consumption. As a compromise, the ECL technique is mainly considered for the implementation of the required logic functions, while the E^2CL counterpart comes into consideration only if a dc level shift of more than $2 \cdot V_{BE}$ is required (cf. sec. 5.2.2).

In the current switch technique, the output signal level is generally referenced to ground (as implicitly assumed for the VCO design in sec. 4.4), thus resulting in a negative power supply. In this way, output signal distortion due to interfering signals in the power supply is avoided. Furthermore, the signal coupling between different circuit blocks is eased, since no bias-T is required.

Series-gating Logic

The series-gating circuit technique consists in cascading several current switches on a single current source to implement logic functions, as illustrated by the circuit concept used for the implementation of the latches (cf. sec. 5.2.2). This circuit technique features the following advantages compared with other circuit techniques (e.g. schottky diode technique [63], [74]):

- Complex logic functions in differential topology are easy to implement.
- The propagation delay between the signal planes is short, thus resulting in high operation speed.
- The power consumption is lower since only one current source is needed.

Transistor Device Selection

High-speed performance of digital circuits is not only determined by the choice of a suitable circuit concept, but also by the right selection of the transistor size within the considered circuit. For a given circuit concept, the propagation delay (or gate delay) τ_d of the data signal from the circuit input to its output serves as device selection criteria. Several works have been performed for determining an analytical expression of τ_d for CML- and ECL-based circuits (cf. [5], [7], [12], and [66]). According to [16] and [66], the minimum gate delay of a basic ECL circuit is determined by a set of time constants of which the following term is a major contributor:

$$\tau_d \propto \frac{C_{CB}\Delta V}{I_C}, \tag{5.1}$$

whereas C_{CB} and I_C represent the collector-base capacitance and the collector current of one current switch transistor, respectively. Furthermore, ΔV is the output voltage swing. Thus, with respect to the transistor geometry, a minimisation of the propagation delay is achieved by reducing the corresponding collector-base capacitance. This capacitance shows a strong proportional dependence on the emitter length L_E of the transistor and a less strong on the emitter width W_E. Therefore, the used transistors feature the minimum available emitter width $W_{E0} = 1$ μm. However, the value of the emitter length can not be set arbitrarily small, since the base resistance R_B is inversely proportional to L_E. In fact, for L_E values smaller than a certain emitter length L_{E0}, R_B features a more rapid increase with respect to the decrease of C_{CB}. The incidence of this fact results in a much more considerable influence of R_B on τ_d.

Figure 5.5 illustrates the variation of the small signal parameters R_B and C_{CB} as a function of the emitter length L_E of the available transistors. These transistors feature an emitter width $W_E = 1$ μm and are biased at a voltage $V_{CE} = 1.75$ V and a collector current density $J_C = 3.0$ mA/μm^2. Thus, from Figure 5.5, a value of 4 μm is extracted for L_{E0}. A further point motivating the choice of L_{E0} is the operation current I_C of the transistor devices. In fact, this current should be minimized in order to keep low the dc

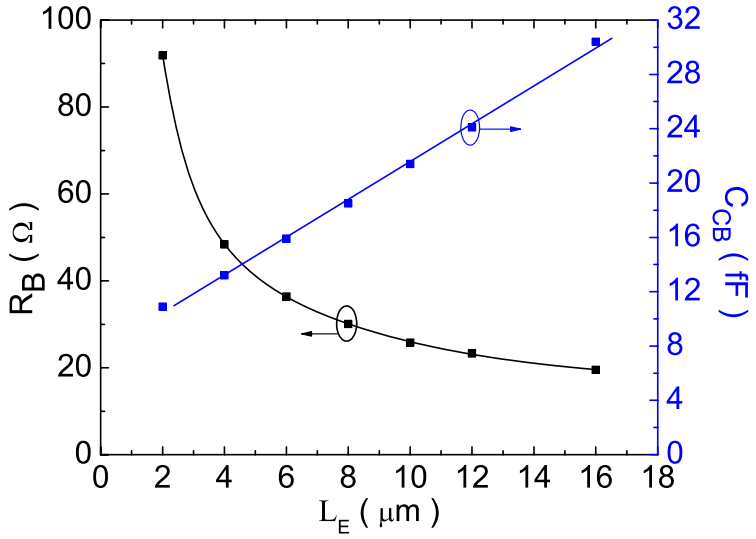


Figure 5.5: Variation of the small signal parameters R_B and C_{CB} as a function of the emitter length L_E. The transitors feature an emitter width of $W_E = 1$ μm and are biased at a voltage $V_{CE} = 1.75$ V and a collector current density $J_C = 3.0$ mA/μm^2.

power consumption of the integrated circuit. That is, the current switches included in the high-speed circuits feature 1×4 μm^2 transistors, except for explicitly mentioned cases.

Low Voltage Swing

Beside the reduction of the capacitance C_{CB}, the minimisation of the propagation delay through a logic gate is further achieved by minimising the voltage swing ΔV across the load resistor R_L, according to equation (5.1). However, ΔV must be kept to a minimal value to continuously ensure transistor switching as well as a good signal-to-noise ratio (SNR). This minimal value depends upon the used transistor, especially the corresponding emitter resistor R_E. The transfer characteristic of a CML gate using 1×4 μm^2 switch transistors is shown in Figure 5.6. According to this figure, a full switching of the switch transistors is achieved at a voltage swing of approximately 150 mV. However, considering the aforementioned SNR, the logic gates are operated with a voltage swing ΔV of 320 mV.

In order to obtain the optimal value of ΔV, the current I_C through the switch transistor is set to a value which arises from a trade-off between a transistor operation at highest f_T and an operation at minimum current consumption. In fact, a switch transistor operation at highest f_T benefits the gate delay through a minimized transistor transit time, while a minimum current consumption is advantageous for minimizing the power consumption of the intended digital circuit. Thus, instead of operating the switch transistor at a current density J_C of 3 mA/μm^2 for maximum f_T (see Figure 3.9), the latter transistor is operated at a J_C of 2 mA/μm^2. This results in a current I_C of 8 mA for a device area of 4 μm^2. The optimum operation voltage V_{CE} ranges between 1.5 V and 2 V, as mentioned in sec. 3.5.2. From the fixed values for I_C and ΔV, a load resistor R_L of 40 Ω is calculated.

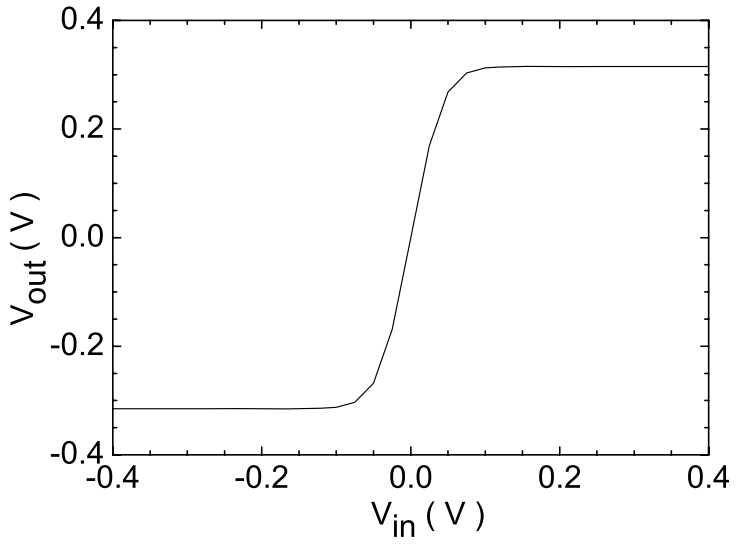


Figure 5.6: Transfer characteristic of a CML gate using 1×4 μm^2 switch transistors. Referring to Figure 5.4(a), the current I_0 amounts to 8 mA while R_L is 40 Ω.

5.2.2 Latch

The implementation of the latches included in the phase detector is based on a well-known circuit concept applying the series-gating technique [62]. Relying on this circuit concept, two circuit variations are used for the implementation of the latches (L_1, L_3) and the latches (L_2, L_4), respectively. These circuit variations are illustrated in Figure 5.7(a) and Figure 5.7(b). Basically, the latch circuits presented in both figures are identical, regarding the data processing by the transistors (Q_1-Q_8). The difference arises from the circuit devices Q_9-Q_{10} and Q_{11}-Q_{14}, which are used as emitter follower for driving the processed data to the respective latch output, thus feeding the following circuit blocks. Hence, the basic operation of the latch can be explained using the circuit variation of Figure 5.7(a). According to this schematic diagram, the differential clock signal (CLK) controls the current switch (Q_5-Q_6). This current switch either activates the amplifier cell (Q_1-Q_2) or the memory cell (Q_3-Q_4), depending on whether the clock signal level is logical high or low. For the first case, the data at the differential input D_{in} are transfered to the latch output $D_{out,L13}$. This state is related to as the acquisition state. In the second case, the latch output is decoupled from the data input and receives only the data stored in the memory cell via the positive feedback (Q_7-Q_8). This state is related to as the memory state. The operation principle of the latch is further illustrated by the time signal diagrams in Figure 5.3, considering the corresponding latch outputs.

The current source is implemented with a resistor, thus avoiding parasitic capacitances, which would be induced by using a transistor current source with the corresponding output

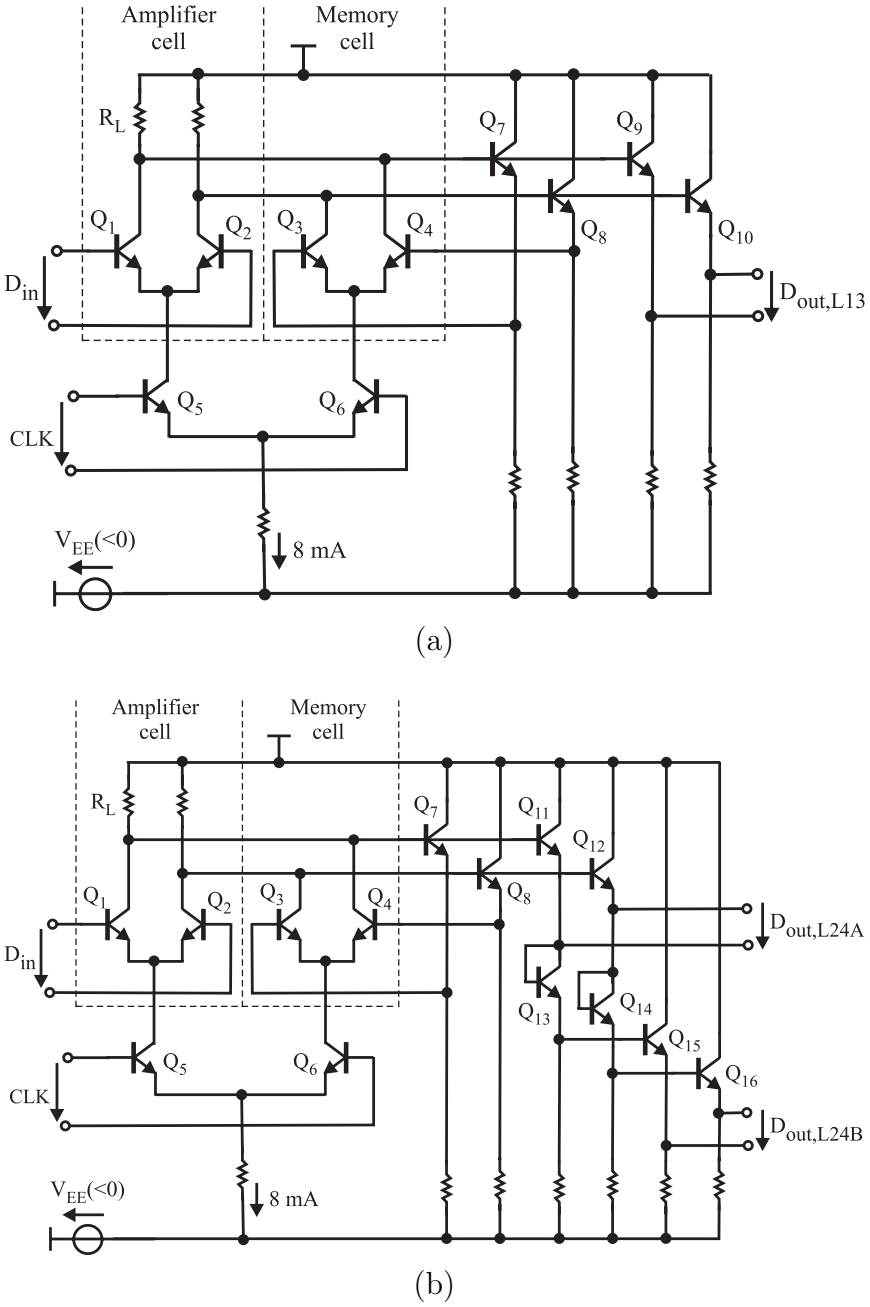


Figure 5.7: Schematic circuit diagrams used for the implementation of the latches included in the phase detector: (a) Circuit variation for L_1 and L_3, (b) Circuit variation for L_2 and L_4.

capacitance. Furthermore, the use of a resistor current source keeps the complexity of the whole phase detector circuit as well as the corresponding power consumption relatively low.

In both latch variations, the tapping of the output data is isolated from the feedback

path of the memory cell. Thus, unlike the topology commonly used for data latches, the critical (in terms of speed) data transfer path from the latch input to its output is less capacitive charged. Namely, the input capacitance of the memory cell does not impact at the data output, thereby minimizing the transfer delay of the data. Considering the latch circuit of Figure 5.7(a), the isolation between data output and feedback path of the memory cell is achieved by using the one-stage emitter followers Q_7-Q_8 and Q_9-Q_{10}. The emitter followers at the latch output ensure a speedy data transfer through fast charging and discharging of the output capacitive load. Furthermore, they supply a dc level shift of $1{\cdot}V_{BE}$, which is necessary for the right operation point setting of the current switches in the next circuit blocks. For example, the upper current switches of L_3, X_1 and X_2 (cf. sec. 5.2.3) are concerned.

In Figure 5.7(b), the isolation between data output and feedback path of the memory cell is achieved by using the one-stage and two-stage emitter follower Q_7-Q_8 and Q_{11}-Q_{16}, respectively. Two data outputs differing in their dc voltage level are available. This measure is necessary since the current switches of the next circuit blocks supplied by L_2 and L_4 require a dc level shift of either $1{\cdot}V_{BE}$ (e.g.: amplifier cell of L_4, output buffer from sec. 5.2.4) or $3{\cdot}V_{BE}$ (e.g.: lower current switch of X_1 and X_2) for proper operation point setting. For the generation of the dc level shift of $3{\cdot}V_{BE}$, the combination of two emitter followers with a diode is preferred to a three-stage emitter follower. The latter alternative results in ringing problems as well as a higher power consumption.

The dc level shift necessary for the operation point setting of the amplifier cell in L_1-L_2 is set by an one-stage emitter follower. This emitter follower further serves as input buffer, as shown in sec. 5.2.4. A resistive voltage divider supplies the dc voltage level required by the clock current switches in the latches L_1-L_4, since the clock signal is ac-coupled to this stage. An advantage of the ac-coupling is the lower power consumption compared to the operation point setting with emitter follower, whereas a two-stage emitter follower in combination with a diode would be necessary for this purpose. The collector emitter voltage V_{CE} of the transistors forming the current switches is set to be between 1.5 V and 1.8 V, thus conforming with the optimum voltage range defined in the previous section. Furthermore, the operation of the devices in the saturation region is avoided at these voltages.

As a trade-off between circuit operation reliability, operation speed and current consumption, the size of the transistors used in one-stage and two-stage emitter followers is chosen to be $1 \times 4\ \mu m^2$. Concerning the one-stage emitter followers, the included transistors are operated at a voltage V_{CE} of 1 V and a current I_C of 4 mA, except for a fan-out of two (e.g.: Q_9-Q_{10}). For the latter case, a higher collector current of 7 mA is set to allow fast charging and discharging of the bigger capacitive load compared to the case with a fan-out of one. Concerning the two-stage emitter followers (Q_{11}-Q_{14}), the transistors included in the first stage are operated at a current I_C of 4 mA and a voltage V_{CE} of 1 V. The transistors used in the second stage are biased at a current I_C of 7 mA and a voltage V_{CE} of 2.4 V. Despite the fact that the emitter followers are operated at operation points deviating from the maximal transit frequency, a circuit operation at the data rate of interest is achieved with good reliability. Namely, emitter followers are broadband circuit

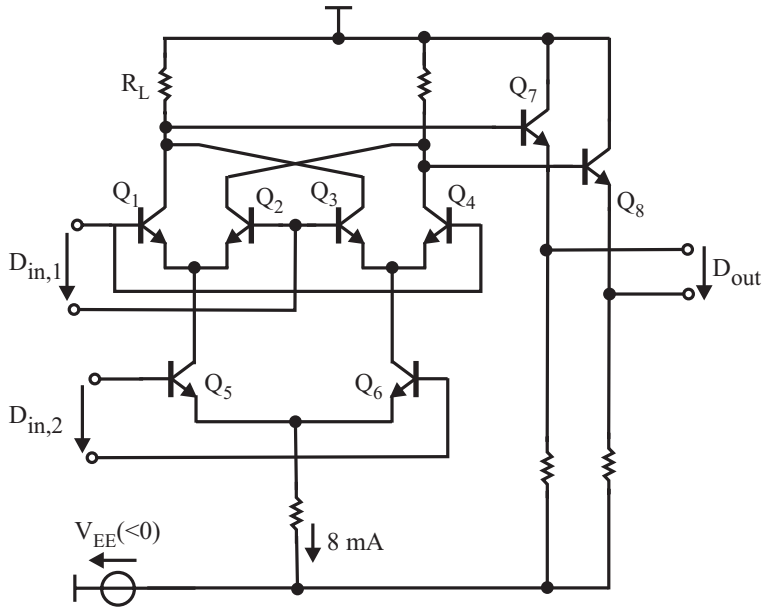


Figure 5.8: Schematic circuit diagram of the applied XOR gate.

with a bandwidth approximately equal to the transit frequency (f_T) at the operation point of the used transistor.

5.2.3 XOR Gate

The realization of the XOR gate is performed according to the schematic circuit diagram of Figure 5.8. The core of this circuit corresponds to the Gilbert cell used for the implementation of multipliers in the design of analog circuits. However, for the effective large-signal operation, the emitter-coupled differential amplifiers act as current switches. Using the circuit concept of Figure 5.8, a topology according to the series-gating technique is available. The operation points (I_C, V_{CE}) of the current switches and emitter followers are similar to those of the corresponding circuit elements included in the latch of the previous section. The operation current is fed by a resistor serving as current source. As already discussed in the previous section, the setting of the voltage V_{CE} across the upper and lower current switch transistors is ensured by the ECL and E^2CL output of the latches, respectively.

According to the logical function of a XOR gate, the operation principle of the latter XOR in relation with the phase detector operation is illustrated in Figure 5.3, considering the outputs E or R.

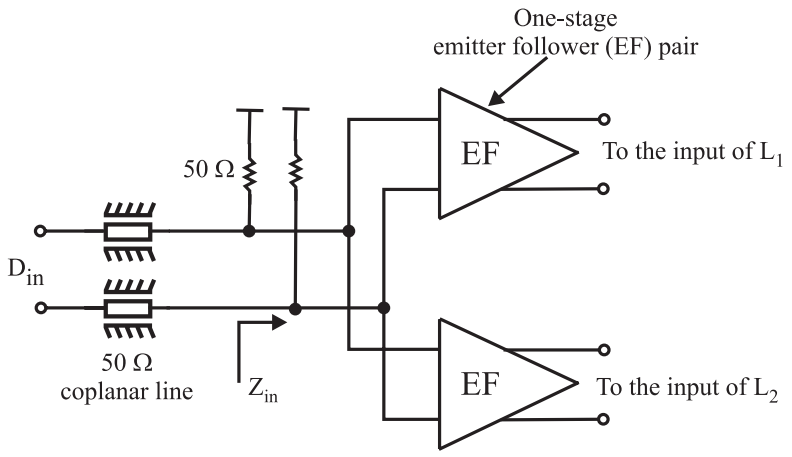


Figure 5.9: Block diagram of the implemented buffer at the phase detector input.

5.2.4 Input and Output Buffer

Input Buffer

The feeding of the data at the phase detector input has to be performed without any signal degradation, i.e. with smallest possible reflection at the phase detector input. Due to their relatively high input impedance as well as the corresponding low output impedance, input buffers in form of one- or several-stage emitter followers allow to match the circuit input to the generator internal resistance (commonly 50 Ω) or to the characteristic impedance of the waveguide used to feed the data signal. The matching is performed by shunting a resistance as close as possible to the input of the emitter follower, whereas the resistance value corresponds to the generator internal resistance or the waveguide characteristical impedance.

Figure 5.9 shows the implemented buffer at the input of the phase detector circuit. An one-stage emitter follower is used to achieve the required broadband input matching. This is illustrated in Figure 5.10, showing the frequency response of the input impedance Z_{in} of the input buffer (with 50 Ω termination at its input). As already discussed in sec. 5.2.2, the one-stage emitter follower further supplies the dc voltage level required for the operation point setting of the upper current switches (Q_1-Q_2) of the latches (L_1-L_2). The bias points I_C and V_{CE} of the latter emitter follower are 4 mA and 1 V, respectively.

Output Buffer

The output buffer ensures data processing within the phase detector without any influence of the external loading, which might degrade the quality of the regenerated signal. The realization of the output buffer is achieved using a current switch, which also acts as limiting amplifier. Beside the decoupling effect, this limiting amplifier also contributes to the data regeneration by smoothing the latter signal. In fact, the processed data in the phase detector experience distortions due to the clock feedthrough as well as spikes

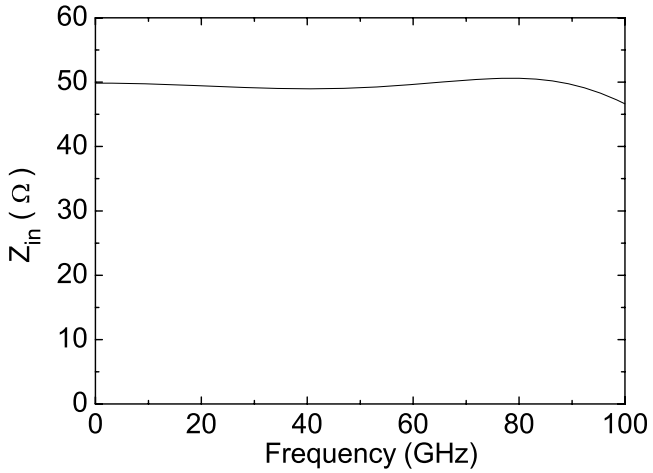


Figure 5.10: Simulated single-end input impedance Z_{in} of the input buffer with 50 Ω termination at its input.

coming from the charging and discharging of parasitic capacitances in the circuit. These distortions are indeed eliminated by the use of the current switch operating as limiting amplifier (see Figure 5.11).

Figure 5.12 shows the schematic circuit diagram of the output buffer. The latter element consists of a two-stage current switch, which allows to maximize the isolation between the external load and the core circuit of the phase detector. Furthermore, the smoothing effect is further enforced by the use of this buffer configuration.

The first stage of the output buffer features a relatively low gain, in order to minimize the corresponding input miller capacitance. Namely, this capacitance might be of negative influence for the operation of the latches L_3-L_4. The current switch included in the first buffer stage is biased at a current of 8 mA, whereas the voltage V_{CE} across the switch transistors amounts to 1.6 V. This voltage is set by the ECL output of the latches L_3-L_4. A load resistance of 40 Ω generates the defined optimum voltage swing of 320 mV for driving the second stage through an emitter follower pair. This second stage features a higher gain than the first stage, thereby generating an output swing of 600 mV across the external 50 Ω load. Therefore, the corresponding switch transistors are biased at a current I_C of 16 mA and a voltage V_{CE} of 1.6 V. Furthermore, the collector load of the transistors is a 200 Ω resistance. The double bias current in the second buffer stage induces the use of switch transistors with a doubled size of 1×8 μm^2 compared to the first stage.

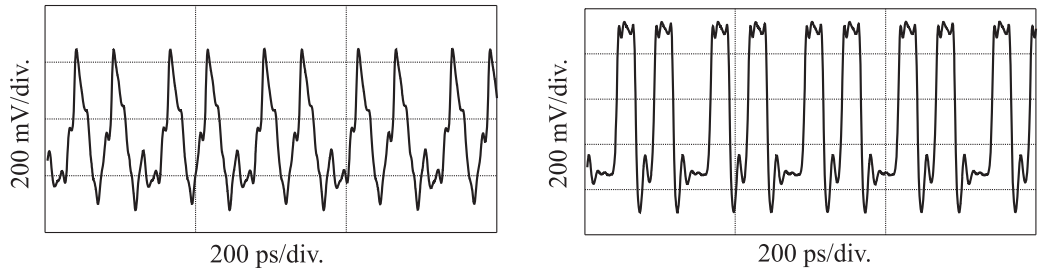


Figure 5.11: (a) Output data arising from processing within the phase detector. (b) Output data after passed through the data output buffer.

5.3 Loop Filter Design

From the pulse signals (E and R) generated by the phase detector, a dc voltage signal has to be extracted, which is then fed to the frequency control input of the VCO for phase adjustment. Therefore, the outputs E and R of the phase detector are sensed differentially and the resulting signal is low-pass filtered, thereby extracting the desired dc control voltage while eliminating the included high frequency components. This operation is performed by applying a charge pump at the outputs E and R, whereas this charge pump is assisted by a passive low-pass filter. This low-pass filter is referred to as loop filter. Since the latter filter allows a better interpretation of the dc signal originating from the phase detector, its way of implementation is presented in relation with the phase detector chapter.

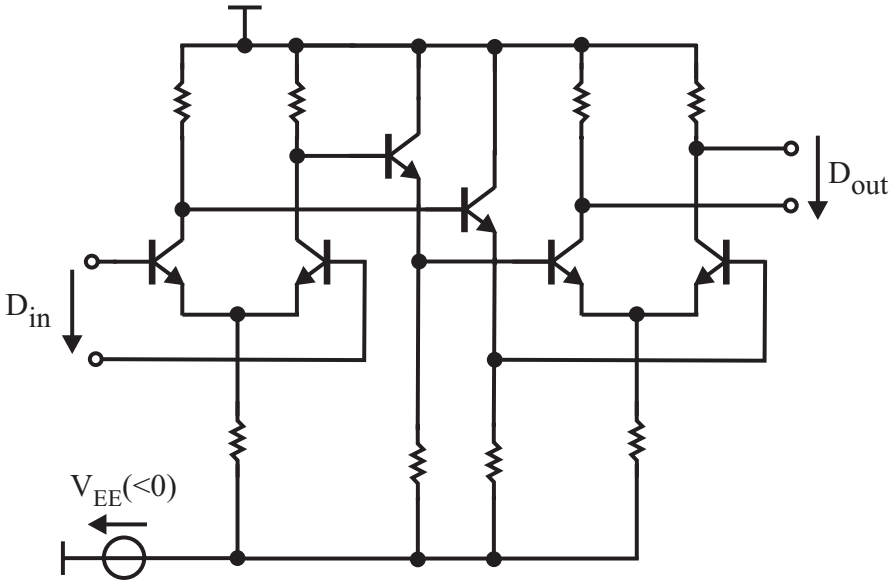


Figure 5.12: Schematic circuit diagram of the implemented buffer at the phase detector data output.

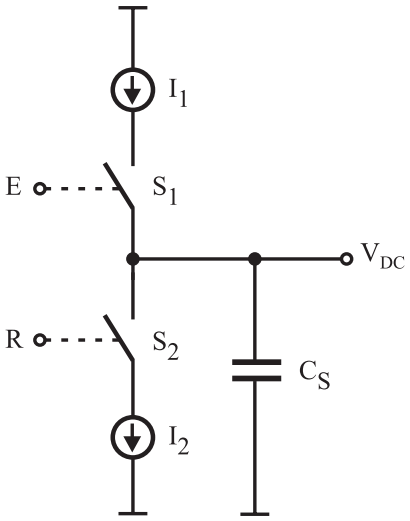


Figure 5.13: General schematic diagram of the charge pump/low-pass filter circuit.

5.3.1 General Considerations

The general operation principle of a charge pump in relation with a low-pass filter can be explained using the schematic illustrated in Figure 5.13. The charge pump is composed of two current switches (S_1-S_2), which are respectively controlled by the outputs E and R of the phase detector. According to the logical level at the respective charge pump inputs, the capacitor C_S corresponding to the loop filter is either charged by the current I_1 or discharged by I_2, thus creating a voltage ramp at the output V_{DC}. The latter current quantities I_1 and I_2 are also referred to as UP and DOWN currents, respectively.

As the CDR loop locks to the input data, the generated voltage signal V_{DC} has to feature a constant and negligible value to maintain the VCO output signal at the adjusted phase state, which is optimal for data sampling. As already mentioned in sec. 5.2, the phase detector in the lock state generates a pulse signal E whose width is half the width of the reference signal R. The width of the latter signal corresponds to half the period of the clock signal. The resulting output signal of the loop filter is then constant and negligible only if the current I_1 is twice as high as the current I_2. Therefore, the latter ratio between I_1 and I_2 corresponds to the operation mode of the charge pump. The corresponding run of the signal V_{DC} as a function of time is illustrated in Figure 5.14(a), thereby showing triangular pulses with a constant and small mean value.

Figure 5.14(b) shows the arising voltage signal V_{DC} when the clock signal is late with respect to the midpoint of the bit. Thus, a steady rising of V_{DC} towards $+\infty$ can be stated. Conversely, V_{DC} drops steadily when the clock signal is early with respect to the middle of the data bit (not shown). As a consequence, the circuit (composed of the phase detector, charge pump, and loop filter) features a gain of infinity as long as the phase deviation between the input data and the clock signal differs from zero. This infinite gain is due to the used charge pump and positively impacts on the phase adjustment. In fact, V_{DC}

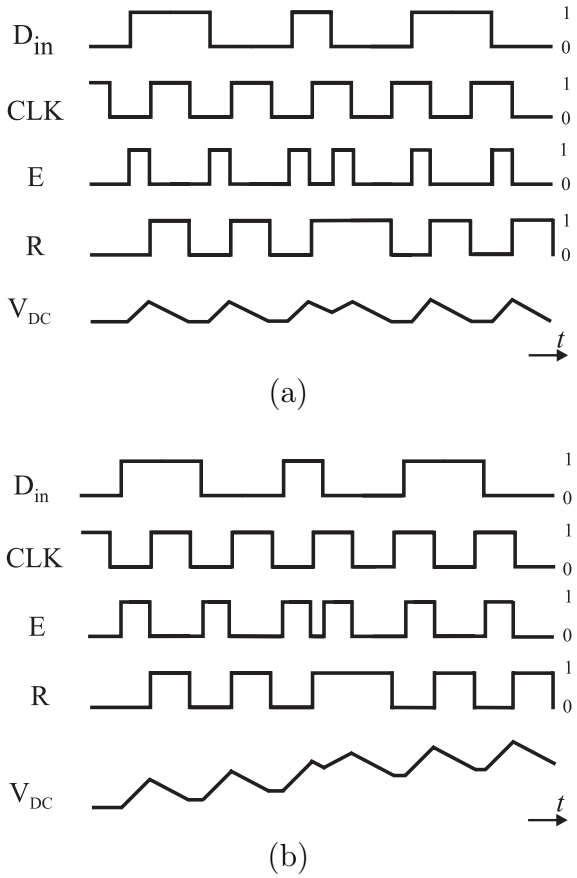


Figure 5.14: Arising voltage V_{DC} at the output of the loop filter for different phase states of the clock signal related to the input data of the phase detector: (a) lock state, (b) clock late.

moves towards $\pm\infty$ as long as a nonzero phase difference between clock and data signal exists, thus forcing the settling of the phase error $\Delta\varphi_s$ to an exact value of zero. However, consequences of parasitics influences (e.g.: parasitics discharging of C_S) within the circuit still yield a finite phase error.

The transfer characteristic of the phase detector including the charge pump and the loop filter is illustrated in Figure 5.15, thereby representing the loop filter output signal as a function of the input phase error, i.e. the phase difference between input data and clock signal. From this curve, a period of 360° can be stated.

In order to obtain the loop filter transfer function H_{LPF} defined in relation with the CDR loop system (cf. sec. 2.4.1), the filter represented by the capacitor C_S must be extended by further passive elements. Figure 5.16 illustrates the passive loop filter satisfying the transfer function defined in equation (2.3). The filter time constants τ_1 and τ_2 are respectively defined as follows:

$$\tau_1 = (2R_C + R_S)C_S \tag{5.2}$$

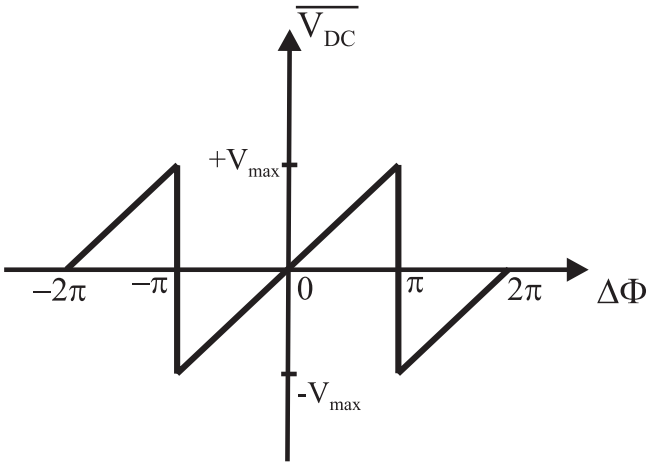


Figure 5.15: Common transfer function of the linear half-rate phase detector, i.e. output control voltage V_{CTR} as a function of the input phase error $\Delta\Phi$.

and

$$\tau_2 = R_S \cdot C_S \tag{5.3}$$

5.3.2 Circuit Design

The schematic circuit diagram of the implemented charge pump inclusive loop filter is illustrated in Figure 5.17. The switches S_1 and S_2 are realized using two current switches, thereby allowing differential operations. The respective current sources of these current switches supply the UP and DOWN currents for the charge injection in the loop filter. Unlike the circuit components introduced in the former sections, transistor current sources are used, thus allowing an external adjustment of the corresponding currents after circuit processing (by using the connection pads V_{B1} and V_{B2}). In this way, potential mismatches with respect to the fixed ratio between the UP and DOWN currents can be counteracted.

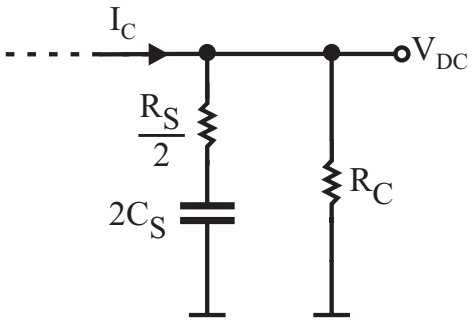


Figure 5.16: Circuit configuration of the filter applied in the charge pump/loop filter circuit. The corresponding transfer function arises from the ratio $\frac{V_{DC}}{I_C}$.

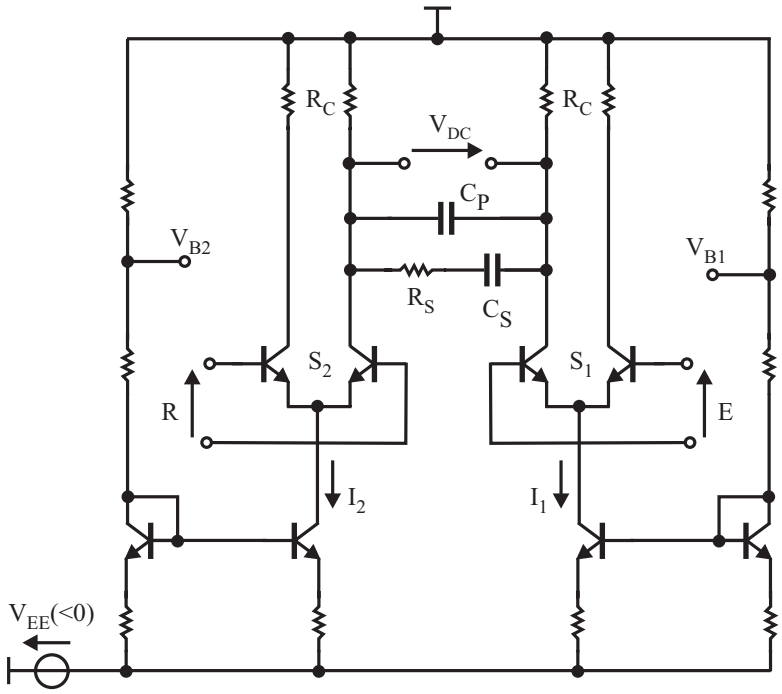


Figure 5.17: Differential charge pump/loop filter circuit for application in a half-rate phase detector.

The filter elements $\frac{R_S}{2}$ and $2C_S$ in Figure 5.16 are weighted by a factor of 2 and 0.5, respectively, in Figure 5.17 in order to consider the differential configuration. The resistance R_C also serves as load for the current switches S_1 and S_2. Actually, the finite value of R_C negatively affects the integrator function of the loop filter. In fact, this resistive load induces parasitic discharging of the capacitors included in the loop filter, thus limiting the gain of this filter to a finite value. For this reason, a relatively high load resistance (ideally infinite) is desired in order to get a high gain of the charge pump/loop filter circuit, which is essential to ensure a phase error close to zero. The maximal adjustable value of the load resistance R_C is determined by the breakdown voltage and especially the saturation voltage of the current switch transistors.

The additional capacitor C_P in the loop filter circuit allows to minimize the undesired ripple included in the output voltage V_{DC}. In fact, this ripple is mainly due to the charge injection by the charge pump and severely distorts the voltage V_{DC}, thus disturbing the VCO operation. C_P is chosen to be about one-fifth to one-tenth of C_S, thereby guarantying a stable operation of the CDR system [60].

The transistors implementing the switch S_1 are biased at a current I_C of 6 mA and a voltage V_{CE} of 1.6 V. The switch transistors for the realization of the switch S_2 are biased at a current I_C of 3 mA and a voltage V_{CE} of 1.6 V. All these transistors feature a size of $1 \times 4\ \mu m^2$. The setting of the loop filter elements accounts for the stability of the CDR system, thereby ensuring a damping factor ζ of at least 0.7 (cf. sec. 2.4.1). Furthermore, the value of the loop filter elements are chosen such that the undesired ripple over the

control voltage is less than 10 mV, as far as the lock state is achieved. With respect to the gain of realized VCO (2.45 GHz/V), this ripple swing induces a relative frequency tuning of far less than 0.1%, which represents a negligible impact on the VCO operation. Thus, R_C, R_S, C_S, and C_P amount to 300 Ω, 500 Ω, 1.6 pF, and 0.15 pF, respectively.

The parasitic discharging of the capacitors C_S and C_P in Figure 5.17 severely limits the amount of maximal achievable dc voltage V_{DC}, regarding variations of the input phase error. This fact negatively affects the performance of the CDR system, thereby limiting the corresponding tracking range. In order to overcome this issue, the charge pump/loop filter circuit is extended by a linear amplifier, whose schematic circuit diagram is shown in Figure 5.18. The role of this amplifier consists in the extension of the interval in which the output signal V_{DC} can be tuned, thereby maintaining the linear relation between the corresponding output voltage signal and the input phase error.

The linear amplifier is composed of a differential amplifier with resistive emitter degeneration, which ensures the aimed linear relation between the output voltage signal and the phase error at the phase detector input. Between the respective collector node of the amplifier transistors and ground, a capacitor (0.1 pF) is set to further reduce the ripple over the arising output voltage signal. These amplifier transistors feature a size of 1×4 μm^2 and are biased by a current source supplying a total current of 10 mA. The respective voltage V_{CE} amounts to 1.6 V. The collector load is a 100 Ω resistance while the degeneration resistance amounts to 150 Ω.

The control voltage can be externally adjusted by means of the connection pad V_{ADJ}. This connection pad allows a coarse tuning of the VCO operation frequency, thus permit-

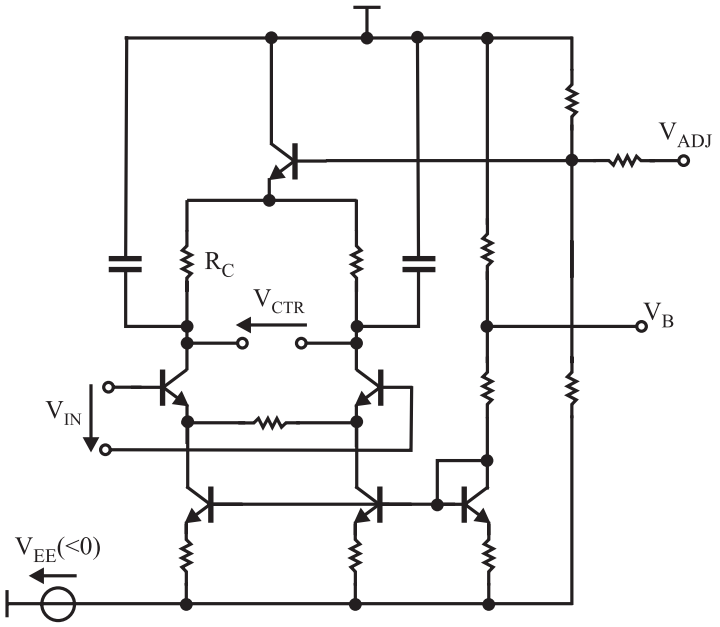


Figure 5.18: Schematic circuit diagram of the linear amplifier responsible for the extension of the tuning range of the control voltage V_{CTR}.

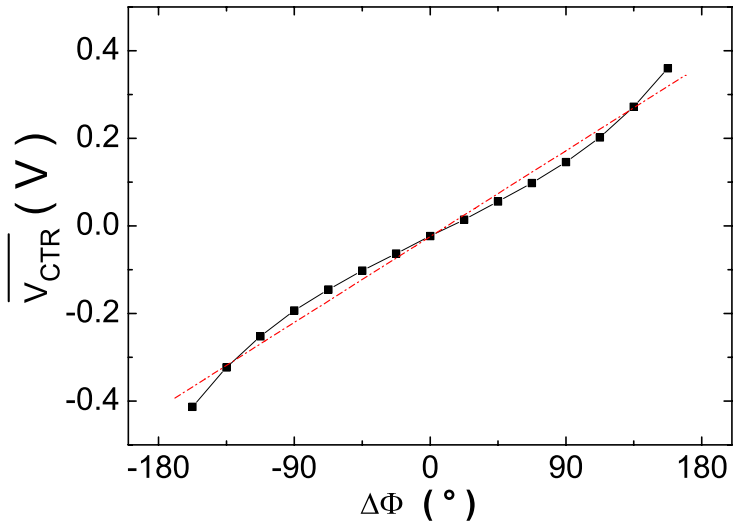


Figure 5.19: Simulated transfer function of the implemented phase detector circuit with the corresponding linear fit (dotted line).

ting to counteract process and temperature variations.

Figure 5.19 shows the simulated transfer function of the phase detector inclusive charge pump and loop filter as well as the linear amplifier. This transfer function is plotted for one period, i.e. for phase error values between $-\pi$ and π (i.e. -180° and 180°). Unlike the ideal transfer function of Figure 5.15, a really linear relation between output control voltage and the input phase error is not achieved. This is due to the already mentioned leakage currents in the charge pump, which are caused by the finite load resistance of the current switches. A linear fit of the simulated transfer function is also represented in Figure 5.19 with a dotted line. From the latter curve, the phase detector gain K_{PD} amounts to 125 mV/rad. Thus, regarding the VCO gain and the value of the loop filter elements, the damping factor of the resulting CDR loop is calculated to be 0.7. In this way, a stable loop is ensured.

5.4 Consideration of Layout Interconnects

Within the phase detector, data feeding and carrying out as well as circuit blocks interconnection and clock distribution require the use of connection lines, which have considerable impact on the circuit performance at the high data rate. This impact may be of destructive form for the circuit operation, thus pointing out the necessity of considering the circuit interconnections during the design phase.

The characterized passive process technology allows the application of two line types for signal guiding. On the one side, matched 50 Ω coplanar lines are used for data feeding

at the phase detector input as well as data carrying out at the corresponding outputs. On the other side, simple metal interconnects are used for circuit blocks interconnection as well as clock distribution within the phase detector, since they occupy less space compared to the coplanar lines counterpart. For the same reason, a transition from coplanar line to simple metal line is performed to drive the input data close to the input buffers preceding the latches L_1 and L_2.

Within the phase detector, the length of the lines serving as interconnects between the circuit blocks are optimized to minimal values ranging between 150 μm and 200 μm. Despite this measure, parasitic oscillations (or ringing) are present at the output of the ECL-based circuit blocks as well as at the input of the current switches driven by the latter circuit blocks, thus severely disturbing the operation of the phase detector. These parasitic oscillations are supported by the low output impedance of the ECL-based circuit blocks as well as the inductive acting connection line in collaboration with the capacitive loading by the following current switches. As illustrated in Figure 5.20, their consistent attenuation is achieved by using 15 Ω damping resistances, which are set in series to the connection lines. Despite a slight degradation in the pulse steepness by applying the latter measure, a proper operation of the phase detector at the aimed data rate is ensured.

Similar to the output of the ECL-based circuit blocks, the respective input of the buffers preceding the latches L_1 and L_2 is particularly exposed to parasitic oscillations. In fact, the emitter followers used in these buffers feature an input impedance with negative real part. The latter negative real part originates from the corresponding capacitive loading at the emitter follower output (e.g. input capacitance of the latch). Furthermore, the imaginary part of the input impedance shows a capacitive behavior. Since simple metal interconnects (optimized minimal length $\approx$ 90 μm) are used for signal guiding close to the buffer input, a favorable environment for parasitic oscillations is given. Therefore, 15 Ω resistances for oscillations damping are applied in series to these simple connection lines.

During the layout of the signal lines, a particular importance is attached to the compliance with a symmetrical architecture. By this measure, advantages of the differential configuration can be fully exploited, such as the minimization of the interactions between

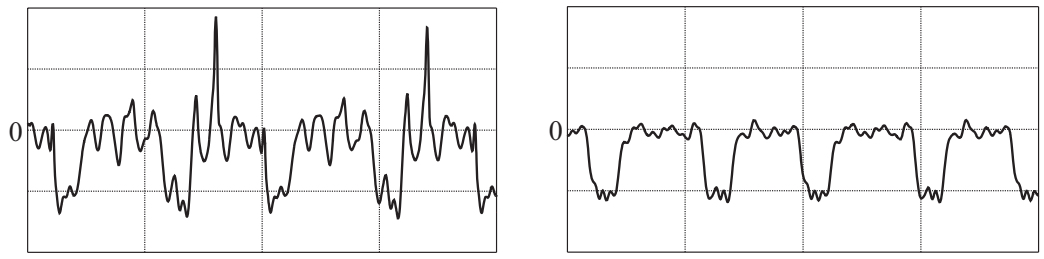


Figure 5.20: (a) Ringing at the output of the ECL-Latch L_1 caused by the connection lines to the gates X_1 and L_3 . (b) Attenuation of the ringing by setting of a 15 Ω damping resistance in series to the connection lines.

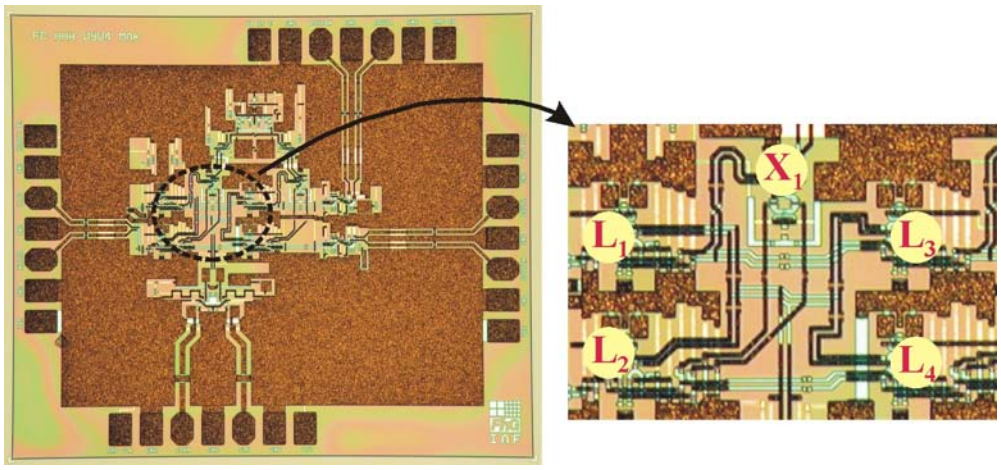


Figure 5.21: Chip photo of the realized phase detector with a section showing the circuit block interconnections.

adjacent (push-pull) signal lines.

The chip photo of the realized phase detector circuit is illustrated in Figure 5.21, which also points out a section showing the circuit block interconnections as well as the clock distribution within the phase detector. The considered circuit blocks are the latches L_1-L_4 and the XOR gate X_1. The integrated circuit features a chip size of 1.5×1.75 mm^2. The corresponding complexity amounts to 150 DHBTs.

The circuit simulations are performed in the simulation environment Cadence (Silvaco), whereas Smartspice serves as the underlying simulator.

5.5 Measurements

5.5.1 Measurement Setup

The measurements of the realized phase detector are performed on-wafer using 65 GHz RF probes for data probing as well as data and clock feeding. The block diagram of the measurement setup is shown in Figure 5.22. The generation of the input data for characterizing the device under test (DUT) is performed using a four-channel pulse pattern generator (PPG, Anritsu MP1758A) as the underlying random data source. The PPG is capable of delivering data at rates up to 12.5 Gbit/s, whereas a word length up to 2^{31}-1 is available for each data channel. Since the functionality of the phase detector circuit has to be tested at data rates up to 80 Gbit/s, the operation range of the PPG, in terms of speed, must be extended. Therefore, the four outputs of the PPG are used to feed two 2:1 multiplexer modules (M10 and M11). These modules are capable of delivering data at rates up to 25 Gbit/s. M10 and M11 serve as data source for a third 2:1 multiplexer module (M2), which delivers data at a speed up to 50 Gbit/s. Finally, the differential data output of the multiplexer module M2 is exploited to feed a fourth 2:1 multiplexer module (M3).

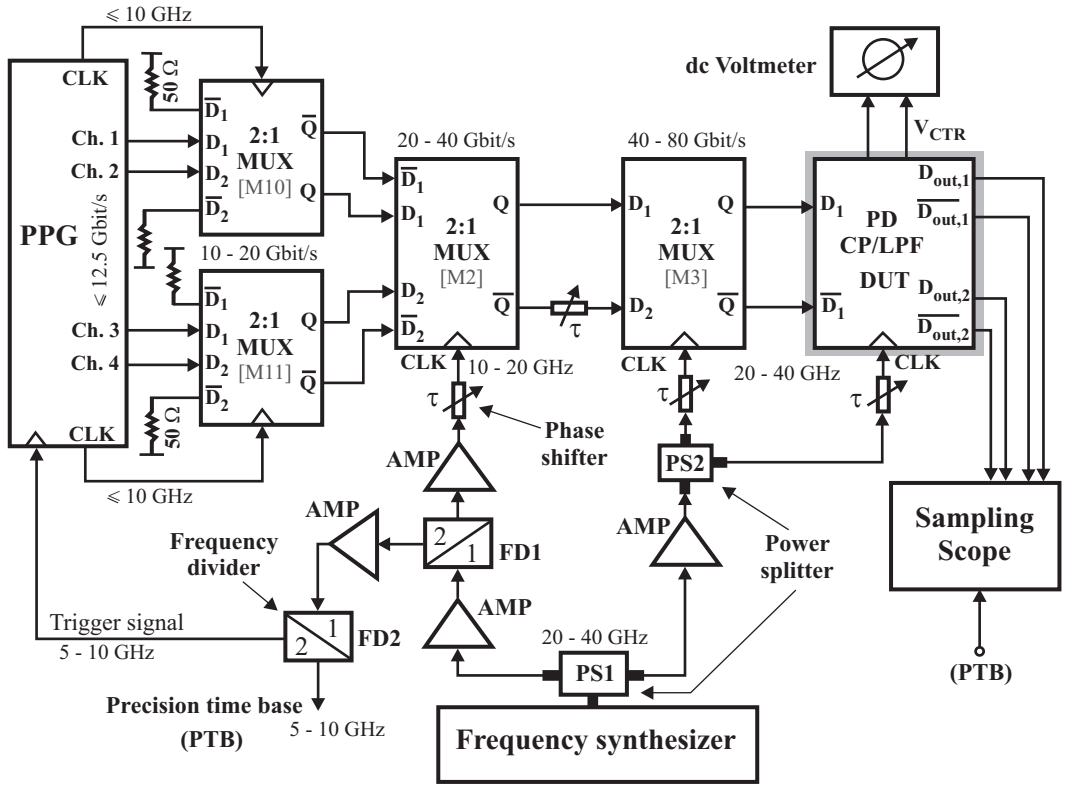


Figure 5.22: Measurement setup used for the characterization of the phase detector circuit.

The latter module generates differential data up to 80 Gbit/s for testing the DUT. All the multiplexer modules are manufactured in-house. The included 2:1 multiplexer chips rely on an in-house metamorphic HEMT technology (AlGaInAs on GaAs, [41]).

The multiplexer modules M10 and M11 require a clock signal featuring frequencies up to 10 GHz for proper data sampling. The inherent frequency source of the PPG covers this frequency range. Therefore, the two frequency signal outputs of the PPG are used for feeding the clock inputs of M10 and M11. For the other multiplexer modules as well as the DUT, a frequency synthesizer (Wiltron 86100B) delivering signal frequencies up to 60 GHz is used as the underlying frequency source. At the output of this frequency synthesizer, a 3 dB power splitter (PS1) is connected for clock signal distribution towards the corresponding inputs of the modules M2 and M3 as well as the DUT. The two outputs of the power splitter is succeeded by an amplifier. This amplifier compensates for the power losses arising from the power splitter. The module M3 and the DUT are clocked at the same frequency corresponding to the highest signal frequency of the measurement setup. That is, the clock feeding path of M3 and the DUT is identical up to a power splitter (PS2). This power splitter drives the frequency signal towards the respective clock input of M3 and the DUT. The two outputs of PS2 are followed by a phase shifter, respectively. This phase shifter is essential for achieving a data sampling in M3 at the best SNR. Furthermore, the phase shifter in the clock feeding path of the DUT allows to achieve a phase state between

input data and clock signal, which corresponds to the lock state of the CDR. Since a single-ended clocking is applied for the phase detector, the corresponding complementary clock input is terminated with a 50 Ω resistance.

The module M2 is clocked at a frequency corresponding to half the sampling frequency of M3. Therefore, a frequency divider (FD1) with differential output is added in the clock feeding path of M2. The clock input of M2 is fed by a single-ended frequency signal, thus requiring one output of FD1. The latter output of FD1 is followed by an amplifier providing sufficient high signal swing for proper data clocking. Similar to the clock input of M3, a phase shifter is used for phase adjustment between input data and clock signal.

The frequency signal arising from the complementary output of FD1 is guided to a second differential frequency divider (FD2) through an amplifier. FD2 allows to generate a clock signal for triggering the PPG. Furthermore, the complementary output of FD2 is used to supply the so-called precision time base (PTB) signal. In fact, the input and output data of the DUT are observed using a sampling scope (Agilent 86100B) with a bandwidth of 70 GHz. The PTB signal allows to eliminate the inherent jitter of this sampling scope during the measurements. This PTB signal is effective only for exclusive frequency windows (given by the scope): 9 GHz - 12.6 GHz, 18 GHz - 25 GHz, and 39 GHz - 45 GHz.

The 80 Gbit/s data signal generated by the measurement setup for testing the DUT is illustrated in Figure 5.23. This data signal features an amplitude swing of 600 mV_{pp}, while the eye opening amounts to about 270 mV. Figure 5.24 and Figure 5.25 show photographs of the different sections forming the measurement setup of the phase detector. The measurement components introduced in the previous paragraphs as well as in Figure 5.22 are also highlighted.

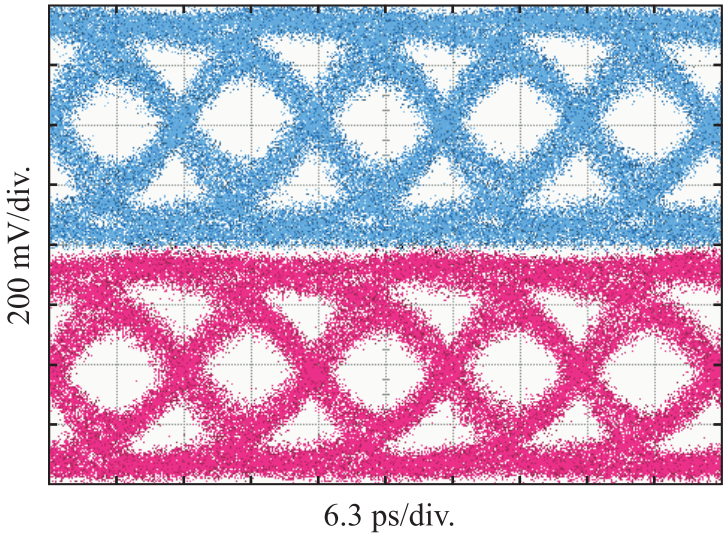
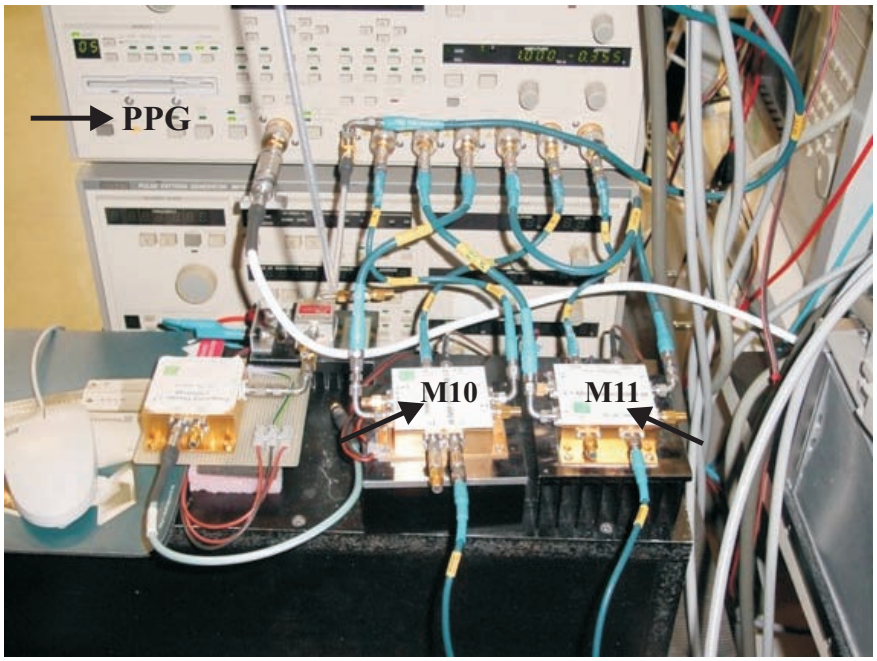
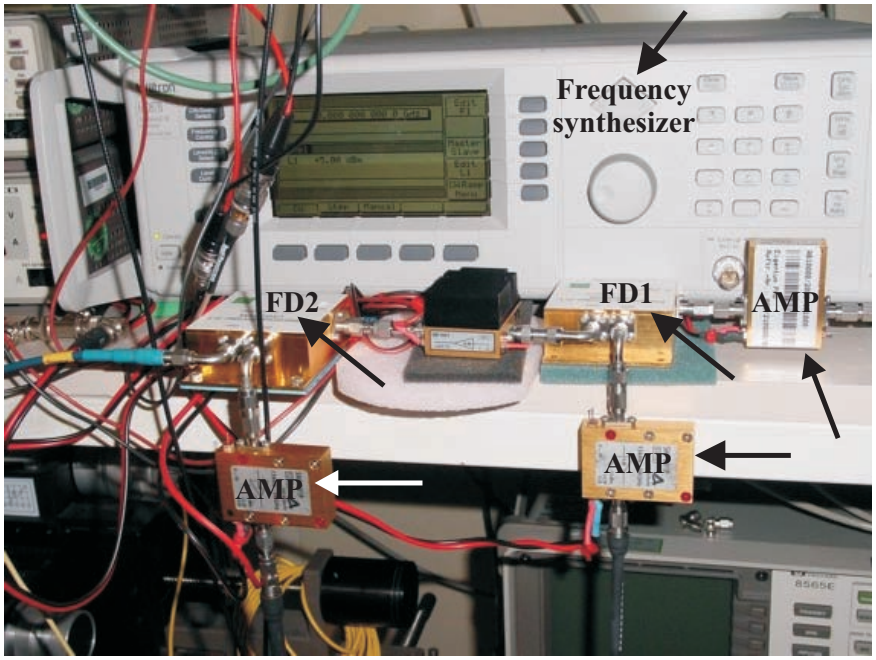


Figure 5.23: Generated 80 Gbit/s data signal using the measurement setup of Figure 5.22 for broadband testing of the realized phase detector. The data signal features an amplitude swing of 600 mV, while the eye opening amounts to about 270 mV.

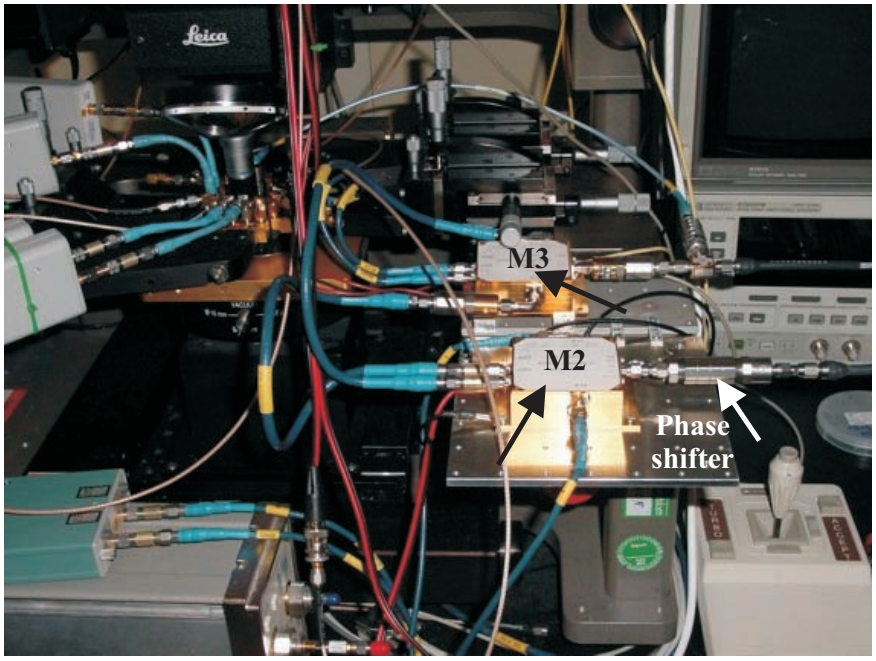


(a)

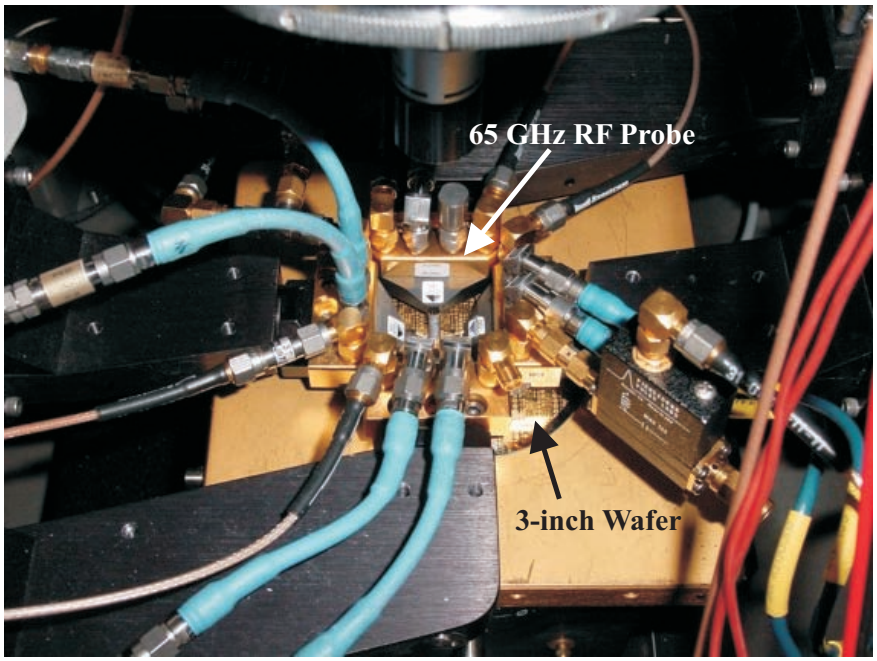


(b)

Figure 5.24: Photograph of the sections building the measurement setup used for characterizing the phase detector: (a) PPG, multiplexer modules M10 and M11. (b) Frequency synthesizer, AMP, FD1, and FD2.



(a)



(b)

Figure 5.25: Photograph of the sections forming the measurement setup used for characterizing the phase detector: (a) Multiplexer modules M2 and M3. (b) 3-inch Wafer and 65 GHz RF probes.

5.5.2 Discussion of the Results

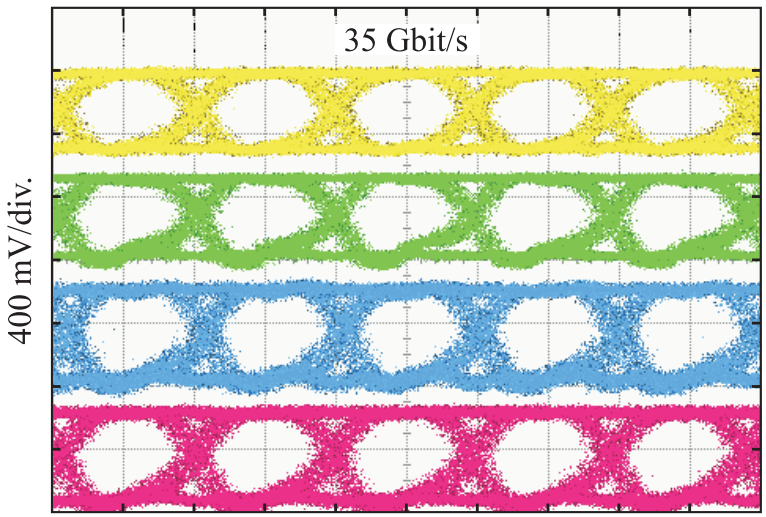
The realized phase detector allows the test of two functions, which are essential during the operation of a complete clock and data recovery circuit. On the one hand, the data recovery is tested, whereas the phase detector acts as an 1:2 demultiplexer. On the other hand, the generation of the dc control voltage V_{CTR} for the frequency tuning input of the VCO is investigated.

The phase detector features proper (broadband) data regeneration up to the maximum input data rate delivered by the data source. This fact is illustrated in Figure 5.26(a) and Figure 5.26(b), showing the differential eye diagrams at the data output for 70 Gbit/s and 80 Gbit/s input data, respectively. An essential control parameter for achieving these results is the phase shifter in the clock feeding path of the phase detector. As already discussed in the previous section, the latter phase shifter allows to simulate the lock state of the CDR loop. In this state, the data are clocked at the best SNR, as is generally known. The voltage swing of the recovered data merges with the eye opening, thereby amounting to approximately 600 mV_{pp}. This value agrees well with that simulated during the design phase.

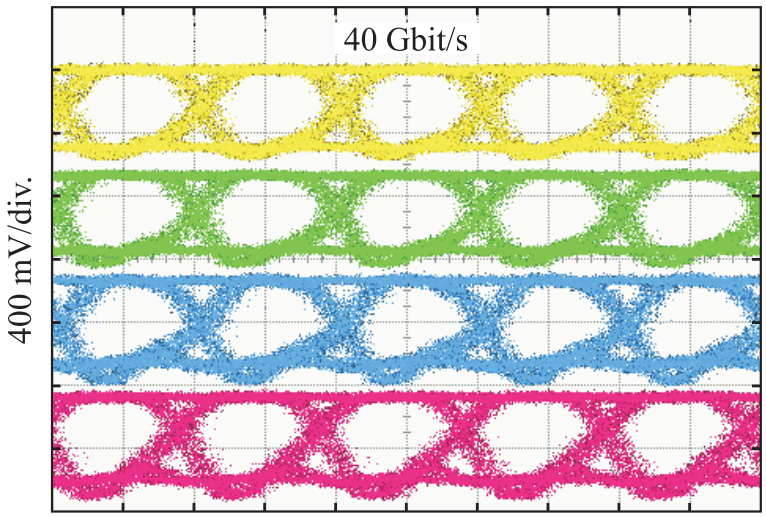
The generated voltage V_{CTR} is measured at the carried out output of the linear amplifier succeeding the charge pump/loop filter circuit. By varying the phase between data and clock using the aforementioned phase shifter, the total tuning range of V_{CTR}, observed at a voltmeter, amounts to about 200 mV, while the simulated tuning range is 800 mV (cf. Figure 5.19). The observed deviation of the measured tuning range from the simulated one is due to process variations, as the NiCr resistances were found to be 20% lower than the nominal value. As a consequence, the gain of the charge pump/loop filter circuit as well as that of the succeeding linear amplifier are severely affected, thus resulting in a smaller tuning range of V_{CTR}. However, by means of the carried out bias pads in the charge pump/loop filter circuit as well as in the linear amplifier, the observed deviation can be considerably reduced. The phase shifter used in the clock feeding path does not allow an unique phase assignment between data and clock. As a consequence, the transfer characteristic of the phase detector cannot be measured.

The clear eye opening of the phase detector output signals at 80 Gbit/s proves their suitability for data regeneration at higher data rates. Since no data source is available for measurement at data rates over 80 Gbtit/s, the functionality of the phase detector is tested using a clock signal with a frequency corresponding to the aimed data rate. Furthermore, data with a speed corresponding to half the targeted data rate are fed at the phase detector input. Thus, the phase detector features a proper operation up to 50 Gbit/s input data and 50 GHz clock frequency (see Figure 5.27), which corresponds to 100 Gbit/s operation. That is, 50 Gbit/s data are available at the phase detector output. These data feature an eye opening as well as a voltage swing of approximately 440 mV_{pp}.

The phase detector circuit features a power consumption of about 1.5 W at a single supply voltage of -5 V.



(a)



(b)

Figure 5.26: Demultiplexed differential output eye diagrams of the phase detector for: (a) 70 Gbit/s input data. (b) 80 Gbit/s input data. The output voltage swing at both data rates amounts to 600 mV_{pp}.

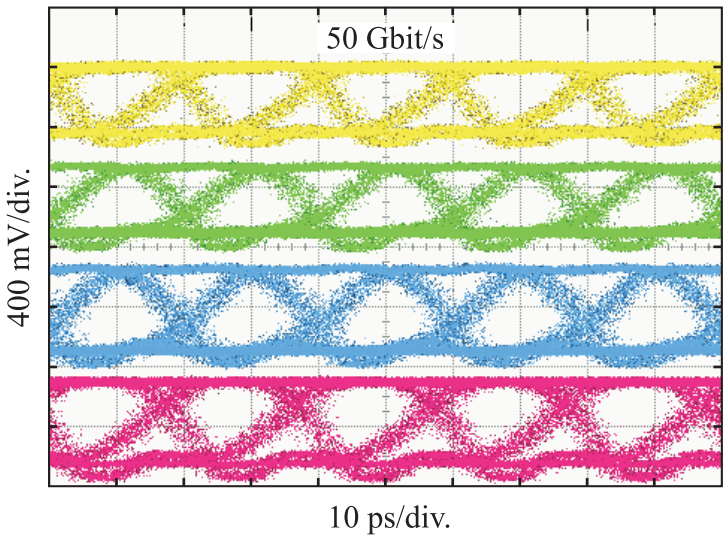


Figure 5.27: Demultiplexed differential output eye diagrams of the phase detector for 50 Gbit/s input data and 50 GHz clock signal.

5.6 Summary

In this chapter, a linear half-rate phase detector with 1:2 DEMUX has been designed and realized. This phase detector is intended for use in half-rate clock and data recovery circuits at a data rate of 80 Gbit/s. In order to get the phase detector operating at such a high data rate, design aspects have been discussed and suitable concepts assumed. Thus, the implemented circuit blocks within the phase detector are of differential topology, whereas the concept is based on the emitter-coupled logic technique. The implementation of the logic gates requiring more than one logical input is performed using the series-gating technique. Within the circuit blocks, a suitable choice of the transistor size as well as an optimisation of the resistive load and the output voltage swing are performed in order to minimize the gate delay.

A charge pump/loop filter circuit has been monolithically integrated with the phase detector, thus allowing a clear interpretation of the dc signal delivered by the phase detector for frequency tuning in the CDR circuit.

The possible destructive effect of layout interconnects on the circuit performance is discussed, pointing out the importance of considering the connection lines (within the circuit) during the design phase.

For characterizing the realized circuit, a measurement system has been set up. This measurement system is composed, to some extent, of in-house manufactured 2:1 multiplexer modules, which allow a circuit characterization up to 80 Gbit/s. Thus, concerning the data regeneration, the realized phase detector has been successfully tested at data rates up to 80 Gbit/s. The latter result agrees well with the simulation, thus proving the suitability of the used design technique for high data rate applications. Moreover, the capability of the phase detector for operating at data rates well beyond 80 Gbit/s has been

proven. Compared with the state-of-the-art, the full demultiplexer included in the phase detector features the highest data rate ever achieved for any HBT-based demultiplexer. Furthermore, the potential for demultiplexing operation at data rates over 80 Gbit/s has been proven.

Chapter 6

Clock and Data Recovery Circuits up to 80 Gbit/s

The main circuit components necessary for the implementation of a clock and data recovery circuit have been successfully designed and realized, as reported in Chapter 4 and Chapter 5. The performance achieved by these components proves the feasibility of a CDR circuit at data rates over 80 Gbit/s. Thus, the next development step consists in confirming the aforementioned feasibility by a monolithic integration of the CDR circuit components.

This chapter deals with the design and realization of two fully integrated half-rate clock and data recovery circuits. These two CDR circuits aim applications at data rates of 70 Gbit/s and 80 Gbit/s, respectively. The 70 Gbit/s CDR circuit was intended as a kind of back-up, since no reliable data source beyond 70 Gbit/s was available at the time of the design phase. Subsequently, as presented in sec. 5.5, an (in-house) 2:1 multiplexer module with maximum operation speed of 80 Gbit/s has been successfully mounted and packaged. Thus, this multiplexer module allows a successful testing of the 80 Gbit/s CDR circuit. According to the applied half-rate principle, the monolithically integrated frequency sources have to deliver 35 GHz and 40 GHz for optimal data clocking at 70 Gbit/s and 80 Gbit/s, respectively. The concepts for the circuit components included in the CDR are completely assumed from the latter chapters. However, interface circuits are necessary to connect the CDR main components together, whereas the resulting configuration forms the well-known CDR loop. Thus, the first part of this chapter consists in the design and implementation of the CDR loop with the corresponding components, whereas this development task is essentially based on a circuit simulation level. The second part deals with the presentation of the achieved performance by the realized CDR circuits, whereas the two CDR functions are pointed out. Finally, as usual, the chapter is closed by a summary.

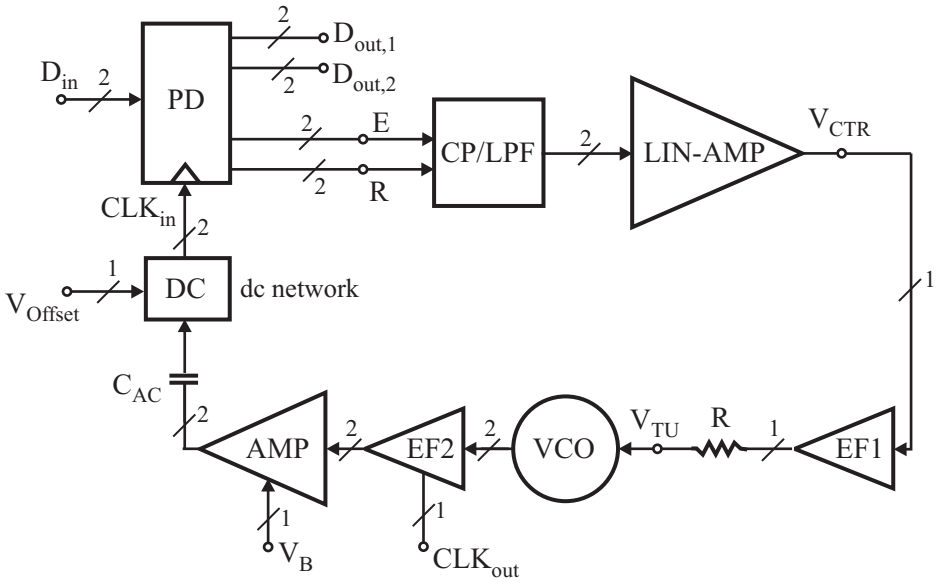


Figure 6.1: Block diagram of the implemented 70 Gbit/s and 80 Gbit/s CDR circuits.

6.1 Circuit Design

The circuit components included in the 70 Gbit/s and 80 Gbit/s CDR loop are shown in the circuit block diagram of Figure 6.1, representing the latter CDR loop. Except for the VCO, all other components are identical for both CDR circuits. The function, the operation principle, and the implementation of most of these components are addressed in the previous chapters. This is the case for the phase detector (PD), the charge pump/loop filter (CP/LPF), and the linear amplifier (LIN-AMP), which are discussed in Chapter 5, while the voltage controlled oscillator (VCO) is addressed in Chapter 4.

6.1.1 Signal Feeding at the VCO Frequency Tuning Input

The dc output voltage V_{CTR} generated by the component LIN-AMP is transferred to the frequency tuning input V_{TU} of the VCO through a circuit interface. This circuit interface is composed of an emitter follower (EF1 in Figure 6.1), which provides the necessary dc level shift for the right operation point setting of the varactors in the VCO. That is, in the absence of data transitions at the phase detector input, the adjusted voltage V_{TU} sets the VCO frequency at a value of 35 GHz (regarding the 70 Gbit/s CDR) or 40 GHz (regarding the 80 Gbit/s CDR). Using the 43 GHz VCO implemented in Chapter 4, a slight change in the resonator dimension is necessary to move the VCO center frequency to 35 GHz and 40 GHz, respectively. With the latter frequencies, the basic condition for CDR locking to 70 Gbit/s and 80 Gbit/s input data is given.

In order to suppress possible common mode oscillations at the shared connection point of both push-pull varactors, a damping resistance is set between the emitter follower output and the frequency tuning input of the VCO. In this VCO, the internal voltage source for bias setting of V_{TU} (cf. Figure 4.21) is eliminated, since V_{TU} is delivered externally.

6.1.2 Signal Feeding at the Clock Input of the Phase Detector

The frequency signal extracted by the VCO is guided by the clock distribution lines to the corresponding clock inputs of the latches included in the phase detector. A driving of these distribution lines, directly from the VCO output, affects the performance of the VCO core. In fact, the power matching at the VCO output necessary for providing sufficiently high signal swing for data clocking can not be performed without considering the characteristics of the VCO core (e.g.: center frequency, signal swing within the resonator, saturation voltage of the cascode transistors). Therefore, an additional buffer amplifier is connected between the VCO output and the clock input of the phase detector, whereas a dc-coupling (via an one-stage emitter follower: EF2 in Figure 6.1) ensures the electrical connection between the VCO output and the amplifier. Thus, the role of the latter amplifier consists in the driving of the clock distribution lines, thereby providing a sufficient high voltage swing at the clock input of the latches. Furthermore, it allows to enforce the reverse isolation effect of the cascode stage (within the VCO), thus minimizing the negative impact of the input data feedthrough to the VCO core. In fact, the random arrival of the data transitions may introduce jitter at the VCO output.

Figure 6.2 shows the schematic circuit diagram of the buffer amplifier serving as interface between the VCO output and the clock input of the phase detector. It is implemented using an emitter-coupled differential amplifier. At the collector of the amplifier transistors, a serial network composed of an inductor and a load resistance is set. The inductor helps achieving sufficient high output voltage swing for a proper operation of the latches in the phase detector. This inductor is preferred to the inductively acting coplanar lines, since the layout space requirement is much lower. Furthermore, the proper operation of the phase detector does not depend upon an exact achievement of the inductance value. A transistor current source is used for current feeding, thus allowing a later adjustment of the output signal amplitude by an externally connected voltage source. The switch transistors are biased at a current I_C of 10 mA and a voltage V_{CE} of 1.6 V. The resistive load R_C amounts to 35 Ω while the serial inductance amounts to approximately 200 pH.

The output signal of the buffer amplifier is fed to the clock input of the phase detector using ac-coupling. The latter method is preferred to the dc-coupling counterpart, since it allows overcoming possible dc-offset originating from the differential output of the buffer amplifier. Furthermore, the use of emitter follower (two-stage emitter follower in this case) for dc level shift can be omitted. Thus, the output of the buffer amplifier corresponds to a CML output, which allows a considerable minimization of the dc power consumption at the clock input of the phase detector. The dc voltage setting of the current switch transistors at the phase detector clock input is performed using a resistive voltage divider (dc network in Figure 6.1). The corresponding schematic circuit diagram is illustrated in Figure 6.3.

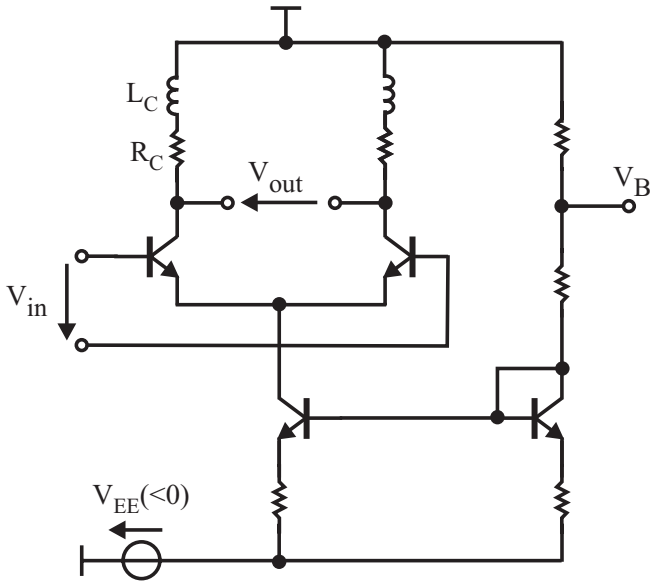


Figure 6.2: Schematic circuit diagram of the buffer amplifier (AMP) used between the VCO output and the clock input of the phase detector (PD).

An external voltage connection (V_{Offset} in Figure 6.1) is intended for offset correction due to possible unsymmetry between the complementary clock signals.

The monitoring of the clock signal extracted within the CDR is performed by carrying out a single-ended output of the VCO to an output pad. The VCO output signal is tapped in the dc-coupling stage succeeding the VCO, whereas a buffer in form of one-stage emitter follower is used for minimizing the influence of the measurement setup on the

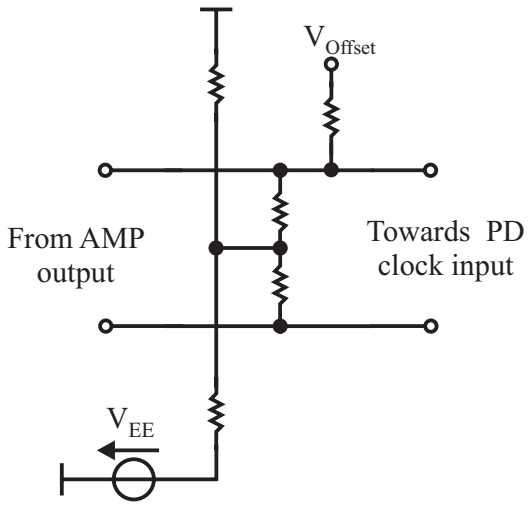


Figure 6.3: Schematic circuit diagram of the voltage source used for the bias point setting of the clock switch transistors within the phase detector.

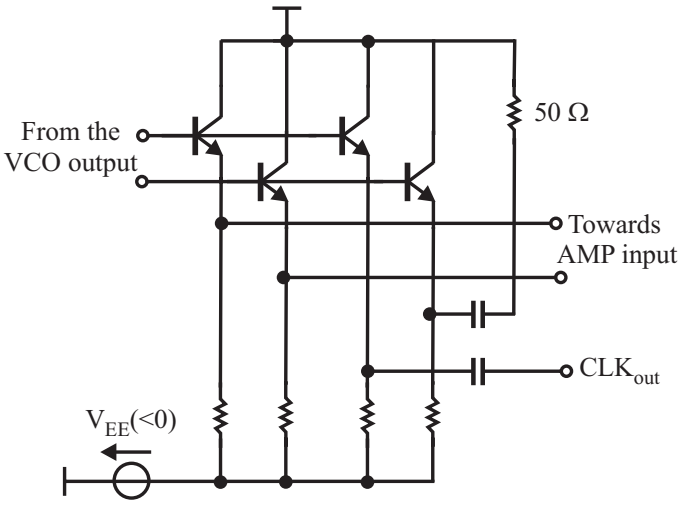


Figure 6.4: Emitter follower buffer used to transfer the VCO output signal to the amplifier (AMP) and to the output CLK$_{out}$ for clock extraction monitoring.

operation of the CDR loop (see Figure 6.4). Since only one signal output is necessary for clock extraction monitoring, the complementary output is terminated with a 50 Ω resistor representing the load of the measurement system. The transistors building the emitter followers in Figure 6.4 are biased at a current I_C of 4 mA and a voltage V_{CE} of 1 V.

The design and simulation of the total CDR circuit is performed in the simulation environment Cadence (Silvaco). Similar to the design of the phase detector, the underlying simulator is Smartspice. Figure 6.5 shows the simulated behavior of the differential signal $V_{CTR,diff}$ at the output of the component LIN-AMP when the CDR locks to 80 Gbit/s input data. After a transient phase, $V_{CTR,diff}$ settles at a value of approximately 0 V, thereby indicating the achievement of the optimal clock signal frequency by the VCO as well as the optimal phase state between the 80 Gbit/s input data and the 40 GHz clock signal.

The chip photographs of the realized 70 Gbit/s and 80 Gbit/s CDR circuits are shown in Figure 6.6 and Figure 6.7, respectively. The main components forming the CDR circuit are pointed out. The VCO and the corresponding buffer amplifier are placed as close as possible to the clock input of the phase detector, thus avoiding additional connection lines, which may negatively impact on the circuit performance. The latter measure is performed at the cost of the length of the connection line from the output of the component LIN-AMP to the frequency tuning input of the VCO. However, the latter connection line does not negatively affect the operation of the CDR loop, since the transferred signal on this line is more ore less a dc signal. For both CDR circuits, the chip size is 1.75 × 1.75 mm^2. The circuit complexity is 170 DHBTs.

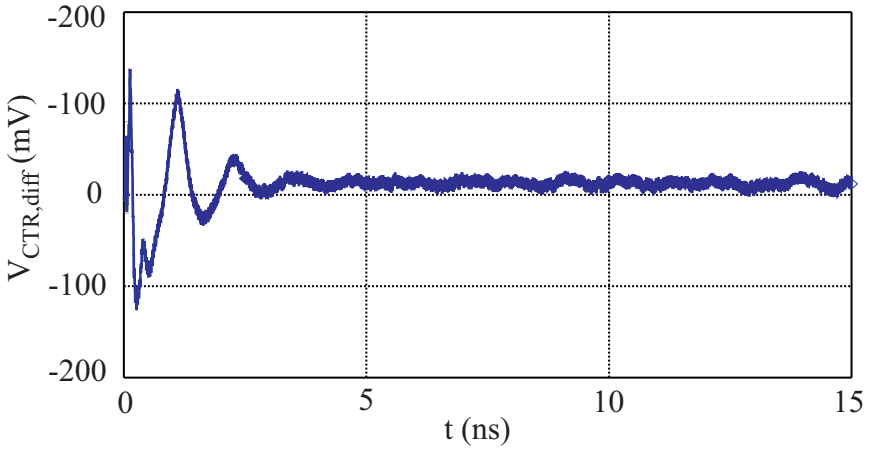


Figure 6.5: Simulated variation in time of the differential ouput signal $V_{CTR,diff}$ as the CDR loop locks to 80 Gbit/s input data.

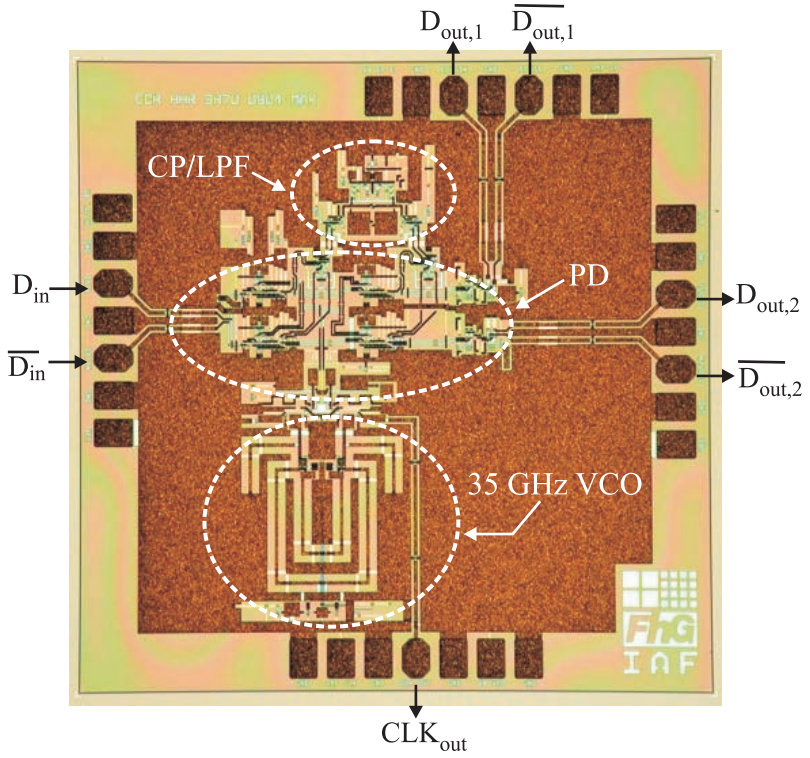


Figure 6.6: Chip photograph of the realized 70 Gbit/s CDR circuit. The chip has a size of 1.75×1.75 mm^2.

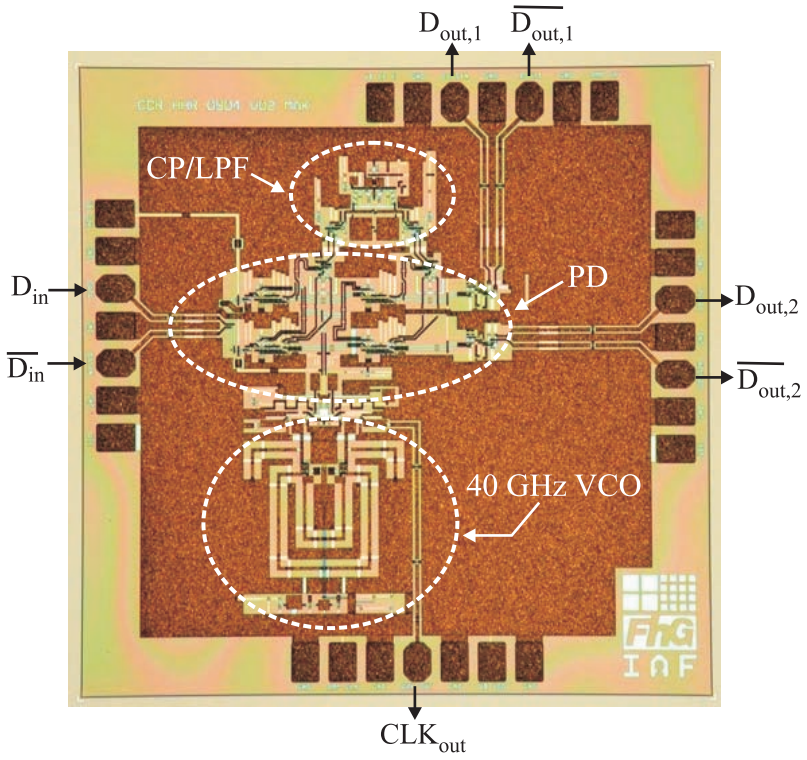


Figure 6.7: Chip photograph of the realized 80 Gbit/s CDR circuit. The chip has a size of 1.75×1.75 mm^2. A readjustment of the lines length in the VCO resonator, compared to the analog resonator in Figure 6.6, is necessary for achieving the higher clock frequency.

6.2 Results

6.2.1 Measurement Setup

The measurements on the realized CDR circuit are performed on-wafer. Figure 6.8 illustrates the measurement setup used for the characterization of the CDR circuit. This measurement setup is similar to that applied for the measurements performed on the phase detector (cf. sec. 5.5), concerning the input data generation as well as the probing and monitoring of the recovered data. Since the clock signal is generated in the CDR circuit, no external frequency source is necessary for operating the latter circuit. However, a spectrum analyzer (HP 8565E) is used to monitor the clock extraction by the VCO. Since the extracted clock signal is stabilized by the CDR loop, reliable phase noise measurements are also performed using the latter spectrum analyzer. Furthermore, measurements of the clock signal on the time base are performed using the same sampling oscilloscope as that used for output data observation.

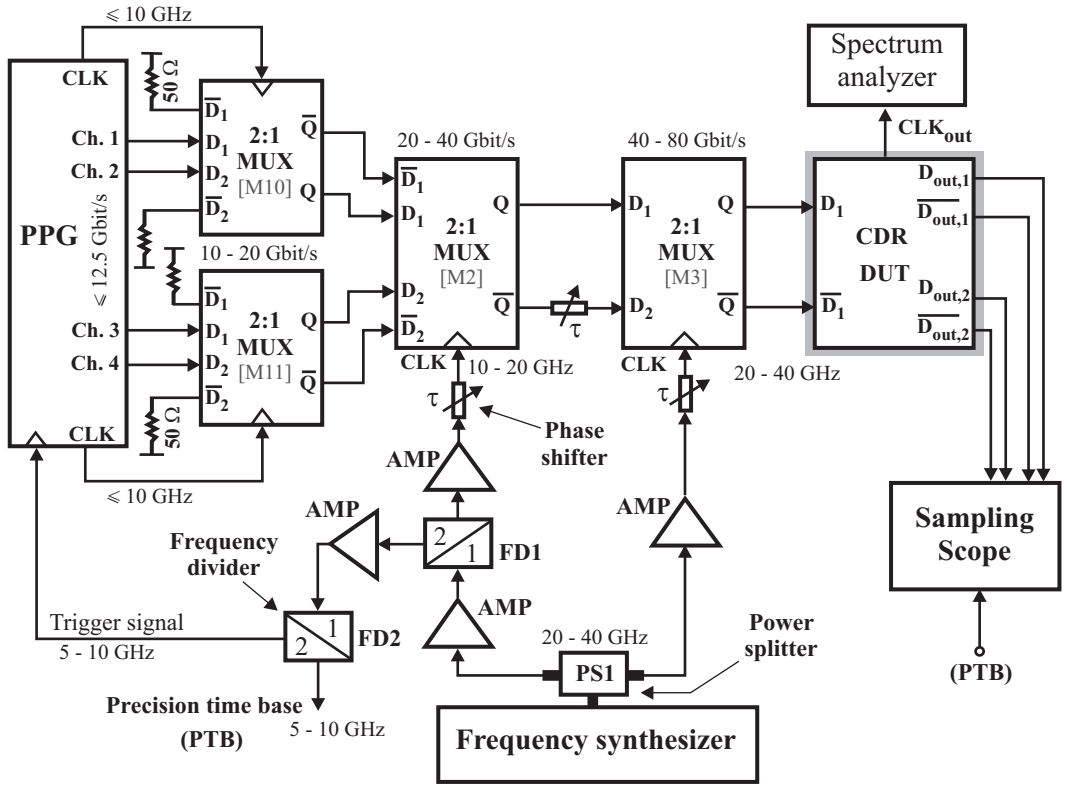


Figure 6.8: Measurement setup used for the characterization of the 70 Gbit/s and 80 Gbit/s CDR circuits.

6.2.2 Discussion of the Results

70 Gbit/s CDR

The measurements on the CDR circuit consist in the investigation of the two CDR functions: data regeneration and clock recovery. Concerning the data regeneration, the realized CDR confirms the performance achieved by the phase detector for 70 Gbit/s input data. Thus, as the CDR loop locks to the input data at the aforementioned data rate, a proper data regeneration is observed at the CDR data outputs. This is illustrated in Figure 6.9, showing the eye diagrams of the demultiplexed data at the two differential outputs of the CDR circuit. The regenerated 35 Gbit/s data feature clear eye opening with a voltage swing of approximately 600 mV_{pp}. This voltage swing merges with the eye opening of the data, thus proving the high-speed potential of the circuit. An essential feature for achieving this proper operation of the CDR circuit is the externally connected voltage V_{Offset} (cf. Figure 6.1). In fact, the latter voltage allows to counteract potential asymmetry (e.g.: dc voltage offset) between the nominal push-pull signals at the clock input of the phase detector.

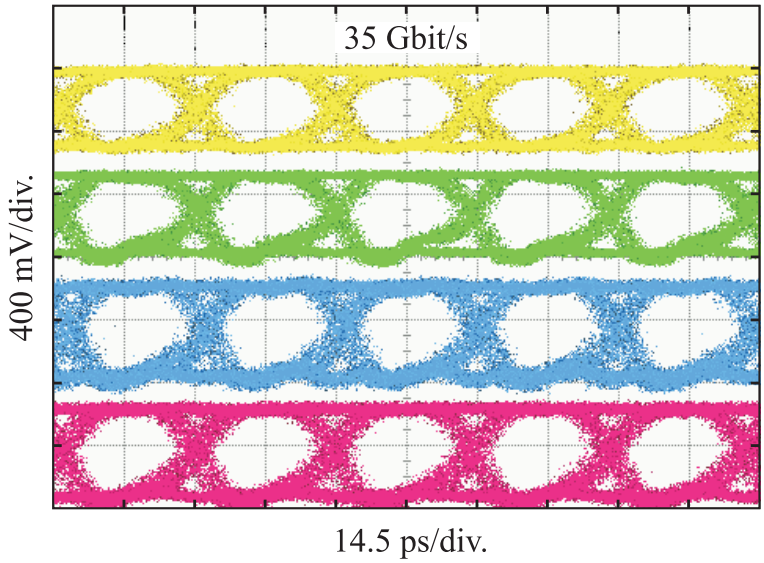


Figure 6.9: Demultiplexed and recovered 35 Gbit/s data at the differential outputs of the 70 Gbit/s CDR circuit. The voltage swing amounts to approximately 600 mV_{pp}.

The spectrum of the extracted 35 GHz clock signal from the 70 Gbit/s input data is shown in Figure 6.10. The latter clock signal features a very low phase noise of approximately -99 dBc/Hz at 100 KHz offset from the carrier. However, at offset frequencies below 25 KHz as well as frequencies beyond 100 KHz, the phase noise behavior is essentially determined by the measurement setup, especially by the signal quality at the CDR input. Within these offset frequency ranges, the noise generated by the measurement setup corresponds more or less to a broadband noise, as illustrated in Figure 6.11. The extracted 35 GHz clock signal features a peak-to-peak (pp) time jitter as low as 1.4 ps (see Figure 6.12), while the measured rms jitter amounts to 0.27 ps.

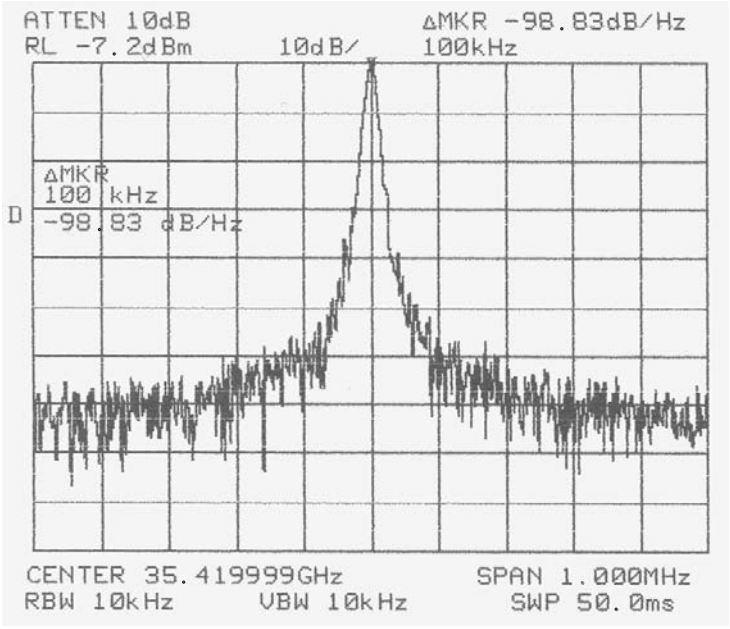


Figure 6.10: Spectrum of the extracted 35 GHz clock signal.

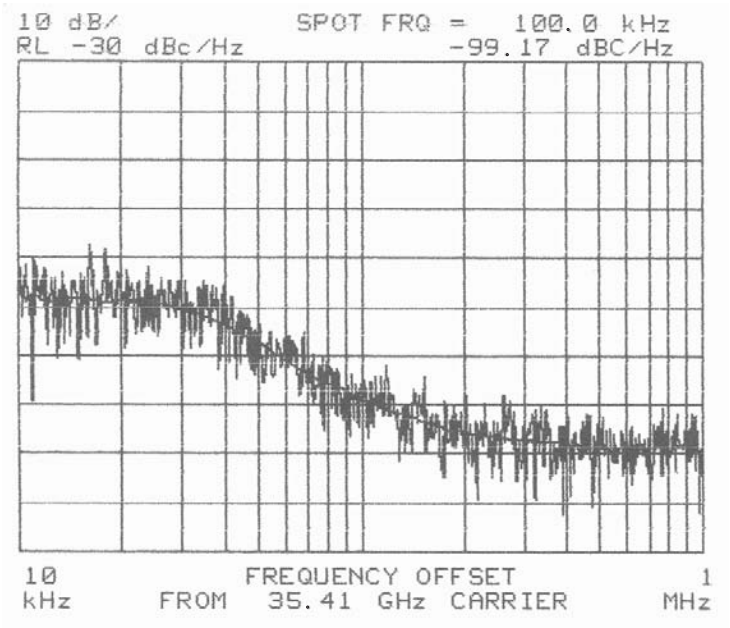


Figure 6.11: Roll-off of VCO phase noise vs. offset frequency for the CDR loop locking to 70 Gbit/s input data.

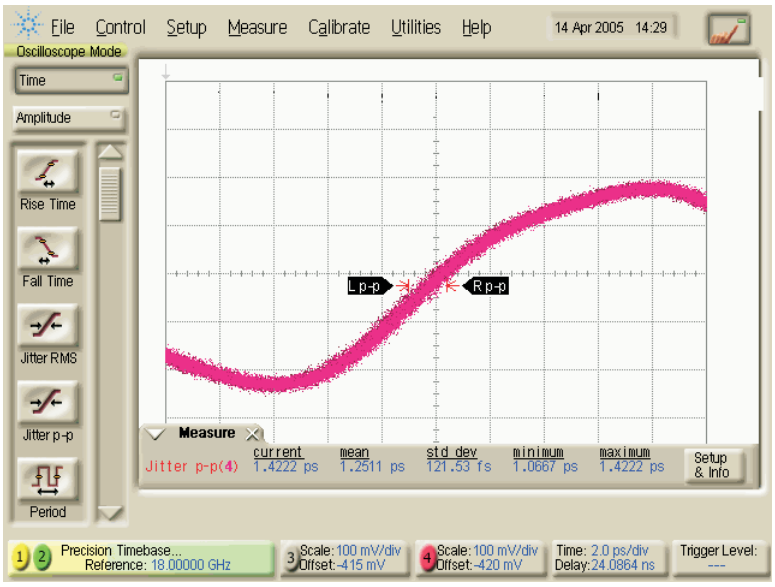


Figure 6.12: Peak-to-peak time jitter measurement of the extracted 35 GHz clock signal.

80 Gbit/s CDR

Figure 6.13 illustrates the recovered and demultiplexed 40 Gbit/s differential data as the CDR loop locks to 80 Gbit/s input data. Similar to the data at the differential outputs of the 70 Gbit/s CDR circuit, the output data of the 80 Gbit/s CDR feature clear eye opening with a voltage swing of approximately 600 mV_{pp}. Since the eye opening still merges with the voltage swing at 80 Gbit/s, higher data rates can indeed be processed by the CDR circuit.

The spectrum of the extracted 40 GHz clock signal from the 80 Gbit/s input data is illustrated in Figure 6.14. A very low phase noise of approximately -98 dBc/Hz is measured at 100 KHz offset from the carrier. As logically expected, the latter phase noise performance is very close to that achieved by the 70 Gbit/s CDR, thus proving the consistency of the circuit concept as well as the measurement results. In the time domain, the extracted 40 GHz clock signal features a peak-to-peak time jitter of 1.6 ps (see Figure 6.15) while the measured rms jitter amounts to 0.365 ps.

Regarding both CDR circuits, the locked CDR loop is capable of tracking input data rate variations, which correspond to a clock signal frequency range of 100 MHz. In other words, the tracking range of the CDR amounts to 100 MHz. The CDR circuits consume a power of $P_{DC} = 1.65$ W at a single supply voltage of $V_{EE} = -4.8$ V.

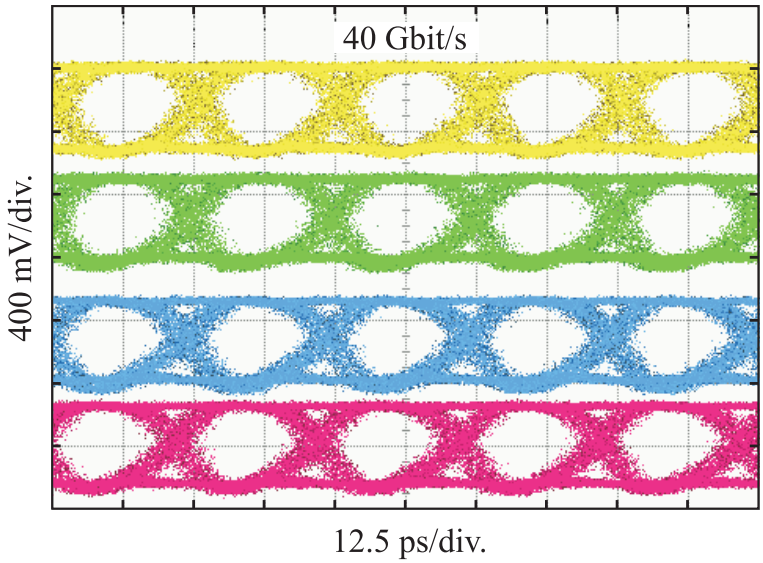


Figure 6.13: Demultiplexed and recovered 40 Gbit/s data at the differential outputs of the 80 Gbit/s CDR circuit. The voltage swing amounts to approximately 600 mV_{pp}.

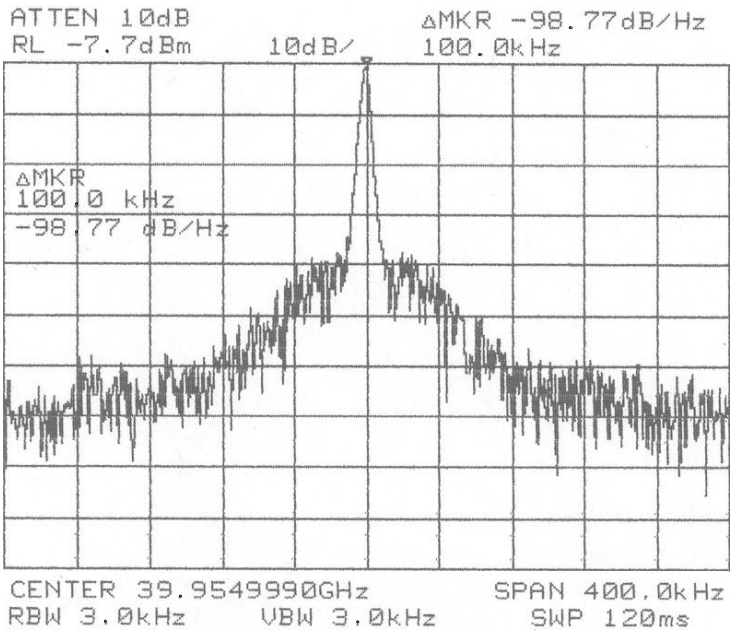


Figure 6.14: Spectrum of the extracted 40 GHz clock signal.

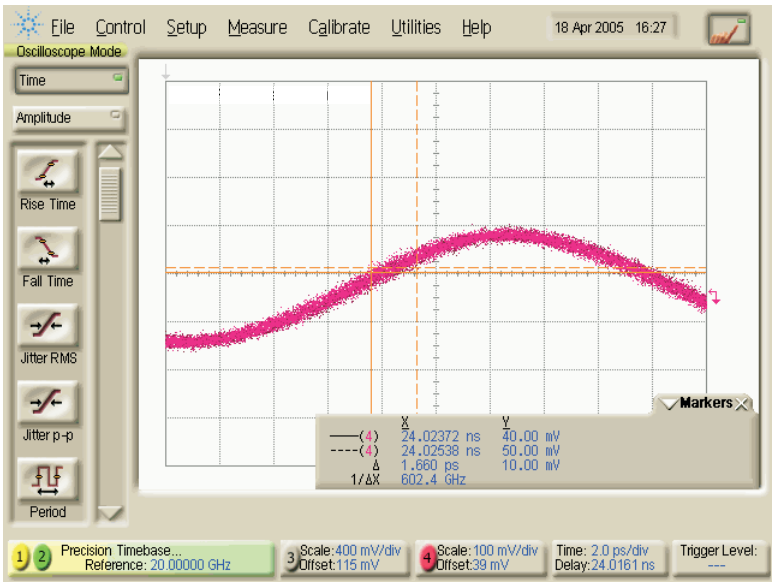


Figure 6.15: Peak-to-peak time jitter measurement of the extracted 40 GHz clock signal.

6.3 Summary

In this chapter, two monolithically integrated half-rate clock and data recovery circuits have been successfully designed and realized. These circuits have been optimized for proper operations at 70 Gbit/s and 80 Gbit/s. The circuit concepts as well as the implementation of the main components (namely: VCO, phase detector, charge pump, and loop filter) included in the CDR have been completely taken from the development performed in Chapter 4 and Chapter 5. The circuit interfaces necessary to connect the latter components for forming the CDR loop have been developed, respecting the circuit design technique defined in Chapter 5.

The performance achieved by the realized CDR circuits is well predicted by the circuit simulation, thus proving the reliability of the design technique for achieving high-speed operations. With respect to the proper operation achieved at the data rate of 80 Gbit/s, this work represents the first demonstration of a monolithically integrated CDR circuit, regardless of all competing technologies. The VCO included in each of the realized CDR circuits features very low phase noise. Furthermore, the extracted clock signal for both CDR circuits shows low peak-to-peak time and rms jitter values. Table 6.1 confronts the performance achieved by the 80 Gbit/s CDR circuit with state-of-the-art performance in the same and in other technologies.

Reference	[50] ('03)	[56] ('02)	[54] ('01)	**This work [47]**
Technology	SiGe BiCMOS	InP HBT	InP HEMT	**InP HBT**
Operation speed	43 Gbit/s	40 Gbit/s	43 Gbit/s	**80 Gbit/s**
rms Jitter	0.23 ps	0.946 ps	1.2 ps	**0.365 ps**
pp Jitter	n.a.	6.67 ps	n.a.	**1.66 ps**
Tracking range	n.a.	n.a.	n.a.	**100 MHz**
SSB PN	-109 dBc/Hz $f_0 = 10$ GHz $f_m = 1$ MHz	n.a.	-102dBc/Hz $f_0 = 43$ GHz $f_m = 1$ MHz	**-98 dBc/Hz** $f_0 =$ **40 GHz** $f_m =$ **100 KHz**
P_{DC}	1.3 W	1.71 W	2.79 W	**1.65 W**

Table 6.1: Comparison of this work with the state-of-the-art. Abbreviations: SSB PN = Single-sideband phase noise; f_0 = Clock frequency; f_m = Offset frequency.

Chapter 7

High-speed Data Sources: > 80 Gbit/s Multiplexing Circuits

The successful testing of high-speed CDR circuits assumes the availability of a data source capable of generating data at the required high speed. Multiplexer (MUX) circuits play a key role in the generation of such high-speed data, as illustrated in the block diagram of the measurement setup used for testing the CDR circuit in sec. 6.2.1. However, the set of multiplexer modules used for data signal generation can deliver data up to a maximum rate of 80 Gbit/s, thereby preventing the testing of the proper operation of the fully integrated CDR circuit at higher data rates. Indeed, the performance achieved by the respective components of the latter CDR circuit proves possible CDR operations at data speed over 80 Gbit/s.

This chapter deals with the design and realization of multiplexing components which are intended for use as data source capable of delivering data at rates over 80 Gbit/s. The first part of the chapter addresses the operation principle of the applied multiplexer concept. Then, the implementation of the presented concept is discussed, whereas two versions for implementing the multiplexing components are introduced. The first version is the so-called selector which features low complexity as well as very high speed operation capability and low power operation. The second version is the full multiplexer which actually includes the selector as core circuit and therefore features a higher complexity and power consumption. However, the full multiplexer is inherently more suitable for direct application in measurement setups. The performance achieved by these two multiplexer versions is addressed in the third part of the chapter. Finally, the chapter is closed by a summary, recapitulating the performance achieved by the realized circuit, thereby relating this performance to the state-of-the-art.

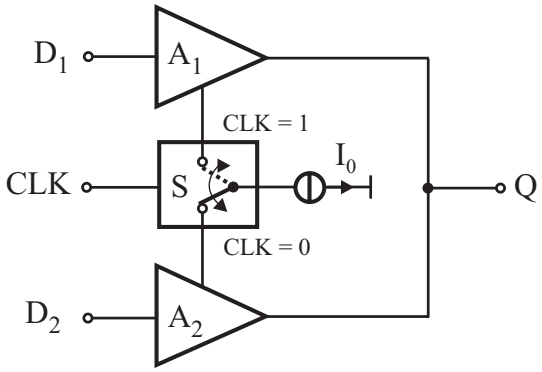


Figure 7.1: Block diagram of the applied 2:1 multiplexer concept.

7.1 Operation Principle

In general, multiplexer circuits are intended for the serialisation of the relatively low-speed (parallel) data channels at their input to one high-speed data channel at their single output. Figure 7.1 illustrates the block diagram of the applied multiplexer concept, showing the operation principle of a 2:1 multiplexer. That is, the multiplexer features two data channels at its input and one channel at the output. Thus, the multiplexer of Figure 7.1 consists of two amplifiers (A_1 and A_2) and a switch (S). The position of this switch is controlled by the logical level of the clock signal (CLK). Depending on the switch position, either the amplifier A_1 or the amplifier A_2 is fed by the current source I_0, thereby activating one or the other amplifier. The activated amplifier transfers the available data bit at its input to the output of the multiplexer.

The operation of the 2:1 multiplexer is further illustrated in Figure 7.2, showing the time diagrams of the corresponding signals. The MUX operation is based on the half-rate principle. That is, as an example, a 40 GHz clock signal is necessary for a proper operation of the MUX at 80 Gbit/s (output data). The maximal clock phase margin (ideally 180°) is achieved by delaying D_1 related to D_2 by half the bit width of the input data. That is, the clock signal can be shifted within a time interval corresponding to half the bit width of the input data without negatively affecting the data sampling. For the clock signal level at logical 1, the data bit at D_1 is transferred to the MUX output, while the data bit at D_2 is switched to the output Q as the clock signal level is at logical 0. The data bit at the MUX output features a width corresponding to half the width of the data bit at the MUX input, thereby indicating the doubled bit rate at the multiplexer output.

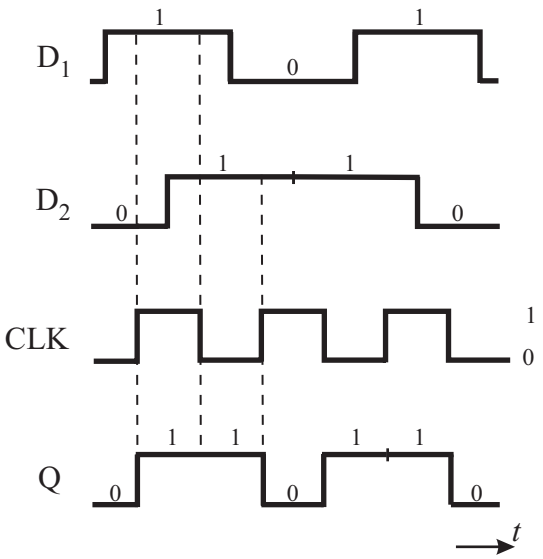


Figure 7.2: Time diagrams of the signal quantities illustrating the operation of a 2:1 multiplexer.

7.2 Circuit Design

7.2.1 2:1 Selector

The block diagram of the implemented selector circuit is shown in Figure 7.3. The core of the circuit is the selector (SEL) itself where the actual multiplexing operation occurs. The implementation of this selector on transistor level is shown in Figure 7.4. Similar to all the digital circuit design presented in the previous chapters, the design of the selector circuit underlies the differential topology, whereas the series-gating technique is applied. Furthermore, the choice of the transistor size within the selector as well as the corresponding dc operation current and the load resistance is taken from the design considerations defined in Chapter 5. The current feeding is ensured by a transistor current source, thus allowing a variation of the dc operation current during measurements. The dc voltage setting as well as the high-speed driving of the circuit stage succeeding the selector is performed by the corresponding ECL output.

The two data inputs of the selector circuit are preceded by input buffers. The composition of these buffers is illustrated in Figure 7.5. An one-stage emitter follower at the buffer input allows a broadband (50 Ω) impedance matching, thus minimizing the reflections at the data inputs of the selector circuit. The emitter-coupled differential amplifier succeeding the one-stage emitter follower acts as limiting amplifier. The latter amplifier keeps the signal to noise ratio of the incoming data sufficiently high for a proper operation within the selector. An ECL output of the limiting amplifier ensures a high-speed driving of the input data to the selector as well as the dc level setting of the data switch transistors in the selector.

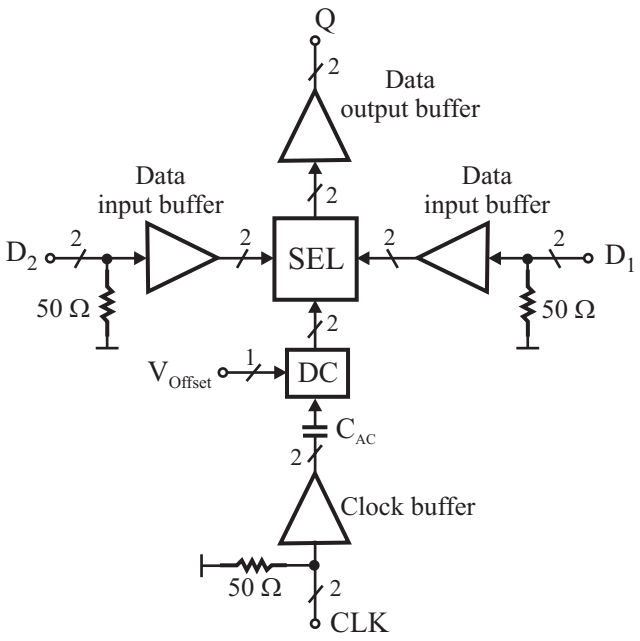


Figure 7.3: Block diagram of the implemented 2:1 selector circuit.

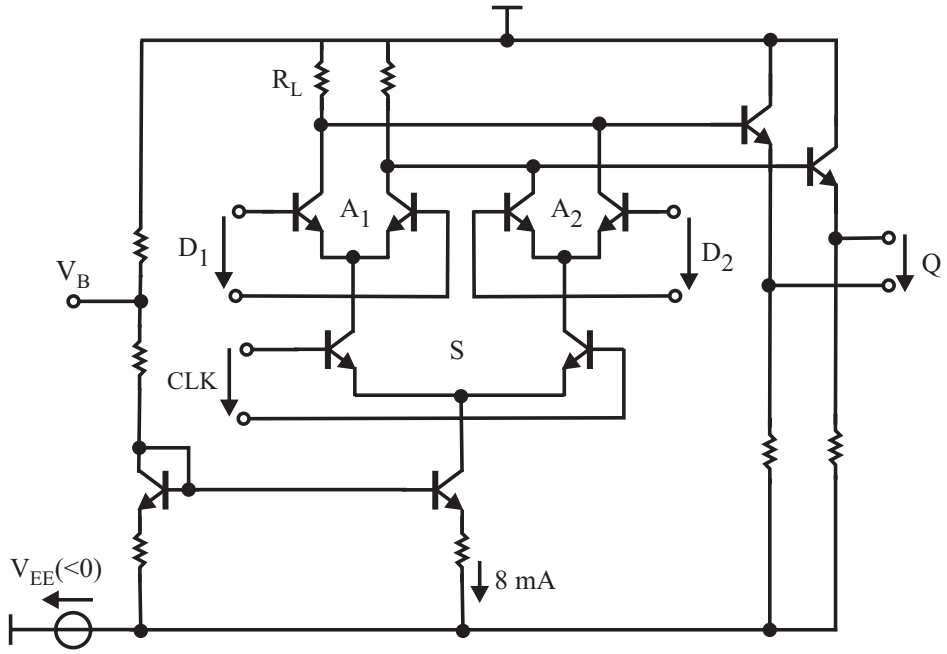


Figure 7.4: Schematic circuit diagram of the selector (SEL) peforming the multiplexing operation.

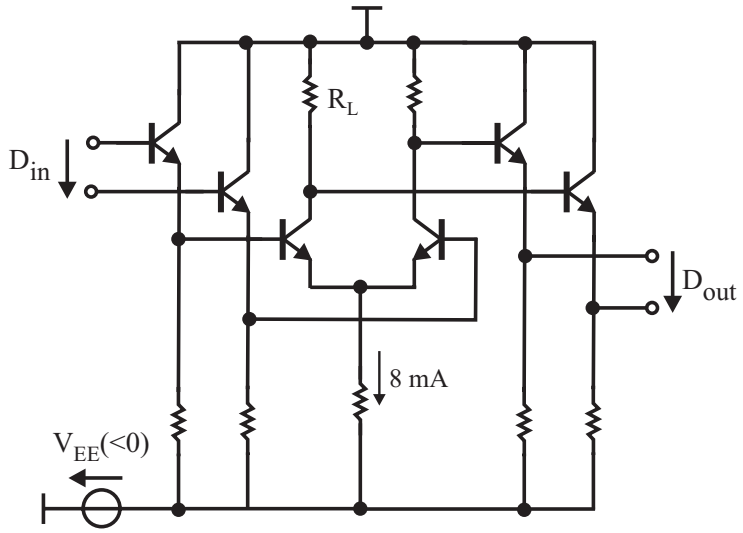


Figure 7.5: Schematic circuit diagram of the data input buffer included in the selector circuit.

The clock signal is fed to the corresponding input of the selector through a clock amplifier. The circuit configuration of this amplifier is assumed from the clock buffer amplifier used in the clock and data recovery circuit (see Figure 6.2). That is, the clock amplifier is implemented by an emitter-coupled differential amplifier using inductive peaking for bandwidth boosting. The output signal of the latter amplifier is ac-coupled to the clock input of the selector. A dc network (DC) similar to the one implemented in Figure 6.3 is used for dc operation point setting of the clock switch transistors within the selector. As for the CDR circuit, an external voltage connection is intended for clock offset correction due to possible device couple mismatch as well as asymmetry between the supposed push-pull clock signals.

The multiplexed output signal of the selector circuit is guided to an output buffer. Similar to the one used in sec. 5.2.4, the latter buffer is composed of a two-stage emitter-coupled differential amplifier, thereby acting as limiting amplifier. Thus, a proper operation of the selector is achieved without any influence of the external loading. Furthermore, the output buffer allows to smoothen the output signal of the selector circuit. That is, spikes due to the charging and the discharging of parasitic capacitances within the selector are substantially reduced.

The chip photograph of the realized 2:1 selector circuit is shown in Figure 7.6. The chip size is 1×1 mm^2. The circuit has a complexity of 30 active devices.

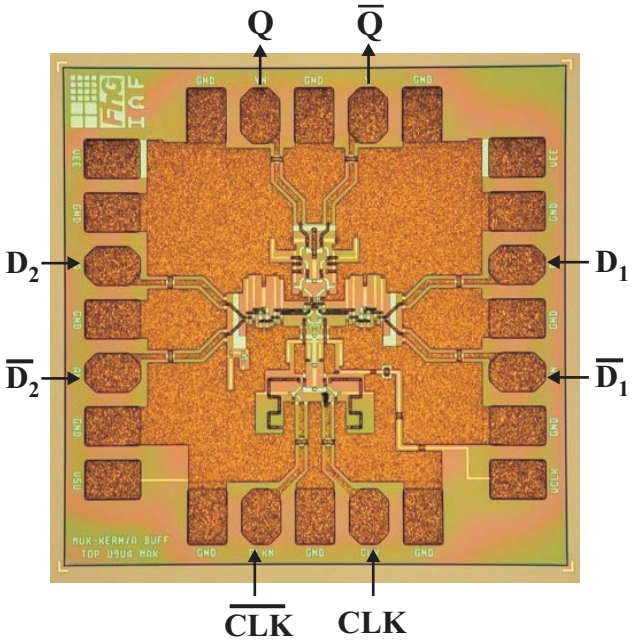


Figure 7.6: Chip photograph of the realized selector circuit. The chip features a size of 1×1 mm^2.

7.2.2 2:1 Full Multiplexer

The block diagram of the implemented 2:1 full multiplexer is shown in Figure 7.7. Similar to the selector circuit introduced before, the core of the full multiplexer is the selector where the multiplexing operations are performed. Unlike the selector circuit, the full multiplexer features data latches at the corresponding data inputs. Thus, the incoming data at D_1 are guided to the corresponding input of the selector through an input buffer followed by a serial connection of two data latches. On the other side, the incoming data at D_2 are guided to the corresponding selector input through an input buffer succeeded by a serial connection of three data latches. These data latches are intended for setting the optimum time delay between D_1 and D_2 corresponding to half the bit width of the input data. Thus, unlike the selector circuit of the previous section, an external time delay setting between D_1 and D_2 for proper operation of the full multiplexer is dispensable.

The circuit concept used for the implementation of the data latches is identical to the one applied for the latches included in the phase detector (cf. sec. 5.2.2). The input buffers preceding the data latches are composed of an one-stage emitter follower. Unlike the data inputs of the selector circuit, emitter-coupled differential amplifiers are omitted due to the presence of the data latches. In fact, the latter latches regenerate the incoming data, thus keeping the signal to noise ratio sufficiently high for a proper operation of the multiplexer core.

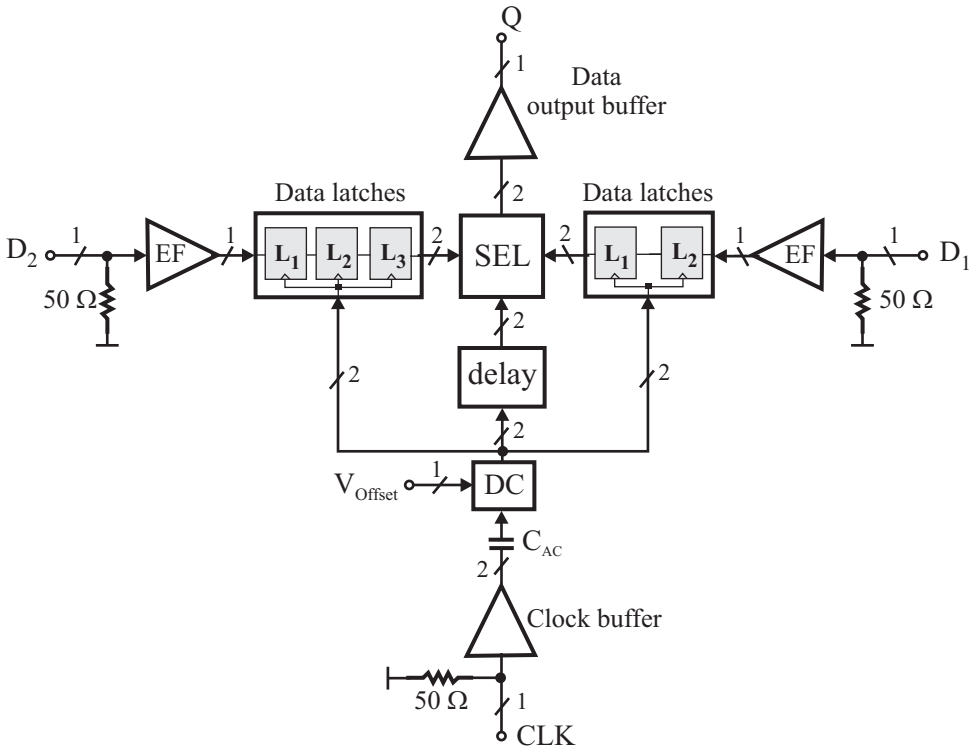


Figure 7.7: Block diagram of the implemented 2:1 full multiplexer.

The distribution of the clock signal to the corresponding input of the data latches as well as the multiplexer core is performed through a clock amplifier (or buffer). This amplifier is identical to that used for the clock input of the selector circuit. As already mentioned in sec. 5.4, the consideration of the clock distribution lines during the design phase is essential. The output signal of the clock amplifier is guided to the clock input of the selector through a delay gate. This gate allows the compensation of the additional time delay caused by the latches preceding the data inputs. Thus, erroneous data sampling in the selector is avoided. The delay gate is implemented using an ECL gate (cf. sec. 5.2.1).

The output data of the multiplexer core are guided to the output pad through an output buffer. The implementation of this buffer is identical to the buffer used in the selector circuit of the previous section.

The chip photograph of the 2:1 full multiplexer is illustrated in Figure 7.8. The chip size is 1.25×1.25 mm^2. The total circuit features a complexity of 200 active devices.

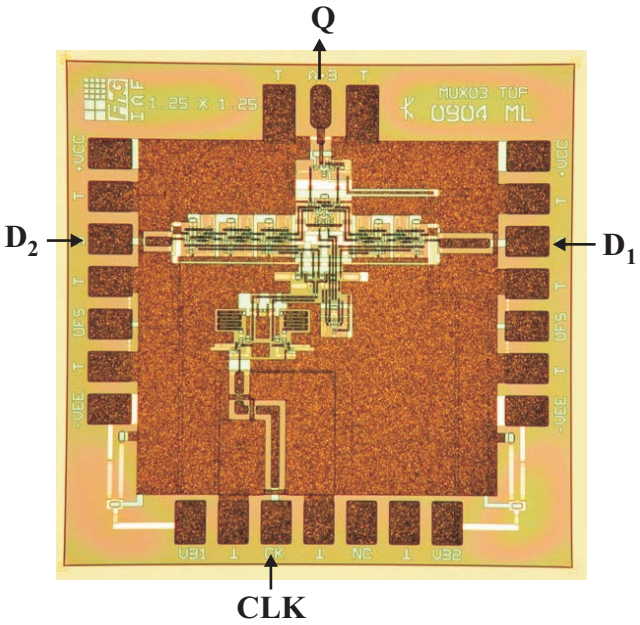


Figure 7.8: Chip photograph of the realized 2:1 full multiplexer circuit. The chip size is 1.25×1.25 mm^2.

7.3 Results

7.3.1 Measurement Setup

The testing of the realized multiplexing circuits are performed on-wafer using 65 GHz RF probes for the feeding and carrying out of the high-speed signals. The used measurement setup is illustrated in Figure 7.9. The generation of the input data is similar to the proceeding applied for the phase detector as well as the CDR characterization (cf. sec. 5.5.2 and sec. 6.2.1). Concerning the generation of the two differential data channels necessary for characterizing the 2:1 selector circuit, the differential output of the last multiplexer module (M3) is exploited. Thus, a power splitter is respectively set at the two outputs of M3, thereby allowing to create the required differential data channels. The data signals at the outputs of the power splitters (PS2, PS3) are respectively guided to the selector inputs D_1 and D_2 as well as to their complementary counterparts. In order to achieve a weak correlation between the data at D_1 and D_2 as well as between their complementary counterparts, signal lines with different lengths are used for data feeding. Figure 7.10 illustrates a photograph showing the section of the measurement setup where the two data channels are generated.

The sampling signal generated by the frequency synthesizer is carried out through a power splitter (PS1) towards the clock input of the multiplexer modules as well as that of the selector circuit under test. The clock feeding path of the latter selector circuit includes an amplifier succeeded by a power splitter (PS5). This power splitter allows to supply a differential sampling signal at the clock input of the selector circuit. The required phase

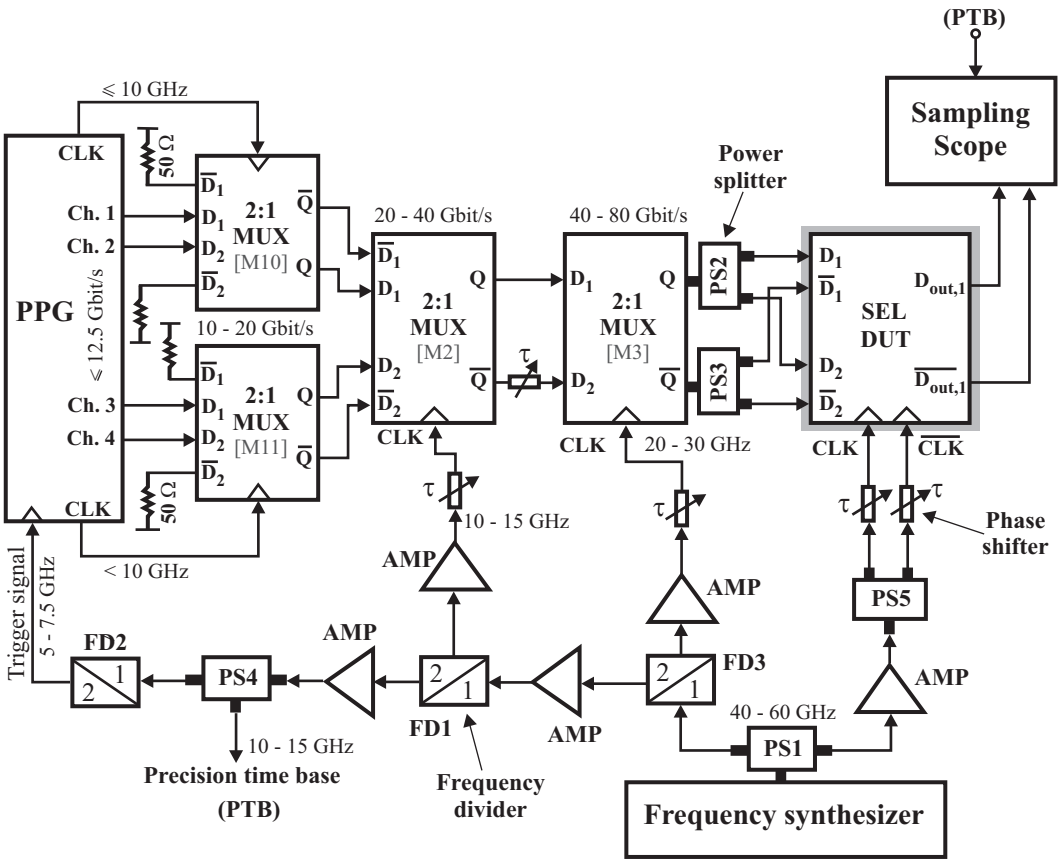


Figure 7.9: Block diagram of the measurement setup used for the characterization of the realized multiplexing circuits.

difference of 180° between the two signals arising from the power splitter is achieved using two phase shifters set at the outputs of the latter power splitter. The latter phase shifters also allow to set the optimum phase difference between input data and differential clock signal for proper multiplexing operations. The possibility of operating the selector circuit using a single-ended clock signal feeding is also investigated. That is the complementary clock input of the selector circuit is terminated by a 50 Ω resistance. Using this clock feeding configuration, the power splitter succeeding the clock signal amplifier is omitted. Considering the maximum signal frequency of 60 GHz deliverable by the frequency source, the measurement setup is able to characterize the multiplexing components up to a data rate of 120 Gbit/s. That is, input data at a rate of 60 Gbit/s have to be delivered. The latter data rate can indeed be achieved by the multiplexer module M3.

Unlike the measurement setup used for the phase detector and CDR circuit, an additional 2:1 frequency divider (FD3) is set in the clock feeding path of the multiplexer modules M2 and M3. That is, as an example, the maximum clock frequency available at the clock input of M3 amounts to 30 GHz which allows to generate the 60 Gbit/s input data for testing the selector circuit up to 120 Gbit/s. Accordingly, the maximum clock

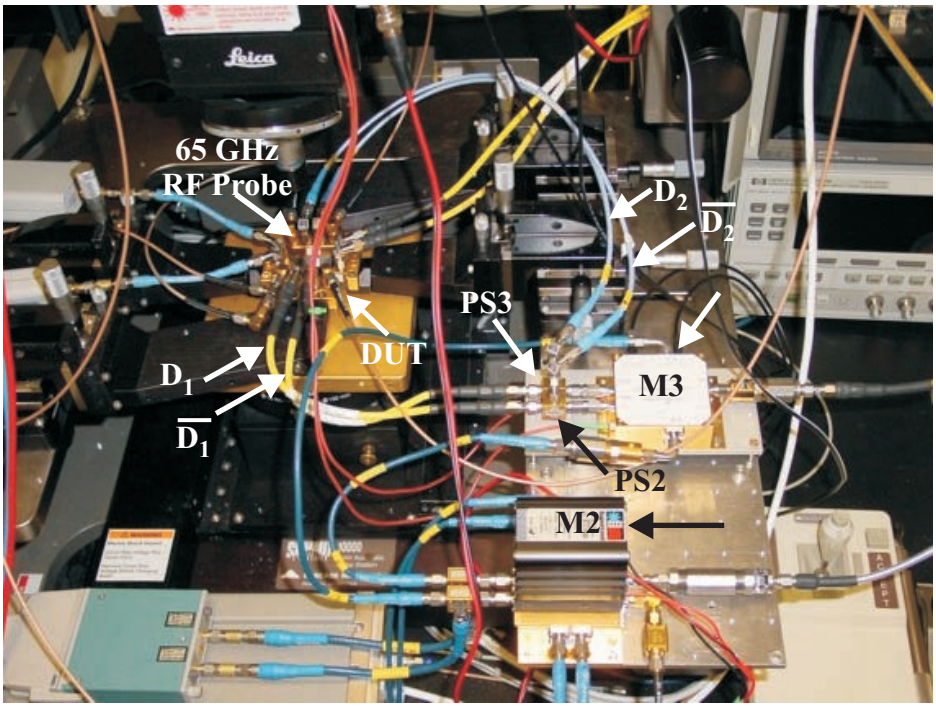


Figure 7.10: Section of the measurement setup (according to Figure 7.9) showing the generation of the two data channels needed for the characterization of the selector circuit.

frequency at the clock input of M2 is 15 GHz. Because of the aforementioned additional frequency divider, the signal frequencies serving as clock for the corresponding input of M2 match the frequency window intended for the precision time base signal of the sampling scope. Thus, the complementary output signal of the frequency divider (FD1) providing the clock signal to M2 allows to generate the precision time base signal as well as the trigger signal of the PPG through a further frequency divider FD2 (see Figure 7.9).

Concerning the characterization of the full 2:1 multiplexer, the introduced measurement setup remains valid, except for the data as well as the clock feeding of the device under test. The power dividers at the output of the multiplexer module M3 are omitted since the two data inputs of the MUX are single-ended. A phase shifter is introduced in one of the data output of M3, thus allowing to generate two uncorrelated data channels. Since the clock input is single-ended, the power divider (PS5) succeeding the clock amplifier is skipped. A section of the modified measurement setup is shown in Figure 7.11.

7.3.2 Discussion of the measured Results

Figure 7.12(a) and Figure 7.12(b) show the differential output eye diagrams of the selector circuit at data rates of 80 Gbit/s and 100 Gbit/s, respectively. A clear eye opening with an output swing of 600 mV_{pp} is observed for both data rates, thus proving the proper operation of the selector circuit. During the measurements, the external bias voltage V_{Offset} (cf. sec. 7.2.1) proves to be an essential control variable for proper operation of

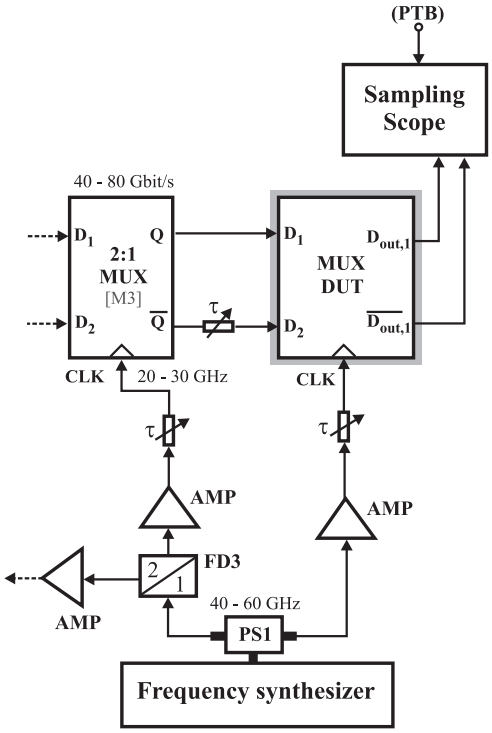
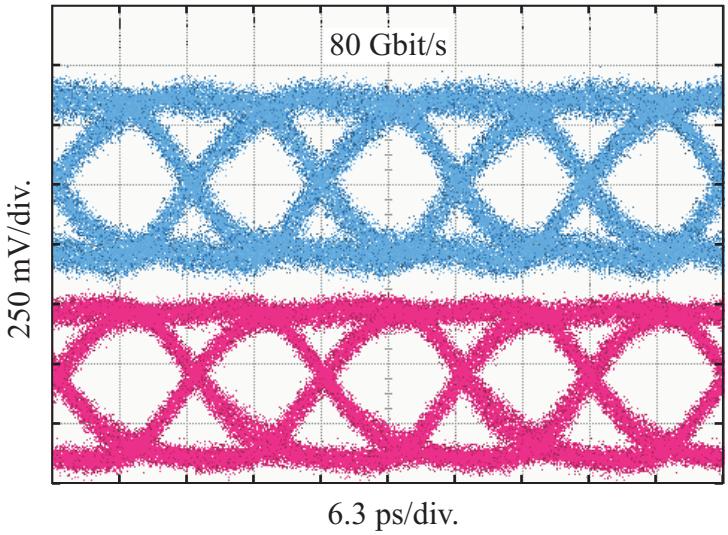


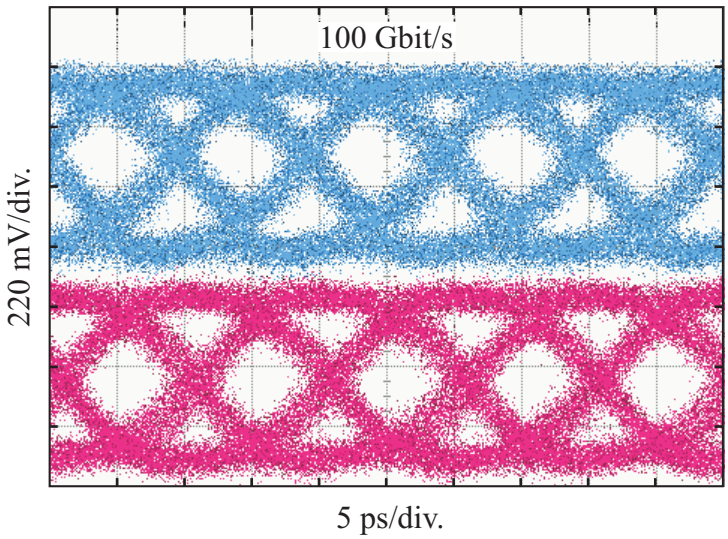
Figure 7.11: Section of the modified measurement setup with respect to Figure 7.9 for characterizing the realized full multiplexer circuit.

the selector circuit at the aforementioned high data speed. Voltage offset corrections are indeed necessary to counteract erroneous duty cycle of the sampling signal at the differential clock input of the selector (SEL). This erroneous duty cycle would otherwise result in an uncorrelated data rate at the selector output with respect to the input data rate. As a further essential control parameter, the phase shifter in the clock feeding path permits an optimum setting of the clock phase with respect to the input data, thus allowing data sampling at the best signal to noise ratio.

The measured jitter at the eye crossing of the output data amounts to 2.5 ps, considering the 80 Gbit/s output data. The latter jitter value is free from the inherent jitter of the sampling scope, the contribution of which amounts to approximately 0.8 ps. As already mentioned, the jitter from the sampling scope is eliminated using the precision time base (PTB) signal generated in the measurement setup. That is, for the selector operation at 80 Gbit/s, a 10 GHz signal is used while a 12.5 GHz signal is used for the selector operating at 100 Gbit/s. For measurements at higher data rates, the signal frequencies delivered by the measurement setup are outside of the frequency window specified for a proper elimination of the inherent sampling scope jitter. This limitation is valid for data rates between 100 Gbit/s and 140 Gbit/s. Despite this constriction, a proper operation of the selector circuit is observed at data rates up to 105 Gbit/s. This is illustrated in Figure 7.13, showing the differential output eye diagrams of the selector with an output swing of approximately 580 mV_{pp}. All these achievements are also available as only a single-



(a)



(b)

Figure 7.12: Differential output eye diagrams of the selector IC at the data rates: (a) 80 Gbit/s, (b) 100 Gbit/s. At the two data rates, the output swing amounts to approximately 600 mV_{pp}.

ended clock signal is fed at the corresponding input of the selector circuit. These results prove the positive impact of the clock amplifier which serves (in this case) as single-ended to differential signal converter. In this way, high-speed operation at single-ended clock supplying is possible. The selector IC consumes a dc current of I_{DC} = 142 mA at a single supply voltage of V_{EE} = -5 V, thus resulting in a power consumption of P_{DC} = 710 mW.

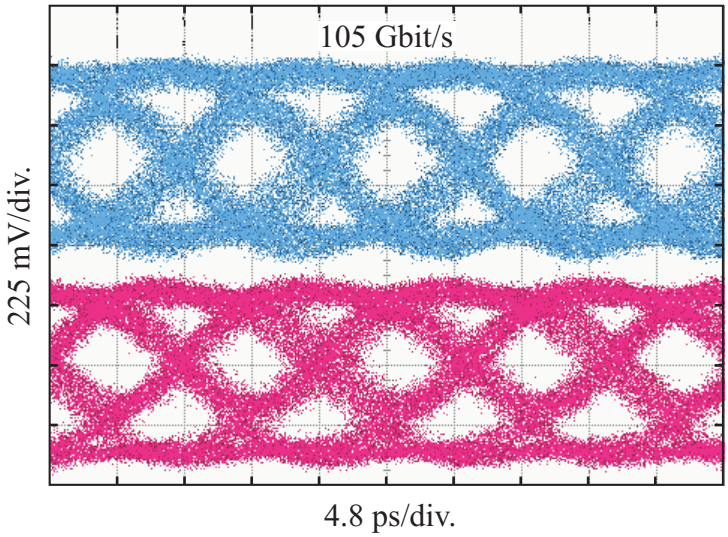
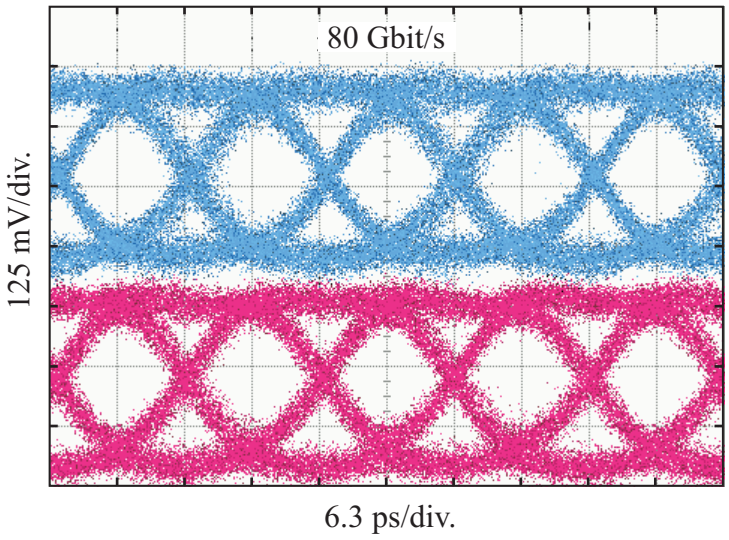


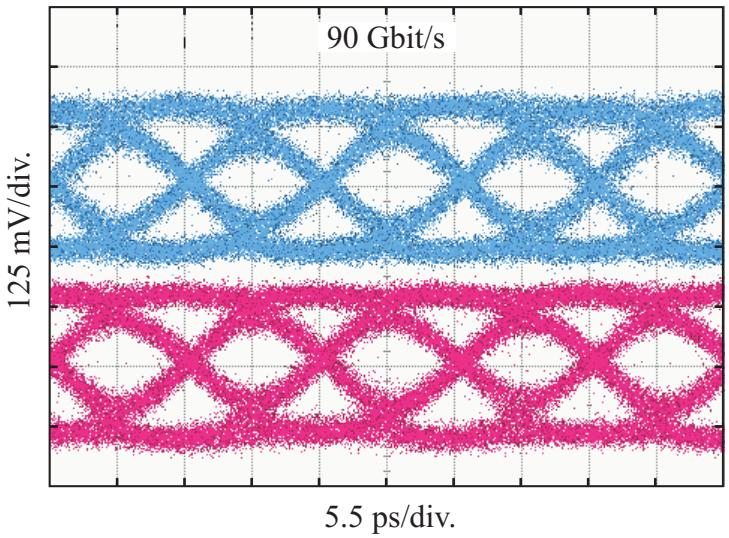
Figure 7.13: Differential output eye diagrams of the selector IC at 105 Gbit/s. The quality of the eye opening suffers from the inherent jitter of the sampling scope. The output voltage swing amounts to approximately 580 mV_{pp}.

The high-speed operation of the selector IC is even proven at low voltage supply. Thus, the selector circuit features proper operation at a single supply voltage of V_{EE} = -3.5 V. In order to keep the switch transistors within the IC out of the saturation region, the dc operation current is reduced by external bias voltage setting, thus driving the total current consumption to 110 mA. Reliable high-speed operations are achieved up to 90 Gbit/s. This is illustrated in Figure 7.14(a) and Figure 7.14(b), showing the differential output eye diagrams at 80 Gbit/s and 90 Gbit/s, respectively. At the data rate of 80 Gbit/s, an output swing of 365 mV_{pp} is obtained, while the output swing amounts to 250 mV_{pp} at 90 Gbit/s. The smaller output swings are due to the lower operation current in the output data buffer.

The 2:1 full multiplexer features reliable operations up to a data rate of 80 Gbit/s. Figure 7.15 shows the corresponding output eye diagram. Similar to the measurements performed one the selector IC, the bias voltage V_{Offset} and the clock phase shifter are crucial for the proper operation of the full MUX. The corresponding output swing amounts to 600 mV_{pp}. The chip consumes a dc power of P_{DC} = 2 W at the two supply voltages V_{CC} = 1 V and V_{EE} = -4 V. The supply voltage V_{CC} at the collector node of the one-stage emitter followers within the multiplexer was primarily intended for preventing the saturation of these emitter follower stages. However, this multiplexer also features proper operation at V_{CC} = 0 V. That is, a proper operation with a single supply voltage is available.



(a)



(b)

Figure 7.14: Differential output eye diagrams of the low supply voltage selector IC at the data rates: (a) 80 Gbit/s, (b) 90 Gbit/s. The output swing at 80 Gbit/s is 365 mV_{pp}, while the output swing at 90 Gbit/s amounts to 250 mV_{pp}.

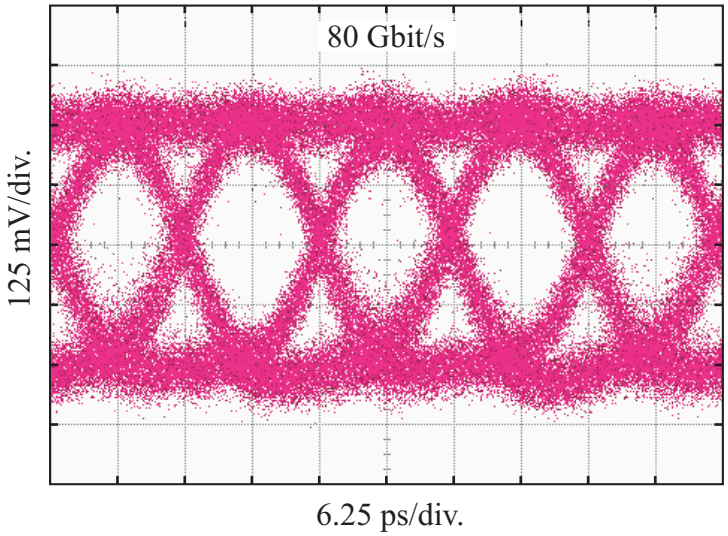


Figure 7.15: 80 Gbit/s single-ended output eye diagram of the 2:1 full multiplexer. The output swing amounts to 600 mV_{pp}.

7.4 Summary

In this chapter, two multiplexing ICs serving as high-speed data sources have been successfully designed and realized. The design technique applied for the development of these circuits is fully assumed from that discussed in sec. 5.2.1. As one of the realized multiplexing circuits, the 2:1 selector IC features very high operation speed up to 105 Gbit/s, to some extent with relatively low power consumption. The other multiplexing circuit is the 2:1 full multiplexer which features high-speed operation up to 80 Gbit/s. The latter value represents the highest data rate ever achieved for an InP-based 2:1 full multiplexer at the time of this work. Table 7.1 and Table 7.2 summarize the performance achieved by the selector and full multiplexer circuit, thereby relating them to state-of-the-art works in the same and other technologies.

Reference	[75] ('04)	[76] ('04)	**This work**	**This work [49]**
Technology	InP HEMT	InP HBT	**InP HBT**	**InP HBT**
Data rate [Gbit/s]	144	120	**105**	**90**
Output swing [mV_{pp}]	500	425	**600**	**250**
Chip size [mm^2]	1.4 × 1.5	1.0 × 1.5	**1.0 × 1.0**	**1.0 × 1.0**
P_{DC} [W]	1.23	1.71	**0.71**	**0.385**

Table 7.1: State-of-the-art and our results on 2:1 selector circuits.

Reference	[75] ('04)	[51] ('04)	[27] ('04)	**This work [49]**
Technology	InP HEMT	SiGe HBT	CMOS	**InP HBT**
Type	4:1	4:1	2:1	**2:1**
Data rate [Gbit/s]	100	132	60	**80**
Output swing [mV_{pp}]	500	250	200	**600**
Chip size [mm^2]	1.9 × 1.9	n.a.	0.63 × 0.47	**1.25 × 1.25**
P_{DC} [W]	1.65	1.71	0.01	**2**

Table 7.2: State-of-the-art works on full multiplexer circuits.

Chapter 8

Conclusion and Outlook

Conclusion

The goal of this work was the design and realization of monolithically integrated clock and data recovery (CDR) circuits with 1:2 demultiplexer using an in-house InP-DHBT technology. The thesis was part of a succesful triennial project targeting the development of an InP-DHBT technology and electronic components included in next generation 80 Gbit/s ETDM-based optical data networks. The achievements in this thesis have led to the first demonstration of an 80 Gbit/s fully integrated CDR circuit, regardless of all competing technologies.

A first development step towards the realization of the CDR circuit has consisted in the analysis and comparison of the competing CDR concepts. Based on defined selection criteria aiming highest CDR performance as well as technological feasibility, a PLL-type CDR architecture including a (digital) half-rate linear phase detector was chosen for implementation. System level considerations were used to define figures of merit, which has served as guidelines during the CDR development.

For the circuit design on transistor level, high-performance InP-DHBTs were used, the optimisation of which has been performed within the scope of a simultaneous thesis [70]. These DHBTs feature a maximum current gain β_{DC} of up to 85, a turn-on voltage of about 0.12 V, a saturation voltage under 1 V, and a breakdown voltage of > 4 V. Moreover, cut-off frequency values of more than 250 GHz for both f_T and f_{max} were achieved. This excellent device performance built the fundament for the realization of high-speed, low-power, and low-noise mixed-signal circuits.

The second development step in this work has addressed the realization of the CDR main components (VCO, phase detector, and loop filter) as stand-alone integrated circuits. Thus, differential LC VCOs were developed, which are suitable for use as frequency source for half- and full-rate data sampling at data rates beyond 80 Gbit/s. A first VCO version targeting the 43 GHz operation range has shown a tuning bandwidth of about 7 GHz. Within this tuning bandwidth, very low phase noise values down to -109 dBc/Hz were observed at 1 MHz offset frequency, while a single-ended output power up to 3 dBm was achieved.

A second VCO version aiming the 86 GHz frequency range was also successfully designed and realized. Regarding the corresponding performance, a tuning range of 6 GHz was obtained. Furthermore, very low phase noise values down to -102 dBc/Hz was observed at 1 MHz offset frequency, while a single-ended output power up to 5 dBm has been achieved. The achievements by both VCO versions are outstanding with respect to the state-of-the-art, irrespective of the transistor technologies.

As a further main component of the CDR circuit in focus, a digital half-rate linear phase detector (PD) including an 1:2 demultiplexer was successfully implemented, in a third development step. This phase detector has been monolithically integrated with the CDR loop filter, thus allowing a clear interpretation of the operation of the PD circuit. Regarding the data regeneration, the realized circuit was successfully tested at data rates up to 80 Gbit/s. Moreover, the potential for operation at data rates well beyond 80 Gbit/s has also been proven, despite the lack of the necessary data source.

Relying on the insight gained from the single development of the CDR main components, the first monolithically integrated CDR circuits operating up to 80 Gbit/s were successfully implemented, in a fourth development step. Considering the CDR circuit operating at 80 Gbit/s, proper data recovery in form of demultiplexing operation was observed. Thus, 40 Gbit/s data with clear eye opening and a voltage swing of 600 mV_{pp} were observed at the two differential outputs of the CDR circuit. Regarding the extracted 40 GHz clock signal from the 80 Gbit/s input data, a very low phase noise value of about -98 dBc/Hz was determined at 100 KHz offset. The corresponding rms jitter was measured to be as low as 0.365 ps while a peak-to-peak jitter of 1.6 ps was obtained. A tracking range of 100 MHz has been determined.

In order to accommodate the lack of data generator for characterizing the high-speed CDR at data rates beyond 80 Gbit/s, multiplexing components serving as high-speed data source were developed. Thus, a 2:1 selector, as a first version realizing the multiplexing operation, was successfully implemented. High-speed operation up to 105 Gbit/s was achieved, whereas differential output data with a respective signal swing of 600 mV_{pp} were obtained. Moreover, very low power operation has been proven at data rates up to 90 Gbit/s.

As a second version implementing the high-speed data source, a 2:1 full multiplexer was also demonstrated. Proper operation was observed up to 80 Gbit/s, whereas single-ended output data with a voltage swing of 600 mV_{pp} were obtained.

Outlook

Current research activities are focused on future Ethernet data networks targeting an operation speed of 100 Gbit/s. The InP-DHBT technology used in this work has the potential for delivering electronic components operating at this very high data rate. This has been proven, on a small scale integration level, by the realized 2:1 selector circuit, showing operation speed beyond 100 Gbit/s.

Regarding the single components building the more complex CDR circuit, the performance shown by the realized VCOs ensures proper 100 Gbit/s operation for a half-rate

CDR architecture. With respect to the implemented phase detector, a potential operation at 100 Gbit/s has been demonstrated. However, in order to guarantee proper operation at this data rate (or at 110 Gbit/s including the forward-error correction), further improvements on the phase detector circuit are necessary. This is especially true for the data and clock signal distribution within the circuit, considering possible parasitic oscillations. Two approaches for accommodating this lack are addressed in the following:

- The use of signal lines with lower characteristic impedance allows to reduce the corresponding effective inductance, thus shifting the resonant frequency of the parasitic LC resonators (in the circuit) to higher value with respect to the data rate. Low-impedance microstrip lines might be useful for this purpose, even because of the less space requirement.

- A data and clock signal distribution using an amplifier network applying the broadband mismatch principle [51] is also an effective method for avoiding parasitic oscillations at the aimed high data rate. A disadvantage of this approach might be the higher power consumption.

Finally, the realization of a monolithically integrated CDR circuit operating at 100 Gbit/s appears to be feasible with the in-house InP-DHBT technology, considering the proposals for improving the critical phase detector component.

Appendix A

Extracted Model Parameters

A.1 Large-Signal Model Parameters

The mixed-signal circuits developed in this work include DHBTs with an emitter size of 1 $\times 4$ μm^2 and 1 $\times 8$ μm^2. The proceeding used for extracting the respective large-signal model parameters is extensively described in [70]. In Table A.1, the parameters of the UCSD-model and their corresponding values, as used in the simulation environments ADS and Cadence, are listed.

A.2 Small-Signal Model Parameters

The small-signal model parameters according to the T-Topology introduced in Figure 3.13 are presented in Table A.2 with their corresponding values. Similar to the large-signal model, the proceeding for the extraction of these small-signal parameters is extensively addressed in [70]. In addition to the model parameters of the devices with a L_E of 4 μm and 8 μm, the parameters of further available devices with higher and smaller emitter length are also presented. In effect, the latter devices are considered during the elaboration of the design considerations for the developed high-speed digital circuits (cf. sec. 5.2).

L_E [μm]	4	8	L_E [μm]	4	8	L_E [μm]	4	8
$TNOM$	25	25	VJE	0.64	0.62	$VTR0$	1.38	1.18
RE	6.0	3.0	MJE	0.08	0.08	$VMX0$	162m	1.04
RCI	7.5	3.2	$CEMAX$	60f	100f	$VTCMININV$	1.42f	1.25f
RCX	10	4.9	$VPTE$	1.45	2.62	$VTRMIN$	786m	689m
RBI	12	7.1	$MJER$	0.17	0.01	$VMXMIN$	3.01	2.64
RBX	15	8.5	CJC	20.8f	31.0f	$VTCINV$	3.10μ	14.4μ
IS	3.37f	6.16f	VJC	0.5	0.5	$VTC2INV$	384m	26.4m
NF	1.20	1.18	MJC	0.6	0.6	$FEXTC$	12.7μ	999m
ISR	2.0f	2.0f	$CCMAX$	70f	100f	$TKRK$	209f	227f
NR	1.05	0.99	$VPTC$	1.0	1.0	$IKRK$	16.5m	29.0m
ISE	1.05p	1.21p	$MJCR$	0.1	0.1	$IKRKTR$	1.0μ	1.0μ
NE	1.91	1.85	$ABCX$	0.75	0.75	$VKRK$	617m	638m
ISC	1.78p	312f	TFB	38.2f	40.3f	$VKRK2INV$	1.94f	1.89f
NC	1.28	1.15	$FEXTB$	0	0	$GKRK$	1.59	1.58
ISA	830p	110p	$TFC0$	600f	248f	$VKTR$	142m	170m
NA	2.67	3.16	$TCMIN$	80.4f	72.0f	$VKMX$	525μ	2.94m
ISB	826f	36.2p	ITC	1.79m	0.92m	$FEXKE$	0	0
NB	3.46	2.27	$ITC2$	3.16m	9.03m	TR	1.0n	1.0n
CJE	13.7f	23.2f	$VTC0INV$	3.76	6.44			

Table A.1: Summary of extracted UCSD-model parameters for two different devices with an emitter length L_E of 4 and 8 μm.

L_E [μm]	2	4	6	8	10	12	16
C_{je} [fF]	12.3	29.9	45.7	62.3	81.0	98.1	136
R_{je} [Ω]	25.2	9.7	6.2	4.6	3.4	2.8	2.1
C_{jc} [fF]	2.7	3.1	3.9	4.8	6.0	7.2	10.1
R_{jc} [Ω]	∞	∞	∞	∞	∞	∞	∞
C_{ex} [fF]	8.2	10.1	12.0	13.7	15.4	16.9	20.3
R_{bb} [Ω]	91.9	48.4	36.4	30.1	25.8	23.3	19.5
α_0	0.990	0.991	0.990	0.988	0.988	0.987	0.987
τ_T [fs]	385	309	296	292	295	296	290

Table A.2: Summary of extracted small-signal model parameters. All devices have an emitter width $W_E = 1$ μm, a base width $W_B = 0.75$ μm and were biased at collector-to-emitter voltage $V_{CE} = 1.75$ and a collector current density of $J_C = 3.0$ mA/μm^2.

List of Abbreviations

ADS	Advanced Design System
AMP	Amplifier
ANSI	American National Standard Institute
BCB	Benzocyclobutene
BER	Bit Error Rate
BJT	Bipolar Junction Transistor
CDR	Clock and Data Recovery
CML	Current Mode Logic
CMOS	Complementary Metal-Oxide Semiconductor
CPW	Coplanar Waveguide
CR	Clock Recovery
DEMUX	Demultiplexer
D-FF	D-Flipflop
(D)HBT	(Double) Heterojunction Bipolar Transistor
DR	Data Recovery
DUT	Device Under Test
dc	direct current
E^2CL	Emitter-Emitter-Coupled Logic
ECL	Emitter-Coupled Logic
ETDM	Electrical Time Domain Multiplexing
FD	Frequency Divider
FEC	Forward-Error Correction
FLL	Frequency-Locked Loop
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
IT	Information and Telecommunication
ITU	International Telecommunication Union
LAN	Local Area Network
LIN-AMP	Linear Amplifier
LPF	Low-Pass Filter
MUX	Multiplexer
NR	Negative Resistance

NRZ	Non-Return to Zero
OC	Optical Carrier
PD	Phase Detector
PLL	Phase-Locked Loop
PN	Phase Noise
PPG	Pulse Pattern Generator
PS	Power Splitter
PTB	Precision Time Base
REF	Reference
RZ	Return to Zero
rms	root mean square
SAW	Surface Acoustic Wave
SCR	Space Charge Region
SDH	Synchronous Digital Hierarchy
SEL	Selector
SEM	Scanning Electron Microscopy
SNR	Signal-to-Noise Ratio
SONET	Synchronous Optical Network
SSB PN	Single Sideband Phase Noise
STM	Synchronous Transfer Mode
TAS	Transadmittance Stage
UCSD	University of California, San Diego
VCO	Voltage Controlled Oscillator

Summary of Personal Publications

[P-1] R. Driad, K. Schneider, **R. E. Makon**, M. Lang, R. Aidam, R. Quay, M. Schlechtweg, M. Mikulla, and G. Weimann, "InP DHBT-based IC technology for high-speed data communications," in *Proc. Gallium Arsenid Application Symposium*, Paris, France, Oct. 2005, pp. 137–140.

[P-2] **R. E. Makon**, R. Driad, K. Schneider, R. Aidam, R. Quay, M. Schlechtweg, and G. Weimann, "80 Gbit/s monolithically integrated clock and data recovery circuit with 1:2 DEMUX using InP-based DHBTs," in *Proc. IEEE Compound Semiconductor IC Symp.*, Palm Springs, CA, USA, Oct. 2005, pp. 268–271.

[P-3] **R. E. Makon**, R. Driad, K. Schneider, H. Maßler, R. Aidam, R. Quay, M. Schlechtweg, and G. Weimann, "Fundamental low phase noise InP-based DHBT VCO operating up to 89 GHz," *IEE Electronics Letters*, vol. 41, no. 17, pp. 961 – 962, Aug. 2005.

[P-4] **R. E. Makon**, M. Lang, R. Driad, K. Schneider, M. Ludwig, R. Aidam, R. Quay, M. Schlechtweg, and G. Weimann, "Over 80 Gbit/s 2:1 multiplexer and low power selector ICs using InP/InGaAs DHBTs," *IEE Electronics Letters*, vol. 41, no. 11, pp. 644 – 645, May 2005.

[P-5] **R. E. Makon**, K. Schneider, R. Driad, M. Lang, R. Aidam, R. Quay, and G. Weimann, "Fundamental low phase noise InP-based DHBT VCOs with high output power operating up to 75 GHz," in *Proc. IEEE Compound Semiconductor IC Symp.*, Monterey, CA, USA, Oct. 2004, pp. 159–162.

[P-6] K. Schneider, R. Driad, **R. E. Makon**, H. Massler, M. Ludwig, R. Quay, M. Schlechtweg, and G. Weimann, "Comparison of InP/InGaAs DHBT distributed amplifiers as modulator drivers for 80-Gbit/s operation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 11, pp. 3378–3387, Nov. 2005.

[P-7] K. Schneider, R. Driad, **R. E. Makon**, A. Tessmann, R. Aidam, R. Quay, M. Schlechtweg, and G. Weimann, "InP/InGaAs-DHBT distributed amplifier MMICs exceeding 80 GHz bandwidth," in *IEEE MTT-S Digest*, Long Beach,CA, USA, June 2005, pp. 1591–1593.

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