A 200 GHz Monolithic Integrated Power Amplifier in Metamorphic HEMT Technology

I. Kallfass, P. Pahl, H. Massler, A. Leuther, A. Tessmann, S. Koch, and T. Zwick

***Abstract*—A millimeter-wave monolithic integrated circuit power amplifier operating in the frequency range between 186 and 212 GHz is presented. The amplifier, dedicated to high-resolution imaging radar and communication systems, is realized in a 100 nm gate length metamorphic high electron mobility transistor technology. The three-stage design with four parallel transistors in the output stage achieves a linear gain of more than 12 dB and provides a saturated output power of more than 9 dBm and 7 dBm at 192 and 200 GHz, respectively.**

***Index Terms*—G-band, mHEMT, millimeter-wave field effect transistor (FET) integrated circuits (ICs), millimeter-wave power amplification, monolithic microwave integrated circuits (MMICs).**

I. Introduction

Amidst today's technologies covering the millimeter-wave (30–300 GHz) frequency range with its applications in remote sensing and communication, the millimeter-wave monolithic integrated circuit (MMIC) offers tremendous advantages in terms of compactness, performance competitiveness as well as ease-of-integration and deployment. The need for high power levels arises predominantly in the transmission paths of active systems, e. g. in high resolution imaging radar and high data rate wireless communication, where operating range is a direct function of the transmit power. In passive systems, heterodyne receivers require high local oscillator power levels to drive their mixers. While MMIC technology has been shown to be capable of providing low-noise amplifiers covering the entire millimeter-wave range [1], [2], relatively few works have been reported on MMIC-based power amplification beyond 100 GHz. In [3], Northrop Grumman Corp. (NGC) demonstrated a power amplifier MMIC based on 70 nm InP high electron mobility transistor (HEMT) technology. This amplifier delivers a saturated output power of 13 dBm and 10 dBm up to 190 GHz when operated under a drain supply voltage of 2 V and 1.2 V, respectively. Entering the sub-millimeter-wave region, NGC recently reported 3 dBm of output power from a three-stage amplifier at 330 GHz [4]. Based on InP double hetero-junction bipolar transistor technology (DHBT) with its high breakdown voltages, a 176 GHz amplifier with 9.1 dBm saturated output power has been realized [5]. In this letter, we report a three-stage power amplifier MMIC based on a 100 nm metamorphic HEMT technology, achieving an output power of 9 dBm and 7 dBm at 192 and 200 GHz, respectively.

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I. Kallfass, H. Massler, A. Leuther, and A. Tessmann are with the Fraunhofer Institute for Applied Solid-State Physics (IAF), Freiburg D-79108, Germany (e-mail: ingmar.kallfass@iaf.fraunhofer.de).

P. Pahl was with the Fraunhofer Institute for Applied Solid-State Physics (IAF), Freiburg D-79108, Germany and is now with the University of Karlsruhe (TH), Karlsruhe D-7613, Germany.

S. Koch is with Sony Deutschland GmbH Sensing Systems Laboratory, Stuttgart D-70327, Germany.

T. Zwick is with the University of Karlsruhe (TH), Karlsruhe D-7613, Germany.

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II. MHEMT Technology

The HEMT based on InGaAs/InAlAs hetero-structures with high In-content in the electron transport channel can be grown either pseudomorphic on InP wafers or by using a metamorphic buffer to adapt the lattice constant on GaAs substrates. Major advantages of the metamorphic approach are cost and quality of the GaAs wafers as well as ease of wafer handling. Disadvantages of the metamorphic HEMT (mHEMT) are the lower thermal conductivity of the metamorphic buffer as well as the additional growth effort. Based on the metamorphic approach, the Fraunhofer Institute for Applied Solid State Physics (IAF) develops advanced MMIC processes including HEMTs with gate lengths from 100 nm down to 30 nm. Up to an operating frequency of 200 GHz and for power applications, the 100 nm variant is the most appropriate choice. It features maximum cutoff frequencies f_{T} of 220 GHz and $f_{\max}$ of 300 GHz. On- and off-state breakdown voltages are evaluated to 3.0 V and 4.3 V, respectively [6].

The mHEMT layers are grown on 4-inch semi-insulating GaAs wafers by molecular beam epitaxy (MBE). For the metamorphic buffer a linear $\mathrm{In}_x\mathrm{Al}_{0.48}\mathrm{Ga}_{0.52-x}\mathrm{As}(\mathrm{x}=0\rightarrow 0.52)$ transition is used. For the 100 nm gate length technology the electrons are confined in an $\mathrm{In}_{0.65}\mathrm{Ga}_{0.35}\mathrm{As}/\mathrm{In}_{0.53}\mathrm{Ga}_{0.47}\mathrm{As}$ composite channel to increase the breakdown voltages. The low energy electrons with high electron mobility are confined in the $\mathrm{In}_{0.65}\mathrm{Ga}_{0.35}\mathrm{As}$ layer. Additionally, the high energy electrons are distributed over both layers, which reduces impact ionization. The split channel is confined by $\mathrm{In}_{0.52}\mathrm{Al}_{0.48}\mathrm{As}$ barriers. The upper barrier layer includes a silicon δ-doping. The layer sequence was capped with a highly doped $\mathrm{In}_{0.53}\mathrm{Ga}_{0.47}\mathrm{As}$ layer to reduce the ohmic contact and source resistance. The 100 nm T-gates are defined by a 100 kV electron beam lithography using a three-layer resist. A Pt-Ti-Pt-Au layer sequence was used for the gate metallization. The devices are passivated with a 250 nm thick CVD deposited SiN layer, which was

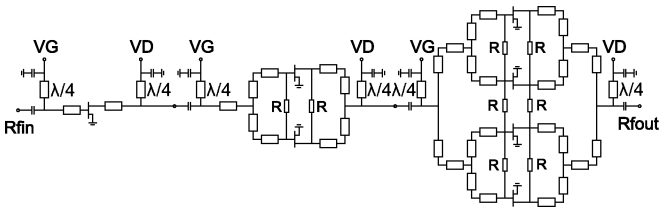

Fig. 1. Circuit schematic of the three-stage power amplifier MMIC.

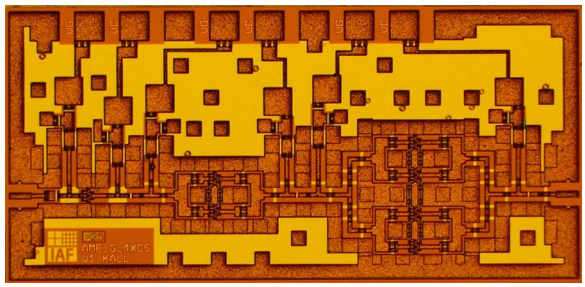

Fig. 2. Chip photograph of the power amplifier MMIC realized in IAF 100 nm metamorphic HEMT technology.

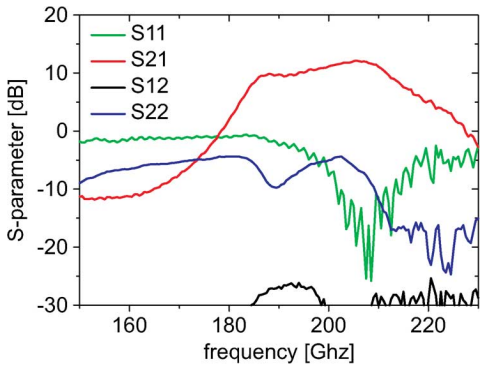

Fig. 3. G-band S-parameter measurement of the 200 GHz power amplifier MMIC.

also used as dielectric layer for the MIM capacitors. Further passive elements are NiCr thin film resistors, an electron beam evaporated Au based interconnection layer, and a 2.7 μm thick plated Au layer in airbridge technology.

For the realization of MMICs operating at frequencies beyond 60 GHz the frontside process is extended by a full backside metallization process, including wafer thinning to 50 μm substrate thickness and via hole etching for increased rejection of parasitic substrate modes in the coplanar transmission line environment.

III. Amplifier Design

The circuit schematic of the power amplifier is shown in Fig. 1. A three-stage topology is adopted, with the first, second and third stage employing one, two and four common-source transistors in parallel, respectively.

The individual transistors use four gate fingers with 10 μm width each, i.e. 4×10 μm devices. The transistor size is chosen for maximum size in order to maximize the output power, while maintaining a reasonable small-signal gain of the overall amplifier of at least 10 dB at 200 GHz. The power splitter and combiner networks in front of and after the transistors also serve as matching networks to achieve a 50 Ω interface impedance at every stage's in- and output. The matching networks are designed for maximum gain. Load-pull simulations with large-signal models indicate that further improvement in output power is possible by choosing the appropriate load impedance for maximum output power. The validation of the large-signal model is currently under way.

It is questionable whether the parallelization of transistors is a practicable way for realizing power amplifiers at high millimeter-wave frequencies. The loss incurred by the combining/splitting networks opposes the achievable gain and output power. Our simulations indicate a power loss of approximately 1.2 dB per combiner/splitter network in the frequency range from 180 to 210 GHz. The parallelization of four transistors in the output stage therefore results in a 3.6 dB increase of the output power from a single transistor. This is paid for by a reduced efficiency, since the DC power consumption scales linearly with the number of parallel transistors.

Shunt resistors at the transistor gate and drain terminals are employed for odd-mode suppression and to ensure stability in parallel amplifier branches. The gate and drain bias voltages are supplied via $\lambda/4$ lines before and after the power splitter/combiner networks.

Fig. 2 shows the chip photograph of the amplifier MMIC, implemented in a coplanar transmission line environment. Its total chip size is $1 \times 2.25\,\mathrm{mm}^2$. The gate and drain supply voltages are provided for each stage individually for ease of testing. Special care is taken in the design of the RF shunt capacitance networks to ensure low-frequency stability of the circuit. This is achieved by a deliberate reduction of the shunt capacitors' quality factor.

IV. Amplifier Performance

S-parameter measurements in G-band (140–220 GHz) show the amplifier's linear gain and power matching characteristics. Fig. 3 shows the measured reflection and transmission coefficients. A linear gain of 12.1 dB is achieved at 205 GHz. The 3-dB bandwidth is 26 GHz (186–212 GHz, corresponding to a relative bandwidth of 13 %). The bias voltages at the drain and gate are set to $V_{\mathrm{D}} = 1.4$ V and $V_{\mathrm{G}} = 0.1$ V. Under these conditions, the amplifier consumes 160 mW of DC power and all transistors operate at a current density of 409 mA/mm.

Output power is measured on-wafer with all power levels normalized to the probe tip reference plane. In order to generate enough input power to drive the amplifier into saturation, a commercial diode-based frequency-doubler module is employed. It can generate up to 5 dBm of output power at the chip input reference plane. The doubler is driven by an IAF power amplifier module delivering more than 100 mW output power up to 110 GHz. The input signal to the power amplifier is generated by a W-band source module. The measurement setup is sketched in Fig. 4.

Fig. 5 shows the measurement results of output power and gain as a function of the input power at 192 and 200 GHz. The bias conditions in the power measurement are as stated above. At 192 GHz the amplifier reaches a saturated output power of 9.5 dBm when driven with 5 dBm input power. At 200 GHz,

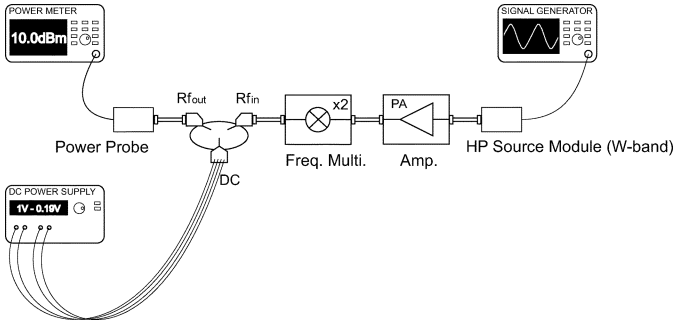

Fig. 4. Output power measurement setup for 200 to 220 GHz.

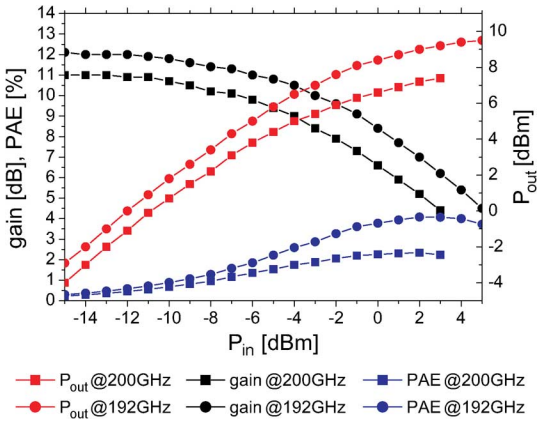

Fig. 5. Output power and gain versus input power at 192 GHz and 200 GHz.

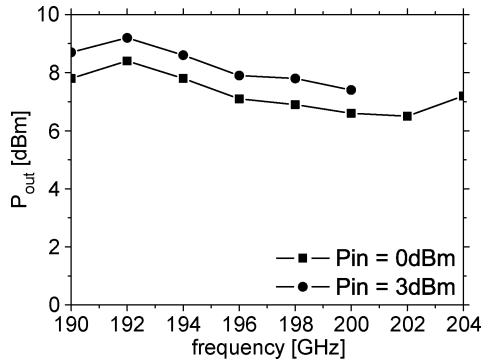

Fig. 6. Measurement of output power in a frequency sweep at constant input power levels.

the output power saturates at 7.4 dBm with a gain of 4.4 dB. The amplifier's output-related 1-dB compression point is at 5.0 dBm and 3.1 dBm for 192 and 200 GHz, respectively.

Within the measurement setup constraints, notably the bandwidth of the G-band frequency doubler, a sweep of the frequency was possible between 190 and 205 GHz. Fig. 6 shows the amplifier output power for two different input power levels. Within the considered frequency range, no significant power degradation is observed.

Table I shows a comparison of reported power amplifiers in the frequency range from 150 to 300 GHz [7], [8].

TABLE I
COMPARISON OF POWER AMPLIFIERS IN THE FREQUENCY RANGE FROM 150 TO 300 GHZ

Technology	Frequency [GHz]	BW [%]	Psat [dBm]	Gain [dB]	PAE [PAE]	Ref.
InP HEMT	260	12	>5.9	16.5	4	[7]
InP HEMT	270	-	7.8	12	5.25	[8]
InP HBT	178	-	9.1	7	3	[5]
InP HEMT	184	8	10@1.2V	20	6.5	[3]
	184		13@2V		9.5	
GaAs mHEMT	192	13	9.5	12.1	4	here
	200		7.4		2.5	

V. CONCLUSION

The 100 nm metamorphic HEMT technology, which was originally developed and optimized for high cutoff frequencies, can be adopted for the implementation of power amplifier MMICs up to G-band frequencies. Combined with low-noise amplifiers, frequency multipliers and mixers based on the same technology, fully MMIC-based high-performance analog frontends for active radar and communication systems operating in the upper millimeter-wave region become feasible.

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