First Evaluation of FPGA Reconfiguration for 3D Ultrasound Computer Tomography

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Abstract—**Three-dimensional ultrasound computer tomography is a new imaging method for early breast cancer diagnosis. It promises reproducible images of the female breast in a high quality. However, it requires a time-consuming image reconstruction, which is currently executed on one PC. Parallel processing in reconfigurable hardware could accelerate signal and image processing. This paper evaluates the applicability of the FPGA-based data acquisition (DAQ) system for computing tasks by exploiting reconfiguration features of the FPGAs. The obtained results show, that the studied DAQ system can be applied for data processing. The system had to be adapted for bidirectional data transfer and process control.**

Keywords-Altera FPGAs, Reconfigurable Computing, 3D Ultrasound Computer Tomography

I. INTRODUCTION

Breast cancer is the most common type of cancer among women in Europe and North America. Unfortunately, an early breast cancer diagnosis is still a major challenge. In today's standard screening methods, breast cancer is often initially diagnosed after metastases have already developed [1]. The presence of metastases decreases the survival probability of the patient significantly. A more sensitive imaging method could enable detection in an earlier state and thus, enhance survival probability.

At the Institute for Data Processing and Electronics (IPE) a three-dimensional ultrasound computer tomography (3D USCT) system for early breast cancer diagnosis is being developed [2]. This method promises reproducible volume images of the female breast in 3D.

Initial measurements of clinical breast phantoms with the first 3D prototype showed very promising results [3, 4] and led to a new optimized aperture setup [5], which is currently built and shown in Figure 1. It will be equipped with over 2000 ultrasound transducers, which are in particular 628 emitters and 1413 receivers. Further virtual positions of the ultrasound transducers will be created by rotational and translational movement of the complete sensor aperture.

In USCT, the interaction of unfocused ultrasonic waves with an imaged object is recorded from many different angles and afterwards computationally focused in 3D. During a measurement, the emitters sequentially send an ultrasonic wave front, which interacts with the breast tissue and is recorded by the surrounding receivers as pressure variations over time. These data sets, also called A-Scans, are sampled and stored for all possible sender-receiver-combinations, resulting in over 3.5 millions data sets and 20 GByte of raw data.

For acquisition of these A-Scans, a massively parallel, FPGA-based data acquisition (DAQ) system is utilized. After DAQ, the recorded data sets are transferred to an attached computer workstation for time-consuming image reconstruction steps. The reconstruction algorithms need a significant acceleration of factor 100 to be clinically relevant.

A promising approach to accelerate image reconstruction is parallel processing in reconfigurable hardware. This preliminary work investigates the applicability of the above mentioned DAQ system for further data processing tasks by a reconfiguration of the embedded FPGAs.

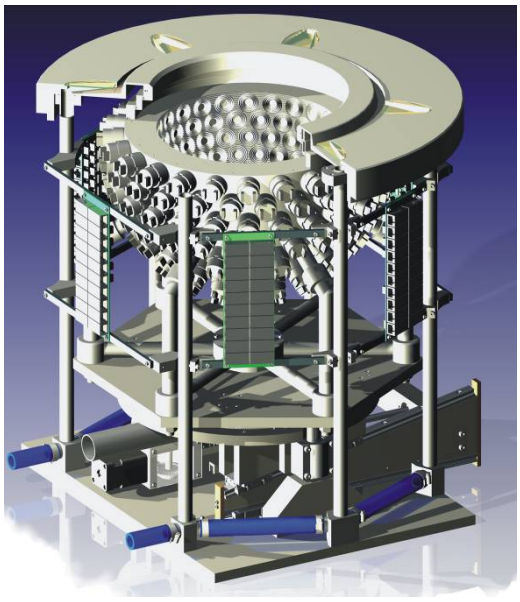

Figure 1. Technical drawing of the new semi-ellipsoidal aperture. It will be equipped with 628 ultrasound senders and 1413 receivers. During measurement, emitters sequentially send an ultrasonic wave front, which interacts with the breast and is recorded by the surrounding recievers.

The remainder of this paper is structured as follows: Section II describes the investigated FPGA-based DAQ system in detail. In Section III, the examined reconfiguration methodology is discussed. This includes derived design considerations and necessary system adaptations. Section IV illustrates an experimental procedure, which was used as proof of functionality of the used reconfiguration methodology and as a performance test of the DAQ system architecture. The paper is concluded in Section V. Therein, the attained performance results and limiting factors are discussed. Section VI gives an outlook into future work in this field of research.

II. Data Acquisition System

The investigated data acquisition (DAQ) system has been developed at IPE as a common platform for multi-project usage, e.g. in the Pierre Auger Observatory [6], the Karlsruhe Tritium Neutrino Project [7], and has also been adapted to the needs of 3D USCT. The DAQ system is described in detail in the following subsections.

A. Setup & Functionality

In the USCT configuration, the DAQ system consists of 21 expansion boards: one second level card (SLC) and 20 identical first level cards (FLC). Up to 480 receiver signals can be processed in parallel by processing 24 channels on each FLC, resulting in a receiver multiplex-factor of three. The complete system fits into one 19" crate, which is depicted in Figure 2. The SLC is positioned in the middle between 10 FLCs to the right and left, respectively.

The SLC controls the overall measurement procedure. It triggers the emission of ultrasound pulses and handles data transfers to the attached reconstruction PC. It is equipped with one Altera Cyclone II FPGA and a processor module (Intel CPU, 1 GHz, 256 MB RAM) running a Linux operating system.

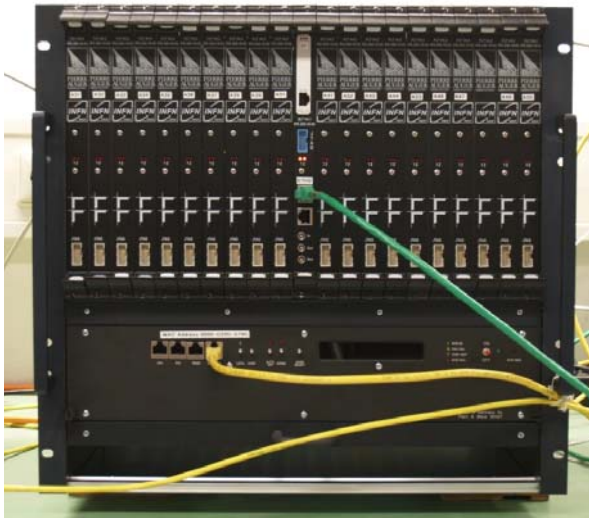

Figure 2. Image of the DAQ system in the USCT configuration. It is composed of one Second Level Card (SLC) for measurement control and communiation management (middle slot) and 20 First Level Cards (FLC) for parallel sensor signal aqcuision and data storage.

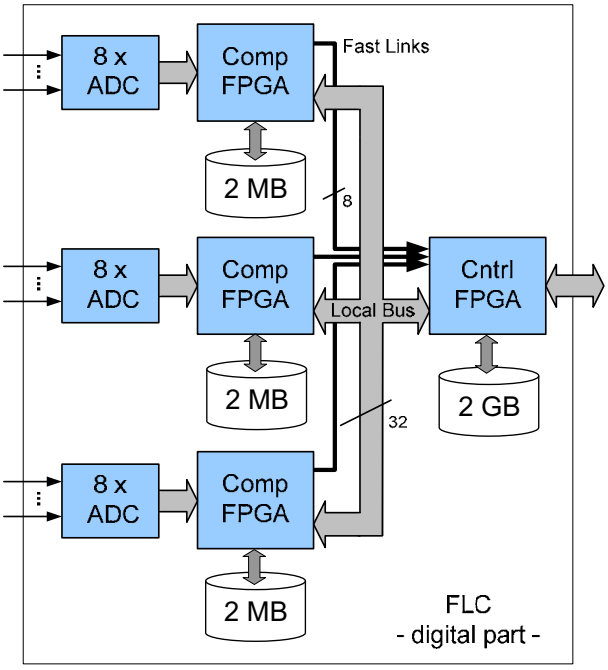

Figure 3. Block diagram of the digital part of an FLC in the 3D USCT DAQ system. It is equipped with four Altera Cyclone II FPGAs. One is used for local control (control FPGA, Cntr FPGA) and three for signal acuisition (computing FPGAs, Comp FPGA). Each Comp FPGA is fed by an 8fold ADC and is attached to a 2 MB QDR static RAM. The Cntrl FPGA is attached to an 2 GB DDRII dynamic RAM. There are two separate means of communication between the FPGAs: the slow local bus (Local Bus, 80 MB/s) and a fast data link (Fast Link, 240MB/s)

Communication with the attached PC is either possible via Fast Ethernet or an USB interface. For communication between SLC and the FLCs within the DAQ system a custom backplane bus is used.

B. First Level Card

A FLC consists of an analogue and a digital part. Only the digital part will be considered throughout this paper. A block diagram of this part is given in Figure 3. Besides three 8fold ADCs for digitization of the 24 assigned receiver channels, one FLC is equipped with four Altera Cyclone II FPGAs, which are used for different tasks:

- Control FPGA (Cntrl FPGA): One FPGA is used as local control instance. It handles communication and data transfer to the other FPGAs and to the SLC via backplane bus.
- Computing FPGA (Comp FPGA): The three other FPGAs are used for actual signal acquisition. Each of these is fed by one ADC and thus processes 8 receiver channels in parallel.

As intermediate storage for the acquired A-Scans, there are two different types of memory modules: Each computing FPGA is connected to a distinct static RAM module (QDRII, 2 MB each) and the control FPGA is attached to a dynamic RAM module (DDRII, 2 GB), summing up to a system capacity of 40 GB.

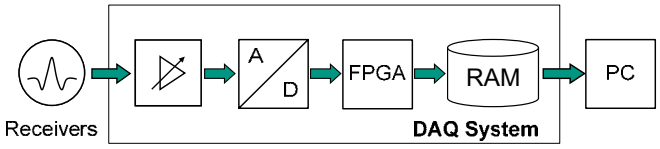

Figure 4. Data-flow of the DAQ system in the current configuration: the acquired signals from the ultrasound receivers are conditioned and afterwards digitized. They are digitally pre-filtered and decimated in the FPGAs and stored in on-board memory. After a complete measurement, they are transferred to an attached PC for further processing.

There are two separate means of communication between the control FPGA and the computing FPGAs, see also Figure 3: a slow local bus with a width of 32bit (Local Bus, 80 MB/s) and 8bit wide direct data links (Fast Links, 240MB/s per computing FPGA). Additionally, there are several connections for synchronization on board.

III. Methodology

As outlined in Section I, 3D USCT promises high-quality volumetric images of the female breast and has therefore a high potential in cancer diagnosis. However, it includes a set of time-consuming image reconstruction steps, limiting the method's general applicability.

To achieve a clinical relevance of 3D USCT, i.e. application in clinical routine, image reconstruction has to be accelerated by at least a factor of 100. A promising approach to reduce overall computation time is parallel processing of reconstruction algorithms in reconfigurable hardware.

In the current design, the DAQ system is only used for controlling the measurement procedure and acquisition of the ultrasound receiver signals. The overall data-flow of the DAQ system is shown in Figure 4. The acquired signals are conditioned and subsequently digitized, digitally pre-filtered and decimated in the FPGAs and afterwards stored in on-board memory. After a complete measurement cycle, the resulting data is transferred to an attached PC for signal processing and image reconstruction.

In this preliminary work, the utilization of the FPGAs in the DAQ system for further processing tasks has been investigated. Due to resource limitations, the full set of the processing algorithms cannot be configured statically onto the FPGAs in an efficient manner, either alone or even less in combination with the abovementioned DAQ functionality.

Therefore, a reconfiguration of the FPGAs is necessary to switch between different configurations, enabling signal acquisition and further processing on the same hardware system.

As the DAQ system has not been designed for further processing purposes, the scope of this work was to identify its capabilities as well as architectural limitations in this regard.

Only a reconfiguration of the FPGAs on the FLCs has been investigated, since these hold the huge majority of FPGAs within the complete system. Therefore, only these cards and their data-flow are considered in the following sections. Furthermore, an interaction of different FLCs has not been considered in this preliminary study.

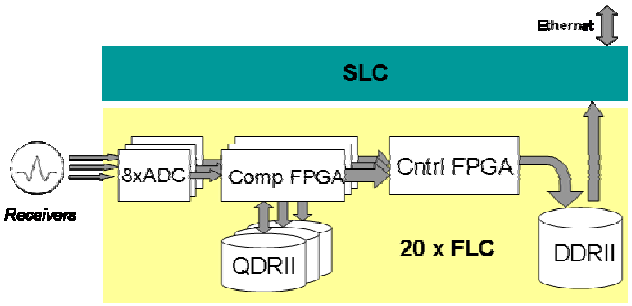

Figure 5. Detailed data-flow on one FLC during the conventional acquisition mode: Every FLC processes 24 receiver channels in parallel, whereas a group of 8 signals is digitized in a single ADC. The resulting digital signals are digitally filtered and averaged in the computing FPGAs. Finally, the signals are transmitted to the control FPGA and stored in DDRII memory.

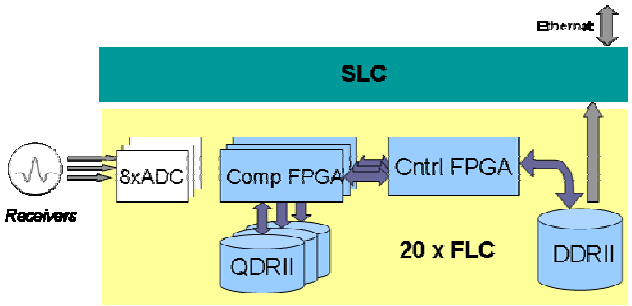

Figure 6. Detailed data-flow on one FLC during the newly craeated processing mode: As the data sets were previously stored in DDRII memory, they are transferred back to QDRII memory and processed in the computing FPGAs. Finally, the resulting data is stored again in DDRII memory.

The hardware setup of a FLC was given in Section II and shown in Figure 3. The detailed data-flow on a FLC in conventional operation mode is shown in Figure 5. During DAQ, 24 receiver channels are processed per FLC. The signals are split into groups of 8. Every group is digitized in one ADC and fed into one computing FPGA. Within a FPGA, the signals are digitally filtered and averaged by means of the attached QDR memory. Finally, the measurement data is transmitted via fast data links to the control FPGA, where it is stored in DDRII memory and afterwards transmitted to the SLC via backplane bus.

In this work, after completion of a measurement cycle, i.e. the data is stored in DDRII memory, the FPGAs were reconfigured to switch from conventional acquisition to data processing mode. As depicted in Figure 6, instead of transmitting the data sets via SLC to the attached PC, they were loaded back to QDR II and subsequently processed in the computing FPGAs. After completion, the resulting data was transmitted back to the control FPGA and again stored in DDRII memory. For providing this reconfiguration methodology, the following tasks had to be performed:

- Preventing data loss during reconfiguration
- Establishing communication and synchronization
- Implementing bidirectional communication interfaces

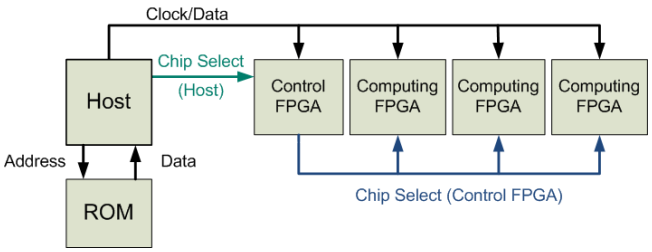

Figure 7. Passive serial configuration of a the FPGAs on a FLC at start-up time: first the control FPGA and then the computing FPGAs are configured in parall with data from an embedded configuration ROM.

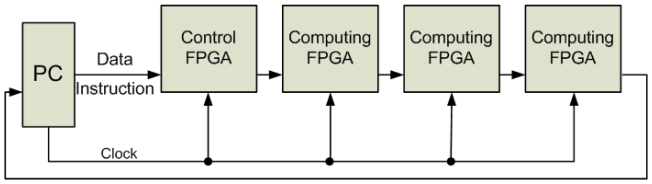

Figure 8. JTAG chain for reconfiguration of a the FPGAs on a FLC. In JTAG reconfiguration mode, each FPGA can be selected seperately for a reconfiguration, whereas deselected FPGAs remain in normal operation mode. Reconfiguration of FPGAs in chain takes place sequentially.

A. *Preventing data loss during reconfiguration*

The DAQ system is built up of Altera Cyclone II FPGAs, which do not allow partial reconfiguration [8]. Therefore, the complete FPGA chip has to be reconfigured. To prevent a loss of measurement data during the reconfiguration cycle, all data has to be stored outside the FPGAs in on-board memory, i.e. QDRII or DDRII memory.

The QDRII is static memory, so that stored data is not corrupted during reconfiguration of the FPGAs on the FLC. However, only the larger memory (DDRII) is capable of holding all the data sets recorded on one FLC. This dynamic memory module needs a periodic refresh cycle to keep stored data. On the FLC, the control FPGA is responsible for triggering these refresh cycles.

During a reconfiguration this FPGA is not able to perform this task. Since a refresh interval of the dynamic memory module is in the order of a few microseconds and a reconfiguration of the control FPGA takes even in the fastest mode about 100ms [8], it must not be reconfigured, or otherwise data in DDRII memory is lost.

Due to this requirement, only the three computing FPGAs are allowed to be reconfigured during operation. At a normal start-up of the DAQ system, all FPGAs on a FLC are configured via passive serial mode [8] with data from an embedded configuration ROM. As depicted in Figure 7, first the control FPGA and then all three computing FPGAs are configured in parallel in this mode.

In the current hardware setup it is not possible to exclude the control FPGA from a configuration in passive serial mode. Thus, each FPGA on the FLC has to be addressed and reconfigured separately, which is only possible in JTAG configuration mode [8] by using a JTAG chain through all four FPGAs as shown in Figure 8. In JTAG mode, each FPGA within the chain has to be configured sequentially.

B. *Communication and Synchronization*

Another important task in establishing the described reconfiguration methodology was to organize communication and control on the FLC as well as synchronization of parallel processing on the computing FPGAs.

As described in Section II, there are two means of communication between the computing FPGAs and the control FPGA, see also Figure 3: the slow local bus (Local Bus) and fast direct data links (Fast Links).

In conventional DAQ operation mode, measurement data is transmitted only in the direction from computing FPGAs to the control FPGA. Unfortunately, due to operational constraints in the FPGA pins, which are assigned for the fast links, this connection can only be used in the abovementioned sense, i.e. unidirectional.

Thus, in processing mode, the slower local bus has to be used for data transfer, since only this connection allows a bidirectional communication. The complete communication infrastructure is shown in Figure 9.

As the control FPGA is not reconfigured during operation, it must be statically configured to handle data transfer in each system state, i.e. DAQ as well as processing mode. Furthermore, it must be able to determine the current state in order to act appropriately. As also depicted in Figure 9, a single on-board spare connection (*conf_state*) is used for that purpose, which is connected to all four FPGAs.

In addition, each computing FPGA can be addressed and selected directly by the control FPGA via further point-to-point links to establish process control and synchronization. The respective *chip_select* signal triggers processing in a computing FPGA and by the *busy* signal completion of processing is indicated to the control FPGA.

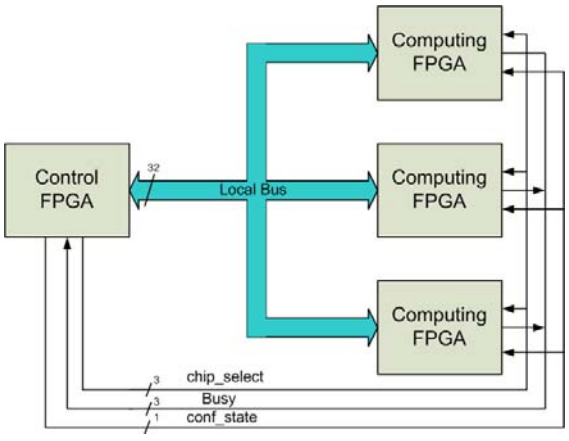

Figure 9. Communication structure during processing mode on a FLC: bidirectional data transfer is only possible via the slower Local Bus (80 MB/s). Separate point-to-point links (chip_select & busy) are used for control and synchronization of parallel processing. A further single point-to-point link is connected to all four FPGAs and indicates the current system state, i.e. DAQ or processing mode.

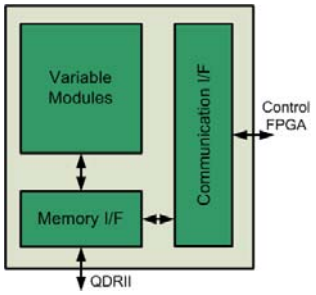

Figure 10. Block diagram of an computing FPGA: defined interfaces for communiation with the control FPGA (communication I/F) via Local Bus or Fast Links and access to QDRII memory (memory I/F). The variable algorithmic part is also indicated.

C. *Communication Interfaces*

A further task was structuring communication and memory interfaces in the computing FPGAs. As a result, modular interfaces for transmitting data over the Local Bus (communication I/F) and storing data in QDRII memory (memory I/F) were created. Figure 10 shows a block diagram of these modules on the computing FPGAs. The created modular design allows a simple exchange of algorithmic modules without the need to change further elements.

The communication interface is controlled by the control FPGA. It performs data transfers via Local Bus during processing or via fast data link during DAQ mode. The memory interface handles accesses to the QDRII memory. It can be either accessed by the control FPGA via Local Bus or by the algorithmic modules. In the current configuration, an algorithmic module only interacts with the memory interface and thus, only processes data which has already been stored in QDRII memory.

In order to guarantee a seamless data transfer over the Local Bus, the respective memory interface in the control FPGA had to be supplemented by a buffered access mode to the DDRII memory. When a data transfer is initialized, enough data words are pre-loaded into a buffer, so that the transmission is not interrupted during a refresh cycle.

IV. Experimental Results

The reconfigurable computing system was tested by acquisition of a test pulse. The used pulse was in the same frequency range as regular measurement data and was handled as a normal data set (A-Scan). This was followed by the reconfiguration of the computing FPGAs and an exemplary data processing. The main goals were to determine the required transfer time per data set over the Local Bus as well as reconfiguration times.

A. *Test setup*

For functional validation and performance measurements, a reduced setup of the complete DAQ system, containing a SLC but only one FLC was used. However, as in the current configuration only a single FLC without interactions with other FLCs has been considered, this setup allows a projection for a fully equipped system.

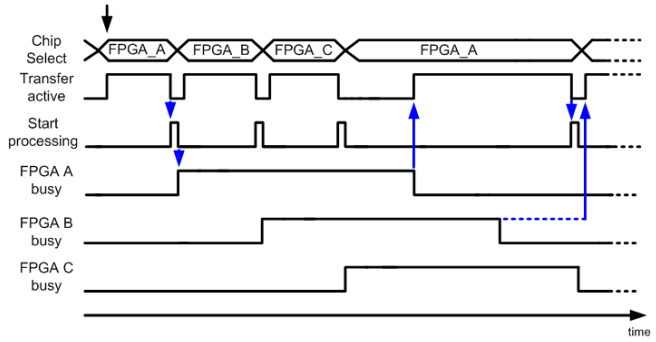

Figure 11. Detailed test procedure after DAQ and manual reconfiguration of the computing FPGAs via JTAG. Firstly, computing FPGA A is supplied with a set of A-Scans and processing on this FPGA is started. While processing is underway, also data transfer and processing on the computing FPGAs B and C is initiated. After completion of processing on FPGA A, the resulting data is tranferred back to DDRII memory and further unprocessed A-Scans are loaded. This scheme is applied repeatedly until all data sets are processed.

B. *Detailed Test Procedure*

The system has been tested as follows: At system start-up, the initial DAQ configuration was loaded into the FPGAs as outlined in Section IIa. Afterwards, the test pulse has been applied at the inputs of the ADCs on the FLC. This pulse was digitized and finally stored in DDRII memory.

The further detailed procedure is indicated in Figure 11. After a manual reconfiguration of the computing FPGAs via JTAG, the first set of A-Scans were transferred to the first computing FPGA (FPGA A) via Local Bus, stored in its attached QDRII memory and subsequently processed. While data in this FPGA is being processed, the other two computing FPGAs (FPGA B and FPGA C) are supplied with their initial data sets and processing on these FPGAs is started.

After completion of processing in FPGA A, the resulting A-Scan data was transmitted back to DDRII memory and subsequently further unprocessed A-Scans were sent to this FPGA. This scheme is repeatedly applied until all A-Scans have been processed.

C. *Results*

A JTAG configuration of a single computing FPGA requires 1.8s, resulting in a reconfiguration time of 5.4s for one FLC, when only the three computing FPGAs are configured in a JTAG chain. A reconfiguration of all 60 computing FPGAs, distributed over the 20 FLCs in the complete DAQ system would take up to 2 minutes by building up a JTAG chain through all FPGAs. The determined JTAG reconfiguration times are illustrated in Table I.

TABLE I. JTAG Reconfiguration Times

Procedure	Required time
Reconf. of one computing FPGA	1.8s
Reconf. of one FLC	5.4s
Extrapolated reconf. of the DAQ system	~2min

TABLE II. COMPUTING FPGA OCCUPATION

Components	Configuration		
	Data Acquisition	*Data Processing*	*Comm & Mem I/F only*
Logic Elements	5766 (17%)	9487 (29 %)	1231 (4%)
Embedded Multipliers	68 (97%)	64 (91%)	0 (0%)
Memory Bits	4236 (<1%)	393268 (81%)	0 (0%)

The transfer of one data set via Local Bus in either direction, i.e. from control FPGA to computing FPGA or vice versa, takes 75us. Usage of the Local Bus limited to one computing FPGA at a time and the same bus is used for data transfer to and from all three computing FPGAs.

Assuming the applied data parallel processing strategy, i.e. each computing FPGAs performs the same computation on a different data set, a high efficiency can only be reached, if the following condition holds:

The parallelized processing time per A-Scan on a computing FPGA has to be longer than 450us, which is 6 times the transmission time of a single data set. In this context, parallelized time is the processing time per A-Scan on one computing FPGA divided by the number of concurrently processed A-Scans on this FPGA. In this case, transfer time to and from all three FPGAs could be hidden. As observable in Figure 11, this requirement was not completely fulfilled by our exemplary data processing.

Table II outlines the occupation of the computing FPGA during the test procedure. The extensive use of embedded multipliers in DAQ mode, which are required due to the hard real-time constraints, state a clear demand for the established reconfiguration methodology. Furthermore, the implemented communication and memory interfaces are lightweight, occupying only 4% of the device's logic elements.

As the main result of this preliminary work, the possibility of reusing the existing DAQ system for data processing has been shown. By the reconfiguration of the FPGAs the functionality of the complete system has been increased.

V. CONCLUSIONS & DISCUSSION

In this paper, the concept of a reconfigurable computing system based on an existing DAQ system for 3D USCT has been presented.

The main drawback of the existing system is the slow data transfer over the Local Bus, which limits the achievable performance during the processing phase. This issue could partly be resolved by using a modified communication scheme, where data transfers from the computing FPGAs to the control FPGA is still done via Fast Links as in DAQ mode and the Local Bus is only used for the opposite direction.

Likewise, due to the long reconfiguration time, the number of reconfiguration cycles gives an essential contribution to the total processing time. To which extend this constraint will restrict the applicability of the presented methodology can not be assessed at this point and needs a further investigation. However, the reconfiguration time could be significantly reduced by separate JTAG chains for each FLC and concurrent reconfiguration.

VI. OUTLOOK

For future work, two obvious aspects have already been derived in the last section. Namely, reducing data transfer time by a modified communication scheme in the processing phase and reducing reconfiguration time by parallel JTAC chains.

Further tasks will also be porting processing algorithms to the DAQ system and thus, evaluating the established reconfiguration ability in real application.

What has not been considered so far is a direct communication between the computing FPGAs on a FLC and an interaction of different FLCs in general. This would open up manifold implementation strategies for algorithmic modules, besides the applied data parallel scheme.

In the long term, the next redesign of the DAQ system will put special focus on processing capabilities, e.g. high-speed data transfer.

VII. REFERENCES

[1] D. van Fournier, H.J.H.-W. Anton, G. Bastert, "Breast cancer screening", P. Bannasch (Ed.), Cancer Diagnosis: Early Detection, Springer, Berlin, 1992, pp. 78-87.

[2] H. Gemmeke and N. V. Ruiter, "3D ultrasound computer tomograph for medical imaging," Nucl. Instr. Meth., 2007

[3] N.V. Ruiter, G.F. Schwarzenberg, M. Zapf and H. Gemmeke, "Conclusions from an experimental 3D Ultrasound Computer Tomograph," *Nuclear Science Symposium*, 2008.

[4] N.V. Ruiter, G.F. Schwarzenberg, M. Zapf, A. Menshikov and H. Gemmeke, "Results of an experimental study for 3D ultrasound CT," *NAG/DAGA Int. Conf. On Acoustics*, 2009

[5] G.F. Schwarzenberg, M. Zapf and N.V. Ruiter, "Aperture optimization for 3D ultrasound computer tomography," *IEEE Ultrasonics Symposium*, 2007

[6] H. Gemmeke, et al., "First measurements with the auger fluorescence detector data acquisition system," *27th International Cosmic Ray Conference*, 2001.

[7] A. Kopmann, et al. "FPGA-based DAQ system for multi-channel detectors," *Nuclear Science Symposium Conference Record*, 2008.

[8] Altera Corporation, "Cyclone II Device Handbook", 2007