Photonic wire bonding: a novel concept for chip-scale interconnects

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Abstract: Photonic integration requires a versatile packaging technology that enables low-loss interconnects between photonic chips in three-dimensional configurations. In this paper we introduce the concept of photonic wire bonding, where polymer waveguides with three-dimensional freeform geometries are used to bridge the gap between nanophotonic circuits located on different chips. In a proof-of-principle experiment, we demonstrate the fabrication of single-mode photonic wire bonds (PWB) by direct-write two-photon lithography. First-generation prototypes allow for efficient broadband coupling with average insertion losses of only 1.6 dB in the C-band and can carry wavelength-division multiplexing signals with multi-Tbit/s data rates. Photonic wire bonding is well suited for automated mass production, and we expect the technology to enable optical multi-chip systems with enhanced performance and flexibility.

OCIS codes: (130.6622) Subsystem integration and techniques; (220.4241) Nanostructure fabrication; (200.4650) Optical interconnects.

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1. Introduction

Photonic integration has witnessed tremendous progress over the last years, and chip-scale transceiver systems with Tbit/s data rates have come into reach [1,2]. However, as on-chip integration density increases, efficient off-chip interfaces are becoming more and more challenging. In this respect, a breakthrough in optical packaging and interconnect technology is indispensable, particularly with regard to short-distance optical data transmission [3].

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Unlike electronics, where highly sophisticated metal wire bonding is the primary method of connecting integrated circuits to the outside world, photonics cannot rely on an interconnect technology of comparable versatility. Monolithic integration is often presented as a method to avoid costly chip-to-chip interfaces in photonic systems, but the associated technological complexity is still prohibitive for many applications. An industrially viable technology for chip-to-chip interconnects could enable novel system concepts that efficiently combine the strengths of different integration platforms, e.g., by complementing large-scale photonic-electronic integration on silicon-on-insulator (SOI) substrates with active optical elements on indium phosphide.

Previous research in the field of optical input/output technologies has primarily focused on refining fiber-to-chip coupling. Out-of-plane coupling has been demonstrated using diffraction gratings etched into the top surface of SOI waveguides [4–11]. When properly designed, such structures can simultaneously act as couplers and integrated polarization splitters [8]. Coupling efficiency can be improved by using bottom mirrors [10,12], silicon overlays [6] or numerically optimized grating designs [7], leading to insertion losses between 1 dB and 2 dB for advanced devices. Grating couplers enable optical access anywhere on the chip surface, but 1 dB-bandwidths are limited to typical values between 40 nm and 50 nm. To achieve broadband transmission, it is necessary to use in-plane coupling schemes that combine inverse tapers [13] with polymer, silicon dioxide (SiO_2) or silicon oxynitride (SiO_xN_y) waveguides [14–17]. With such structures, coupling losses of less than 1 dB for a single fiber-to-chip interface can be maintained over wavelength ranges of more than 100 nm [15], but spatial interconnect density is usually limited by the pitch of the connecting fibers. It was recently demonstrated that advanced multichannel spot size converters can be used to interface an array of single-mode fibers with a pitch of 250 µm to an array of SOI waveguides with a 20 µm pitch, thereby enabling a spatial data transmission density of 8 Tbit/s per millimeter of chip edge [17]. Scaling to high numbers of input/output waveguides, however, results in increasingly complex fabrication processes for the spot size converters. Moreover, all state-of-the-art off-chip interconnect techniques rely on highly precise positioning of external fibers with respect to on-chip coupling structures. Fabrication is mostly based on intricate active alignment techniques, where the coupling efficiency is dynamically monitored and optimized, and often involves manual fabrication steps. As on-chip integration density increases further, the restrictions of costly fabrication and limited interconnect density will become even more pronounced, and single-mode interconnect technologies with improved scalability and the potential for automated production will become vitally important.

In this paper, we introduce photonic wire bonding as a novel technology for single-mode chip-to-chip interconnects. In analogy to electronics, where metal wire bonds connect integrated circuits to the outside world, we use transparent polymer waveguides to bridge the gap between nanophotonic circuits located on different chips. In our approach, the shapes of the photonic wire bonds (PWB) are adapted to the actual positions of the integrated waveguide facets, so that high-precision alignment of optical devices becomes obsolete. The fabrication of three-dimensional freeform photonic wire bonds is experimentally demonstrated, and the viability of the devices is confirmed by optical characterization and high-speed data transmission at 5.25 Tbit/s. While our first-generation PWB structures introduced in 2011 had high losses [18], our latest prototypes allow for efficient broadband coupling with average insertion losses of only 2.5 dB between 1240 nm and 1580 nm, and 1.6 dB within the infrared telecommunication C-band (1530…1565 nm). Photonic wire bonding can enable co-integration of different photonic device technologies in flexible multi-chip systems, and we expect the concept to be of great importance for the industrial deployment of photonic integrated circuits.

The paper is structured as follows: In Section 2, we introduce the basic concept of photonic wire bonding and its viability for realizing photonic multi-chip systems. Section 3 presents the results of numerical investigations, where we concentrate on the taper structures

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that connect photonic wire bonds to on-chip waveguides. Sections 4 and 5 are dedicated to the fabrication and characterization of photonic wire bond prototypes. The Terabit/s data transmission experiment is described in Section 6.

2. Photonic wire bonding and multi-chip systems

Photonic integration is characterized by the coexistence of several integration platforms, each having specific strengths: Silicon-on-insulator (SOI) is well suited for dense integration of passive devices, electro-optical modulators, and germanium photodetectors together with electronic circuitry using mature CMOS processes. III-V-materials enable efficient optical sources and amplifiers. Waveguides made from silicon oxide, silicon nitride or polymers are the mainstay for high-quality optical filters and other passive components. Hence, high-performance components for basically all optical functionalities are readily available. Combining the strengths of the various integration platforms in flexible multi-chip assemblies could reduce technological complexity and increase system performance significantly.

Figure 1(a) illustrates a multi-chip system with photonic wire bonds (PWB) acting as chip-to-chip and chip-to-fiber interconnects. The wire bonds are fabricated in situ by two-photon polymerization (TPP) of negative-tone resist in the focus of a pulsed laser beam with large numerical aperture [19]. Two-photon lithography enables feature sizes below the diffraction limit of the exposure wavelength [20] and has previously been used to realize functional photonic structures such as three-dimensional (3D) photonic crystals for telecommunication wavelengths [21] or multimode optical waveguides embedded into large-area printed circuit boards [22]. We use the technique to realize free-standing single mode polymer waveguides that are directly attached to on-chip photonic circuits.

The envisaged fabrication of multi-chip systems comprises several steps. First, fibers and photonic chips are fixed to a common submount using standard pick-and-place machinery with modest precision. The interconnect regions are then embedded into a photosensitive resist, and the actual positions of waveguide facets and coupling structures within the resist are detected. This can be done in an automated process using existing 3D machine vision techniques with sub-micrometer resolution. The shape of the PWB waveguide is adapted to the recorded facet positions such that high-precision alignment of optical devices becomes obsolete. After direct-write TPP lithography, unexposed resist material is removed, and the structures are embedded in a low-index cladding material.

Photonic wire bonding allows for both out-of-plane and in-plane coupling [18,23,24], and offers a flexible way of connecting photonic chips with different waveguide technologies in an automated industrial production process. For chip-to-chip interconnects, lateral dimensions of PWB waveguides typically amount to 1…2 µm, and the interconnect pitch can be smaller than 5 µm. It is hence possible to accommodate hundreds of interconnects per millimeter of chip edge, or tens of thousands PWB links per square millimeter of chip surface.

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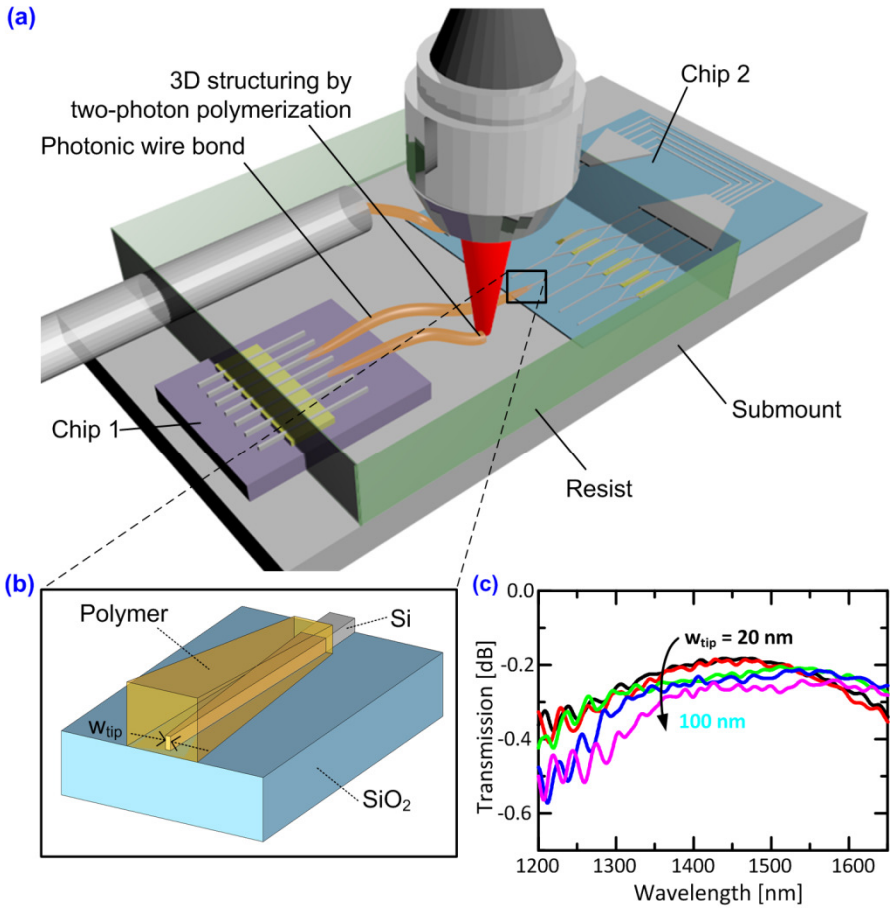

Fig. 1. (a) Artist impression of a photonic multi-chip system based on photonic wire bonding: Photonic chips (Chip 1, Chip 2) and optical fibers are mounted on a common submount and embedded into a photosensitive resist. Two-photon polymerization in the focus of a pulsed laser beam is then used to define three-dimensional freeform photonic wire bond (PWB) structures in the volume of the resist. **(b)** Inverse-taper transition between an SOI nanowire waveguide and a polymer PWB interconnect. The SOI waveguide is typically 500 nm wide and 220 nm high, and it is tapered down over a length of 32 µm to a tip width w_{tip} between 20 nm and 100 nm. **(c)** Simulated transition loss spectrum for different tip widths.

3. Modeling and design

Broadband coupling between integrated waveguides and PWB interconnects is essential for maximum data transmission capacity. To this end, we use SOI waveguides which are inversely tapered in the lateral direction, and combine them with 3D tapers in the polymer, Fig. 1(b).

Simulations of the transition between the integrated SOI waveguide and the PWB section were performed using a commercially available fully vectorial time-domain solver (CST Microwave Studio). In our model, the SOI waveguide consists of a 500 nm wide and 220 nm high silicon strip (refractive index n_{Si} = 3.48 at 1550 nm) deposited on a silicon dioxide buffer layer (n_{SiO2} = 1.44 at 1550 nm). The PWB waveguide core is made of a polymer material (SU-8, n_{SU8} = 1.57 at 1550 nm) and features a rectangular cross section with 1.4 µm width and 1 µm height to enable single-mode propagation. In the transition region, the SOI waveguide width is tapered down to a tip width w_{tip} between 20 nm and 100 nm over a length of 32 µm. The inverse SOI taper is enclosed by the 3D polymer taper of the PWB with an initial height

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of 450 nm, an initial width of 760 nm, and a length of 20 µm. The PWB waveguide core is immersed into a low-index cladding (e.g., Cytop, n_{Cy} = 1.34 at 1550 nm), which is not depicted in Fig. 1 for the sake of clarity.

The investigated structures exhibit very good transmission properties. The coupling efficiency increases if the tip width w_{tip} of the silicon taper is decreased, but even for relatively large widths of w_{tip} = 100 nm, broadband transmission with less than 0.5 dB loss is predicted by simulations, see Fig. 1(c). In our design, the geometrical parameters were obtained from a few systematic trials, taking into account the limitations of the underlying fabrication processes. The structures do not represent the overall optimum and further improvement of the coupling efficiency is possible by systematic numerical optimization. Absorption losses in the polymer waveguide of the PWB can usually be neglected: Bulk material absorption loss for prevalent TPP photoresists ranges from 0.5 dB/cm to 3 dB/cm, whereas PWB lengths are typically less than 0.1 cm.

4. Sample fabrication

For a proof-of-principle experiment, we fabricated PWB interconnects between two SOI waveguides on the same chip, Fig. 2(a), and between waveguides on different chips, Fig. 2(b). The SOI waveguides were produced on a 200 mm-wafer CMOS line using 193 nm deep-ultraviolet (DUV) lithography and chlorine-based reactive ion etching [25]. The standard waveguide width is 500 nm, the waveguide height amounts to 220 nm, and the buried oxide is 2 µm thick. We realized different inverse SOI tapers with lengths ranging from 20 µm to 100 µm, and tip widths between 80 nm and 100 nm. The PWB structures were written in MicroChem SU-8 2075 photoresist (refractive index n = 1.57 at 1550 nm) using a commercially available 3D laser lithography system based on an inverted microscope (Photonic Professional, Nanoscribe GmbH [26]). The system uses a frequency-doubled fiber laser emitting pulses at 780 nm wavelength with approximately 100 MHz repetition frequency and 150 fs pulse width. To attach the wire bond to the SOI waveguides, the lateral positions of the inverse tapers were visually determined from the wide-field image taken by the microscope camera through the lithography objective. The vertical position was adjusted manually by optimizing the focus of the image. Achievable alignment tolerances of the photonic wire bond with respect to the SOI waveguides are estimated to be better than 500 nm in all directions. We expect that a more precise alignment using machine vision techniques will improve the repeatability of the fabrication process, and further reduce the insertion losses. After development of the exposed resist, the structure was immersed in an index-matching liquid (Cargille Laser Liquid, code 3421, n = 1.30 at 1550 nm) to emulate a low-index cladding material. Some residual index matching liquid is visible in Fig. 2(b).

The chip-to-chip bond depicted in Fig. 2(b) bridges a distance of approximately 100 µm between the two SOI waveguide tips. It compensates a lateral displacement of the waveguide axes of approximately 25 µm in the horizontal and 12 µm in the vertical direction. Fourth-order polynomials are used to define the 3D PWB trajectory connecting the two SOI waveguide tips for ensuring kink-free transitions between the SOI waveguides and the PWB. The PWB apex reaches a height of 18 µm above the top surface of the upper chip (Chip 2).

The PWB prototypes exhibit excellent mechanical and chemical stability: The samples are stored in a laboratory environment, and no special measures are taken to protect the waveguide against influences such as oxygen or humidity. Repeated testing of the waveguides over several weeks with optical powers of up to 100 mW did not reveal any degradation of the transmission loss. The mechanical stability of the structures is excellent – free-standing waveguide arches with less than 2 µm diameter can easily span distances of more than 100 µm and are not affected by manual handling of the chip with tweezers or by intensive rinsing in water after the development step. Moreover, the fabricated wire bonds exhibit strong adhesion to the silicon chip surface and do not detach even when treated with oxygen plasma or when immersed in acetone.

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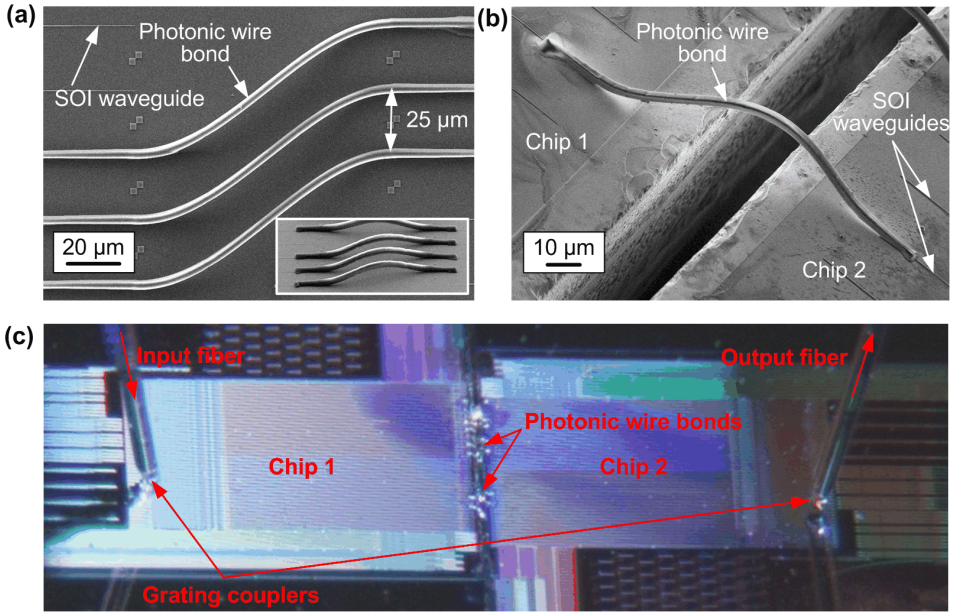

Fig. 2. Fabricated photonic wire bonds (PWB) and optical characterization setup. **(a)** PWB prototype connecting two SOI waveguides on the same chip. The PWB waveguide core consists of SU-8 and features a rectangle-like cross section of approximately 2 µm width and 1.6 µm height. **(b)** PWB chip-to-chip interconnect: The SOI waveguides are displaced with respect to each other by approximately 25 µm in the horizontal and by approximately 12 µm in the vertical direction. The PWB apex reaches a height of 18 µm above the top surface of the upper chip (Chip 2). Index matching liquid was used to emulate a low-index cladding material, residues of which are still visible on the surface of the chip. **(c)** Optical characterization setup of a PWB assembly linking two SOI chips (Chip 1, Chip 2). Light is coupled to the SOI waveguides using standard single-mode fibers ('Input fiber', 'Output fiber') and conventional grating couplers.

5. Optical characterization

The expected low-loss broadband transmission capabilities of photonic wire bonds were experimentally confirmed. For optical characterization, light is coupled to the integrated SOI waveguides using standard single-mode fibers and conventional grating couplers, Fig. 2(c). Figure 3 shows the results obtained from a photonic wire bond linking two SOI waveguides on the same chip, see SEM picture in Fig. 2(a).

In this device, the inverse SOI tapers were 60 µm long, and they were embedded in a 100 µm long SU8-taper. To obtain the net insertion loss of the photonic wire bond, we first measured the transmission through the entire assembly consisting of two grating couplers, two SOI waveguide sections and the PWB itself; see green trace in Fig. 3. The transmission spectrum is then normalized to that of a reference structure comprising only two grating couplers and an SOI waveguide, see black trace in Fig. 3. The net insertion loss of the photonic wire bond is represented by the red trace in Fig. 3. Within the C-band (1530…1565 nm), we obtain an essentially wavelength-independent total insertion loss of 1.6 dB with wavelength-dependent root-mean square (RMS) variations of ± 0.13 dB. These figures comprise both the propagation loss in the PWB section and the coupling losses of both interfaces to the SOI waveguides. For the entire wavelength range between 1240 nm and 1580 nm, the measured average insertion loss amounts to 2.5 dB with spectral variations of ± 1.1 dB. Extrapolating the transmission spectrum to wavelengths beyond 1580 nm, we estimate the 1 dB bandwidth to be larger than 300 nm.

We note that the strong variations of the measured loss spectrum below 1480 nm are not caused by the PWB itself, but by the connected SOI structures: The SOI grating couplers are

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optimized for an operating wavelength of 1550 nm with a 1 dB bandwidth of approximately 38 nm. For wavelengths outside that range, only residual scattered light is coupled between the fibers and the SOI waveguides, and the measurement data is subject to large uncertainties. In addition, a systematic inaccuracy of the measured insertion loss arises from the fact that the efficiency of the grating couplers can vary from one measurement to another. To quantify these errors, we have performed repeated transmission measurements of three nominally identical SOI reference waveguides. One device showed increased insertion loss compared to the other devices and was discarded from the analysis to avoid an underestimation of the PWB loss by using a bad on-chip waveguide as a reference. For the measurements performed with the two remaining devices, we estimate RMS variations of 0.38 dB within the C-band and 0.52 dB for the entire wavelength range. To estimate the error bounds for the PWB transmission loss, we take the square root of the sum of the squares (RSS) of the wavelength-dependent RMS variations and the RMS uncertainty of the reference waveguide measurement. We obtain error bounds of approximately ± 0.4 dB for the C-band and ± 1.2 dB for the entire wavelength range.

The results show that photonic wire bonds outperform high-efficiency fiber-chip grating couplers [6] and can well compete with planar coupling schemes fabricated by advanced electron beam lithography [15]. Results similar to those reported above have been obtained for three more PWB prototypes realized on the same chip and showing C-band losses of 2.0 dB, 2.1 dB and 2.8 dB. The variations are due to different lengths of the inverse silicon taper sections and alignment inaccuracies of the PWB structures with respect to the on-chip feed waveguides.

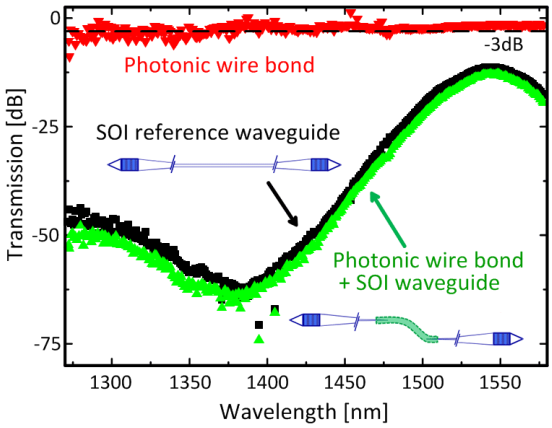

Fig. 3. Transmission measurement of a photonic wire bond (PWB) prototype: The lower curve ('Photonic Wire Bond + SOI waveguide', green) represents the transmission through the entire PWB assembly consisting of two grating couplers, two SOI waveguide sections and the PWB interconnect, see Fig. 2(c). To obtain the net insertion loss of the PWB (red), the measured transmission spectrum (green) was normalized to that of an SOI reference structure comprising only two grating couplers and an SOI waveguide (black). For comparison, we plotted a dashed reference line at an insertion loss of 3 dB. Within the measured wavelength range, the net loss of the PWB amounts to (2.5 ± 1.2) dB. Within the C-band (1530…1565 nm), we find an even lower loss of (1.6 ± 0.4) dB. Extrapolating the transmission spectrum to wavelengths beyond 1580 nm, we estimate that the 1 dB bandwidth is larger than 300 nm. Results similar to those depicted here were reproduced with different samples

6. Tbit/s data transmission

Photonic wire bonds can handle multi-Terabit/s data streams comprising dozens of wavelength channels, even if phase-sensitive advanced modulation formats are used. We experimentally confirm the absence of transmission impairments through reflection, polarization mode dispersion, or nonlinearities. For the experimental verification we use a

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transmitter setup similar to the one described in [27] and generate a wavelength-division multiplexing (WDM) data stream with an aggregate rate of 5.25 Tbit/s. The data stream covers the wavelength range between 1543.42 nm and 1555.74 nm and consists of 105 carriers, each of which is modulated with a 16 QAM signal at a symbol rate of 12.5 GBd.

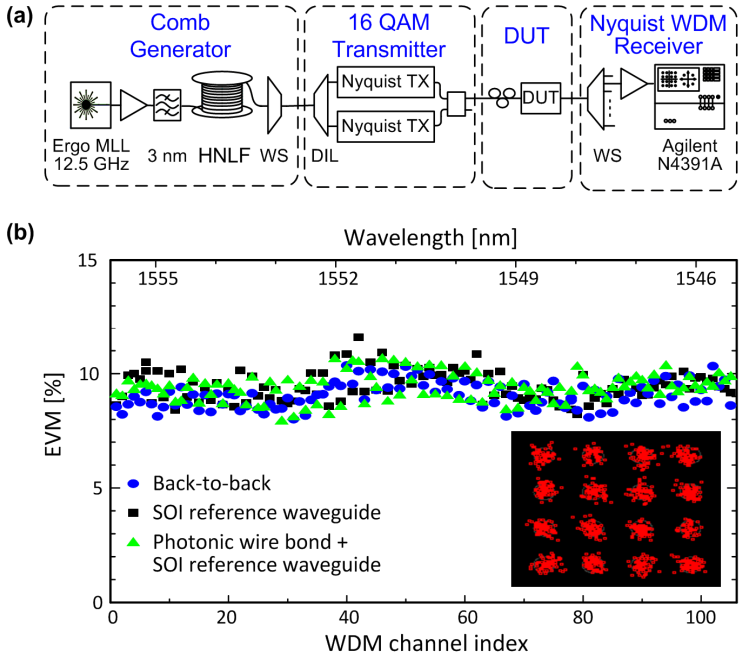

Fig. 4. Experimental testing of a photonic wire bond (PWB) prototype: (a) Data transmission setup: A number of 105 optical carriers are generated by a mode locked laser (MLL) and a highly nonlinear fiber (HNLF). After spectral shaping of the comb spectrum in a programmable optical filter (Finisar WaveShaper, WS), odd and even carriers are separated in an optical disinterleaver (DIL). The carriers are subsequently encoded with 16QAM signals at a symbol rate of 12.5 GBd. Odd and even carriers are recombined and the compound signal is transmitted through the device under test (DUT). At the receiver side, individual WDM channels are isolated in a second WaveShaper, and an optical modulation analyzer (Agilent N4391A) is used to measure the signal quality. (b) The error-vector magnitude (EVM) was measured for the back-to-back case, for the transmission through the SOI reference waveguide, and for the transmission through the photonic wire bond assembly, which consisted of two SOI waveguides on a single chip, linked by a photonic wire bond, see Fig. 2(a). The EVM for all carriers is below the threshold for second generation forward-error correction, and no EVM penalty could be observed for the transmission through the wire bond. Inset: Typical 16 QAM constellation diagram of a single channel, measured at the carrier closest to 1550 nm.

The transmitter setup is depicted in Fig. 4(a). The optical carriers are derived from a single mode-locked laser (MLL, Ergo-XG, Time-Bandwidth Products) operating at a repetition frequency of 12.5 GHz. The output spectrum of the MLL was broadened in a highly nonlinear fiber (HNLF), and a programmable optical filter (Finisar WaveShaper, WS) was used to extract a comb spectrum with uniform power distribution. Carriers belonging to even and odd channels are separated in an optical disinterleaver (DIL) and subsequently encoded with a 16-state quadrature-amplitude modulation (QAM) format. Bandwidth-limited sinc-shaped Nyquist pulses are used to enable densely packed WDM channels. The signal is then coupled to the device under test (DUT). For the transmission through the PWB assembly or the SOI reference waveguide, an erbium-doped fiber amplifier (EDFA) compensates for the fiber-to-chip coupling losses. The power in the input fiber before the device under test amounts to 13 dBm. At the receiver side, individual WDM channels are isolated in a second programmable filter (WaveShaper, WS). The signal is then demodulated and characterized by an optical

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modulation analyzer (Agilent N4391A) with a tunable laser serving as local oscillator. An optical attenuator is used to keep the input power into the second WaveShaper at a constant value of 0 dBm. A typical 16QAM constellation diagram of the received signal is depicted in the inset of Fig. 4. As a quantitative measure of the signal quality, we use the error vector magnitude (EVM), which describes the effective distance of a received complex symbol from its ideal position in the constellation diagram. The EVM can be interpreted as an extension of the Q-factor method to the case of higher-order modulation formats and is directly connected to the bit-error ratio (BER) if the signal is impaired by additive white Gaussian noise only [28,29].

Figure 4(b) depicts the results for back-to-back transmission (blue), transmission through the SOI reference waveguide (black), and transmission through the PWB assembly (green). For the back-to-back case, we found an average EVM of 9.1%, which corresponds to a BER of approximately 0.9×10^{-4}. For the transmission through the SOI reference waveguide, the average EVM is only slightly increased to 9.5% (BER = 1.6×10^{-4}), and the transmission through the PWB yields essentially the same value (EVM = 9.4%, BER = 1.4×10^{-4}). The PWB does hence not introduce any EVM penalty, and the BER for all carriers is below the threshold of 2.3×10^{-3} (1.9×10^{-2}) for state-of-the-art (advanced) forward-error correction [28,30]. The low insertion loss of the PWB keeps the launched on-chip signal power low and hence prevents signal impairments from nonlinearities in the nanophotonic SOI waveguides. To the best of our knowledge, the demonstrated 5.25 Tbit/s is the highest data rate that was ever transmitted through an SOI nanowire. The data rate was only limited by the available transceiver equipment, not by the PWB or the SOI waveguide. Assuming a 5 µm pitch between neighboring PWB waveguides, our concept enables unprecedented interconnect densities of at least 1 Pbit/s/mm along the chip edge (200 Pbit/s/mm^2 on the chip surface). This is more than two orders of magnitude larger than recently reported values [17].

7. Future work

While this work demonstrates the basic viability of photonic wire bonding for chip-to-chip connections, further research is necessary to turn the concept into a widely applicable interconnect technology. One of the key aspects is the reproducibility of the fabrication process, where a highly precise positioning of photonic wire bonds with respect to the on-chip waveguides is crucial. Moreover, long-term stability of the PWB structures is essential, and further investigations are needed to systematically assess different resist materials that can be structured by two-photon polymerization. In addition, PWB interfaces between on-chip waveguides and single-mode fibers are of great importance: For free-standing photonic wire bonds, the reach is currently limited to typical values below 1 mm. Connecting optical chips over distances of several centimeters will therefore still rely on optical fibers and require advanced fiber-chip coupling schemes.

8. Summary

We have introduced photonic wire bonding as a novel concept to connect nanophotonic systems integrated on different chips. Direct-write two-photon lithography is deployed to fabricate 3D freeform photonic wire bonds that connect standard SOI waveguides. Our structures realize highly efficient coupling with insertion losses of 2.5 ± 1.2 dB between 1240 nm and 1580 nm, and with losses of 1.6 ± 0.4 dB in the C-band (1530…1565 nm). In a proof-of-principle experiment, a wavelength-division multiplexing (WDM) signal with 5.25 Tbit/s aggregate data rate was transmitted through a photonic wire bond without any measurable signal degradation. Photonic wire bonding paves the path towards interconnects with spatial densities in the Pbit/s/mm range. Enabling efficient combination of different photonic device technologies, we believe the concept to be of great use for large-scale photonic integration.

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