Memory Effects in Multi-Terminal solid state devices and their Applications

Davide Sacchetto, Pierre-Emmanuel Gaillardon, Yusuf Leblebici and Giovanni De Micheli

1 Introduction

The main source of the CMOS success lies in the exponential increase of device density that the silicon industry kept true for more than 40 years reducing the unit cost of integrated circuits. Recently, the pace of scaling has been slowing down due to approaching fundamental limits at the device level. While the paradigm of scaling is still alive, researchers are striving to follow Moore's law by focusing on new materials, new device structures and new state variables. The basic building block for circuits has always been the four-terminal planar transistor but new versions of the MOSFET structure such as the double-gate FET, the FinFET, the gate-all-around nanowire FET can be found in commercial products. Due to the natural limitations of materials, future nano-scale circuits will have to exploit more efficient ways for computation and memory storage. One possible scenario envisages an end of charge-based technologies, after which computation will rely on alternative, more power efficient state variable manipulation. A long list of fundamental state variables other than charge includes the spin, phase, multipole orientation, mechanical position, polarity, orbital symmetry, magnetic flux quanta, molecular configuration, and other quantum states [1]. Technologies using new state variables would have to be implemented within a completely new technological platform, and cannot be seen as CMOS-compatible alternatives. The recent realization of devices by Stanley Williams and his team [2] gave new push to solid state research for logic and memory applications. For instance, ultra-dense crossbar memristive memory arrays can be made thanks to the compactness of the two terminal junction. Complementary logic based on two-terminal memristive devices (see Fig. 1a) or ultra-dense crossbar arrays with memristive cross-points (see Fig. 1b) can dramatically improve

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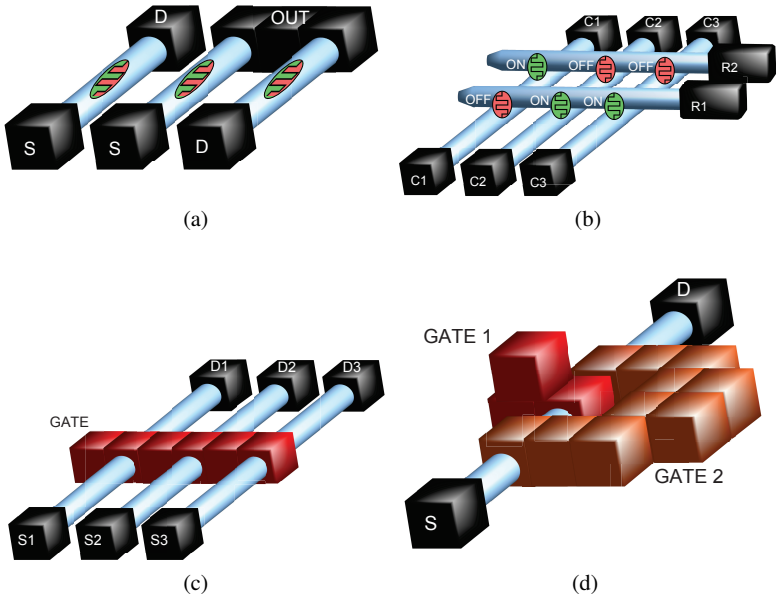


Fig. 1: (a) Parallel nanowire two-terminal memristive devices. (b) Crossbar array consisting of memristive cross-points (two-terminal). (c) Gate controlled three-terminal nanowire memristive device. (d) Double-gate four-terminal nanowire memristive devices.

device density up to 10^{11} bits per square centimetre [3]. Moreover, the use of memristive effects as new state variables for computation can be exploited to build new types of functional devices with three- or four-terminals (see Fig. 1c and Fig. 1d, respectively). The physical realization of the memristor, whose behavior was postulated by Leon Chua [4] and generalized by Chua and Kang [5] for memristive devices and systems, offers a completely new set of possibilities for logic operations [6]. It is worth noting that, a generalized model for memristive systems can be implemented under DC, small signal and sinusoidal excitation [5]. The implications of such modeling is linked with the observation of memristive functionalities over a broad range of technologies based on nanoelectronic and nanoionic behaviors. The content of this chapter is organized as follows. First, a generalization of memristive devices is given (Section 2). Then two-terminal devices with memory are discussed in Section 2.1. Applications of two-terminal memristive devices are discussed for application, such as standalone memory (Section 3.1), FPGAs (Section 3.2) and programmable TSVs (Section 4). Then, a broader categorization and discussion on multi-terminal memristive devices is given in Section **??** and applications are discussed in Section 5. Finally, we draw the conclusions.

2 Generalization of the Memristive Devices

In this section we survey the generalization of memristive theory, which is mainly a mathematical description of memory effects that can be experimentally observed in several electronic devices. The memristive functionality is not a unique property of two-terminal passive devices but mainly a memory effect related to internal state variable changes. For instance, the memristive functionality can also arise from a delayed switching response of a Zener diode [7]. As described by Di Ventra et al. [8], the memory effects in nanoscaled devices can be generalized for resistance, capacitance and inductance to their time dependent and non-linear responses. If *u(t)* and *y(t)* are two complementary constitutive circuit variables, denoting the input and the output of the system, respectively, and x is a n-order vector of internal state variables, the existance of a n-th order u-controlled memory element as that defined by:

$$\begin{cases} y(t) = g(x,u,t)u(t) \\ \dot{x} = f(x,u,t) \end{cases} \tag{1}$$

where g is a generalized system response and f is a continuous n-dimensional vector function. As described in [8], the relation between current and voltage defines a *memristive system*, while the relation between charge and voltage defines a *memcapacitive system* and the flux-current relation defines a *meminductive system*. Equations 1 can be further generalized for cases where the internal state is described by a continuous function or functions instead of discrete variables as well as cases for which the internal state variables follow a *stochastic differential equation* rather than a deterministic one. In the next sections, we review some of the two-terminal passive devices that can be modeled as memristive. The memristive functionality is seen as arising from different physical mechanism for different device classes. Thus, three- and four-terminal devices that show memristive functionality can be used for electrical control signals (either voltage or current). It is important to remember that a device showing a "pure" flux-charge relationship has not been found yet. Conversely, internal state variables can provide a stimulus response that can be modeled as memristive, thus adding more degrees of freedom for circuit designers.

2.1 Resistive RAMs

A mathematical definition of two-terminal passive mem-resistive devices has been formulated by Chua and based on this interpretation a mem-resistive device would present three fingerprints:

- pinched hysteresis loop in the *i(t)-v(t)* plane;
- passive: *i=0* when *v=0*;
- frequency dependence with the input signal *u(t)*

However, many electronic devices that were previously classified as *"memristors"* or as *"memristive devices and systems"* have been recently re-classified as their ac-

tual behavior requires an extension of the memristive theory. [9]. Nevertheless, by looking at these three fingerprints, it has been recently reported that mem-resistive behavior has been noticed in several electric devices in the past two centuries [10]. More specifically, a predominance of mem-resistive behavior seems to be linked with an electric discharge phenomenon, and as such it is believed that the first memristor was actually found in 1899 by Herta Ayrton (see Fig. 2). Later on the solid-state realization of devices by Stanley Williams and his team [2] which showed mem-resistive fingerprints gave new push to research on nano-scaled mem-resistive devices. It has been stated that the mem-resistive "fingerprints criteria" are satisfied by several resistive switching materials, and as such it becomes clear that the mathematical formulation of memristors and memristive devices does not necessarily link to a specific physical phenomenon. Considering resistive switching materials, a classification based on physical phenomena has been provided by Waser (see Fig. 3) [11].

Two-terminal memristive devices can be based on metal/oxide switches, such as for SiO_x [12], HfO_2 [13], CuO [14], NiO [15], ZnO [16], Al_2O_3 [17], VO_2 [18], $SrTiO_3$ [19]. These devices behave as solid-state electrochemical switches, whose resistance is defined by a metallic filament formation mechanism related to the solid-state redox reactions stimulated by the polarity of the applied electric field [20]. One example is the CuO-based ReRAM of Dong et al. [14], that shows repeatable resistive switching at very low voltages.

The well known TiO_2-based ReRAM [21, 22] seems to be based on a different mechanism, which is attributed to the vacancy/dopant diffusion in the oxide layer. The re-distribution of oxygen vacancies into the TiO_2 depends on the polarity of the applied voltage, and it causes the switching between a semiconductor state into a metallic one. Typical ReRAM functionality of the TiO_2-based ReRAM is shown in Fig. 4 [23], with the resistivity switching by 5 orders of magnitude.

Another type of two-terminal memristive device is the *phase change (PC)* RAM [24]. The main switching mechanism is based on phase transition between an amorphous and a crystalline type due to Joule heating effects controlled by a voltage pulse. For instance, Si nanowires can be engineered such that melting and solidification processes can be iterated, thus giving rise to alternate resistance states [25].

Another class is based on polymers [26]. Several memristive switches can be build by inter-posing a bio-molecule layer with properties ranging from molecule-dependent switching, such as rotaxanes [3], or more in general on inter-locked molecules [27] but also on molecule-independent switching, where a filament formation mechanism through the molecular layer is involved [28].

A fifth class belongs to spintronics [29]. The spin-transfer induced domain wall motion in a spin valve structure is by nature a memristive effect and is confirmed by some recently published results [30]. Moreover, Pershin et al. demonstrated that electron-spin polarization controlled by the external voltage applied to a spintronic device, acts as a state variable that can be modeled as memristance [31].

In all these devices the amplitude and frequency of the input signal contribute in the formation of a so called pinched hysteresis loop, whose salient feature is its zero crossing property [5], which is critical for ultra low power operation.

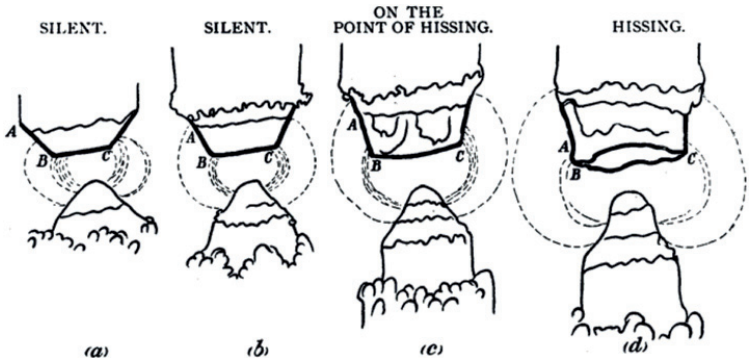


Fig. 2: The "hissing of the electric arc" as presented to the Institution of Electrical Engineers in 1899 by Hertha Ayrton. The image is taken from [10].

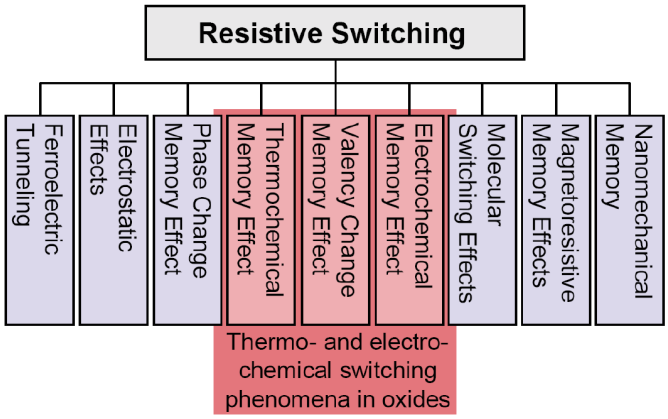


Fig. 3: A classification of resistive switching devices depending on the underlying physical mechanisms as provided by Waser [11].

2.2 Mem-Capacitive Switching Devices

As per two-terminal memristive devices, two-terminal memcapacitive devices can be based on several mechanisms. A classification has been given by Pershin et. al [8], and it is divided mainly in two categories: geometrical and permittivity-related memcapacitors.

An example of mem-capacitive switching device based on geometrical effects consists of a capacitor with a movable plate, whose movement depends on the applied electric field [32]. One such device would be a capacitor having one of the electrodes being elastic. If a voltage pulse is applied across the capacitor, the elastic plate moves towards the other electrode, in response of the electric field, thus mod-

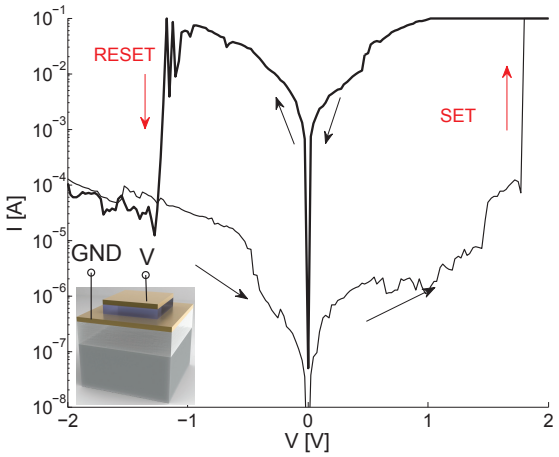


Fig. 4: Resistive switching through I-V sweeps for planar $Pt/TiO_2/Pt$ [23]. The inset shows the $Pt/TiO_2/Pt$ ReRAM sandwich layer on top of an insulated substate with the two terminal electrical contacts.

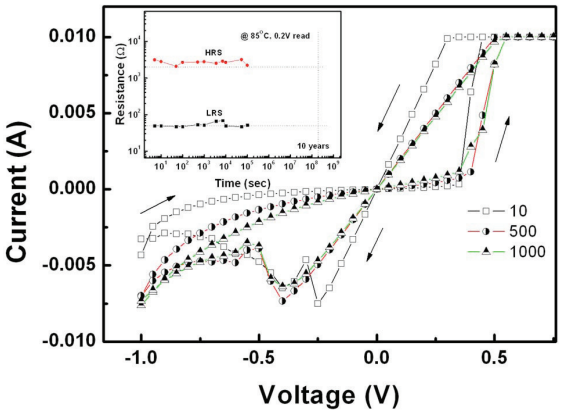


Fig. 5: Switching mechanism of a CuO-based ReRAM. The image is taken from [14].

ifing its capacitance. One possible realization of the geometrical mem-capacitor can be obtained from a *Nano Electro Mechanical System (NEMS)* resonator configuration. Such devices can be, for instance, fabricated with a CMOS compatible process flow on SOI substrates. As depicted in Fig. 8, a NEMS device consisting of a suspended SiNW and Al metal electrodes can be utilized as a geometrical-effect memcapacitor. In this device, the SiNW in the middle is utilized as an elastic electrode [33]. It is worth mentioning that the NEMS resonator can also be utilized as

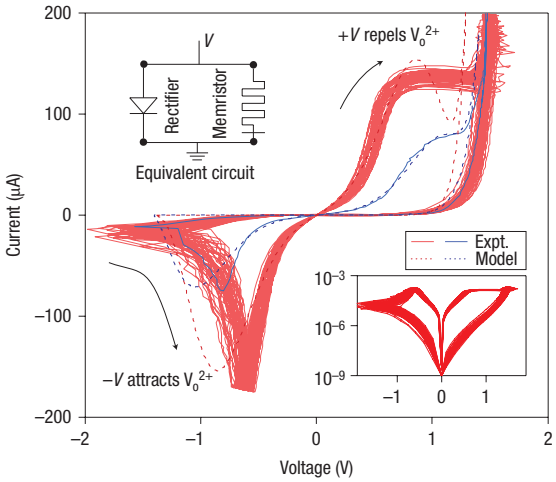


Fig. 6: Pinched hysteresis loop from a Pt/TiO_2/Pt memristive junction. The image is taken from [21].

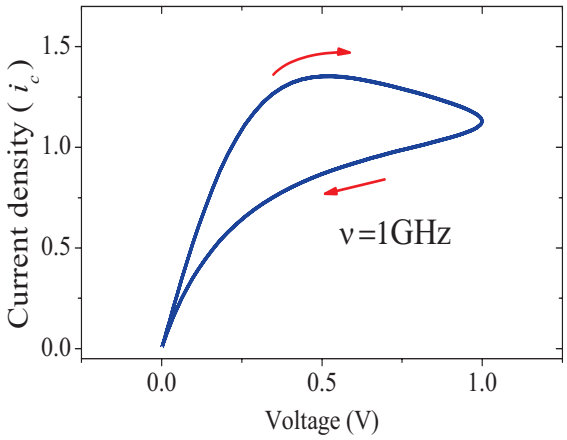


Fig. 7: Unipolar I-V simulation for a semiconductor spintronic system. The image is taken from [31].

resistive switching device, but this does not represents a case of two-terminal memristive device because its pinched hysteresis loop does not depend on the frequency of actuation, as it results on the absolute value of the DC signal (see Fig. 9).

A second example is a device whose permittivity modifies upon the application of a voltage bias. A memcapacitor proposed by Di Ventra et al [34], consists of a parallel plate capacitor with additional floating plates in between, separated by dielectrics. The internal charge can move between the different plates and its polar-

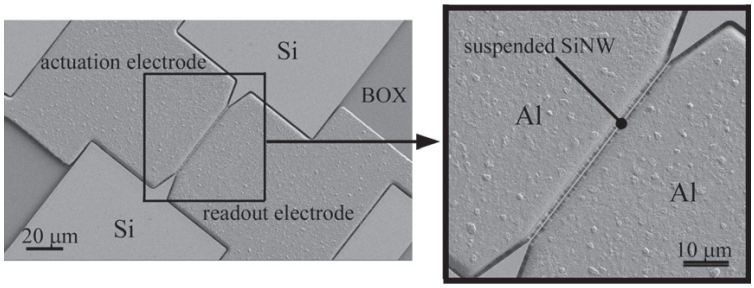


Fig. 8: NEMS resonator consisting of a SiNW and two Al side-electrodes. A two-terminal memcapacitor configuration can be obtained by using the elastic SiNW and either one of the Al pads as the electrodes. The image is taken from [33].

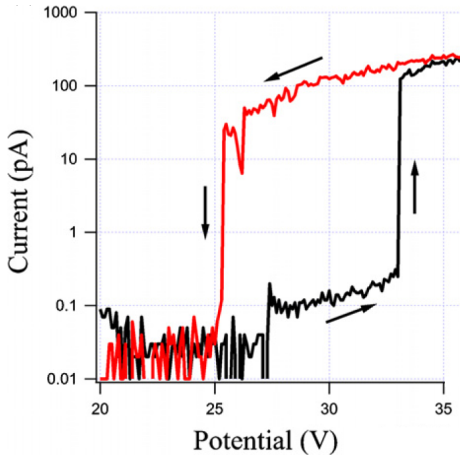


Fig. 9: Resistive switching characteristic of SiNW NEMS [33]. The hysteresis arise from the var-der-Walls forces that retain the SiNW at pull-out. Since the hysteresis does not depends on the actuation frequency, this resistive switching mechanism cannot be considered as mem-ristive.

ization can screen the electric field applied at the external plates. This way, based on the distribution of the charges in the polarized plates, a memcapacitive behavior is obtained [34].

Another memcapacitive device has been demonstrated with a III-V diode and high-κ dielectrics [35].

2.3 Mem-Inductive Switching Devices

Similarly to the memcapactive devices, geometrical effects [36] and permeability-related effects [37] can lead to an inductive system showing memory, thus forming a mem-inductive device. Several properties, including mechanical, electrical, magnetic and thermal were discussed by Pershin et al. [8] as possible mechanisms that can be exploited in a mem-inductive system.

2.4 Three-terminal memristive devices

The new concept of three-terminal memristive device is presented in terms of memristive functionality for logic and memory applications.

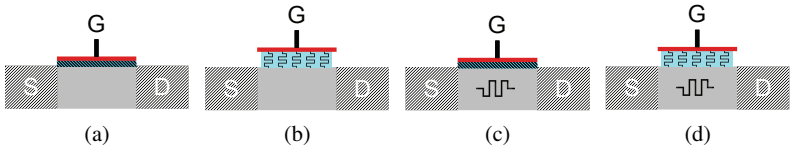
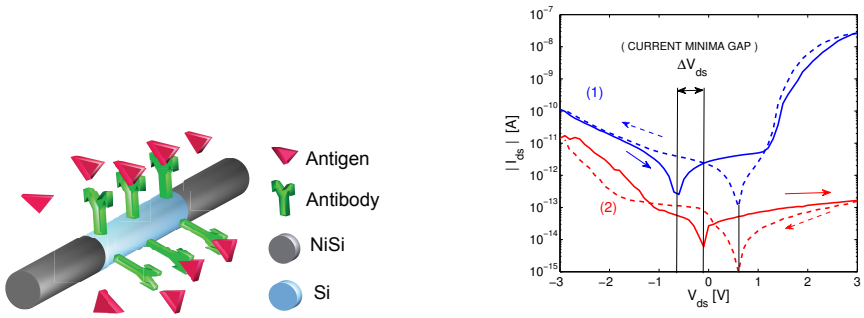


Fig. 10: Categorization of FETs with memristive functionalities: (a) Conventional FET. (b) FET with memristive gate dielectric. (c) Gated memristor (memristive channel). (d) Gated memristor with memristive dielectric.

Examples of three-terminal memristive devices are the electrochemical organic memristor [39], the solid-electrolyte nanometer switch [40], the ferroelectric FET [41], non passivated transistor devices (here cite the non-passivated CNT and graphene transistors), Carbon Nanotube and/or graphene transistors and the ambipolar Si nanowire Schottky barrier FET [42, 43].

A classification of three-terminal memristive devices can be based from the general concept of the FET structure (see Fig. 10a) in which memristive functionality can be inserted either by engineering the gate dielectric or by gating a memristive channel. For instance, trap charging dielectric layers inserted between the channel and the gate fall into the category of FET with capacitive memory storage (Fig. 10b). One example in this category can be the flash memory for which the trap charging into the gate dielectric influences the transconductance state of the channel [44]. Thus a first category that exploits the operation of writing/erasing cycles into the gate dielectric will be a generalization of the flash memory concept, for which volatility of the charges that are injected into the trap charging layer can be tuned accordingly to a desired frequency response. Such a device has been recently demonstrated by Ziegler et al. [44] by using a FLASH transistor in a two-terminal configuration. As depicted in Fig. 13, the device can be operated such that a bipo-



(a) (b)

Fig. 11: a)Suspended functionalized Si nanowire with NiSi extremities. The functionalized layer is capable of trapping antigen molecules which in turn affects the memristive hysteresis behavior, giving a new method for bio-sensing [38]. b) A typical memristive hysteresis is observed; the blue curve (1) is measured after drying the sample from de-ionized water. The red curve (2) is measured after dipping in 5 pM antigen solution and drying. The measured ΔV_{ds} is proportional to the concentration of antigen [38].

lar resistive switching behavior is measured and non-volatility is a consequence of trap-charging into the floating gate.

Another memristive functionality is linked with charging/decharging mechanisms into the gate dielectric. We measure I_{ds} for constant $V_{ds} = 1$ V while sweeping V_{gs} back and forth between -5 V and $+5$ V (see Fig. 14d). The devices are not annealed, and the source is connected to the substrate. This measurement is repeated for different integration times; which is a parameter of the measurement set-up that can be set by the operator; and it represents the time over which the measurement is repeated and averaged. The $I_{ds} - V_{gs}$ curves show an ambipolar behavior, meaning a large current conductance under either high and low gate bias. This is mainly due to the utilization of a silicide (NiSi) having a work function value that falls within the silicon bandgap, and to the utilization of a lightly doped silicon. On the other hand, the $I_{ds} - V_{gs}$ curves have a hysteretic behavior that suggests the hypothesis of charge trapping at the semiconductor/oxide interface of the MOS capacitor, as well as the existence of interface states at the metal/semiconductor junction. Both ambipolarity and hysteresis depend on the integration time (see Fig. 14). When V_{gs} reaches $+5$ V in forward mode, the electrons experience a maximum probability of charges being trapped in the gate oxide, which is enhanced when the integration time is longer. Due to the electron trapping at the gate oxide, the channel operates in accumulation mode, with a lower conductance state for positive V_{gs}, than in the inversion mode for negative V_{gs}. Sweeping V_{gs} back to negative values, reduces the amount of electrons trapped and the device operates in inversion mode, which restores the higher conductance state.

The threshold at which this high conductance state is reached depends on the integration time. The hysteresis window is larger when the integration time is shorter, because the charges have less time to be trapped and detrapped. In the case of a very short integration time the charges cannot be completely trapped and the lower conductance state is not reached (see Fig. 14).

Another example can be the *zero-capacitor RAM (ZRAM)* and the *twin-transistor RAM (TTRAM)*, which rely on floating body effects in SOI transistor to provide a volatile hysteresis effect [45, 46].

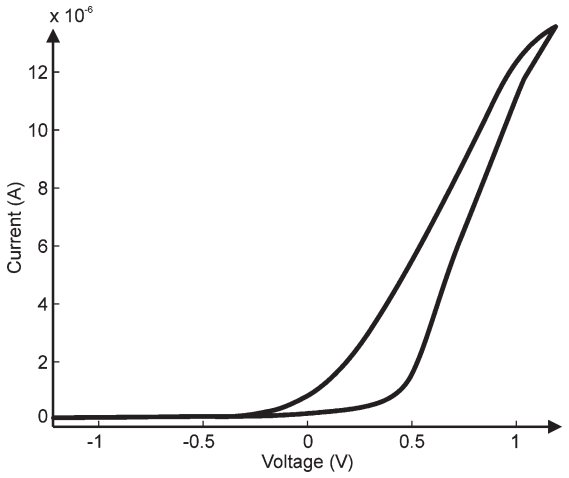


Fig. 12: Cyclic voltage measurement showing bistable memristive behavior. The image was taken from [39].

A second category is the one of the gated memristor (Fig. 10c). A few examples are the electrochemical organic memristor [39], the bio-memristive nanowire [38] and the solid-electrolyte nanometer switch [40]. In the electrochemical organic memristor the gate potential is represented by the potential of the bath, which is used to transfer positively charged Rb^+ ions into a polyaniline (PANI) layer [47]. The conductivity change can be iterated by switching the polarity of the bath potential, thus giving rise to a unipolar I_{ds}-V_{ds} curve that can be modeled as a memristor. In this case the device can be set into either memristive or diode functionality. Similarly, a novel method for bio-sensing that has been recently proposed exploits the memristive effect to detect low concentration of bio-molecules [38]. The device consists of a NiSi/Si/NiSi nanowire structure coated with antibody layer (see Fig. 11) shows memristive behavior. The hysteresis loop of this device has been demonstrated for detection of low concentrations of bio-molecules (antigen) in a dry environment (see Fig. 11b). Conversely, the three-terminal solid-state electrolyte nanometer switch shows a typical bistable resistance state but using 100 times less

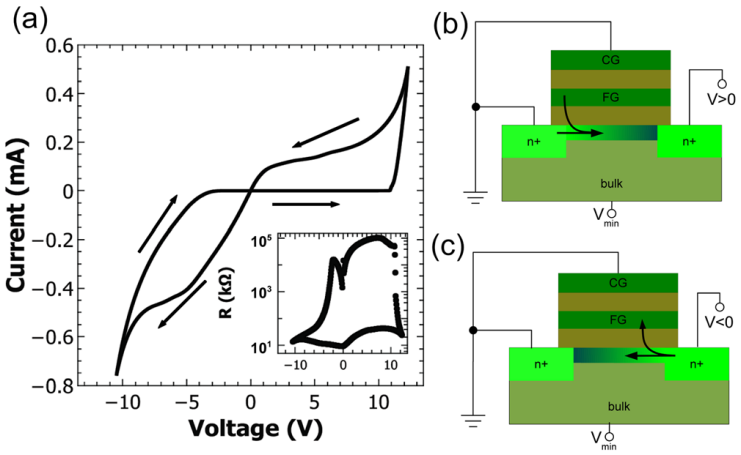


Fig. 13: Two-terminal memristive configuration of a FLASH memory cell. Depending on the polarity of the applied voltage, trap charging dynamics of electrons to and from the floating gate and dielectric is responsible of the hysteresis. The image was taken from [44].

current than standard two terminal operation [48]. This device is based on controlling the filament formation mechanism using the voltage of a gate terminal (see Fig. 15).

The ambipolar SB FET with SiNW channel reported in [49] (see Fig. 10d), falls in both categories of gated memristor and trap charging dielectric, as it shows dynamic trap charging mechanisms at the Schottky junctions and in the gate dielectric insulator. The result depicted in Fig. 16 shows a hysteretic behavior that is reminiscent of a two-terminal monolithic memristive device [50]. The hysteresis reflects the fact that the $I_{ds} - V_{ds}$ curve for forward V_{ds} sweep is not identical to the same curve for backwards V_{ds} sweep. It can be attributed to the presence of interface states at the metal/semiconductor junctions as reported in literature for Schottky diodes [51]. First, two-terminal measurements are performed. The drain-source current I_{ds} is measured vs. the drain-source voltage V_{ds} at constant $V_{gs} = 5\ V$. The device is equivalent to two back-to-back Schottky diodes. The two diodes operate in opposite regimes: for negative V_{ds}, the source-to-channel diode is reversely biased while the drain-to-channel diode is forward biased. For positive V_{ds} both diodes invert their respective bias conditions. In either case, I_{ds} is limited by the current flowing in the reverse-biased diode. The reverse current of a metal-insulator-semiconductor diode has been observed to be very sensitive to charge trapping at the metal/semiconductor interface [17]. The large current value in the range of mA is most likely due to the large parallel parasitic structure in the bulk. In an ideal Schottky diode, the current is given by:

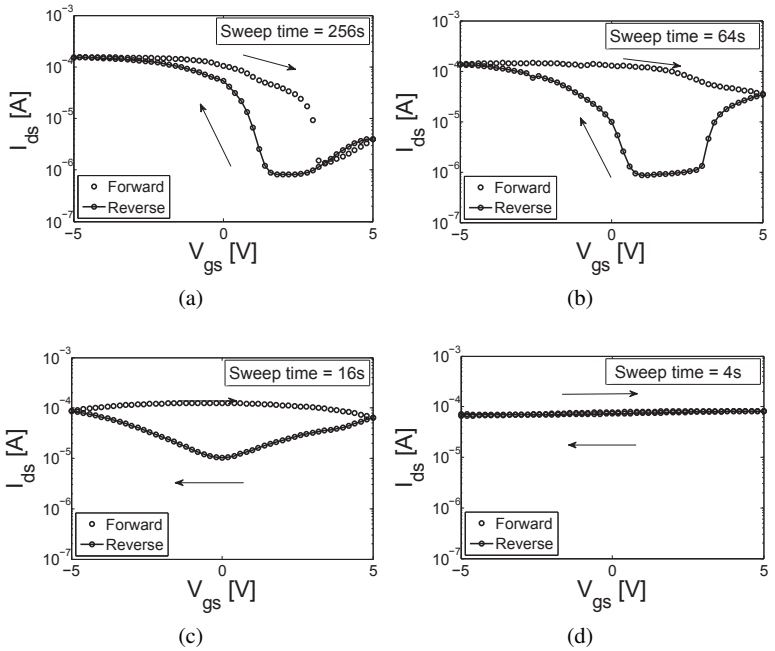


Fig. 14: Hysteretic dependence with the measurement (sweep time) duration, the hysteresis window closes by reducing the measurement time: (a) 256 sec. (b) 64 sec. (c) 16 sec. (d) 4 sec.

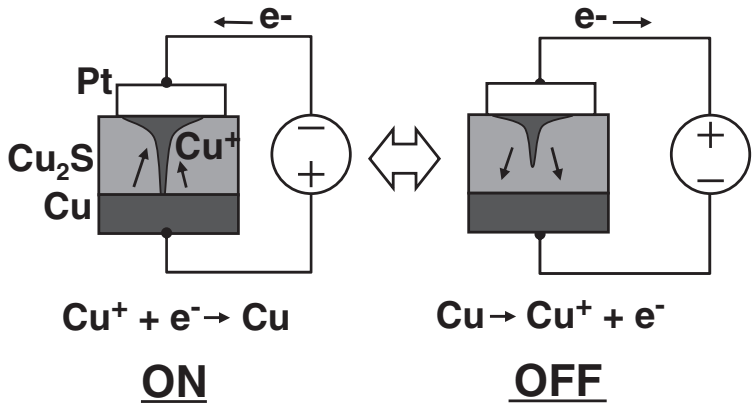


Fig. 15: Controlled filament formation of the three-terminal nanobridge device. The image was taken from [48].

$$I = I_S \cdot e^{-\phi_B q/kT}(e^{Vq/kT} - 1) \tag{2}$$

with I and V the diode current and voltage respectively, ϕ_B the Schottky barrier, k the Boltzmann constant, q the elementary charge and T the absolute temperature. From the measured hysteretic behavior, it seems that the diode curve is modified as follows:

$$I = I_S \cdot e^{-\phi_B q/kT}(e^{(V-V_0(V))q/kT} - 1) \tag{3}$$

with V_0 a built-in voltage at the Schottky contact that is positive for a positive V sweep and negative for a negative V sweep.

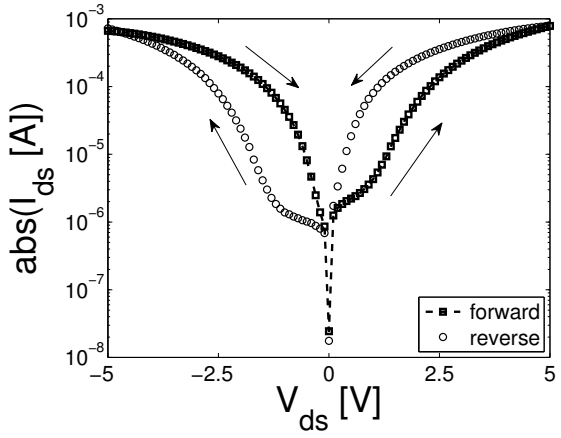
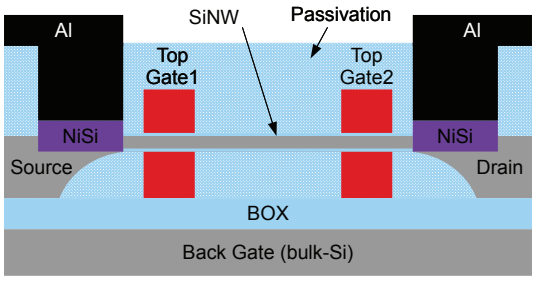


Fig. 16: $I_{ds} - V_{ds}$ characteristic showing the trapping/detrapping of charges at the metal/semiconductor junction. The device channel consists of 10 SiNW in parallel. The forward sweep curve has a symmetrical correspondence with the reverse sweep curve, showing the respective Schottky barrier modulation. A current ratio of about 50 is found at either $V_{ds} = \pm 1V$. This behavior is typical of two-terminal memristive devices for ReRAM applications.

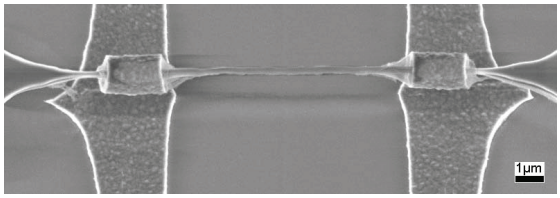
2.5 Four-terminal memristive devices

Memristive functionality can be seen as state variable that can be used for more expressive logic gates [6]. For instance, the memristive behavior reported in Section 2.4 for the SB SiNW FETs can be tuned by operating on the polarity of the gate voltage. This type of behavior is linked with the double conductance, for holes and electrons. As described in [52] for SB *carbon-nanotube (CNT)* FETS, the ambipolarity can be controlled by using an additional control gate, such that it blocks

one type of carrier conductance. Following this principle, four-terminal memristive SB SiNW FETs can be built (see Fig. 17). In the following, two modes of operation are reported, depending on the nature of the controlling signal applied at the Si nanowire channel.



(a)



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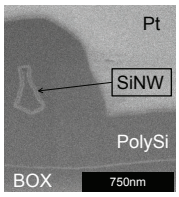
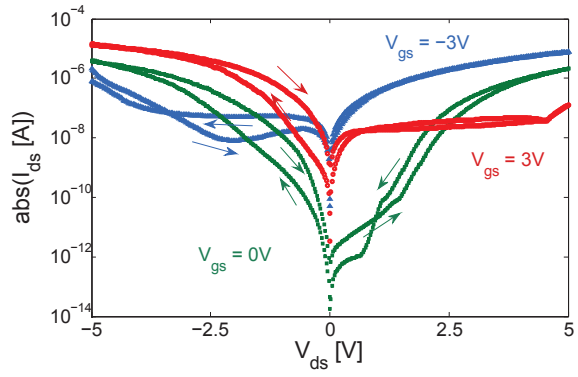


(c)

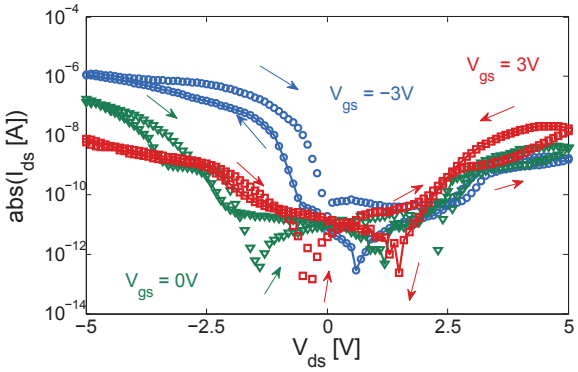
Fig. 17: (a) Schematic cross-section of a dual gate device with NiSi source and drain regions on SOI substrate. (b) A 20 μm long SiNW with 2 parallel GAA polysilicon gates having 4 μm gate lengths. (c) A FIB cut cross-section image showing the SiNW channel surrounded by a 500 nm polysilicon top gate.

2.5.1 Voltage-controlled 4-T memristive device

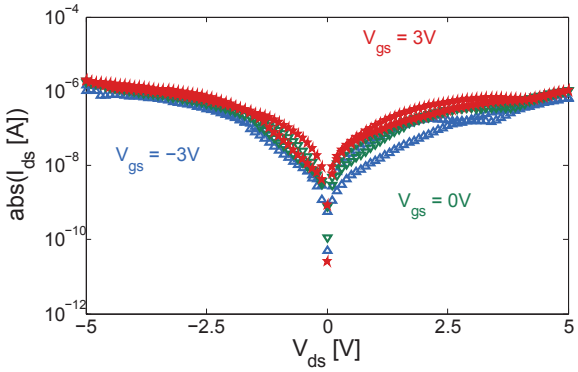
A voltage-controlled four-terminal memristive Schottky barrier SiNW FET is obtained by using a dual gate configuration such that one of the two gate is controlling a portion of the channel that is between the source/drain contacts and the main gate. This configuration is exploited to control the ambipolarity imbalance, such as for CNT FETs [52]. Since the back-gate voltage modifies the ambipolar conductance, this fact can be used in ambipolar memristive devices to limit the current levels for one of the carriers. A fixed back-gate voltage V_{bg}=+5 V (see Fig. 18a) leads to imbalanced bistable hysteresis loops under different V_{gs} voltages. By applying a negative V_{bg}=-5 V this imbalance is toggled to the negative side of the characteristics, giving a complementary effect (Fig. 18b). Finally, a V_{bg}=0 V (Fig. 18c) levels off the conductances of electrons and holes, giving a fairly symmetric hysteresis.



(a)



(b)



(c)

Fig. 18: (a) Controlled memristance for fixed top and back gate voltages V_{bg} = + 5 V. (b) Controlled memristance for fixed top and back gate voltages V_{bg} = - 5 V. (c) Controlled memristance for fixed top and back gate voltages V_{bg} = 0 V.

2.5.2 Current-controlled 4-T memristive devices

A current-controlled version of the four-terminal memristive Schottky barrier SiNW FET is obtained by using a current I_{ds} bias instead of a V_{ds}. The output voltage is then compared with V_{gs} (Fig. 19). The obtained hysteresis can be used as a latch device, whose position in the $V_{out} - V_{in}$ plane can be adjusted by using a different value of the current bias. A similar behavior has been exploited with three-terminal Schottky-barrier polysilicon nanowire FETs circuits to build a new logic family based on precharge and evaluation scheme [53]. Moreover, a similar scheme has been demonstrated for DRAM type of memory [54] and for pA current and temperature detection [55]. Similarly, SB Si nanowire transistors fabricated with a low termal budget process and biased in current-controlled mode shows a similar hysteresis. Moreover, polycrystalline SiNWs SB FETs can give an hysteretic transfer characteristic (Fig. 20) very similar to the one reported for crystalline SiNW SB FETs fabricated with a low thermal budget process [56]. As it is shown in Fig. 20 the maximum output voltage in the transfer characteristics increases with the I_{ds} bias current. From Fig. 20a-20c the sweep time is reduced. Similarly to what was discussed for the three terminal SB SiNW FET memristive device, the sweeping time impacts on the amount of charge that traps at the gate oxide/channel interface, thus influencing the conductance state of the nanowire channel. A faster sweeping time outbalances the charge trapping/detrapping mechanism, resulting in lower output voltages (see Fig. 20a-20b compared with Fig. 20c).

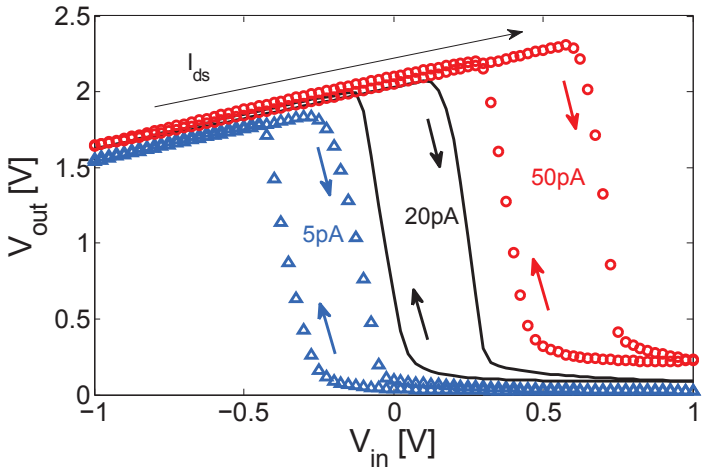


Fig. 19: Current-controlled memristive Schottky barrier SiNW FET hysteresis loop.

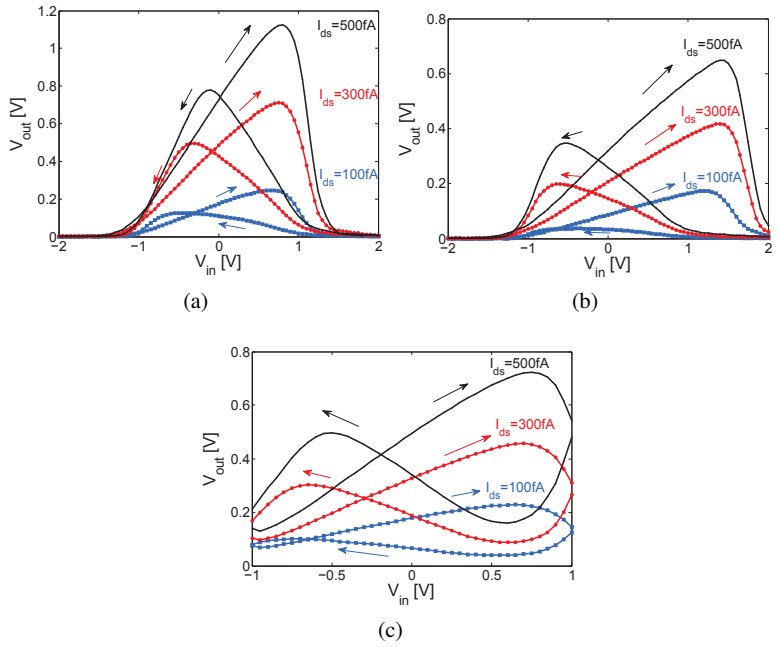


Fig. 20: V_{out} voltages for increasing with I_{ds} current bias. In all the figures I_{ds} bias values are 100 fA, 300 fA and 500 fA. Notice the output voltage hysteresis narrows for increasing frequency sweep: (a) 24sec. (b) 6sec. (c) 0.5sec.

3 Applications of Resistive RAMs

3.1 Standalone Memories

Future deeply scaled circuits will see their performances limited by the physical limitations of the materials. To keep pushing the performance of computation and the density of storage, the microelectronics industry envisages using more efficient state variable than the electronic charge. In this sense, the memristor is an attractive candidate for both computation and memory, thanks to its programmable resistive state. When considering the Resistive RAM (ReRAM) memories, which can be classified as memristors, excellent scalability and programming time can be obtained if compared to traditional Flash, which make ReRAMs suitable candidates for standalone memory applications.

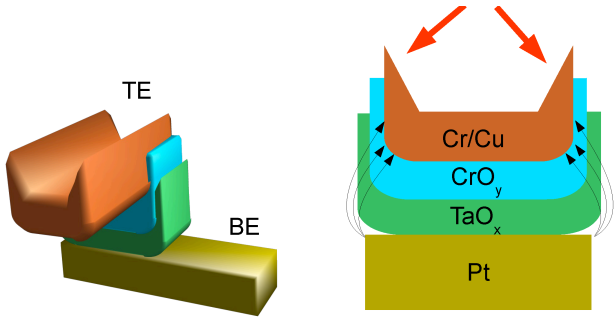
In this section, a ReRAM technology demonstrating a *Multi-Level (ML)* forming-free $Pt/TaO_x/CrO_y/Cr/Cu$ crossbars built with low thermal budget $\leq$200°C is discussed. The devices show excellent scalability down to $2.5x10^9 bit/cm^2$ with device half-pitch of 100nm with projections of practical storage density of up to $10^{12} bit/cm^2$ at the 10nm technology node [57].

3.1.1 Fabrication

The basic device concept is a ReRAM consisting of 2 metal lines crossing orthogonally and a transition metal oxide stack in between (see Fig.37a). Moreover, the shape of the *Top Electrode (TE)* has been fabricated such that corners are smoothed (Fig.37b). This feature reduces the fringing field intensity at the wire ends, thus improving both reliability and scalability of the devices. Two different ReRAM ($Pt/TaO_x/CrO_y/Cr/Cu$ and $Al/TiO_2/Al$ with the Bottom Electrode/Transition Oxide/Top Electrode order) stacks have been built and compared in terms of performance. Both stacks have forming-free property and as such they do not require special forming steps to form the devices. This is a considerable advantage for actual implementation on chip. Several devices have been built in a passive crossbar array fashion as explained in the following text. Si bulk wafers are first isolated by depositing 100nm thick Al_2O_3 with *Atomic Layer Deposition (ALD)* (Fig. 38a). Then, PMMA bi-layers are patterned with e-beam lithography as lift-off masks for 10nm/80nm Pt *Bottom Electrodes (BE)* deposition (Fig.38b). In the next step, a second lift-off mask is defined and 15nm TaO_x oxide layer (Fig.22c) is deposited by sputtering from a Ta_2O_5 target with increasing RF power in Ar/O_2 atmosphere (Fig.22e). Finally, 50nm/100nm thick Cr/Cu bi-layers TE are deposited by e-beam evaporation (Fig.22d). For $Al/TiO_2/Al$ devices, the Al electrodes are deposited with e-beam evaporation while 10nm thick TiO_2 is deposited by ALD. In Fig.23a and 23b SEM images of 100nm wide BE lines and 64bit passive crossbar are shown, respectively. In Fig.23c, a 3D reconstructed AFM profile is shown. About 250 individual $Pt/TaO_x/CrO_y/Cr$ cross-points for area sizes varying from 100nm x 100nm to 1μm x 1μm, and 64bit crossbars with half-pitch varying from 100nm x 100nm to 500nm x 500nm are built on the same sample following the proposed fabrication steps. In Fig.24a and Fig.24b, a tilted SEM view, and a 3D reconstructed AFM profile of a cross-point device with fence-like TE are shown, respectively.

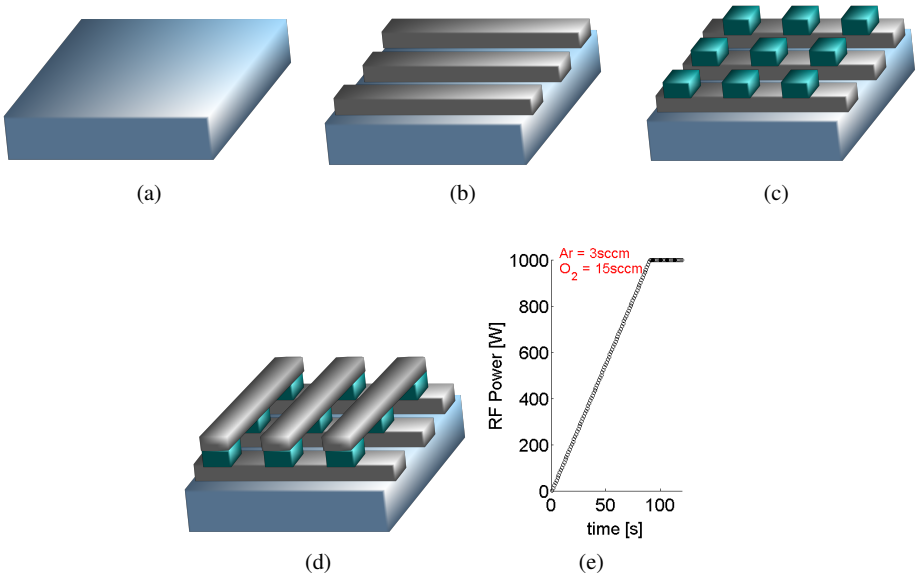
3.1.2 Electrical Characterization

Electrical measurements are carried out with an Agilent B1500 semiconductor device analyzer. Pulse mode sweeps with pulses of 500μs demonstrate forming-free *Bipolar Resistive Switching (BRS)* for $Pt/TaO_x/CrO_y/Cr/Cu$ (Fig.39c). The BRS is obtained for a voltage range of less than 1V with pristine ON state in the same range of the *Low Resistance State (LRS)*. This is an important advantage compared with non forming-free ReRAM devices, because the forming operation requires higher voltages. A forming voltage of -3.4V has indeed been necessary for the $Al/TiO_2/Al$ (Fig.25b), that then show similar performance as the $Pt/TaO_x/CrO_y/Cr/Cu$ devices. In Table I structural and electrical parameters of the different cells are reported.



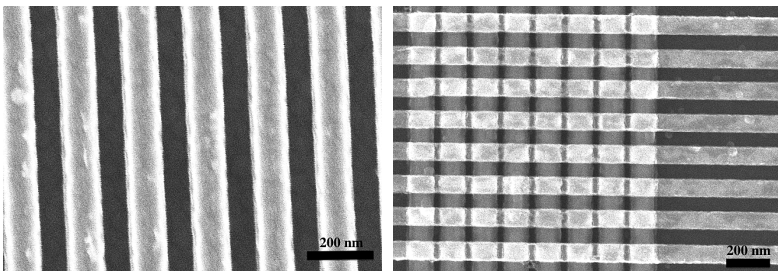
(a) (b)

Fig. 21: (a) 3D cross-point ReRAM concept with fence-like Top Electrode (TE) shape. (b) Lateral cross-section view of $Pt/TaO_x/CrO_y/Cr/Cu$ cross-point ReRAM device. The fence-like TE enables better scalability of the cross-point device thanks to a reduction of the intense electric field distribution at the corners.

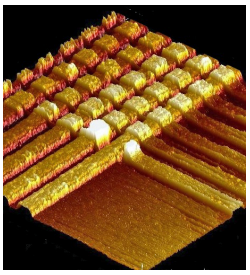


(a) (b) (c) (d) (e)

Fig. 22: Process Flow. (a) Insulated Si substrate; (b) Pt bottom electrode lift-off; (c) TaO_x sputtering deposition; (d) TE lift-off (e) Sputtering parameters of TaO_x, with increasing RF power and constant 3sccm/15sccm Ar/O_2 flows.

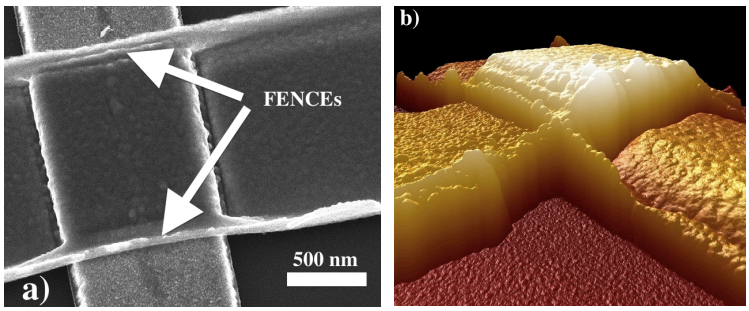


(a) (b)



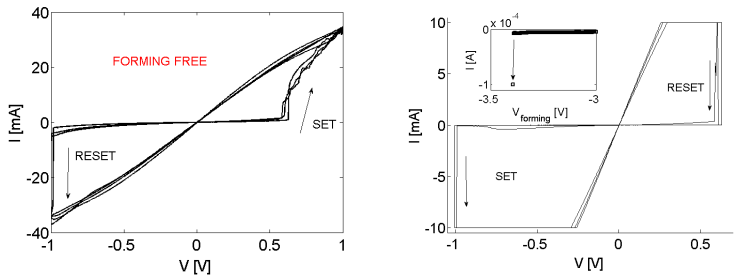
(c)

Fig. 23: Top SEM view of: (a) bottom electrode lines; (b) complete 64bit cross-bar array of devices with 100nm half-pitch; (c) reconstructed 3D image from AFM profile.



(a) (b)

Fig. 24: $Pt/TaO_x/CrO_y/Cr/Cu$ cross-point device with 900nm x 900nm cross-point area. (a) Tilted SEM image view. Notice the fence-like structures at the edges of the TE line. (b) Reconstructed 3D AFM image of the pristine cross-point device. Average roughness on TE is $\sigma \approx$42.6nm.



(a) (b)

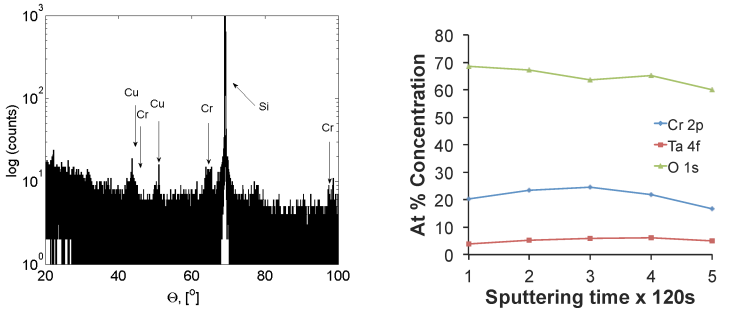
Fig. 25: (a) Typical I-V characteristic of the $Pt/TaO_x/CrO_y/Cr/Cu$ ReRAM cell showing resistance ratio of 10^4. Notice very low $V_{SET} = +0.8V$ and VRESET=-1V. After fabrication the devices are forming-free and in the ON state. (b) Typical I-V characteristic of the $Al/TiO_2/Al$ ReRAM cell after forming with $V_{SET} = -1V$ and $V_{RESET} = +0.8V$. Inset shows $V_{FORMING} = -3.4V$.

3.1.3 Discussion

Material characterization has been carried out to understand the pristine ON state of the $Pt/TaO_x/CrO_y/Cr/Cu$ device. The X-ray diffraction pattern of Fig.26a shows peaks from the TE and the Si substrate. The absence of any Ta_2O_5 or TaO_2 peaks indicates that the material is in amorphous state, due to the low deposition temperature. The visible peaks are related to the presence of Cu and Cr metal layers on top of the TaO_x/CrO_y. The Si peak comes from the substrate and it has been utilized for the calibration of the X-ray diffractometer. The pristine ON state excludes the conductive filament mechanism and observing the double logarithmic plot of the I-V curve (Fig.27a), quasi-Ohmic regimes with slopes $\approx$1 are obtained for regions far from the SET condition. Typical trap-assisted *Space-Charge-Limited-Conduction (SCLC)* is observed close to the SET condition. The SCLC conduction is also observed for $Al/TiO_2/Al$ devices (Fig.27b) whose slopes indicate a more abrupt distribution of trap density, which can be related to the different deposition methods. In both devices, the resistive switching mechanism can be attributed to Redox reaction linked with the motion of oxygen-vacancies [58, 59]. Moreover, structural modification is observed from the roughness profile of $Pt/TaO_x/CrO_y/Cr/Cu$ cross-point after 100 cycles. As shown in Fig.28a and Fig.28b, the $Pt/TaO_x/CrO_y/Cr/Cu$ average roughness (Ra) measured above the TE broadens. The Ra changes from a pristine 100nm variation into a 200nm broad window, indicating structural modification by the motion of oxygen vacancies upon switching. In addition, XPS-depth analysis (Fig.26b) confirms that $Ta_2O_{5-\delta}$ and $TaO_{2-\gamma}$ phases are present, with more conductive $TaO_{2-\gamma}$ close to the Pt BE and mixture of $TaO_{2-\gamma}$ and CrO_y at the Cr/Cu TE that is consistent with the Redox switching mechanism.

3.1.4 High Density Multi-Valued Crossbars

Several resistance levels of $Pt/TaO_x/CrO_y/Cr/Cu$ devices can be programmed. As shown in Fig.29a, four levels of resistance (encoding 2bits) are found within a 4 orders of magnitude range. A larger resistance window of 1bit is found for $Al/TiO_2/Al$ devices, which show a LRS around 30Ω and a *High Resistance State (HRS)* at $1M\Omega$ within 2 orders of magnitude variation (see Fig.29b). The $Al/TiO_2/Al$ show stable LRS and HRS in a large V_{READ} voltage range (Fig.30a). The $Pt/TaO_x/CrO_y/Cr/Cu$ devices demonstrate excellent scalability, as the HRS/LRS ratio improves for smaller device sizes (Fig.30b). For instance, 2bit can be written in a $Pt/TaO_x/CrO_y/Cr/Cu$ by using shorter SET pulses in order to program the cell in one of the stable *Intermediate Resistance (IR)* states. An example of 2bit storage using LRS, HRS and 2 IRs is demonstrated in Fig 31, each level is separated of about one order of magnitude from each other for various V_{READ}. The devices could be easily assembled into dense $2.5x10^9 bit/cm^2$ passive crossbar arrays whose storage density improves to $10^{10} bit/cm^2$ thanks to ML capability of $Pt/TaO_x/CrO_y/Cr$ ReRAMs.

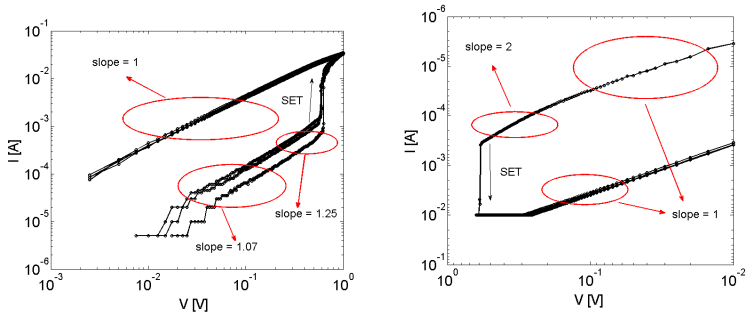


(a) (b)

Fig. 26: (a) X-ray diffraction pattern on a Si wafer demonstrating amorphous TaO_x/CrO_y. The peaks are related to the presence of Cu and Cr metal layers on top of the TaO_x/CrO_y. The Si peak comes from the substrate and it has been utilized for the calibration of the X-ray diffractometer. (b) XPS depth profile analysis showing the presence of both Cr and Ta in oxidized states. Both $Ta_2O_{5-\delta}$ and$TaO_{2-\gamma}$ are present, with more conductive $TaO_{2-\gamma}$ close to the Pt BE and mixture of $TaO_{2-\gamma}$ and CrO_y at the Cr/Cu TE.

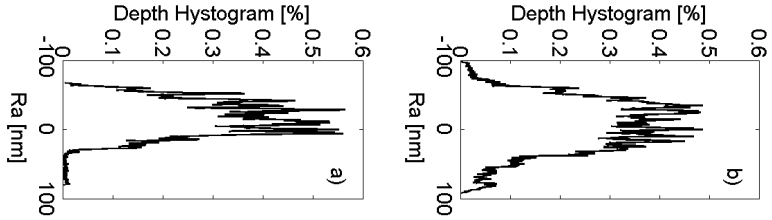
3.1.5 Summary

Bipolar Resistive Switching $Pt/TaO_x/CrO_y/Cr/Cu$ and $Al/TiO_2/Al$ devices built with thermal budget $\leq 200°C$ have been fabricated and characterized. Very large



(a)

Fig. 27: (a) The log(I)-log(V) plot of $Pt/TaO_x/CrO_y/Cr/Cu$ shows typical trap-controlled conduction of *Space-Charge-Limited-Conduction (SCLC)* before SET. In the SET region, the slope is about 25 and it is indication of gradual distribution of defects. (b) The log(I)-log(V) plot of the $Al/TiO_2/Al$ shows typical trap-controlled conduction of SCLC with quadratic V dependence before SET condition, thus following Childs law dependence. In the SET region, the slope is about 50, and it is indication of an abrupt distribution of defects.



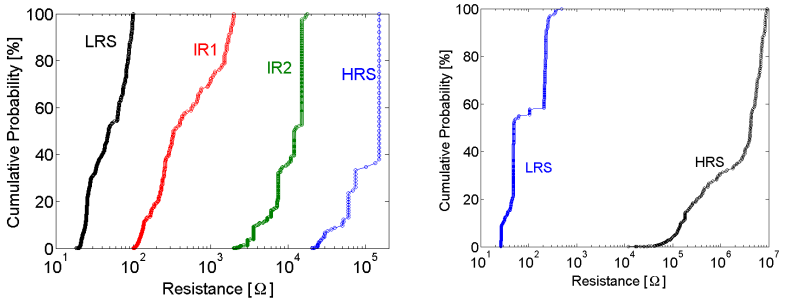
(a) (b)

Fig. 28: Average roughness profiles for TaO_x cross-points: (a) $\sigma \approx 42.6$nm after fabrication; (b) $\sigma \approx 56.3$nm after 100 cycles. The broadening is attributed to the structural change induced by the motion of oxygen-vacancies upon cycling.

storage density of TaO_x/CrO_y-based ReRAMs is demonstrated up to 10^{10}bit/cm^2 thanks to the excellent scalability of the fence-like top electrode lines.

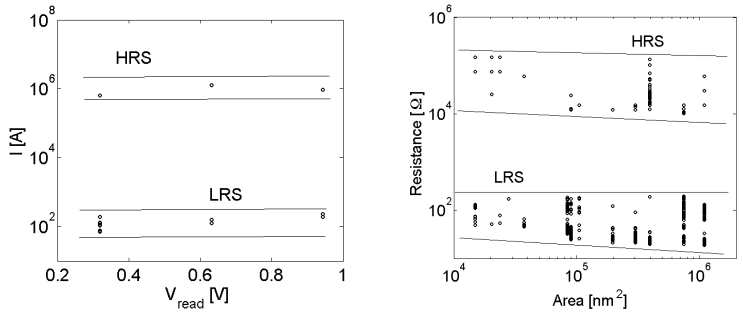
3.2 Generic Memory Structure (GMS) for non-volatile FPGAs

While a lot of research effort targets high density ReRAM-based standalone memories [60], the focus of this work is the usage of ReRAMs for FPGAs. The reason



(a) (b)

Fig. 29: (a) Cumulative probability of *Low Resistance State (LRS)*, *Intermediate Resistance states 1 (IR1) and 2 (IR2)* and *High Resistance State (HRS)* for $Pt/TaO_x/CrO_y/Cr$ devices are shown. The LRS, IR1 and IR2 are obtained by using SET pulses of 2ms, 1ms and 500μs at 1V, respectively. The HRS is obtained with a 500μs RESET pulse at -1V. (b) Cumulative probability of LRS and HRS for $Al/TiO_2/Al$ devices are shown. The LRS and the HRS are obtained by using SET and RESET pulses of 500μs at -1V and +1V, respectively.



(a) (b)

Fig. 30: (a) LRS and HRS resistance distributions for increasing V_{READ} of the $Al/TiO_2/Al$ cell. The 10^4 resistance ratio is constant over a large range of reading voltage. (b) Measured HRS and LRS values for the $Pt/TaO_x/CrO_y/Cr$ cell devices with different cross-point area demonstrating excellent scalability, indicating local switching at the nanoscale.

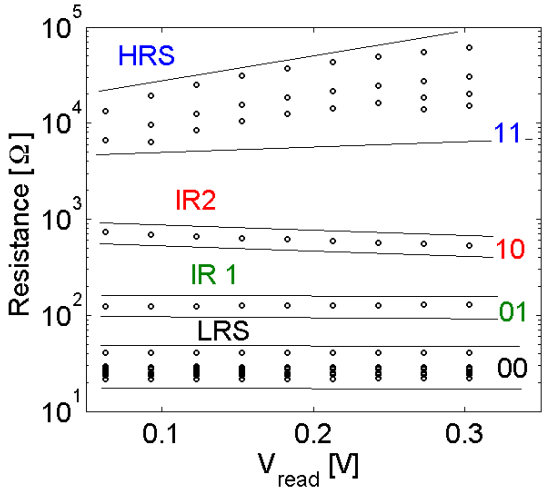
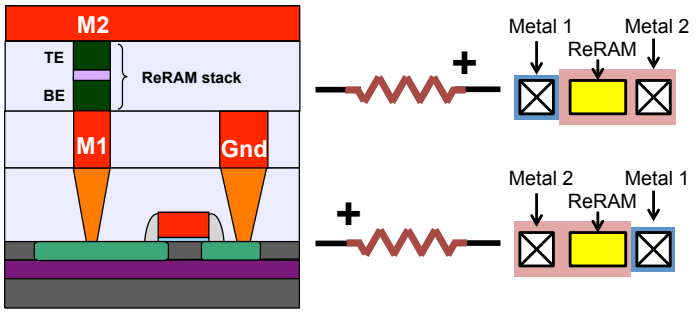


Fig. 31: Resistance distributions for multi-value storages vs. increasing V_{READ} of the $Pt/TaO_x/CrO_y/Cr$ cell. The HRS, IR2, IR1, LRS are encoded in 2bit.

behind this choice is that in reconfigurable logic, up to 40% of the area is dedicated to the storage of configuration signals [61]. Traditionally, the configuration data is serially loaded in SRAM cells, distributed throughout the circuit [62]. As a consequence, power up of the circuit is limited by the slow serial configuration. To overpass SRAM volatility and loading time issue, Flash NVM have been proposed [63]. Nevertheless, the use of an hybrid CMOS-Flash technology results in high fabrication costs. Conversely, ReRAMs are fabricated within the Back-End-of-the-Line (BEoL) metal lines, moving the configuration memory to the top of the chip and reducing the area utilization [64]. Similarly, the ReRAM cells can be utilized in combination with TSVs, enabling 3-D stacked FPGA architectures [23]. In this section, we propose a complete proof of concept of an ReRAM-based *Generic Memristive Structure (GMS)* circuit for FPGAs from technology development to architectural evaluation. The main idea is to replace the pass-transistors in SRAM-based FPGAs by ReRAMs. Hence, the ReRAMs store the information in their resistive states and can be either used to route signals through low resistive paths, or to isolate them by means of high-resistive paths. Such a functionality is envisaged either to build routing Multiplexers (MUXs) or configuration nodes. In order to keep the programming complexity in the same range of SRAM-based FPGAs, we propose an efficient methodology based on the inherent GMS complementary programming. The proposed methodology, with GMS-based complementary programming has been validated by electrical measurements on a fabricated device.

3.2.1 BEoL integration of ReRAMs

As per the previous section, ReRAMs can be fabricated within the BEoL processing. Hence, it is possible to fabricate them between two metal layers (e.g. in between Metal 1 and Metal 2). Because of the BRS of the ReRAMs of this study, depending on the forming polarity, either the Metal 1 or the Metal 2 terminal can be utilized as the positive electrode of the memory, giving two possible configurations (see Fig.32a).



(a) (b)

Fig. 32: Cross sectional schematic showing the integration of a ReRAM integrated between the M1 and M2 interconnection levels in the Back-End-of-the-Line. (a) The bottom electrode is thus directly connected to a MOSFET selector (bottom) forming a 1-Transistor 1-Resistor (1T1R) memory node. (b) ReRAM polarity selection by physical design.

3.2.2 Device Description

In the GMS, two ReRAMs are interconnected as shown in Fig.33a. The positive terminal of the top memory is connected to the negative terminal of the bottom memory. This arrangement enables complementary programming of the two ReRAMs composing a GMS. We call the concurrent programming of the GMS a complementary programming operation. A similar programming scheme was previously used for low power crossbars [65]. Fig.33b illustrates the programming of the top path (i.e. left to right arrow in the programming graph shown in Fig. 33d). R_1 andR_2 are switched simultaneously to R_{OFF} and to R_{ON} respectively. This operation is achieved by grounding the common right terminal and biasing the left terminal to Vth (which corresponds to the SET voltage -Vth for R_1 and to the RESET voltage +Vth for R_2). The programming of the bottom path (see Fig.33c) is obtained by inverting the Vth and the GND (which corresponds to the RESET voltage for R_1 and

to the SET voltage for R_2). In addition to speed up the programming operation, due to the complementary scheme, only two voltages are needed (GND and Vth). The complementary programming operation has been validated by electrical measurements, while the MUX performances have been extracted by electrical simulations. Fig.34 depicts the resistance values of R_1 and R_2 of an GMS-based MUX21. Resistances are read at $V_{READ} = +0.1V$. After a preliminary forming step, R_1 and R_2 are set to R_{ON}. The devices are then read for 10 cycles, showing a stable non-volatile resistance. Hence R_1 and R_2 are switched using the complementary programming operation. During the first writing operation SET and RESET events are induced on R_2 and R_1, respectively (see Fig.33c) by applying a voltage pulse for 500μs. After reading the resistance values for another 10 cycles, again validating the non-volatility of the resistance states, a second complementary switching operation is performed. Now the resistance states of R_1 and R_2 are complementary switching, as seen in the reading sequence of Fig.34. As can be noticed the resistance values of R_1 and R_2 do not exactly match. This is due to the different ReRAM geometries and to the large variability of the cells utilized for the demonstrator. Nevertheless, improved variability of one order of magnitude has been demonstrated for ReRAM prototypes fabricated with industrial methods [66].

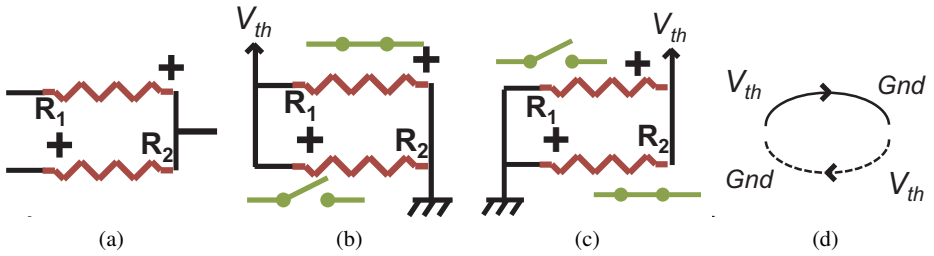


Fig. 33: GMS complementary programming. (a) Two BRS resistive RAMs are in series connected after forming. (b) When V_{th} is applied, R_1 switches ON, while R_2 switches OFF. (c) When $-V_{th}$ is applied, R_1 switches OFF, while R_2 switches ON. (d) Graph representation of the complementary switching operation.

3.2.3 GMS memory node

In this section, we present an elementary circuit used to move most of the configuration part of reprogrammable circuits to the back-end, reducing their impact on front-end occupancy. Such a memory node is dedicated to drive LUT inputs. The memory node is based on a unique GMS node and provides intrinsically the retained information as a voltage level. Furthermore, it shall allow a layout efficient line sharing.

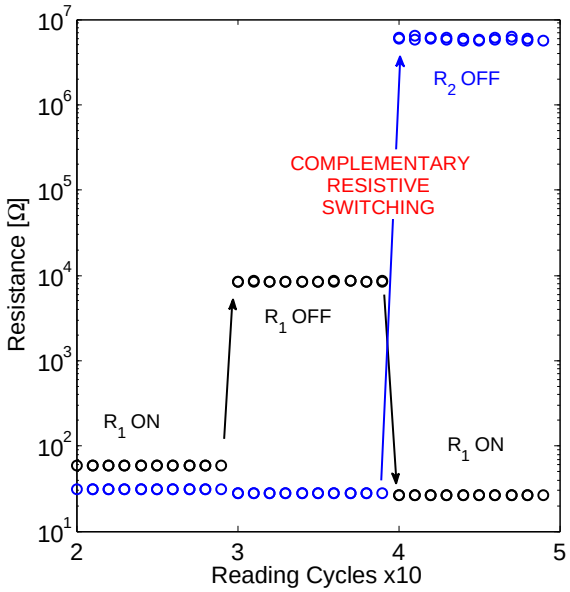


Fig. 34: Complementary switching operation for the ReRAM-based GMS.

3.2.4 Overall Structure

The basic memory node is presented in Fig. 35c . The circuit consists of 2 ReRAMs connected in a voltage divider configuration between 2 fixed voltage lines (L_A and L_B). The memories are used in a complementary manner, in order to improve reliability. Reliability is required as far as the output is not restored by an inverter for compactness purpose. The output is designed to place a fixed voltage on a conventional standard cell input. Read operations are intrinsic with the structure, while programming is an external operation to perform on the cell.

3.2.5 Read operation

A voltage divider is used in this topology to intrinsically realize the conversion from a bit of data stored in the variable resistance to voltage level. Fig. 35b presents a configuration example where the node stores a 1. Voltage lines L_A and L_B are connected to Vss and Vdd, respectively. For example, consider that the resistive memory R_1, connected to the Vdd line, is configured to the low resistivity state. The other memory R_2, connected to Vss, is in the high resistivity state. As a consequence, a voltage divider is configured and the output node is charged close to the voltage of the branch with a high conductivity.

3.2.6 Write Operation

Fig. 35c presents the programming phase of the node. First, the lines L_A and L_B are disconnected from the power lines and connected to the programming signals. The programming signals are chosen according to the GMS programming scheme. Fig. 36 presents the programming circuits required to program an array of GMS-based configuration memories. To provide individual access, each GMS has its own selection transistor. Thus, the different lines can be shared in a standalone-memory-type architecture, yielding an efficient layout strategy. The different modes and programming signals are selected by line-driving multiplexers.

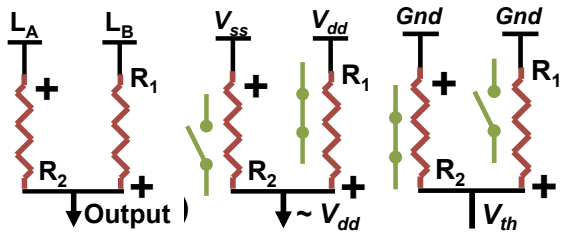


Fig. 35: GMS complementary programming: (a) Two in-series connected BRS RAMs forming a voltage divider between 2 metal lines, L_A, L_B. (b) Voltage distribution to program a logic 1 into the GMS cell. (c) Voltage distribution to program a logic 0 into the GMS cell.

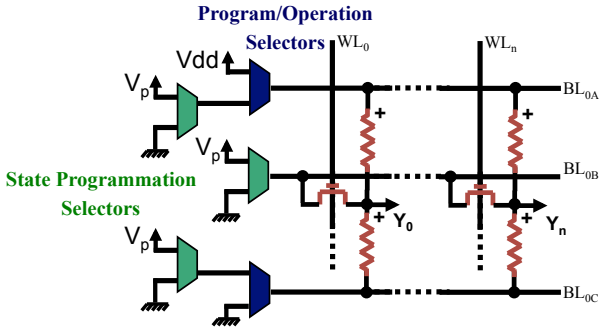


Fig. 36: Complementary switching operation for the ReRAM-based GMS.

3.2.7 Summary

This section introduced a novel design, called GMS, based on resistive memories, designed to replace traditional routing resources in reconfigurable logic circuits. Resistive RAM memories combined into a complementary switching GMS cells were used to reduce the footprint and to improve the electrical performances of the data path. The GMS cell can also be used to replace standalone memories, leading to more compact LUTs and steering logic, due to the BEoL integration of ReRAMs. Thanks to ReRAMs, the area and the delay are reduced by 7% and 58% respectively due to the compactness and the low on-resistance of ReRAMs.

4 Resistive Programmable TSVs

In this section, Back-End-of-the-Line technology for 3D interconnects is addressed, as the interconnect delay is a limiting factor of semiconductor system integration. In this respect, there is a steadily increasing interest in *three-dimensional (3D)* wafer/chip stacking solutions utilizing *Through Silicon Vias (TSVs)* [1] as well as in reconfigurable interconnect fabrics. The discussed BEoL demonstrate the co-integration of TSVs with ReRAM stacks, offering a new path for re-programmable 3D chip routing. Moreover, the authors report on several device schemes that show different write/erase voltage windows, suggesting a new way for programmable 3D chip interconnects. the fabrication and characterization of titanium dioxide (TiO_2)-based *resistive RAM (ReRAM)* co-integration with 380 μm-height Cu *Through Silicon Via (TSV)* arrays for programmable 3D interconnects is discussed. Non-volatile resistive switching of $Pt/TiO_2/Pt$ thin films are first characterized with resistance ratio up to 5 orders of magnitude. Then co-integration of $Pt/TiO_2/Pt$ or Pt/TiO_2 memory cells on 140 μm and 60 μm diameter Cu TSV are fabricated. Repeatable non-volatile bipolar switching of the ReRAM cells are demonstrated for different structures.

4.1 Fabrication

4.1.1 Planar ReRAM devices

First, high resistivity p-type ($N_A \approx 10^{15} atoms/cm^2$) bulk-Si wafers are prepared by 500 nm thermal oxidation in H_2O atmosphere. Then the deposition of the resistive switching materials is performed by sputtering of $Pt/TiO_2/Pt$ layers with 270 nm/80 nm/270 nm thicknesses. A conceptual picture is shown in Figure 37a. The top electrode area of 100 μm by 100 μm squares were patterned by standard lithography and etched by ion milling technique. The etching step reveal the bottom Pt electrode, which can be now accessed for electrical measurements.

4.1.2 TSV devices

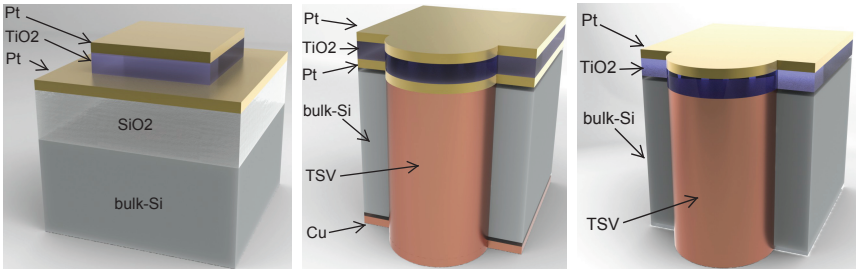
The resistive switching materials were integrated with TSVs producing two different devices:

- 140 μm TSV diameter in 380 μm thick wafer, using $Pt/TiO_2/Pt$ memory stack
- 60 μm TSV diameter in 380 μm thick wafer, using $Cu/TiO_2/Pt$ memory stack. The relatively thin wafer is needed due to TSV aspect ratio limitation.

The TSVs are fabricated using the same process in both cases. A standard optical lithography is used to define the TSV openings. The lithographic step is followed by through wafer etch, RCA wafer cleaning and thermal oxidation in water atmosphere to grow a 3 μm thick oxide. A 750 nm thick Cu layer is sputtered on the backside of the wafer and the TSVs are filled using Cu electroplating. At this step the seed layer remains on the back of the wafer and the TSV create a positive topography on the front side.

4.1.3 TSV with $Pt/TiO_2/Pt$ ReRAM

For the first type of devices, once the TSVs are fabricated the front side of the wafer is processed with *Chemical Mechanical Polishing (CMP)* technique to form a flat surface. The $Pt/TiO_2/Pt$ stack is sputtered with layer thicknesses 270 nm/80 nm/270 nm accordingly. A concept picture of the fabricated structure can be seen in Figure 37b.

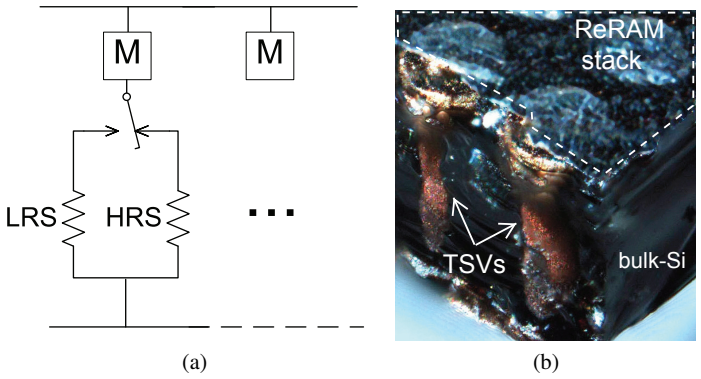


(a) (b) (c)

Fig. 37: (a) Concept image of planar ReRAM made of $Pt/TiO_2/Pt$ stack. (b) Concept image of the ReRAM-TSV using $Pt/TiO_2/Pt$ programmable fuse. (c) Concept image of the ReRAM-TSV using $Cu/TiO_2/Pt$ programmable fuse.

4.1.4 TSV with $Cu/TiO_2/Pt$ ReRAM

For the second type of devices the wafer is polished using CMP on both sides to remove the seed layer and to planarize the surfaces. The Cu was then cleaned using a $NH_4 : H_2SO_4$ etching solution at room temperature for 10 minutes. Then the wafer was loaded into a vacuumed sputtering chamber and a TiO_2/Pt layer was deposited with thicknesses of 80 nm and 270 nm respectively. The Cu of the TSV is acting as the bottom electrode of the ReRAM (see Figure 37c). Equivalent electrical schematics and the photograph of the devices in a cleaved substrate are shown in Figure 38a and 38b, respectively.



(a) (b)

Fig. 38: (a) Equivalent electrical schematic of the TSV with ReRAM memory elements (denoted by the switch and the "ideal" memory element M). (b) Reconstructed 3D photograph of the TSV $-$ $Cu/TiO_2/Pt$ device stack. The die is cleaved to reveal the TSV and the ReRAM stack deposited on top.

4.2 Electrical Characterization

Electrical measurements were carried out with an HP4156A semiconductor parameter analyzer and cascade probe station in dark conditions. For electrical contacts, standard tungsten needles with 15 μm apex diameter were placed on the top electrode area very softly, since a dependence of the switching with needle pressure has been observed, similarly to the observation of local pressure modulated conductance with AFM tips [21]. Then double $I-V$ DC sweeps have been used to investigate the resistive switching behavior. In all the cases, bipolar switching mechanism with different write/erase window and resistance states has been observed. The measured electrical parameters are summarized in Table 1.

4.2.1 Planar ReRAM devices

First the planar $Pt/TiO_2/Pt$ are characterized and it showed stable and repeatable bipolar switching behavior between 10 Ω and 1 MΩ read or measured at $+1$ V (see Figure 39a). Originally the devices are in the high resistance state (HRS). By sweeping from negative to positive voltages the devices hold the HRS until a SET transition to a low resistance state (LRS) occurs at $+1.8$ V. After the SET event, the voltage sweep continues until $+2$ V and then move backward toward negative voltage region. When -1.3 V is reached, the device is RESET to the original HRS state. An HRS to LRS ratio of about 5 orders of magnitude is read at $+0.5$ V.

4.2.2 $TSV-Pt/TiO_2/Pt$ devices

Next, $TSV-Pt/TiO_2/Pt$ with the same layer thicknesses are measured, showing resistance switching below $\pm$ 1V (see Figure 39b). This voltage reduction is attributed to a larger surface roughness of the films deposited on the TSVs, which would lead to a denser electric field at the hillocks as well as to surface states acting as dopants for the TiO_2 [67]. Similar to the planar ReRAM case, the devices are originally in the HRS, and bipolar resistive switching is obtained. Nevertheless, the SET condition is found to be only $+0.6$ V, while the RESET voltage is measured at -0.5 V. Using a reading voltage of $+0.2$ V, an HRS of 2 MΩ and a LRS of 666 Ω, with resistance ratio of 3000 are measured.

4.2.3 $TSV-Cu/TiO_2/Pt$ devices

Since the programming voltages also depend on the current density that can flow into the switching element, a different approach that limits the current flux is investigated. As the electrode material influences the Schottky barrier contact with the TiO_2 layer [68, 69], that is a n-type semiconductor, an alternative device is obtained by depositing TiO_2 and Pt directly on top of the $Cu-TSV$. Thus, thanks to a larger Schottky barrier height at the $Cu-TiO_2$ interface, a larger programming window is obtained (Figure 39c). The SET and RESET voltage positions are now reversed with respect to the other devices, as the Cu has been used as the top electrode. A HRS of 500 MΩ and LRS of 5 kΩ are read at $+1$ V.

Device	V_{SET}	V_{RESET}	HRS	LRS	R_{RATIO}	V_{READ}
Planar $Pt/TiO_2/Pt$	$+1.8$ V	-1.3 V	10 MΩ	10 Ω	10^5	$+1$ V
$TSV-Pt/TiO_2/Pt$	$+0.6$ V	-0.5 V	2 MΩ	666 Ω	3003	$+0.2$ V
$TSV-Cu/TiO_2/Pt$	-4.2 V	$+5$ V	500 MΩ	5 Ω	10^5	$+1$ V

Table 1: Obtained ReRAM electrical parameters for the different devices

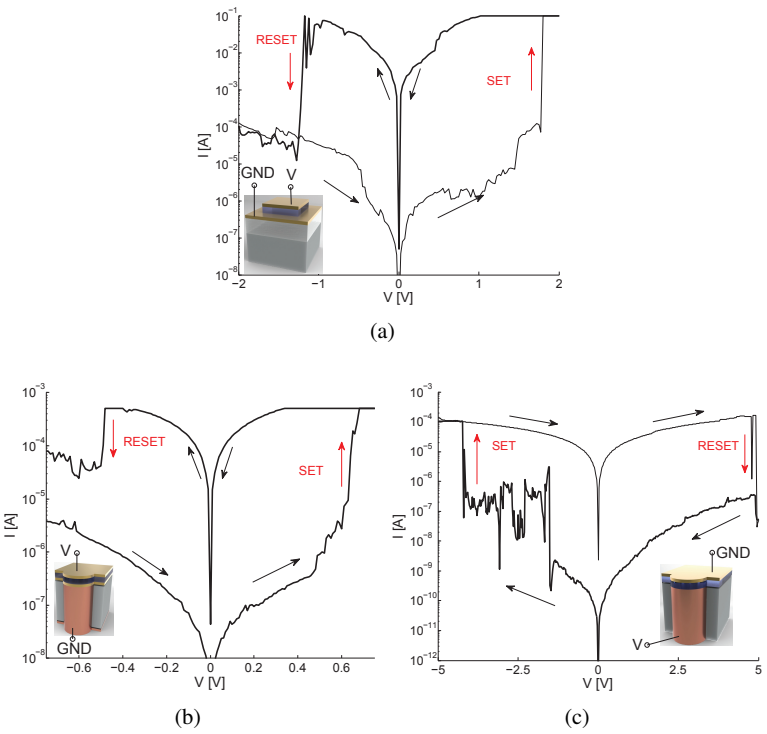


Fig. 39: (a) Resistive switching through $I-V$ sweeps for planar $Pt/TiO_2/Pt$. (b) Resistive switching through $I-V$ sweeps using $TSV-Pt/TiO_2/Pt$ programmable fuse. (c) Resistive switching through $I-V$ sweeps using $TSV-Cu/TiO_2/Pt$ programmable fuse.

4.3 Summary

In this study, $Pt/TiO_2/Pt$ obtained by standard sputtering techniques on oxidized Si wafers showed stable bipolar resistive switching without the need of a forming step and with LRS to HRS resistance ratio up to 5 orders of magnitude. The device is successfully integrated on top of 140 μm and 60 μm TSV arrays either in the full $Pt/TiO_2/Pt$ stack or using the Cu as the top electrode, demonstrating different write/erase voltage windows. The co-integration of ReRAM stacks with TSVs is envisaged as a new and compact solution for programmable/reconfigurable 3D chip interconnects.

5 Applications of multi-terminal memristive devices

Multi-terminal memristive devices can be exploited by their additional functionality. For instance, the amplification of the filament formation in the atomic switch [40] is used to improve writing time and to reduce power consumption during switching phases. Recently, the authors demonstrated the use of three-terminal memristive Si nanowires for bio-molecule detection in dry environment [38]. More specifically, in [38] the third terminal is represented by an organic functionalization layer that wraps the Si nanowire all-around. Another example can be the use of a four-terminal GAA SB Si nanowire FETs for low current and temperature sensing, as demonstrated by the authors [55]. Regarding logic/memory applications, the integration of a three-terminal memristive device realized with Schottky-barrier polysilicon nanowire FETs demonstrated the concept of using this devices for new logic families and hybrid logic/memory gates [53]. For instance in [53], the three-terminal configuration can be used to compute basic digital functions, such as NAND, NOR and flip-flop by using a precharge-evaluation phase scheme. Another application for the three-terminal SB polysilicon nanowire transistors can be the design of a circuit cell reproducing an hysteretical negative differential resistance [54]. In thin-polysilicon grain SB FETs, the hysteresis can arise from the granularity of the channel. In Section 2.4, it is shown that a similar hysteresis can also be obtained independently on the phase state of the Si nanowire channel. Similarly, the same structure can exploit the functionality of an additional gate to tune the polarity of a SB SiNW FET, thus giving even more functionality (as discussed in Section 2.4). A very high expressive power architecture can be made of four-terminal memristive devices arranged in a crossbar implementation that exploits the high-density of the SiNW arrays.

5.1 Neuromorphic circuits

The non-volatile property of the two-terminal memristive devices has a tremendous potential for neuromorphic circuits, in particular forming artificial synapses following the Hebbian rule of learning based on *Spike-Rate Dependent Plasticity (SRDP)* as well as new building elements for hybrid CMOS/memristor circuits. For instance, when considering the perceptron model of the neuron (see Fig. 40), the weighted connections of the inputs to the summation element can be modeled with the properties of non-volatile memristive devices.

With this respect, the Hudgkin-Huxley model, can be mathematically described by first order differential equations. More specifically, Chua and Kang demonstrated that the H-H model of the potassium channel can be identifyied as a first-order time invariant voltage-controlled memristive one-port and that the sodium channel can be described as a second-order time invariant voltage-controlled memristive one-port. Since this representation is compatible with the mathematical representation of memristive devices, it is noteworthy to notice that memristive devices based cir-

cuits can be built to emulate the behavior of biological systems, in this particular case emulating the potassium and sodium channels of the neurons. One example is an energy-efficient memristor-based integrate and fire neuron circuit which exploit the bistability of a ReRAM to model both the short time spike event and the refractory period [70]. Another example is the use of the analog programmability of the ReRAM devices that can be used to emulate the weighted connections of the perceptron model.

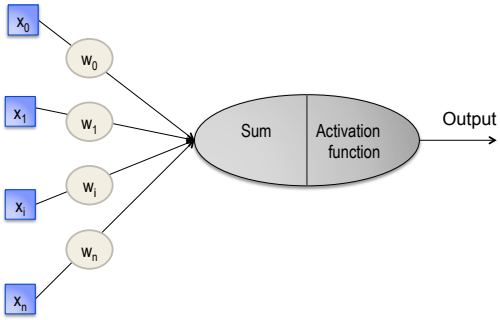


Fig. 40: Perceptron model of a neuron. Input signals x_i are weighted by programming each weight w_i and then summed. The output signal will be an activation function that depends on the summation.

5.2 Current and temperature sensor

This section reports on the fabrication and characterization of a pA current and temperature sensing device with ultra-low power consumption based on a Schottky barrier silicon nanowire transistor. Thermionic and trap-assisted tunneling current conduction mechanisms are identified and discussed on the base of the device sensitivity upon current and temperature biasing. In particular, very low current sensing properties are confirmed also with previously reported polysilicon-channel nanowire Schottky barrier transistors. demonstrating that these devices are suitable for temperature and current sensing applications. Moreover, the process flow compatibility for both sensing and logic applications makes these devices suitable for heterogeneous integration. A range of device operation conditions are investigated, showing how an ambipolar device can be used for different applications, the only requirement being the biasing condition.

The $I_{ds} - V_{gs}$ dependence with T is mainly attributed to the I_{th}, however T also influences the Itunnel since hotter carriers pass through a narrower Schottky barrier, leading to an increasing current level [51]. The I_{OFF} current is increasing exponentially with temperature and its main contribution is a thermionic emission

component. A different behavior has been observed for the I_{ON} current. Increasing the temperature makes the I_{ON} current to decrease until the temperature reaches 55°C and then it rise exponentially with linear increase of T. At lower temperatures tunneling and trap-assisted tunneling are more important than thermionic emission. Rising T up to 70°C makes the charges trapped into the gate oxide to un-trap, reducing the Itunnel component. A different behavior is observed for the I_{ON} currents for $70°C \leq T \leq 115°C$. In this range, the I_{ON} exponentially increases with T. This effect is evidence of two main current components, for which the I_{ON} changes from a tunneling to a thermionic emission dominated regime. A set of $I_{ds} - V_{gs}$ curves (Fig. 41a) taken at different temperatures at constant $V_{ds} = 100mV$ and $V_{bg} = 5V$ are used to extrapolate the Arrhenius plot (Fig. 41c). The constant $V_{bg} = 5V$ is used to set the device operation more favorable for electron conductance at low Vgs. Constant subthreshold swings$\approx 110mV/dec$ are observed independently from the temperature (see Fig. 41b). Low negative V_{gs} voltages ranging from -1V to 0V show an almost linear slope with inverse of temperature and can be correlated to a thermionic-emission regime. However, for this V_{gs} range the current level is on the order of fAs, which is comparable to the background noise, and it cannot be used to extrapolate the Schottky barrier height. Another distinct regime is observed for$-0.3V \leq V_{gs} \leq -0.5V$, for which the slopes are greatly affected by tunneling. This regime shows a dominant tunneling component for the two lowest temperatures. Finally, an exponential dependence with T is observed again for $V_{gs} \geq 0V$ with the exception of the lower temperature. All these regimes demonstrate that the current in our device is mainly thermionic for $\geq 70°C$ and that the tunneling contribution is trap assisted. The slopes from the Arrhenius plot are then used to extract the effective Schottky barrier height ϕ_{Beff} with the activation energy E_a method. As shown in inset A of Fig. 41d, an average effective barrier height $E_a \approx 450 \pm 5meV$ is found over a large range of $V_{gs} \geq 0.2V$. However, these values cannot be taken as Schottky barrier height since in this regime the device has both tunneling and thermionic components. As suggested by Svensson et al. [71], a better evaluation of the Schottky barrier height can be taken at the maximum of Ea for low current levels. As shown in the inset B of Fig. 41d, this maximum corresponds to $V_{gs} = -0.45V$ and gives a $\phi_{Beff} = 525meV$, confirming the mid-gap Schottky barrier height.

5.2.1 Current sensing

Current biasing the devices with a constant Ids current makes the device to behave as a pseudo-inverter configuration with hysteretic transfer function. Thanks to the ambipolarity, the Vout-Vin curves shift linearly with the applied current bias. For instance in Fig. 42a, low pA current levels can be either read from the high-to-low or the low-to-high transition voltage with sensitivities of 17 mV/pA. A similar biasing scheme for polysilicon nanowires has been previously characterized by the authors show a similar trend. In Fig. 42b, forward and reverse threshold voltages for currents between 100 fA and 500 fA show a linear increase with current (adapted from [72]).

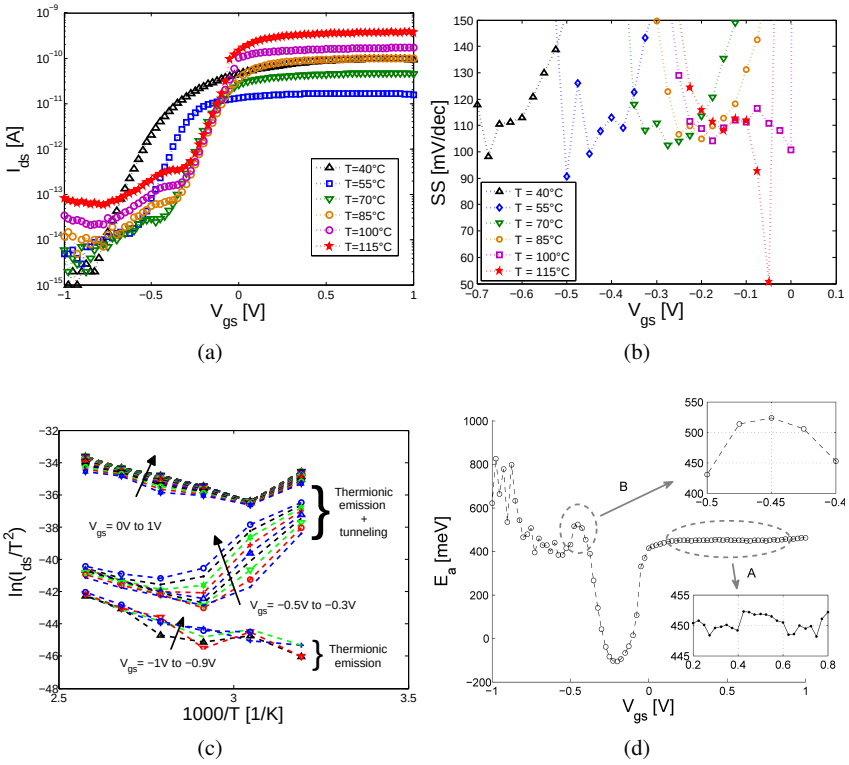
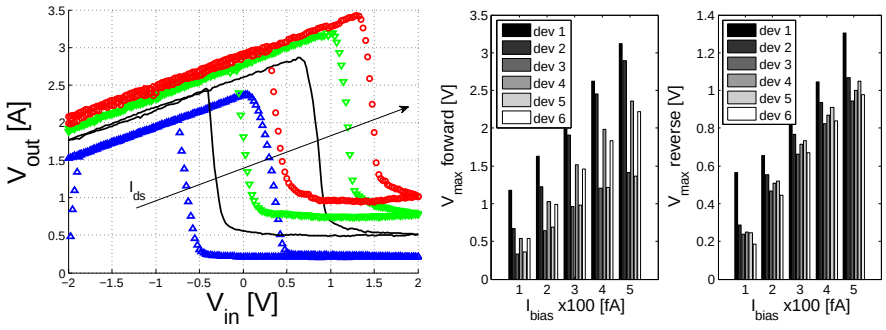


Fig. 41: (a) Effect of the temperature on the $I_{ds}-V_{gs}$ at $V_{ds}=100$mV (b) Subthreshold swings associated with the $I_{ds}-V_{gs}$. Very low swing minima are measured at 100°C and 115°C close to threshold voltages. Notice the voltage shift with temperature increase and the extremely low minima of 40mV/dec for the highest temperature. (c) Arrhenius plot for different V_{gs} values showing both thermionic emission and tunneling mechanisms. The linear decreasing slopes are associated with thermionic emission regimes. (d) Extracted E_a over a large range of V_{gs}. Inset A shows constant $E_a \approx 450 \pm 5$meV. Inset B shows a maximum at 525meV which is taken as the value of the effective Schottky barrier height.

5.2.2 Temperature sensing

Another application is temperature sensing. Upon application of increasing temperature of operation, the hysteresis window observed in pseudo-inverter biasing scheme shrinks. The crystalline Si nanowire Schottky barrier FET shows different sensitivities at different temperature regimes, depending on which mechanism dominates the conductance. Since the hysteresis is attributed to the storage of charges in either gate oxide and/or at the Schottky barrier junctions [49], an increased hysteresis window is expected for the lowest temperatures. The highest sensitivity of



(a) (b)

Fig. 42: (a) Measured input-output transfer characteristics of a hysteretic inverter based on a single Si nanowire FET with low current bias, showing current-dependent thresholds. (b) Forward and reverse threshold voltages for polysilicon Schottky barrier FETs under constant current biasing from 100 fA up to 500 fA (adapted from ref. [72]).

40mV/°C is found in the T range around 40°C at which the trap tunneling mechanisms dominates. For temperatures higher than 55°C the sensitivity tends to saturate according to the dominance of thermionic current contribution, leading to lower sensitivity of 10mV/°C. In Fig. 43 the hysteresis window shrinks for increasing T when $70°C \leq T \leq 100°C$.

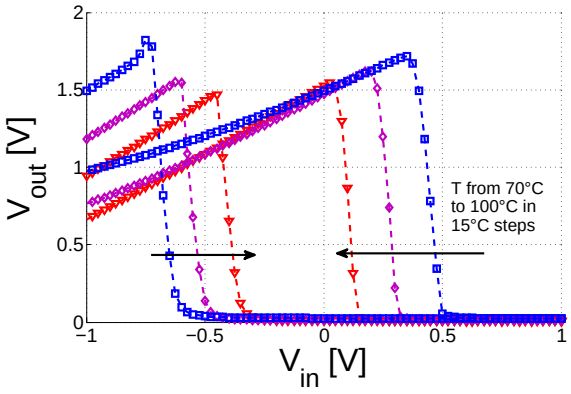


Fig. 43: The hysteresis window shrinks with increasing temperature. Within this T range, the temperature sensitivity of 10mV/°C is related with the thermionic current regime.

6 Conclusions

A general overview on multi-terminal memristive devices is reported. The functionality of the devices can be used for logic, memory and sensing applications. Ultra-dense memristive ReRAMs crossbar arrays can be used for ultra-dense non-volatile memory storage. It was shown that three- and four-terminal memristive devices can be used for both logic and memory applications. In particular, Schottky-barrier silicon nanowire FETs are very interesting devices due to their CMOS-compatibility and ease of fabrication. Disruptive applications exploiting the high expressive power of four-terminal memristive devices arranged in crossbar arrays are foreseen as a significant advance in the electronic computation.

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