FO-transmission of a 1 PPS signal

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31st July 2013 (`Revision: 10720`)

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1 General description

1.1 Purpose

At BFO we synchronize seismic data acquisition systems to a 1 PPS (pulse per second) signal generated by GPS disciplined clocks (Meinberg GPS 166 and GPS 167). While the clocks are operated in the laboratory building, the 1 PPS signal must be distributed to the instruments in the mine. We use optical fibres (FO) to transmit the signal over distances of several hundred meters.

The circuits described below are used to convert the TTL level 1 PPS signal to an FO signal. And they are used to serve mutiple FOs from one single input signal. A distributor (sec. 2.1) is installed in the electronics vault in the mine. This circuit receives the 1 PPS signal through one FO input and feeds six FO outputs. Finally the optical signal is converted to TTL, RS 422, or RS 232 near the data acquisition system (secs. 2.2 and 2.3).

1.2 FO Signal converters

We use FO converters provided by ratioplast[1]. The transmitting diode 905SE850ST1Z1 produces a wavelength of 850 nm and is attached to the optical fibre through ST connectors. The parameters for the transmitter are provided in Tab. 16. Its I/V characteristic curve is displayed in Fig. 8a.

On the receiving side we use the 905EM850ST1Z2 with open collecter inverted TTL output. Its parameters are listed in Tab. 17. The results of a sensitivity-test is shown in Fig. 8b.

1.3 FO Signal polarity

The FO signal polarity with respect to TTL polarity is defined due to the 905EM850ST1Z2 FO receiver. The logic levels are provided by Tabs. 1 and 9. At high level the FO light is switched off and vice versa. TTL+ outputs have a positive logic, while TTL- outputs have negative (inverted logic). TTL inputs are always positive as well as FO inputs and outputs. When driving the TTL input from the Meinberg GPS167 the systems must synchronize on the rising edge of TTL+ and RS232- outputs and on the falling edge of TTL- and RS232+ outputs. Voltage levels of available output signals are discussed in sec. 2.3. Further comments on polarity conventions of clock systems and 1 PPS signal clients at BFO are given in sec. 4.1.

Logic level	FO light	Voltage level
High	off	TLL high: $> 2\,\mathrm{V}$
Low	on	TLL low: $< 0.8\,\mathrm{V}$

Table 1: Definition of signal levels in all circuits described in this document. At high level the FO light is switched off. Notice that polarity at the consumer side can be different.

1.4 LED indicators

Control LEDs in the distributor (sec. 2.1) and the receiver (sec. 2.2) will be bright when the FO is dark. A bright control LED is thus identical with a logic high level. Table 2

[1] http://www.ratioplast.com/opto/docs/efs_news.htm

summarizes possible states of the system indicated by the crontrol LEDs.

LED state	possible reason
blinking	circuit operates well: the 1 PPS signal is indicated
bright	no FO signal is received: FO is dark or FO receiver is defective
dark	general failure: LED is defective or power supply is missing or input is permanently high

Table 2: States indicated by the control LEDs.

2 Circuit description

2.1 Distributor

The purpose of the 1 PPS distributor is to receive a 1 PPS signal from one source either through an optical fibre (FO) or as a TTL signal and to provide this signal to several clients at once either through an optical fibre (FO) or as a TTL signal. It comprises four modules:

FO: The FO diode (transmitter) module, possibly with several diodes in series (part list in Tab. 14).

CCS: A constant current source that drives the transmitter (part list in Tab. 11).

SC: A high-speed switching circuit (part list in Tab. 13).

SIOC: A signal input and TTL output circuit (part list in Tab. 15).

The circuit diagram is displayed in Fig. 9.

Circuit description starts at it (FO) output and proceeds to the input (SIOC): The transmitting diodes (FO, Tab.16) are driven by a constant current source (CCS, Fig. 9). The constant current source is adjusted to provide the maximum drive current of 100 mA. The current is sensed through the voltage drop across R3. The resistor R3 must thus be selected to have the exact resistance of 20 Ω when setting the voltage at TP1 to 2 V (see sec. 3.2). To drive several transmitting diodes at once, they may be placed in series as shown for the FO diode module in Fig. 9. If the total forward voltage drop becomes too large, which will happen for $N > 3$ at a supply voltage of 13 V, more than one FO diode module must be used. Each FO diode module must be connected to its own constant current module via connection B. In fact the single constant current source module (CCS) is provided with a layout for two identical constant current sources (Fig. 10). Connection C of the switching circuit module (SC) in Fig. 9 may be connected to connection C of several FO diode modules, since they are decoupled by D5. The series resistor R9 is used to provide a faint biasing for the FO diodes to reduce switch-on time delays. However, if too many FO modules are used in parallel with one switching module, the performance of the switching module can deteriorate.

Fast switching of the transmitters is accomplished by by-passing the drive current through transistor T3 of the high-speed switching module. By keeping the current through T1 and R3 constant the slew rate and the transition frequency of T1 will not limit the switching speed. High-speed switching transistors T2 and T3 together with speed-up capacitors C6 and C7 and the Shottky diodes D2 and D3 (Horowitz and Hill, 1989, sec 13.23, so-called Baker clamps) control the switching performance. The circuit performance is discussed in sec. 3.4.

The input signal can be provided by FO via IC4 or by TTL from connection E to IC5 in the signal input and TTL output circuit (SIOC). Connect only one of them to the input of the next stage. Optional connections to be used alternatively are shown by dashed lines in Figs. 9 and 10. Connection D provides the input signal to the fast switching module (SC).

The signal input and TTL output module (SIOC) provides auxilliary TTL outputs (direct and inverted). While the circuit diagram (Fig. 9) shows only two of each of them, the board layout is prepared for three each (Fig. 10). If desired external pull-up resistors to a higher voltage can be used at the outputs. The board layout is also prepared to drive an LED display which is not shown in the circuit diagram. A luminescent LED indicates that the FO light is of and that the logic level is high. In normal operation the LED should be blinking synchronously with the 1 PPS signal. If the LED is permanently off, this might indicate at problem with the electronics. If the LED is permanently on, this could indicate problems with the FO signal reception. See also Tab. 1 and section 1.4.

Alternatively to the SIOC in Fig. 10 and Fig. 9 the multifunctional receiver circuits in Fig. 20 or Fig. 23 should be used if the focus is on voltage level outputs. The circuits are described in sec. 2.3. They are more flexibel than the solution in Fig. 10.

The pure wiring diagram is displayed in Fig. 15 and the part placement is available from Fig. 16. A photograph of the prototype board is displayed in Fig. 11 and the corresponding FO diode board for six FO output is shown in Fig. 12.

2.2 Receiver

A single receiver is used to convert the FO 1 PPS signal to TTL or RS 232 signal levels near the data acquisition system. While the 905EM850ST1Z2 directly provides TTL compatible signal levels, we have supplemented the circuit with a TTL buffer IC and the MAX 232 circuit to generate RS 232 signal levels as required by the Quanterra Q330 data acquisition systems. For this circuit only the board layout is provided by Fig. 17.

The pure wiring diagram is displayed in Fig. 18 and the part placement is available from Fig. 19.

The simple receiver module has been superseded by the multifunctional receiver with RS-422 output (sec. 2.3.6). See sec. 4.1.3 for the standard layout at BFO.

2.3 Multifunctional receiver

In Fig. 20 and Fig. 23 the layout for alternatives to the simple signal receiver circuit and to the signal input and TTL output module (SIOC, part of the 1 PPS signal distributor) are displayed. These circuits essentially contain the same circuit groups as those mentioned previously. However, they are more flexibel in terms of output signal characteristics and the possibility to omit parts of the circuit that are not required in an application. The circuit consists of six modules. Only

- the 5V power supply,
- the 1 PPS signal input,
- and the TTL output a

are mandatory. For the TTL output modules and the TTL high voltage open collector output all chips listed in Tab. 24 are appropriate. However, TTL output modules a and b do not provide pull-up resistors for open collector outputs. In the BFO standard layout (sec. 4.1.3) IC3 is populated with a SN74LS04 inverting buffer with totem pole output.

The pure wiring diagram is displayed in Fig. 21 and the part placement is available from Fig. 22. The RS-422 variant is provided in Fig. 24 and Fig. 25, respectively.

2.3.1 Power supply

The module takes 12 V as input and provides 5 V power supply to the TTL circuitry. A parts list is provided in Tab. 18.

2.3.2 1 PPS signal input

This module provides an FO and a TTL logic level input (pin E) alternatively. Connections to IC3 must be made appropriately (dashed green wire). A parts list is provided in Tab. 19.

2.3.3 TTL output a and b

Both modules are connected in parallel to the input. TTL output b is fully optional and may be discarded. The input (or IC2) must drive up to 12 buffers. TTL typically has a fanout of 10. If you want to use all possible buffers be careful. Possibly use a buffer from IC3 to drive IC4. Or disconnect some of the buffer inputs if your fanout is insufficient. Inputs of unused buffers should be connected to GND or +5V. Any of the chips listed in Tab. 24 can be used for IC3 and IC4. However, notice that these modules do not provide pull-up resitors. The totem pole output type should be preferred for this reason. Each of the buffers provides a series resistor to drive an LED on one of the outputs. Connect the cathode to pins LED1 or LED2 and the anode to +5V. A parts list is provided in Tab. 20. Since non-inverting circuits are only available in their open-collector form, it can be appropriate to operate IC3 and IC4 in series with inverting totem pole output devices like the SN7404 or SN74LS04. By connecting two of them in series, TTL signals of both logical polarity are provided. Fig. 21 shows both alternative wirings. TTL voltage levels are given in Tab. 3 (Horowitz and Hill, 1989, sec. 8.02).

signal	logic level	voltage
TTL	high	$< +0.8\,\mathrm{V}$
TTL	low	$> +2.0\,\mathrm{V}$

Table 3: TTL voltage levels.

2.3.4 TTL high voltage open collector output

This module can switch larger currents from higher voltages than TTL voltage levels. This module is fully optional. If required it can be connected to the same supply rail as the TTL output modules. Open collector outputs are provided by IC5 and and such chip may be selected from Tab. 24. SN74LS06, SN7406, SN74LS07, or SN7407 are recommended here. The outputs are provided with pull-up resistors. The diodes are used to decouple higher switching voltages from the +5V supply line. Inputs I1 to I6 have to bo connected to one of the outputs Oa1 to Oa5 or Ob1 to Ob5 each. Input I1 controls output Oc1, input I2 controls output Oc2, and so on. Unused inputs should be connected to GND or +5V. A parts list is provided in Tab. 21.

2.3.5 TTL to RS-232 level converter

This module provides voltage level conversion. IC6 is used to drive an RS-232 level output from a TTL level input. TTLa input controls 232a output and TTLb input controls 232b output. This module is fully optional. If required it can be connected to the same supply rail as the TTL output modules. The input signals should be obtained from one of the outputs of the TTL output module. Unused inputs should be connected to GND or +5V. A parts list is provided in Tab. 22. Notice that RS-232 voltages have reverse polarity (Horowitz and Hill, 1989, sec. 10.19) when compared to TTL. A TTL rising edge is converted to an RS-232 falling edge. The MAX232 integrated circuit internally inverts the signal. RS-232 voltage levels are given in Tab. 4.

signal	logic level	voltage
RS-232	high	$-5\,\mathrm{V}$ to $-15\,\mathrm{V}$
RS-232	low	$+5\,\mathrm{V}$ to $+15\,\mathrm{V}$

Table 4: RS-232 voltage levels. Notice that RS-232 has reverse polarity.

2.3.6 TTL to RS-422 level converter

This module provides voltage level conversion. IC6 is used to drive an RS-422 level output from a TTL level input. Four channels for level conversion are available. This module is fully optional. Since RS-422 uses differential signals, polarity can easily be inverted by swapping signal wires. If required the module can be connected to the same supply rail as the TTL output modules. The input signals should be obtained from one of the outputs of the TTL output module. Unused inputs should be connected to GND or +5V. A parts list is provided in Tab. 23. The circuit uses an SN75ALS192 quadruple differential line driver. Several other pin-compatible integrated circuits are available on the market for this purpose. The board layout ist displayed in Figs. 23, 24, and 25.

The standard configuration for the multifunctional RS-422 receivers as used at BFO is described in sec. 4.1.3.

RS-422 signal definition: RS-422 is designed for differential voltage signal transmission. It provides a high noise immunity. Transmitter outputs are commonly labelled A and B, where A is positive and B is inverted. Corresponding receiver inputs are labelled A' and B'. Some devices (like the SN75ALS192) replace A by Y and B by Z.

The RS-422 standard is defined by TIA-422. The definition can be obtained from ITU-T recommendation V.11 (International Telecommunication Union, 1996). Signal under different conditions are discussed by Soltero et al. (2010). Both references are at variance with respect to allowed signal voltage levels. The voltage at each of the inputs may be in the range from -6 V to +6 V and the diffrential mode voltage $U_A - U_B$ must not exceed the range from -10 V to +10 V. A differential mode voltage $U_A - U_B > 300\,\text{mV}$ corresponds to high (H) or logic 1, while a differential mode voltage $U_A - U_B < 300\,\text{mV}$ corresponds to low (L) or logic 0. The meaning of differential mode voltages between -300 mV and +300 mV is not specified. RS-422 voltage level as used by the SN75ALS192 are given in Tab. 5 and in Tab. 6.

The differential output voltage ($U_Y - U_Z$) swing between H and L state recorded at the output of an SN75ALS192 is about 7 V without signal termination, 6 V with 130 Ω termination, and about 5.5 V with 100 Ω termination. Termination resistors are placed beween Y and Z outputs.

RS-422 cable recommendations: Recommendations for appropriate cabling are given by Hess and Goldie (1993, Tab. 3), Wilson (2000), Abbot and Goldie (1993), and Horowitz and Hill (1989, Sec. 9.14). We use a shielded twisted-pair 24 AWG cable. Connections should be terminated. Termination resistors should have about 100 Ω. We use 120 Ω. Wilson (2000, Fig. 7) recommends to add transient surge supressors (TransZorb) for ESD-protection of source and receiver.

signal	logic level	differential mode voltage level
RS-422 (A-B)	high (H)	$U_Y - U_Z = +2\,\text{V}$
RS-422 (A-B)	low (L)	$U_Y - U_Z = -2\,\text{V}$

Table 5: RS-422 voltage levels used by the SN75ALS192.

sig A	sig Y	sig Z	sig A	sig Y	sig Z
			voltage level		
logic level			TTL	RS-422	
H	H	L	> 2 V	2.5 V	0.5 V
L	L	H	< 0.8 V	0.5 V	2.5 V

Table 6: Conversion polarity of SN75ALS192.

3 Technical aspects

3.1 Transmitting diodes in series

The emitter voltage of T1 is set to 2 V. The minimum collector to emitter voltage of T1 in case of saturation is 2.5 V. The drop across D1 will be about 1.1 V. Hence, at an operating voltage of 12 V the total forward voltage drop across all sending diodes D4 should not be larger than 6 V. This limits the number N of diodes in series to $N \leq 3$.

3.2 Calibration of constant current source

To support the use of different voltage regulater ICs for IC1, R18, R19, and Rx19 can be used to adjust the forward current through the transmitting diodes. Notice, that the L78L02 has a nominal output voltage of 2.6 V, while the L78L05 has one of 5.0 V. If U_o ist the output voltage of IC1, than you should choose

$$R_{x19} = \frac{R_{18}}{\frac{U_o}{0.1\,\text{A}\,R_3} - 1} - R_{19} \tag{1}$$

to obtain a forward current of 100 mA. At the same time you should choose $R_{18} + R_{19} + R_{x19}$ appropriatly for a reasonable bias current to load IC1. For a bias current of 10 mA choose

$$R_{x19} = \frac{U_o}{0.01\,\text{A}} - R_{18} - R_{19}. \tag{2}$$

Suggestions for appropriate initial values are given in Tab. 12.

3.3 General considerations

3.3.1 Jitter immunity

Consider a harmonic signal

$$f(t) = A\sin(\omega t) \tag{3}$$

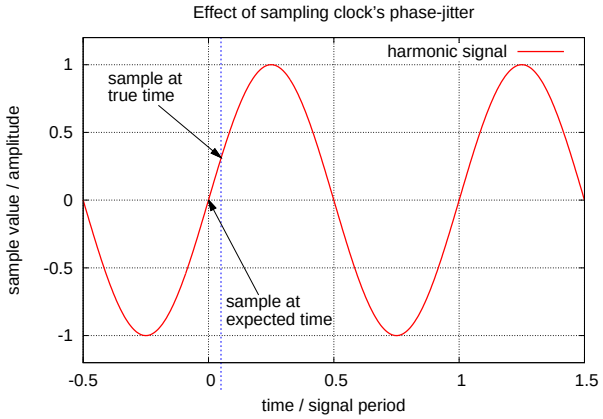

Figure 1: Jitter noise is a result from unstable sampling time.

f_{samp}	f_{Ny}	T_{Ny}	max. Δt
100 Hz	50 Hz	0.02 s	0.32 ns
80 Hz	40 Hz	0.025 s	0.4 ns
1 Hz	0.5 Hz	2 s	32 ns
0.1 Hz	0.05 Hz	20 s	320 ns

Table 7: Maximum 1 PPS jitter allowed for 24 bit data acquisition systems at different sampling rates (eq. 7).

sampled at expected time t. The actually sampled value at sampling time t will be

$$g(t) = A\sin(\omega(t+\Delta t)) \tag{4}$$

due to clock jitter Δt (Fig. 1). The residual signal

$$r(t;\Delta t) = g(t) - f(t) = f(t+\Delta t) - f(t) = 2A\,\sin(\omega\Delta t/2)\,\cos(\omega\,(t+\Delta t/2)) \tag{5}$$

can be understood as noise. The amplitude of residual signal with respect to amplitude of true signal with period T is

$$E(T;\Delta t) = \frac{2A\sin(\omega\Delta t/2)}{A} \approx \omega\Delta t = \frac{2\pi\Delta t}{T}. \tag{6}$$

The worst case is a data signal close to the Nyquist frequency at full amplitude. To ensure that the jitter-noise amplitude is below the LSB in a 24 bit data acquisition system

$$E \overset{!}{<} 10^{-7} \qquad \text{or} \qquad \Delta t \overset{!}{<} 1.6\cdot 10^{-8}\,T_{\mathrm{Ny}} \tag{7}$$

is required (Tab. 7). The jitter produced by DCF77 receivers is too large for standard 24 bit seismic data acquisition systems but can be tolerated for the BFO (HPMO) data acquisition system (Tab. 8).

3.3.2 Prefer RS-323 or RS-422 level signals?

RS-422 appears superior to RS-232 in our applications. The RS-232 signal converters usually require an internal power supply to provide ±12V. This is of limited power and slew-rate usually is low at their outputs resulting in signal propagation delays of more than 1 μs. The delay itself is not critical. However, the low-slew rate together with 50 Hz pickup can modulate the signal thus causing a jitter. RS-422 voltage converters usually are powered from 5 V and have signal propagation delays in the range of 10 ns. Since the Q330HR takes 1 PPS signals also optionally with RS-422 voltage level, we make the transition to RS-422 for all data acquisition systems which not directly take TTL level 1 PPS signals.

Proper use of twisted pair signale cables properly terminated together with the differential mode RS-422 signals provide comparably high noise immunity (sec. 2.3.6).

3.4 Circuit performance

The prototype circuit was tested for its performance. A photograph of the setup is shown in Fig. 14. The board was supplied with 13.8 V and 293 mA (total power consumption, Fig. 13) during the test. Each constant current source (CCS) was calibrated to provide 100 mA or slightly less to an accurancy of 3 mA. A high-frequency TTL test signal was obtained from a laboratory signal generator and provided at input E of the signal input and TTL output module (SIOC).

3.4.1 Signal propagation delay

Fig. 3a displays the signal propagation delays in the SIOC module from the TTL input (E) to the TTL outputs (TTL+ and TTL-). Delay times for rising and falling edges are less than 100 ns. As has to be expected the performance for the falling edge of open collector TTL outputs is slightly better than for the rising edge. For this reason push-pull outputs should be preferred over open collector outputs if this is appropriate for the next stage's input. However, the delays in the circuit are much smaller than the propagation delay over several hundred meter long optical fibres and are not critical in our application.

Figs. 3b and 4 display the signal propagation delays to the TTL output of an external FO receiver. For the rising edge the total delays are less than 200 ns and for the falling edge they are less than 300 ns and thus are not critical in our application. The internal delay to the input of the swichting module (SC) is much smaller (Fig. 3b). The rising edge delay to the FO diode is less than 50 ns. Hence there must be a significant contribution of the receiver 905EM850ST1Z2 to the overall delay times.

In fact the total delay times (Fig. 4) are smaller than for the module DI/2LWT-8-1R/AHS provided by Meinberg which is specified for transmission speed up to 100 kHz and which turns out to have delay times of 3.2 μs and 1.5 μs, respectively.

Compared to time delays observed in DCF77 receivers used at BFO (sec. 4.2.2) the signal propagation delay in the 1 PPS signal distribution system is negligible.

DCF77 carrier frequency:	77.5 kHz (period: 12.9 μs)
PZF509 internal reference frequency:	2.5 MHz (period: 400 ns)
Jitter of 1 PPS signal from Meinberg DCF77 receiver:	400 ns
Required for GRSN data acquisition (24 bit; f_{samp}=80 Hz):	$<$0.4 ns

BFO data acquistion system (20 bit):

f_{samp}	f_{Ny}	T_{Ny}	Δt for $E < 10^{-6}$
0.2 Hz	0.1 Hz	10 s	1.6 μs

Table 8: The Meinberg DCF77 receivers produce a time jitter of 400 ns amplitude (see section 4.2.2). This is too large to the GRSN data acquisition system which would require the jitter to be smaller than 0.4 ns. The BFO (HPMO) data acquisitions system however can safely be operated with a PZF509.

3.4.2 Switching module (SC) performance

Fig. 5 displays the performance of the switching module (SC) on two different time scales. While the overall delay for the rising edge to the module's output C is less than 50 ns and is thus highly satisfactory, the performance for the falling edge appears not optimal. Already the voltage at the collector of T2 (TP6) reveals a larger time constant. This potentially could be improved by reducing the value of R7. But refering to the specifications required in our application the performance is fully satisfactory.

3.4.3 Constant current source (CCS) performance

A by-pass switch is used to avoid large voltage swings of the circuit controlling the constant current source. This is done to avoid the influence of the OpAmp's slew rate or the transition frequency of T1. Fig. 6 displays the performance of the constant current source module on two different time scales. Transients generally are small but reach a level of 10 % for the current observed at TP5 by the voltage drop accross R3. This is due to the compensation capacitor C3 that is required to stabilize the circuit that otherwise would have a tendency for high-frequency oscillations. The current transients are not desirable, since they add inertia to the switching of the FO diodes. They are of the wrong polarity. While a circuit without R1, R2, and C3 would heavily oscillate in response to each edge of the 1 PPS signal, the circuit behaves quite well. The collector of T1 at connection B certainly has a signifcant voltage swing since it must follow the switching cycle.

3.4.4 Supply power performance

The main module (CCS) that contains the large by-pass capacitors for the supply power uses power line wiring in a starlike arrangement to avoid cross-talk due to voltage drops along supply lines. The other modules are supplied through rather thin wires as can be seen in Fig. 11. For this reason supply voltage transients can be observed (Fig. 7) at connection A on the FO board. Even differences between ground levels of different modules may reveal transients. Proper probe grounding in test setups is thus necessary.

4 Time synchronization at BFO

4.1 1 PPS polarity

The relation of TTL signal level to FO state is defined in section 1.3 and Tab. 9. Below a definition of signal polarity is given in terms of the edge to synchronize on with respect to 1 PPS signal sources and data acquisition systems.

4.1.1 Meinberg GPS167

A GPS-disciplined clock manufactured by Meinberg (GPS167) is used as the primary source of 1 PPS for digitizer synchronization. The GPS167 provides an electrical and an optical output.

Electrical output: We use the signal P_SEC at DB9 connector F_SYNTH. The beginning of each second is indicated by a rising TTL edge. The TTL signal remains in the high state for 200 ms (Tab. 25).

Fibre optic output: The polarity of the FO output is selectable by jumpers on the LWL4T board that hosts the FO transmitters. The jumpers at BFO are set such that the beginning of each second is indicated by a falling edge (Tabs. 9 and 26). The falling edge is indicated by a transition from bright to dark FO. The FO remains dark for 200 ms. This polarity matches that of the 1 PPS distributor as defined in Tab. 9 and sec. 1.3.

circuit location		edge to synchronize on
fibre optics	FO	bright to dark
1 PPS distributor TTL	D	rising edge

Table 9: Edges to synchronize on.

4.1.2 1 PPS receiver and distributor

Applying the 1 PPS signal from the clock with polarity described above (sec. 4.1.1), synchronization has to take place on a transition from bright FO to dark FO. Edges to synchronize on are listed in Tab. 9. The distributor (sec. 2.1), the receiver (sec. 2.2), and the multifunctional

receiver (sec. 2.3) all use the same circuitry (SIOC) for converting the FO-signal to a TTL level signal. This circuit is shown in Fig. 9 (bottom).

Internal signal voltage levels: The timing diagrams of signals in the different circuits are given in Tab. 26. The falling edge fibre optics signal is received by IC4 and inverted to a rising edge TTL level signal. Alternatively the TTL level signal is provided from the Meinberg reference clock (sec. 4.1.1) directly through circuit point E and a buffer (1/6 IC5). In both cases the rising edge signal is present at circuit point D. In the case of the distributor, the signal is propagated to the high speed switching circuit (SC, middle of Fig. 9). A TTL high level at point D activates the by-pass for the transmitter current thus turning the rising edge TTL signal into a transition from bright to dark at the FO output. The MAX232 converter (sec. 2.3.5) has to take the signal with the polarity present at point D (rising TTL edge) at its input, in order to provide an RS-232 falling edge (RS-232+ signal) as expected by the Q330HR (sec. 4.1.4, Tab. 27). The RS-422 converter must be driven from a TTL- signal (falling edge) to match the specification in Tab. 26 (sec. 4.1.3).

Output signal voltage levels: The edge polarity of different output signals provided by the multifunctional receivers are defined in Tab. 26. TTL+ and TTL- signals are produced by using inverters and concatenating converters (Tab. 24). In the same way RS-232+ and RS-232- are produced by driving the MAX232 either with a TTL+ or TTL- level signal in the multifunctional receiver. The RS-422 output signal level however always must match the definition given in Tab. 26. If RS-422 signal polarity reversal is required by a client, wire A and B can simply be swapped. The RS-422 signal voltage level polarity is according to the standard wiring used at BFO (next section: sec. 4.1.3).

4.1.3 BFO standard RS-422 multifunctional receiver

Since most clients at BFO take an RS-422 voltage level 1 PPS signal to synchronize, all locations are equipped with an RS-422 multifunctional receiver. The RS-422 multifunctional receiver board (Fig. 23) is populated with 7404 or 74LS04 inverters (Tab. 24) with totem pole output for IC3 and IC4, both. Both ICs are connected in series, by taking the wiring alternative which connects output pin 12 of IC3 to the inputs of IC4. This way the outputs of IC3 provide TTL- level signals, while the outputs of IC4 provide TTL+ signals (Tab. 26). IC6 is the TTL to RS-422 converter. All its TTL inputs are connected to TTL- level signals present at the outputs of IC3 (PD uses red wires).

To match the specification for the LED inidcator as defined in sec. 1.4 the LED1 must be populated. This is the output of the first inverter (IC3 in Fig. 23). The LED is connected with its cathode to the series resistor at pin 2 of IC3 and with its anode to +5 V.

A	B	C	D	E	F
1	8	-out	blue	black	2
1	7	+out	green	red	1
2	6	-out	blue	black	2
2	5	+out	green	red	1
3	4	-out	blue	black	2
3	3	+out	green	red	1
4	2	-out	blue	black	2
4	1	+out	green	red	1

Table 10: 1 PPS wiring in cabinet of the BFO vault's wall installation. A: section on the RS-422 multifunctional receiver board (Fig. 23). B: pin no. of the D-Sub DA15 female socket in the box of the RS-422 multifunctional receiver. C: RS-422 output signal. D: wire color inside box of the RS-422 multifunctional receiver. E: wire color from D-Sub DA15 connector to box of the RS-422 multifunctional receiver to Buccaneer 400 connector inside fixed cabinet on vault's wall. F: pin no. of Buccaneer 400 socket (Fig. 2).

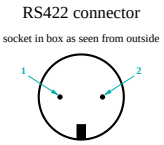

Figure 2: 1 PPS signal connector socket in fixed cabinet on vault's wall. Pin location is displayed as seen from outside the housing. The socket is a female Buccaneer 400 PX0412/02S.

In each vault of the mine a cabinet is bolted to the wall. This cabinet contains a power supply, a LAN switch, and a 1 PPS multifunctional receiver. Signals (LAN and 1 PPS) are received from optical fibres and are converted to voltage signals in the cabinet. For this purpose an RS-422 multifunctional receiver is installed in a box inside the cabinet. The output signals from the RS-422 multifunctional receiver are presented at a D-Sub DA15 female socket. The wiring in the cabinet picks these signals up and presents them on Buccaneer 400 female sockets (Fig. 2) at the outside of the cabinet. The wiring inside the RS-422 multifunctional receiver box and inside the cabinet is given in Tab. 10. Consequently pin 1 of the Buccaneer 400 socket (Fig. 2) in the cabinet provides a falling edge, while pin 2 provides a rising edge RS-422 signal voltage level.

4.1.4 1 PPS clients at BFO

The 1 PPS signal edge polarity as expected by several clients used at BFO are given in the following tables:

Q330: Tab. 27

DAC-3, SG056: Tab. 28

EarthData digitizer: Tab. 29

PDAS-100: Tab. 30

4.1.5 Meinberg PZF509

The PZF509 provides both, rising and falling egde signals. After the transition that indicates the beginning of a second, the signal remains in its new state for 200 ms.

4.1.6 Old EarthData supply box

The old pair of EarthData supply boxes uses an FO transmitter (OSDH 50M2) and an FO receiver (OEDH 50M2) which was produced by Hirschmann and that is no longer on the market. These modules are used in this old system to transmit the 1 PPS signal. **Notice:** The polarity of these modules is non-inverting. Thus supplying an electrical 1 PPS signal to them will produce and FO-signal of opposite polarity compared to the 1 PPS distributor as defined in section 1.3 (Tab. 9).

4.2 Clock performance

4.2.1 DCF77

The DCF77 receivers provide a correction factor for radio wave travel times. For this purpose the receiver must be configured with the correct distance to the DCF77 transmitter at Mainflingen. The distance from BFO to Mainflingen is approximately 195 km. However this apparently does not provide the optimal correction (see next subsection).

4.2.2 GPS167 and PZF509

On June 6th 2008 the optical output of the GPS167 (GPS-receiver) was compared to the TTL output of the PZF509 (DCF77-receiver). Without correction for radio wave travel times in the DCF77 receiver both 1 PPS signals are offset by 760 μs, where the PZF509 is delayed compared to the GPS167's signal. The delay is minimized when setting the PZF509 to a distance of 231 km for the travel-time correction. The clock apparently uses the speed of light in vacuum, which is $3 \cdot 10^8\,\mathrm{m\,s^{-1}}$. This is consistent with the travel-time estimate used for the transmission to Braunschweig by Piester et al. (2004). Using a distance of 200 km for the corrections the PZF509 is delayed by 101 μs. This is at the magnitude of travel-time differences between the ground-coupled wave and the wave reflected by the ionosphere as well as variations of the travel-time of the wave reflected by the ionosphere at 200 km distance to the DCF77 transmitter (Piester et al., 2004, Fig. 15)

The mean time difference between the GPS167 and PZF509 is stable, but sometimes changes abruptly by a few microseconds to be then stable at a new value. At least one of the clocks does not synchronize continuously. The time difference drifts by about 50 ns per second and is abruptly adjusted by a correction of about 400 ns after a few seconds. The variation of the residual with time thus has a sawtooth shape.

According to Werner Meinberg (pers. comm., 2008) these observations are reasonable. His statements are:

1. The GPS167 is more precise than the PZF509 by about a factor of 1000 (one thousand).
2. The influence of the wave reflected by the ionosphere still can be neglected at a distance of 200 km to the DCF77 radio transmitter.
3. Offsets of the PZF509 up to 100 μs can easily be explained by calibration tolerance and the installation of the aerial.
4. The observed drift is that of the TCXO oscillator in the PZF509. It should become smaller after warming up. The size of the correction steps are the period of the internal counter at 2.5 MHz.
5. Due to the much higher carrier frequency the GPS-system can be more precise than the DCF77 system. Further the GPS receiver is able to derive an appropriate travel-time correction himself from the position coordinates obtained from the analysis of the GPS signals.

References

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International Telecommunication Union, 1996. Electrical characteristics for balanced double-current interchange circuits opertaing at data signalling rates up to 10 Mbits/s. ITU-T Recommendation V.11, <http://www.itu.int/rec/T-REC-V.11-199610-I/en>.

Piester D., Hetzel P. and Bauch A., 2004. Zeit- und Normalfrequenzverbreitung mit DCF77. PTB-Mitteilungen, 114(4): 346–368. <http://www.ptb.de/de/org/4/44/442/index.htm.

Soltero M., Zhang J., Cockril C., Zhang K., Kinnaird C. and Kugelstadt T., 2010. RS-422 and RS-485 Standard Overview and System Configurations. Texas Instruments Inc. Application Report SLLA070D.

Teledyne Geotech, 1989. PDAS User's Guide. Garland, Texas, USA.

Wilson M.R., 2000. TIA/EIA-422-B Overview. National Semiconductor Corporation. Application Note 1031.

Part #	Parameters
IC1	L78L05
IC2	LM358N
T1	BD675 (provide a heat sink!)
D1	1N4001
C1	1 μF ceramic multilayer
C2	220 nF ceramic multilayer
C3	100 pF
C4	470 μF electrolyte
C5	1 μF ceramic multilayer
R1	2.2 kΩ
R2	10 kΩ
R3	20 Ω, 1 W
R18	330 Ω
R19	220 Ω
Rx19	0 Ω

Table 11: 1 PPS distributor: Parts for the constant current source module.

IC1	R3	R18	R19	Rx19
L78L05	20 Ω	300 Ω	200 Ω	0 Ω
L78L05	20 Ω	270 Ω	180 Ω	0 Ω
L78L05	20 Ω	330 Ω	220 Ω	0 Ω
L78L02	20 Ω	60 Ω	200 Ω	0 Ω
L78L02	20 Ω	56 Ω	180 Ω	4.7 Ω
L78L02	20 Ω	68 Ω	220 Ω	10 Ω

Table 12: 1 PPS distributor: Calibration of constant current source module. See section 3.2.

Part #	Parameters
T2	2N2219A
T3	2N2905
D2	BAT43
D3	BAT43
C6	100 pF
C7	50 pF
C8	1 μF ceramic multilayer
R4	560 Ω
R5	35 kΩ
R6	1 kΩ
R7	3.6 kΩ
R8	3.3 kΩ

Table 13: 1 PPS distributor: Parts for the high-speed by-pass switching module.

Part #	Parameters
D4	905SE850ST1Z1
D5	1N4148
R9	$(N\,1\,\mathrm{V} - 2\,\mathrm{V})/100\,\mathrm{mA}$, where N is the number of diodes D4 to be used; use 10 Ω 1 W in the case of $N = 3$

Table 14: 1 PPS distributor: Parts for the FO diode module.

Part #	Parameters
IC3	MC7805CT (provide a heat sink!)
IC4	905EM850ST1Z2
IC5	74LS07
IC6	74LS06
D6...D18	1N4148
C9	470 μF electrolyte
C10	1 μF ceramic multilayer
C11	1 μF ceramic multilayer
R10...R18	560 Ω
R19	330 Ω

Table 15: 1 PPS distributor: Parts for the signal input and TTL ouput module.

Parameter	Value
Diode number:	3
Wavelength:	850 nm
Data rate:	85 MHz
Coupled power:	$>29\,\mu$W at 100 mA into 50/125 μm glass fibre
Max. forward current:	100 mA
Typ. forward voltage:	1.8 V at 100 mA
Operating temperature:	-40...+85 °C

Table 16: Parameters of Ratioplast FO transmitter number 905SE850ST1Z1. The IV characteristiv curve of the transmitter is displayed in Fig. 8.

Parameter	Value
Receiver number:	4
Wavelength:	850 nm
Data rate:	max. 5 MBit/s
Opt. sensitivity:	min. 3 μW
Supply voltage:	5 V (4.5 V min., 7 V max.)
Supply current:	15 mA
Output signal:	digital, TTL compatible, inverted, open collector, 18 V max.
Min. pull-up resistor:	390 Ω (VCC=5 EHV)
Delay times:	$t_{\mathrm{PLHR}} = 65\,\mathrm{ns}$, $t_{\mathrm{PHLR}} = 49\,\mathrm{ns}$ (8 μW, 560 Ω pull-up, output voltage transition from 0.5 V to 2.4 V)
Operating temperature:	-40...+85 °C

Table 17: Parameters of Ratioplast FO receiver number 905EM850ST1Z2. The signal sensitivity of the receiver is displayed in Fig. 8.

Part #	Parameters
C1	470 μF
C2	1 μF ceramic
IC1	MC7805CT (provide a heat sink!)

Table 18: 1 PPS multifunctional receiver: Parts for the power supply module.

Part #	Parameters
IC2	905EM850ST1Z2
R1	560 Ω
C1	470 µF
C2	1 µF ceramic
IC1	MC7805CT (provide a heat sink!)

Table 19: 1 PPS multifunctional receiver: Parts for the 1 PPS signal input module.

Part #	Parameters
IC3, IC4	select from Tab. 24; totem pole outputs are recommended
R2, R3	630 Ω for 5 mA LED current; 330 Ω for 10 mA; select current and LED type appropriately (Tab. 24)
C3, C4	220 nF ceramic

Table 20: 1 PPS multifunctional receiver: Parts for the TTL output modules.

Part #	Parameters
IC5	SN74LS06, SN7406, SN74LS07, or SN7407; see Tab. 24
C5	1 µF ceramic
R4…R9	560 Ω
D1…D6	1N4148

Table 21: 1 PPS multifunctional receiver: Parts for the TTL high voltage open collector output module.

Part #	Parameters
IC6	MAX 232
C6…C11	1 µF ceramic

Table 22: 1 PPS multifunctional receiver: Parts for the TTL to RS232 level converter module.

Part #	Parameters
IC6	SN75ALS192
C6 and C7	1 µF ceramic

Table 23: 1 PPS multifunctional receiver: Parts for the TTL to RS422 level converter module.

chip		output		
Part #	type	type	I_{OL}	V_{OH}
SN74LS04	INV	TP	8 mA	TTL
SN7404	INV	TP	16 mA	TTL
SN74LS05	INV	OC	8 mA	TTL
SN7405	INV	OC	16 mA	TTL
SN74LS06	INV	OC	40 mA	30 V
SN7406	INV	OC	40 mA	30 V
SN74LS07	DIR	OC	40 mA	30 V
SN7407	DIR	OC	40 mA	30 V
SN74LS14	ST INV	TP	8 mA	TTL
SN7414	ST INV	TP	16 mA	TTL

Table 24: 1 PPS multifunctional receiver: Buffer ICs. TP: totem pole, OC: open collector, INV: inverter, DIR: buffer, ST INV: Schmitt trigger inverter

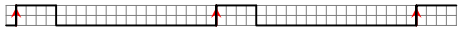
PPS (P_SEC at Meinberg GPS 167)	

Table 25: Definition of the PPS signal provided by the Meinberg reference clocks. The beginning of a new second is indicated by the front edge of a 200 ms wide pulse. All systems must synchronize to the front edge. Since clients expect different voltage level polarities (rising or falling edge) there is a finite risk to apply the wrong polarity causing the client to synchronize on the rear edge of the 200 ms pulse. **The only bullet-proof method to check the correct polarity is to record the PPS signal itself on the respective data acquisition system thus checking whether each front edge coincides with the beginning of a new second.**

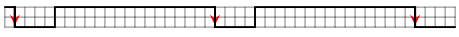
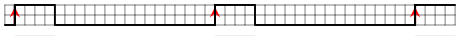
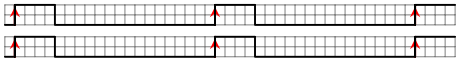
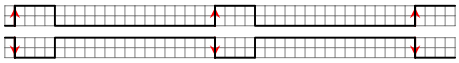
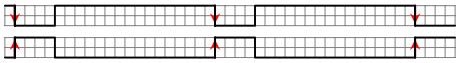
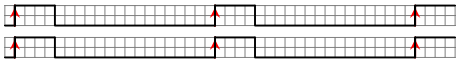
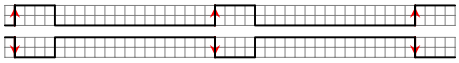
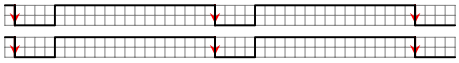
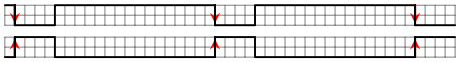
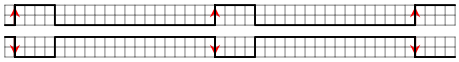
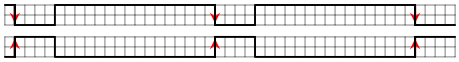
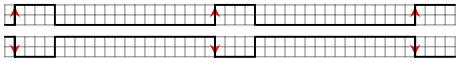
Signal	Edge polarity
FO (light)	
E (TTL)	
D (TTL)	
C	
TP6	
LED (light)	
TTL+ out	
TTL- out	
RS232+ out	
RS232- out	
$+$ out, Y (RS-422 A)	
$-$ out, Z (RS-422 B)	
RS-422 ($U_A - U_B$)	

Table 26: Polarity of 1 PPS edges provided for synchronization. FO (light) levels are defined in Tab. 1. All other diagrams (except LED signal) are given for voltage levels of electric signals. Points E, D, C, and TP6 refer to the circuit diagram in Fig. 9. The specification for the LED is as given in secs. 1.4 and 4.1.3. TTL, RS-232, and RS-422 voltage levels are defined in Tab. 3, Tab. 4, and Tabs. 5 and 6, respectively.

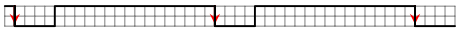
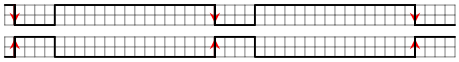
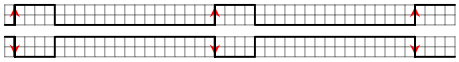
Client / Signal	Edge polarity
Q330 / RS-232, pin F, X41PPSIN	
Q330 / RS-422, pin H, X41PPS+	
Q330 / RS-422, pin J, X41PPS-	
Q330 / RS-422, $U_{\text{pin H}} - U_{\text{pin J}}$	

Table 27: Polarity of 1 PPS edges as expected by the Q330. Given are voltage levels on the pins of the EXT GPS port (plug type: ITT Canon KPT06F12-14P, Q330 manual page 226). Notice that RS-232 has reverse logic level definition (Tab. 4). RS-232 voltage levels are given with respect to GPS COM (X4GND, pin C). Synchronization to RS-232 falling voltage level edge is due to Kinemetrics' Technical Support (email to RWS 28.2.2008). RS-422 polarity was confirmed by PD and RWS due to tests (10.5.2012).

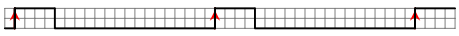
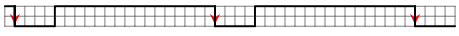
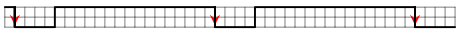
Client / Signal	Edge polarity
UIPC DAC-3 / RS-422, J3-11 RB(B)-GPS_1PPS	
UIPC DAC-3 / RS-422, J3-12 RB(A)-GPS_1PPS	
UIPC DAC-3 / RS-422, A-B	

Table 28: Polarity of 1 PPS edges as expected by the DAC-3 controller of SG 056. Given are the voltage level signal diagrams at GPS connector (J3, pins 11 and 12) on the back panel of the DAC-3 controller. This pins take the GPS 1 PPS signal from an external source with RS-422 voltage level. The J3 connector is of type CPC-17-14. **Beware:** The internal wiring on the RS-422/RS-232 optoisolator module in the DAC-3 is highly confusing (Drawing No. 981025-S2, GWR Inst. B2000-028 Rev. 2, `DAC-3-2B.SCH`, sheet 2)! J 3 pin **11** is called RB(**B**)-GPS_1PPS and is connected to U 11 pin **12**, which is input **A** of the 75ALS180. Similary J 3 pin **12** is called RB(**A**)-GPS_1PPS and is connected to U 11 pin **11**, which is input **B** of the 75ALS180.

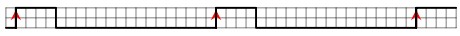
Client / Signal	Edge polarity
EDD / pin 4 or pin F, TTL	

Table 29: Polarity of 1 PPS edges as expected by the Earth-Data digitizer (EDD). The EDD has two connectors to receive a 1 PPS signal. It expects a rising edge TTL signal like produced by the GRAMIN GPS 35HV receiver on pin 2 or pin F with respect to ground on pin 2 or pin D, respectively.

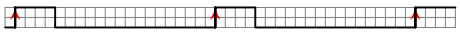
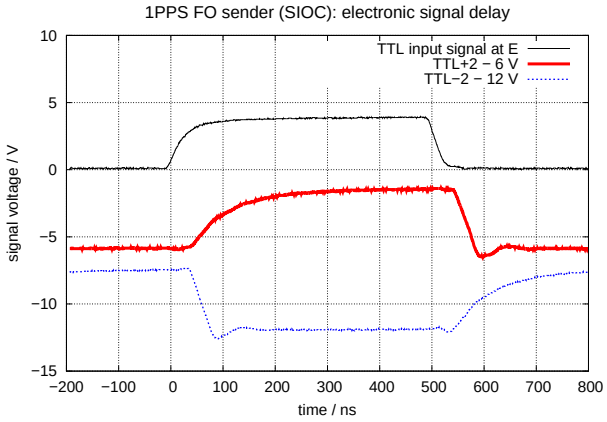
Client / Signal	Edge polarity
PDAS / TTL	

Table 30: Polarity of 1 PPS edges as expected by the PDAS-100 data acquisition system. The user's manual (Teledyne Geotech, 1989) specifies the expected signal to be rising edge (Teledyne Geotech, 1989, Fig. 3-22) with 5 V CMOS logicl levels and TTL thresholds (Teledyne Geotech, 1989, sec. 2.4.2, page 2-15). Voltages below 0.8 V indicate low (L) state and voltages larger than 2.0 V indicate high (H) state.

a)



b)

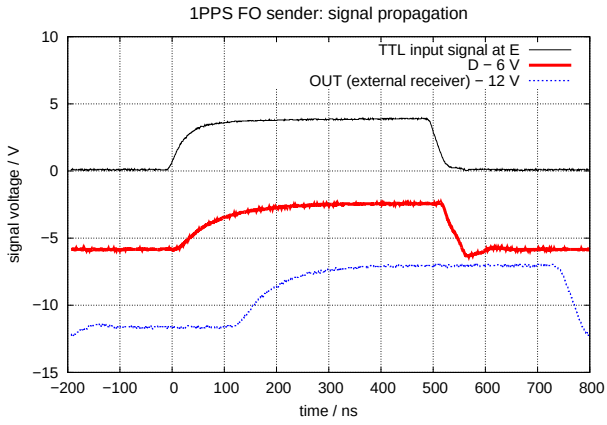
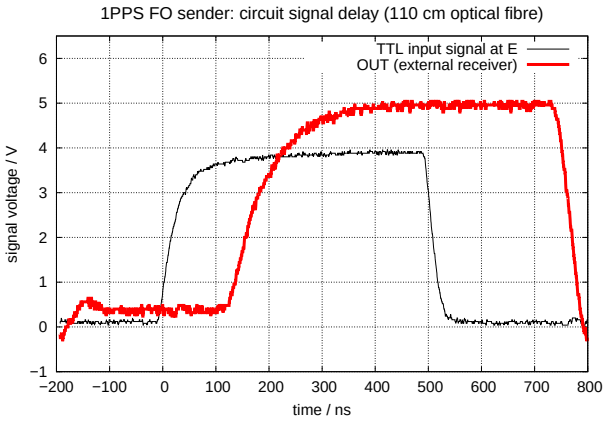


Figure 3: 1 PPS distributor: Internal signal propagation performance. a) Propagation of electric input signal (E, black) to positive (TTL+2, thick red) and inverted (TTL-2, blue dotted) electric TTL signal outputs. b) Propagation of TTL input signal (E, black) to switching circuit input (D, thick red) and to the output of an external receiver (blue dotted). Signals are offset intentionally for better visibility (see graph legend).

a)



b)

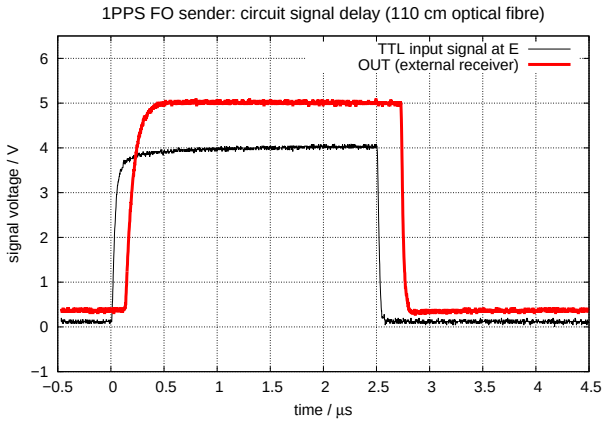


Figure 4: 1 PPS distributor: Signal propagation performance. Propagation of TTL input signal (E, black) to the output of an external receiver (thick red) on two different time scales.

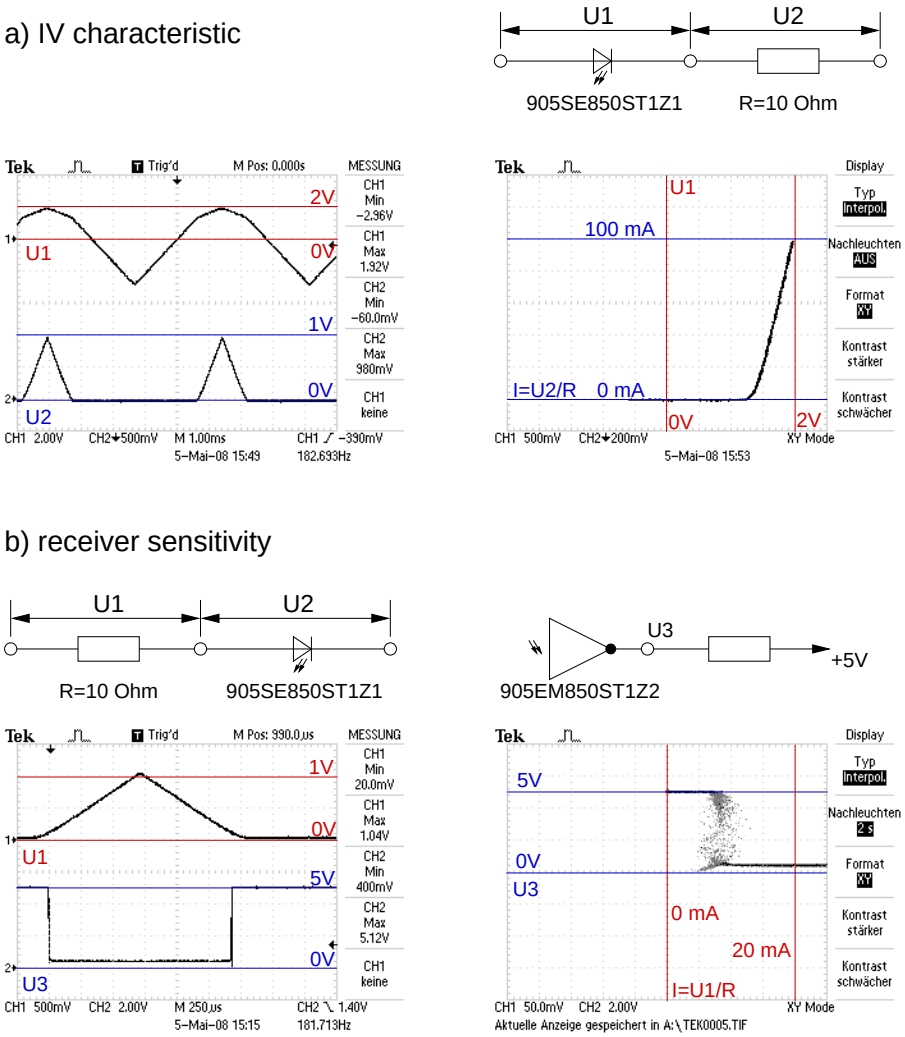
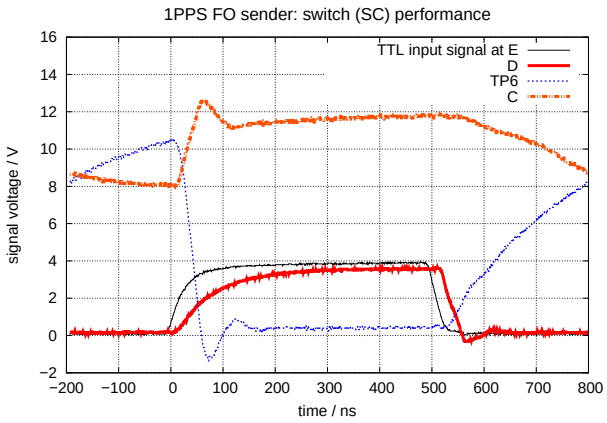


Figure 8: Characteristics of the FO sender and receiver. The characteristics are recorded by applying a symmetric triangular voltage to the resistor and diode connected in series. a) IV characteristic curve for the FO sender diode 905SE850ST1Z1. The diode has a forward voltage of 1.8 V when driven with the maximum current of 100 mA. b) The sensitivity of the receiver 905EM850ST1Z2. Sender and receiver are connected by a short (approx. 1 m long) optical fibre. The receiver switches at a transmitter forward current of approx. 8 mA.

a)



b)

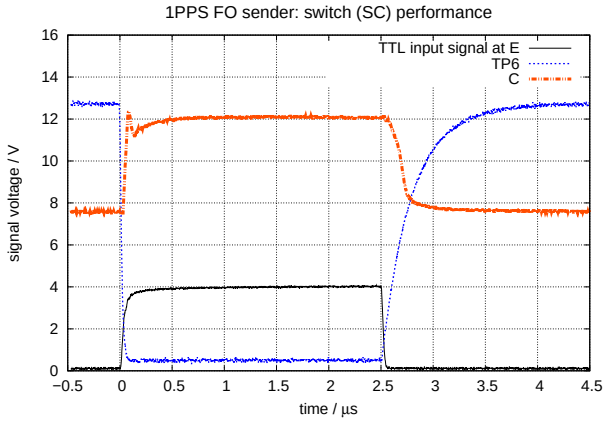
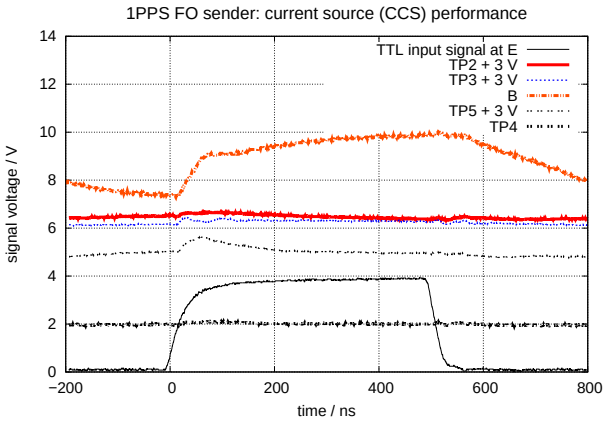


Figure 5: 1 PPS distributor: Switching circuit (SC) performance on two different time scales. black: TTL input signal (E). thick red: signal at switching circuit input (D). dotted blue: signal at collector of switching transistor T2 (TP6). thick dotted orange: signal at output of switch (C), i.e. collector of switching transistor T3.

a)



b)

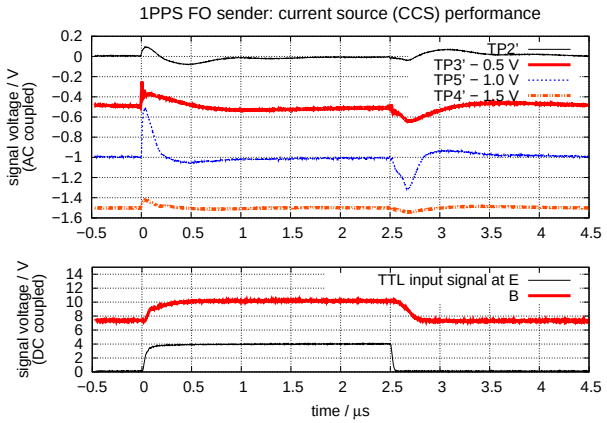


Figure 6: 1 PPS distributor: Current source (CCS) performance on two different time scales. E: TTL input signal. TP2: Output of OpAmp IC2. TP3: Base of Darlington power transistor T1 (current regulator). TP4: Inverting input of OpAmp IC2. TP5: Emitter of Darlington power transistor T1 at current sensing resistor R3. B: Collector of Darlington power transistor T1. Signals at TP2', TP3', TP4', and TP5' are recorded with AC coupling in b). Some of the signals are offset intentionally for better visibility (see graph legend).

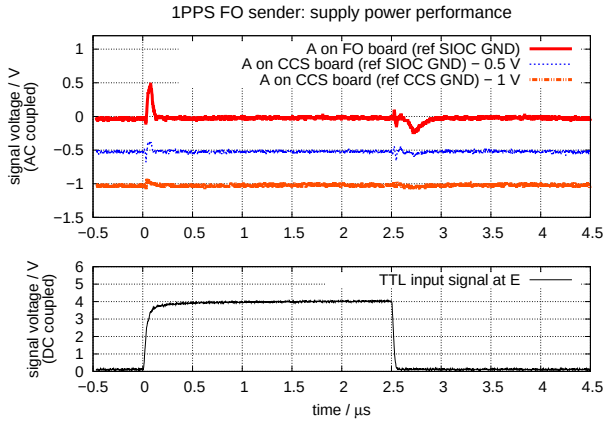
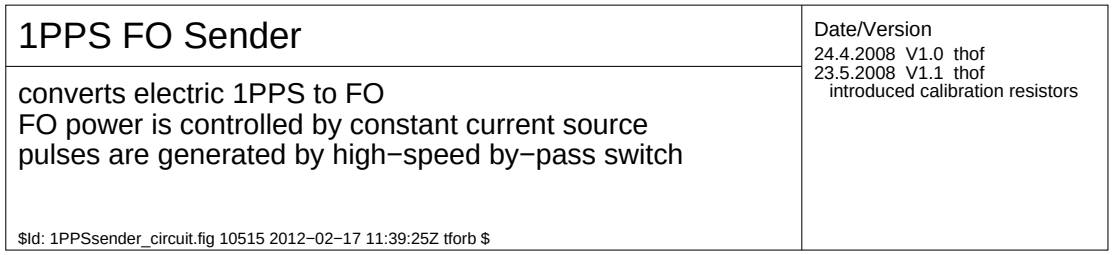


Figure 7: 1 PPS distributor: Supply voltage performance. The supply power (A) is recorded at different locations AC coupled. thick red: FO board with reference to GND on SIOC board. dotted blue: CCS board with reference to GND on SIOC board. thick dotted orange: CCS board with reference to GND on CCS board. The signals are offset intentionally for better visibility (see graph legend). In the lower panel the TTL input signal (E) is displayed for timing reference.



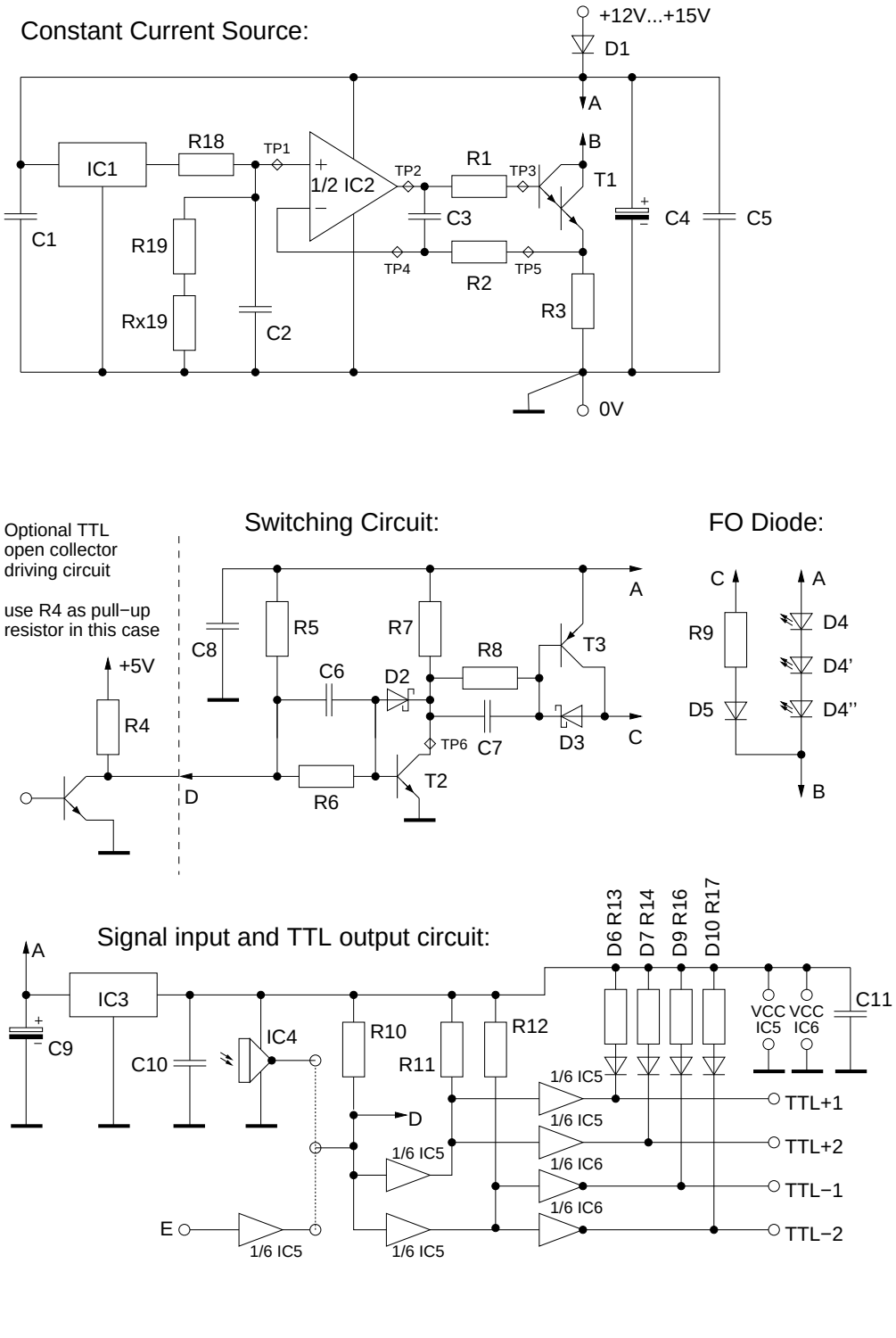
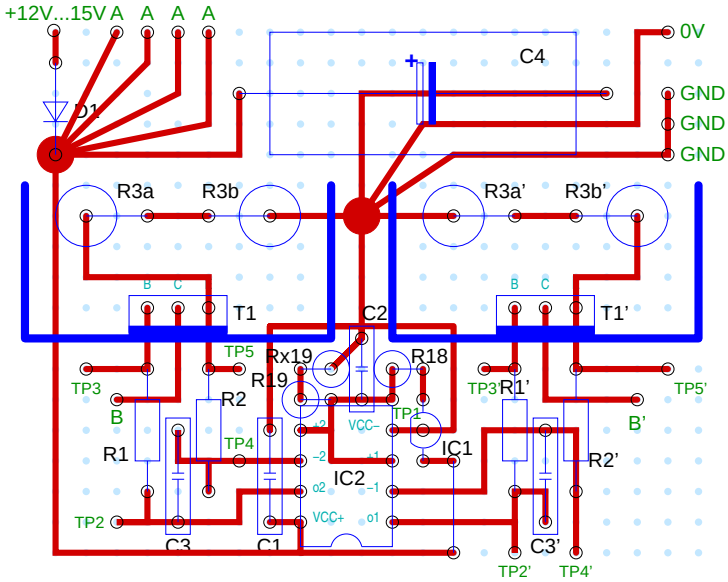


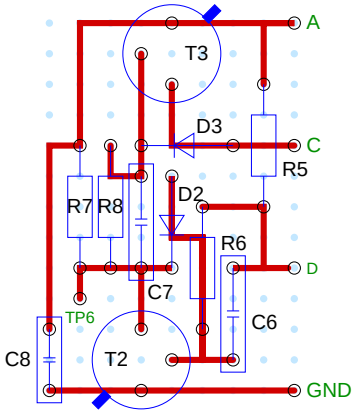
Figure 9: 1 PPS distributor: Circuit schematics.

1PPS FO Sender Board Layout	Date/Version
Layout is split into different modules $Id: 1PPSsender_layout.fig 10515 2012−02−17 11:39:25Z tforb $	24.4.2008 V1.0 thof 9.5.2008 V1.1 thof Corrections in SC and CCS 23.5.2008 V1.2 thof Calibration resistors in CCS

Constant Current Source (CCS):



Switching Circuit (SC):



Signal input and TTL output circuit (SIOC):

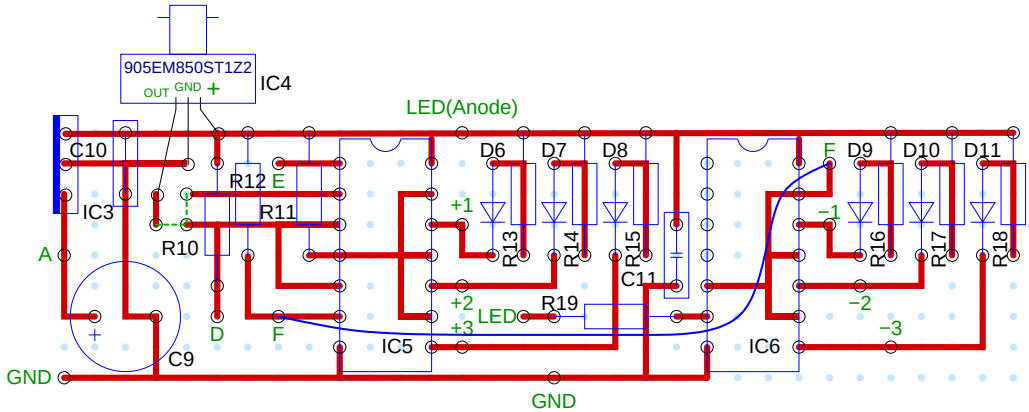


Figure 10: 1 PPS distributor: Board layout.

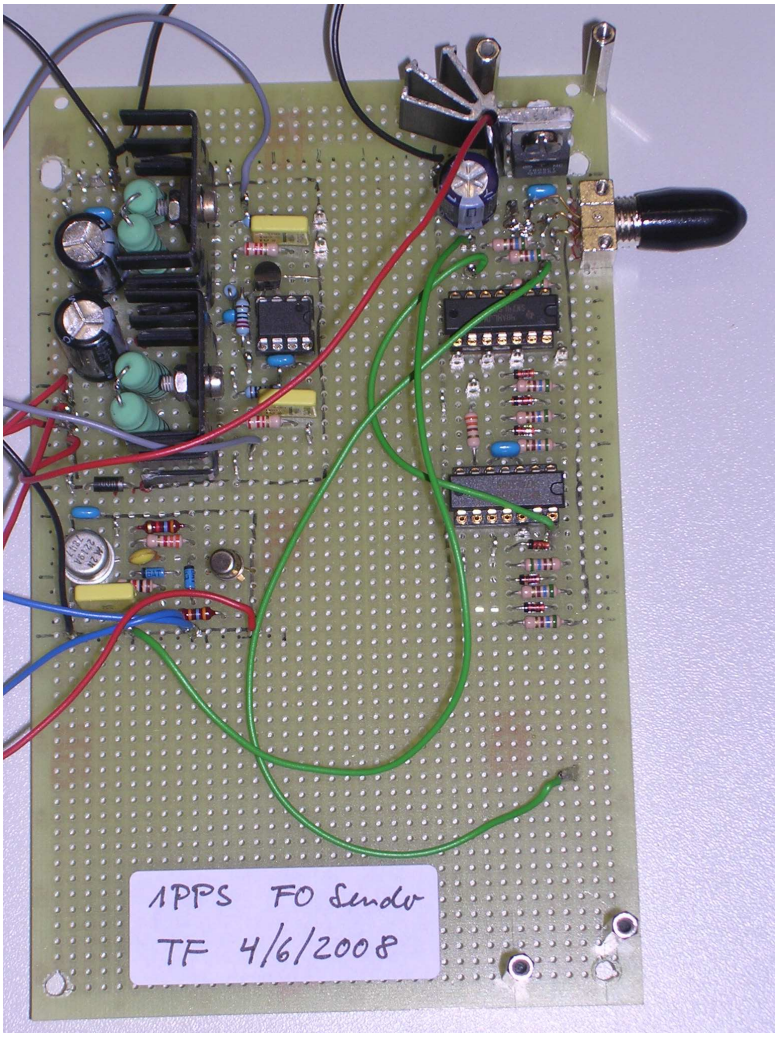


Figure 11: 1 PPS distributor: Prototype board.

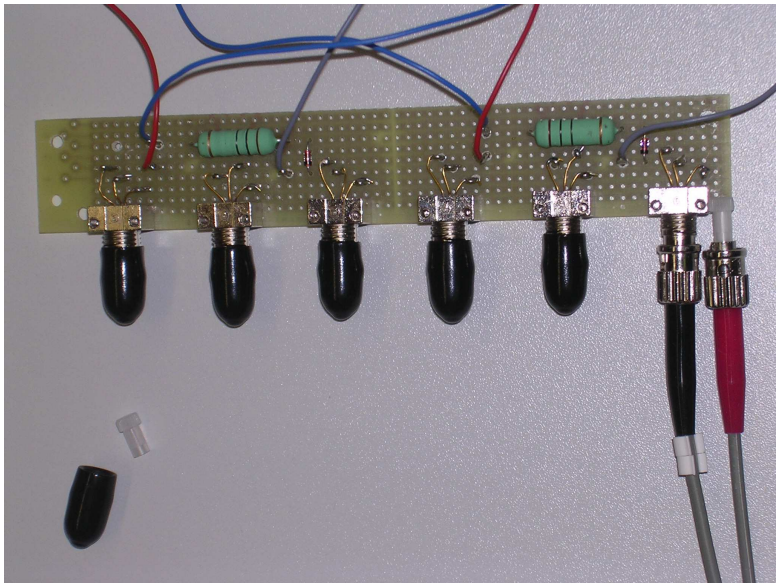


Figure 12: 1 PPS distributor: Prototype FO diode board.

Figure 13: 1 PPS distributor: Supply power during performance test.

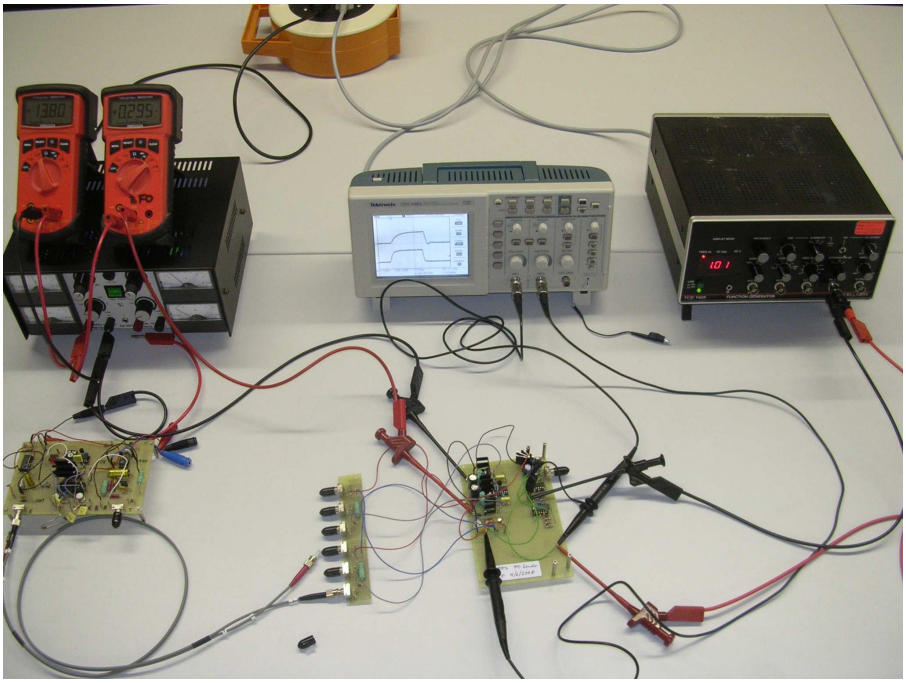


Figure 14: 1 PPS distributor: Performace test setup.

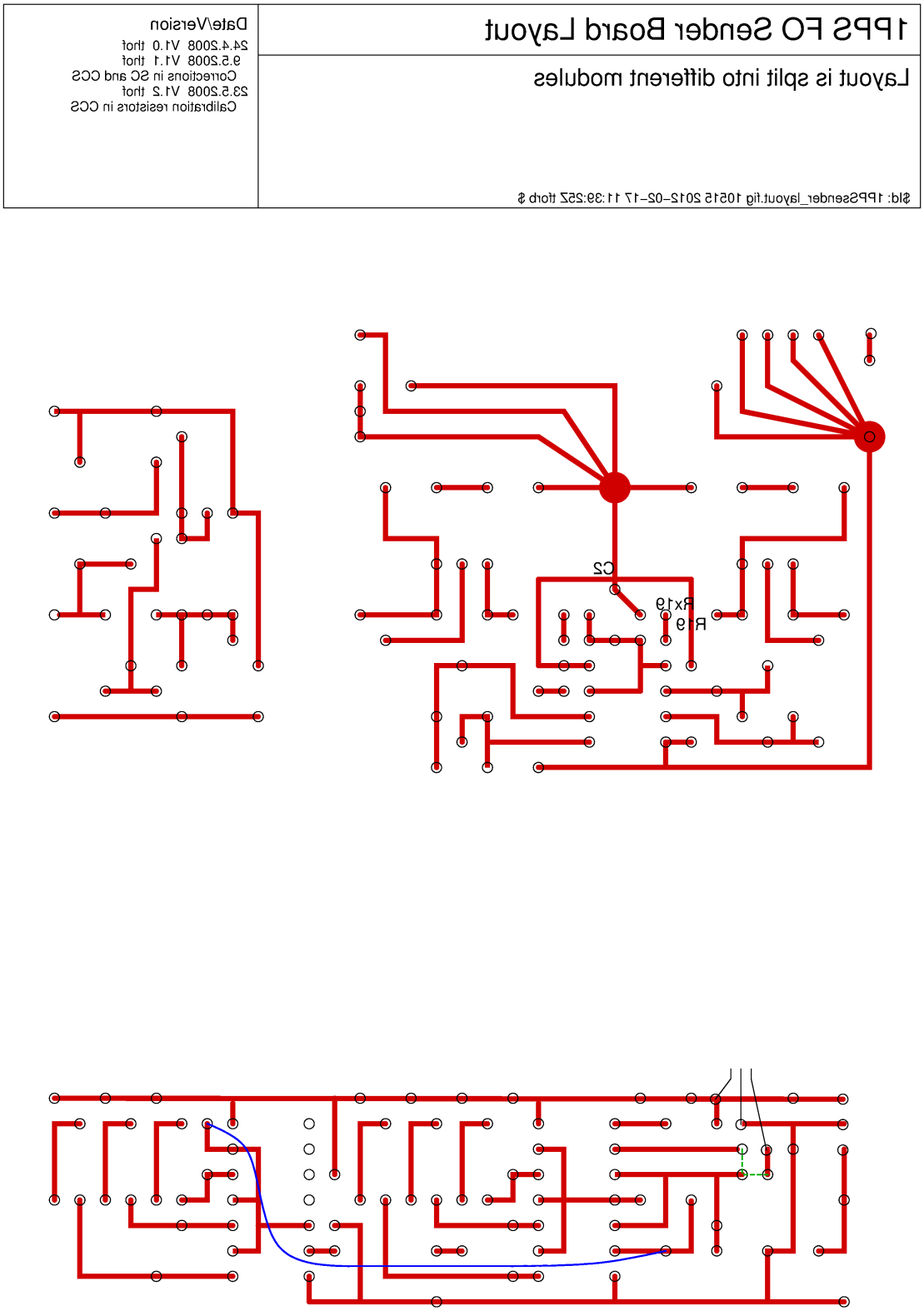
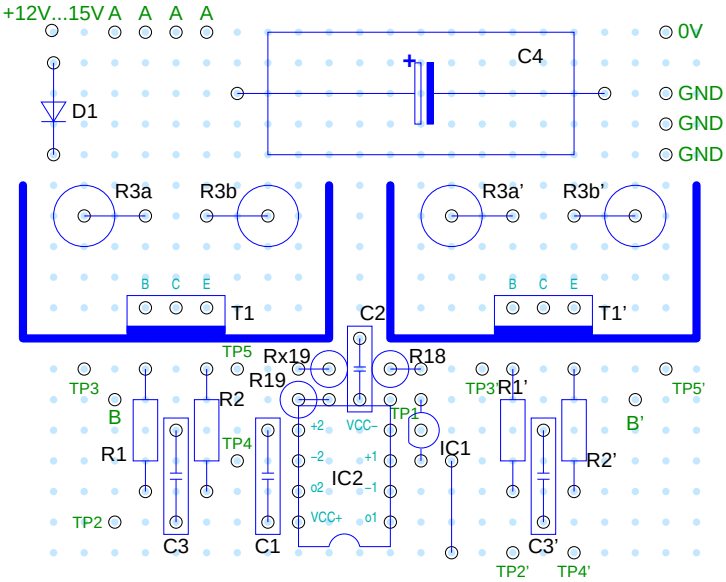


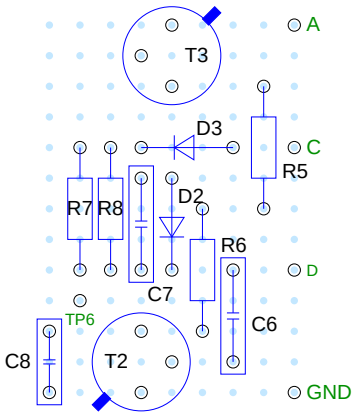
Figure 15: 1 PPS distributor: Board layout wiring diagram.

1PPS FO Sender Board Layout	Date/Version
Layout is split into different modules	24.4.2008 V1.0 thof 9.5.2008 V1.1 thof Corrections in SC and CCS 23.5.2008 V1.2 thof Calibration resistors in CCS
$Id: 1PPSsender_layout.fig 10515 2012−02−17 11:39:25Z tforb $	

Constant Current Source (CCS):



Switching Circuit (SC):



Signal input and TTL output circuit (SIOC):

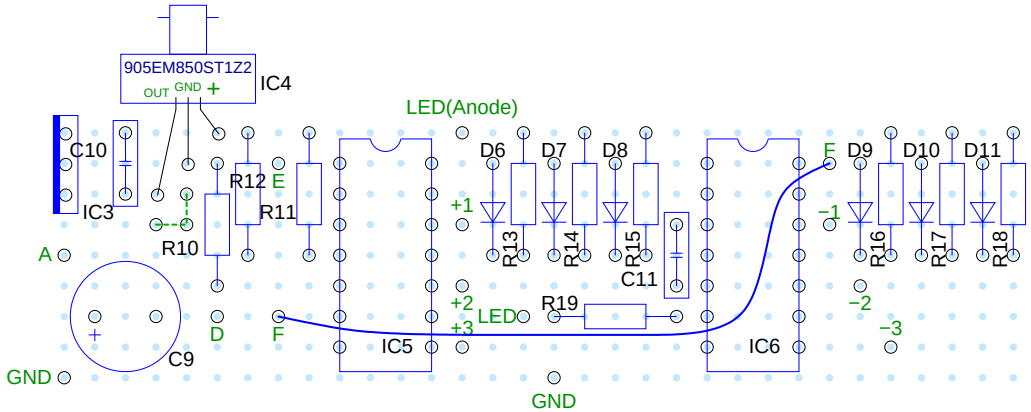
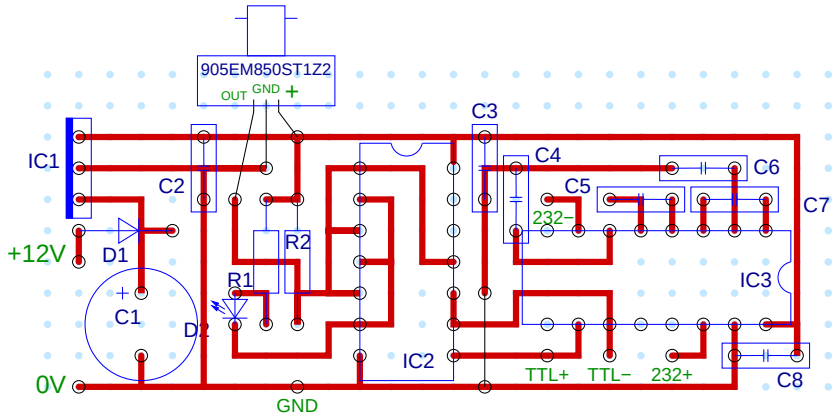


Figure 16: 1 PPS distributor: Board layout parts placement.

1PPS FO−Receiver	Date/Version
Receiver for 1PPS signal with FO input Outputs: TTL and RS−232 levels with rising and falling edge are available. If RS−232 levels are not required, IC3 and C4−C8 can remain unpopulated. Connect IC2's outputs only in parallel if using an open−collector SN74LS06.	1.4.2008 V1.0 (thof) 5.6.2008 V1.1 (thof) signal polarity convention

$Id: 1PPSempfaenger.fig 10515 2012−02−17 11:39:25Z tforb $

Component side:



IC1: 7805
IC2: SN74LS04 (open collector output SN74LS06 can be used alternatively)
IC3: MAX232
D1: 1N4004
D2: LED rot (evtl. auf Lötpfosten)
R1: 390 Ohm
R2: 560 Ohm
C1: 100 uF/40V
C2−C8: 1 uF Kermaik

Figure 17: 1 PPS FO receiver: Board layout.

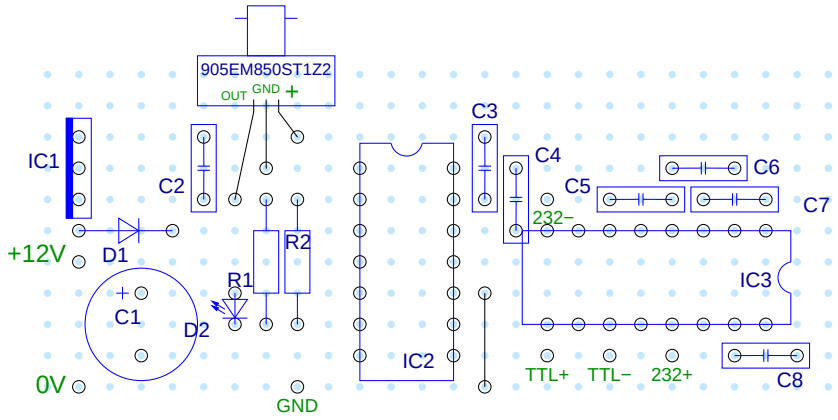
1PPS FO–Receiver	Date\Version 1.4.2008 V1.0 (thof) 5.6.2008 V1.1 (thof) signal polarity convention
Receiver for 1PPS signal with FO input Outputs: TTL and RS–232 levels with rising and falling edge are available. If RS–232 levels are not required, IC3 and C4–C8 can remain unpopulated. Connect IC2's outputs only in parallel if using an open–collector SN74LS06.	

Figure 18: 1 PPS FO receiver: Board layout wiring diagram.

1PPS FO−Receiver	Date/Version
Receiver for 1PPS signal with FO input Outputs: TTL and RS−232 levels with rising and falling edge are available. If RS−232 levels are not required, IC3 and C4−C8 can remain unpopulated. Connect IC2's outputs only in parallel if using an open−collector SN74LS06.	1.4.2008 V1.0 (thof) 5.6.2008 V1.1 (thof) signal polarity convention

$Id: 1PPSempfaenger.fig 10515 2012−02−17 11:39:25Z tforb $

Component side:



IC1: 7805
IC2: SN74LS04 (open collector output SN74LS06 can be used alternatively)
IC3: MAX232
D1: 1N4004
D2: LED rot (evtl. auf Lötpfosten)
R1: 390 Ohm
R2: 560 Ohm
C1: 100 uF/40V
C2−C8: 1 uF Kermaik

Figure 19: 1 PPS FO receiver: Board layout parts placements.

1PPS FO Multireceiver	Date/Version
Receiver for electrical and FO input. Distributes 1PPS signal to TTL outputs and optionally to open collector and RS232 level outputs. $Id: 1PPSmultireceiver_layout.fig 10515 2012−02−17 11:39:25Z tforb $	2.7.2008 V1.0 thof 16.2.2009 V1.1 IC3 and 4 in series

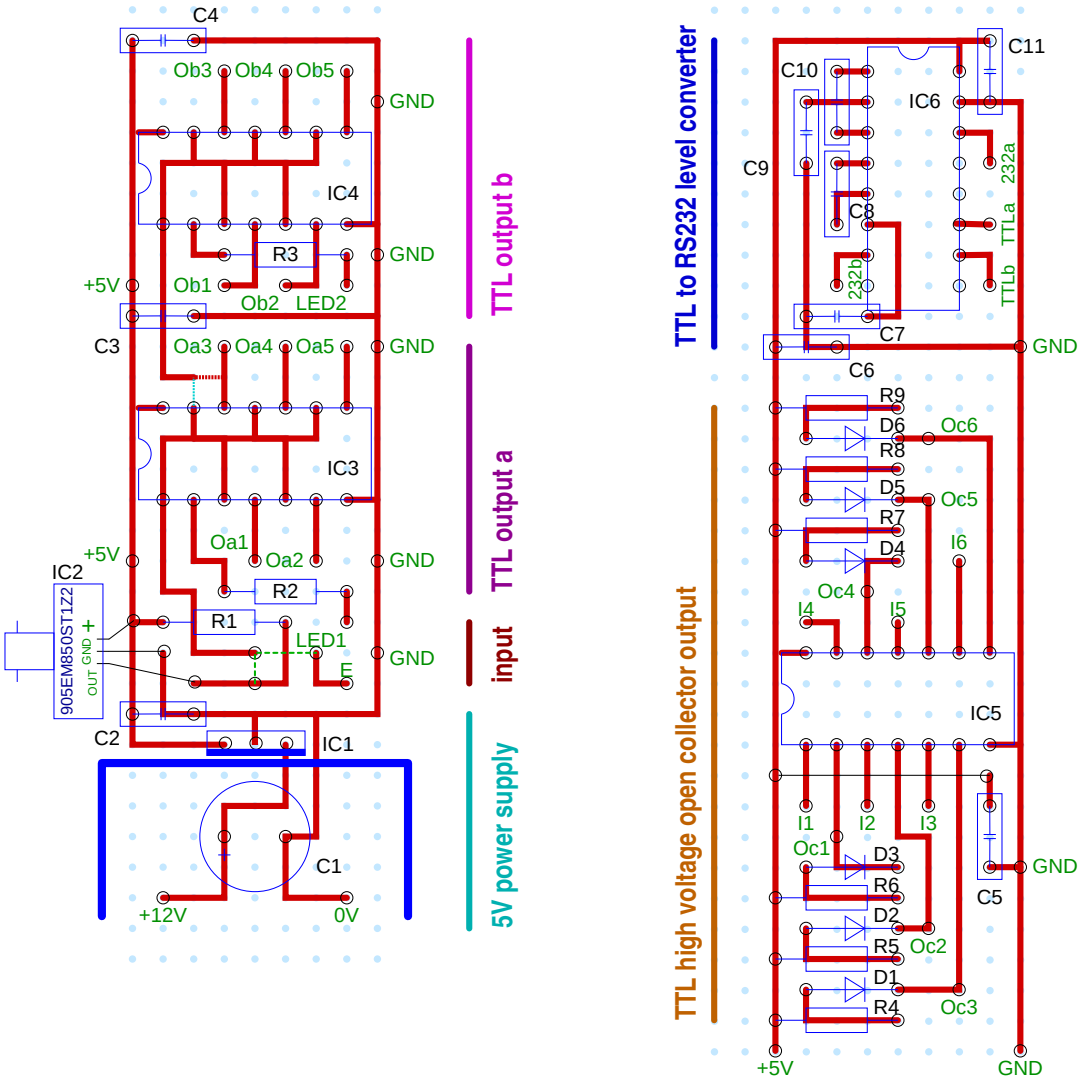


Figure 20: 1 PPS multifunctional receiver with RS-232 output: Board layout.

Figure 21: 1 PPS multifunctional receiver with RS-232 output: Board layout wiring diagram.

1PPS FO Multireceiver	Date/Version
Receiver for electrical and FO input. Distributes 1PPS signal to TTL outputs and optionally to open collector and RS232 level outputs. $Id: 1PPSmultireceiver_layout.fig 10515 2012−02−17 11:39:25Z tforb $	2.7.2008 V1.0 thof 16.2.2009 V1.1 IC3 and 4 in series

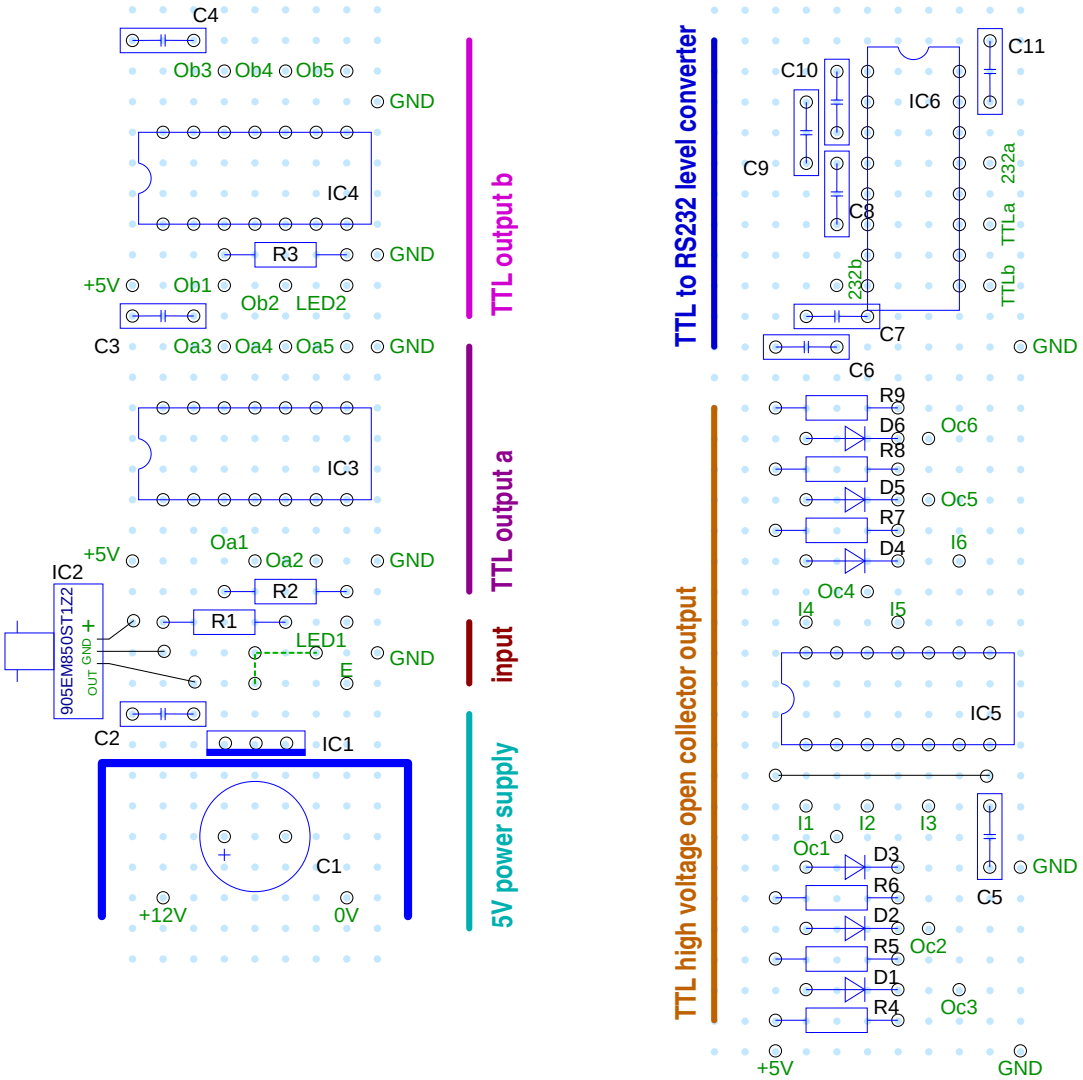


Figure 22: 1 PPS multifunctional receiver with RS-232 output: Board layout parts placement.

1PPS FO Multireceiver with RS−422 output	Date/Version
Receiver for electrical and FO input. Distributes 1PPS signal to TTL outputs and optionally to open collector and RS422 level outputs. $Id: 1PPSmultireceiverRS422_layout.fig 10515 2012−02−17 11:39:25Z tforb $	2.7.2008 V1.0 thof 16.2.2009 V1.1 IC3 and 4 in series 26.4.2010 V1.2 RS422 replaces RS232

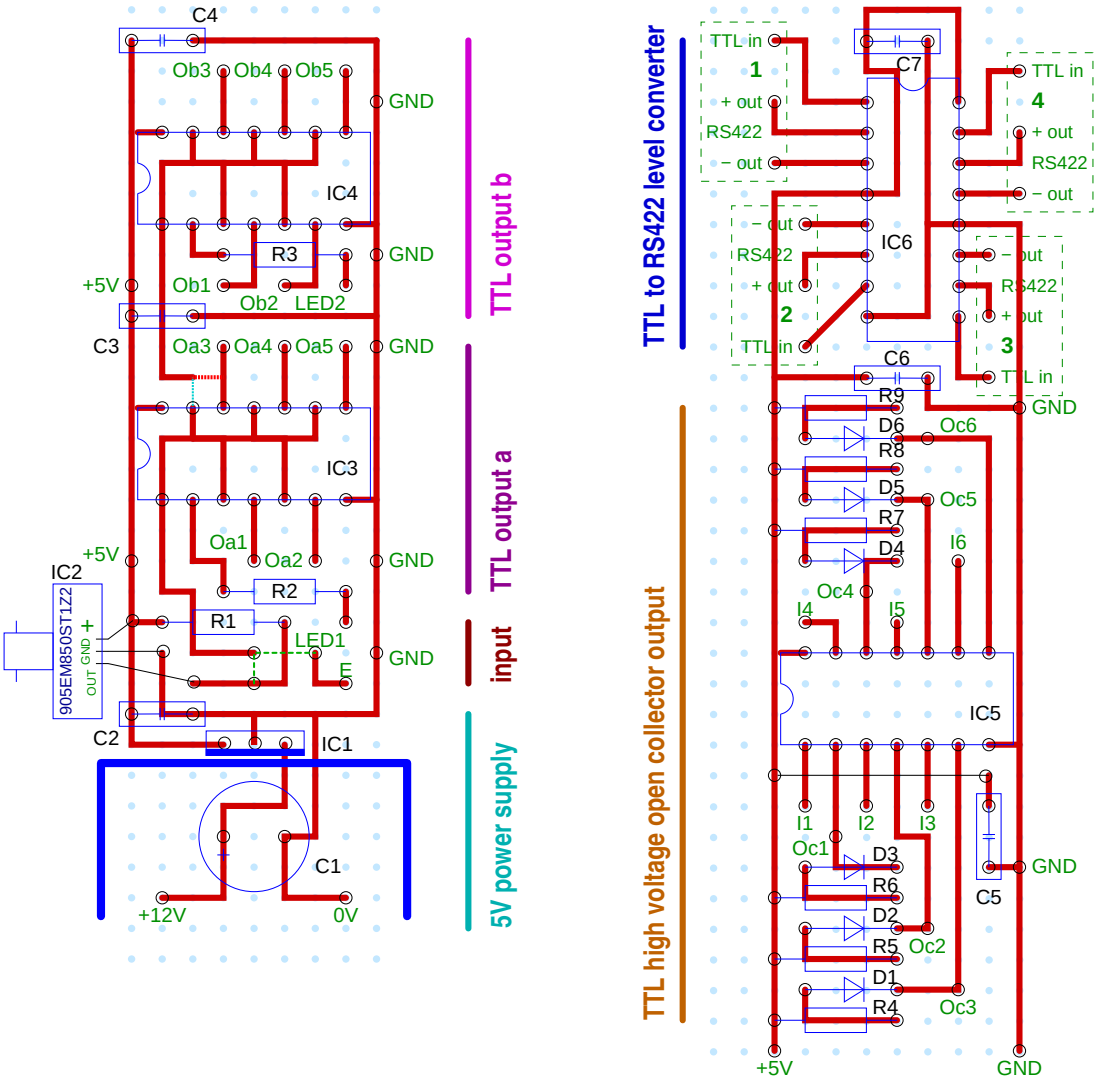


Figure 23: 1 PPS multifunctional receiver with RS-422 output: Board layout.

Figure 24: 1 PPS multifunctional receiver with RS-422 output: Board layout wiring diagram.

1PPS FO Multireceiver with RS−422 output	Date/Version
Receiver for electrical and FO input. Distributes 1PPS signal to TTL outputs and optionally to open collector and RS422 level outputs. $Id: 1PPSmultireceiverRS422_layout.fig 10515 2012−02−17 11:39:25Z tforb $	2.7.2008 V1.0 thof 16.2.2009 V1.1 IC3 and 4 in series 26.4.2010 V1.2 RS422 replaces RS232

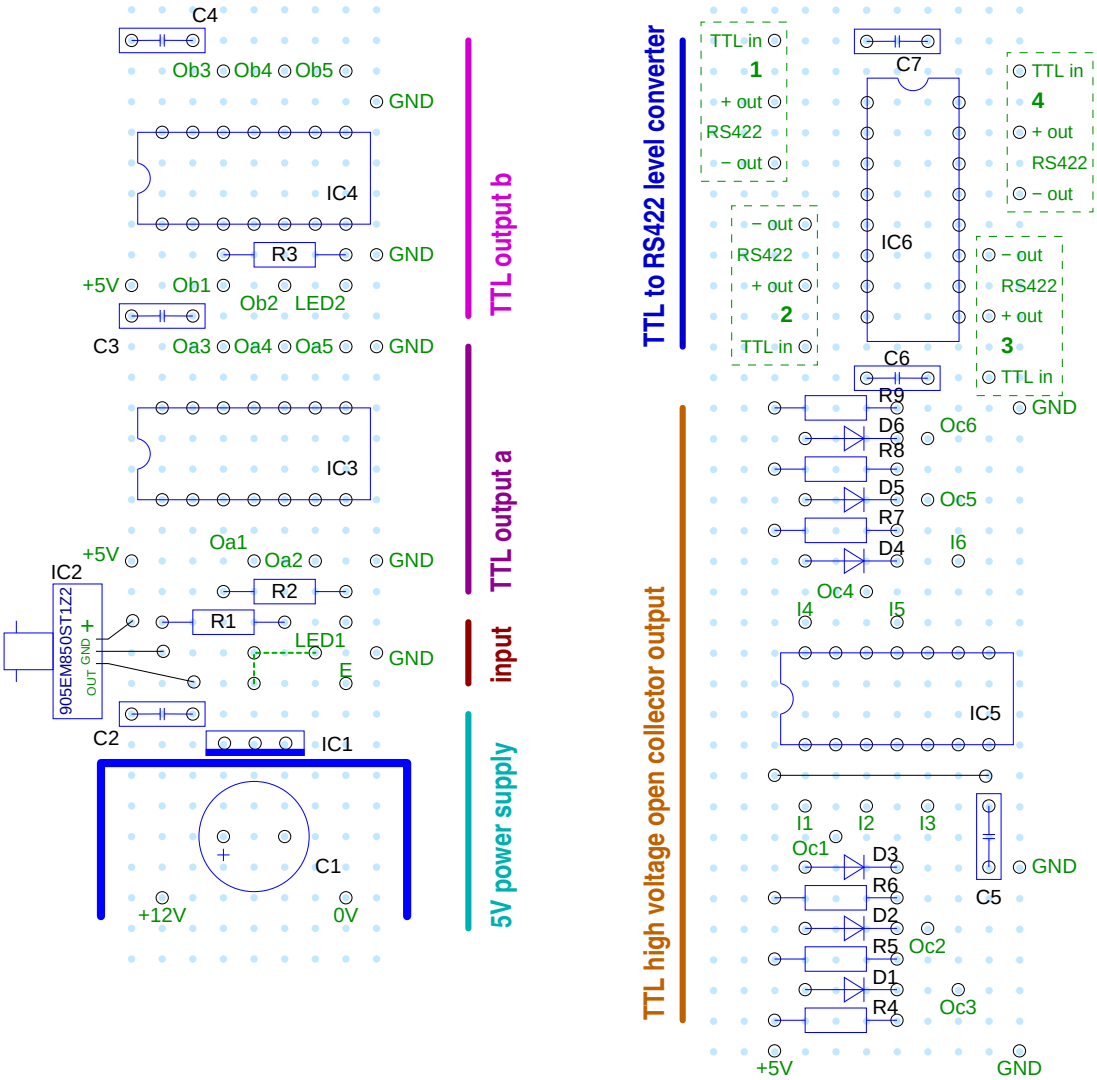


Figure 25: 1 PPS multifunctional receiver with RS-422 output: Board layout parts placement.