Graphene field-effect devices at high frequencies

Zur Erlangung des akademischen Grades eines
DOKTORS DER NATURWISSENSCHAFTEN
durch die Fakultät für Physik
des Karlsruher Instituts für Technologie

genehmigte

DISSERTATION

von

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aus Karlsruhe

Tag der mündlichen Prüfung:	31.10.2014
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List of publications

Papers related to this thesis

Paper A E. Pallecchi*, C. Benz*, A. C. Betz, H. v. Löhneysen, B. Plaçais, and R. Danneau. "Graphene microwave transistors on sapphire substrates", *Appl. Phys. Lett.* **99**, 113502 (2011). *These authors contributed equally to this work.

Paper B C. Benz, M. Thürmer, F. Wu, Z. Ben Aziza, J. Mohrmann, H. v. Löhneysen, K. Watanabe, T. Taniguchi, and R. Danneau. "Graphene on boron nitride microwave transistors driven by graphene nanoribbon back-gates", *Appl. Phys. Lett.* **102**, 033505 (2013).

Other papers not related to this thesis

Paper C N. Gruhler, C. Benz, H. Jang, J.-H. Ahn, R. Danneau, and W. H. P. Pernice. "High-quality Si_3N_4 circuits as a platform for graphene-based nanophotonic devices", *Opt. Express* **21**, 31678 (2013).

Contents

Nomenclature

Abbreviations

ALD	Atomic layer deposition
CNT	Carbon nanotube
CVD	Chemical vapor deposition
DOS	Density of states
FET	Field-effect transistor
GFET	Graphene field-effect transistor
GNR	Graphene nanoribbon
hBN	Hexagonal boron nitride
HEMT	High electron mobility transistor
LNA	Low noise amplifier
MOSFET	Metal oxide semiconductor field-effect transistor
QED	Quantum electrodynamics
RF	Radio frequency
SEM	Scanning electron microscope

Notations

c_0	Speed of light in vacuum
C_{dg}	Drain-gate capacitance
C_{gd}	Gate-drain capacitance
C_{gs}	Gate-source capacitance
C_{pd}	Pad-drain capacitance
C_{pg}	Pad-gate capacitance
C_{q}	Quantum capacitance of graphene

E_F	Fermi energy
ε, κ	Dielectric permittivity
f_T	Transit frequency
g_m	Transconductance
h_{21}	Short circuit current gain
h	Planck constant
$\hbar$	Reduced Planck constant
I_ds	Drain-source current
k_B	Boltzmann constant
l_ch	Channel length (drain-source distance)
l_g	Gate length
n	Charge carrier density
n_0	Residual charge carrier density
R_c	Contact resistance
R_ds	Total drain to source resistance
R_g	Gate resistance
σ	Electrical conductivity
σ_min	Electrical conductivity at Dirac voltage
t_diel	Dielectric thickness
v_drift	Carrier drift velocity
v_F	Fermi velocity ($10^8\,\mathrm{cm/s}$)
v_sat	Carrier saturation velocity
V_Dirac	Dirac voltage
V_ds	Drain-source voltage
V_gs	Gate-source voltage
w_ch	Channel width
w_g	Gate width

Introduction

In the interconnected world of today, a growing demand for high-frequency electronics emerges. The rising amount of data transmitted at ever-increasing speed requires the development of new circuits with amplifiers operating in the microwave frequency range ($300\,\mathrm{MHz} - 300\,\mathrm{GHz}$). In most cases, field-effect transistors (FET) are used as the basic building block of those complex electronics.

The first FETs operating at gigahertz frequencies were realized already in 1967 using GaAs.[1] Current state-of-the-art high electron mobility transistors (HEMT) reach transit frequencies (f_T) of 650 GHz and a maximum frequency of oscillation (f_max) of 1.2 THz.[2] The substantial performance improvements were established through down-scaling of the device dimensions (especially the gate length), and reduction of the dielectric thickness while using materials with high dielectric constant. However, the classical semiconductor-based FET technology is approaching the scaling limit. Further reduction of the device geometry may not be possible in the foreseeable future.

Higher operating frequencies can also be achieved by using a channel material with larger charge carrier mobility and increased saturation velocity. Therefore, alternative materials are desperately looked for. Initially, carbon nanotube (CNT) FETs were investigated to some extent[3,4,5,6,7], however the high resistivity and low drain currents of single nanotubes remain a limiting factor. By complex arrangement of multiple CNT in an array, the device performance recently was increased to the current record for radio frequency (RF) CNT of $f_\mathrm{T} = 153\,\mathrm{GHz}$ and $f_\mathrm{max} = 30\,\mathrm{GHz}$.[8]

The discovery of graphene, a two-dimensional crystal comprised of carbon atoms arranged in a hexagonal lattice, brought new momentum to the search for semiconductor alternatives.[9] The zero-bandgap material possesses an intrinsic charge carrier mobility and saturation velocity considerably larger than that of competing materials,[10] which makes it ideal for high frequency applications.[11] Indeed, already in 2009 graphene was listed as a potential emerging material in the international technology roadmap for semiconductors (ITRS).[12] In contrast to carbon nanotubes, device dimensions can be scaled easily, supporting high current densities of $> 2 \cdot 10^8\,\mathrm{A/cm^2}$.[13] Apart from outstanding electronic transport properties, graphene offers excellent heat conduction,[14] is transparent,[15] stretchable, yet extremely stiff[16] and thin. Therefore it may be used for specialized applications unachievable with traditional semiconductors.

The development of RF graphene field-effect transistors (GFET) progressed very fast compared to CNT FETs.[17,18,19,20,21,22,23] Less than five years have passed from the first-time realization of GFET operating at GHz frequencies[17] to the current record holding GFET with $f_\mathrm{T} = 427\,\mathrm{GHz}$ at a gate length of 67 nm[22]. In terms of transit frequency, graphene FET can already compete with state-of-the-art HEMT.[13] Further down-scaling of the gate length and improvements in graphene quality could pave the way for GFETs approaching

the THz regime. However, due to the missing band gap in graphene, current saturation is limited, which explains the rather low $f_{\max} \leq 105\,\mathrm{GHz}$[24] values seen so far.

Along with graphene, a whole new group of 2D materials such as hexagonal boron nitride (hBN), molybdenum disulfide (MoS_2), and black phosphorus were discovered.[25] Through combination (stacking) of multiple 2D materials, advanced heterostructures can be created, potentially offering unprecedented electrical conductivity and mechanical strength while being transparent and flexible.

Outline of this thesis

Chapter 1 addresses the basic properties of graphene such as its unique band structure and its electronic transport properties. In chapter 2 we discuss the peculiarities of graphene FETs and offer a comparison to classical, semiconductor-based FETs.

The experimental part is divided into three chapters. Chapter 3 deals with optimization of the substrate and dielectric for high frequency graphene FETs. We fabricate GFETs on sapphire, an insulating substrate reducing parasitic losses. Two representative devices reaching transit frequencies of up to $f_{\mathrm{T}} = 80\,\mathrm{GHz}$ are discussed. In chapter 4, graphene FETs on atomically flat hexagonal boron nitride substrates are investigated. Thin layers of hBN serve both as substrate and as dielectric for the bottom gate. Exploiting the thinness of graphene, we use few-layer graphene as gate material for extremely thin GFETs operating at gigahertz frequency. The metal-gated and graphene-gated devices are compared, highlighting their individual advantages. In the last experimental chapter, we demonstrate an array of similar GFETs using large area CVD-grown graphene for improved device comparability and reproducibility. We employ several contact reducing measures such as double contacts and local etching of the graphene for improved charge carrier injection. Devices are patterned with local double gates for increased gate effect. The resulting GFET performance is analyzed in dependence of the gate length. Lastly, fabrication methods and recipes as well as details on the high-frequency measurement techniques can be found in the appendix.

1 Properties of graphene

Graphene is the two-dimensional (2D) building block for numerous carbon allotropes. Wrapped up to a spherical object one obtains fullerenes (0D), rolling up a graphene sheet creates a carbon nanotube (1D) and stacks of a large number of graphene sheets lead to a graphite crystal (3D), as visualized in fig. 1.1.

The theoretical aspects of graphene as a part of graphite have been studied for almost 70 years.[27,28,29,30] Already in 1946, P.R.Wallace reported on the band structure of the semimetal and its linear dispersion relation.[27] Later, the more advanced Slonczewski-Weiss-McClure (SWM) model was used to describe the band structure of graphite.[29,30] Approximate 30 years ago, scientists began to use graphene as theoretical "toy" model for (2+1)-dimensional quantum electrodynamics (QED).[31]

For a long time, graphene was thought to be mechanically unstable and presumed not to exist. It was argued that in thin films, thermal fluctuations would lead to crystal defects and a decreased melting temperature rendering them thermodynamically unstable.[32,33] Despite the concerns many theories raised, substrate-supported graphene was confirmed experimentally roughly 10 years ago by K. Novoselov and A.K. Geim.[9] In 2010, the authors were awarded with the Nobel prize for their achievements. Although graphene is a true 2D material, its stability may be based on corrugations in the third dimension.[34] Over time it turned out that apart from graphene, a variety of other two-dimensional crystals existed (e.g.

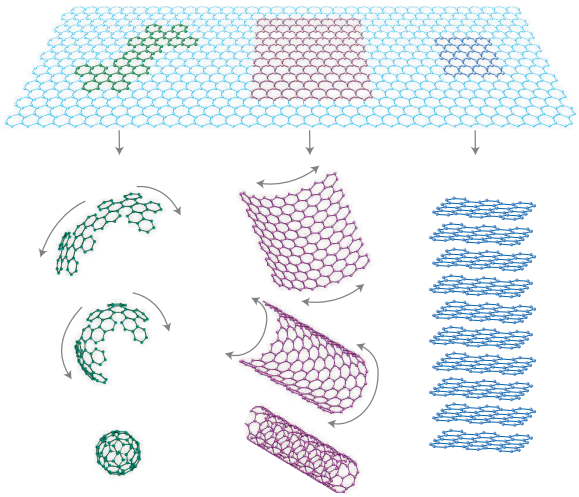

Figure 1.1: Carbon allotropes: 2D graphene is the building block for fullerenes (0D), carbon nanotubes (1D), and graphite (3D). *Source: adapted from*[26].

hexagonal boron nitride and MoS_2)[25], and in spite of exhibiting defects, they were of very high quality.[26]

Initially, graphene was produced by mechanical exfoliation (also referred to as micromechanical cleavage) of bulk graphite crystals with adhesive tape, the so called "scotch tape technique"[9]. So far this method yields unprecedented quality, however only small quantities of graphene can be obtained. Therefore, its main field of application is in scientific research. When larger amounts are required, two methods of epitaxial growth of graphene have been established: growth by chemical vapor deposition (CVD) on catalytic surfaces like Cu[35] or Ni[36], and thermal decomposition (sublimation) of silicon carbide (SiC) to graphene[37]. With these methods, mass production is possible, but often at the cost of inhomogeneous quality and usually with the need for additional transfer after growth.

In the following, an introduction to graphene's mechanical and electronic properties is given. For deeper insight, we suggest reverting to the review papers by A.K. Geim[26], A.H. Castro Neto[38], N.M.R. Peres[39], and S. Das Sarma[40].

1.1 Carbon

The carbon atoms in graphene are arranged in a hexagonal lattice held together by sp^2-hybridized electrons forming σ-bonds. With a binding energy of 4.3 eV between two adjacent carbon atoms, they are responsible for the mechanical strength of graphene. These localized, sp^2-hybridized electrons (see fig. 1.2) account for the carbon-carbon binding distance $a_b \approx 1.42$ Å. The remaining, delocalized valence electrons form weaker π-bonds and are responsible

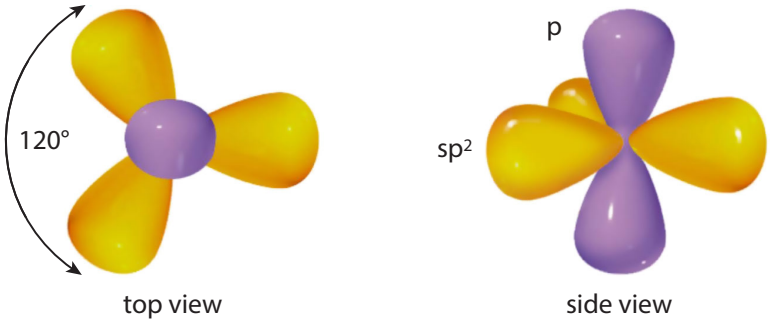

Figure 1.2: Schematic view of the three orbitals of sp^2-hybridized electrons. The angular spacing between the orbitals is 120°, while the orbitals of the π-electrons are arranged perpendicular to the hybridization plane. *Source: adapted from*[41]*, complemented.*

for the electronic transport properties of graphene. They are located outside of the sp^2 hybridization plane (symbolized by violet orbitals in fig. 1.2), enabling collision free, ballistic transport with a mean free path in the µm-range at very high charge carrier velocity[9,10,42].

The distance between multiple layers of graphene is 3.4 Å, defined by the lateral extend of the out-of-plane π-electrons. Adhesion between layers takes place only through the weak van-der-Waals bonds with a binding energy of just 0.07 eV. For that reason, it is very easy to cleave a graphite crystal along its basal plane.

1.2 Basics properties of graphene

1.2.1 Real space and reciprocal lattice

Graphene's honeycomb lattice is visualized in fig. 1.3(a). The two atom basis of the elementary unit cell is spanned by the two primitive lattice vectors

$$\boldsymbol{a_1} = \frac{a_\mathrm{b}}{2}\left(3,\sqrt{3}\right), \quad \boldsymbol{a_2} = \frac{a_\mathrm{b}}{2}\left(3,-\sqrt{3}\right).$$

$a_\mathrm{b} \approx 1.42\,\text{Å}$ is the carbon-carbon binding distance between the two triangular sublattices A and B, and $a = |\boldsymbol{a_1}| = |\boldsymbol{a_2}| = \sqrt{3}a_\mathrm{b} \approx 2.46\,\text{Å}$ is the lattice constant. Both sublattices are linked by the nearest-neighbor vectors

$$\boldsymbol{\delta_1} = \frac{a_\mathrm{b}}{2}\left(1,\sqrt{3}\right), \quad \boldsymbol{\delta_2} = \frac{a_\mathrm{b}}{2}\left(1,-\sqrt{3}\right), \quad \boldsymbol{\delta_3} = a_\mathrm{b}\left(-1,0\right).$$

In reciprocal space (fig. 1.3(b)), the first Brillouin zone is defined by the reciprocal lattice vectors

$$\boldsymbol{b_1} = \frac{2\pi}{3a_\mathrm{b}}\left(1,\sqrt{3}\right), \quad \boldsymbol{b_2} = \frac{2\pi}{3a_\mathrm{b}}\left(1,-\sqrt{3}\right)$$

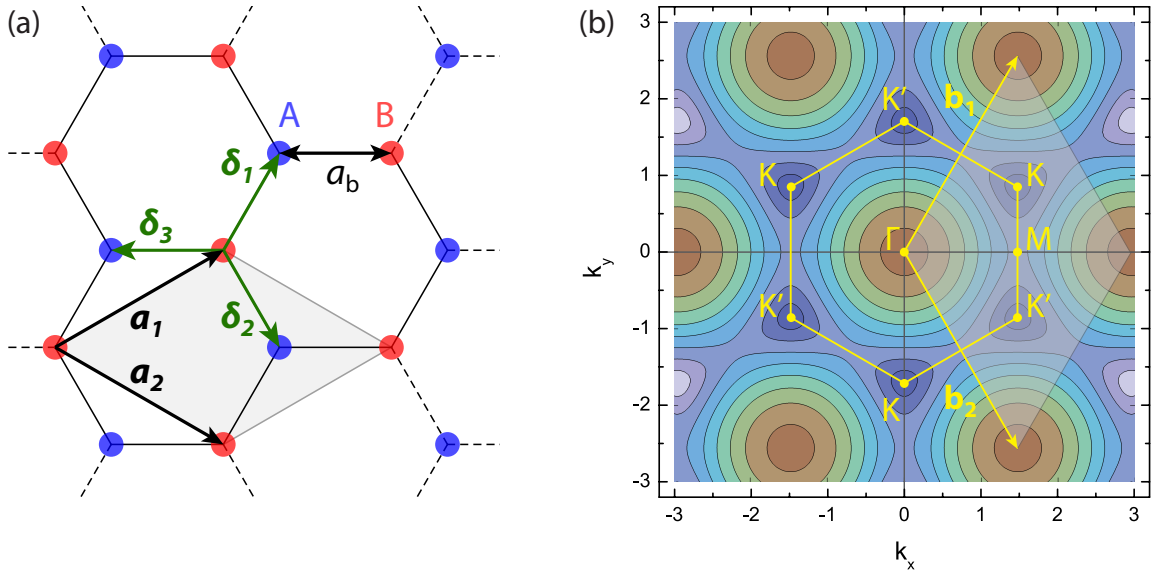

Figure 1.3: (a) The hexagonal graphene lattice consists of two sublattices A (blue) and B (red), separated by $a_\mathrm{b} \approx 1.42\,\text{Å}$. The lattice vectors $\boldsymbol{a_1}$ and $\boldsymbol{a_2}$ span the elementary unit cell (here shaded in gray). $\boldsymbol{\delta_i}$ are the nearest-neighbor vectors. (b) Contour plot of the conduction band. The inequivalent $\boldsymbol{K}$ and $\boldsymbol{K'}$-points reside at the corners of the first Brillouin zone. The reciprocal unit cell is indicated in light shading.

leading to a hexagonal structure just like in the real space lattice. The two inequivalent corners of the first Brillouin zone

$$\boldsymbol{K} = \left(\frac{2\pi}{3a_\mathrm{b}}, \frac{2\pi}{3\sqrt{3}a_\mathrm{b}}\right), \quad \boldsymbol{K'} = \left(\frac{2\pi}{3a_\mathrm{b}}, -\frac{2\pi}{3\sqrt{3}a_\mathrm{b}}\right)$$

are called Dirac points. Electronic transport in graphene is mainly governed by the charge carriers close to these points.

1.2.2 Ripples and corrugations

Before the discovery of graphene, it was believed that perfect crystals could not exist in two-dimensional space, since they would collapse at finite temperatures due to thermal fluctuations[32,33,43,44]. However, TEM measurements of freely suspended graphene flakes revealed that graphene is not perfectly two-dimensional but exhibits small corrugations or ripples in the third dimension.[34] The out-of-plane deformations extend up to $\sim 1\,\mathrm{nm}$ and provide structural stability for the membrane. The rippling can also be observed extenuated in bilayer graphene and disappears completely in bulk graphite. For an artistic representation of these corrugations, see fig. 1.4. In scanning tunneling microscopy (STM) measurements of graphene on SiO_2 in ultrahigh vacuum (UHV), variations in height on the order of 1 nm were found as well.[45] Since comparable roughness also appeared in the plain SiO_2 surface, the authors suggest the graphene film may simply be following the substrate roughness, at least partially. These findings were also verified in scanning-probe experiments with atomic-resolution STM.[46] The authors claim that in most experiments, resist residues have an impact on the corrugations and may prevent the graphene from assuming its intrinsic shape. More recent STM and atomic force microscopy (AFM) measurements of graphene on SiO_2 indicate the additional existence of corrugations is caused by intrinsic rippling of graphene.[47,48] However, when deposited on an atomically flat substrate such as mica or hexagonal boron nitride, even those intrinsic corrugations are completely suppressed.[49,50]

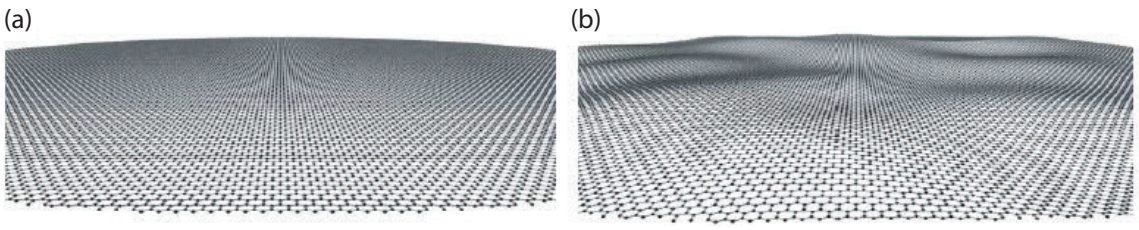

Figure 1.4: Artistic representation of (a) flat and (b) corrugated graphene. The ripples in (b) are $0.5\,\mathrm{nm}$ in height with a lateral size of $5\,\mathrm{nm}$. *Source: adapted from*[34].

1.3 Band structure

The energy dispersion of graphene can be described by a tight-binding approximation. In this approach, we assume that coupling takes place only between nearest and next-nearest neighboring atoms. The Hamiltonian for this problem is given by [38]

$$H = -t \sum_{\langle i,j\rangle,\sigma} \left(a^{\dagger}_{\sigma,i} b_{\sigma,j} + \text{H.a.} \right) - t' \sum_{\langle\langle i,j\rangle\rangle,\sigma} \left(a^{\dagger}_{\sigma,i} a_{\sigma,j} + b^{\dagger}_{\sigma,i} b_{\sigma,j} + \text{H.a.} \right), \tag{1.1}$$

where $a^{\dagger}_{\sigma,i}$ ($a_{\sigma,j}$) creates (annihilates) an electron with spin σ on sublattice A, and equally for the Hermitian adjoint (H.a.). The mechanism works similarly for $b^{\dagger}_{\sigma,i}$ and $b_{\sigma,j}$ in sublattice B. Traveling between sublattices requires the nearest-neighbor hopping energy $t \approx 2.8\,\text{eV}$. The value of the next nearest-neighbor hopping energy t' usually is assumed $t' \approx 0.1t$. Two energy bands can be derived from the Hamiltonian: [27]:

$$E_{\pm}(\boldsymbol{k}) = \pm t\sqrt{3 + f(\boldsymbol{k})} - t' f(\boldsymbol{k})$$

with

$$f(\boldsymbol{k}) = 2\cos\left(\sqrt{3}k_y a_{\text{b}}\right) + 4\cos\left(\frac{3}{2}k_x a_{\text{b}}\right) 4\cos\left(\frac{\sqrt{3}}{2}k_y a_{\text{b}}\right).$$

Positive solutions of E apply for the conduction ($\pi^{\star}$) band and negative for the valence (π) band, under the assumption of electron and hole symmetry. In fig. 1.5 the band structure is plotted for the even more simplified nearest-neighbor tight-binding approach ($t' = 0$) for $|\boldsymbol{k}| \leq a$. As can be seen from the plot, the conduction and valance band touch at the six corners of the first Brillouin zone (Dirac points). In the vicinity of these points (e.g. for low energies $|E| \lessapprox 1\,\text{eV}$) the dispersion relation can be approximated by assuming linear expansion; it then has the the shape of a cone (fig. 1.5(b)). The energy states now can be described as [51]

$$H\Psi = \hbar v_{\text{F}} \begin{pmatrix} 0 & k_x - ik_y \\ k_x + ik_y & 0 \end{pmatrix} \Psi = E\Psi$$

with the linear (rather than quadratic) energy momentum relation

$$E_{\pm} = \pm\hbar v_{\text{F}} |\boldsymbol{k}|.$$

Here, $v_{\text{F}} = \sqrt{3}ta_{\text{b}}/2\hbar \approx 10^6\,\text{ms}^{-1} \approx c_0/300$ is the Fermi velocity, and the positive (negative) solution corresponds to the conduction (valence) band. Hence, charge carriers in graphene behave as if they were massless Dirac fermions. This opens up the possibility to observe quantum electrodynamic effects at much slower speeds, such as the anomalous integer quantum Hall effect [52,53] and Klein tunneling [54,55].

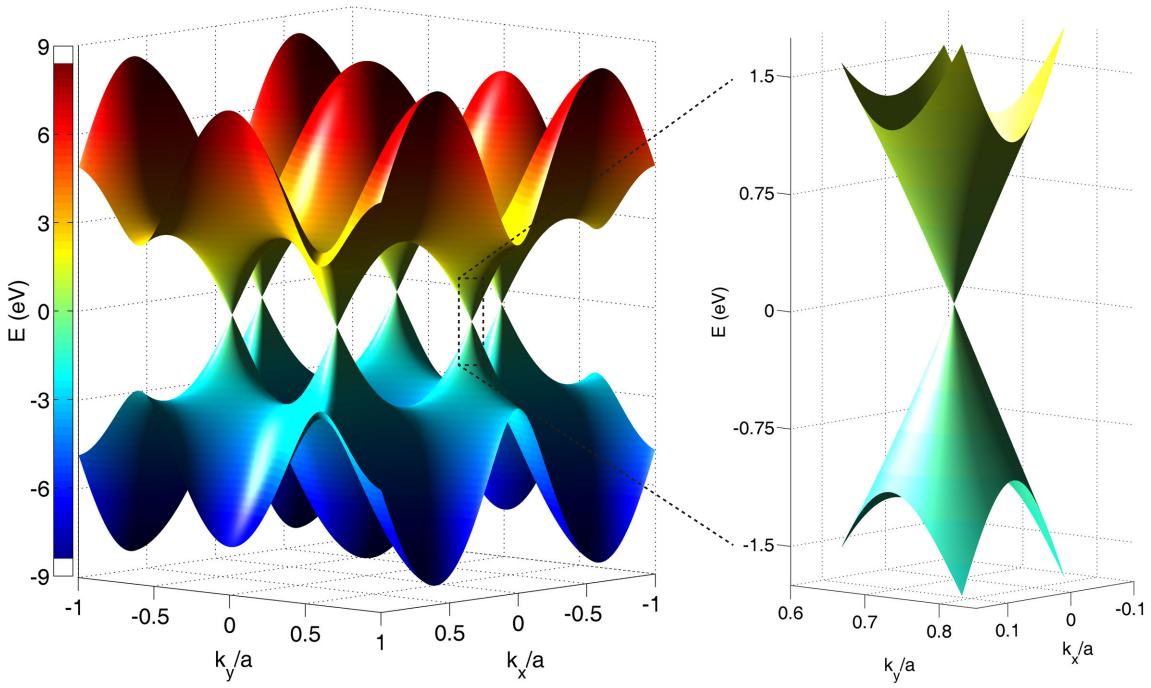

Figure 1.5: Nearest-neighbor tight-binding approximation of graphene's band structure. Conduction and valence band touch at the Dirac points. The colors represent the energy level whereas the shading only serves as improved visual presentation and has no physical meaning. On the right hand side, a zoom-in to one of the Dirac cones is shown. The dispersion relation expands linearly for Fermi energies smaller than $|E| \lessapprox 1\,\mathrm{eV}$.

Minimum quantum conductivity

Apart from the band structure, eq. 1.1 can also deliver the density of states (DOS) per unit cell. For small energies $|E| \ll |t|$ and considering only nearest-neighbor hopping ($t' = 0$), the DOS simplifies to

$$\rho(E) = \frac{g_\mathrm{s} g_\mathrm{v} |E|}{2\pi\hbar^2 v_\mathrm{F}^2}, \tag{1.2}$$

where g_v is the double valley degeneracy due to the two Dirac points at K and K', and $g_\mathrm{s} = g_\mathrm{v} = 2$ is the double spin degeneracy. Hence in the energy range considered here, the DOS is proportional to the energy and vanishes at the Dirac point (see fig. 1.6). Intuitively, with vanishing charge carriers one would expect the conductivity to vanish as well. However, at zero energy (no external electric field in undoped graphene) the conductivity remains finite. This phenomenon is referred to as quantum-limited conductivity.[39] At zero density of states, propagating states vanish and electronic transport is realized through evanescent

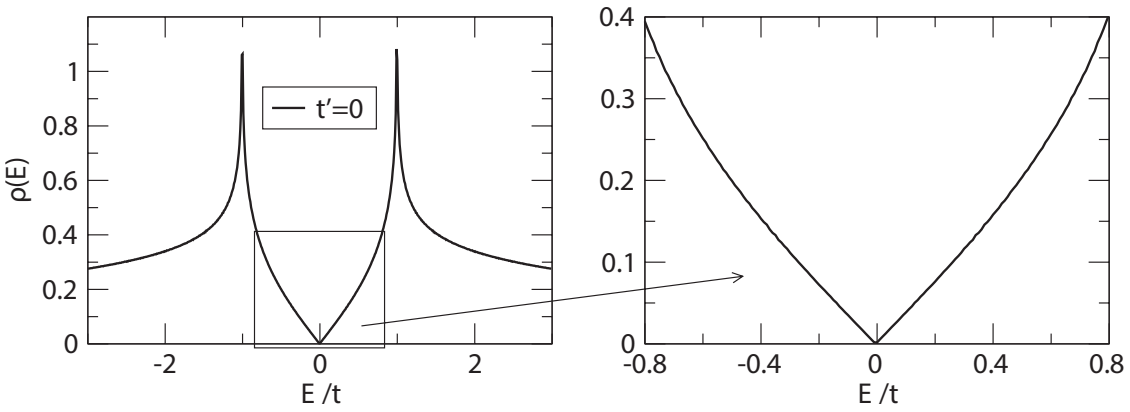

Figure 1.6: Density of states $\rho(E)$ in units of t for $t' = 0$. For low energies ($|E| \lessapprox 1\,\mathrm{eV}$) the DOS expands linearly: $\rho(E) \sim |E|$, refer to eq. 1.2. *Source: adapted from*[38].

states only.[56] This mechanism accounts for a ballistic minimum conductivity

$$\sigma_{\min} = \frac{4e^2}{\pi h}$$

provided that $w \gg l$, where w is the width and l the length of the device. In most experiments however, conductivity did not drop below[26]

$$\sigma_{\min} = \frac{4e^2}{h}.$$

The reason for the finite conduction at the charge neutrality point is found in the formation of electron-rich and hole-rich regions, so called "charge puddles".[57] These potential variations enable residual conduction even in totally undoped graphene samples. With rising temperature, this inhomogeneous charge distribution is "smeared out" leading to a large minimum conductivity at room temperature.[58] The non-vanishing conductivity is the main reason for large off-currents in graphene field-effect devices.

1.4 Electronic transport in graphene

The electric field effect describes the ability to modulate a material's electrical conductivity through the application of an external electric field. In normal metals, the electric field is screened at distances of $< 1\,\mathrm{nm}$ to the surface. The induced charges play no significant role compared to the amount of free charge carriers available in the bulk. However, due to the 2D nature of graphene and the resulting absence of screening, it shows a very pronounced, ambipolar electric field effect. Charge carriers can be changed from electrons to holes by variation of the gate voltage which in turn tunes the Fermi level. A negative gate voltage shifts the Fermi level to the valence band by p-doping the graphene, leading to hole conduction (see fig. 1.7(a)). For positive gate voltages, the effect is reversed accordingly. The electric

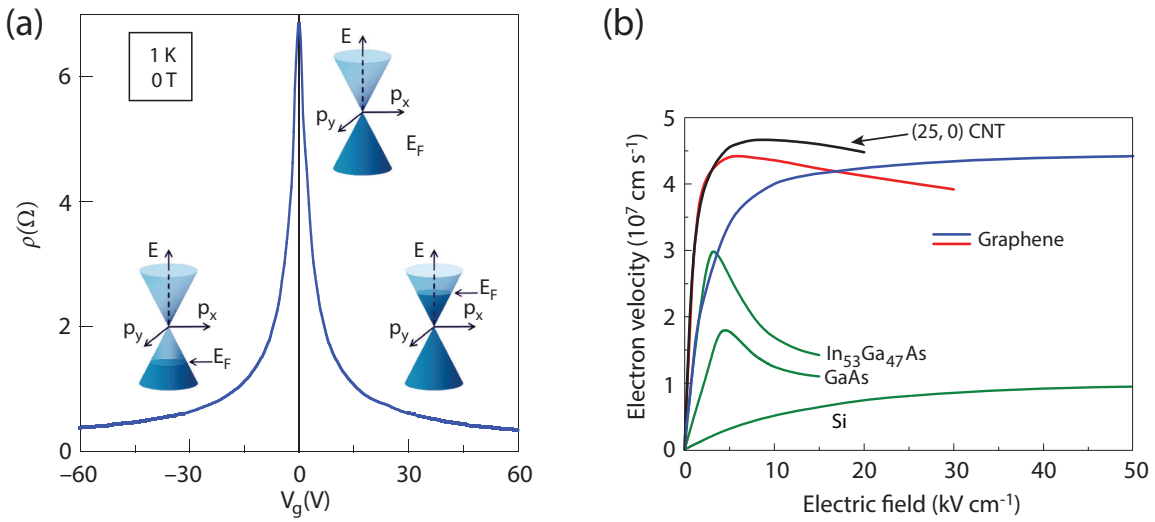

Figure 1.7: (a) Ambipolar electric field-effect in undoped graphene. An external electric field perpendicular to the graphene, induced by a gate voltage V_g, is used to tune the Fermi energy from hole to electron conduction (with increasing gate voltage). (b) With increasing electric field, the electron drift velocities of graphene and CNT (simulations) decay much slower than in semiconducting counterparts. *Source: (a) adapted from*[26]*, complemented, (b) adapted from*[11].

field is usually applied by a local, metallic gate electrode or by using the substrate as a back gate, separated from the graphene by a dielectric material or air in the case of suspension. The graphene-dielectric-gate stack acts as a capacitor with capacitance

$$C_g = \frac{Q}{V_{gs}} = \frac{\varepsilon_0 \varepsilon_r A}{t_{diel}}. \tag{1.3}$$

$Q = en_{2D}A$ is the capacitor charge, A the total surface, ε_0 the vacuum permittivity, V_{gs} the gate voltage and t_{diel} the thickness of the dielectric layer with dielectric constant ε_r. The charge carrier density can be obtained by transformation of eq. 1.3:

$$n_{2D} = \frac{Q}{eA} = \frac{D}{e} = \frac{\varepsilon_0 \varepsilon_r}{et_{diel}} V_{gs} = \alpha V_{gs}.$$

Hence, the charge carrier concentration depends linearly on the gate voltage allowing values of $n \sim 10^{13}\,\mathrm{cm}^{-2}$ before reaching dielectric breakdown. With decreasing electric field strength, the resistivity of a graphene sheet increases steadily until it reaches its maximum at the charge neutrality (Dirac) point. Here, the Fermi level resides exactly at the intersection of valence and conduction bands, leading to vanishing carrier concentrations n.

Without extrinsic disorder, intrinsic charge carrier mobilities greater than $200{,}000\,\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ at room temperature have been predicted.[59] One of the reasons for these exceptionally high values is the extremely weak electron-phonon scattering in graphene. Due to the suppressed phonon cooling, the charge carriers dissipate energy mostly through electron-electron interactions, hence transport takes place in the "hot electron regime". Clean Si/SiO_2-based graphene

devices exhibit mobilities in the order of $\sim 15{,}000\,\mathrm{cm^2V^{-1}s^{-1}}$ [26] with an intrinsic limit to values below $40{,}000\,\mathrm{cm^2V^{-1}s^{-1}}$ [60]. When placed on an atomically flat substrate such as hexagonal boron nitride, mobilities of up to $100{,}000\,\mathrm{cm^2V^{-1}s^{-1}}$ [42,50] were reached while a record mobility of $200{,}000\,\mathrm{cm^2V^{-1}s^{-1}}$ at 4 K was found in suspended graphene [10], where acoustic phonons represent the main scattering mechanism. However, these exceptional values were obtained at ideal conditions in ultra-clean samples. When preparing samples under normal conditions there are several factors reducing the mobility, e.g. local structural defects, molecules adsorbed by the graphene, or impurity charges from the dielectric and/or substrate. These residual impurity charge carriers accumulate to a charge carrier concentration which can easily reach values of $n_0 \sim 10^{12}\,\mathrm{cm^{-2}}$ for Si/SiO_2 substrates, leading to a shift of the Dirac point and a widening of the σ_{min} plateau at room temperature. [61] The shifting of the charge neutrality point to V_{Dirac} due to external doping of the graphene has been taken into account when deriving the charge carrier density:

$$n_{2\mathrm{D}} = \alpha\,(V_{\mathrm{gs}} - V_{\mathrm{Dirac}})\,.$$

When the electric field is applied through a local top or bottom gate, the mobility is usually reduced substantially by charged impurities inherent to the gate dielectric. Typical mobilities for locally gated graphene field-effect devices are in the order of $\sim 1{,}000\,\mathrm{cm^2V^{-1}s^{-1}}$. [19,62,63] The field-effect mobility can be extracted from two-terminal measurements using [11]

$$\mu_{\mathrm{FE}} = \frac{l_{\mathrm{ch}} g_{\mathrm{m}}}{w_{\mathrm{ch}} C_{\mathrm{g}} V_{\mathrm{ds}}}.$$

C_{g} is the gate capacitance, which usually is approximated as described in equation 1.3. At low density of states, the filling (high-energy states) and emptying (low-energy states) of the electronic bands alters the gate capacitance in a way that it seems as if there was a second capacitance in series. This capacitance is referred to as quantum capacitance C_{q} and may dominate the total gate capacitance

$$C_{\mathrm{g},q} = \frac{C_{\mathrm{q}} \cdot C_{\mathrm{g}}}{C_{\mathrm{q}} + C_{\mathrm{g}}}$$

when very thin gate dielectrics are used. Ignoring the quantum capacitance may lead to underestimation of the mobility. [11]

In transistors with very short gate lengths operating at electric fields of $10\,\mathrm{kV\,cm^{-1}}$ or more, the carrier mobility is not the main contributor to the device performance any more. Instead, the electron drift velocity v_{drift} may serve as alternative figure of merit. The high field drift velocity is given by the empirical approximation

$$v_{\mathrm{drift}} = \frac{\mu_{\mathrm{LF}} E}{\sqrt[n]{1 + \left(\frac{\mu_{\mathrm{LF}}|E|}{v_{\mathrm{sat}}}\right)^n}}$$

where μ_{LF} is the low field mobility and n is a fitting parameter. [64] After reaching velocity saturation at rather low electric fields, the drift velocity decays much slower with increasing field

in graphene than in common semiconductors, as suggested by simulations, see fig. 1.7(b).[11]

1.5 Metal-graphene junctions and contact resistance

When performing electronic transport measurements, graphene is usually connected by metal leads. The choice of the right metal at this contact/graphene interface is of great importance since it affects the contact resistance R_c which considerably impacts the device performance. Being able to control the contact properties is argued to be more favorable than achieving a high charge carrier mobility.[65,66] Currently however, theory and experiments do not explain conclusively which parameters affect the contact resistance.

DFT calculations by Giovanetti et al. showed that metals leading to strong bonding (chemisorption) of graphene (Co, Ni, Pd, Ru, Ti etc.) severely alter its electronic band structure due to the high binding energy $\Delta E \sim 0.1\,\mathrm{eV}$ per C atom.[67] Metals with low binding energy $\Delta E \leq 0.04\,\mathrm{eV}$ (Al, Ag, Au, Cd, Cu, Ir, Pt etc.) leading to weak bonding (physisorbtion) cause only small alterations in the band structure. In both cases however, the metal contacts shift the Fermi level, effectively doping the graphene, depending on the work function difference between metal ϕ_M and graphene ϕ_G

$$\Delta E_F = \phi_M - \phi_G.$$

However, determining the work function of graphene itself is not unambiguous as it depends on the charge carrier density. It ranges from $\phi_G \sim 4.5\,\mathrm{eV}$ for undoped graphene to roughly $4.8\,\mathrm{eV}$ in the presence of an electric field.[68] Also, the charge transfer region is not limited to the area below the metal contacts but extends far into the graphene channel region due to low DOS close to the Dirac point.[69]

Giovanetti et al. as well as the majority of successive studies concluded that a high work function difference has a reducing effect on the contact resistance.[65,70,71,72,73] Drawbacks are an increased amount of charge transfer and the formation of a p-n junction in the channel region.[65]

In 2010 the contact resistance in graphene was determined experimentally for the first time by Russo et al.[71] The authors measured $R_c = 800 \pm 200\,\Omega\mu\mathrm{m}$ and found that R_c consists of two parts: One part independent of the gate voltage, temperature and number of layers and a second, gate dependent part. The dominant, gate-voltage independent part is believed to be caused by charge transfer initiated at the metal/graphene interface shifting the Fermi level away from the Dirac point. Charge transfer in graphene is unique due to its 2D nature. Experiments suggest that the contact resistance depends on the width of the graphene sheet rather than on its area.[65] Thus, charge carrier injection may take place preferably at the graphene/metal edges. Also, the charge carrier injection from a 3D metal contact into the 2D graphene is impeded because of charge transfer doping.

The theoretical minimum value in an ideal metal–graphene junction is $40\,\Omega\mu\mathrm{m}$.[74] Record minimum contact resistances of $200\,\Omega\mu\mathrm{m}$ were reported for untreated monolayer graphene[63], in contrast to state-of-the-art silicon metal–oxide–semiconductor field-effect transistors (MOSFET) with R_c as low as $80\,\Omega\mu\mathrm{m}$[12]. With the same contact materials (a stack of Ti/Pd/Au), in another study a contact resistance of $\approx 350\,\Omega\mu\mathrm{m}$ was reached[75], while a third study

found $\approx 750\,\Omega\mu m$ [66], indicating that other parameters such as the pressure of the metal evaporator [71] or the graphene interface quality [63] may affect the contact resistance. In the last study it was shown that depending on the choice of contacting metal, a tenfold decrease in R_c is possible[1]. The contact resistances reported in previous studies show a large variation ranging from $100\,\Omega\mu m$ to $> 100{,}000\,\Omega\mu m$. A reason for this spread in R_c is the different level of contamination present in graphene. Several methods for decreasing the contact resistance were reported in the literature:

Post annealing procedures and cleaning by scanning with an AFM tip in contact mode [76] provide countermeasures for unwanted contamination (e.g. resist residues).

Franklin et al. found that contacting graphene from both sides (top and bottom) leads to a substantial decrease in contact resistance compared to usual top or bottom contacts. [77] Using Ti/Pd contacts they were able to reduce contact resistance by $\geq 40\,\%$, improving transconductance by $\geq 30\,\%$ while passing larger currents through their graphene FETs. The additional layer of metal enables stronger doping of graphene and improves the effective graphene-metal coupling. The improvements due to the second metal contact are more pronounced far away from the Dirac point.

In a theoretical work Matsuda et al. suggest "end-contacting" graphene at the edges could lead to a noticeable reduction in contact resistance. [78] This hypothesis was verified by multiple studies, in which graphene was introduced to artificial defects by chemical etching to enable edge contacting. Robinson et al. etched a graphene sheet in the area under the contacts with a low-power oxygen etch treatment (*ashing*) followed by annealing at $\sim 450\,°C$. [79] They claim to obtain a 6000-fold improvement in contact resistance compared to untreated graphene. Leong and coworkers used Ni particles as metallic catalyst to etch nano-pits into the contact region of graphene, creating end-contacted graphene edges. [80] They report record minimum contact resistances of $100\,\Omega\mu m$ for monolayer and $11\,\Omega\mu m$ for bilayer graphene. By patterning (etching) the graphene underneath the contacts, Smith and coworkers maximized the edge-contacted region, decreasing R_c by more than $20\,\%$ compared to non-patterned graphene. [81] While varying the width of the cuts they found that patterning the graphene is always beneficial however for distances of 40 nm or less between the cuts, the positive impact begins to decline. Another advantage of this technique is the reduction in spread of the contact resistance that leads to better device consistency.

1 Using a stack of Ti (0.5 nm)/Pd (20 nm)/Au (40 nm) they reached $\approx 750\,\Omega\mu m$, whereas a stack of Ti (5 nm)/Au (50 nm) yielded $\approx 7500\,\Omega\mu m$.

2 Graphene field-effect transistors

Transistors can be used to switch or amplify electrical signals and thus are by far the most important elements of electronic circuits. Bipolar junction transistors (BJT), the first mass-produced transistor type[1], are current controlled and suffer from low input impedances and slow switching times. These drawbacks were reduced by voltage controlled field-effect transistors (FET). In FETs, a voltage applied between gate and source electrodes induces an electric field into the channel region, tuning the charge-carrier density and thereby the conductivity. A schematic explaining the working principle of FETs is given in fig. 2.1(a). The speed of a FET is inversely proportional to the time charge carriers travel below the gate electrode. Therefore, to reach the lowest possible switching times, the length of the gate has to be minimized and a channel material with high charge-carrier velocity is needed. The latter requirement is met by carbon nanotubes and graphene, whose carrier velocities supersede that of many materials currently used in commercial FETs. As the charge-carrier

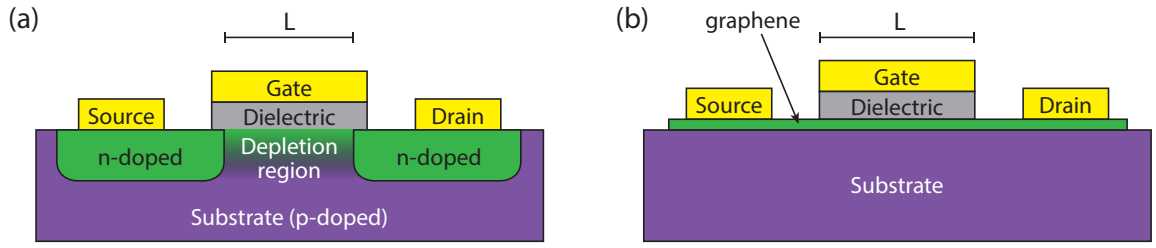

Figure 2.1: (a) Schematic of a n-type semiconductor-based field-effect transistor. It is a unipolar device and thus limited to one type of charge carriers (here electrons). In the region of the ohmic source and drain contacts (yellow) the substrate is heavily n-doped. A gate electrode deposited on top of a dielectric material between the doped regions can be used to apply an electric field to the depletion region below. For gate-source voltages above a certain threshold value, a channel is formed in the depletion region, enabling a drain-source current as a function of the gate voltage. (b) In graphene FETs, a graphene sheet is contacted by source and drain electrodes, forming a continuous channel. Doping parts of the substrate as in semiconductor-based FETs is not necessary. Either a single (semi-) insulating substrate is used to support the graphene, or a combination of a thin insulating layer and a conductive substrate (e.g. SiO_2/Si) which in turn can be used as a global back gate to bias the graphene. Just like in conventional FETs, modulating the gate voltage controls the conductivity of the channel. However, the channel of GFETs is ambipolar allowing both n-type or p-type conduction depending on the gate voltage.

1 Historically, the first type of transistor invented was the field-effect transistor patented in 1925 and experimentally realized in 1947, shortly before the bipolar junction transistor in 1948. Still, BJT were the most popular transistors until the late 1960s due to simpler and less expensive production methods.

density and thus the conductivity in these carbon allotropes can be varied by an external electric field (as discussed in chapter 1.4 for the case of graphene), they can be used directly as the channel material in FETs. Different than for semiconductor-based channels, local doping of the substrate is not required. The differences between classical and graphene FETs are depicted in fig. 2.1.

Classical FETs utilize semiconducting channels, therefore they are unipolar allowing only one type of carriers (usually n-type). Due to the ambipolarity of the electric field effect in graphene, GFETs can be switched from n-type to p-type conduction just by tuning the gate voltage.

Historically, the first carbon-based field-effect transistors operating at high frequencies were realized with carbon nanotubes.[3] In the first approaches, single CNT were used as the FET channel.[3,7] While CNTFETs offer substantial on/off current ratios, due to the limited dimensions of the tubes they suffer from low drain currents and high impedances, much larger than required by typical circuits and the measurement setups. The aforementioned issues can be solved partially by arranging multiple CNT in an array, enabling scaling of the device dimensions. Even though this procedure imposes new challenges such as accurate separation and high-density parallel alignment of the CNTs, CNTFETs reaching intrinsic transit frequencies in the GHz range[4,5,6,8] with the current record at $f_T = 153\,\mathrm{GHz}$[8] were realized lately.

First graphene field-effect devices were realized using a 300-nm layer of SiO_2 as dielectric and the Si substrate as global back gate.[9] To overcome the inherent problems of parasitic capacitances and the lacking ability to locally gate the graphene, the next generation of devices was fabricated with local top or bottom gates, as depicted in fig. 2.1(b).[82]

Soon after the presentation of radio frequency (RF) CNTFETs, the first graphene field-effect transistor operating at GHz frequencies emerged.[17] Due to the "graphene goldrush" sparked by the famous 2004 paper by K. Novoselov and A.K. Geim[9], progress in RF GFET research advanced very fast. Reduction of device dimensions, especially the gate length, as well as improving the cleanliness of the graphene and the use of more suitable substrates were the key enhancements leading to these advancements. High-frequency graphene FETs have been fabricated from manually exfoliated[17,18,20,22,62,83], CVD grown [84,85,86,87,88] and epitaxial graphene[19,89,90,91], but none of these fabrication methods sticks out to be clearly superior.

Due to fast and efficient optimization, the maximum transit frequency of GFETs was increased from initially 14.7 GHz[17] to 427 GHz[22] within less than five years. The most important results are compiled in fig. 2.6 table 2.1 at the end of this chapter. Through the availability of high quality large scale graphene, the issues of scalability could be overcome. Still, GFETs suffer from the lack of a bandgap in graphene and the resulting weak current saturation.

In the following the peculiarities of graphene field-effect transistors are discussed, as well as their differences and advantages over classical, semiconductor based FETs. Special attention is paid to the design and characterization of high-frequency graphene-based devices. For further information, the review papers of F. Schwierz[11,13] are recommended.

2.1 Comparison of graphene FETs to classical MOSFETs

Due to its remarkable properties, graphene often is predicted to play a big role in high-frequency devices.[11,13,21,92] Already in 2009, graphene was included in the emerging research materials section of the International Technology Roadmap for Semiconductors (ITRS).[12] However, digital logic components are very sophisticated and completely fixed to Si-based processes - changing the base material would require extensive adjustments. Also, to be considered a silicon replacement, graphene would have to offer on/off current ratios $> 10^4$. The $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio is below 20 for typical GFETs due to finite conductivity at the charge neutrality point and the lack of a band gap.[11,58] FETs made from bilayer graphene could offer one order of magnitude higher on/off current ratios.[93] Given present limitations, instead of a replacement for silicon, graphene will rather become a complementation, e.g. for transparent[94], flexible[95], or printable electronics in niche products.[13] However, since processing graphene is compatible with silicon technology, it may be favored over silicon-incompatible III-V high electron mobility (HEMT) technology currently leading in terahertz (THz) applications.

Without overcoming the issue of low on/off current ratios, graphene will not be suitable for digital logic devices. Analog and radio-frequency applications, on the other hand, are within reach, as here switching capabilities are not a necessity. Small-signal amplifiers for example operate while the transistor is in the on-state. The main benefits of graphene are its extremely high charge carrier mobility and saturation velocity (refer to chapter 1), and the fact that it is atomically thin. Theoretically, thin-channel materials should suffer less from so called short-channel effects[96] which arise when scaling the channel length. Apart from that, using graphene the total device thickness can be reduced dramatically and creating heterostructures is facilitated.

2.2 DC characterization of graphene FETs

The performance of electronic devices can be approximated using a small-signal equivalent circuit. Fig. 2.2 depicts a commonly used simplified circuit containing the most important parameters to represent a RF FET. The complete circuit including all extrinsic and intrinsic parameters is discussed in more detail in the appendix, chapter A.7. In this representation, the FET is operated in common-source mode. All potentials are referred to with respect to the source, which usually resides on the ground potential. The response of the transistor can be characterized by a drain current, dependent on the gate voltage V_{gs} and drain voltage V_{ds}

$$I_{\mathrm{ds}}\left(V_{\mathrm{gs}},V_{\mathrm{ds}}\right) = g_{\mathrm{m}}V_{\mathrm{gs}} + g_{\mathrm{ds}}V_{\mathrm{ds}},$$

where g_{m} is the transconductance and g_{ds} the drain conductance. The transconductance describes how effective the gate voltage modulates the drain current. It is defined as the partial derivative of I_{ds} with respect to V_{gs}

$$g_{\mathrm{m}} = \left.\frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{gs}}}\right|_{V_{\mathrm{ds}}=\mathrm{const}}$$

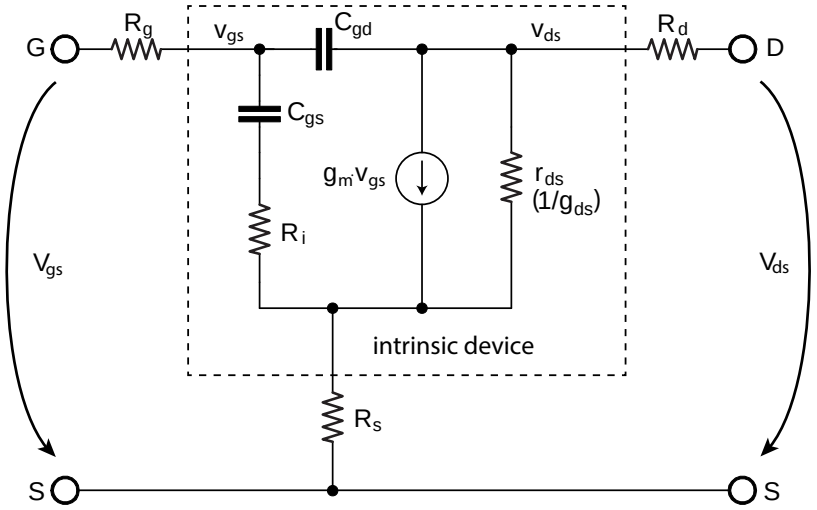

Figure 2.2: Simplified small-signal equivalent circuit for a FET in common-source mode operating at microwave frequency. It is composed only of passive (linear) elements RC and current/voltage sources. The area within the dashed rectangle represents the bias dependent elements of the intrinsic transistor. It consists of the capacitances C_{gs} and C_{gd} which result from the channel/dielectric capacitance, a current source producing the drain current $i_{\mathrm{ds}} = g_{\mathrm{m}} v_{\mathrm{gs}}$, and the resistances R_{i} and r_{ds}. R_{i} accounts for the time required to charge/discharge the channel when following the modulation from the gate, while the drain conductance g_{ds} is defined as the inverse of r_{ds}. The bias independent external parameters of the circuit, consisting of the gate access resistance R_{g} as well as drain and source access/contact resistances R_{d} and R_{s}, can be obtained by performing a de-embedding procedure. This procedure and the complete version of the circuit above is discussed in the appendix, chapter A.7. *Source: after[13].*

at a given operating point (constant V_{ds}). Operating the transistor at the point of highest transconductance is most advantageous, as here a small change in gate voltage leads to a maximum change in drain current and hence to maximum current amplification.

When plotting drain current versus gate voltage $I_{\mathrm{ds}}\,(V_{\mathrm{gs}})$ in a so called *transfer characteristic* as shown exemplarily in fig. 2.3(a), the transconductance is represented by the slope of the curve. These transfer characteristics (also called gate sweeps) can be used to verify proper gate operation. Contrary to semiconductor FETs, the IV-transfer characteristics for graphene FETs is mirrored at the Dirac voltage, with the drain current increasing for both positive and negative voltages $V = V_{\mathrm{gs}} - V_{\mathrm{Dirac}}$. In undoped ideal graphene transistors, the Dirac point is located at $V_{\mathrm{Dirac}} = 0$. When the graphene is doped (e.g. by charge traps in the dielectric) the Dirac point is shifted with respect to zero gate voltage.

During the first gate sweep only relatively small gate voltages are applied to prevent gate leakage or dielectric breakdown. For highly doped samples the sweep range has to be increased to be able to map the Dirac point. Most transfer characteristics measured under ambient conditions feature a pronounced hysteresis, as can be seen in fig. 2.3(b). While sweeping the gate voltage, charges trapped in resist residues or in the dielectric are reloaded causing the hysteresis. The curves from fig. 2.3(b) also exhibit an electron/hole asymmetry. Since

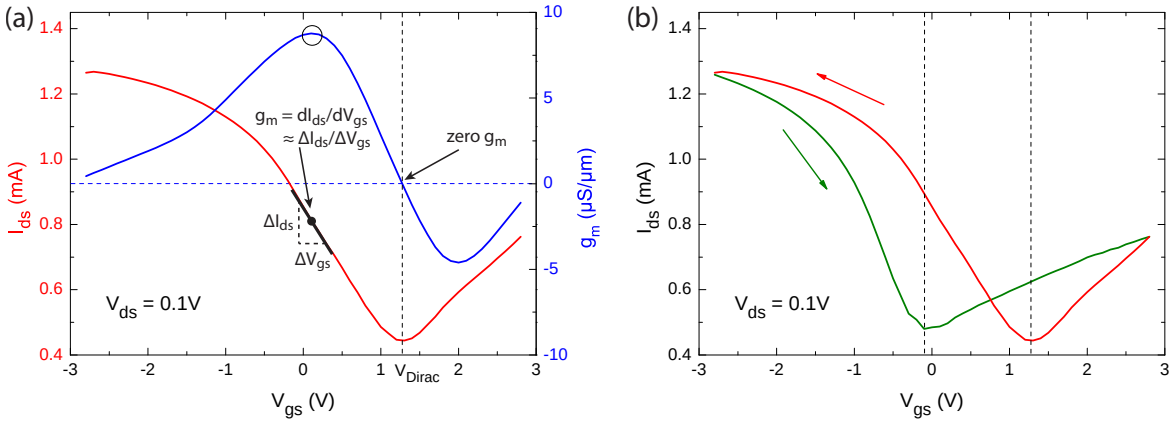

Figure 2.3: (a) Typical transfer characteristics (red curve) for one of our graphene FETs, measured at a fixed bias voltage $V_{\mathrm{ds}} = 0.1\,\mathrm{V}$. The channel is conductive for both negative and positive voltages $V = V_{\mathrm{gs}} - V_{\mathrm{Dirac}}$, with a minimum drain current at V_{Dirac}, corresponding to the Dirac point. The blue curve shows the transconductance, obtained from the partial derivative of I_{ds} with respect to V_{gs}. At $V_{\mathrm{gs}} \approx 0.2\,\mathrm{V}$ the point of highest transconductance is indicated exemplarily, corresponding to the steepest slope of the drain current curve. At this bias condition, maximum RF transistor performance is expected. Note the vanishing transconductance at the Dirac voltage V_{Dirac}. (b) Charge traps in the graphene/gate dielectric interface are responsible for a hysteresis observed in room-temperature measurements. The sweep direction is shown by colored arrows, and the corresponding Dirac voltages are indicated by dashed vertical lines. A strong asymmetry between hole and electron conduction can be observed.

in suspended graphene, electron and hole branches are symmetrical [10], the asymmetry has to be attributed to substrate-related effects. [97,98] Also, depending on the bias conditions, a pn-junction can form in the channel which increases the contact resistance leading to asymmetrical dc characteristics. [99]

Another useful form of representation is the *transport characteristic* diagram, where the drain current is plotted versus the drain voltage $I_{\mathrm{ds}}\,(V_{\mathrm{ds}})$ as depicted in fig. 2.4. In the following, only positive drain-source bias is discussed - for negative drain voltages the results are inversed due to graphene's ambipolarity. A typical transport curve is divided into four bias condition regions [11,13,17,63], as shown in fig. 2.4(1-4). At $V_{\mathrm{ds}} = 0$ (region 1), the Fermi level is constant throughout the n-type channel. In the second region where the drain voltage is still below the critical voltage $V_{\mathrm{ds,crit}}$, the drain current depends approximately linearly on the drain voltage, and the conduction is governed completely by electrons. With increasing V_{ds}, saturation begins to set in, and the charge carrier concentration decreases close to the drain electrode. Reaching the critical voltage $V_{\mathrm{ds,crit}}$ (region 3), the minimum charge carrier concentration resides at the drain side of the channel, creating a high-resistance "pinch-off" region. As the drain bias is further increased, the minimum carrier density moves into the channel, creating a *n-p*-junction. In this fourth, linear region, mixed potential conditions prevail, leading to simultaneous n- and p-type conduction at different positions within the channel due to the ambipolarity and the gapless nature of graphene.

In many devices however, the third and fourth region are not present or can not be reached

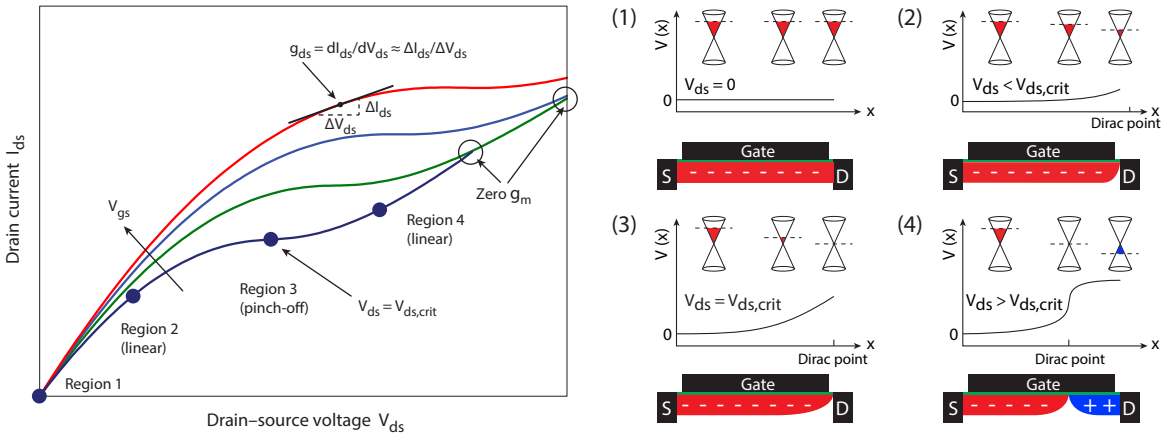

Figure 2.4: Typical transport characteristics of a GFET for positive drain-source voltages at positive gate-source voltages increasing from bottom to top. The curves consist of four regions schematically described on the right side (1-4). For each region, the channel bias conditions are indicated below the chart. Region (1): at zero drain bias, the Fermi level is constant throughout the channel, residing in the conduction band (electron conduction). (2) For drain-source voltages smaller than the critical voltage $V_{\mathrm{ds,crit}}$, the charge carrier density decreases at the drain end of the channel. (3) When $V_{\mathrm{ds}} = V_{\mathrm{ds,crit}}$, a pinch-off region is created at the drain side where the bias conditions are equal to those at the Dirac point. (4) For $V_{\mathrm{ds}} > V_{\mathrm{ds,crit}}$, the minimal density point shifts into the channel, leading to hole conduction close to the drain end of the channel and a second linear region emerges. Note that due to the pinch-off regions, curves measured at different gate-voltages may touch or cross leading to vanishing or even negative transconductance. *Source: (left) adapted from[11], complemented. (1-4) after[17,100].*

without risking dielectric breakdown. Even if the third region is present, its saturation usually is much weaker than in semiconductor based FETs.

The slope of the transport characteristic curve delivers the small-signal drain-source conductance (or *output conductance*), defined as the partial derivative of I_{ds} with respect to V_{ds} at a fixed operating point (constant V_{gs})

$$g_{\mathrm{ds}} = \frac{1}{r_{\mathrm{ds}}} = \left.\frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{ds}}}\right|_{V_{\mathrm{gs}}=\mathrm{const}} .$$

In classical MOSFET devices, g_{ds} becomes small once the saturation regime is reached. In graphene however, due to the absent or only weak current saturation, g_{ds} remains relatively large even at high drain bias. The lowest output conductance values reported so far were on the order of $< 0.1\,\mathrm{mS/\mu m}$. Complete current saturation is out of reach without opening a sizable bandgap in graphene. This could be achieved for example through lateral confinement by patterning a narrow graphene nanoribbon (GNR),[101] or by applying an electric field perpendicular to a bilayer graphene sheet[102,103]. However, all efforts to induce a bandgap so far lead to a reduction of mobility and other key properties.[13]

2.3 High-frequency graphene FET characterization

For characterization at microwave frequency, the GFET is biased at those V_{gs},V_{ds} conditions where the optimum transconductance was found in previously performed dc characteristics. A vector network analyzer (VNA) is used to superimpose ac signals on the dc gate and drain voltages (shown exemplarily in fig. 2.5). The variation of the gate voltage leads to a change in drain current that can be detected by the VNA through scattering parameter (S parameter) measurements. For the definition of scattering parameters and more information on vector network analysis, please refer to the appendix, chapters A.6 and A.7. The data acquisition is repeated while sweeping the frequency of the RF signal. For each bias condition, the VNA typically measures the S parameters at hundreds of predefined frequencies within the frequency band. The dc drain bias can be varied after each gate sweep, rendering a matrix of sets of S parameters. Each set fully describes the GFET's high-frequency characteristics, from which all relevant figures of merit (FOM, e.g. the transit frequency f_{T}) and parameters (e.g. g_{m}, R_{g}, C_{gs} etc.) can be extracted using the small signal equivalent circuit discussed in the previous sub-chapter.

The most important figures of merit describing the high-frequency performance of a FET are the transit frequency f_{T} and the maximum oscillation frequency f_{max}. These FOM specify up to which frequencies the transistor offers current and power gain, respectively. For practical applications, the transistor should be operated well below these limits. The transit frequency is defined as the upper-bound frequency at which the current gain $|h_{21}|$ reaches unity

$$h_{21}(f)|_{f=f_{\mathrm{T}}} = 1.$$

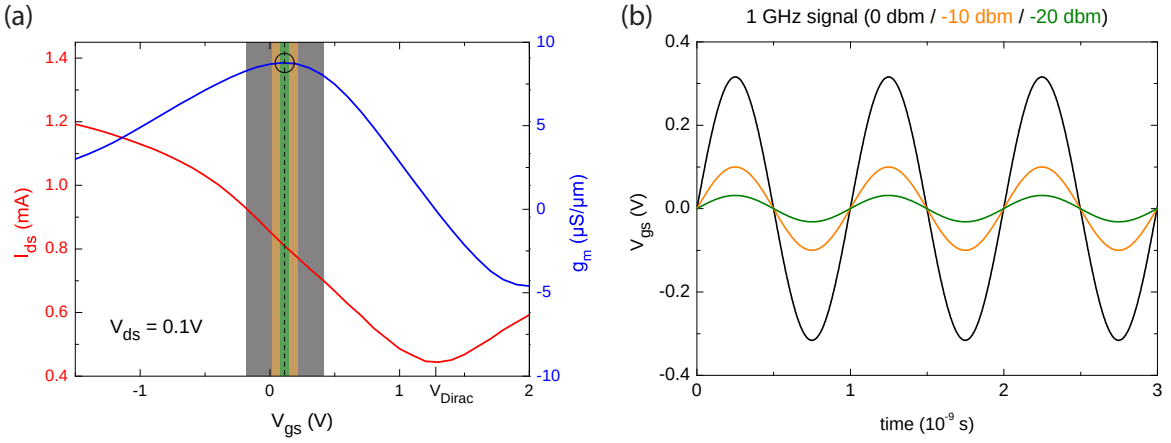

Figure 2.5: a) After dc-biasing the sample to the gate voltage corresponding to the maximum transconductance (here $V_{\mathrm{gs}} \approx 0.2\,\mathrm{V}$) a RF signal (shown in (b)) is superimposed. This RF signal modulates V_{gs} proportionally to the signal amplitude as indicated by the different colors in (a) and (b). Higher power levels reduce signal noise but may lead to non-linear response signal distortion (e.g. for $0\,\mathrm{dbm}$, black range in (a)).

In S parameter representation, the current gain can be expressed as

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}.$$

The extrinsic transit frequency can also be derived from the small-signal equivalent circuit introduced in the previous sub-chapter (fig. 2.2):

$$f_{\mathrm{T,\,ex}} = \frac{g_{\mathrm{m,in}}}{2\pi} \frac{1}{(C_{\mathrm{gs}} + C_{\mathrm{gd}})\left[1 + g_{\mathrm{ds,in}}\left(R_{\mathrm{s}} + R_{\mathrm{d}}\right)\right] + C_{\mathrm{gd}} \cdot g_{\mathrm{m,in}}\left(R_{\mathrm{s}} + R_{\mathrm{d}}\right)}, \tag{2.1}$$

where $g_{\mathrm{m,in}}$ and $g_{\mathrm{ds,in}}$ are the intrinsic transconductance and output conductance, respectively. The transit frequency of the intrinsic device, excluding all parasitic elements, is defined as

$$f_{\mathrm{T,in}} = \frac{g_{\mathrm{m,in}}}{2\pi} \frac{1}{C_{\mathrm{gs}} + C_{\mathrm{gd}}}.$$

Fig. 2.6(a) shows the intrinsic transit frequencies of state-of-the-art FETs made of graphene, CNT and classical semiconducting materials with respect to the gate length. The inverse proportionality of $f_{\mathrm{T,in}}$ to l_{g} can clearly be observed. In terms of transit frequency, graphene FETs are able to compete well with FETs based on other materials. For more information on select GFETs from fig. 2.6, please refer to table 2.1.

As can be seen from eq. 2.1, g_{m} needs to be maximized to reach high transit frequencies, while minimizing all remaining parameters of the small-signal model. The gate capacitances can be reduced by using shorter gates, enabling faster switching times. However, a reduction of the gate length decreases the transconductance especially for $l_{\mathrm{g}} < 200\,\mathrm{nm}$.[75]

The unilateral power gain U (also referred to as Mason's gain[104]) is a quantity invariant

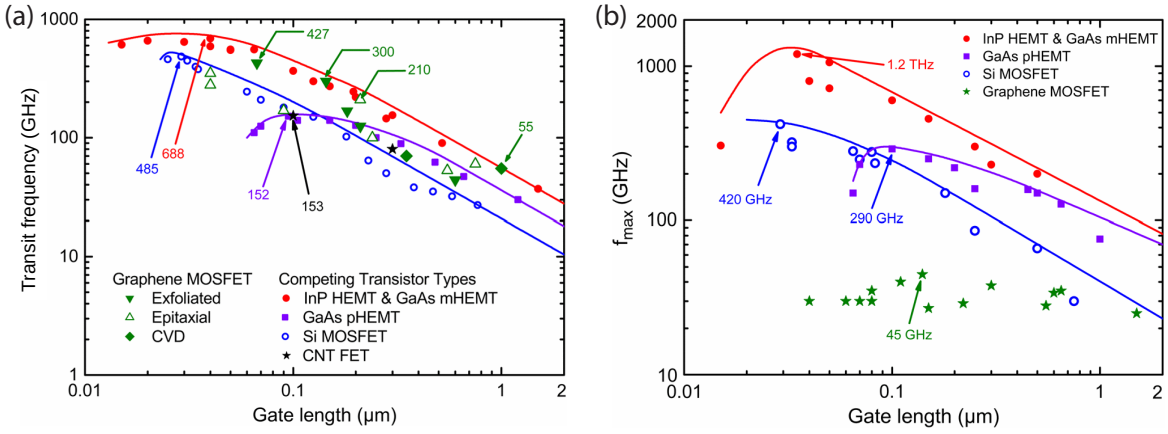

Figure 2.6: (a) Intrinsic transit frequencies $f_{\mathrm{T,in}}$ and (b) maximum oscillation frequencies f_{max} of state of the art graphene and semiconductor-based FETs. While graphene devices competes well with respect to $f_{\mathrm{T,in}}$, f_{max} values remain small and independent of the gate length due to the missing band gap and the resulting limited current saturation. *Source: adapted from*[13].

Author	[unit]	Meric et al.	Lin et al.	Lin et al.	Lin et al.	Liao et al.	Wu et al.	Cheng et al.	Feng et al.
Year		2008 [17]	2009 [18]	2010 [62]	2010 [19]	2010 [20]	2012 [21]	2012 [22]	2014 [24]
$f_{T,in}$	GHz	14.7	26	50	100	300	350	427	93
$f_{T,ex}$	GHz	-	-	-	-	2.4	10.5	-	-
$f_{T,in}/f_{T,ex}$		-	-	-	-	125	33.3	-	-
f_{max}	GHz	< 1	-	-	10	-	22	-	105
l_g	nm	500	150	350	240	144	40	67	100
w_{ch}	µm	2.5	-	27	30	~ 2	2×10	8	2×8
I_{ds}	mA/µm	0.19	-	0.3	-	3.3	-	3.56	2
C_{gs}	fF	5.95	-	38	14	2.2	-	-	5.29
C_{ds}	fF	-	-	-	-	0.2	-	-	4.47
C_{gd}	fF	-	-	-	-	0.2	-	-	5.29
R_s	Ω	100	-	-	-	2.4	-	-	9.63
R_d	Ω	-	-	-	-	13.9	-	-	10.83
R_g	Ω	-	-	-	-	157	-	-	2.23
g_m	mS/µm	0.22	-	-0.22	0.14	1.27	-	1.33	0.64
g_{ds}	mS/µm	-	-	-	-	-	-	-	0.65
substrate		Si/SiO_2	Si/SiO_2	Si/SiO_2	SiC	Si/SiO_2	SiC	Si/SiO_2	SiC
dielectric		HfO_2	$\mathbf{Al_2O_3}$	$\mathbf{Al_2O_3}$	Polymer+HfO_2	$\mathbf{Al_2O_3}$	$\mathbf{Si_3N_4}$	$\mathbf{Al_2O_3}$	$\mathbf{Al_2O_3}$
t_{diel}	nm	30	12	2+10	10+10	5	15	22	6
mobility	$cm^2s^{-1}V^{-1}$	105	< 400	2700	$900 - 1500$	-	3000	-	1170
graphene		exfoliated	exfoliated	exfoliated	epitaxial	exfoliated	epitaxial	exfoliated	epitaxial

Table 2.1: Comparison of the graphene field-effect transistors from recent publications. In all GFETs monolayer graphene is used.

under specific classes of transformations, making it an intrinsic device property and thus an ideal figure of merit.[104,105] U can be expressed in terms of S parameters

$$U = \frac{|S_{21} - S_{12}|^2}{\det(\mathbb{1} - SS^\star)}.$$

It is defined only for linear two-port devices connected as an amplifier[105], which represents a small limitation compared to similar device properties such as the maximum available gain. For state-of-the art devices, usually rather small values $U \gtrsim 1$ are reached. Another expression of U is its representation in terms of the stability factor k

$$U = \frac{|S_{21}/S_{12} - 1|^2}{2k\,|S_{21}/S_{12}| - 2\mathrm{Re}\,(S_{21}/S_{12})}.$$

Rollet's stability factor[106]

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{12}S_{21}|}, \qquad \Delta = S_{11}S_{22} - S_{12}S_{21}$$

is used to verify the unconditional stability in twoports (independent of the input and output impedance), which is achieved for $k > 1$ and $|\Delta| < 1$. The maximum oscillation frequency $f_{\max}$ is reached when the unilateral power gain equals unity

$$U(f)|_{f=f_{\max}} = 1.$$

The maximum available power gain (MAG or $G_{\max}$) is another figure of merit used in device engineering to measure the high-frequency performance of FETs. It can be expressed in S parameter representation

$$\mathrm{MAG} = G_{\max} = \left|\frac{S_{21}}{S_{12}}\right| k - \sqrt{k^2 - 1}$$

and is only defined for stability factors $k > 1$ where the MAG remains finite. Unlike U however, the MAG is not invariant and thus susceptible to external conditions. Regardless of this limitation, the MAG is used more widely in the device engineering community since usually both MAG and U deliver similar results and the calculation of the MAG is more convenient. Also, the maximum oscillation frequency $f_{\max}$ can be obtained equally from both parameters. Similar to f_{T}, the maximum oscillation frequency $f_{\max}$ can be found from the small-signal equivalent circuit

$$f_{\max} = \frac{f_{\mathrm{T,\,in}}}{2\sqrt{g_{\mathrm{ds,in}}\,(R_{\mathrm{g}} + R_{\mathrm{s}} + R_{\mathrm{i}}) + 2\pi R_{\mathrm{g}} C_{\mathrm{gd}} f_{\mathrm{T,in}}}}. \tag{2.2}$$

Above the frequency of maximum oscillations, power gain can no more be obtained. In

active devices, $f_{\max}$ also marks the maximum frequency of activity. Unlike f_T, $f_{\max}$ depends strongly on the gate resistance R_g. $f_{\max}$ can be maximized by using device geometries that enhance current saturation, by increasing the thickness of the metal[107], and by using a T-shaped gate (T-gate or mushroom gate) which reduces the gate resistance[108]. Using a more conductive material for the gate reduces R_g as well.

f_T values discussed so far were intrinsic values, extracted from the extrinsic, as-measured S parameters through a de-embedding procedure. In this procedure, the parasitic elements of the contacting structure are eliminated to obtain the (hypothetical) behavior of the isolated FET. For a detailed description, please refer to the de-embedding chapter (A.7) in the appendix. Usually large differences between intrinsic and extrinsic f_T are obtained, especially for devices with gate length below 1 µm. In short-channel devices, the parasitic pad capacitance of the gate exceeds the intrinsic gate capacitance by far.[109] This causes a large deviation between extrinsic and intrinsic data, rendering the de-embedding procedure vulnerable to uncertainties. $f_{T,in}/f_{T,ex}$ ratios of 2 to 40 are observed in most GFET, however $f_{T,in}/f_{T,ex} = r_{in/ex} = 125$ was reported for a GFET operating at $f_T = 300\,\text{GHz}$ with a 144-nm long nanowire gate[20]. Considering the increasing uncertainties caused by large $r_{in/ex}$ ratios, corresponding $f_{T,ex}$ values should be regarded as rough approximations. For practical applications, a $r_{in/ex}$ ratio close to 1 is desirable. The largest extrinsic f_T reported to date is 55 GHz[110], but in most cases, only the intrinsic $f_{T,in}$ values are reported, not quoting $f_{T,ex}$.

$f_{\max}$ is generally very low in graphene FETs and, opposite to f_T, practically independent of the gate length. A phenomenon only observed in graphene FETs is that $f_{\max}$ usually is smaller than f_T while $f_{\max}/f_T \gtrsim 1$ in regular semiconductor-based FETs. The intrinsic $f_{\max}$ of representative FETs is plotted in fig. 2.6(b).

For device engineers, U, $G_{\max}$ and $f_{\max}$ of a FET are often more important than f_T, as normally RF amplifiers are used to amplify power rather than current. Being fully aware of this, many studies still lay their focus solely on f_T without even mentioning $f_{\max}$. The main reason for poor $f_{\max}$ values is the drain conductance g_{ds} which remains large even at high drain bias, as it depends only slightly on V_{ds} due to the limited current saturation in graphene.[19,86,110] The absent or at best limited current saturation in RF GFETs remains the biggest obstacle in reaching high power gain.

All of the small-signal parameters vary substantially with the drain voltage V_{ds}, thus it is not trivial to maximize f_T and $f_{\max}$. Still, the following measures usually lead to increasing the device performance:

- In regular FETs, the current gain h_{21} decreases with a $1/f$ slope corresponding to $-20\,\text{dB/decade}$. This $1/f$ dependence is observed in GFETs as well. It is caused by the gate impedance $Z = 1/i\omega C_g$ which decays proportionally to $1/f$.[18] Decreasing the gate length reduces the gate capacitance C_g and thus increases f_T.

- The charge carrier mobility can be increased by using clean and flat substrates and dielectrics free of charge traps. However, carrier mobility is overrated: state of-the-art GFETs rarely possess mobilities $> 2{,}000\,\text{cm}^2\text{V}^{-1}\text{s}^{-1}$.[22] Instead, in short-channel devices the saturation velocity starts to play a major role due to the prevailing high fields, and mobility loses importance.[11,111] In these devices, the intrinsic transit frequency is

proportional to the saturation velocity[58], therefore maximizing v_{sat} the will increase f_T.

- Reducing the contact resistance positively impacts f_T and f_{max}, especially in short-channel devices. The contact resistance in graphene FETs is usually still one order of magnitude lower than in silicon FETs.[58]

2.3.1 Device layout of RF graphene FETs

Graphene devices operating at GHz frequencies typically are measured with a probe station using a vector network analyzer (VNA). For most applications, two high-frequency probes with ground-signal-ground (GSG) configuration are required. The fingers of the probes are arranged with a pitch of usually 75 µm − 150 µm, setting the lower limit for total device dimensions to approximately 200 µm × 200 µm. Since graphene flakes are typically much smaller than that, the flakes have to be embedded in a contacting structure consisting of probe pads and transmission lines to the source, drain and gate electrode. Fig. 2.7(a) depicts two such probes contacting one of our GFETs. To minimize transmission losses, high-frequency signals are usually transmitted through shielded transmission lines such as coaxial cables. These transmission lines have a characteristic impedance that depends on their geometry, e.g. the diameter of the inner conductor and its distance to the outer conductor. Practically all measurement equipment operates at an impedance of $Z_0 = 50\,\Omega$ as a compromise between maximum power capacity, reached at $Z_0 = 30\,\Omega$ and minimum attenuation at $Z_0 = 77\,\Omega$. To keep signal reflection to a minimum, the structure contacting the graphene has to match this impedance of $50\,\Omega$ as closely as possible. The most flexible transmission line offering these requirements is the coplanar waveguide (CPW), which in principle is the projection of a 3D coaxial cable onto the 2D substrate. It consists of a central conductor surrounded by two outer conductors, which are usually grounded. Fig. 2.7(a) exemplarily shows a GFET embedded into a CPW contacted by two probes. The impedance of coplanar waveguides can

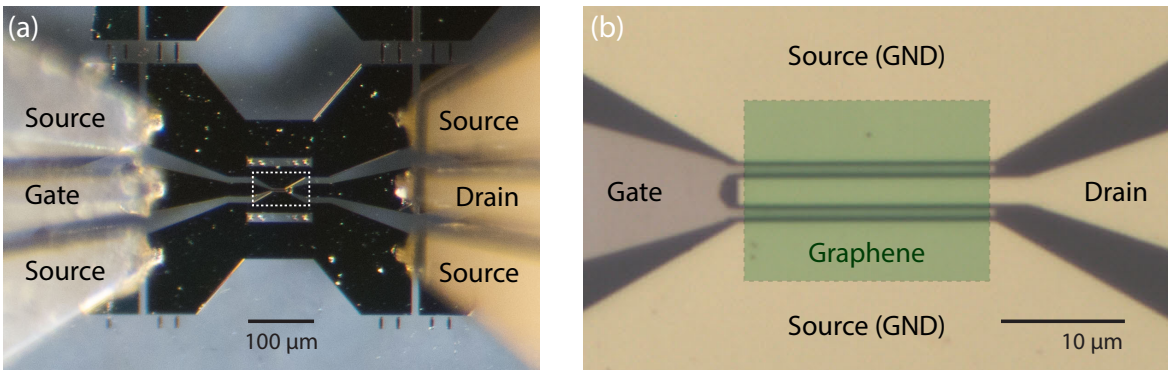

Figure 2.7: (a) A GFET embedded into a coplanar waveguide (CPW), contacted by two high-frequency probes. (b) Zoom-in of the dashed area from (a) showing the intrinsic device. The graphene, here invisible but indicated by the green rectangle, is contacted by drain and source electrodes. Two gate fingers reside centered in the two symmetrical channels, electrically insulated by a dielectric layer.

be tuned simply by adjusting the width of the central conductor and its distance to the outer conductors, allowing for tapering of the transmission line. Thus, the CPW can be extended very closely to the intrinsic graphene FET which typically has a much higher impedance. Coplanar waveguides are used in practically all RF GFETs.

The most widely used GFET layout is the common-source configuration (see fig. 2.7(b)) where one probe is used to modulate the gate and the other to modulate the drain electrode while the outer probe fingers connect the source electrodes to ground. A means of overcoming the limited size of graphene flakes is to divide them into two separate FETs working in parallel, as depicted in fig. 2.8(a). By placing a gate finger to the left and right of the shared drain contact, followed by a separate source contact, the available channel width is effectively doubled. Other layouts are possible[88] (see fig. 2.8(b)) but are not more effective while requiring greater effort during fabrication.

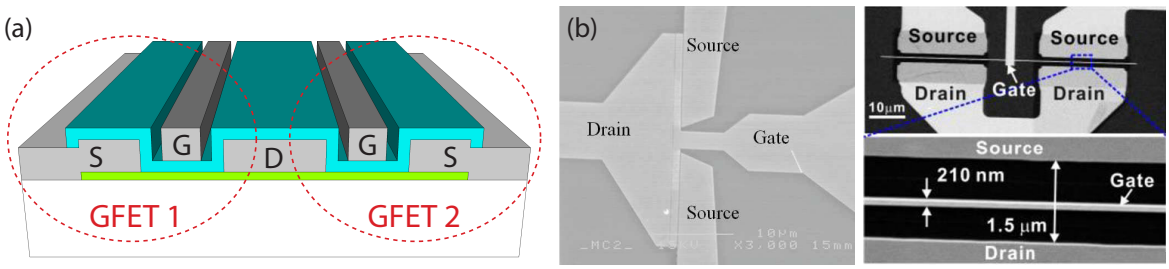

Figure 2.8: The most common GFET configuration: The graphene sheet (green) is separated into two FETs using two gate fingers (G) and source contacts (S) left and right from the shared drain contact (D), thereby effectively doubling the channel width. The gate dielectric is indicated in cyan. (b) Alternative GFET layouts. *Source: (b) adapted from*[75,88].

3 Graphene FETs on sapphire substrates

3.1 Substrate choices for RF graphene devices

As graphene has a thickness of merely one atomic layer, its environment and especially the supporting substrate strongly affect its transport properties. The choice of a suitable substrate therefore is an important task. Most early graphene devices were fabricated on Si/SiO_2 substrates.[9,25,52] While there are several advantages of this substrate, including the possibility to use the conductive Si layer as a global back gate, or enhancing the detectability of graphene when viewed in an optical microscope[1], multiple drawbacks inherent to Si/SiO_2 limit the potential of graphene.[60] Oxide charges trapped in the SiO_2 layer form so called "charge puddles" in graphene[57] leading to enhanced scattering. Additionally, SiO_2 has only a modest dielectric constant of $\varepsilon_r \approx 4$, even though offering high break-down fields. SiO_2, which is usually grown thermally, suffers from high surface roughness, facilitating scattering and hindering homogeneous adhesion of the graphene to the substrate. Scattering is also enhanced due to the low energy of SiO_2 surface phonons.[86] Lastly, the capacitor created by the relatively low-resistance Si substrate and the metallic contacting structure causes loss when transmitting high-frequency signals. Resistive substrates in general exhibit an increased amount of parasitic pad capacitances leading to inferior RF transistor performance and making the de-embedding procedure more susceptible to errors.[109] Some of the best performing GFET reported so far were realized on insulating or semi-insulating substrates.[110]

Considering the aforementioned issues, the optimal substrate for high-frequency graphene devices should be flat, insulating, and free of charge traps. Graphene devices on insulating substrates have been realized already. The most promising candidates are shown in fig. 3.1(b-e). Epitaxial graphene often is grown on SiC $(000\bar{1})$, which can serve as semi-insulating substrate after growth without the need for additional transfer. Compared to Si/SiO_2, SiC substrate enables superior device performance.[19,21,23,114] However, SiC substrates are very expensive and suffer from a terraced surface, inducing scattering in the graphene. Also, growing single layers of graphene on SiC is challenging, and covalent bonds of the carbon interface layer[115] to the substrate have to be broken (e.g. by hydrogen intercalation[90]). Another option is the growth of an insulating layer such as diamond-like carbon (DLC) on top of arbitrary substrates. Surface phonons in DLC exhibit very high energies reducing scattering[86], however the growth of DLC is also very complex and expensive. Pure insulators such as mica, glass or sapphire on the other hand can be used as-is without the need for an

1 Initially, it was argued that graphene is visible only when deposited on a layer of SiO_2 of proper thickness (300 nm) and small deviations would make detection by optical microscope impossible.[112] In fact, monolayer graphene can be spotted on various other substrates including mica[113], glass, and sapphire, however with reduced contrast compared to SiO_2.

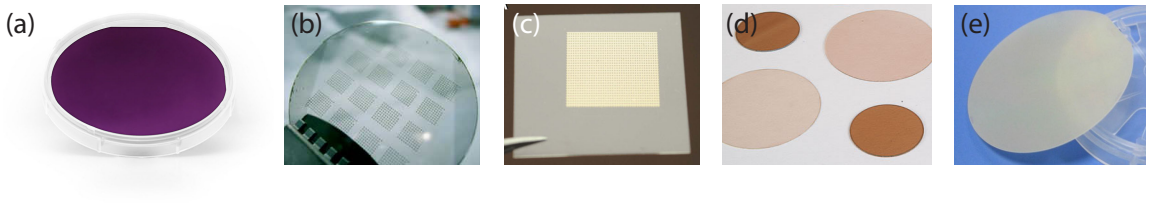

Figure 3.1: (a) Standard low-resistance Si/SiO_2 substrate. (b-e) Potential substrates for graphene, offering low loss, smooth surfaces, vanishing amounts of charge traps and insulating capabilities: (b) SiC wafer with epitaxial grown graphene, integrated into RF GFET.[19] (c) Glass substrate with arrays of RF GFET.[22] (d) Atomically flat mica discs of variable thickness. (e) Sapphire wafer.

insulating add-on-layer. Moreover, mica's atomic flatness reduces scattering in graphene.[49] However, its hydrophilicity leads to accumulation of water and the formation of charge puddles. Also, the adhesion of metallic electrodes is very weak.[113] Sapphire has a well-proven applicability in RF semiconductors. Apart from being an excellent electric insulator, its strengths are low dielectric losses and good heat conduction. Lastly, glass substrates have been tested to some extent and shown to be reliable and RF performance improving.[110] Although glass possesses no imminent disadvantages, in direct comparison we decided in favor of sapphire. Unfortunately, the transparency of insulating substrates for visible light renders focusing on and detection of graphene a complex task. In some cases (e.g. for sapphire), this can be avoided by sand-blasting the backside of the substrate.

3.2 Sapphire - an insulating, low loss substrate

Considering the advantages and disadvantages of the substrates introduced in the previous sub-chapter, we chose sapphire since additional to fulfilling our requirements, it offers several benefits. Sapphire is sometimes referred to as corundum or α-Al_2O_3. It has a high dielectric constant of $\varepsilon_r = 9.39$ (E perpendicular to the C-axis) and $\varepsilon_r = 11.58$ (E parallel to the C-axis)[116] which decreases impurity scattering by reduction of Coulomb scattering in the graphene[117] and allows further circuit miniaturization. C-plane (0001) or basal plane sapphire is technologically most relevant, it is used as substrate for superconductors and semiconductors such as LED and laser diodes.[116] Sapphire wafers are available *epitaxial-growth-ready* polished, offering high surface flatness. Exfoliated graphene attaches very tightly to the sapphire substrate surface as observed in AFM measurements,[118] indicating the absence of air bubbles and trapped molecules such as adsorbed H_2O.

When propagating signals at high frequencies, a substrate with low dielectric loss is advantageous as it minimizes substrate coupling effects. The loss tangent δ, defined as the ratio of the imaginary and real part of the dielectric constant $\varepsilon_r(\omega) = \varepsilon_r'(\omega) + i\varepsilon_r''(\omega)$:

$$\tan\delta = \frac{\varepsilon_r''(\omega)}{\varepsilon_r'(\omega)}$$

is a measure of the energy lost by dissipation. Sapphire exhibits the lowest loss tangent of all

substrates previously discussed ($\tan\delta = 10^{-4}$ @ 3 GHz for the employed substrates).[116] The resistivity $> 10^{14}\,\Omega$cm of sapphire[116] is orders of magnitude larger than in high resistive Si, reducing parasitic capacitances originating from the pads and interconnecting traces. This improves the de-embedding accuracy due to smaller errors in the subtraction process. Sapphire substrates have been used in high-power, high-frequency CMOS integrated circuits for decades.[119] Peregrine Semiconductor pioneered with its UltraCMOS technology in developing silicon-on-sapphire RF integrated circuits that are used in a variety of areas including aerospace and mobile wireless devices such as the iPhone 5S.[120]

Apart from its good electrical insulation, a reason for the use of sapphire as substrate for RF semiconductors is its high thermal conductivity of $46\,\mathrm{Wm^{-1}K^{-1}}$[116] which enables fast cooling and thus greater current densities. Investigations of artificial diamond substrates indeed suggest that current-induced breakdown of graphene devices is thermally activated.[121]

3.3 Gate dielectric

After choosing the optimum substrate for our purposes, we investigated which gate dielectric to employ. A material had to be found that limits performance loss while coupling capacitively to the gate in the best possible way.[58] As graphene is in direct contact with the gate dielectric it is strongly affected by the latter. Impurities and charge traps induce strain, dope the graphene and degrade its charge carrier mobility. Coulomb scattering can be reduced by using a gate dielectric with a high dielectric constant (high-ε_r or more commonly high-κ), which effectively screens the charged impurities at the graphene/dielectric interface.[122] However, this positive impact is diminished as high-κ dielectrics usually exhibit low surface phonon energies[75] thus increasing the occurrence of remote surface optical phonon scattering.[60] Still, compared to using SiO_2, high-κ dielectrics enable higher gate capacitances (at equivalent dielectric thickness t_{diel}) and lower leakage currents. Fig. 3.2 shows the band gap versus dielectric constant of some materials commonly used as gate dielectric.

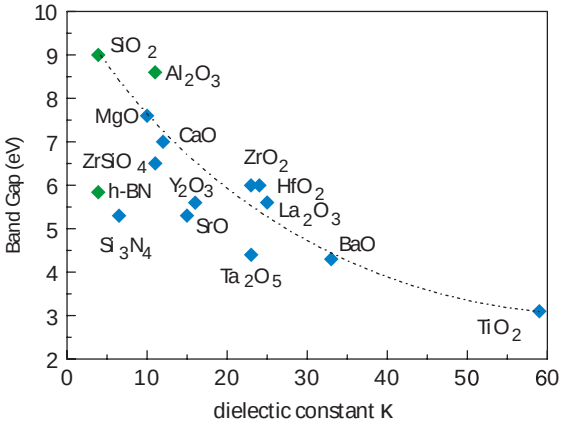

Figure 3.2: Bandgap vs. dielectric constant of some common gate dielectrics. *Source: adapted from[123], complemented.*

The approach chosen by most groups investigating top- or bottom-gated graphene FETs is the growth of high-κ oxides via atomic layer deposition (ALD). Usually Al_2O_3 or HfO_2 are used due to their good electrical insulation. The rather "soft" ALD process can be performed at low temperatures ($< 100\,°C$) and allows for local deposition using PMMA masks. ALD enables homogeneous dielectrics with exact control over the thickness by tuning the number of layers deposited. However, due to graphene's inertness, direct growth of closed films via ALD is not possible. Growth preferably occurs at graphene step edges and small imperfections which serve as nucleation sites initiating the ALD process.[124] Another reason is the hydrophobicity of graphene hindering H_2O-precursor-based ALD procedures.[125] One solution is the deposition of a non-H_2O-based functionalization layer such as NO_2 / trimethylaluminum (TMA) prior to the actual oxide growth.[18] Another option was proposed by Farmer et al. who spin-coat an organic polymeric buffer layer before the ALD process, claiming it poses little effect on the electronic transport properties of graphene.[126] Both solutions however use the combination of two different low-κ and high-κ materials rendering an inhomogeneous dielectric layer and making simulations more complicated. A more elegant solution was found by Kim et al. who evaporated a thin ($< 4\,nm$) layer of aluminum which they oxidized in air.[127] This layer does not form a closed film yet, but the originating Al_2O_3 islands serve as nucleation centers for the subsequent ALD process. We chose this process for the fabrication of the devices presented in this chapter.[1]

3.4 Sample preparation

All samples discussed in this thesis were fabricated entirely in our group at the Institute of Nanotechnology (INT). In the following, the fabrication process is described briefly. The most important steps are visualized in fig. 3.3. More insight into the used fabrication techniques and detailed recipes are provided in the appendix, chapter A.3.1.

We begin with a 330-µm thick C-plane (0001) sapphire wafer from Roditi Ltd[116], pre-patterned with unique markers for easier mapping of the graphene flakes, which are distributed randomly when deposited via mechanical exfoliation. Using an optical microscope, the substrate is scanned for flakes with suitable dimensions. Once found, their mono or bilayer nature is verified with Raman spectroscopy. A contacting pattern is designed in the "eLine" software suite of the electron beam lithography (EBL) system. We spin-coat the sample with an electron sensitive resist (e.g. polymethyl methacrylate (PMMA), a positive resist) and a charge dissipation layer, necessary for EBL on insulating substrates. The pattern is written with the EBL system by selectively exposing the resist to the focused electron beam. This leads to breaking (crosslinking) of the molecular chains in the positive (negative) resist, which improves (impedes) the solubility in a solvent called "developer". After selective removal of the resist with the developer, a metal bilayer, usually consisting of Ti (10 nm) and Al (100 nm), is deposited on the newly created mask using an ultra high vacuum (UHV) metal evaporator. The thin layer of titanium is needed for better adhesion of the subsequent metal.

1 In samples produced earlier, we fabricated gate dielectrics from evaporated MgO and Hf (oxidized *in-situ*), however sufficient insulation was not reached by these methods.

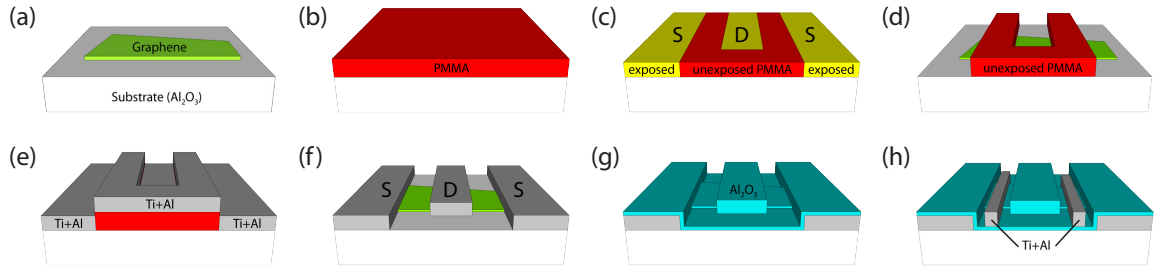

Figure 3.3: Fabrication steps of the graphene-on-sapphire FETs discussed in this chapter. (a) A graphene sheet is deposited via mechanical exfoliation onto sapphire substrate. (b) The sample is spin-coated with a layer of resist (PMMA) which subsequently is exposed to a focused electron beam, defining the pattern for source (S) and drain (D) electrodes (c). (d) Immersing the sample into a developing agent removes the exposed resist. (e) Metal for the electrodes is deposited onto the PMMA mask in an ultra high vacuum (UHV) metal evaporator, followed by a lift-off procedure (f). (g) An Al_2O_3 dielectric layer is grown via a combination of evaporated, naturally oxidized aluminum and ALD. Finally, repeating steps (b)-(f), the gate electrode is patterned (h).

However, it is also the contact material for the graphene. Next, the sample is immersed into a strong solvent (e.g. acetone) which completely removes the resist including the metal residing on top of the mask. This procedure is referred to as "lift-off" and marks the last step in the fabrication of metallic electrodes.

The steps from above are repeated accordingly to create a mask for local dielectric deposition in the circumference of the graphene channel. A thin layer of aluminum (2 nm) is deposited with subsequent natural oxidization in air. The aluminum oxide serves as seed layer for the following atomic layer deposition of Al_2O_3. We deposit the gate electrode in the same fashion as the drain and source electrodes described above. In fig. 3.4(a), an image of a completed sample is shown.

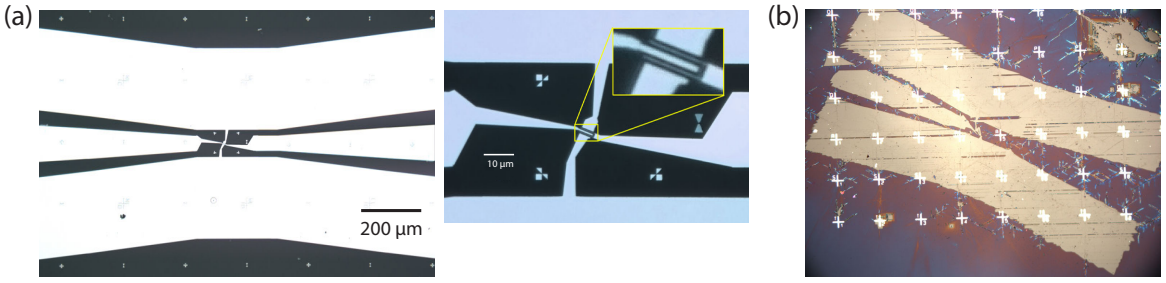

Figure 3.4: (a) Finished GFET (sample SP15) with coplanar waveguide contacts. A zoom-in shows the active device. The graphene and the gate dielectric are not visible in the image. (b) Distorted pattern after electron beam lithography on an insulator without the use of a charge dissipation layer. The negative charges of the electron beam accumulate, thereby deflecting subsequent electrons, leading to distortion and stitching errors.

3.4.1 Electron beam lithography on insulating substrates

When performing electron beam lithography on insulating substrates, additional fabricating steps are required. Negative charges introduced by the electron beam accumulate in the insulating substrate leading to beam deflection and ultimately to a distortion of the pattern (see fig. 3.4(b)). To avoid charge accumulation during EBL, a charge dissipation layer can be applied. Often a thin conductive layer (i.e. Au, ITO) is deposited below or on top of the resist. This additional evaporation step is time consuming and requires subsequent removal by an etchant that may degrade the graphene or the substrate. Moreover, metallic layers induce e-beam scattering thereby limiting the achievable resolution.[128] In our approach, we used a thin layer of Espacer 300Z, a conductive polymer from Showa Denko K.K., that can be spin-coated on top of the e-beam resist. Best results were achieved at a spin-coater rotation speed of 3000 RPM for 60 s with subsequent baking at 100 °C for 10 min resulting in a layer thickness of 20 nm. Removal prior to development is achieved simply by immersing the sample into distilled water, which has no degrading effects on the resist nor the graphene. The conductive polymer strongly reduces beam distortion and increases the maximum achievable resolution[129].[1]

3.5 Sample overview

A total of 17 monolayer and 2 bilayer graphene-on-sapphire devices were fabricated with a yield of 4 devices operating at extrinsic transit frequencies > 0.1 GHz. Some of the devices have already been fabricated during the time of the diploma thesis[131] and have been characterized in the present work. Table 3.1 gives an overview of the device parameters and RF performance of those GFETs. The best performing monolayer GFETs (SP15, SP28) are discussed in more detail in the following. Unfortunately, complete analysis of the bilayer GFET was not possible due to a defective de-embedding structure. However, full coverage of

sample	layer	l_g	l_ch	w_ch	t_diel	$I_\mathrm{ds,max}$	$g_\mathrm{m,max}^\mathrm{RF}$	$f_\mathrm{T,ex}$	$f_\mathrm{T,in}$	f_max
unit		nm	nm	µm	nm	mA/µm	µS/µm	GHz	GHz	GHz
SP15	mono	200	800	3.7	22	0.77	250	2.79	≈ 80	3.9
SP19	mono	200	1000	5.9	12	0.10	18	0.5	4.4	1.7
SP28	mono	100	500	14.4	15	-0.45	50	2.9	16.4	4.6
SP16	bi	200	1000	3.3	22	N/A	N/A	0.68	N/A	N/A

Table 3.1: Table of select graphene-on-sapphire FETs, listing the number of layers, gate length (l_g), channel length (l_ch), channel width (w_ch), thickness of the dielectric layer (t_diel), maximum drain current and transconductance, embedded and de-embedded transit frequency ($f_\mathrm{T,in}$ and $f_\mathrm{T,ex}$) and maximum oscillation frequency f_max. The dielectric in all devices is Al_2O_3 grown by ALD.

1 Interestingly, even graphene can be used as discharge layer improving the resolution compared to a metallic layer and suppressing the proximity effect.[130] Given the high production costs of graphene and the complex transfer involved, this procedure seems to be limited to very special applications.

another bilayer GFET is provided in the next chapter.

Our first samples (up to sample no. 19) were measured at and in collaboration with École normale supérieure (ENS), Paris using the setup described in the appendix (chapter A.5.1). Later, an improved setup was built and tested in our lab at KIT (for details see chapter A.5.2). From sample no. 20 on, all proceeding samples were measured and characterized entirely at the Institute of Nanotechnology, KIT.

3.6 Characterization of sample SP15 (monolayer graphene FET)

3.6.1 DC characterization of sample SP15

The first step of a typical dc characterization is measuring the transfer characteristics (I_{ds} vs. V_{gs}) of the device, as described in chapter 2.2. Direct measurement of the drain current was not possible with the experimental setup as explained in the appendix, chapter A.5.1. Instead, we derive I_{ds} from drain-source voltage measurements using a bias resistor with a well known resistance of $R_{\mathrm{bias}} = 1\,\mathrm{k\Omega}$ placed in series with the channel. The voltage drop at the bias resistor then is translated into a drain current I_{ds}. Fig. 3.5 shows the low-bias transfer characteristics taken at room temperature as well as at 77 K. Since the characterization was performed in a two probe measurement, the total drain-source resistance R_{ds} includes the contact resistance. As the charge neutrality point could not be reached in the first measurement (fig. 3.5(a)) the charge carrier density $n_{\mathrm{2D}}\,(V_{\mathrm{gs}} - V_{\mathrm{Dirac}})$ can not be derived. Instead, in this and all following transfer characteristics we plot R_{ds} additionally versus D/e (top abscissa), with D being the displacement field which corresponds directly to the gate voltage and does not take the shift of the Dirac peak into account (refer to chapter 1.4). This enables us to plot several curves with charge neutrality points at different gate voltages in one graph. The on/off current ratio of the device is rather low (≈ 3) as expected for top-gated GFETs.[11] We observe a strong n-doping of the sample with the Dirac point shifted far into the negative gate voltage region. This can be explained by electron doping introduced by the aluminum contacts.[132] Judging by the slope of the curves in fig. 3.5, best RF transistor performance is expected at gate voltages between $-5.5\,\mathrm{V}$ and $-3\,\mathrm{V}$.

We measured the output characteristics at various gate voltages (plotted in fig. 3.6(a)). At low bias ($V_{\mathrm{ds}} < 0.2\,\mathrm{V}$), the drain current depends linearly on the drain voltage. With increasing drain bias, the current begins to saturate. However, no full saturation is observed for the transistor within the bias regime. The transconductance $g_{\mathrm{m}}^{\mathrm{dc}}$ increases almost linearly with drain voltage reaching a maximum of $\approx 200\,\mu\mathrm{S}/\mu\mathrm{m}$ (fig. 3.6(b)).

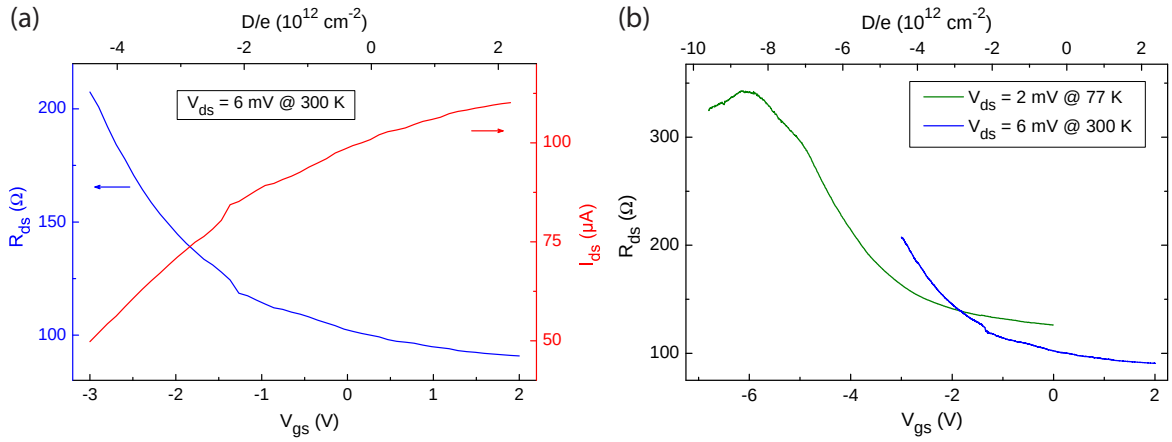

Figure 3.5: Low bias transfer characteristics of SP15. (a) R_{ds} (blue) and I_{ds} (red) vs. V_{gs}. To avoid leakage, the gate voltage was limited to $-3\,\mathrm{V}$ in these initial room temperature gate voltage sweeps. (b) Measurement of $R_{\mathrm{ds}}\,(V_{\mathrm{gs}})$ at $77\,\mathrm{K}$ (green) in comparison to room temperature (blue). The Dirac point is reached at $V_{\mathrm{gs}} = -6\,\mathrm{V}$ indicating strong negative doping of the graphene.

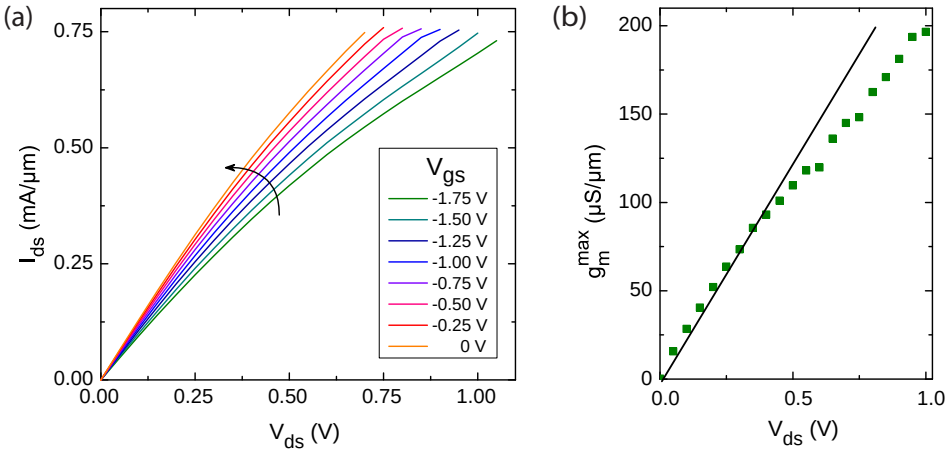

Figure 3.6: (a) Positive branch of the output characteristics of SP15, normalized to the channel width. The gate voltage is varied from $V_{\mathrm{gs}} = -1.75\,\mathrm{V}$ to 0 in $0.25\,\mathrm{V}$ steps. An onset of current saturation is observable with increasing drain voltage. (b) Maximum dc-transconductance $g_{\mathrm{m}}^{\mathrm{max}}$ vs. drain voltage with a peak value of $\approx 200\,\mu\mathrm{S}/\mu\mathrm{m}$. The black line is a guide for the eye.

3.6.2 Microwave characterization of sample SP15

Initially, the high-frequency response of the GFET was analyzed in the gate voltage range of highest dc-transconductance (−5.5 V to −3 V), where maximum GFET performance is expected. Indeed, the highest current gain of the GFET was found at gate and drain voltages $V_{gs} = -5.2\,\mathrm{V}$ and $V_{ds} = -1.1\,\mathrm{V}$, respectively, reaching unity at an extrinsic transit frequency of $f_{T,ex} = 3\,\mathrm{GHz}$. Fig. 3.7(a) shows the extrinsic (blue dots) and intrinsic (red circles) current gain at these bias conditions. The intrinsic device properties are obtained by de-embedding of the measured S parameters using *open* and *short* dummy structures (see appendix A.7 for the de-embedding procedure). Note that the as-measured as well as the de-embedded current gain closely follows a $1/f$ dependence as expected for a MOSFET. When extrapolating the de-embedded current gain, a transit frequency $f_T \approx 80\,\mathrm{GHz}$ is reached. The rather large ratio of intrinsic to extrinsic f_T (here: $r_{in/ex} \approx 27$) can be explained by the fact that in this particular device, the channel width ($w_{ch} = 3.7\,\mu\mathrm{m}$) is much smaller than in typical FETs. In this case, the parasitic pad capacitance is much larger than the gate capacitance, which can lead to such large ratios.[20] Because of the small device geometry we also observe increased variation in the de-embedded $|h_{21}|$ data. This effect is less prominent in devices with wider channels. We extract a maximum RF transconductance $g_m^{RF} \approx 250\,\mu\mathrm{S}/\mu\mathrm{m}$ at a frequency of 100 MHz. This value is in good agreement with the value $g_m^{dc} \approx 200\,\mu\mathrm{S}/\mu\mathrm{m}$ found in dc measurements. Maximum available gain (MAG) and unilateral power gain (U) are plotted in fig. 3.7(b). These figures of merit are extracted from the non-corrected data as they are inherent device properties. U and MAG reach unity at a maximum oscillation frequency $f_{max} = 3.9\,\mathrm{GHz}$.

The high-frequency measurements were also performed in a probe station cooled with a flow of liquid N_2 to a temperature of $\sim 77\,\mathrm{K}$, where we obtained similar results. We repeated the measurements several times within a time frame of four months. Except for small differences in the position of the Dirac point, no significant transistor performance changes were observed. We attribute this to the aluminum oxide dielectric which encapsulates the graphene, shielding it from external perturbations.

The high-frequency response of the GFET was additionally mapped with a “2D sweep”, for which we varied both gate voltage (−2 V to 0 in 50 mV steps) and drain voltage (−0.65 V to 1.2 V in ∼ 3 mV steps), totaling in 1394 individual S parameter measurements. The gate voltage was limited to −2 V to avoid leakage currents during the 12 hours of measurement. For each data point, the extrinsic transit frequency f_T was extracted and plotted versus V_{ds} and V_{gs} (see fig. 3.8). A clear gate dependence is visible. The distribution of f_T does not show any sudden jumps or inhomogeneities. As expected, at zero drain voltage, f_T vanishes (independent of V_{gs}). The transit frequency increases almost symmetrically both for rising negative and positive drain voltages. For any given drain voltage, f_T rises when decreasing the gate voltage from 0 to −2 V.

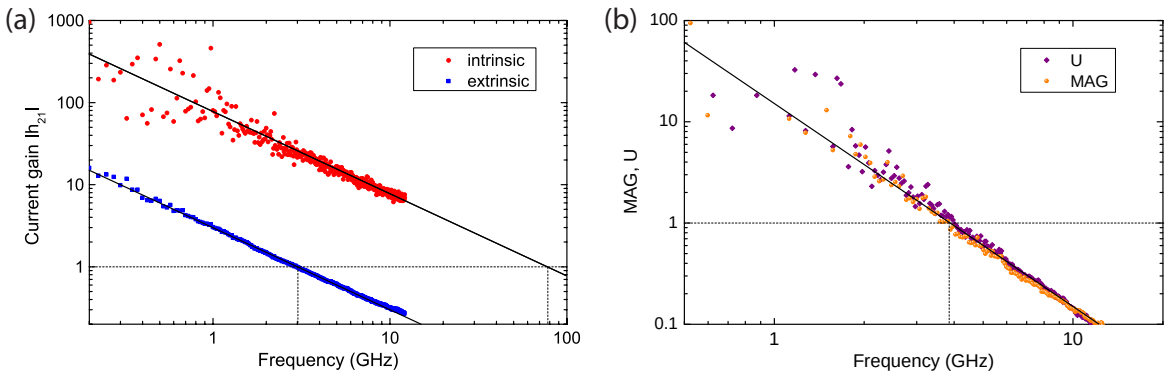

Figure 3.7: High-frequency characteristics of SP15. (a) Current gain of the extrinsic (blue) and intrinsic (red) device, yielding transit frequencies of $f_{\mathrm{T}} = 3\,\mathrm{GHz}$, $f_{\mathrm{T}} \approx 80\,\mathrm{GHz}$ respectively. These maximum values were found at $V_{\mathrm{gs}} = -5.2\,\mathrm{V}$ and $V_{\mathrm{ds}} = -1.1\,\mathrm{V}$. b) Maximum available gain (purple) and unilateral power gain (yellow) both reach $f_{\mathrm{max}} = 3.9\,\mathrm{GHz}$. Note the good $1/f$ dependence of all quantities indicated by the black lines as a guide for the eye.

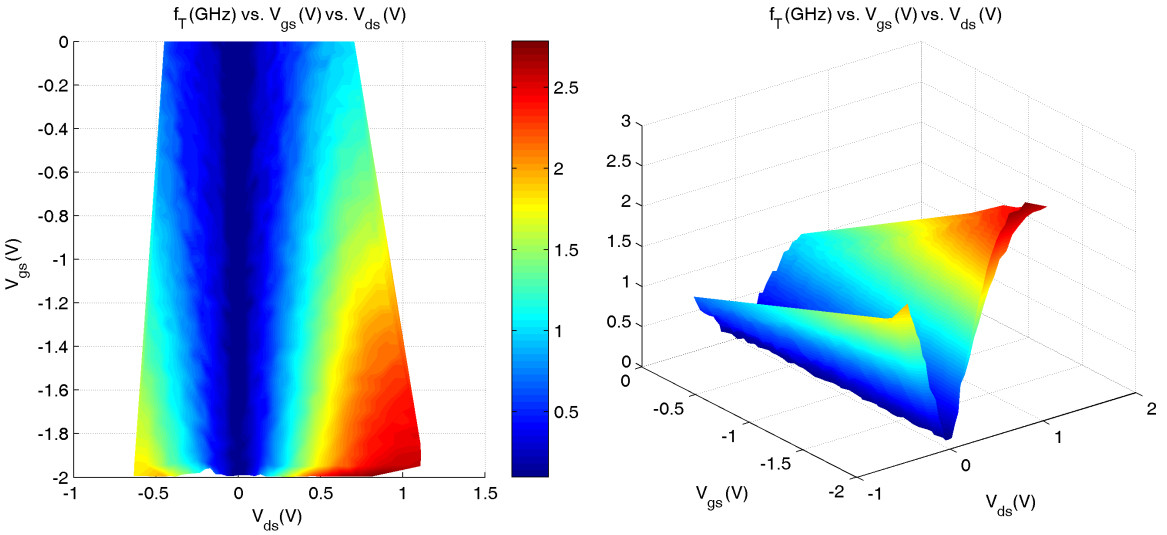

Figure 3.8: SP15: Extrinsic transit frequency $f_{\mathrm{T,ex}}$ versus V_{ds} (x-axis) and V_{gs} (y-axis). On the right hand side, the data from the left is visualized in a 3D contour plot.

3.7 Characterization of Sample SP28 (monolayer graphene FET)

Sample SP28 is a monolayer graphene-on-sapphire FET similar to SP15, but with a wider channel (14.4 µm instead of 3.7 µm), and reduced gate and channel length of $l_g = 100\,\text{nm}$ and $l_{ch} = 500\,\text{nm}$, respectively. In this sample (and for all future samples), we used a symmetrical layout to contact the graphene flake (see fig. 3.9(f)) to minimize interference from the two individual channels (refer to chapter 2.3.1). The sample was measured entirely on the new probe station at KIT. The results are assembled in fig. 3.9. From the low-bias transfer characteristics ($V_{ds0} = 3\,\text{mV}$, fig. 3.9(a)) we find the Dirac point located at $V_{gs} = 0.7\,\text{V}$, indicating less unintentional doping than in the previous sample. With increasing drain bias, the Dirac point shifts to positive gate voltages, while the on/off current ratio declines. Both effects are usually observed in GFETs. The transport characteristics in fig. 3.9(b) show an asymmetrical gate effect in the negative and positive drain-source voltage branch. After a small linear region in the negative branch, we observe crossing of the curves taken at different gate voltages leading to zero g_m at these particular bias conditions as discussed in chapter 2.2. Therefore, we expect higher device performance for positive drain voltages. Indeed we find higher current gain for positive drain-source bias (compared to equal negative bias). Maximum current gain occurs at $V_{ds} = 0.92\,\text{V}$ and $V_{gs} = 0.71\,\text{V}$, where transit frequencies $f_{T,ex} = 2.89\,\text{GHz}$ and $f_{T,in} = 16.4\,\text{GHz}$ are reached (fig. 3.9(c)). At the same bias conditions we observe the maximum transconductance $\left|g_m^{RF}\right| \approx 50\,\mu\text{S}/\mu\text{m}$ (fig. 3.9(e)). We explain the lower $f_{T,in}/f_{T,ex} \approx 5.7$ ratio compared to sample SP15 with the considerably wider channel, which offers smaller transconductance and larger resistance per µm. Again, the maximum oscillation frequency $f_{max} = 4.6\,\text{GHz}$ (fig. 3.9(d)) is greater than the extrinsic transit frequency, but still far from $f_{T,in}$. Unfortunately, further characterization is not possible as the device was destroyed while inadvertently passing a too high current (corresponding to a current density of$-0.45\,\text{mA}/\mu\text{m}$) through the channel, melting the metallic drain and source leads.

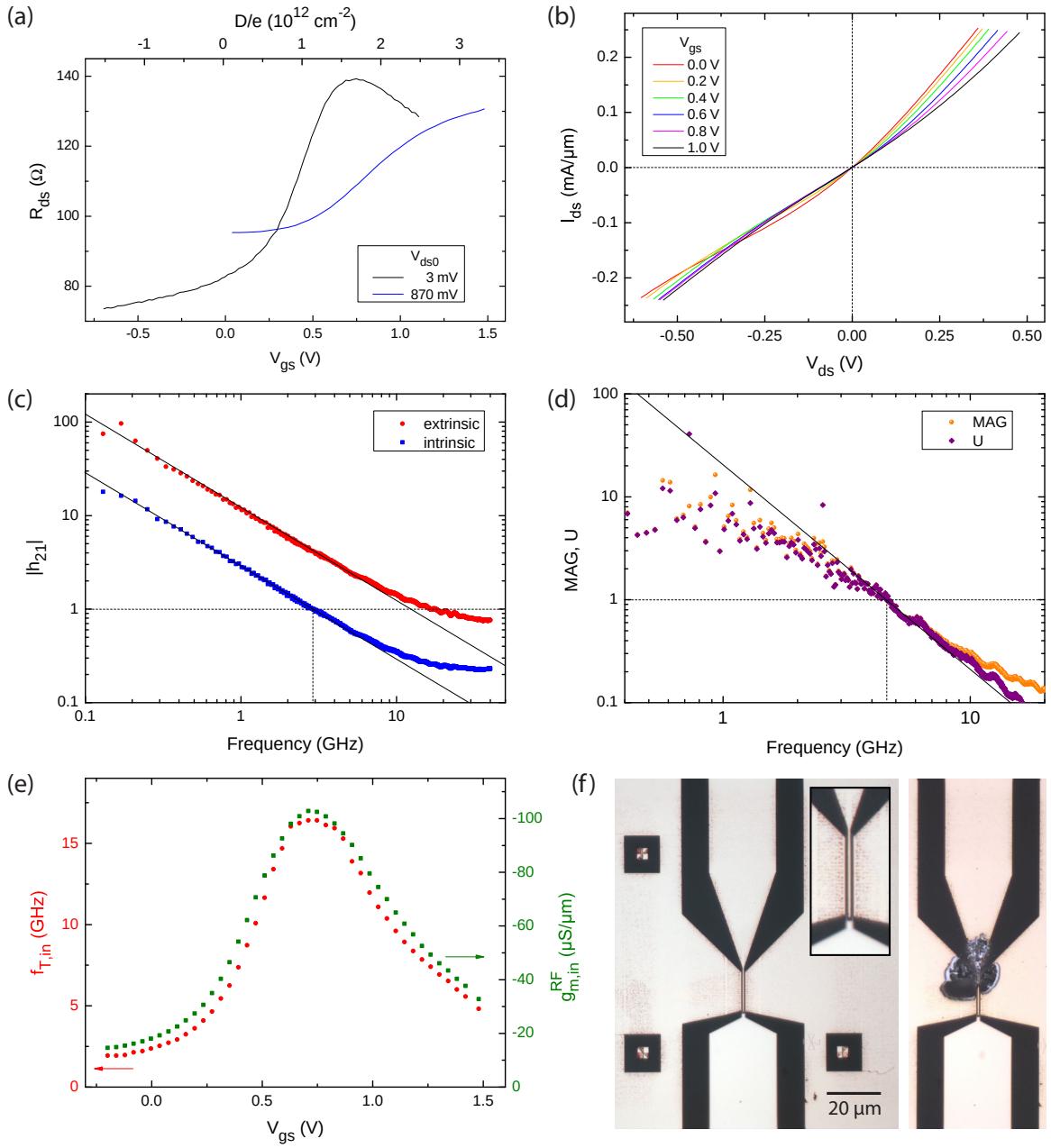

Figure 3.9: Characterization of SP28. (a) Transfer characteristics measured at different bias voltages. (b) The transport characteristics show a slightly superlinear behavior without indication of saturation. (c) Maximum current gain of the device is observed at $V_{\mathrm{gs}} = 0.71\,\mathrm{V}$ and $V_{\mathrm{ds}} = 0.92\,\mathrm{V}$, yielding transit frequencies of $f_{\mathrm{T,ex}} = 2.89\,\mathrm{GHz}$ and $f_{\mathrm{T,in}} = 16.4\,\mathrm{GHz}$. d) Maximum available gain and unilateral power gain reach unity at $f_{\mathrm{max}} = 4.6\,\mathrm{GHz}$. (e) Intrinsic transit frequency (red circles) and high-frequency transconductance (green squares) versus gate-source voltage at fixed drain bias $V_{\mathrm{ds}} = 1\,\mathrm{V}$. (f) Zoom-in to the active device consisting of two symmetrical graphene channels with the drain electrode in the center. A too high drain-source current ($-0.45\,\mathrm{mA/\mu m}$) destroyed the device, melting the ohmic contacts.

3.8 Conclusions

Our goal was the realization and test of graphene FETs operating at microwave frequency on an insulating substrate. After weighting the pros and cons of several substrate candidates, we chose sapphire due to its low loss at high frequencies and large thermal conductivity. We established a fabrication process for graphene devices on sapphire.[131] It involves the use of a conductive polymer as charge dissipation layer to enable non-destructive, distortion-free, and high resolution electron beam lithography. The devices sustained current densities of up to $\approx$1 A/mm, thanks to sapphire's excellent thermal conductivity.

For the gate dielectric we effectually implemented the aluminum oxide deposition technique via ALD as proposed by Kim et al.[127] Consecutive measurements in a time period of four month revealed no degradation of the high-frequency performance of the devices. We conclude that the aluminum oxide dielectric preserves the device properties by encapsulating the graphene, effectively screening external interference. However this beneficial effect comes at the expense of reduced charge carrier mobility. Gate leakage was not observed - if present, leakage currents must have been smaller than the detection limit of our ampere meters. This implies the possibility to reduce the thickness of the dielectric layer even further to values smaller than 10 nm.

Device operation was verified with transfer characteristics and transport characteristics measurements. We find a clear gate voltage dependance of the drain-source current. Complete current saturation is not observed, still the devices offer considerable transconductances.

Our work represents the first-time characterization of graphene-on-sapphire FET at microwave frequency.[133] Multiple samples exhibit intrinsic transit frequencies in the GHz-range (refer to table 3.1), with one GFET operating at frequencies of up to $f_{\mathrm{T,in}} = 80\,\mathrm{GHz}$. Repeating the high-frequency measurements at liquid-nitrogen temperature yielded unchanged device performance, suggesting our GFET could be used in a cryogenic low-noise amplifier. We have to stress again that our GFETs are made from exfoliated graphene, limiting the number of devices that can be prepared in a given time interval. At the time of publication (September 2011), the performance of our GFET was comparable to similar devices (e.g. an epitaxial GFET on SiC with a gate length of $l_{\mathrm{g}} = 240\,\mathrm{nm}$ operating at 100 GHz presented by Lin et al.[19]). In 2012, Wang et al. reported a CVD-graphene-on-sapphire FET with $l_{\mathrm{g}} = 210\,\mathrm{nm}$ reaching $f_{\mathrm{T,ex}} = 22\,\mathrm{GHz}$.[88] Our extracted maximum frequencies of oscillations f_{max} are larger than $f_{\mathrm{T,ex}}$ but considerably smaller than $f_{\mathrm{T,in}}$. This behavior is typical for graphene FET, due to the large drain conductance caused by the weak current saturation.[13] Despite the lack of current saturation, sample SP15 exhibited a considerable maximum transconductance of $g_{\mathrm{m}}^{\mathrm{RF}} \approx 250\,\mu\mathrm{S}/\mu\mathrm{m}$ which is roughly five times the value found in sample SP28. We attribute this difference to a cleaner fabrication of SP15 enabling lower contact resistance. Close examination of sample SP28 (fig. 3.9(f)) reveals a pattern of inhomogeneities in the contact area. This could be an indicator of resist residues trapped between the graphene and the contacts due to insufficient development of the resist before metal evaporation, causing increased contact resistance.

The satisfactory results of our graphene-on-sapphire FET could be further improved by using a thinner gate dielectric and by decreasing the gate length as well as the channel length. Also, minimizing the ungated graphene region by decreasing the channel length to

values close to the gate length is expected to improve overall device performance. Using a smoother (potentially atomically flat) substrate additionally could lead to a decrease in substrate induced scattering as well as reduced graphene corrugation, resulting in further optimization.

4 Graphene on atomically flat hBN substrates

In the last chapter we discussed the benefits of sapphire as a substrate for graphene-based devices. We highlighted its potential for high-frequency applications. Still, the Al_2O_3 dielectric and the remaining roughness of sapphire (although reduced compared to SiO_2) impairs the charge carrier mobility in graphene. Depositing graphene on an atomically flat substrate is predicted to result in increased mobility.[59] Ideal substrates for graphene are insulators with high dielectric strength and a wide band gap, possessing few charged impurities, offering good thermal and mechanical properties, and a surface free of dangling bonds.

The first demonstration of graphene on an atomically flat substrate was realized using mica.[49] Mica is a layered material that can be cleaved just like graphite. AFM measurements show that graphene conforms to mica substrates down to the atomic level, completely suppressing intrinsic ripples (see fig. 4.1(a,b)). However, due to its strong hydrophilicity water films get adsorbed forming islands on the surface leading to dipoles. These water islands are also responsible for a certain degree of graphene roughness. Moreover, performing EBL/lift-off is complicated and the contact metals adhere only weakly to the substrate.[113] Therefore, only few electronic transport measurements have been performed with graphene on mica so far, and high-frequency graphene devices have not been realized to date.

Hexagonal boron nitride (hBN) is more suitable as substrate for graphene in many ways. Also being atomically flat, it is free of trapped charges and dangling bonds.[50] Its surface is chemically inert and it possesses larger optical phonon mode energies than SiO_2 which allows better high-temperature and high-electric-field performance. Being a layered material with

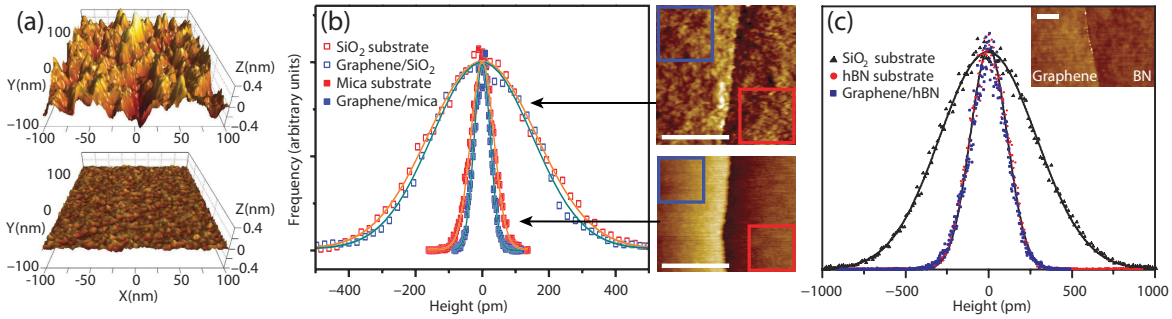

Figure 4.1: (a) Topographic AFM images representing the surface roughness of SiO_2 (top) and mica (bottom). (b) Histograms of the height distribution show that graphene follows the morphology of the underlying substrate. On the right, corresponding topographic images with the graphene/substrate boundary are shown. (c) Height distribution histogram of graphene on hBN and of SiO_2 substrate for comparison. The corresponding AFM image is shown in the inset. All scale bars are 250 nm. *Source: (a,b) adapted from[49], (c) adapted from[50], complemented.*

the boron and nitrogen atoms arranged in a hexagonal lattice (see fig. 4.2), it sometimes is referred to as "white graphite". Boron and nitrogen are carbon's closest neighbors in the periodic table with the atomic numbers 5 and 7, respectively. The lattice constant mismatch is only 1.8 %[70], leading to microscopic Moiré patterns when graphene and hBN are stacked[134]. It is a direct bandgap material with a large bandgap energy of 5.97 eV.[135] Its dielectric constant $\varepsilon_r \approx 3-4$ and breakdown voltage $V_{\mathrm{br}} \approx 0.7\,\mathrm{Vnm}^{-1}$[50] are similar to that of SiO_2 ($\varepsilon_r = 3.9$ and $V_{\mathrm{br}} \approx 1\,\mathrm{Vnm}^{-1}$, respectively). Besides, it offers almost three orders of magnitude higher thermal conductivity.[58]

In theory, when a graphene sheet is placed on top of a hexagonal boron nitride layer, the symmetry of the two graphene sublattices is broken. In the energetically most favorable configuration, the carbon atoms of sublattice A are located on top the boron atoms, and the carbon atoms of sublattice B are situated in the center of the hexagon rings. Depending on the configuration, density functional theory (DFT) calculations predict the opening of a bandgap of at least ≈ 50 meV.[70] However, the authors neglected the lattice mismatch and assumed zero relative rotation, thereby not taking into account the resulting short range Moiré patterns which restore the sublattice symmetry. Nevertheless, Moiré patterns with periods larger than 10 nm were found in recent experiments.[136,137] The bandgap predicted by theory has not been verified experimentally, yet.

In 2007, Taniguchi and Watanabe realized the growth of large, millimeter-sized high-quality hBN crystals for the first time, using a high-pressure high-temperature (HP-HT) environment.[138] Initially developed with the acclaimed goal of producing a wide-bandgap material for laser diodes, its enormous potential as a substrate for graphene quickly was discovered. Compared to typical graphene-on-SiO_2 devices, a tenfold increase in charge carrier mobilities ($25{,}000\,\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ at room temperature) is achieved using these crystals.[50] In the same study, the tight conformation of the graphene to the surface of the hBN substrate is demonstrated using high resolution AFM. In fig. 4.1(c) the corresponding height distribution diagrams are shown. More recent STM measurements demonstrate the increased flatness in graphene on hBN[134,139], also verifying a reduction of charge puddles. Several experiments confirmed the benefits of hBN as substrate for graphene in general[140] and especially for high-frequency applications[58,83,141], including bilayer GFET[142].

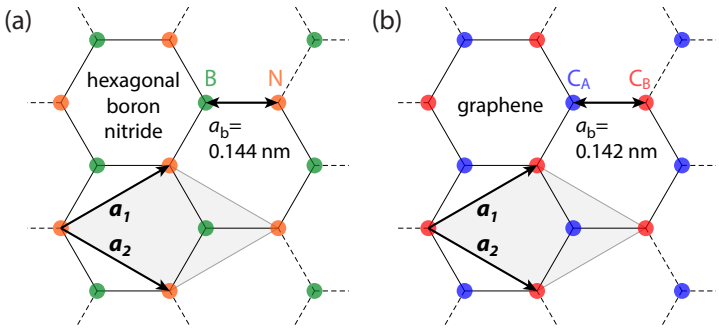

Figure 4.2: (a) Hexagonal boron nitride lattice compared to (b) graphene lattice. The lattice constant mismatch is only 1.8 %.

4.1 Device fabrication

To benefit from the atomic flatness as well as the insulating nature of hBN, we developed a new device layout. By patterning a local bottom gate instead of a top gate, hBN can serve both as the gate dielectric and as substrate for graphene (see schematic in fig. 4.3). Compared to the GFET discussed in chapter 3, the sequence of the fabrication steps is almost reversed. Also we do not require to deposit Al_2O_3 dielectric which degrades the mobility. In a collaboration with Watanabe and Taniguchi (National Institute for Materials Science, Tsukuba, Japan), our group was provided with millimeter-sized, high-quality hBN single crystals. These crystals were produced under HP-HT conditions as described in [138]. We obtain nanometer-thin hBN films by mechanical exfoliation onto Si wafers with a 300-nm thick layer of thermally grown SiO_2. On this substrate, each hBN layer adds an optical contrast of 1.5 %. When the thickness of the SiO_2 is adjusted to 80 ± 10 nm, the per-layer contrast is increased to ≈ 2.5 %, making it possible to optically identify even monolayer flakes. [143] Crystals of our desired thickness ($\approx 5 - 50$ nm) appear light blue, simplifying preliminary identification with an optical microscope. After this coarse thickness estimation, we transfer the crystals onto our pre-patterned sapphire substrates. The actual crystal thickness is determined via AFM after the transfer.

4.1.1 Wedging transfer technique ("wet" transfer)

Since the exfoliated hBN crystals are usually hardly wider than the bottom gate, a precise transfer and alignment technique is needed. A special transfer setup was established in our group [113,144], consisting of a high-precision piezo stage (Physik Instrumente M-686.D64 xy-piezo linear-motor with C-867 controllers) in combination with a Mitutoyo microscope with large working distance objectives. The setup is depicted in fig. 4.5(a). Transfer is achieved with a water-based wedging transfer technique, following Schneider et al. [145] The most important steps of the procedure are visualized schematically in fig. 4.4. The procedure is identical for graphene and hBN crystals. We begin by mechanical exfoliation of the crystals onto Si substrate using the scotch tape technique. After locating a suitable flake (fig. 4.6(a)) with an optical microscope the substrate is cleaned with a cotton swab, excluding the vicinity of the particular flake to ease PMMA detachment. The substrate is spin-coated with a thick layer of resist (PMMA 8 %, 1500 RPM, 90 s). The resist is then mechanically removed at the edges of the substrate using a small wooden slat, again to facilitate subsequent

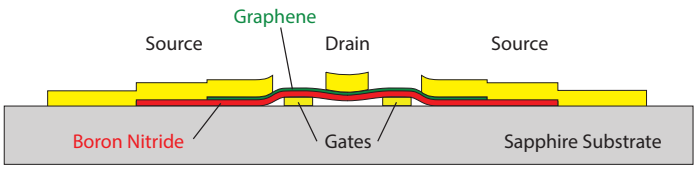

Figure 4.3: Schematic of the graphene on hBN device layout. Prior to the transfer of hBN and graphene layers, a metallic bottom gate is deposited on our sapphire substrate. In the last step, source and drain electrodes are fabricated by e-beam metal deposition. Bending of the hBN and graphene is exaggerated for better visibility.

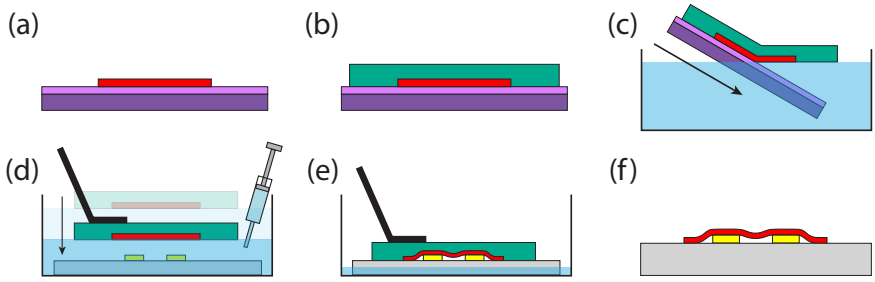

Figure 4.4: Schematic of the "wet" transfer technique, applicable to graphene and hBN flakes (here demonstrated for hBN). (a) Hexagonal boron nitride (red) is deposited on Si/SiO_2 substrate for better visibility. (b) After locating a suitable flake, the sample is spin-coated with a thick layer of PMMA (turquoise). (c) The sample is slowly immersed in water. The PMMA layer detaches from the substrate, floating on the water surface. (d) Using a micro manipulator, we align the transparent PMMA mask roughly to the pattern on the target substrate, which is fixed to the beaker. Precise alignment is achieved by moving the beaker with the piezoelectric xy-stage. (e) We slowly remove the water with a syringe, until the hBN/PMMA stack attaches to the target substrate. (f) After drying the sample in a furnace, the PMMA is removed in acetone.

detachment. We slowly immerse the substrate into a beaker filled with distilled water. The water intercalates between PMMA and Si substrate, detaching the hydrophobic polymer layer until it floats freely on the surface of the water. Sometimes, intercalation is suppressed by strong adhesion of the PMMA to the substrate. In these cases, the Si substrate is fixed to the bottom of a beaker which we gradually fill with water until, due to surface tension, the water starts pulling at the PMMA layer. After waiting for some time (between a few minutes and several hours, depending on the level of adhesion) the PMMA film fully detaches. Next, we fix the target substrate to the bottom of the beaker. While slowly removing the water from the beaker with a syringe, the PMMA layer is held by a xyz-stage and can be aligned to the bottom gate on the target substrate. The beaker containing the sample can be moved by the piezoelectric stage, offering a $25 \times 25\,\mathrm{mm}^2$ travel range with high resolution allowing for accurate alignment with a precision of $\sim 1\,\mu\mathrm{m}$ under optimum circumstances. After the removal of all water from the beaker, the PMMA is dried with nitrogen to conform to the substrate. This step is shown exemplarily in fig. 4.5(b). Finally we bake the sample at 165 °C for 30 min to further improve adhesion before complete removal of the resist in acetone. Fig. 4.6 shows a hBN and graphene flake transferred to a target substrate using this technique. Taking a closer look at this sample via AFM and SEM (fig. 4.7(a) and (b) respectively) reveals that wrinkles in the graphene have emerged. $\mu\mathrm{m}^2$-sized, flat areas of graphene ruptured by $\approx 50 - 100\,\mathrm{nm}$ wide wrinkles are visible. We believe that water trapped between graphene and hBN created these wrinkles during the drying process. Another possible explanation is shrinking of the PMMA when baked at temperatures higher than 80 °C, while it is still attached to the graphene. The impact of these wrinkles on the device performance remains to be examined in experiments.

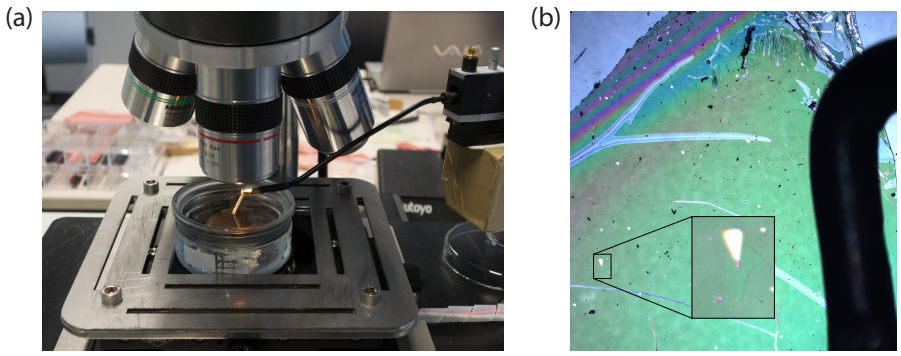

Figure 4.5: Setup for wedging transfer of graphene and boron nitride. (a) The PMMA flake, floating on the water surface, can be aligned to the sample using a micro manipulator. For precise alignment, the sample (attached to the bottom of the beaker) can be moved in x and y-direction with a piezoelectric stage. (b) Transfer of a PMMA mask containing a hBN flake (magnified in the inset) on top of the pre-patterned back-gate electrode of sample SP34. Fig. 4.6(b) shows the device after transfer of the graphene. We remove the intercalated water with a nitrogen gun and subsequently by heating the substrate. The PMMA mask is fixed to the substrate by a metallic clamp attached to the micro manipulator, visible on the right hand side of the image.

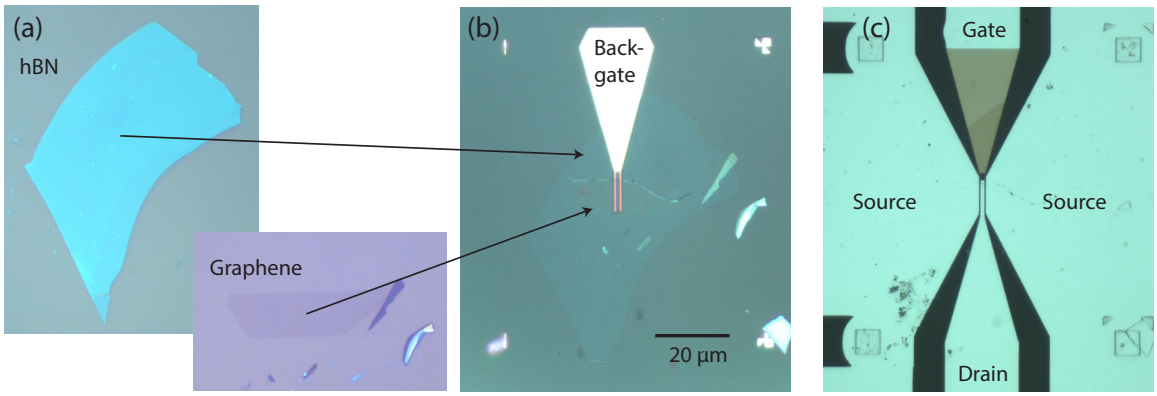

Figure 4.6: Fabrication of sample SP34: (a) hBN and monolayer graphene are exfoliated on SiO_2 for better contrast. (b) Both flakes are transferred sequentially onto the bottom gate situated on a sapphire substrate. Note that the top edge of the graphene flake has partially curled during transfer. (c) Final device with Ti/Al source and drain contacts. The transparent hBN dielectric is still visible on top of the metallic bottom gate.

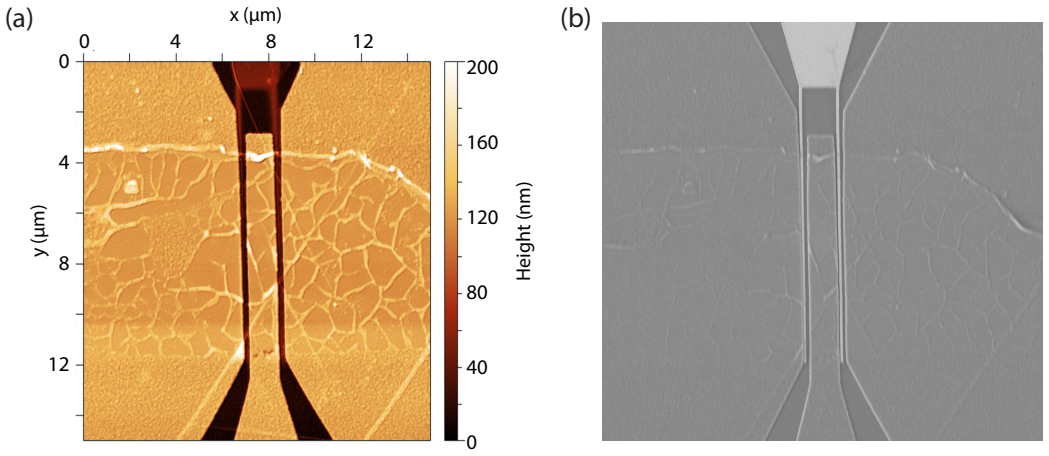

Figure 4.7: Wrinkles in the graphene made visible by AFM (a) and SEM (b) images of sample SP34 (identical scales). The wrinkling is likely to be caused by the wet-transfer technique and may have a negative impact on the device performance.

4.2 DC characterization

A total of 10 graphene-on-hBN GFETs were fabricated and measured, 6 of which operate at extrinsic transit frequencies exceeding 0.1 GHz. Their specifications are listed in table 4.1. In the following, the two best performing devices SP34 (monolayer) and SP46 (bilayer) are discussed. All of the devices were fabricated and characterized entirely at KIT. Fig. 4.8 shows the transfer characteristics of the two GFET. For better comparability of the curves taken at different drain-source voltage, we again plot the total drain-source resistance R_{ds} versus D/e. In both samples, we observe the Dirac point very close to zero gate voltage, indicating little extrinsic doping of the graphene, as expected for hBN substrate. The residual doping may originate from oxygen due to small amounts of water, trapped during the transfer process. With increasing drain voltage, the Dirac point shifts due to additional bias-induced doping of

sample	layer	l_{g}	l_{ch}	w_{ch}	t_{hBN}	$I_{\mathrm{ds,max}}$	$g_{\mathrm{m,max}}^{\mathrm{RF}}$	$f_{\mathrm{T,ex}}$	$f_{\mathrm{T,in}}$	f_{max}
unit		nm	nm	µm	nm	mA/µm	µS/µm	GHz	GHz	GHz
SP34	mono	100	300	8	12	0.58	90	6.4	61	10.5
SP37	mono	100	500	9	5.4	-0.39	64	4.6	25	13.9
SP43	mono	100	300	13	40	-0.75	17	2.3	N/A	5.4
SP40	bi	100	300	11.8	N/A	0.78	6	0.65	N/A	N/A
SP41	bi	200	450	10	≈ 55	0.47	19	1.7	N/A	0.8
SP46	bi	100	500	18.2	57	-0.85	20.5	3.0	38	N/A

Table 4.1: Table of graphene-on-hBN FET, listing number of layers, gate length (l_{g}), channel length (l_{ch}), channel width (w_{ch}), thickness of the dielectric layer (d_{hBN}), maximum drain current and transconductance, embedded and de-embedded transit frequency ($f_{\mathrm{T,ex}}$ and $f_{\mathrm{T,in}}$) and maximum oscillation frequency f_{max}.

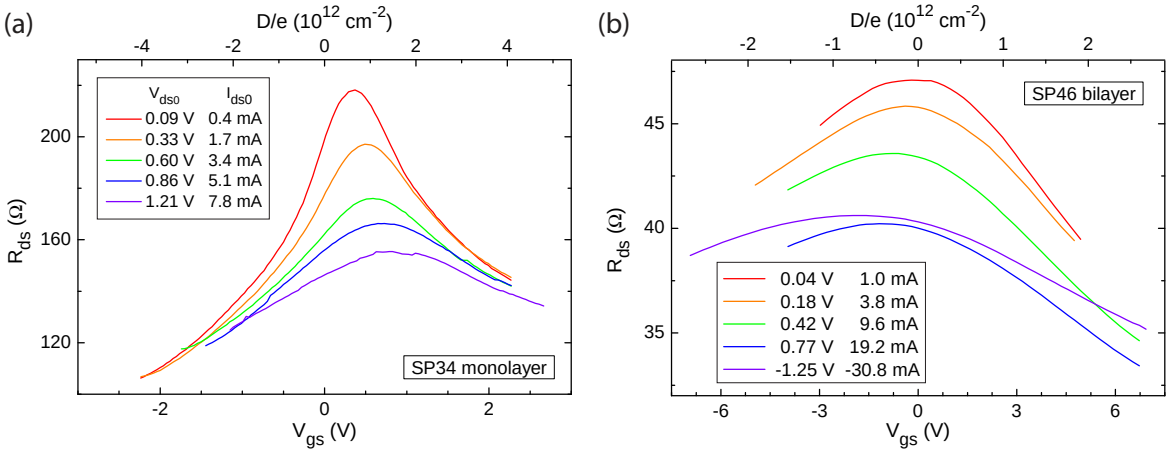

Figure 4.8: Transfer characteristics of (a) SP34 (monolayer graphene) and (b) SP46 (bilayer graphene) for various drain-source voltages. Only one sweep direction is shown for better graphical representation. The hysteresis is minimal however, $\leqslant 0.1\,\mathrm{V}$ (SP34) and $\leqslant 0.6\,\mathrm{V}$ (SP46).

the channel. At the same time the ratio between on- and off-current decreases as a result of short-channel effects.[146] There is also a slight asymmetry between the hole and electron branches. Due to the workfunction missmatch, our Ti/Al contacts p-dope the graphene locally, creating a p-n junction at the metal/graphene interface for positive gate voltages in the electron branch.[97,98] Comparing the two samples, we find several differences: In the bilayer graphene device, the ratio between on and off-current is smaller than in the monolayer device. We attribute the reduction in gate modulation to the interlayer screening in bilayer graphene. Due to the five-fold thicker hBN dielectric of the bilayer device, a larger gate voltage range is needed to map the Dirac peak. The corresponding range of the displacement field is smaller, therefore the Dirac peak appears broader in fig. 4.8. Lastly, with increasing bias voltage, the Dirac point shifts into the positive direction for the monolayer device whereas for the bilayer device, it shifts to negative gate voltage. In both samples, we find very small hysteresis in the transfer characteristics corresponding to $\Delta D/e = 1.8 \cdot 10^{11}\,\mathrm{cm}^{-2}$ (monolayer) and $\Delta D/e = 2.3 \cdot 10^{11}\,\mathrm{cm}^{-2}$ (bilayer). This is another indication for reduced unintentional doping of the graphene channels.

Output characteristics of SP34 are shown in fig. 4.9. The device responds with an almost linear increase in drain current to rising drain voltage, with a slight onset of saturation at high bias. Full current saturation is not achieved within the measured drain voltage range. Still we observe sizable maximum drain currents of $0.6\,\mathrm{mA/\mu m}$.

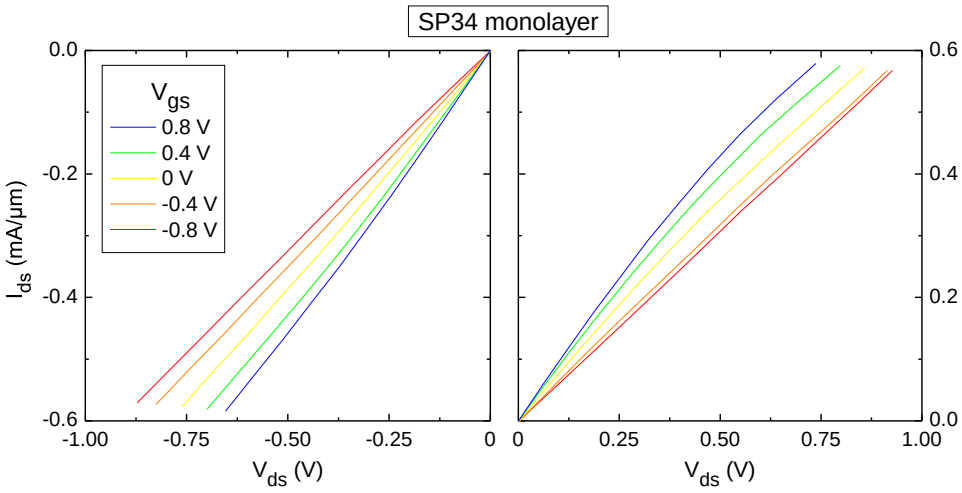

Figure 4.9: Output characteristics of sample SP34. Clear gate dependence is observed as we sweep the gate voltage from $-0.8\,\mathrm{V}$ to $0.8\,\mathrm{V}$ in $0.4\,\mathrm{V}$ steps. Within the probed voltage range, the device still operates in the linear regime, although a slight curvature is visible starting at $\pm 0.25\,\mathrm{V}$. Unfortunately, output characteristics of the bilayer sample are not available for comparison.

4.3 Microwave characterization

High-frequency analysis was carried out using a Rhode & Schwarz ZVA40 network analyzer with a custom made probe station, see chapter A.5.2 in the appendix for details. The setup is capable of S parameter measurement at frequencies of up to 40 GHz. Accurate calibration of the VNA was performed before each measurement session with a calibration substrate (CSR-8) specifically designed for the utilized probes.

In the monolayer device (SP34) at bias voltages $V_{\mathrm{gs}} = 0.48\,\mathrm{V}$ and $V_{\mathrm{ds}} = 0.8\,\mathrm{V}$, we find maximum transit frequencies of $f_{\mathrm{T}} = 6.4\,\mathrm{GHz}$ (extrinsic) and $f_{\mathrm{T}} = 61\,\mathrm{GHz}$ (intrinsic), derived from current gain measurements (see fig. 4.10). Agreement with the $1/f$ dependence of the current gain $|\mathrm{h}_{21}|$ up to highest frequencies can be observed. However, small wiggles appear for frequencies above $\sim 2\,\mathrm{GHz}$. Reasons for this may be the time delay of up to several hours between measurement of the GFET and the de-embedding structures and influences of standing waves in the RF-setup. Also the calibration of the VNA degrades over time, leading to slight deviations. Fig. 4.11(a) shows the intrinsic and extrinsic transit frequency of the device depending on the drain-source bias conditions. Initially, with increasing drain-source voltage, f_{T} increases, as expected. However, after a peak at $V_{\mathrm{ds}} = 0.8\,\mathrm{V}$, the performance declines again. The reason for this behavior is twofold: At high bias the effect of the gate loses impact, also the FET operates out of equilibrium, as increased V_{ds} dopes the graphene channel. The device offers a maximum RF transconductance of $g_{\mathrm{m,max}}^{\mathrm{RF}} = 90\,\mu\mathrm{S}/\mu\mathrm{m}$. We reach a maximum oscillation frequency of $f_{\mathrm{max}} = 10.5\,\mathrm{GHz}$ (see fig. 4.11(b)) which is larger than $f_{\mathrm{T,ex}}$, but considerably smaller than $f_{\mathrm{T,in}}$ as expected for graphene FET[13]. The frequency dependence of both maximum available gain (MAG) and unilateral power gain U follows the typical $1/f^2$ dependence.

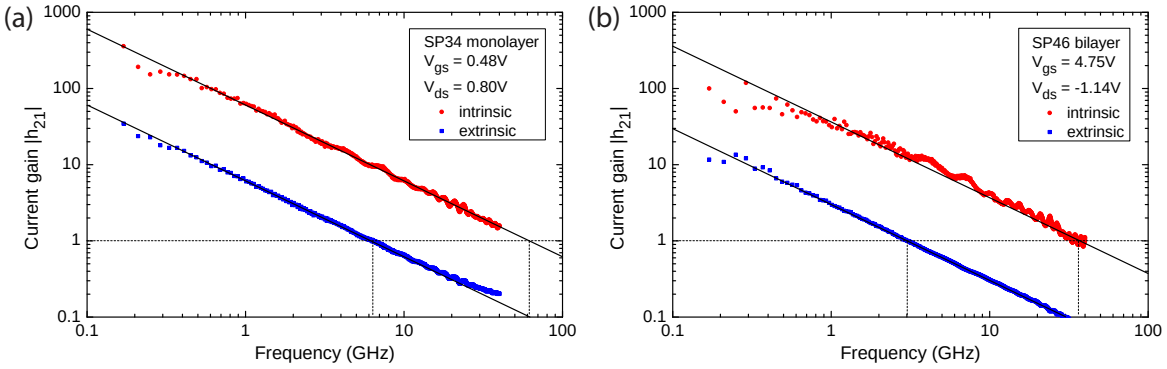

Figure 4.10: Current gain of the embedded (blue) and de-embedded (red) device, resulting in transit frequencies of (a) $f_{\mathrm{T,ex}} = 6.4\,\mathrm{GHz}$ and extrapolated intrinsic $f_{\mathrm{T,in}} = 61\,\mathrm{GHz}$ for SP34 monolayer graphene and (b) $f_{\mathrm{T,ex}} = 3.0\,\mathrm{GHz}$ and $f_{\mathrm{T,in}} = 38\,\mathrm{GHz}$ for SP46 bilayer graphene device, respectively. Black lines indicate the ideal $1/f$ dependence.

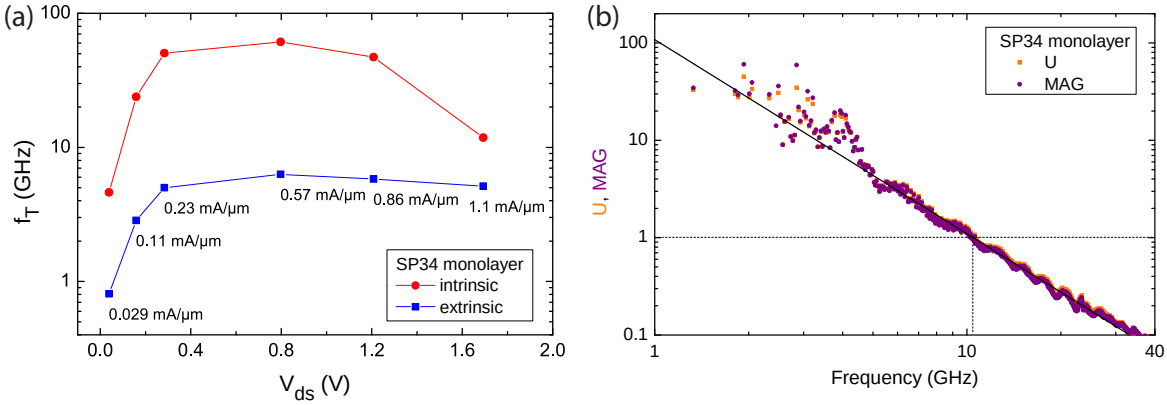

Figure 4.11: (a) Transit frequencies versus drain-source voltage. Each data point is labeled with the corresponding drain-source current density. $f_{\mathrm{T,in}}$ peaks at $V_{\mathrm{ds}} = 0.8\,\mathrm{V}$. Note the very high current density of $1.1\,\mathrm{mA/\mu m}$ at $V_{\mathrm{ds}} = 1.7\,\mathrm{V}$. (b) Maximum available gain (purple) and unilateral power gain (orange) both reach unity at $f_{\mathrm{max}} \approx 10.5\,\mathrm{GHz}$. Both follow the ideal $1/f^2$ slope indicated by a black line.

Our bilayer graphene device (SP46) reaches maximum $f_{\mathrm{T,ex}} = 3.0\,\mathrm{GHz}$ and $f_{\mathrm{T,in}} = 38\,\mathrm{GHz}$ at bias voltages $V_{\mathrm{gs}} = 4.75\,\mathrm{V}$ and $V_{\mathrm{ds}} = -1.14\,\mathrm{V}$. Lower performance than in the monolayer device is expected since the gate is twice as long in the bilayer device (considering $f_{\mathrm{T}} \sim 1/l_{\mathrm{g}}$, refer to chapter 2.3).

Both devices show best RF performance for gate voltages $V_{\mathrm{gs}} < V_{\mathrm{Dirac}}$, where the conduction is governed by holes. We note that for these devices, the ratio $r_{\mathrm{in/ex}}$ of intrinsic f_{T} to extrinsic f_{T} (SP34: $r_{\mathrm{in/ex}} = 9.5$, SP46: $r_{\mathrm{in/ex}} = 12.7$) is approximately two to three times smaller than in the monolayer graphene-on-sapphire sample (SP15: $r_{\mathrm{in/ex}} \approx 27$). The reason for this is the much larger channel width present in the hBN-based devices, leading to a higher intrinsic capacitance. Therefore, the ratio of parallel parasitic capacitance of the de-embedding

structure to intrinsic capacitance of the device is much smaller.

4.4 Discussion of metal bottom-gated GFET

We have fabricated and characterized graphene FETs on hexagonal boron nitride substrate. In our device layout the hBN serves both as substrate for the graphene and as dielectric for the bottom gate. One monolayer and one bilayer graphene device were presented in detail. In both devices, the charge neutrality point is close to zero gate voltage and very little hysteresis is observed compared to the graphene-on-sapphire devices. This is an indicator for a decreased amount of residual charge traps and the cleanliness of the hBN substrate. Within the probed gate voltage range, the transfer characteristics response is close to linear, as expected for short channel devices.[58] The devices operate at high current densities of up to 1.1 mA/µm, equal to comparable hBN-based GFETs reported by Wang et al.[142] However, we did not find a significant improvement of the charge carrier mobility.

We probed the high-frequency response of the GFET at frequencies of up to 40 GHz and extract maximum transit frequencies $f_T = 61$ GHz for the monolayer and $f_T = 38$ GHz for the bilayer device. Extrapolation of f_T is justified as a continuous trend of the current gain is observed, closely following the $1/f$ dependence within the full measurement range. The monolayer device offers larger $f_{max} = 10.5$ GHz and a larger f_{max}/f_T ratio than our graphene-on-sapphire FET. At the time of publication (January 2013)[147] the devices marked the record f_T for monolayer and bilayer graphene-on-hBN FET, respectively.[141,142,148]1 Although our GFETs reach substantial f_T, the performance is lower than in devices with comparable gate lengths fabricated on regular substrates such as SiC[21] or highly resistive Si[22]. We attribute the lack of improvement of f_T and g_m through hBN to the formation of bubbles and wrinkles in the graphene during the wet transfer process. These transfer-induced wrinkles were also reported in similar works.[142] They represent unintended scattering centers which markedly decrease the charge carrier mobility. The creation of wrinkles could be reduced using an optimized, water-free transfer process.[50] Also, the hBN crystals might have been bent more strongly in the vicinity of the gate fingers and contacts as anticipated (depicted in the idealized schematic in fig. 4.3). The bending of the hBN crystal is imposed on the graphene introducing an additional source of scattering. One could embed the bottom gate into the substrate, following Meric et al.[148] However, this process is elaborate as it requires precise etching of the substrate and smooth polishing of its surface.

1 It has to be noted however, that the competing hBN-based GFET exhibit longer gate lengths, resulting in lower transit frequencies.

4.5 Graphene bottom gates

Inspired by the idea to minimize the thickness of the bottom gate for improved hBN flatness, we explore in this chapter the use of graphene as gate material for our high-frequency FET. Graphene has been used successfully as gate electrode in multiple field-effect devices.[94,149,150,151] Park et al. increased the performance of a nonvolatile flash memory by using monolayer graphene as the top-gate material.[149] According to the authors of this study, the stretchable graphene gate reduces mechanical stress which normally is induced on the dielectric by metallic top gates, thereby improving the dielectric quality. Also, tunneling currents are limited due to the high work function of graphene. All-carbon based transistors using graphene as source, drain and bottom gate material were demonstrated recently.[94,150] S. Lee et al. fabricated an all-graphene FET used for quaternary digital modulations[94] and G. Lee et al. realized a gate electrode made from few-layer graphene with hBN dielectric used in a MoS_2 FET.[152] However, graphene had not been used as gate material for microwave GFET before. Extremely thin, flexible and transparent gate electrodes made of graphene could open up new applications for high-frequency GFETs.

Fig. 4.12 shows the schematics of our device layout, where we replace the metal bottom gate by few-layer graphene. Using this layout, only one metal evaporation step is required. A total of three devices was fabricated (see table 4.2) out of which the two best-performing devices (SP38 and SP48, both feature monolayer graphene channels and a graphene gate length of 100 nm) are analyzed in detail in this chapter.

4.5.1 Dry transfer technique

To avoid formation of wrinkles due to trapped water between graphene and substrate, we use a more advanced "dry-transfer" process, depicted in fig. 4.13.[50] We begin by exfoliation of graphene or hBN crystals on top of a Si substrate covered by a layer of PMMA. Next,

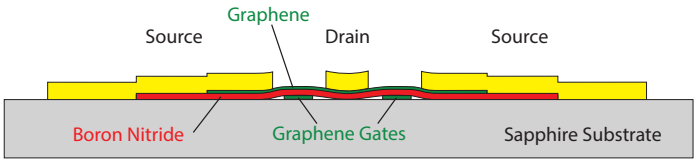

Figure 4.12: Schematic of the graphene-on-hBN device layout using a graphene bottom gate. The smaller thickness of the graphene gate ($\approx 2\,\mathrm{nm}$) compared to the metal gate ($\approx 30\,\mathrm{nm}$) improves flatness of the graphene channel above.

sample	layer	l_g	l_{ch}	w_{ch}	t_{hBN}	$I_{ds,max}$	$\lvert g_{m,max}^{RF} \rvert$	$f_{T,ex}$	$f_{T,in}$	f_{max}
unit		nm	nm	µm	nm	mA/µm	µS/µm	GHz	GHz	GHz
SP24	mono	100	500	3.1	N/A	0.52	61	1.3	≈ 14.3	0.3
SP38	mono	100	500	12.5	≈ 4	0.26	85	3.2	≈ 20.5	0.9
SP48	mono	100	500	13.6	≈ 4	0.31	113	4.8	≈ 30	1.5

Table 4.2: List of graphene-on-hBN FET with graphene gate.

the same steps as described in the previous transfer technique (chapter 4.1.1) are followed until the PMMA has fully detached from the substrate and flows on the water surface. As the crystals are located on top of the PMMA layer, they never come into direct contact with water. A metal frame with a hole in the center is inserted into the beaker. While slowly removing the water from the beaker with a syringe, we align the crystal on top of the PMMA layer to the center of the circular hole in the metal frame. When all water is removed, the PMMA layer conforms neatly to the metal frame. Meanwhile, the target substrate is fixed to the heatable and rotatable sample holder, located in the center of our piezo stage (see fig. 4.13). The metal frame supporting the flake-PMMA stack is flipped by 180° and attached to the stage. Lifting the sample holder reduces the distance to the PMMA layer which starts adhering to the substrate immediately after first contact. Heating the sample holder can speed up and improve the adhesion while also reducing the amount of residual water between substrate and graphene or hBN. After transfer, the sample can be spin-coated with yet another layer of resist to cure it. Again, the sample is baked at 165 °C for 30 min to improve adhesion before the resist is removed by acetone. Lastly the samples are cleaned in a vacuum furnace.

We begin fabrication of the graphene bottom gate by exfoliating graphene on sapphire substrate. After locating sufficiently large few-layer graphene sheets, we use a negative resist (ma-N 2403, thickness 300 nm) to define the dual-gate-finger layout. The graphene is etched by RIE with an oxygen plasma. The remaining fabrication steps are identical to those of the metal bottom gate devices. Fig. 4.14 exemplarily visualizes the preparation of a graphene-gated sample (SP38).

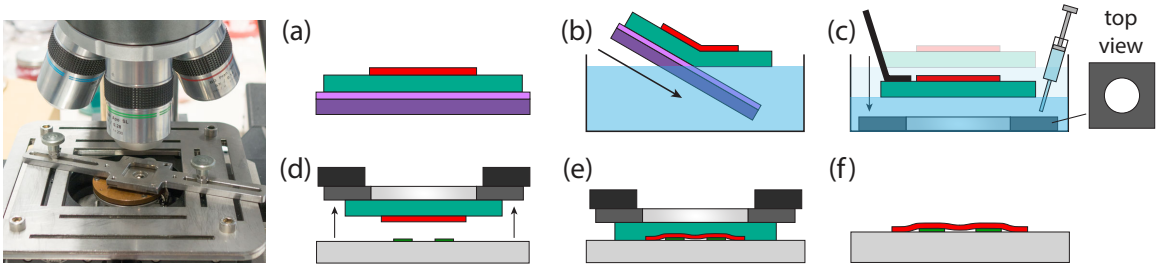

Figure 4.13: Schematic of the "dry" transfer technique, explained exemplarily for hexagonal boron nitride. (a) HBN (red) is deposited on Si/SiO_2 substrate which we spin-coated with a thick layer of PMMA (turquoise). (b) The sample is slowly immersed into a beaker filled with distilled water. As the hBN faces upwards, it does not come in contact with water at any stage of the process. (c) The hBN is roughly aligned to the hole centered in a metallic transfer frame, attached to the bottom of the beaker. We remove the water with a syringe, until the PMMA mask attaches to the metal frame. (d) Fixed to a movable scaffold, the frame can be aligned to the graphene bottom gate on the underlying target substrate (see image on the left). (e) We heat the substrate and bring it into contact with the hBN/PMMA stack. The heat softens the PMMA and causes it to detach from the metal frame. (f) After drying the sample in a furnace, the PMMA is removed by acetone.

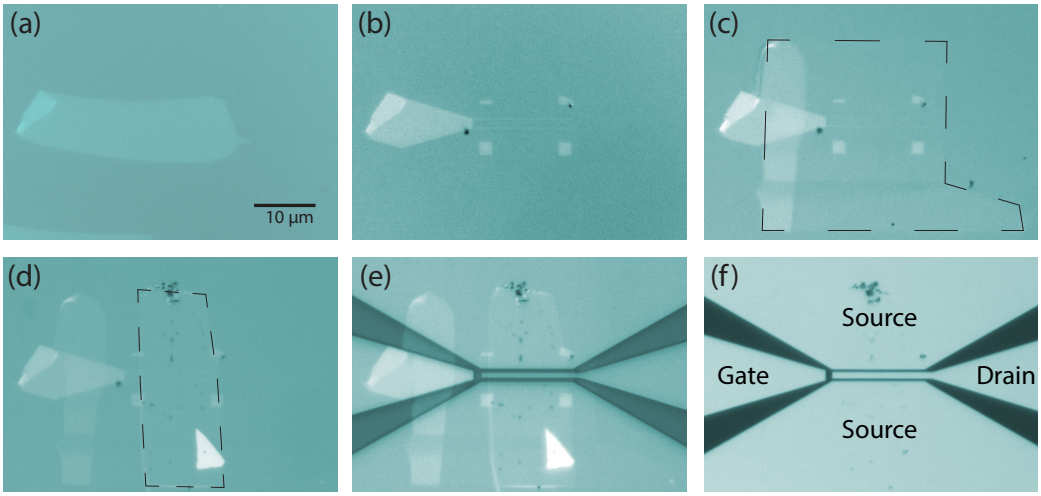

Figure 4.14: SP38 fabrication steps: (a) Exfoliation of few-layer graphene on sapphire substrate. (b) Etching of graphene bottom gate and markers for subsequent alignments. (c) Transfer of hBN crystal and (d) monolayer graphene channel, their shapes are indicated by dashed lines. (e) Developed PMMA mask for gate, drain and source electrode deposition. (f) Final device with metallic electrodes.

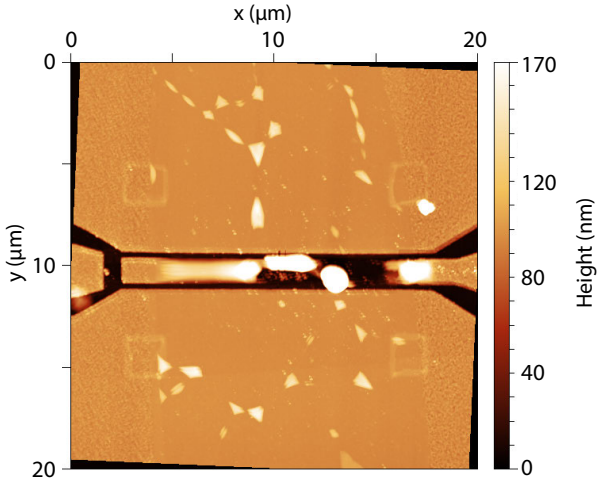

Figure 4.15: AFM image of sample SP38 (after device breakdown). The amount of wrinkles in the graphene has decreased dramatically. Still some bubbles are visible which most likely have formed due to trapped air during transfer.

4.6 DC characterization

Comparison of the transfer characteristics of both graphene bottom-gated samples (fig. 4.16) to the metal bottom-gated device (SP34, monolayer graphene) reveals several similarities: In both types of devices, the Dirac point shifts towards positive gate voltages with increasing drain bias while the on/off current ratio decreases, albeit much less pronounced. Again the Dirac point is located very close to $V_{\mathrm{gs}} = 0$ in both samples, indicating low amounts of charged impurities in the hBN dielectric. We observe a very narrow peak with a strong electron/hole asymmetry which is reversed with respect to the metal bottom gate device. Therefore, we expect maximum transistor performance in the electron-governed conductance branch, at gate voltages in the range of $V_{\mathrm{gs}} = 0.3\,\mathrm{V}$ to $V_{\mathrm{gs}} = 0.5\,\mathrm{V}$ where the largest slope of the transfer characteristics occurs.

The distribution of the output characteristics (shown in fig. 4.17) is comparable to that of the metal-gate device. However, the drain-source currents are smaller due to reduced conductivity of the channel, especially in the second sample. We observe a slight onset of saturation for positive V_{ds} in both samples.

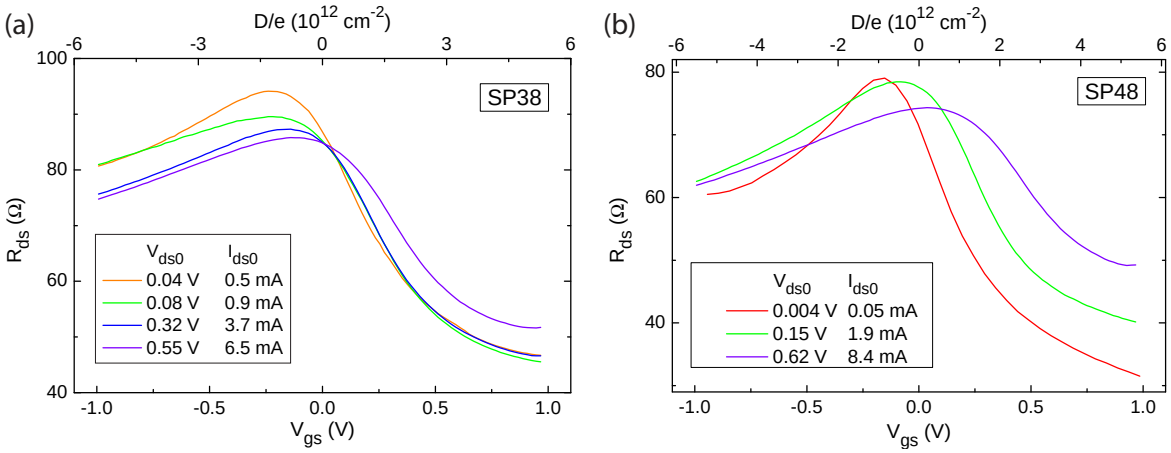

Figure 4.16: Transfer characteristics of the graphene-gated samples (a) SP38 and (b) SP48

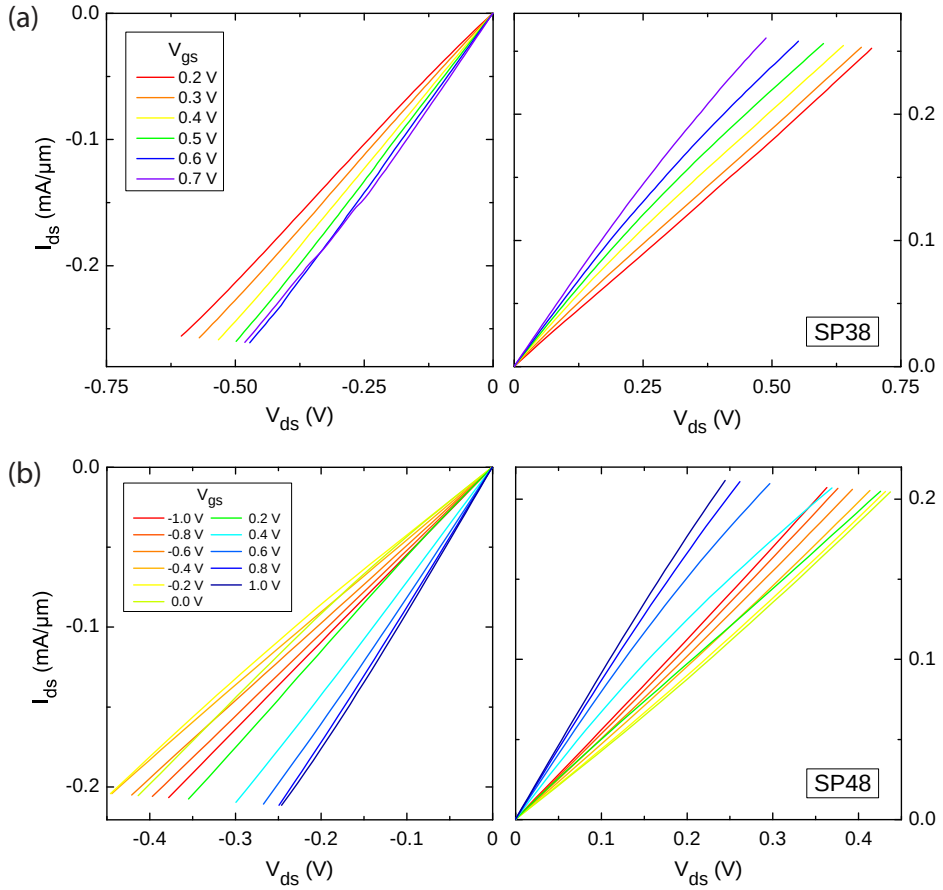

Figure 4.17: Output characteristics of (a) SP38 and (b) SP48. For bottom gate voltages between $V_{\mathrm{gs}} = 0.4\,\mathrm{V}$ and $V_{\mathrm{gs}} = 0.6\,\mathrm{V}$, SP48 begins to saturate slightly.

4.7 Microwave characterization

High-frequency probing of the graphene bottom-gated devices was carried out in the same fashion as described for previous samples. However, it has to be noted that the *short* structures we used for de-embedding are fully metallic. These structures may not exactly mirror the graphene gates. Therefore, the de-embedded data has to be regarded as an approximation to the real intrinsic GFET characteristics. Current gain plots of both devices are presented in fig. 4.18. Maximum transit frequencies occur at gate voltages $V_{\mathrm{gs}} = 0.35\,\mathrm{V}$ (SP38) and $V_{\mathrm{gs}} = 0.53\,\mathrm{V}$ (SP48), as expected from dc measurements. At high frequencies we observe a deviation of the FET-characteristic from the $1/f$ dependence for both embedded and de-embedded data. The intrinsic current gain deviates only slightly at highest frequencies, which we attribute to the aforementioned possibly inaccurate de-embedding procedure. In the extrinsic device, the deviation occurs in form of a kink at rather low frequencies $f_{\mathrm{kink}} = 0.9\,\mathrm{GHz}$ in SP38 and $f_{\mathrm{kink}} = 1.5\,\mathrm{GHz}$ in SP48. Interestingly, these frequencies also correspond to the maximum frequencies of oscillation f_{max} of these devices. We assume that

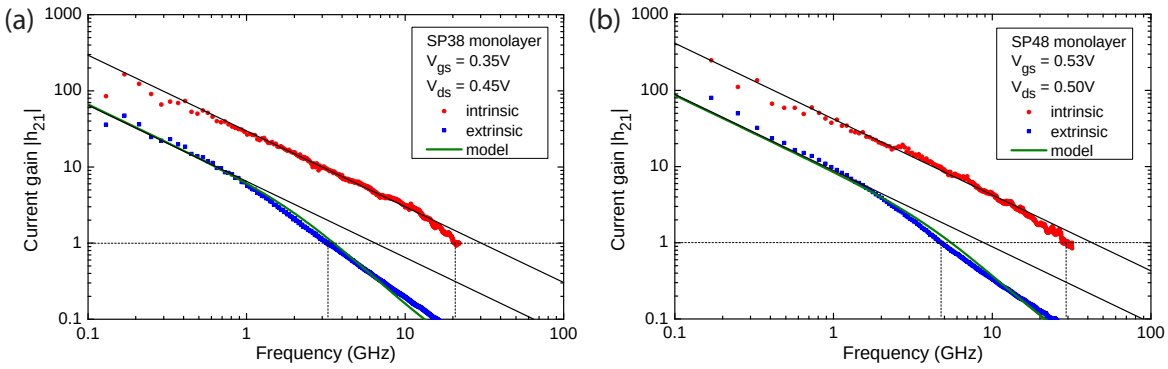

Figure 4.18: Embedded (blue) and de-embedded (red) current gain of both graphene bottom gate devices. SP38 (a) reaches peak transit frequencies of $f_{\mathrm{T,ex}} = 3.2\,\mathrm{GHz}$ and $f_{\mathrm{T,in}} \approx 20.5\,\mathrm{GHz}$, while in SP48 (b) we achieve slightly higher values of $f_{\mathrm{T,ex}} = 4.8\,\mathrm{GHz}$ and $f_{\mathrm{T,ex}} \approx 30\,\mathrm{GHz}$ respectively. The kink in the extrinsic current gain can be described well by our model (green curves).

the graphene bottom gate is responsible for a very high gate access resistance R_{g} which in turn causes a more rapid decline in current gain at high frequencies. An approximation with a simplified small-signal model[153] can give further insight. The simplified circuit used in this model (sketched in fig. 4.19) includes only the most important parameters to describe the GFET, such as the gate resistance R_{g}, transconductance g_{m}, pad capacitance C_{pg}, and total gate capacitance $C_{\mathrm{g}} = C_{\mathrm{gd}} + C_{\mathrm{gs}}$ consisting of the gate to drain and gate to source capacitances. According to the model, the frequency dependence of the current gain can be described by

$$h_{21}(\omega) = \frac{(g_{\mathrm{m}} - i\omega C_{\mathrm{gd}}) \cdot (\omega R_{\mathrm{g}}(C_{\mathrm{gd}} + C_{\mathrm{gs}}) - i)}{\omega(1 + i\omega R_{\mathrm{g}}(C_{\mathrm{gd}} + C_{\mathrm{gs}})) \cdot (i\omega R_{\mathrm{g}}(C_{\mathrm{gd}} + C_{\mathrm{gs}})C_{\mathrm{pg}} + C_{\mathrm{pg}} + (C_{\mathrm{gd}} + C_{\mathrm{gs}}))}. \quad (4.1)$$

C_{pg} and g_{m} are static parameters which can be extracted from the measured S parameters of the *open* structure (C_{pg}) and the active device (g_{m}). The parameters R_{g}, C_{gd}, and C_{gs} remain to be adjusted as fitting parameters. For sample SP38, using the measured/extracted

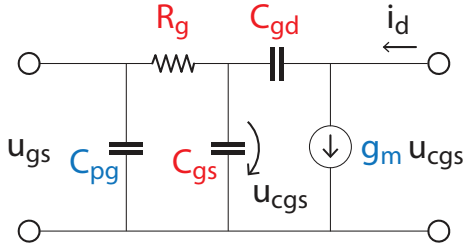

Figure 4.19: Sketch of our simplified small-signal model, derived from[153]. The elements highlighted in blue can be extracted from the measured S parameters, whereas the red elements are fitting parameters. We neglect all inductances as well as drain and source series resistances, as these parameters have little effect on R_{g}. *Source: after*[153].

static parameters $g_m = 2.0\,\mathrm{mS}$ and $C_{pg} = 29.8\,\mathrm{fF}$, our model yields $C_{gd} \approx 17\,\mathrm{fF}$, $C_{gs} \approx 1.0\,\mathrm{fF}$, and $R_g \approx 6.5\,\mathrm{k\Omega}$. Similarly for sample SP48, with $g_m = 2.6\,\mathrm{mS}$ and $C_{pg} = 31.2\,\mathrm{fF}$, we obtain $C_{gd} \approx 13.8\,\mathrm{fF}$, $C_{gs} \approx 2.9\,\mathrm{fF}$, and $R_g \approx 3.3\,\mathrm{k\Omega}$. We note that the gate resistances found by this method are roughly two orders of magnitude larger than in the metal bottom-gated device. This large gate resistance is mainly responsible for the deviation of the current gain from the ideal $1/f$ dependence at high frequencies. Also, since $f_{max} \sim 1/\sqrt{R_g}$, the rather low f_{max} values of the graphene-gated devices are little surprising.

Lastly, we examine the S parameters to get a better understanding of the two differently gated GFETs. In fig. 4.20 we compare the two best-performing devices of each kind, sample SP34 (metal bottom gate) and SP48 (graphene bottom gate). A polar plot is chosen for best visual representation. S_{11}, the input voltage reflection coefficient, is a measure of the device impedance mismatch to Z_0 (typically $50\,\Omega$). The level of impedance mismatch defines the amount of reflection - with increasing frequency, S_{11} is expected to rise. The graphene bottom gate device has a wider channel which is located closer to the gate, increasing the gate-coupling capacity. Therefore we would expect the graphene gate device to be more reflective than the metal gate device at higher frequencies. However, the opposite is the case which we explain by two effects: For very thin gate dielectrics (here $t_{hBN} \approx 4\,\mathrm{nm}$), the quantum capacitance plays an increasingly important role (refer to chapter 1.4).[154,155] As the quantum capacitance is connected in series with the gate capacitance, the overall gate capacitance may in fact be much smaller than assumed.[11] Secondly, compared to the metal bottom gates that are more than one order of magnitude thicker, fringing fields are substantially reduced in the few-layer graphene bottom gate. S_{12}, the reverse voltage gain, is an indicator for the back-coupling of the electromagnetic fields from the graphene channel into the gate. While the effect increases with rising frequency in the metal-gated device, it is suppressed in the graphene-gated device for high frequencies. The voltage amplification

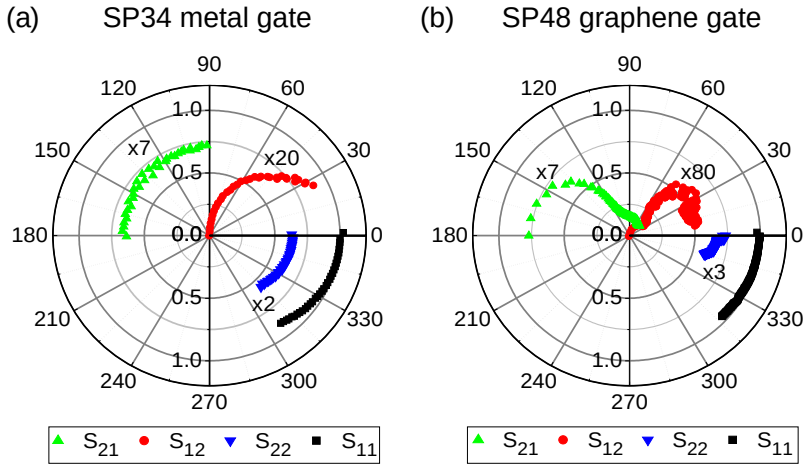

Figure 4.20: Polar plot of the S parameters corresponding to the best current gain of (a) SP34 (metal bottom gate) and (b) SP48 (graphene bottom gate). The frequency ranges from 10 MHz to 40 GHz (clockwise). Individual parameters were scaled up for better visibility, as indicated in the plot.

factor S_{21} is low but comparable to other studies. We attribute this to insufficient current saturation leading to a rather large output conductance of $\approx 100\,\mathrm{mS}$ in both devices. The deviation of S_{21} at high frequencies is due to the large gate access resistance in the graphene gate device. Lastly, the output voltage reflection coefficient S_{22} is similar in both devices, decreasing slightly at higher frequencies.

4.8 Conclusions

We have fabricated graphene FET using standard metal bottom gates as well as bottom gate electrodes made of few-layer graphene. The devices have equal gate lengths and comparable channel widths. Transfer of the hBN and monolayer graphene flakes was carried out with a technique avoiding direct contact with water, leading to a drastic decrease of wrinkles in the graphene. Despite a more then tenfold reduction in thickness, the graphene-gated devices reach intrinsic transit frequencies by only a factor of two to three lower than the corresponding metal-gated device. In the graphene-gated devices larger gate resistances were observed which lead to slower charge reversal in the gate fingers and thus to slightly lower transit frequencies. Our work represents the first successful use of graphene as gate material for microwave FET.[147] In the graphene gated devices, the as-measured current gain deviates from the typical $1/f$ dependence which we attribute to the large gate resistance. We extracted R_g from our simplified small-signal model. The large gate resistance combined with the persistently high output conductance is also the reason for reduced maximum available gain in these samples. Nevertheless, due to suppressed back-coupling from the channel into the gate, our graphene-gated device could be used in applications where high source/load back-action isolation is required.

Our few-layer graphene-gated GFET are transparent ($\approx 85\,\%$ transmission of visible light) and extremely thin with a cumulative device thickness of approximately 7 nm (excluding the metallic leads). They could be used in circuitry where currently rare and expensive transparent conductive materials like ITO are employed. For further device improvement the thickness could be reduced using monolayer graphene as gate electrode. Although we realized an enhanced transfer process, PMMA-based transfer always leaves behind traces of polymer. Improvement of the sample cleanliness could be achieved through a polymer-free transfer, e.g. using a polydimethylsiloxane (PDMS) stamp.[156] There is also progress in direct growth of hBN[141,157] and subsequent growth of graphene on hBN.[158] Following this path, transfer-free all-carbon GFETs with hBN substrate and dielectric might be realized in the future.

5 Large scale optimization of graphene FET

The devices presented in the previous chapters lack two important properties: reproducibility and comparability. Since the integration of several of our GFETs into an amplifier is intended, the capability of producing identical transistors with well defined characteristics is needed. Using exfoliated graphene and boron nitride, this goal is hard to achieve, since each crystal flake has a different shape resulting in varying properties thus making it virtually impossible to design the same GFET twice. The rather extensive and time-consuming preparation of this type of devices impedes the systematic characterization with respect to multiple device properties, which is needed to optimize the geometry of our GFET.

For geometry optimization, large numbers of GFET with varying gate length have to be fabricated and characterized. For best comparability, all devices are to be fabricated simultaneously on one chip, using a homogeneous large-area graphene film. To meet the required homogeneity and reduce production spread, we use CVD-grown graphene films, as these offer relatively consistent properties. However, due to unavoidable cracks and grain boundaries in CVD graphene, we expect noticeable lower device performance compared to exfoliated graphene. As to the gate dielectric, we reverted to the well established homogeneous ALD growth of aluminum oxide. However, we grew thinner films than in the previous samples to increase the gate capacitance and thereby the effectivity. These material choices enable us to fabricate hundreds of devices on one chip within a reasonable time frame.

While optimizing the device design, we implemented several measures reducing contact resistance (refer to chapter 1.5), compatible with our fabrication process. Inspired by the work of Franklin et al.[77] we use a layout for our GFET where the graphene sheet is connected by top and bottom contacts, as shown in fig. 5.1(h). Following Smith and coworkers[81], we pattern the graphene channels underneath the contacts by vertical cuts (see fig. 5.1(i,j)). These cuts decrease the area of the graphene while creating additional edges to improve charge carrier injection.[65] Only 70 % of the devices were etched in this fashion to allow verification of the positive effect of this modification.

We realized a total of 280 similar devices on one chip (sample SP75/76), varying only the gate length while leaving all other device dimensions identical to achieve optimum device comparability. Fig. 5.2 shows a detail of the GFET array and a zoom into the active area of three individual GFETs. The channel length is kept constant at $l_{\mathrm{ch}} = 1400\,\mathrm{nm}$ in all devices to allow for $\pm 200\,\mathrm{nm}$ realignment error at the maximum gate length of 1000 nm. Due to the similar layout of all devices, only one type of *open* de-embedding structures is needed, as these do not contain the gate fingers. With each row of GFETs (28 devices) we increase the gate length: 50 nm, 100 nm (2 rows), 200 nm, 300 nm, 400 nm, 500 nm (2 rows), 750 nm, and 1000 nm. We expect to achieve current saturation for long gates with $l_g > 300\,\mathrm{nm}$.[159]

Similar to the double contacts, we extend our layout to local double gates. Local double gates for graphene device were proposed recently[160], but have not been reported experimentally

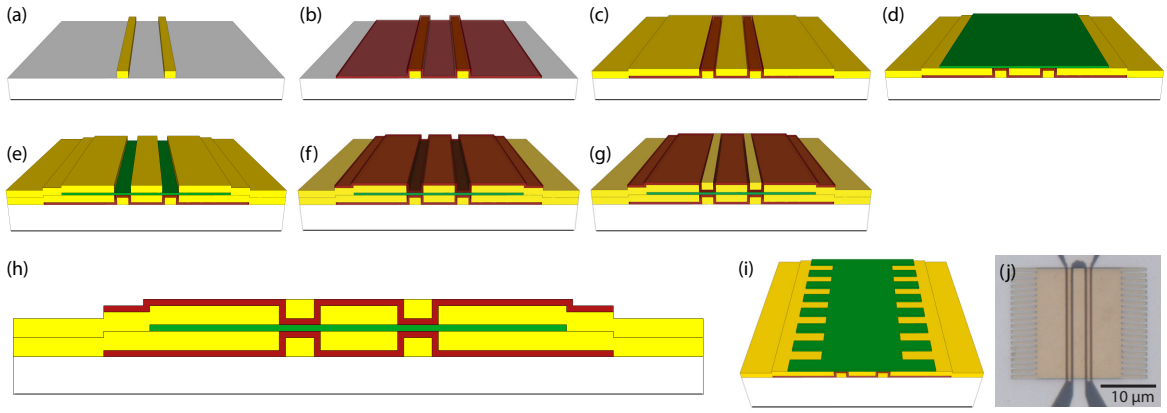

Figure 5.1: Fabrication steps of the doubly clamped graphene FET in sample SP75/76. (h) The graphene (green) is sandwiched between two vertically symmetrical contacts (yellow), dielectric layers (red) and gates (yellow). (a) First, the bottom gate (Ti/Au $5/20\,\mathrm{nm}$) is covered locally by (b) a layer of ALD-grown Al_2O_3 ($8\,\mathrm{nm}$). (c) After deposition of the bottom contacts (Ti/Au $5/20\,\mathrm{nm}$), (d) a CVD-grown graphene film is transferred and etched into rectangular channels. (e) Top contacts are evaporated (Ti/Au $5/40\,\mathrm{nm}$) and the devices are covered locally by (f) a second layer of Al_2O_3 ($8\,\mathrm{nm}$). A top gate is patterned in half of the devices (g). (f) Single and (g) double-gated GFETs are fabricated simultaneously side by side and are strictly identical except for the additional metallic top gate. (i) Schematic of a patterned graphene channel. The cuts reduce the graphene area but increase the length of its edges. (j) Picture of the actual etch mask with cut width and gap distance of $500\,\mathrm{nm}$ each.

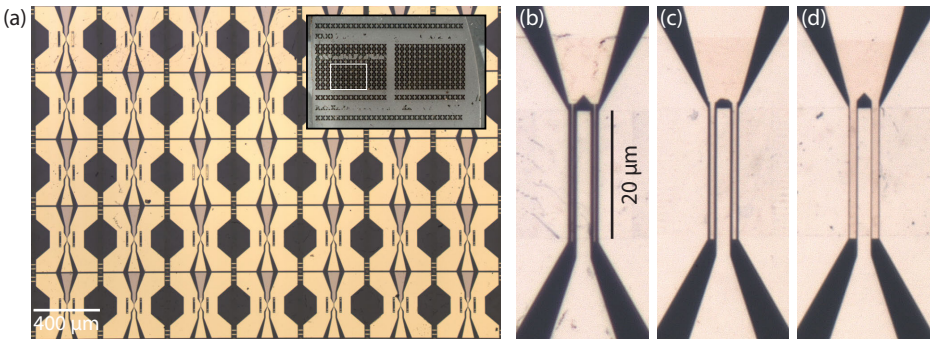

Figure 5.2: (a) Array of GFETs. The whole sample SP75/76 is shown in the inset. (b-d) Zoom into the channel region of three representative devices with various gate lengths ($l_g = 100/500/1000\,\mathrm{nm}$). The channel length is fixed to $l_{ch} = 1400\,\mathrm{nm}$ in all devices for better device comparability.

so far. In our layout, the top- and bottom-gate fingers are on the same electric potential. We expect enhancement of the gate effect through the mirrored electric field and the increased gate capacitance. We prepared half of the devices exclusively with bottom gates whereas the other half is equipped with bottom and top gates. Both bottom and top dielectric layers are grown with the same thickness (8 nm) to provide identical electric field strength to both sides of the graphene.

The devices are fabricated in the same fashion as the samples described in previous chapters. However, as we use CVD-grown graphene deposited on Si substrate, a customization of our new dry-transfer technique is required (see fig. 5.3).

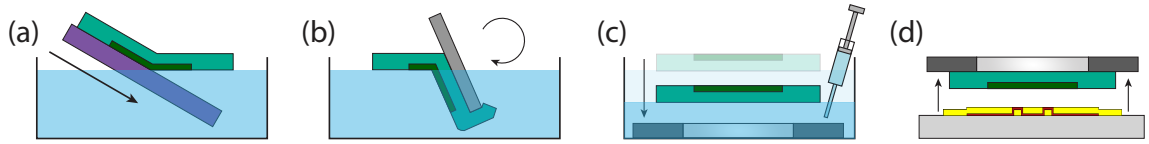

Figure 5.3: The transfer process is a mixture of the "wet" and "dry"-transfer techniques described in chapter 4. (a) CVD graphene on Si substrate is spin-coated with PMMA and immersed into distilled water. (b) After detachment, the PMMA/graphene stack is flipped by 180 ° so that the graphene faces upwards. (c) The graphene is roughly aligned to the hole in the metallic transfer frame while removing the water with a syringe. The PMMA/graphene stack is dried in a furnace at 160 °C to remove adsorbed films of water. (d) We align the metal frame to the GFET structures on the target substrate. The remaining steps are equivalent to the "dry"-transfer technique, refer to fig. 4.13.

5.1 Device comparison - DC analysis

In total, ≈ 160 out of the available 280 devices were measured and characterized. In general we find that devices with identical geometry exhibit similar dc characteristics. However, as the CVD graphene film contains cracks and holes, the channels of some devices are partially damaged. This is reflected in noticeably higher resistivity and reduced high-frequency performance.

We begin by discussing four representative GFETs, all with a gate length of 500 nm. Each of these devices represents another type (single/double-gated, patterned/unpatterned contact area). Analysis of the corresponding low-bias transfer characteristics (left panel in fig. 5.5) shows that in all devices the Dirac point is shifted towards positive gate voltages. This positive doping is due to the charge transfer coming from the work-function mismatch between graphene and the contacting metals (Ti/Au). We observe similar hysteresis in all of the devices, which we attributed to similar amounts of charged impurities introduced by the aluminum oxide dielectrics. At higher drain voltages, the Dirac point is shifted considerably due to bias-induced doping (not shown in fig. 5.5). In all devices, an electron/hole asymmetry in favor of hole conduction is observed. The patterned graphene devices offer slightly higher on-off ratios. In these devices we also observe a steeper slope in the vicinity of the Dirac point, which corresponds to higher transconductance.

Transport characteristics of the devices are shown in the right-hand panel of fig. 5.5. While the single-gated devices exhibit rather linear IV curves, current saturation is achieved in

the double-gated devices at high negative drain source bias $V_{ds} < -1.0\,V$ for gate voltages $V_{gs} < -0.4\,V$. The double-gated GFETs reach higher drain currents at equivalent drain voltages, while offering stronger current saturation. We observe an asymmetry in I_{ds} for positive and negative drain voltage which can be explained by the Dirac point not being located at zero gate voltage.

In the following, we explicitly examine the transfer curves of the double-gated, patterned device (SP75_L10, fig. 5.5(d)). The output characteristics of the other three devices are similar but the described effects are less pronounced. With increasing positive drain voltage, the Dirac point is shifted to positive gate voltage up to $V_{gs} \geq 2\,V$. Therefore, the transfer curves for different gate voltages do not cross. With decreasing gate voltage, their slope becomes slightly sublinear, but current saturation is not achieved. The situation is different for negative drain bias. For better visual representation, the negative I-V curves of the device are shown in fig. 5.4. Here, the Dirac point is shifted bias-induced from $V_{gs,Dirac} = 1.2\,V$ at $V_{ds} = -0.05\,V$ to $V_{gs,Dirac} = -0.4\,V$ at $V_{ds} = -2.6\,V$. The negative bias transfer curves can be divided into three gate-voltage regimes. For V_{gs} between $2\,V$ and $0.8\,V$, where the conduction is governed by electrons, the transfer curves run superlinear without indication of current saturation. In the regime close to the Dirac point ($V_{gs} = 0.4\,V$ to $-0.8\,V$), the GFET cycles through the four regions discussed in chapter 2.2: the transfer curves begin with a linear region, then current saturation sets in roughly between $V_{ds} = -0.5\,V$ and $-1.7\,V$, followed by a second linear region. In the last regime (gate voltages below $-0.8\,V$), the saturation is even more pronounced and no second linear region can be observed.

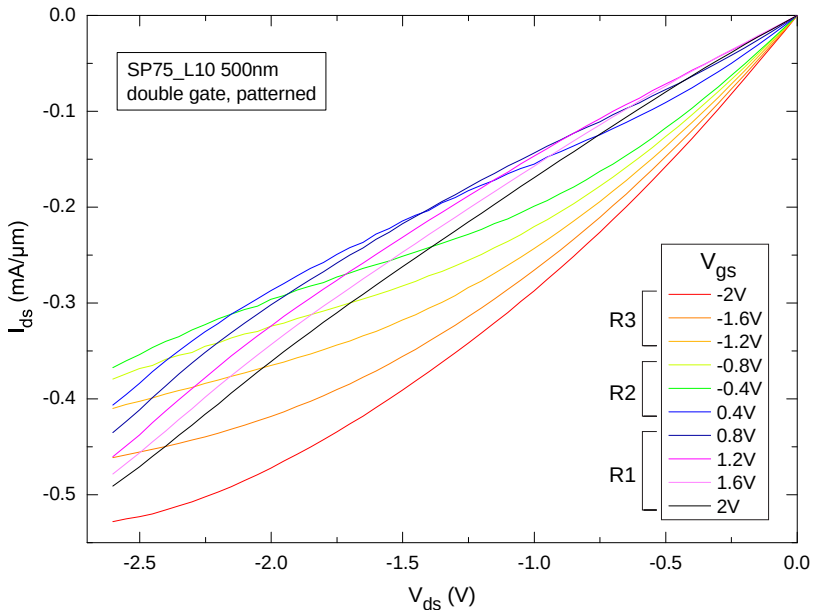

Figure 5.4: Depending on the gate voltage, the output characteristics of GFET SP75_L10 ($l_g = 500\,nm$) are superlinear (R1, $V_{gs} = 2\,V$ to $0.8\,V$), can be described by the four regions discussed in ch. 2.2 (R2, $V_{gs} = 0.4\,V$ to $-0.8\,V$), or show current saturation at high negative bias (R3, $V_{gs} < -0.8\,V$).

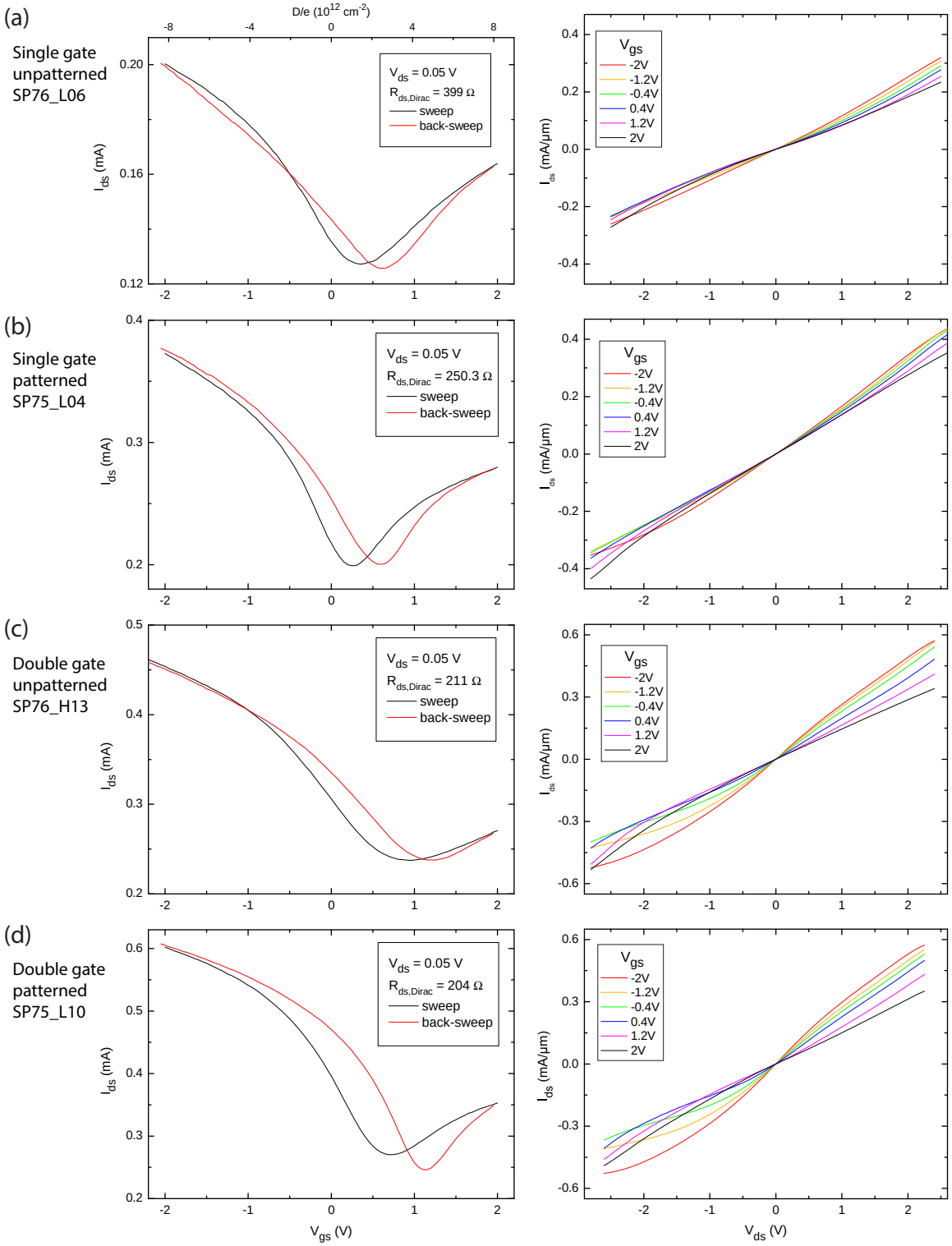

Figure 5.5: Transfer and transport characteristics of representative single-gated (a,b) and double-gated (c,d) graphene FET. The total drain-source resistance at the Dirac point is given by $R_{\mathrm{ds,Dirac}}$. The effect of the additional gate is clearly visible in the amount of drain current modulation. The graphene in (b,d) was patterned with cuts of $500\,\mathrm{nm}$ width. An increase in drain current compared to the non patterned devices can be observed.

Next, we analyze the dependence of the transport characteristics on the gate length. In figure 5.6 the IV-curves for devices with gate length from 50 nm to 1000 nm are plotted. The scale is kept constant in all plots for best comparability of the graphs. For each gate length, the curves of a single-gated and a double-gated device are presented side by side. All selected devices have patterned graphene channels (except for $l_g = 1000\,\mathrm{nm}$ due to insufficient data), as we usually observe lower drain-source resistances in these GFET. Apart from this, the selection of the devices for our comparison occurred arbitrarily. Several identical devices with similar performance exist for each device presented in the following.

We limit the discussion to the negative drain-source bias region, as the positive bias region corresponds to linear output characteristics in practically all devices, as previously seen in the $l_g = 500\,\mathrm{nm}$ GFET. Since in all devices hole-governed conduction is enhanced, we show only data for negative gate voltages in the range of $-2\,\mathrm{V} \leq V_{gs} \leq -0.4\,\mathrm{V}$, as here strongest current saturation is observed.

We find that for short gate length (50 nm to 200 nm) the IV curves are almost linear even at high bias. In the single-gated devices, this trend suppressing saturation continues up to gate lengths of 500 nm. Contrarily, in the double-gated devices a clear onset of saturation is observed from $l_g = 200\,\mathrm{nm}$ onward. The effect of the gate on the drain current is substantially more pronounced than in all corresponding single-gated devices. For gate length $> 400\,\mathrm{nm}$, current saturation begins to takes place for both types of devices at high negative bias ($V_{ds} \leq -1\,\mathrm{V}$). The effect of current saturation increases steadily with increasing gate length. Especially in the double-gated GFET with the highest gate length of 1000 nm (fig. 5.6(d)), at high bias the drain current is almost independent of the bias voltage. The saturation performance of this device compares well with a single-gated $l_g = 2\,\mu\mathrm{m}$ device reported by Bai et al.[159]

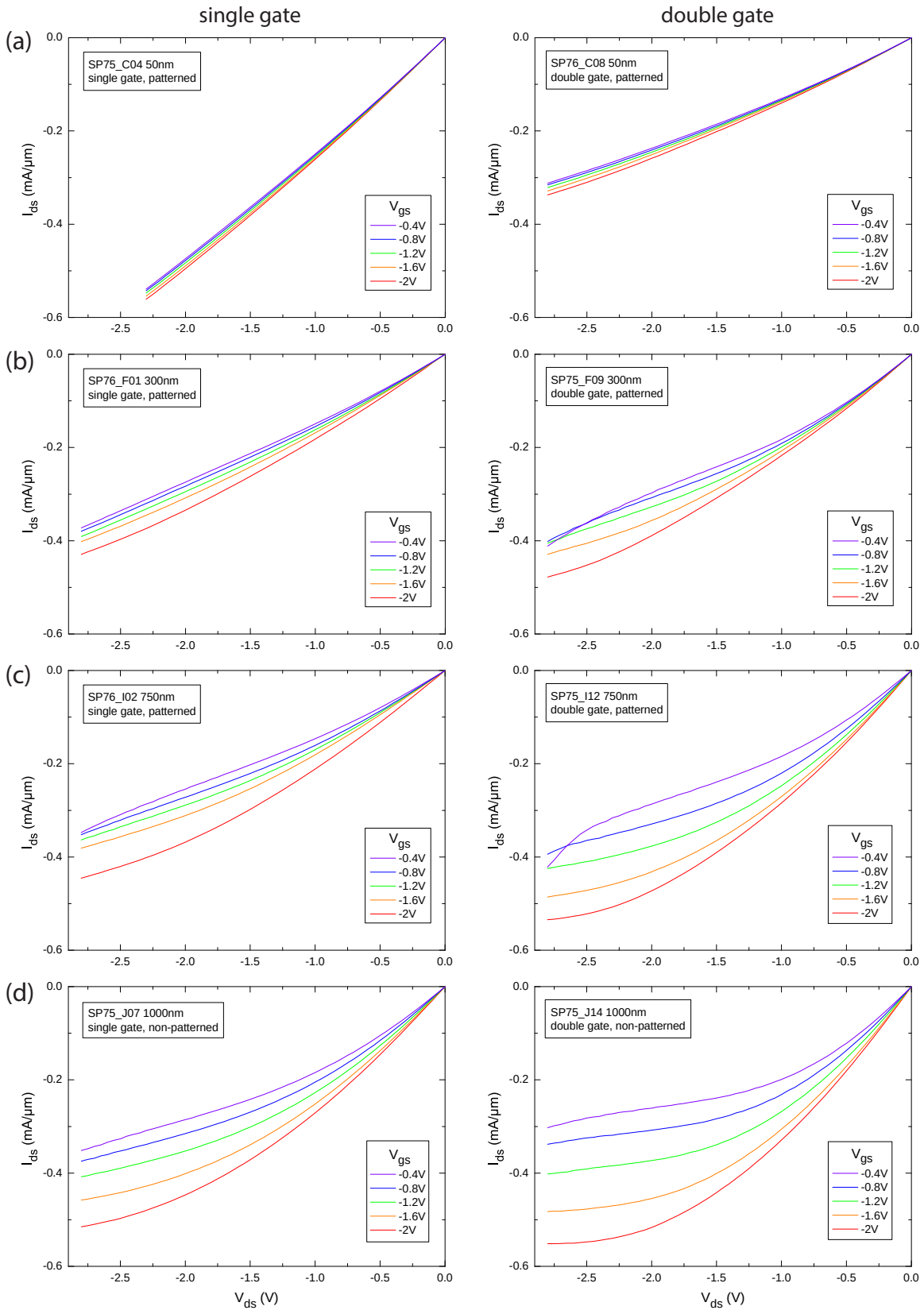

Figure 5.6: Transport characteristics of representative single and double-gated GFET in the negative drain bias regime. The gate length varies from of $50\,\mathrm{nm}$ to $1000\,\mathrm{nm}$.

5.2 High-frequency characterization

We begin our high-frequency analysis by extracting the FET parameters using the small signal model from chapter 2.2. The parameters of all GFET discussed in the previous sub-chapter are given in table 5.1. The pad capacitances (C_{pg}, C_{pd}), source and drain resistances (R_{s}, R_{d}), and inductances (L_{g}, L_{d}, L_{s}) vary only slightly. They are independent of the gate length, as these parameters are extracted solely from the *open* and *short* de-embedding structures. Each device was measured on a different date, with renewed calibration of the VNA. The small variation ($< 4\,\%$ on the average) of these parameters is an indicator of the high accuracy of the de-embedding procedure. R_{g} decreases only weakly with increasing l_{g}, as the *short* structures take the length of the gate fingers into account. However, no difference in R_{g} is observed for single- or double-gated devices. The source inductance L_{s} is too small in all GFET and could not be extracted.

The parameters g_{m}, C_{gd}, C_{gs}, C_{ds} and R_{i} on the other hand are proportional (R_{i} inversely proportional) to the gate length. g_{m} and C_{gs} are shown representatively in fig. 5.7. In all cases, a substantial difference is observed between single and double-gated devices. g_{m} increases on average by $100\,\%$ in the double-gated devices, and similar behavior is observed for the remaining parameters: C_{gd} ($92\,\%$ increase), C_{gs} ($57\,\%$ increase), C_{ds} ($75\,\%$ increase), and R_{i} ($50\,\%$ decrease). Considering the different device geometries, we would have expected an effective doubling of the total gate capacitance $C_{\mathrm{g}} = C_{\mathrm{gs}} + C_{\mathrm{gd}}$ for the double gate. However, in these devices C_{g} increases only by $75\,\%$ on the average. As g_{m} grows in a more pronounced fashion than C_{g}, we expect higher transit frequencies according to the small-signal equivalent circuit (refer to chapter 2.3)

$$f_{\mathrm{T,in}}^{\mathrm{model}} = \frac{g_{\mathrm{m,in}}}{2\pi} \frac{1}{C_{\mathrm{gs}} + C_{\mathrm{gd}}} \tag{5.1}$$

compared to single-gated devices of the same gate length. Indeed, we find very good agreement

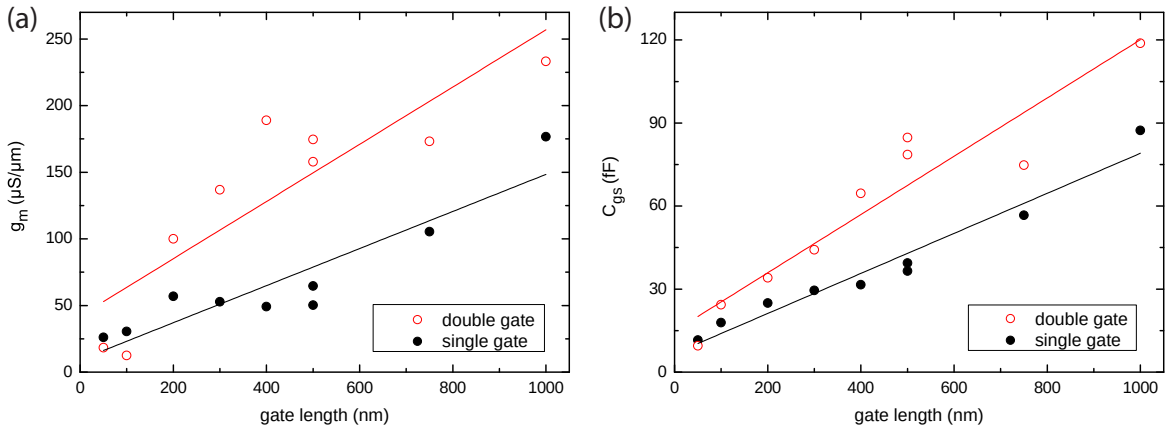

Figure 5.7: (a) RF transconductance and (b) gate-source capacitance of the single and double-gated GFETs.

device name	type	l_g	$f_{T,ex}$	$f_{T,in}$	$f_{T,in}^{model}$	f_{max}	g_m	C_{gd}	C_{gs}	C_{ds}	C_{pg}	C_{pd}	R_g	R_s	R_d	R_i	L_g	L_d
unit		nm	GHz	GHz	GHz	GHz	µS/µm	fF	fF	fF	fF	fF	Ω	Ω	Ω	Ω	pH	pH
SP76_C04	SG, P	50	3.0	8.3	8.7	1.0	26.0	7.6	11.6	27.3	27.7	29.7	12.6	0.60	12.4	697.3	97.7	99.0
SP75_K04	SG, P	100	3.4	8.4	7.4	4.4	30.5	8.5	17.9	36.9	28.1	29.5	13.1	0.61	12.2	236.3	93.8	92.1
SP76_E05	SG, P	200	4.4	8.0	7.8	4.8	56.8	21.5	25.0	63.3	26.6	30.0	12.4	0.61	12.2	221.4	98.1	94.0
SP76_F01	SG, P	300	4.0	6.9	6.9	5.0	52.8	19.4	29.5	63.7	27.4	28.9	11.8	0.61	12.8	154.6	93.8	98.5
SP76_G02	SG, P	400	3.7	5.9	5.3	4.4	49.0	27.0	31.6	78.2	26.6	29.2	11.2	0.59	12.4	164.4	89.6	100.1
SP76_L06	SG, NP	500	3.2	5.1	5.4	3.8	50.3	23.0	36.5	74.7	27.6	29.3	11.0	0.61	11.9	164.9	94.9	92.5
SP75_L04	SG, P	500	4.4	6.7	6.3	6.2	64.8	26.2	39.4	85.8	26.6	29.6	11.0	0.61	12.6	143.9	89.6	99.6
SP76_I02	SG, P	750	4.9	6.7	6.2	5.6	105.5	50.8	56.7	144.2	26.6	29.1	10.7	0.61	12.0	112.4	87.5	90.1
SP75_J07	SG, NP	1000	5.7	7.3	7.2	6.7	176.5	69.0	87.3	211.3	27.1	29.3	10.4	0.59	12.0	71.9	94.3	92.7
SP76_C08	DG, P	50	2.3	7.2	7.4	1.6	18.4	6.3	9.5	21.2	27.7	29.7	12.6	0.60	12.4	516.3	97.7	99.0
SP75_K09	DG, P	100	1.0	1.9	2.0	0.7	12.4	15.3	24.3	55.8	26.7	30.4	12.0	0.60	12.1	184.9	87.8	97.2
SP76_E10	DG, P	200	5.7	9.3	9.1	6.3	100.0	35.8	34.0	96.0	28.1	30.1	12.5	0.61	12.8	158.4	93.4	95.5
SP75_F09	DG, P	300	7.9	12.4	10.1	9.3	136.8	42.0	44.2	117.8	27.0	29.5	11.9	0.62	12.7	137.5	96.0	98.7
SP75_G08	DG, P	400	7.7	10.9	10.0	7.9	189.0	56.2	64.6	169.4	26.6	29.2	11.2	0.59	12.4	89.0	89.6	100.1
SP76_H13	DG, NP	500	6.0	7.6	6.7	7.4	158.0	66.5	84.8	197.2	26.6	29.6	11.0	0.61	12.6	64.9	89.6	99.6
SP75_L10	DG, P	500	6.6	8.5	7.9	7.7	174.5	61.6	78.6	189.2	26.6	29.6	11.0	0.61	12.6	72.6	89.6	99.6
SP75_I12	DG, P	750	6.2	8.4	7.2	6.4	173.3	77.6	74.8	200.4	26.6	29.1	10.7	0.61	12.0	86.9	87.5	90.1
SP75_J14	DG, NP	1000	5.3	6.6	5.9	6.6	233.3	134.0	118.8	357.0	27.1	29.3	10.4	0.59	12.0	48.9	94.3	92.7

Table 5.1: AC parameters extracted from the S parameters of the GFET and *open* and *short* de-embedding structures. The table is separated into single-gated (SG, upper half) and double-gated (DG, lower half) devices.

between $f_{\mathrm{T,in}}^{\mathrm{model}}$ values calculated from eq. 5.1 and $f_{\mathrm{T,in}}$ of current gain (h_{21}) extractions from the de-embedded S parameters (see table 5.1). Analysis of the current gain reveals an only weak dependence of the intrinsic transit frequency on the gate length (fig.5.8). For the single-gated devices, $f_{\mathrm{T,in}}$ increases for short l_{g}, whereas for the double-gated GFET the gate length dependence is more pronounced with $f_{\mathrm{T,in}}$ peaking at 300 nm. The current gain of both types of GFETs for $l_{\mathrm{g}} = 300\,\mathrm{nm}$ is plotted in fig. 5.9. We observe slight deviation from the $1/f$ slope in the embedded as well as the de-embedded current gain plots, especially for frequencies below 1 GHz. In both types of devices, the ratio $r_{\mathrm{in/ex}}$ decreases with increasing gate length. This is to be expected as the intrinsic capacitance rises with the gate length while the parallel parasitic capacitance of the embedding structure stays constant. With increasing gate length, the maximum oscillation frequency approaches $f_{\mathrm{T,in}}$, as a direct consequence of the increasing current gain (fig. 5.10).

Nevertheless, the high-frequency performance is lower than one could have expected, especially for short gate lengths. It has to be considered, however, that a different type of graphene was used for fabrication of the GFET in this chapter. The quality of the large-area CVD graphene (grown on Cu) does not reach that of exfoliated graphene yet. Apart from local defects, surfactants from the copper etchant and multiple transfers deteriorated its electronic properties. Additionally, the graphene channels are in contact with the Al_2O_3 dielectric layers for top and bottom gate, degrading the mobility. The rather low intrinsic transit frequencies, especially for short gate length, are due to the chosen device geometry: The goal of this study was to create comparable devices, therefore the layout of all devices is identical except for the gate length. Accordingly, in a device with $l_{\mathrm{g}} = 50\,\mathrm{nm}$ only a fraction of 1/28 of the 1.4 µm long graphene channel is gated actively. The ungated parts of the channel lead to high access resistances,[20,161] which would have been avoided in an individually optimized layout with a shorter channel.

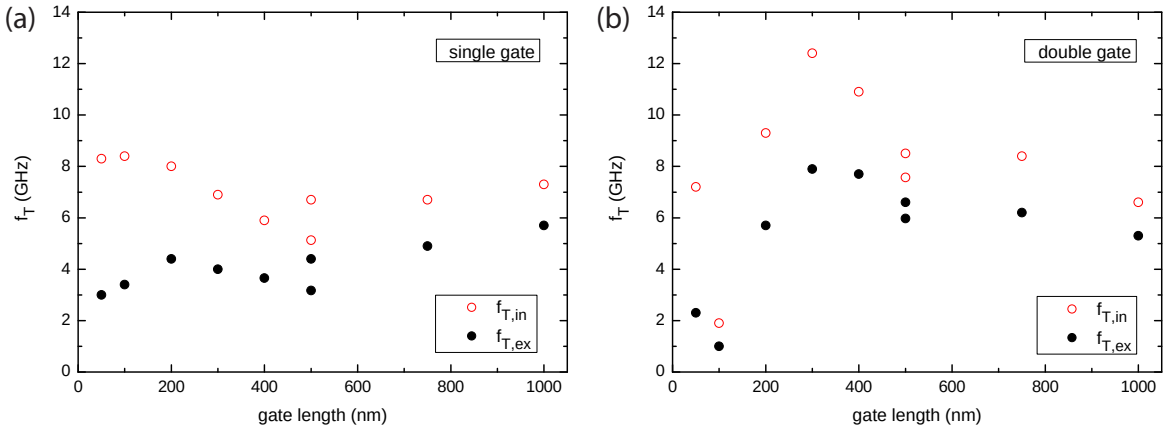

Figure 5.8: High-frequency performance of the single and double-gated GFET. In most cases, the double-gated devices exhibit higher f_{T}.

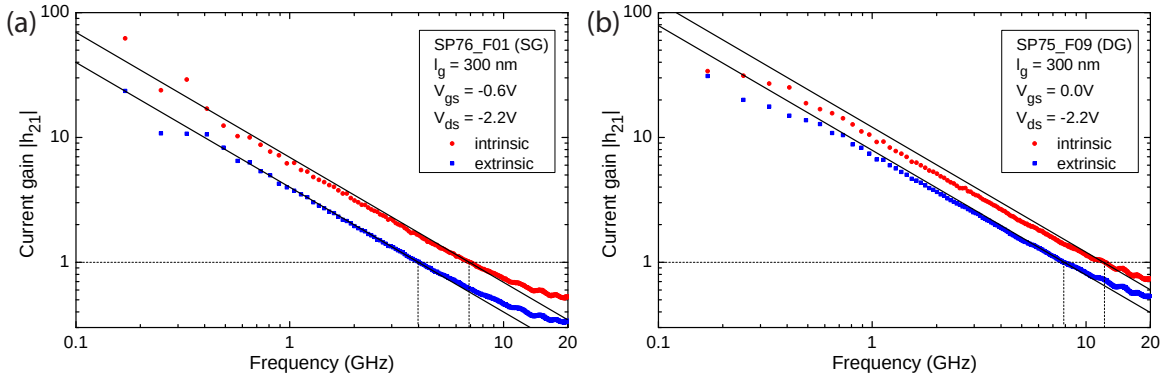

Figure 5.9: As measured and de-embedded current gain of a (a) single-gated and a (b) double-gated GFET, both with a gate length of $300\,\mathrm{nm}$.

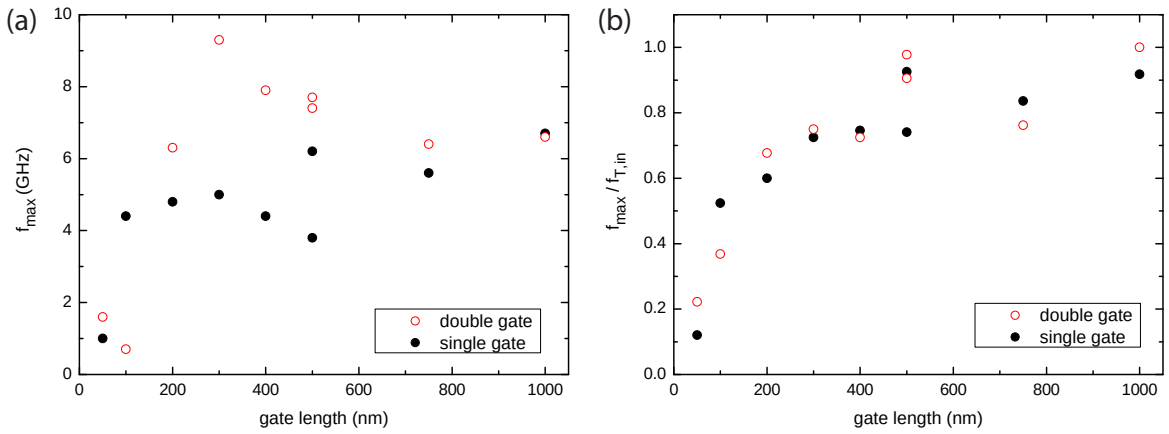

Figure 5.10: Comparison of f_{max} of the single and double-gated GFET. Towards longer gate length, f_{max} adapts to values close to $f_{\mathrm{T,in}}$.

5.3 Conclusions

We have fabricated an array of graphene field-effect transistors with varying gate lengths from 50 nm to 1000 nm. A yield of $> 50\,\%$ is achieved, and we find that devices with identical geometry exhibit similar transfer and transport characteristics. In this work we experimentally realized local double-gating of graphene for the first time. Devices with local top and bottom gates are compared to equivalent GFETs with only bottom gates of the same gate length. We show that the effectivity of the double-gates is larger compared to single-gates of equal gate length, enabling larger drain currents at equivalent drain bias. In both types of devices, current saturation is achieved due to drain-source bias-induced shifting of the Dirac point. In single-gated devices, complete current saturation occurs for $l_{\mathrm{g}} = 1000\,\mathrm{nm}$ whereas in double-gated devices, it is observed already for $l_{\mathrm{g}} \geq 400\,\mathrm{nm}$. The additional gate doubles the achievable transconductance while the total gate capacitance is only increased by $75\,\%$ leading to higher intrinsic transit frequencies $f_{\mathrm{T,in}}$ compared to single-gated devices. The maximum

oscillation frequency $f_{\max}$ adapts to the same values as the intrinsic transit frequency for $l_g \geq 400\,\mathrm{nm}$ where current saturation begins to set in.

Although our characterization indicates that the dc performance of the devices is homogeneously distributed over the $11 \times 5\,\mathrm{mm}^2$ sample, high-frequency response is rather poor which we attribute to the reduced quality of large-area CVD graphene. However, in a fully optimized GFET design with the channel length reduced to the gate length, a second gate could safely improve the device performance rather than halving the gate dielectric thickness with increased risk of leakage currents.

6 Conclusion and outlook

In this thesis we studied graphene field-effect transistors operating at microwave frequency using various device designs and substrate materials. In a first step, by using sapphire, a fully insulating substrate, we aim to reduce parasitic losses. When creating the layout of our GFET, we focused on increasing the intrinsic transit frequency by gate-length scaling, while maintaining power gain at frequencies $f_{\max} > 1\,\mathrm{GHz}$. We observe current gain up to frequencies of $f_{\mathrm{T,in}} = 80\,\mathrm{GHz}$, even without reaching current saturation. The transit frequency is only a factor of two smaller than that achieved in the best comparable devices with equivalent gate length. We also find considerable maximum transconductance of $g_{\mathrm{m}}^{\mathrm{RF}} \approx 250\,\mu\mathrm{S}/\mu\mathrm{m}$ in this device. Repeated measurements at liquid nitrogen temperature suggest that our GFET could be used in a cryogenic low noise amplifier. We show that the aluminum oxide dielectric conserves the device performance over long periods of time, however intrinsic charge traps cause a hysteresis and degrade the mobility of the graphene. Our findings represents the first-time characterization of graphene-on-sapphire FET at microwave frequency.[133]

In a subsequent study, we use atomically flat hexagonal boron nitride (hBN) as substrate for the graphene channel in our GFET. We aim to increase charge carrier mobility by decreasing substrate-induced scattering and corrugations. The hBN substrate also serves as dielectric for the pre-patterned bottom gate. A 40-GHz probe station was designed and set up at INT for in-house device characterization. Monolayer and bilayer graphene devices were fabricated and characterized. We observe less hysteresis compared to the graphene-on-sapphire devices, indicating smaller amounts of residual charge traps, due to the hBN substrate. Maximum intrinsic transit frequencies $f_{\mathrm{T}} = 61\,\mathrm{GHz}$ and $38\,\mathrm{GHz}$ were extract for the monolayer and bilayer device, respectively. These frequencies currently represent the record for monolayer and bilayer graphene-on-hBN FETs.[147] The monolayer device offers a maximum oscillation frequency $f_{\max} = 10.5\,\mathrm{GHz}$ at an increased $f_{\max}/f_{\mathrm{T}}$ ratio compared to our graphene-on-sapphire samples. However, the device performance could have been even higher if a wrinkle-free graphene transfer process was used.

In a novel approach, we realize few-layer graphene bottom-gated GFETs operating at GHz frequencies for the first time.[147] Transfer of hBN and graphene is established with a new corrugatation-reducing process. The devices have a comparable geometry as the metal bottom-gated GFET. Despite a tenfold decrease in gate thickness and a larger gate resistance, intrinsic transit frequencies of up to $f_{\mathrm{T}} = 30\,\mathrm{GHz}$ are reached. We derive the gate resistance values of our thin graphene gate devices from a simplified small-signal model. The large R_{g} is also responsible for a deviation of the current gain from the typical $1/f$ dependence, which can be described by our model. The extreme reduction in total device thickness combined with its transparency opens the possibility of new applications for our graphene-gated FET.

In an array of CVD-grown graphene FETs we systematically investigated the dependence of the transport characteristics on the gate length, keeping other device properties constant.

We find that current saturation can be achieved by operating the devices in the gate-voltage regime where bias-induced shifting of the Dirac point occurs. In devices with local double gates, current saturation is substantially enhanced. Also, the additional gate increases the transconductance more strongly than the total gate capacitance, enabling higher intrinsic transit frequencies $f_{\mathrm{T,in}}$ compared to single-gated devices. The diminished RF performance of these GFET is expected to rise by minimizing the ungated graphene region by decreasing the channel length, for instance by using a self aligning gate.[24]

Using fully insulating substrates like sapphire or hBN has become a trend for realizing high-RF-performance graphene field-effect transistors.[58,88] While excellent high-frequency performance and versatile applications of GFET were demonstrated,[21,22] further optimization is necessary to compete with the HEMT/GaAs technology, especially in terms power gain. Since the production of graphene FETs is CMOS compatible, facilitating implementation with Si technology, GFET could nevertheless be favored over changing to silicon-incompatible high electron mobility (HEMT) technology.[13] Besides complementing Si technology, the design of novel circuits making use of graphene's peculiar features like its ambipolarity and nonlinearity will become an interesting task. Simpler and more effective niche-products like, e.g., a mixer consisting of only one GFET[162] or modulators fully made of graphene[94] have already been demonstrated.

While FET made from exfoliated graphene can serve as proof-of-concept studies, for real-world applications mass-fabricated devices with identical performance are required. To achieve this goal, defect free, high quality large area graphene and a simple fabrication method with improved transfer is needed. Water- and polymer-free transfer is currently under investigation in our group. Transfer-free direct growth of graphene[158] and hBN[141,157] on substrate denotes another promising path which could enable ultrathin, flexible and transparent high-frequency electronics.

A Appendix

A.1 Fabrication techniques

In the following, a variety of techniques used for the fabrication of our samples is presented. Each technique represents one step of the fabrication recipes found in the next chapter.

Pre-patterning markers: We pre-pattern our substrates with a grid of unique markers using *electron beam lithography* (see fig. A.1(a)). These markers serve as reference points for subsequent lithography steps and for locating graphene/hBN flakes after deposition by mechanical exfoliation.

Substrate cleaning in RIE: The substrates are cleaned in an oxygen plasma for 2 min in an Oxford Instruments Plasmalab 80 Plus chamber with the following parameters: oxygen flow 20 sccm, pressure 100 mTorr, forward power 200 W. This procedure removes organic materials like resist residues or glue from the tape.

Mechanical exfoliation of natural graphite: Graphene is mechanically exfoliated from a graphite crystal with adhesive tape. We use very pure natural graphite crystals from India. The so called "scotch tape technique" is depicted in fig. A.1(b). The majority of flakes deposited on the substrate is comprised of multiple layers of graphene, only a tiny fraction is mono or bilayer graphene. We scan the substrate for graphene flakes using an optical microscope. Usually, less then 10 flakes of suitable size and shape are found per cm^2.

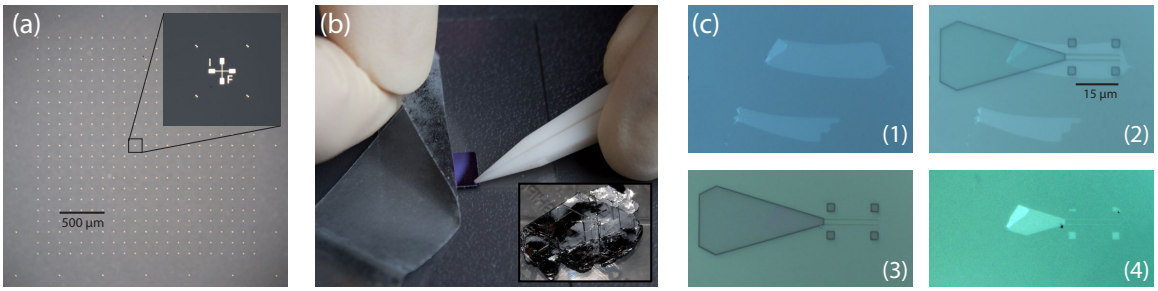

Figure A.1: (a) Sapphire substrate, pre-patterned with unique markers. (b) Graphene exfoliation by the "scotch-tape technique": flakes of graphite are deposited on an adhesive tape, which in turn is pressed onto the substrate. The inset shows a crystal of natural graphite. (c) Multilayer graphene (1) is etched by exposing it to a low power oxygen plasma. The desired parts of the graphene are covered by a negative resist mask (2). Picture (2) and (3) show the mask before and after etching, respectively. In (4), the etched structure is shown after removal of the resist.

Spin-coating of PMMA resist: Unless stated otherwise, substrates are spin-coated with PMMA (polymethyl methacrylate, molecular weight 950.000 solved at 4.5 wt% in anisol) at 6000 RPM for 90 s, resulting in an average thickness of 200 nm. For complete removal of the solvent and hardening of the resist, the samples are baked in a furnace at 165 °C for 30 min.

Development of PMMA resist: First, the conductive polymer is washed off by immersing the sample into distilled water. Then, the resist is developed in 1:3 MIBK:IPA for 15 s, rinsed with IPA and dried using a nitrogen gun. Development is repeated for another 5 s if found to be necessary after inspection with an optical microscope.

Spin-coating of ma-N2403 negative resist: The substrate is heated in a furnace at 200 °C for 20 min to treat the surface for improved adhesion of the negative resist. Immediately after removing the substrate from the furnace it is spin-coated with ma-N2403 at 3000 RPM for 30 s leading to a thickness of 300 nm. For complete removal of the solvent and hardening of the resist, the samples are baked in a furnace at 90 °C for 20 min.

Development of ma-N2403 resist: First, the conductive polymer is washed off by immersing the sample into a beaker filled with water. Then, the resist is developed in AZ 726 MIF developer for 20 s, rinsed with water and dried using a nitrogen gun. Development is repeated for another 5 s if found to be necessary after inspection with an optical microscope.

Spin-coating of Espacer conductive polymer: To avoid beam deflection caused by charge accumulation in the insulating substrate, a charge dissipation layer is needed. We use Espacer 300Z, a conductive polymer from Showa Denko K.K., which is spin-coat at a speed of 3000 RPM for 60 s with subsequent baking at 100 °C for 10 min resulting in a layer thickness of 20 nm.

Electron beam lithography (EBL): EBL is used to create a polymer mask e.g. for metal deposition or local etching. A focused electron beam is scanned over the sample surface to write the desired pattern into a charge sensitive resist layer. The high energy primary electrons of the beam scatter inelastically at the resist and the substrate, creating a cascade of secondary electrons. The low energy (< 50 eV) secondary electrons then are capable of breaking the molecule chains of the (positive) resist, thereby locally changing its solubility. When immersed into a developer, the exposed areas of the resist can be removed faster, leaving behind a mask consisting only of unexposed resist. When using a negative resist, exposing the resist to the electron beam leads to crosslinking and hinders solubility in the developer.

We use a Raith eLine EBL system (fig. A.3(a)) to write our patterns into the resist. It operates at a maximum acceleration voltage of 30 keV with a gun pressure of $6 \cdot 10^{-10}$ mbar and a chamber pressure of $< 2 \cdot 10^{-6}$ mbar. Its laser-interferometric stage offers an accuracy of 2 nm. Our patterns are divided into two parts: One small, inner part with a size of $100 \times 100\,\mu m^2$, containing the drain, source and gate electrodes for the active graphene device. This part requires high resolution, achieved by using the 20 µm aperture and a small step size of 8 nm. The second, outer part (usually

$400 \times 400\,\mu m^2$) comprises of the contacting pads for the high-frequency probes and the coplanar waveguide, which overlaps slightly with the inner part. This part is written using the broader 120 µm aperture and a step size of 69 nm, resulting in lower resolution but substantially faster writing speed. Alignment between inner and outer part is accomplished by using pre-patterned markers. We write all patterns at the maximum acceleration voltage of 30 keV to obtain highest resolution. At this voltage, best focus is achieved at a working distance of ≈ 12.6 mm.

During sample fabrication, several consecutive steps of EBL have to be performed, e.g. when patterning the gate electrode after dielectric deposition. In this case, very accurate realignment to the existing drain-source pattern is necessary. This is accomplished by scanning special realignment markers immediately before writing the actual pattern. These alignment markers were patterned at the same time as the existing pattern, therefore evaluating their coordinates can accurately predict the optimum writing position for the new pattern.

-*UHV metal evaporation:* For Ti/Al metal deposition we use the ultra high vacuum chamber of the Beckmann group (fig. A.2(a)). It consists of a main chamber and a prechamber and features six metal sources. Depending on the source, the metals are evaporated on the basis of molecular beam epitaxy (thermal evaporation) or electron beam heating of the source. The main chamber is evacuated by an ion (getter) pump reaching an ultra high vacuum of down to $\approx 4 \cdot 10^{-10}$ mbar. During metal evaporation, the pressure rises to values between 10^{-9} and 10^{-8} mbar. The prechamber is equipped with a turbomolecular pump (reaching $2 \cdot 10^{-7}$ mbar) and a load lock that allows for easy and fast sample transfer to the main chamber. Rotating and tilting the sample holder in arbitrary directions is possible, enabling angular metal evaporation. The samples can be cooled with liquid nitrogen to temperatures of approximately 190 K to 140 K to avoid the formation of metal-islands and to facilitate the creation of smooth, high quality metallic films.

For contacting graphene, out of the available six sources only titanium and aluminum are of interest. Initially, we grow a thin film of titanium which acts both as the contact material for the graphene and as adhesive layer for the subsequent aluminum deposition. When aluminum films are exposed to oxygen (e.g. in air), the outer layer (roughly 4 nm) oxidizes. If a second layer of metal is deposited onto an oxidized aluminum film, a tunnel junction is created increasing the contact resistance. For samples where multiple steps of metal evaporation are required (e.g. for the gate electrodes in our bottom-gated GFET) we revert to *HV metal evaporation* of non-oxidizing metals like Au.

HV metal evaporation: The metal evaporator of the Schimmel group at INT (fig. A.2(b)) is equipped with two separate evaporation units, each featuring five crucibles loaded with different metals. A high voltage (3 kV) electron beam is deflected onto the target crucible by a magnetic field, heating the source metal until it locally melts and evaporates. Out of the available metals, Au, Al, Ti, Cr, and Pd are relevant for our applications. Evaporation of other metals is possible, as exchanging the sources can be accomplished with relatively little effort. The main and prechamber both are evacuated

Figure A.2: (a) UHV metal evaporator (Beckmann group), (b) HV metal evaporator (Schimmel group).

by turbomolecular pumps reaching a base pressure of $1.2 \cdot 10^{-8}$. During evaporation, the pressure rises to values between $1.4 \cdot 10^{-7}$ mbar (Cr) and $8 \cdot 10^{-7}$ mbar (Au), depending on the metal and evaporation speed. The sample holder can not be cooled, but the evaporation rate is much higher than with the UHV metal evaporator.

Atomic layer deposition (ALD): Atomic layer deposition is a self limiting process, thus one has control over the exact number of layers deposited. The working principle is the sequential chemical reaction of two or more different chemicals (so called precursors) at the sample surface via chemical vapor deposition. In each injection cycle, only one additional atomic layer is grown. Excess reaction products and residual precursor molecules are removed from the chamber by purging with an inert gas (e.g. nitrogen) and pumping the chamber. In the case of Al_2O_3 growth, the two precursors required are trimethylaluminum (TMA) and water (H_2O). Methane (CH_4) is created in a reaction of the hydrogen atoms from the H_2O molecules with the $-CH_3$ groups of TMA. The $-CH_3$ groups then are replaced by the remaining oxygen atoms:

$$2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 6CH_4,$$

with a enthalpy of reaction $\Delta H = -376\,\text{kcal}$.
However, H_2O-precursor based growth of closed films via ALD is not possible directly on graphene.[124,125] Therefore, prior to the ALD procedure we deposit a thin film of aluminum by *UHV metal evaporation*, followed by oxidization in air.[127] We then use a Cambridge Nanotech Savannah ALD (fig. A.3(b)) for the Al_2O_3 growth. 91 cycles correspond to a film thickness of 10 nm. Due to amorphous growth, the dielectric constant is lower than in crystalline Al_2O_3. Values in the range of $\kappa = 5.9$ (12 nm) to $\kappa \approx 8$ (> 100 nm) are expected.[163] Optimum reaction speed is achieved at temperatures of approximately 250 °C where the delay between two cycles is set to 15 s. When local deposition is required, we use a low temperature process (90 °C) to protect the PMMA

mask. The reaction speed at such low temperatures is reduced, therefore we increase the cycle time to 1 min. Independent of the process temperature, pulse times of 20 ms (TMA) and 200 ms (H_2O) are used.

Lift-off: After metal evaporation or dielectric deposition via ALD, the resist mask and the unwanted material deposited atop has to be removed using a so called resist stripper. Typical resist strippers for PMMA are acetone, N-methyl-2-pyrrolidone (NMP) or dimethyl sulfoxide (DMSO). The negative resist ma-N is removed using AZ 100 remover. Usually, samples are left in a beaker with the remover for one to two hours. The resist strippers can be heated to ease the removal process.
Materials grown by ALD form a closed film covering also the resist sidewalls. Thus, the lift-off process often is impeded as the resist stripper cannot access the resist below the ALD-grown layer. In this case, ultra-sonication can be used for removal of the resist. However, ultra-sonication can not be reverted to in all cases, as it may destroy the graphene.

Graphene etching in RIE: We etch graphene using a soft oxygen plasma for 60 s with the following settings: oxygen flow 15 sccm, pressure 60 mTorr, forward power 30 W. This process suffices to etch several tens of layers of graphene, while leaving the protective PMMA mask (200 nm) intact. We use an Oxford Instruments Plasmalab 80 Plus reactive ion etching chamber.

Wet transfer technique: Transfer of graphene or hBN flakes from Si/SiO_2 substrate to arbitrary substrates. Since the flakes are exposed to water during transfer, the technique is called "wet" transfer. The procedure is explained in detail in chapter 4.1.1.

Dry transfer technique: For transfer of graphene or hBN flakes to a target substrate, they are deposited on a Si/SiO_2 substrate covered by a layer of PMMA. In this procedure exposition to water is avoided, thus it is called "dry" transfer. The technique is explained in detail in chapter 4.5.1.

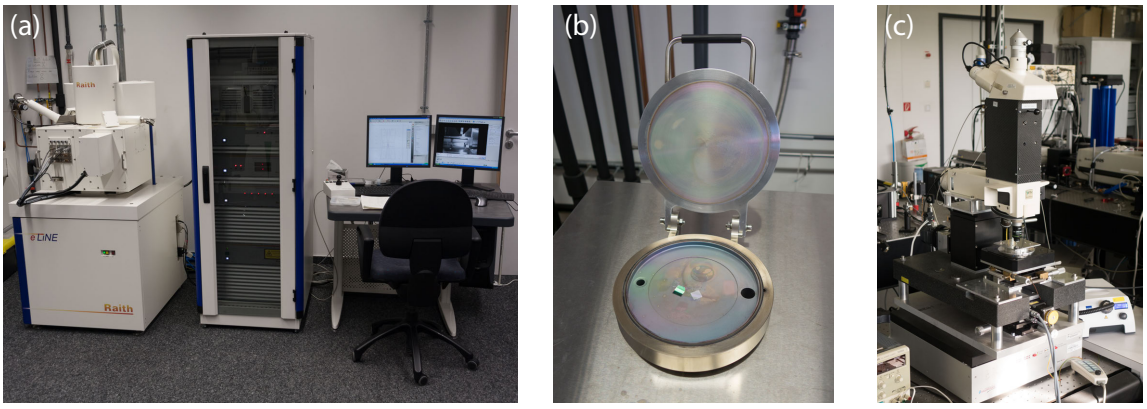

Figure A.3: (a) Raith "eLine" electron beam lithography system, (b) Cambridge Nanotech Savannah ALD, (c) WITec Raman spectrometer.

A.2 Raman spectroscopy

Raman spectroscopy is a non-destructive tool for quick and unambiguous distinction between mono, bi and multilayer graphene.[112,164,165,166] When shining light from a laser onto a target, most photons are scattered elastically (Rayleigh scattering). However, a small part is scattered inelastically, exciting virtual phonon states. The emitted photons resulting from the relaxation of these states can have either a lower energy (Stokes scattering) or higher energy (anti-Stokes scattering) than the incident photons. The difference in energy (wavelength shift) and the intensity of the photons are detected by a spectrometer.

In monolayer graphene, due to the missing bandgap, electronic states instead of virtual states are excited, largely enhancing Raman scattering. As the graphene unit cell is comprised of two carbon atoms, there are three acoustic and three optical phonon branches. These are categorized into **i**n or **o**ut-of plane, **L**ongitudinal/**T**ransverse **A**coustic/**O**ptic (short oTA, iTA, iLA, oTO, iTO, iLO). DFT calculations of these six phonon bands are shown in fig. A.4(b). The Raman spectrum of graphene exhibits several characteristic peaks. The three most prominent features, the G, D and 2D peaks and their corresponding bands are described below. A sketch of the associated scattering processes is depicted in fig. A.4(a). The G or graphite peak located at $\sim 1580\,\mathrm{cm}^{-1}$ corresponds to the double degeneracy of the iTO and iLO phonon modes at the Γ point (red circle in fig. A.4(b)). It is the only normal, first order resonant Raman scattering process in graphene.[165] In the vicinity of the K point the iLA and iLO phonon branches cross, creating another doubly degenerate phonon (blue/green semi-circle in fig. A.4(b)). This gives rise to two second-order processes responsible for the D and 2D band. Their location is dependent on the energy of the incident light. In the following, approximate wavenumbers are given for an incident wavelength of 633 nm. For

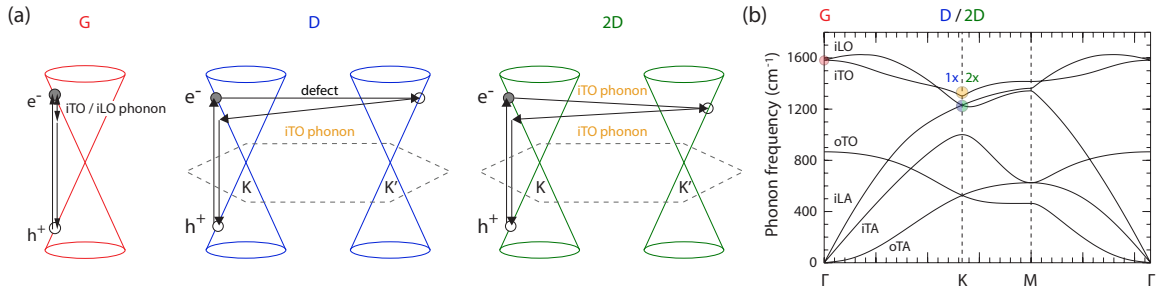

Figure A.4: (a) Processes responsible for the G, D and 2D bands in the Raman spectrum of graphene. In all processes, an incident photon creates an electron/hole pair. G peak: The electron (or hole) excites either an iTO or iLO phonon (red circle in (b)) and recombines. 2D peak: The electron (or hole) excites an iTO phonon (orange circle in (b)) and is scattered inelastically to a state in the opposite valley. Simultaneously, in a second process involving an iTO phonon, an electron is scattered back to the initial valley and recombines. The D peak process is similar to the 2D process, however here one of the two inelastic iTO phonon scattering processes is substituted by an elastic scattering by a defect. (b) DFT calculation of graphene's phonon dispersion. The double degenerate modes responsible for the processes in (a) are highlighted by a red circle and blue/green semicircles. *Source: (a) after[165] (b) adapted from[167], complemented.*

the D or "defect peak", a second order intra-valley double-resonant process is caused by a phonon from the iTO branch and a defect. The intensity of the D peak thus is a measure of the crystal quality of graphene. It is located approximately at $1350\,\mathrm{cm}^{-1}$. For the 2D peak (sometimes also referred to as G' or D* peak) two iTO phonons are excited simultaneously in an intervalley double-resonant process. As two phonons are involved, the energy of the 2D band is approximately twice the energy of the D band ($\sim 2700\,\mathrm{cm}^{-1}$). In monolayer graphene, two out of three theoretically possible processes are suppressed ($q < K$ and $q \approx K$), leaving only one possible process ($q > K$). Thus the 2D peak of monolayer graphene possesses a lorentzian shape as depicted in fig. A.5. In bilayer graphene, four processes are allowed resulting in a broader 2D peak with a distinctive kink. With increasing number of layers, two of these contributions decline and the kink vanishes. Therefore, by examination of the 2D peak alone, a clear distinction between mono, bi and multilayer graphene is possible in most of the cases.

We use a customized Raman setup from WITec (fig. A.3(c)), where the spectrometer is integrated with a confocal optical microscope. A laser with a wavelength of 633 nm is focused on the graphene, allowing local measurements of areas below $1\,\mu\mathrm{m}^2$. The emitted power is limited to 1 mW to not overheat or damage the graphene. We supress Rayleigh scattering using a notch filter. Spectra are recorded by a 1024 channel CCD which is cooled to $-60\,^{\circ}\mathrm{C}$ to reduce noise. An integration time of 60 s delivers satisfactory intensities for the G and 2D peak. Fig. A.5 shows typical Raman spectra of mono-, bi- and multilayer graphene. Additional spectra of some of the remaining samples presented in this thesis can be found in chapter A.4.

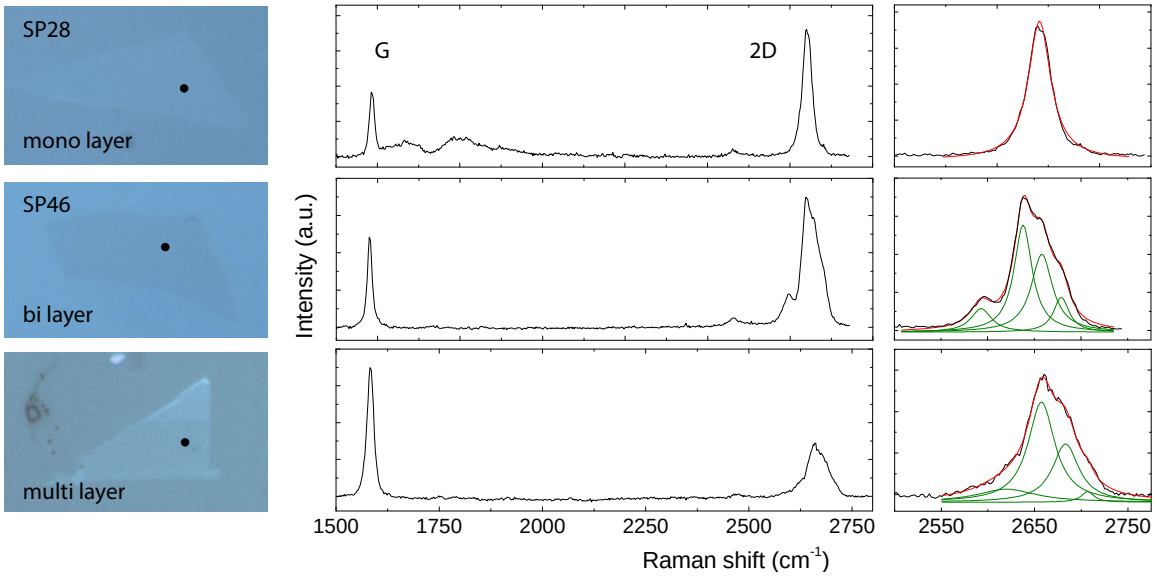

Figure A.5: Raman spectra of monolayer (sample SP28), bilayer (SP46) and multilayer graphene deposited on sapphire substrate. The corresponding flakes are depicted on the left. The position of the laser during measurement is indicated by a black spot. On the right, a zoom-in to the 2D peak is shown for better visualization of the Lorentz fits. For monolayer graphene, the 2D peak has a lorentzian shape and is much more intense than the G peak due to enhanced Raman scattering. The 2D peak in bilayer graphene can be fitted with 4 individual Lorentzian functions. Its hallmark is a pronounced kink. In multilayer graphene, 2 of the 4 contributions to the 2D peak decline and its intensity decreases compared to the G peak.

A.3 Fabrication recipes

The following recipes describe the fabrication steps for all samples discussed in this thesis. Individual steps spelled in *italic letters* are described in detail in the previous chapter. In all cases, 330 µm thick C-plane (0001) sapphire wafer from Roditi Ltd[116] was used.

A.3.1 Graphene FET on sapphire substrate

1. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
2. *Pre-patterning markers*
3. *substrate cleaning in RIE*
4. Mono- or bilayer graphene is deposited via *mechanical exfoliation of natural graphite.*
5. Verification by *Raman spectroscopy*
6. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
7. Patterning of the drain and source electrodes and the CPW contacting structure using *electron beam lithography.*
8. *Development of PMMA resist*
9. *UHV metal evaporation* Ti (10 nm) + Al (100 nm)

10. *Lift-off* in acetone
11. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
12. The area for the gate dielectric deposition is defined using *electron beam lithography.*
13. *Development of PMMA resist*
14. *UHV metal evaporation* of Al (2 nm), followed by natural oxidization.
15. Dielectric growth of Al_2O_3 (usually 10 nm) via *atomic layer deposition (ALD)*
16. *Lift-off* in acetone
17. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
18. The top gate electrode is defined by *electron beam lithography.*
19. *Development of PMMA resist*
20. *UHV metal evaporation* Ti (10 nm) + Al (100 nm)
21. *Lift-off* in acetone

A.3.2 Graphene FET on hBN substrate with metal bottom gate

1. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
2. *Pre-patterning markers*
3. *substrate cleaning in RIE*
4. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
5. The bottom gate electrode is defined by *electron beam lithography.*
6. *Development of PMMA resist*
7. *HV metal evaporation* Ti (1 nm) + Au (30 nm)
8. *Lift-off* in acetone
9. Hexagonal boron nitride is deposited via mechanical exfoliation on a Si/SiO_2 substrate.
10. The hBN flake is transferred on top of the bottom gate with the *wet transfer technique.*
11. Mono- or bilayer graphene is deposited via *mechanical exfoliation of natural graphite* on a Si/SiO_2 substrate.
12. Verification by *Raman spectroscopy*
13. The graphene flake is transferred on top of the hBN flake with the *wet transfer technique.*
14. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
15. The drain, source and gate electrodes and the CPW contacting structure is established using *electron beam lithography.*
16. *Development of PMMA resist*
17. *UHV metal evaporation* Ti (10 nm) + Al (100 nm)
18. *Lift-off* in acetone

A.3.3 Graphene FET on hBN substrate with graphene bottom gate

1. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
2. *Pre-patterning markers*
3. *substrate cleaning in RIE*
4. (Multilayer) graphene is deposited via *mechanical exfoliation of natural graphite.*
5. *spin-coating of ma-N2403 negative resist* and *spin-coating of Espacer conductive polymer*
6. An etch mask for the graphene bottom gate is defined using *electron beam lithography.*
7. *Development of ma-N2403 resist*
8. *Graphene etching in RIE*
9. ma-N2403 negative resist is removed with AZ 100 remover.
10. The sample is cleaned in a vacuum furnace at 250 °C.
11. Hexagonal boron nitride is deposited via mechanical exfoliation on a Si/SiO_2 substrate covered with PMMA.
12. A thin ($< 10\,nm$) hBN flake is transferred on top of the graphene bottom gate with the *dry transfer technique.*
13. Mono- or bilayer graphene is deposited via *mechanical exfoliation of natural graphite* on a Si/SiO_2 substrate covered with PMMA.
14. Verification by *Raman spectroscopy*
15. The graphene flake is transferred on top of the hBN flake with the *dry transfer technique.*
16. The sample is cleaned in a furnace at 300 °C at air.
17. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
18. The drain, source and gate electrodes and the CPW contacting structure is established using *electron beam lithography.*
19. *Development of PMMA resist*
20. *UHV metal evaporation* Ti (10 nm) + Al (100 nm)
21. *Lift-off* in acetone

A.3.4 CVD graphene FETs with doubly clamped contacts and double gates

1. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
2. *Pre-patterning markers*
3. *substrate cleaning in RIE*
4. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
5. The bottom gate electrodes are defined by *electron beam lithography.*
6. *Development of PMMA resist*
7. *HV metal evaporation* Ti (5 nm) + Au (25 nm)
8. *Lift-off* in acetone
9. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*

10. The area for the bottom gate dielectric deposition is defined using *electron beam lithography.*
11. *Development of PMMA resist*
12. Dielectric growth of Al_2O_3 (72 cycles, 8 nm) via *atomic layer deposition (ALD)*
13. *Lift-off* in DMSO at 80 °C
14. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
15. The bottom drain and source electrodes and the CPW contacting structures are established using *electron beam lithography.*
16. *Development of PMMA resist*
17. *HV metal evaporation* Ti (5 nm) + Au (25 nm)
18. *Lift-off* in acetone
19. CVD graphene is transferred on top of the bottom contacts with the *wet transfer technique.*
20. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
21. An etch mask for the graphene channel is defined using *electron beam lithography.*
22. *Development of PMMA resist*
23. *Graphene etching in RIE*
24. Removal of PMMA mask in acetone
25. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
26. The top drain and source electrodes and the CPW contacting structures are established using *electron beam lithography.*
27. *Development of PMMA resist*
28. *HV metal evaporation* Ti (5 nm) + Au (40 nm)
29. *Lift-off* in acetone
30. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
31. The area for the top gate dielectric deposition is defined using *electron beam lithography.*
32. *Development of PMMA resist*
33. *UHV metal evaporation* of Al (2 nm), followed by natural oxidization.
34. Dielectric growth of Al_2O_3 (54 cycles, 6 nm) via *atomic layer deposition (ALD)*
35. *Lift-off* in DMSO at 80 °C
36. *Spin-coating of PMMA resist* and *spin-coating of Espacer conductive polymer*
37. The top gate electrodes are defined by *electron beam lithography.*
38. *Development of PMMA resist*
39. *HV metal evaporation* Ti (5 nm) + Au (40 nm)
40. *Lift-off* in acetone

A.4 Raman spectra of selected samples

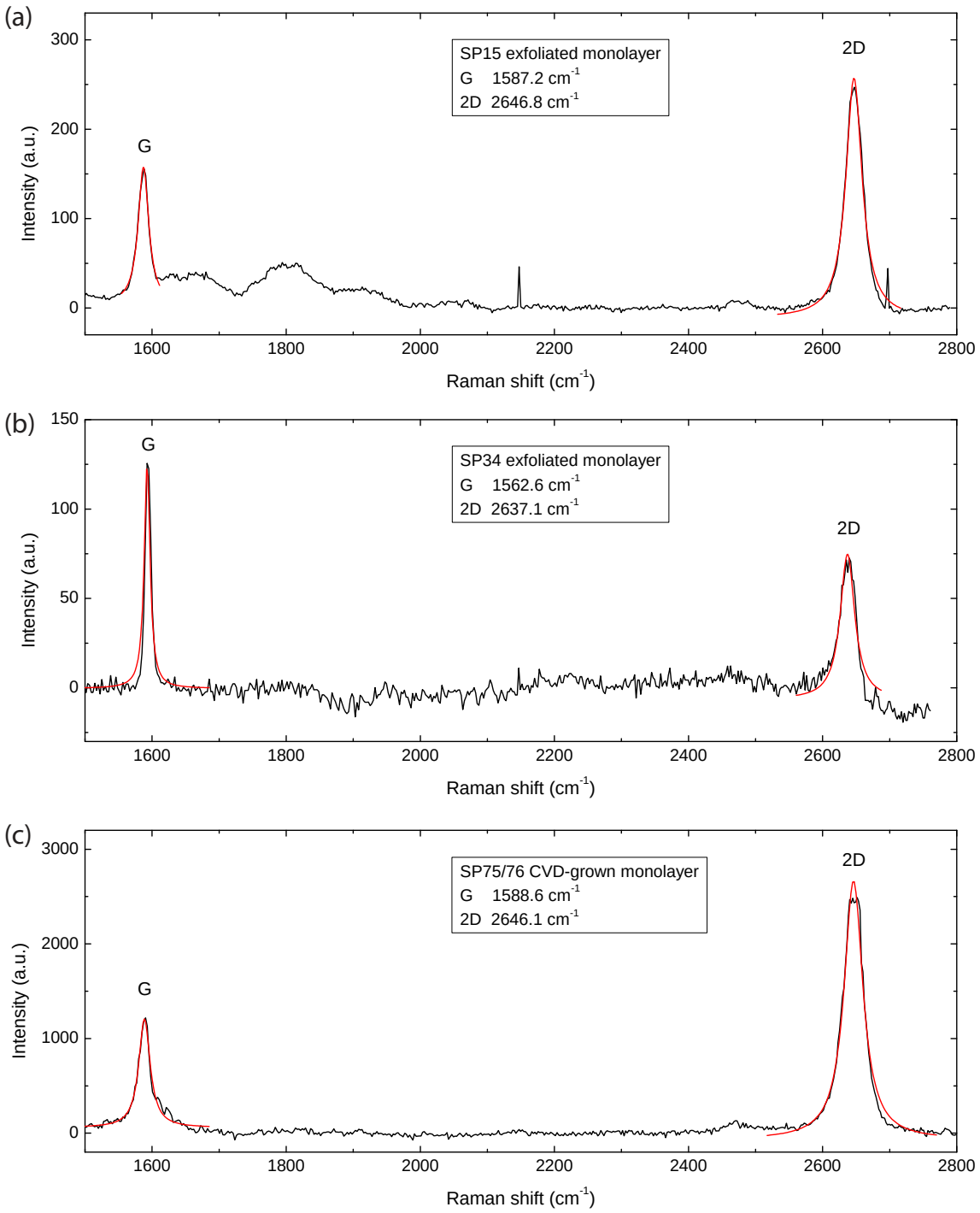

Figure A.6: Raman spectra of sample (a) SP15, (b) SP34, and (c) SP75/76.

A.5 Measurement setups

A.5.1 Setup at ENS, Paris

Our first samples up to sample no. SP19 were measured in collaboration with ENS, Paris. Their setup consists of a Cascade Microtech Summit 9000 probe station with Infinity Probes attached to an Anritsu 37369C vector network analyzer. It is capable of measuring the S parameters up to a frequency of 20 GHz. SOLT calibration is performed using a calibration substrate. The full setup is shown in fig. A.7. By using bias-tees we superimpose dc bias voltages supplied by voltage sources (Yokogawa 7651) onto the RF signal generated by the VNA. For each of the two ports (gate and drain) a bias resistor is placed in series as a protective current limiter and as means to calculate the current flowing through the graphene. The drain-source current is derived by measuring the voltage drop across the bias resistor with a voltage meter (Keithley 2000). A schematic of the setup is given in fig. A.8. When sweeping the gate voltage, only the total voltage applied to the series of bias resistor and graphene channel is kept constant. As the conductivity of the graphene changes depending on the gate voltage, the effective drain voltage applied to the graphene changes during gate voltage sweeps. This marks a limitation of the setup.

A.5.2 Setup at KIT

A setup similar to the one at ENS was built at KIT. It is based on the same measurement principle (fig. A.8), but is comprised of more recent hardware. We use a Rhode & Schwarz ZVA40 vector network analyzer with |Z|PROBE probes attached to PH110HF probe heads. The setup is shown in fig. A.9. For superposition of ac and dc signals, we employ BTN-0040 ultra-broadband bias tees from Marki Microwave. All components are specified for operation at frequencies of up to 40 GHz. Gate-source and drain-source voltages are applied by a Yokogawa 7651 programmable dc voltage source and a Stanford Research SR844. DC measurements are performed with Agilent 34410 6½ digit voltmeters. We designed a custom probe station, built specifically to meet our requirements. The probe heads can be moved

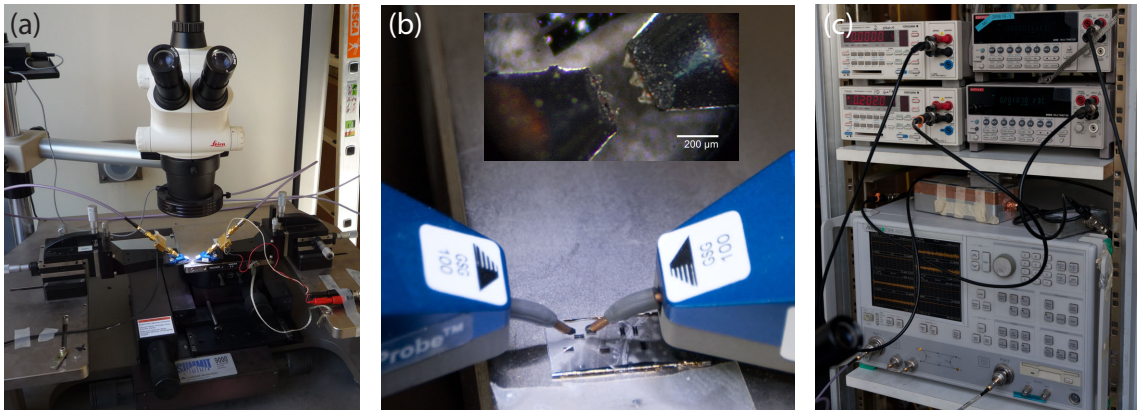

Figure A.7: High-frequency probe station and measurement setup at ENS, Paris.

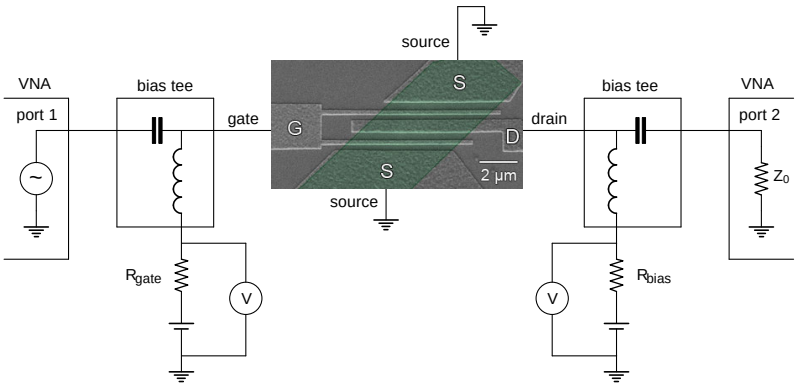

Figure A.8: Schematic of the measurement setup used at ENS and KIT. The VNA applies sinusoidal high-frequency signals to gate and drain electrode, while the dc bias point is set by voltage sources. Superposition of ac and dc signals is accomplished with bias tees. We measure the dc voltages V_{gs} and V_{ds} with voltage meters.

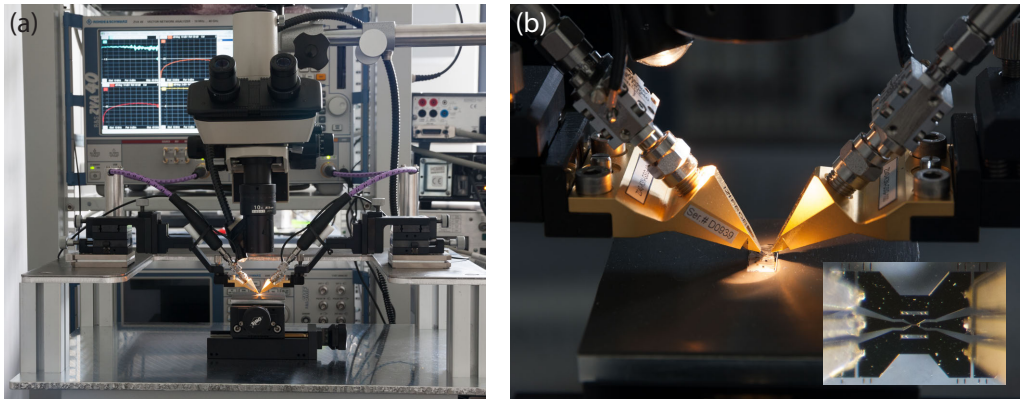

Figure A.9: Custom made probe station with RF probes attached to the VNA, visible in the background. The whole setup is placed on an anti-vibrational table keeping the probes steady. The sample can be moved $\pm 25\,\mathrm{mm}$ in x- and y-direction and each probe has a travel range of $\pm 5\,\mathrm{mm}$ in x,y, and z.

freely on the U-shaped table. For dampening, the setup resides on an active anti-vibrational table.

A.5.3 Improved setup at KIT with automatically readjusting bias voltage

Both previously described setups lack the possibility to keep the drain-source voltage applied to the graphene at a constant value while sweeping the gate voltage. To overcome this limitation, we redesigned the setup. Instead of an external bias resistor, we use the internal shunt resistor of our new voltmeter (Keithley 2010) to directly measure the current. A schematic of the adjusted setup is shown in fig. A.10. We removed the protective resistor in series with the gate, as it did not prove necessary. Using the sense-inputs of the new voltage

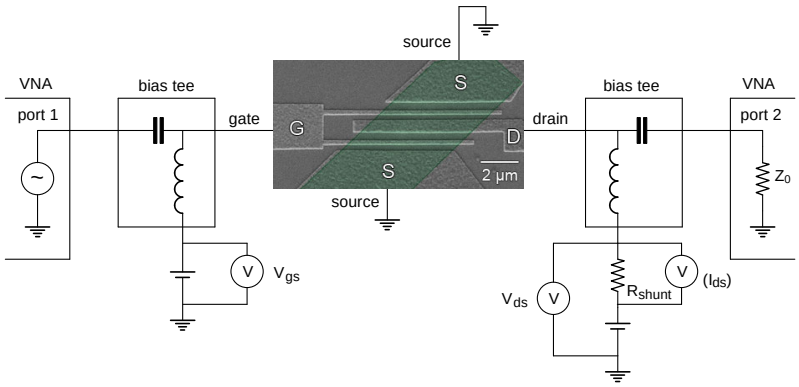

Figure A.10: Schematic of the new, automatically voltage readjusting measurement setup. Direct current measurement is possible via the built-in shunt resistance of the new voltmeter.

sources (Yokogawa GS200), the output voltages are corrected for resistive losses in the cables and the voltage drop across the shunt resistor. This ensures the voltages applied to gate and drain electrode comply with the voltages set by our measurement program. Additionally, our measurement program monitors and adjusts the voltage compliance. Each time the program changes one of the bias voltages, we use the voltmeter to sequentially measure V_{gs}, V_{ds} and I_{ds}. If the measured gate-source or drain-source voltage deviate from the specified value more than a certain threshold (usually 0.5 %), the program automatically adjusts the corresponding voltage source accordingly in a loop until the deviation falls below the threshold.

A.6 Scattering/admittance/impedance parameters

For the description of the electrical characteristics and small-signal response of linear electrical components and networks, a variety of similar parameters is used. For this work, out of these the scattering (S), admittance (Y), and impedance (Z) parameters are of particular importance. Each of those parameters is obtained under different conditions: matched-load termination (S parameters), short-circuit condition (Y parameters), and open-circuit condition (Z parameters). Lossless conversion between the different representations is possible through mathematical transformations. For simplicity, only linear two-port networks are described in this brief overview following [131].

In the scattering parameter representation, the conditions at each port are described by an incident (a) and a reflected (b) power wave, rather than by a voltage and a current. A schematic is depicted in fig. A.11. The corresponding scattering parameter matrix is given by

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} \mathrm{S}_{11} & \mathrm{S}_{12} \\ \mathrm{S}_{21} & \mathrm{S}_{22} \end{pmatrix} \cdot \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}. \tag{A.1}$$

Scattering parameters are measured using matched loads: while sending a stimulus through port 1, port 2 is terminated in the system load Z_0 (usually $Z_0 = 50\,\Omega$). An incident wave

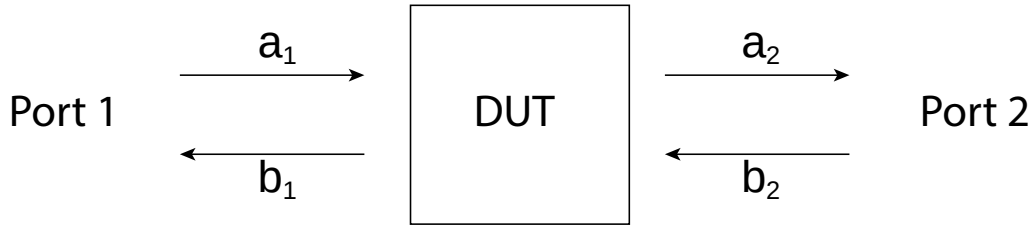

Figure A.11: Schematic of the scattering parameters of a linear two-port network, here represented as device under test (DUT). a_1,a_2 are the incident and b_1,b_2 the reflected waves from port 1 or 2, respectively.

from port 1 (a_1) is either reflected back into port 1 (b_1) or scattered by the device under test (DUT) and transmitted into port 2 (b_2). As port 2 is currently terminated in a matched load, back-reflection (b_2) from port 2 is absorbed completely leading to $a_2 = 0$. Considering $a_2 = 0$, an expansion of eq. A.1 delivers the corresponding S-parameters S_{11}, S_{21} as follows:

$$b_1 = S_{11}a_1 + S_{12}\underbrace{a_2}_{=0} \quad \Rightarrow \quad S_{11} = \frac{b_1}{a_1}$$

$$b_2 = S_{21}a_1 + S_{22}\underbrace{a_2}_{=0} \quad \Rightarrow \quad S_{21} = \frac{b_2}{a_1}.$$

Similarly, the S parameters for measurement of port 2 are obtained (port 1 terminated in Z_0, $a_1 = 0$)

$$S_{12} = \frac{b_1}{a_2} \qquad S_{22} = \frac{b_2}{a_2}.$$

It follows that each individual S parameter can be expressed as the ratio of the corresponding reflected to incident wave

$$S_{nm} = \frac{b_n}{a_m}.$$

The diagonal elements of the scattering matrix associated to only one port are called reflection coefficients

- S_{11}: input voltage reflection coefficient
- S_{22}: output voltage reflection coefficient

whereas the off-diagonal elements are referred to as transmission coefficients

- S_{12}: reverse voltage gain
- S_{21}: forward voltage gain.

Due to the matched load termination, S parameters can be measured conveniently with a vector network analyzer, even at very high frequencies. However, multiple relevant figures of merit can be obtained more simplistic in the admittance parameter representation. For instance, the small-signal current gain is defined as

$$|h_{21}| = \left|\frac{\mathrm{Y}_{21}}{\mathrm{Y}_{11}}\right|. \tag{A.2}$$

Also, conversion to admittance and impedance parameters is necessary when performing de-embedding (refer to the next sub-chapter). Transformation of the scattering parameters to the admittance representation is possible using the following equations

$$\begin{aligned}
\mathrm{Y}_{11} &= \frac{1}{Z_0}\frac{(1-\mathrm{S}_{11})(1+\mathrm{S}_{22})+\mathrm{S}_{12}\mathrm{S}_{21}}{\Delta_S} \\
\mathrm{Y}_{12} &= \frac{1}{Z_0}\frac{-2\mathrm{S}_{12}}{\Delta_S} \\
\mathrm{Y}_{21} &= \frac{1}{Z_0}\frac{-2\mathrm{S}_{21}}{\Delta_S} \\
\mathrm{Y}_{22} &= \frac{1}{Z_0}\frac{(1+\mathrm{S}_{11})(1-\mathrm{S}_{22})+\mathrm{S}_{12}\mathrm{S}_{21}}{\Delta_S},
\end{aligned}$$

where $\Delta_S = (1+\mathrm{S}_{11})(1+\mathrm{S}_{22}) - \mathrm{S}_{12}\mathrm{S}_{21}$. Conversion from admittance to impedance parameters can be accomplished by

$$\begin{aligned}
\mathrm{Y}_{11} &= \frac{\mathrm{Z}_{22}}{\Delta_Z} \\
\mathrm{Y}_{12} &= \frac{-\mathrm{Z}_{12}}{\Delta_Z} \\
\mathrm{Y}_{21} &= \frac{-\mathrm{Z}_{21}}{\Delta_Z} \\
\mathrm{Y}_{22} &= \frac{\mathrm{Z}_{11}}{\Delta_Z},
\end{aligned}$$

where $\Delta_Z = \mathrm{Z}_{11}\mathrm{Z}_{22} - \mathrm{Z}_{12}\mathrm{Z}_{21}$. As $Y = Z^{-1}$ and $Z = Y^{-1}$, back-conversion can be performed similarly.

A.7 De-embedding and extraction of device parameters

To be able to measure and characterize the intrinsic properties of our graphene transistors, two correction procedures have to be applied to the VNA, correcting for external parasitic effects originating from the cables, probes and interconnect pattern. The first procedure is the calibration of the VNA which shifts the reference plane to the tips of the probes. However, RF measurements after proper calibration still include parasitic effects of the contacting pads and on-chip coplanar waveguide lines connecting the probes with the sample. To correct for

and extract these parasitic effects, it is common practice to use a so called de-embedding procedure. Historically, the actual transistor was measured at zero bias voltage for extraction of the series parasitic elements.[153] A more robust but still simple procedure consists of measuring an *open*-structure (see fig. A.12) which consists of the same contact pads and interconnection lines as the device under test (DUT).[168] In the admittance representation the Y-parameters of the intrinsic transistor can then be found by simple subtraction:

$$\mathrm{Y}_{\mathrm{transistor-simple}} = \mathrm{Y}_{\mathrm{DUT}} - \mathrm{Y}_{\mathrm{open}} \tag{A.3}$$

This procedure removes the parallel parasitic capacitances which represent the largest contribution, while neglecting series parasitics. Since f_{T} is independent of series parasitics, this de-embedding procedure is sufficient for basic device characterization.

Further refinement of the correction can be achieved by measurement of an additional *short*-structure, in which the active device is replaced by metal, connecting the gate, drain and source electrodes. This second pattern accounts for losses and phase rotation in the contacting structure. The first step of this "two-step" de-embedding procedure consists of the correction of the *short* Y-parameters for parallel parasitics gained from the *open* pattern

$$\mathrm{Y}_{\mathrm{series\,parastics}} = \mathrm{Y}_{\mathrm{short}} - \mathrm{Y}_{\mathrm{open}}. \tag{A.4}$$

As a result we obtain *short* Y-parameters $\mathrm{Y}_{\mathrm{series\,parastics}}$ that contain only series parasitics, assuming all parallel parasitics are located in the contacting pads. This assumption is justified, as the parallel parasitics of the DUT is substantially smaller compared to the *open* structure

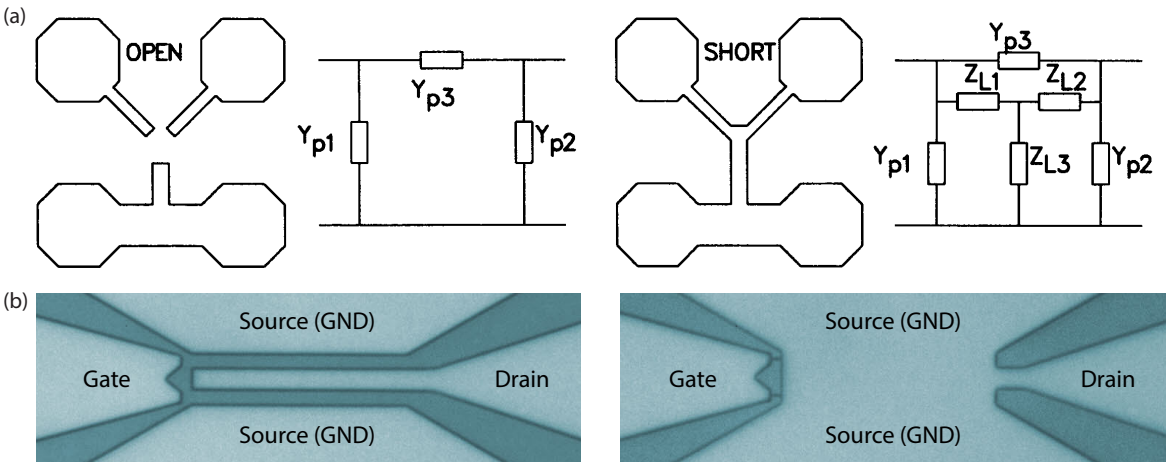

Figure A.12: (a) Generalized *open* and *short* patterns and their corresponding equivalent circuits. The *open* pattern accommodates only parallel parasitics, whereas the *short* structure additionally contains a T-network of series impedances. (b) Corresponding *open* and *short* de-embedding structures of our GFET (here SP75/76). The *open* structures are fabricated without gate fingers, as these are part of the active device. In the *short* structures, gate, drain and source are connected. *Source: (a) adapted from*[168]

for calibration. In the second step, these are subtracted from the corrected admittance parameters of the DUT (eq. A.3) leading to the intrinsic transistor Y-parameters

$$\begin{aligned} \mathrm{Y}^{-1}_{\mathrm{transistor}} &= \mathrm{Y}^{-1}_{\mathrm{transistor-simple}} - \mathrm{Y}^{-1}_{\mathrm{series\,parastics}} \\ \mathrm{Y}_{\mathrm{transistor}} &= \left((\mathrm{Y}_{\mathrm{DUT}} - \mathrm{Y}_{\mathrm{open}})^{-1} - (\mathrm{Y}_{\mathrm{short}} - \mathrm{Y}_{\mathrm{open}})^{-1} \right)^{-1}. \end{aligned} \tag{A.5}$$

For frequencies above a few GHz, differences between the two de-embedding procedures become prominent. The simple one-step *open* correction (eq. A.3) results in discrepancies of admittance values especially for Y_{11} and Y_{21} leading to potential underestimation of device performance. More advanced, three-step procedures on the other hand have only little further impact on the outcome of the corrected admittance parameters. [168,169]

To improve de-embedding results, we took great care in placing the *open* and *short* patterns on the same chip close to the actual transistor and producing them in the same fabrication steps.

For extraction of FET parameters we use the small signal model depicted in fig. A.13. It consists of two parts: the inner, intrinsic device containing the bias dependent elements $g_{\mathrm{m}}, g_{\mathrm{ds}}, \mathrm{C_{gs}}, \mathrm{C_{gd}}, \mathrm{C_{ds}}, \mathrm{R_i}$ and τ and the outer, bias independent elements $\mathrm{L_g}, \mathrm{L_s}, \mathrm{L_d}, \mathrm{R_g}, \mathrm{R_s}, \mathrm{R_d}, \mathrm{C_{pg}}$ and $\mathrm{C_{pd}}$. [153] All of these parameters can be obtained from the measured S parameters and (after lossless conversion) their Y and Z parameter representation. Fig. A.14 shows a visual representation of this extraction/de-embedding process from eq. A.5. After measurement of the extrinsic device as well as the *open* and *short* patterns, the corresponding S parameters are converted to Z parameters (fig. A.14a). The series gate and drain inductances $\mathrm{L_g}$,$\mathrm{L_d}$ can then be subtracted (fig. A.14b), followed by a conversion to Y parameters. Now the parallel

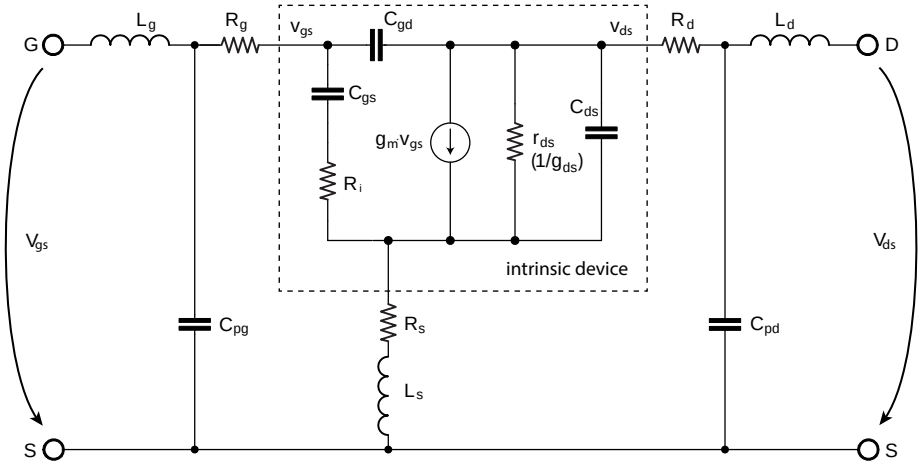

Figure A.13: Complete version of the small-signal equivalent circuit discussed in chapter 2.1 (fig. 2.2). The series inductances L_{d}, L_{s} and pad capacitances C_{pg}, C_{pd} account for the wave impedance in the contacting region and transmission line leading to the intrinsic device. [170] All extrinsic and intrinsic parameters R,C,L as well as g_{m} and g_{ds} can be extracted from S/Y/Z parameters obtained by measuring the actual transistor and de-embedding patterns. The model is valid for frequencies of up to 25 GHz. *Source: after* [153].

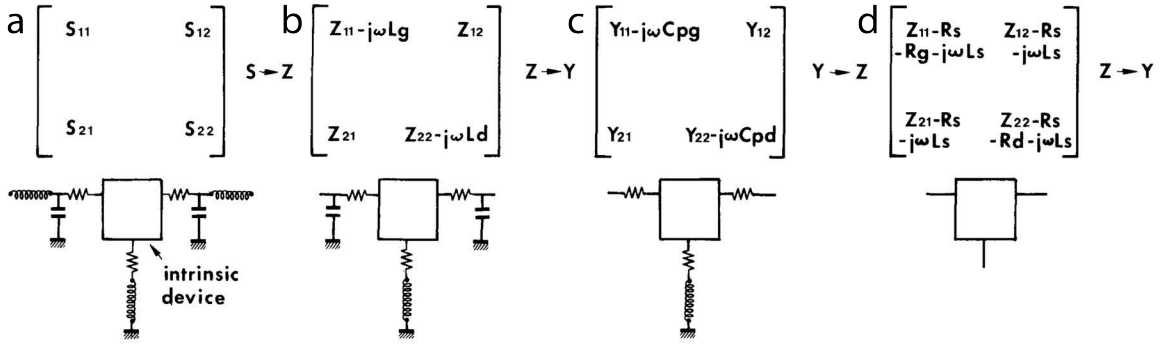

Figure A.14: Intrinsic and extrinsic device properties can be extracted from the measured S parameters by conversion to impedance (Z) and admittance (Y) representation. *Source: adapted from*[153].

gate and drain pad capacitances $\mathrm{C_{pg}}$,$\mathrm{C_{pd}}$ are retrieved from the *open* pattern (fig. A.14c) using

$$\begin{aligned} \mathrm{Im}\left(\mathrm{Y_{11}}\right) &= \omega \mathrm{C_{pg}} \\ \mathrm{Im}\left(\mathrm{Y_{22}}\right) &= \omega \mathrm{C_{pd}} \end{aligned}$$

followed by another transformation back to Z parameters. This enables us to subtract all series resistances $\mathrm{R_g}$,$\mathrm{R_s}$,$\mathrm{R_d}$ as well as the source inductance $\mathrm{L_s}$ from the *short* pattern (fig. A.14d) using the relations

$$\begin{aligned} \mathrm{Z_{11}} &= \mathrm{R_s} + \mathrm{R_g} + j\omega\left(\mathrm{L_s} + \mathrm{L_g}\right) \\ \mathrm{Z_{12}} &= \mathrm{R_s} + j\omega \mathrm{L_s} \\ \mathrm{Z_{22}} &= \mathrm{R_s} + \mathrm{R_d} + j\omega\left(\mathrm{L_s} + \mathrm{L_d}\right). \end{aligned}$$

Lastly we transform the resulting Z-matrix back into Y parameter representation which yields the final matrix of the intrinsic device. The elements of this matrix are

$$\begin{aligned} \mathrm{Y_{11}} &= \frac{\mathrm{R_i C_{gs}^2}\omega^2}{D^2} + j\omega\left(\frac{\mathrm{C_{gs}}}{D^2} + \mathrm{C_{gd}}\right) \approx \mathrm{R_i C_{gs}^2}\omega^2 + j\omega\left(\mathrm{C_{gs}} + \mathrm{C_{gd}}\right) \\ \mathrm{Y_{12}} &= -j\omega \mathrm{C_{gd}} \\ \mathrm{Y_{21}} &= \frac{g_\mathrm{m} e^{-j\omega\tau}}{D} - j\omega \mathrm{C_{gd}} \approx g_\mathrm{m} - j\omega\left(\mathrm{C_{gd}} + g_\mathrm{m}\left(\mathrm{R_i C_{gs}} + \tau\right)\right) \\ \mathrm{Y_{22}} &= g_\mathrm{ds} - j\omega\left(\mathrm{C_{ds}} + \mathrm{C_{gd}}\right) \end{aligned} \tag{A.6}$$

where $D = 1 + j\omega \mathrm{C_{gs}R_i}$. Since $\omega \mathrm{C_{gs}R_i} \ll 1$, $D \to 1$ and $\omega\tau \ll 1$ are common approximations (see $\mathrm{Y_{11}}$ and $\mathrm{Y_{21}}$ in eq. A.6). Now that all bias independent extrinsic elements are known, starting with $\mathrm{C_{gd}}$ from $\mathrm{Y_{12}}$ the remaining intrinsic elements $g_\mathrm{m}, g_\mathrm{ds}, \mathrm{C_{gs}}, \mathrm{C_{ds}}, \mathrm{R_i}$ and τ can be determined from the Y-matrix.

Acknowledgements

I would like to thank everybody who supported me during my time at the INT.

I am very grateful to Prof. Dr. Hilbert von Löhneysen for enabling me to pursue a Ph.D., and for his continuous support. I also would like to thank Prof. Dr. Georg Weiß for taking the position of secondary referee and Prof. Dr. Guido Drexlin for supervising this work as a mentor.

This work would not have been possible without the guidance and resourcefulness of my thesis advisor Dr. Romain Danneau. Thanks for the enduring encouragement during the past 4 years.

I really enjoyed working in our group and want to thank all my colleages for their help and support: Geethu Balachandran, Zeineb Ben Aziza, Muraleetharan Boopathi, Dr. Julien Bordaz, Renjun Du, Marco Giambra, Saumya Gupta, Kristina Hönes, Simon Ketterer, Jens Mohrmann, Himadri Pandey, Chirojyoti Rava, Dr. Pablo Robert, Joachim Schönle, Maximilian Thürmer, Julian Winter, Dr. Fan Wu and Philipp Zukowsky. Special thanks to Jens Mohrmann, Maximilian Thürmer, and Dr. Fan Wu for proofreading parts of this thesis.

Without Dr. Emiliano Pallecchi, initial measurements and data treatment would have been much more complicated and exhausting. Thanks for the continuous help and fruitful collaboration.

Many thanks to PD Dr. Detlef Beckmann, Simone Dehm, Dr. Matthias Hettler, Dr. Wolfram Pernice, and Dr. Michael Wolf for help with fabrication and all the advice in general.

During my time at the INT, many new friendships have formed. I thank Dr. Tatjana Archipov, Daniel Gandyra, Nico Gruhler, Feliks Pyatkov, Patrik Rath, Dr. Cornelius Thiele, and Paul Vincze for all the nice moments spent together.

Finally I would like to thank my family, especially my wonderful wife Svetlana and our newborn daughter Katharina. I appreciated their never-ending support and motivation.

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