A High Current, High Frequency Modular Multiphase Multilevel Converter for Power Hardware-in-the-Loop Emulation

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Abstract

This paper presents a simple Modular Multiphase Multilevel Converter (MMPMC) especially for the usage in Power Hardware-in-the-Loop Emulation systems. Standard half-bridges connected to flux compensated chokes are used to build up an inductive voltage divider to form the multilevel voltage waveform. A modulator with a sorting algorithm is employed to calculate the switching signals of the particular branches. The selection of the switching states is depending on the instantaneous branch currents to ensure a symmetrical distribution of the load current to the branches. A modular and scalable converter system has been engineered, which allows the generation of a six level voltage waveform with a PWM-frequency up to $100\ \mathrm{kHz}$. The prototype is controlled by a specifically designed high-performance signal processing system and offers an output current of more than $100\ \mathrm{A}$. Measurements were performed to evaluate the proper functionality of the converter.

1. Introduction

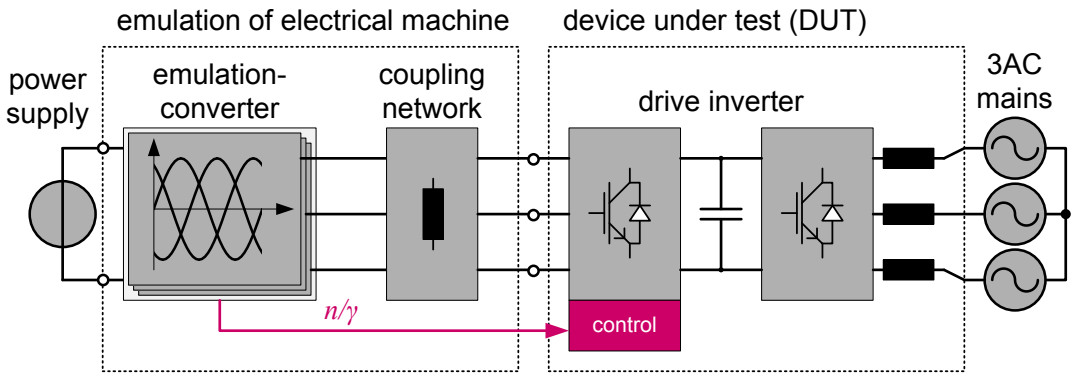

Fig. 1: Typical Power Hardware-in-the-Loop Emulation test bench

Power Hardware-in-the-Loop Emulation test benches (Fig. 1) are used to test control strategies or manufacturing processes of power converters instead of a real machine test bench with rotating components. Thereby, it is common practice to connect the device under test (DUT) to a second converter by means of a coupling network to emulate the electric machine. Depending on the emulation concept, the coupling network consists of a simple choke or a LCL-Filter-Network [1]. The emulation-converter either controls the current in the coupling network, which is similar to the stator current, or the voltage at the coupling network which equals the Electro-Magnetic-Force (EMF) of the emulated machine. However, to emulate the machine behavior at the best rate, it is preferable to feed the coupling network by a high-precision 3AC voltage

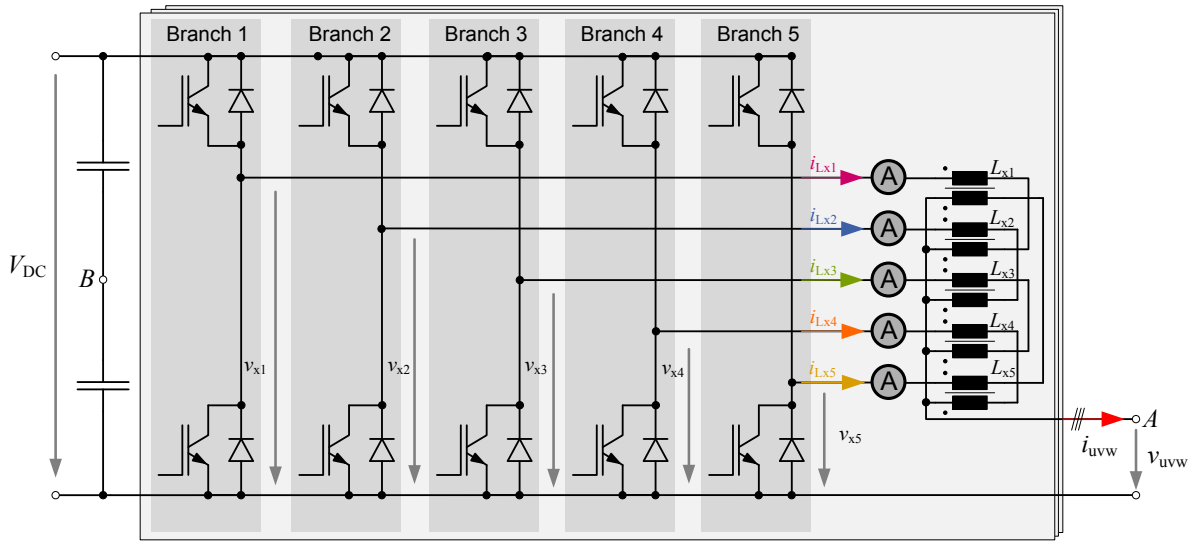

Fig. 2: Proposed converter topology for Power Hardware-in-the-Loop Emulation (n = 5)

source. The most important requirements to this voltage source are a low harmonic distortion (THD), high dynamics, high precision and a low internal resistance. There are a lot of different topologies in the literature [2, 3, 4, 5, 6] to realize a converter with high voltage quality. To obtain a flexible Power Hardware-in-the-Loop test bench it is desirable to use a modular converter topology which uses only standard components. If required, it should be possible to increase the output power as well as the number of voltage levels. Modular Multilevel Converters (MMC) perform most of those requirements [2]. Although, Modular Multilevel Converters are a serial topology why the output power is scalable by the output voltage. Furthermore, MMCs have critical operation points because of the internal cell balancing tasks [3, 7]. Due to the fact that Power Hardware-in-the-Loop Emulation systems are commonly used to emulate low voltage drives, multilevel converters with parallel branches are more adequate to scale the output power. Yet a lot of the parallel topologies have also disadvantages like the missing scalability [5] or the need of special chokes [4] and power modules [6].

2. The Proposed Converter Topology

The proposed converter, see Fig. 2, consists only of standard components like standard IGBT-half-bridges and two winding flux compensated chokes and is very easy scalable. With the use of n-half-bridges and n-chokes, $n+1$ constant voltage levels are possible. Additionally, the associated modulation strategy offers a resulting control frequency f_c of the output voltage and a resulting output current i_{uvw} which are approximately n times greater than the individual switching frequency f_s or output currents of the single IGBT-branches i_{Lxy} ($x \mathrel{\widehat{=}}$ output phase number, $x \in \{u, v, w\}$ and $y \mathrel{\widehat{=}}$ branch number, $y \in \{1, 2, ..\}$). Hence, it is possible to generate an output power of several hundred kW and an output voltage waveform with a resulting switching frequency of more than $100\ \mathrm{kHz}$ with a very low harmonic distortion (THD).

2.1. Functionality of the Proposed Converter Topology

The multilevel output voltage is generated by means of an inductive voltage divider consisting of the flux compensated chokes L_{x1} to L_{xn} (Fig. 3.a). The use of flux compensated chokes

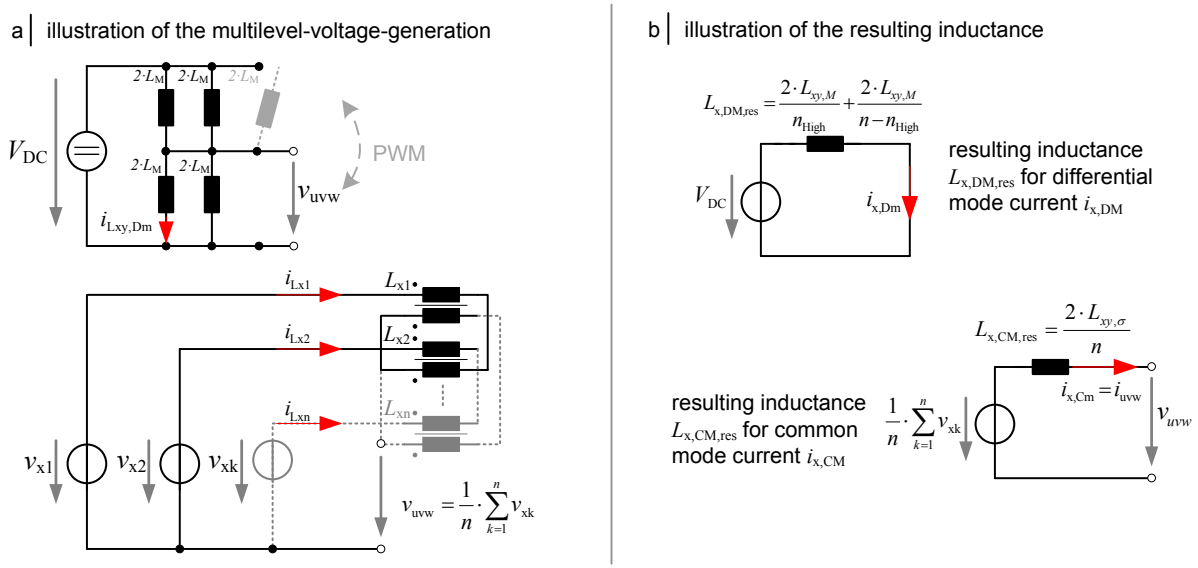

Fig. 3: Illustration of the voltage generation and the resulting output inductance of the proposed converter

yields two advantages. Firstly, the resulting output inductance is only the leakage inductance of the chokes divided by the number of chokes $L_{\mathrm{x,CM,res}} = \frac{2 \cdot L_{\mathrm{xy},\sigma}}{n}$ (Fig. 3.b). Therefore, the load dependent voltage change of the output voltage v_{uvw} is negligible. Secondly, the magnetic design of the chokes is independent from the load current. For this reason only the differential branch current $i_{\mathrm{Lxy,Dm}}$ has to be considered for the magnetic design of the chokes. Hence, the inductance of the voltage divider $L_{\mathrm{x,Dm,res}}$ can be very high. Under worst case conditions $L_{\mathrm{x,Dm,res,min}}$ (Fig. 3.b) is at least:

$$L_{\mathrm{x,Dm,res,min}} = \frac{8 \cdot L_{\mathrm{xy,M}}}{n} \qquad \text{for} \qquad n = 2 \cdot m \qquad m \in \mathbb{N} \tag{1}$$

$$L_{\mathrm{x,Dm,res,min}} = \frac{8 \cdot n \cdot L_{\mathrm{xy,M}}}{n^2 - 1} \qquad \text{for} \qquad n = 2 \cdot m + 1 \qquad m \in \mathbb{N} \tag{2}$$

Consequently, the current $i_{\mathrm{x,Dm}}$ in the voltage divider is negligible compared to the output current i_{uvw}.

$$i_{\mathrm{uvw}} = \sum_{k=1}^{n} i_{\mathrm{Lxk}} - i_{\mathrm{x,Dm}} \approx \sum_{k=1}^{n} i_{\mathrm{Lxk}} \tag{3}$$

2.2. Modulation Scheme

A novel modulation scheme (Fig. 4) is used to set the output voltage v_{xw}. First of all, the current in every branch is measured at the beginning of the pulse-period (Fig. 4.a). Subsequently, an algorithm sorts the choke currents i_{Lxy} in ascending order (Fig. 4.b). Dependent on the desired output voltage v_{xw}, n_{High} branches are switched to "$High$" (Fig. 4.c) during the whole modulation period. n_{High} is defined as:

$$n_{\mathrm{High}} = \left\lfloor \frac{v_{\mathrm{xw}} \cdot n}{V_{\mathrm{DC}}} \right\rfloor . \tag{4}$$

Each branch with activated top switch generates an output voltage level of $\frac{V_{DC}}{n}$. One branch is modulated by a pulse width modulation (PWM) to generate the desired voltage v_{xw} as short-time mean value over one switching period (Fig. 4.d). The duty-cycle of the PWM-switch is

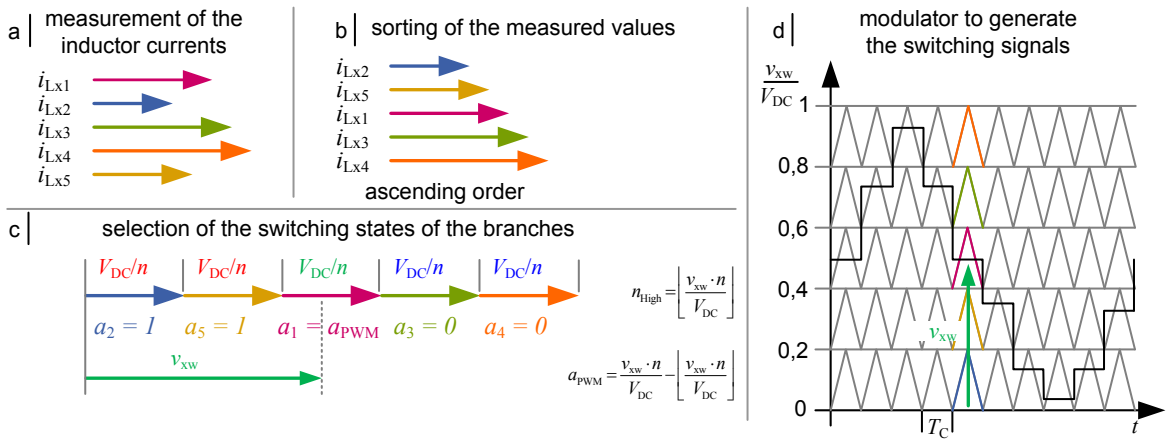

Fig. 4: Modulation cycle of the proposed converter

calculated to:

$$a_{\mathrm{PWM}} = \frac{v_{\mathrm{xw}} \cdot n}{V_{\mathrm{DC}}} - n_{\mathrm{High}} \tag{5}$$

The sorting algorithm ensures that the branch with the lowest current is first switched to "$High$" and the branch with the highest output current is first switched to "Low", therefore an unbalance in the branch currents is avoided. This kind of balancing is similar to the cell balancing in Modular Multilevel Converters [8] and is adapted to this application. A modulator, based on the well-known Split-Carrier-Modulation (Fig. 4.d), is implemented to generate the switching signals. The frequency of the reference carrier signals is $f_c = \frac{1}{T_c}$. The assignment of the branches to the particular triangular reference carrier signals is corresponding to the sort sequence of the branch currents. The duty-cycle (a_{xy}) of the branch with the lowest current is compared to the lowest triangular reference carrier signal. The duty-cycle (a_{xy}) of the branch with the highest current is compared to the top triangular reference carrier signal (Fig. 4.d). It has to be considered that the assignment is different in each modulation period. Assuming the sorting algorithm works under ideal conditions, the average switching frequency of a branch is calculated to:

$$f_{\mathrm{s}} = \frac{f_{\mathrm{c}}}{n} + \frac{n_{\mathrm{vlc}}}{2 \cdot n} \cdot f_{v_{\mathrm{w}}} \tag{6}$$

where $f_{v_{\mathrm{w}}}$ is the frequency of a sinusoidal output voltage and n_{vlc} the number of voltage level changes over one period $T_{v_{\mathrm{w}}} = \frac{1}{f_{v_{\mathrm{w}}}}$. Since, f_{s} is highly affected by the number of voltage level changes, the switching frequency can be higher if there is a control unit that demands a voltage with harmonic components.

3. Hardware Platform

A single phase prototype was developed to evaluate the performance of the proposed converter (Fig. 5.a). The prototype consists of five branches of a specifically designed modular power converter (standard six-pulse bridge). The power converter (Fig. 5.b) is based on the FS75R12KT4-B15 IGBT-module from Infineon ($V_{\mathrm{CE}} = 1200\ \mathrm{V}$, $I_{\mathrm{C}} = 75\ \mathrm{A}$), has double euroboard format and is built as plug-in unit for a 19" rack to get a scalable test bench. A FPGA-Board was also developed to implement the modulator. The core of the FPGA-Board is a Cyclone 4 FPGA (EP4CE40F23C6) from Altera. The FPGA-Board is directly connected to

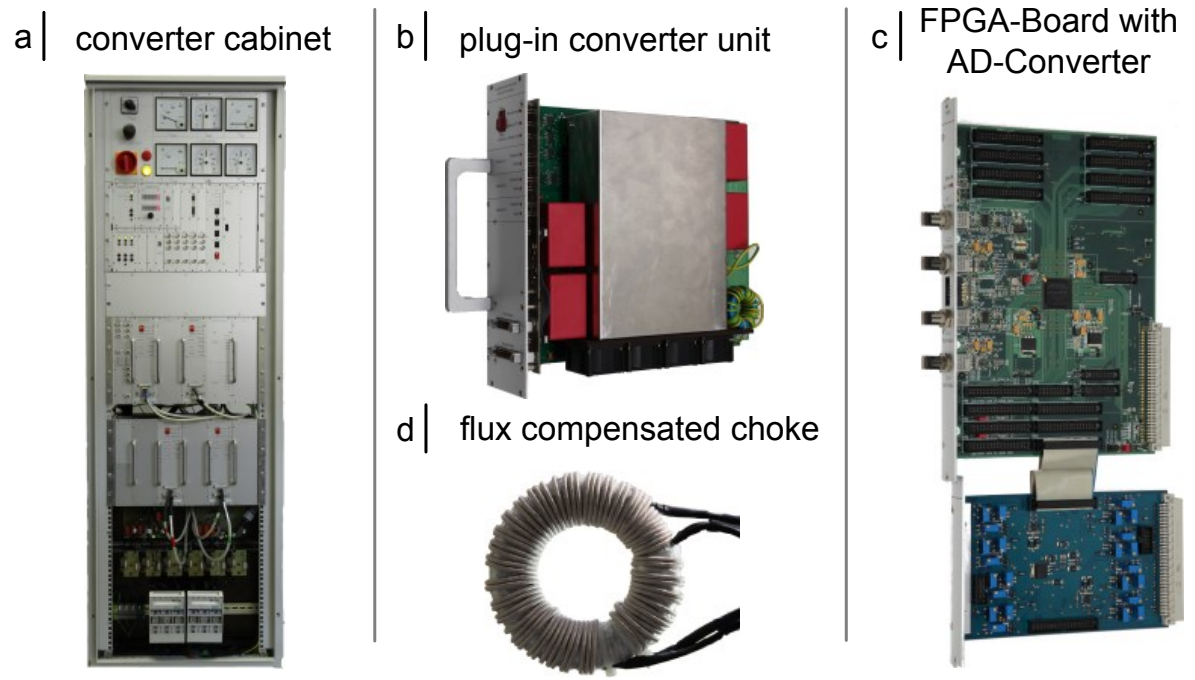

Fig. 5: Hardware setup of the proposed converter

THS1206 A/D-Converters from Texas Instruments with a sample rate of 1.5 MS/s to measure the output currents (Fig. 5.c).

3.1. Design of the flux compensated choke

The flux compensated choke (Fig. 5.d) is also specifically designed. The core of the flux compensated choke is a ring shaped strip-wound core and consists of the nanocrystalline material Vitroperm 500F from VAC. This material offers a saturation flux density of $1.2\ \mathrm{T}$ combined with very low core-losses ($P_{VK} \approx 60\ \frac{\mathrm{W}}{\mathrm{kg}} \cdot m_K$ @ $20\ \mathrm{kHz}, \hat{B} = 1\ \mathrm{T}$) [9]. One of these cores has the dimensions: $\varnothing = 130\ \mathrm{mm}, w = 25\ \mathrm{mm}$ and weighs $m_K = 0.727\ \mathrm{kg}$. The cross-section of the core is $A_K = 274\ \mathrm{mm}^2$. The mutual inductance $L_{\mathrm{xy,M}}$ of the designed choke was set to $18\ \mathrm{mH}$ and the remaining leakage inductance is $L_{xy\sigma} \approx 8\ \mu\mathrm{H}$. This causes a maximum differential current of $\hat{i}_{\mathrm{Lxy,Dm,max}} = \pm 0.56\ \mathrm{A}$ under worst case conditions ($U_{\mathrm{DC}} = 800\ \mathrm{V}, f_{\mathrm{s}} = 20\ \mathrm{kHz}$). The windings are realized with high frequency litz wire.

4. Measurement results

The voltage waveform of the MMPMC as well as the waveforms of the differential and common mode branch currents were measured with a 12 Bit oscilloscope (HRO64Zi) from Le Croy combined with a Tektronix A6303Zi current probe and a P5200 differential probe. An oscillogram of the six-level output voltage in open-circuit operation is shown in Fig. 6. The DC-Link voltage was set to $700\ \mathrm{V}$. The frequency of the reference carrier signals in the modulator is $f_{\mathrm{c}} = 100\ \mathrm{kHz}$. The fundamental frequency of the output voltage is $f_{v_{\mathrm{w}}} = 100\ \mathrm{Hz}$. It has to be considered that the measurements were made in feed-forward operation. According to equation (6), the average switching frequency of an IGBT-branch in steady-state operation should

branch [n]	switching frequency f_s / kHz	difference / %
1	20.852	3.844
2	21.572	7.430
3	20.818	3.673
4	21.144	5.296
5	20.798	3.576

Tab. 1: Switching frequency of the particular branches for open-circuit operation

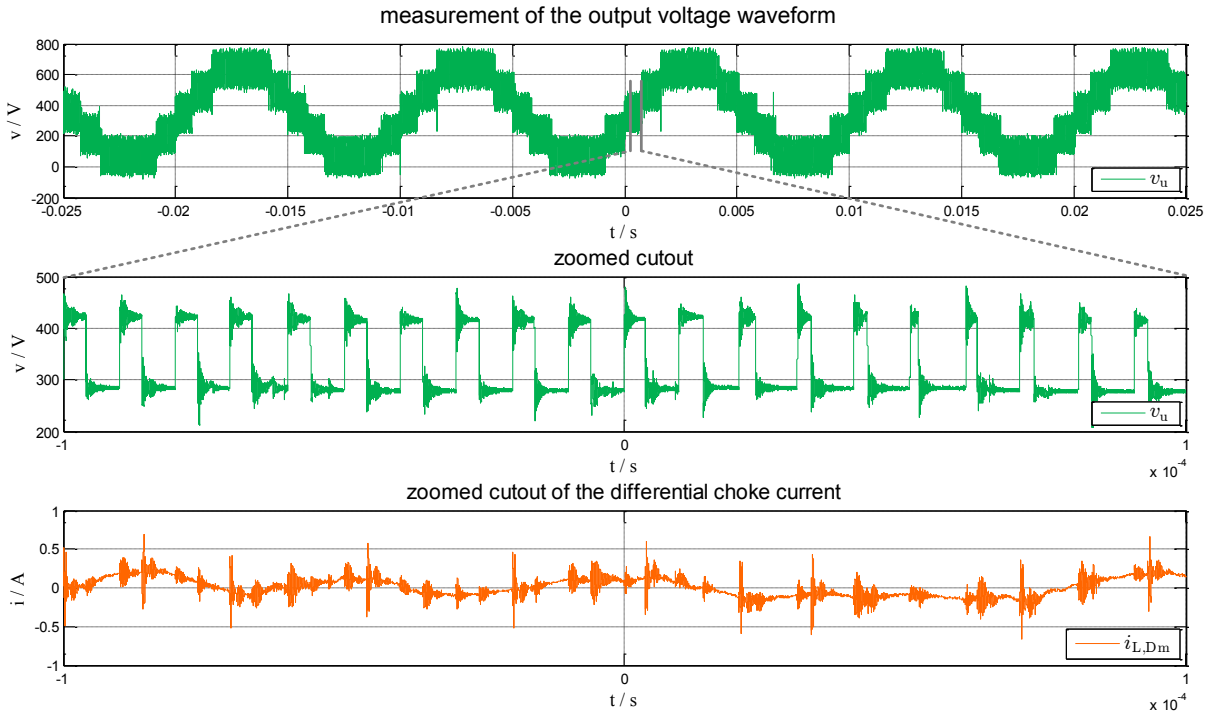

Fig. 6: Measurement results in open-circuit operation

be $f_\mathrm{s} = \frac{100\ \mathrm{kHz}}{5} + \frac{8}{2 \cdot 5} \cdot 100\ \mathrm{Hz} = 20.08\ \mathrm{kHz}$. Tab. 1 shows the measured values of the switching frequencies of the particular branches and the relative difference to the theoretical switching frequency. The switching cycles were counted over $1\ \mathrm{s}$ in the FPGA. It is obvious that the switching frequency in every branch is higher than the expected value. The reason for this are measurement inaccuracies of the branch current measurements which affects the sorting algorithm and leads to additional switching operations. The unbalance of the switching frequency is due to the tolerance of the magnetic material of the chokes which leads to different mutual inductances $L_\mathrm{xy,M}$ and therefore to dissimilar differential current slopes in the branches. This causes also additional switching operations in the branches with the lowest mutual inductance. Furthermore, the quality of the output voltage waveform was evaluated. Therefore, the output voltage waveform was analyzed by the power analyzer LMG500 from ZES Zimmer to estimate the harmonics and the THD of the output voltage. The THD of the unfiltered output voltage u_uvw was measured by the power analyzer to $THD = 1.645\%$. Due to the fact that the LMG500 analyzes only the fundamental frequency and 99 harmonics ($10\ \mathrm{kHz}$), the THD will be higher if especially the harmonics around the modulation frequency would be considered.
Subsequently, the converter was connected to a RL-load with a resistance of $0.4\ \Omega$ and an inductance of $4\ \mathrm{mH}$. The load was connected between the output of the Modular Multiphase

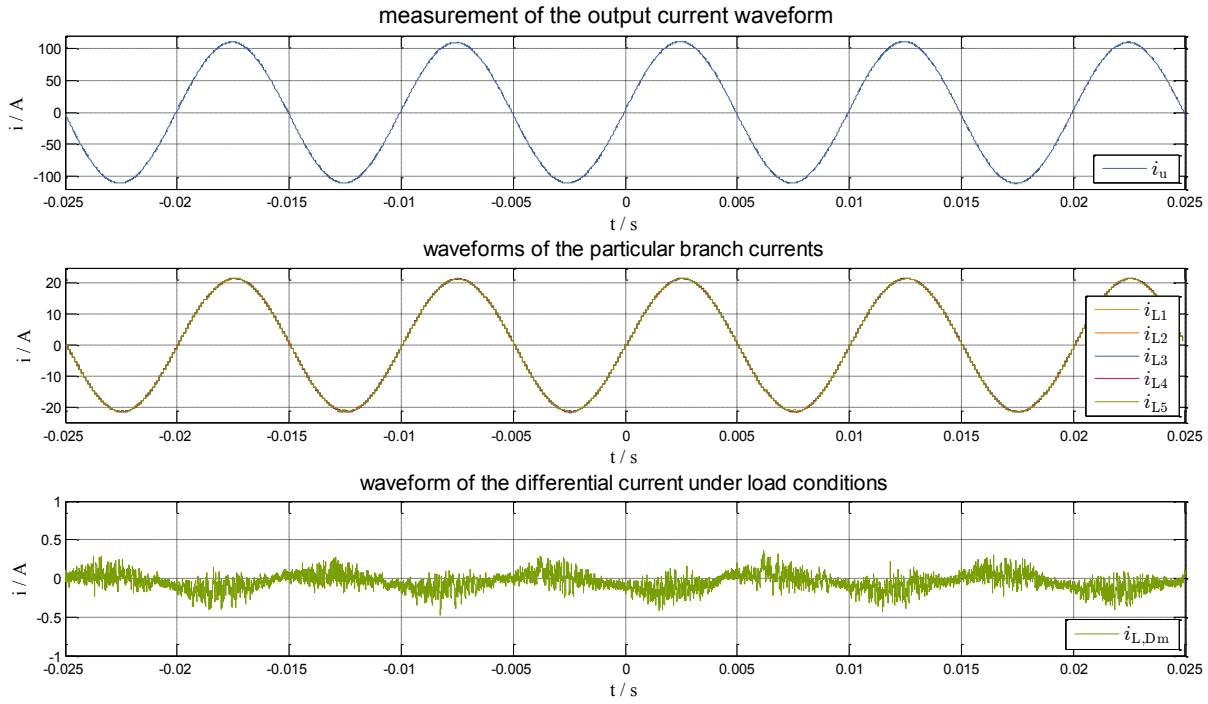

Fig. 7: Measurement results under load conditions for a RL-Load ($R = 0,4\ \Omega$, $L = 4\ \mathrm{mH}$)

Multilevel Converter (A) and the middle of the DC-Link capacitor (B), see Fig. 2. In this case the DC-Link voltage was set to $V_{\mathrm{DC}} = 500\ \mathrm{V}$. Fig. 7 shows the resulting output current (Fig. 7, 1st plot), the five identical branch currents (Fig. 7, 2nd plot) and a differential choke current under load conditions (Fig. 7, 3rd plot). The branch currents were measured with the AD-Converter of the modulator and read out from the FPGA every $100\ \mu\mathrm{s}$. It can be seen that the sorting algorithm works well and the differential mode current of one branch is negligible compared to the branch and load current.

5. Conclusion

A highly flexible Modular Multiphase Multilevel Converter for the usage in Power Hardware-in-the-Loop Emulation systems is introduced. The converter is easy scalable and uses only standard components like IGBT-half-bridges and flux compensated chokes. The multilevel output voltage is generated by an inductive voltage divider and a Split-Carrier-Modulator with a sorting algorithm. The sorting algorithm calculates the switching states of the particular branches depending on the instantaneous branch currents and ensures a symmetrical distribution of the load current to the branches. A single-phase prototype converter with an output current of more than $100\ \mathrm{A}$ is designed as well as a high-performance signal processing system which allows a resulting switching frequency of the multilevel voltage waveform of $100\ \mathrm{kHz}$. Measurements were performed to evaluate the proper functionality of the converter.

5.1. Outlook

Future research will investigate if a direct measurement of the differential choke current is advantageous. This offers the advantage that the differential current can be measured with very high resolution for the sorting algorithm to avoid additional switching operations. Afterwards, a Power Hardware-in-the-Loop Emulation test bench with a three-phase MMPMC will be build up. In the test bench the inverse machine model as well as the modulator of the MMPMC will be directly implemented in the FPGA of the high-performance signal processing system. This offers the possibility of calculating the machine model with $1.5\ \mathrm{MHz}$ and to create the EMF of the emulated machine without additional dead-times.

6. References

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