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# A Transformerless Single-Phase PV Inverter Circuit for Thin-Film or Back-Side Contacted Solar Modules

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**Abstract**— This paper deals with a new transformerless single-phase photovoltaic inverter circuit. The circuit is well suited for thin-film or back-side contacted solar modules because one pole of the solar module can be directly connected to the neutral conductor. The circuit uses a flying capacitor for one of both half-waves, requires only five transistors and is capable of providing inductive as well as capacitive reactive power.

**Keywords** – Power Electronic Converters

## I. INTRODUCTION

Solar inverters have to fulfill several requirements dependent on the configuration of the photovoltaic system. Many thin-film solar modules require positive voltages to earth to prevent them from an irreversible damage by corrosion of the Transparent Conductive Oxide (TCO). In contrast to this, many back-side contacted solar modules require negative voltages to earth to achieve a high efficiency. The technical background of these effects is described in [1] and [2]. Furthermore, some grid codes, e.g. [3], specify that photovoltaic inverters must be able to provide reactive power at the AC-side.

Efficient and transformerless single phase solar inverters are described in [4-8]. They are well-suited for standard silicon modules but it is not possible to connect one pole of the solar generator to earth. Furthermore capacitive leakage currents with fundamental grid frequency occur at the solar modules because the DC input is floating. Inverters with transformer [9] allow a galvanic isolation between input and output but they are usually less efficient and more bulky than transformerless circuits. A transformerless circuit with flying inductor, where one pole of the solar modules can be directly connected to the neutral conductor is described in [10]. However, this topology is not capable of delivering reactive power at the AC-side. A combination of a boost converter with a DC-AC inverter for the usage with thin-film solar modules is described in [11]. The additional boost converter requires additional components and causes additional losses. The circuit described in [12] allows a connection of one pole of the solar modules with earth and is capable of delivering reactive power at the AC-side. There, a flying inductor is used to transfer energy from the solar module to an internal DC-Link. Inductors have a long lifespan compared to electrolytic capacitors, but it is disadvantageous that they require much more space per storable electrical energy than flying electrolytic or flying film capacitors. The circuit described in [13] uses a flying capacitor which is

charged from the DC-side during the free-wheeling states. This inverter allows a connection of one pole of the solar modules with earth but the flying capacitor has to be used for both half-waves. Another circuit where one pole of the solar module string is connected to the neutral conductor is described in [14]. That circuit requires only five transistors and is capable of delivering inductive as well as capacitive reactive power but is built up with a relatively large flying electrolytic capacitor.

In this paper, a new circuit arrangement for the usage with thin-film or back-side contacted solar modules is described and investigated. It uses a relatively small flying film capacitor for the energy transfer during one of both half-waves.

## II. INVERTER CIRCUIT AND FUNCTION

The circuit diagram of the inverter is shown in Fig. 1. The negative pole of the solar module string  $G1$  is directly connected to the neutral conductor  $N$ , which is usually connected to protective earth (PE). This configuration allows the connection of thin-film solar modules. For back-side contacted solar modules, all power semiconductors and electrolytic capacitors have to be connected in reversed polarity, so that the positive pole of the solar module string is connected to the neutral conductor  $N$ .

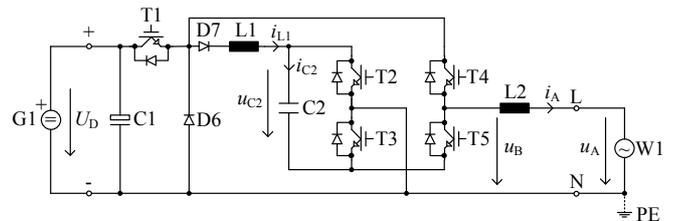


Fig. 1. The single-phase PV inverter circuit

The blocking voltages of all power semiconductors (T1 – T5, D6 – D7) do not significantly exceed the voltage  $U_D$  of the string, so that standard 1200V semiconductors can be used in applications with string voltages up to 800..1000V.

### A. Basic switching states

Fig. 2 shows the switching states 1, 2, 3a and 3b of the circuit. In 3a and 3b the same switches are closed but in 3b an additional current, flowing through the inductor  $L1$ , is highlighted.

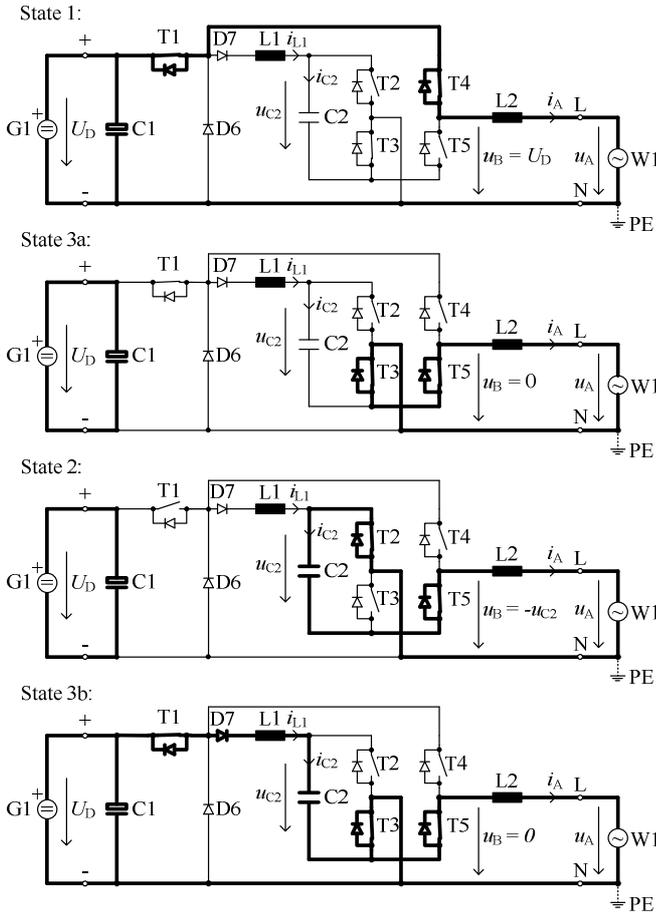


Fig. 2. Basic switching states of the single-phase PV inverter circuit

As long as the reference value  $u_B^*$  of the output voltage is positive, the states 1 and 3a are used. In state 1,  $u_B = U_D$  is applied and in state 3a,  $u_B = 0$  is applied by a pulse width modulation. This operation mode is similar to a buck converter. The durations of the states 1 and 3a during one pulse period  $T$  are calculated to:

$$\frac{T_1}{T} = \frac{u_B^*}{U_D} \quad (1)$$

$$\frac{T_{3a}}{T} = 1 - \frac{u_B^*}{U_D} \quad (2)$$

$T$  is the reciprocal of the switching frequency  $f_{sw}$ :

$$T = \frac{1}{f_{sw}} \quad (3)$$

As long as  $u_B^*$  is negative, the states 2 and 3b are used. In state 2,  $u_B = -u_{C2}$  is applied and energy is transferred from the flying capacitor  $C_2$  to the AC-grid  $W_1$ . In state 3b,  $u_B = 0$  is applied and the capacitor  $C_2$  is recharged from  $G_1$  and  $C_1$  via  $T_1$ ,  $D_7$ ,  $L_1$  and  $T_3$ . The durations of the states 2 and 3b are:

$$\frac{T_2}{T} = \frac{-u_B^*}{u_{C2}} \quad (4)$$

$$\frac{T_{3b}}{T} = 1 - \frac{-u_B^*}{u_{C2}} \quad (5)$$

The circuit is capable of providing reactive power at the AC-side because energy from the AC side can be stored in its capacitors. If  $u_B^*$  is positive and  $i_A$  is negative, energy is transferred from  $W_1$  to  $C_1$ . If  $u_B^*$  is negative and  $i_A$  is positive, energy is transferred from  $W_1$  to  $C_2$ .

The described circuit and its function is close to [14] but in contrast to [14] the flying capacitor  $C_2$  is charged by a DLC (diode, inductor, capacitor) circuit. This allows the use of a very small capacitance value for  $C_2$ . A DLC circuit for charging a flying capacitor is known from [13]. In [13] the flying capacitor is used to transfer the energy for both half-waves of the sinusoidal output voltage, whereas the described circuit only uses the flying capacitor for one half-wave. This leads to low losses and a smaller RMS current in the capacitor which is connected parallel to the solar module string (here:  $C_1$ ).

### B. Charging process of the flying capacitor

The energy  $\Delta W_{C2}$  that is transferred from  $C_2$  to  $W_1$  in state 2 is:

$$\Delta W_{C2} = u_B^* \cdot i_A \cdot T \quad (6)$$

During state 2, the capacitor  $C_2$  is discharged from the voltage  $U_{C2,max}$  to  $U_{C2,max} - \Delta U_{C2}$ . The voltage difference  $\Delta U_{C2}$  can be calculated to:

$$\Delta U_{C2} = U_{C2,max} - \sqrt{U_{C2,max}^2 - \frac{2 \cdot \Delta W_{C2}}{C_2}} \quad (7)$$

The charging process of  $C_2$  is initiated by closing  $T_1$ , see Fig. 3. When  $T_1$  is conducting, the half-sinusoidal charging current  $i_{L1} = i_{C2}$  is rising until  $u_{C2} \approx U_D - U_f$  and then decreasing again.  $U_f$  is the sum of the forward voltage drops of  $T_1$ ,  $D_7$  and the parallel diode of  $T_3$ . The charging process is automatically terminated by  $D_7$  when  $i_{L1}$  reaches zero. Hence, a measurement of  $i_{L1}$  is not necessary for the operation of the circuit. The blocking voltage of  $D_7$  is only a fraction of  $U_D$ . Therefore,  $D_7$  can be a lower voltage type than the other semiconductors.

Assuming, that  $C_1 \gg C_2$ , the charging time  $T_{charge,ZCS}$  which is necessary for a zero-current-switching charging process can be calculated by:

$$T_{charge,ZCS} = \frac{1}{2 \cdot f_{res}} = \pi \cdot \sqrt{L_1 \cdot C_2} \quad (8)$$

The energy  $W_{L1}$ , that has to be stored in  $L_1$  is:

$$W_{L1} = \frac{1}{2} \cdot L_1 \cdot \hat{i}_{L1}^2 = \frac{1}{8} \cdot C_2 \cdot \Delta U_{C2}^2 \quad (9)$$

$W_{L1}$  is only a fraction of the transferred energy  $\Delta W_{C2}$  and decreases with increasing DC-voltage  $U_D$ . Therefore,  $L_1$  will

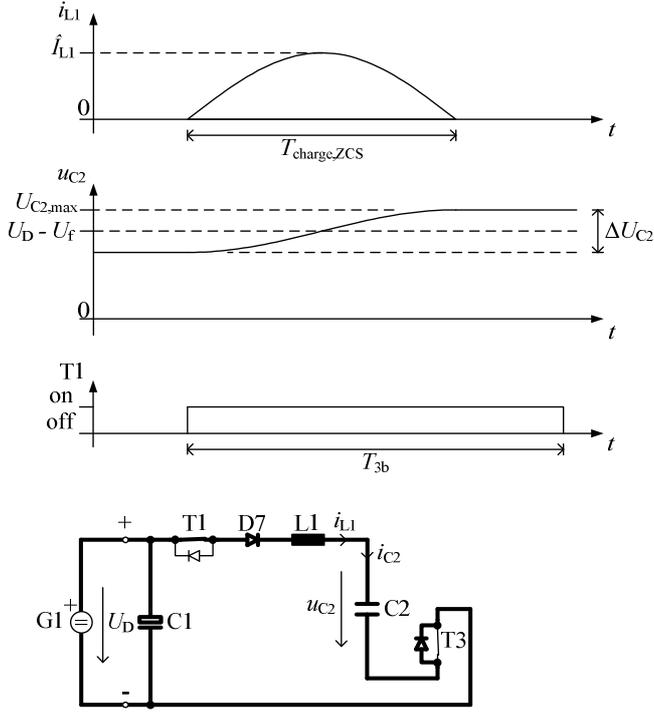


Fig. 3. DLC circuit and charging process of the capacitor C2

be small and cheap, compared to inductors of boost converters [11] and compared to the flying inductors of the circuits that are described in [10] and [12]. The peak value of the charging current  $\hat{I}_{L1} = \hat{I}_{C2}$  is:

$$\hat{I}_{L1} = \frac{1}{2} \cdot \sqrt{\frac{C_2}{L_1}} \cdot \Delta U_{C2} \quad (10)$$

The components D7 and L1 allow high values of  $\Delta U_{C2}$  at acceptable values of  $\hat{I}_{L1}$ . Because of this the required capacitance of C2 is relatively small, so a film capacitor can be used here.

If T1 is opened before the resonant charging process is completed ( $T_{3b} < T_{\text{charge,ZCS}}$ ), the diode D6 protects T1 from overvoltage. The minimum DC-voltage  $U_D$  that is necessary for a zero-current switching charging process can be calculated by:

$$U_{D,\text{min,ZCS}} = \sqrt{2} \cdot U_{A,\text{RMS}} \cdot \frac{T}{T - T_{\text{charge,ZCS}}} \quad (11)$$

An operation below  $U_{D,\text{min,ZCS}}$  is possible but additional switching losses occur, when T1 is opened and  $i_{L1} = i_{C2} \neq 0$ .

### C. Recommended sequence of switching states

A recommended sequence of switching states is shown in Fig. 4. When switching from state 1 to 3 and back, a dead time shall be maintained. During the dead time, the transistors T4 and T5 are opened (state 4). When switching from state 2 to 3 and back, a dead time shall be maintained as well. During this dead time, T2 and T3 are opened (state 6). T3 shouldn't be opened as long as T1 is conducting to avoid an overvoltage at T4. For this reason, the states 5 and 7 are added.

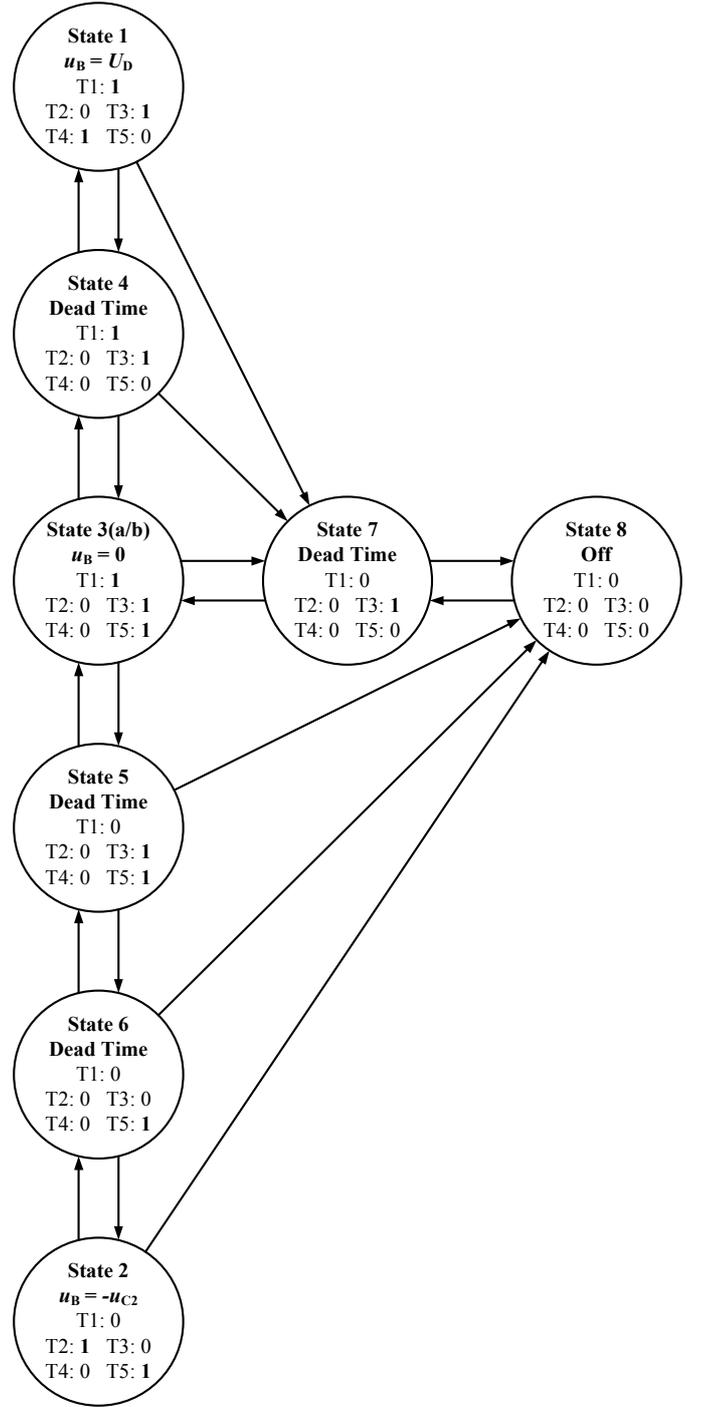


Fig. 4. Recommended sequence of switching states

## III. CONSTRUCTION OF A PROTOTYPE

A prototype has been built up to validate the function of the circuit (Fig. 5). The technical data of the prototype is listed in TABLE I. Important values and part names of components are listed in TABLE II. The semiconductors T1, D7 and the parallel diode of T3 have to be dimensioned for the peak charging current  $\hat{I}_{L1}$ . Therefore T1 is realized by two IGBTs in parallel and T3 is an IGBT with external parallel diode. The diode D7 is a type with a blocking voltage of only 200V and a

low forward voltage. All other semiconductors are 1200V types.

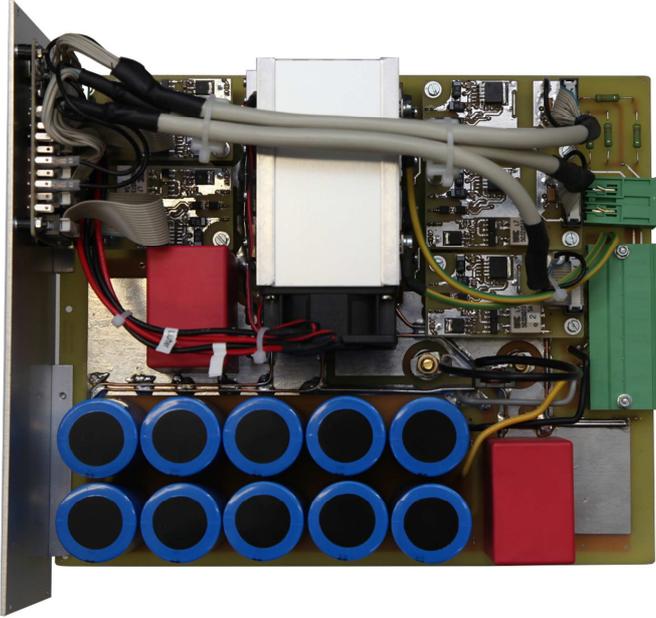


Fig. 5. The PV inverter prototype

TABLE I. TECHNICAL DATA OF THE PROTOTYPE

Description	Symbol	Value
AC voltage	$U_A$	230V
Output frequency	$f_A$	50Hz
Switching frequency	$f_{sw}$	12kHz
Rated power	$S$	3,7kVA

TABLE II. COMPONENT VALUES AND NAMES

Part	Value / Part Name
C1	1750 $\mu$ F
C2	50 $\mu$ F
L1	Coilcraft SER2011-501ML (500nH) + 170nH Air Coil
L2	5mH
D7	DSEI60-02A
T1	2x IRG7PH42UDPbF in parallel
T2, T4, T5	IRG7PH42UDPbF
T3	IRG7PH42UPbF + DSEI120-12A in parallel

L1 is a Coilcraft SER2011-501ML surface-mounted-device (SMD) inductor with an inductance of 500nH. The saturation current, at which the inductance drops 10%, is specified with 100A [15]. A loop wire in series with L1 is used to connect an external current probe for measurement purposes. This loop adds 170nH to the inductance of the SMD coil (Fig. 6). L1 is located on the board shown in Fig. 5, whereas L2 and the current sensor for the AC current  $i_A$  are placed externally.



Fig. 6. The inductor L1 with measurement loop

The system is controlled by a TMS320VC33 Digital Signal Processor from Texas Instruments. The DC voltage  $U_D$ , the capacitor voltage  $u_{C2}$ , the line voltage  $u_A$  and the line current  $i_A$  are measured by a THS1206 A/D-converter from Texas Instruments with a resolution of 12 bits. An EP1C6 FPGA from Altera is generating the signals for the gate-drivers of T1-T5 with a state machine according to Fig. 4. Instead of an FPGA, an ordinary PWM control unit of a microcontroller could be used as well to generate the gate signals for T1-T5 if a few logic circuits are added between PWM control unit and gate drivers.

#### IV. EXPERIMENTAL RESULTS

The following measurements have been performed at the 50Hz grid with a line voltage of  $U_{A,RMS} = 230V$ . A DC laboratory power supply with an external series resistance of 1,8 $\Omega$  for decoupling purposes is feeding the inverter. The DC voltage at the input of the circuit is set to  $U_D = 500V$  and the line current is set to  $i_{A,RMS} = 16,3A$ .

Fig. 7 shows the line voltage  $u_A$ , the three level output voltage  $u_B$ , the line current  $i_A$  and the charging current  $i_{L1}$  at  $\cos \varphi = 1$ .

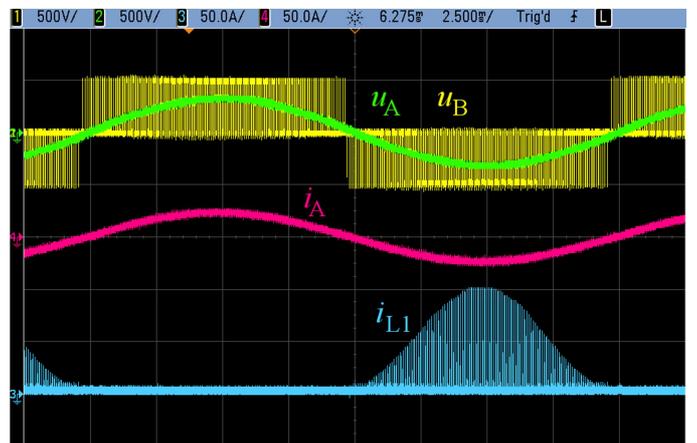


Fig. 7. Line voltage  $u_A$ , output voltage  $u_B$ , line current  $i_A$  and charging current  $i_{L1}$  at  $\cos \varphi = 1$

The ability of delivering capacitive and inductive reactive power at the AC-side has been successfully tested with  $\cos \varphi = 0,9$ . Fig. 8 shows measurement results with leading current and Fig. 9 with lagging current.

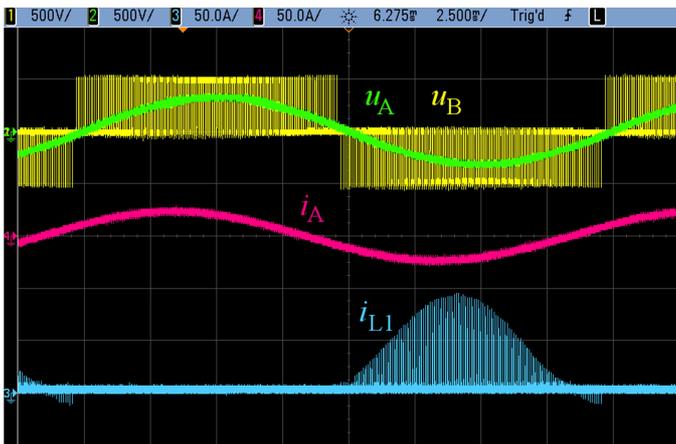


Fig. 8. Line voltage  $u_A$ , output voltage  $u_B$ , line current  $i_A$  and charging current  $i_{L1}$  at  $\cos \varphi = 0,9$ ; leading current



Fig. 9. Line voltage  $u_A$ , output voltage  $u_B$ , line current  $i_A$  and charging current  $i_{L1}$  at  $\cos \varphi = 0,9$ ; lagging current

The charging current  $i_{L1}$  is plotted more detailed in Fig. 10. At  $U_D = 500V$ ,  $T_{3b}$  is larger than  $T_{charge,ZCS}$ , so the charging process is terminated by D7 at a current of zero.

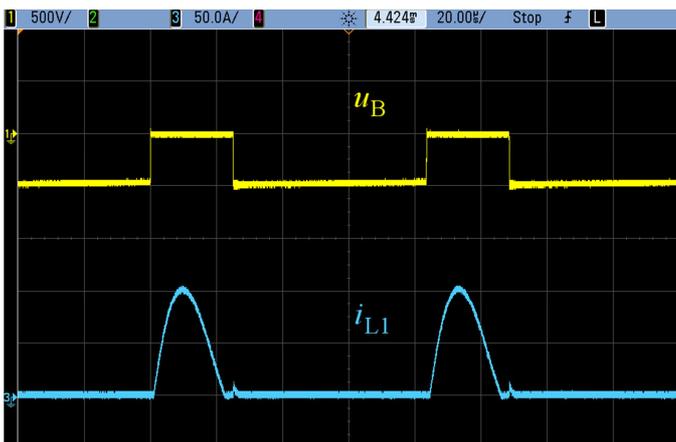


Fig. 10. Output voltage  $u_B$  and charging current  $i_{L1}$  at  $U_D = 500V$  (two switching cycles)

Fig. 11 shows the charging current at  $U_D = 450V$ ,  $U_{A,RMS} = 230V$ ,  $i_{A,RMS} = 16,3A$  and  $\cos \varphi = 1$ . At this operating

point  $T_{3b}$  is smaller than  $T_{charge,ZCS}$ . Here, the charging process is terminated by opening T1 at a current greater than zero.



Fig. 11. Output voltage  $u_B$  and charging current  $i_{L1}$  at  $U_D = 450V$  (two switching cycles)

Efficiency measurements of the circuit were performed with a LMG500 precision power analyzer by ZES Zimmer and the measurement setup shown in Fig. 12, configuration a). The inverter's control system was supplied by an external power supply, so these losses are not taken into account. Fig. 13 shows the measured efficiency  $\eta = P_A / P_D$  at different input voltages  $U_D$ . Below  $U_D = 450V$ , the maximum output power had to be reduced to keep  $i_{L1}$  in a tolerable range.

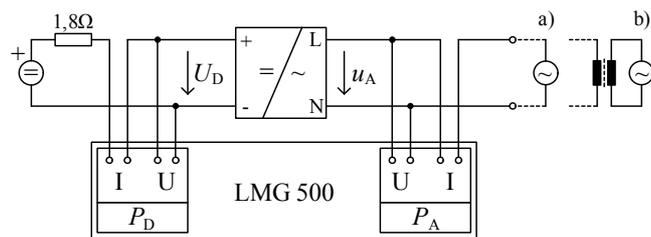


Fig. 12. Setup for efficiency measurement; a) without isolating transformer; b) with isolating transformer

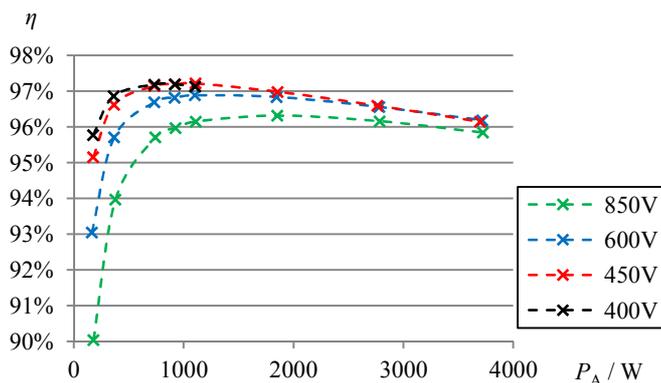


Fig. 13. Efficiency at different values of  $U_D$ ; dashed lines are interpolated

Comparative measurements with an H-Bridge were performed as well to separate the losses in the resonant charging circuit (T1, D7, L1 and T3) from the losses in the AC-

sided bridge (T2-T5 and L2). For this purpose, the inverter circuit was modified, see Fig. 14, while the semiconductors T2-T5, the gate-units and the three level PWM scheme were left unchanged.

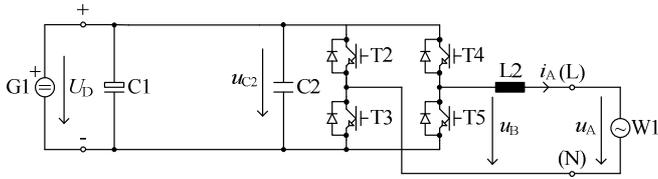


Fig. 14. H-Bridge circuit for loss comparison

The relative additional losses  $p_{CC}$ , caused by the resonant charging circuit are calculated with:

$$p_{CC} = \frac{P_{D, TI} - P_{D, HB}}{P_{D, HB}} \quad (12)$$

$P_{D, TI}$  is the power at the DC-side of the transformerless inverter circuit (Fig. 1) and  $P_{D, HB}$  is the power at the DC-side of the H-Bridge at the same operating point. The chosen three level modulation scheme causes capacitive leakage currents with switching frequency at the terminals of the H-Bridge. Therefore an isolating transformer was added, see Fig. 12 b). The transformer was used for the measurement of  $P_{D, HB}$  as well as for the measurement of  $P_{D, TI}$ .

Measurement results are shown in Fig. 15. Compared to the total inverter losses, the additional losses of the resonant charging circuit are relatively low and decrease with increasing DC voltage  $U_D$ . The main part of the losses is caused by the AC bridge circuit, consisting of T2-T5 and L2.

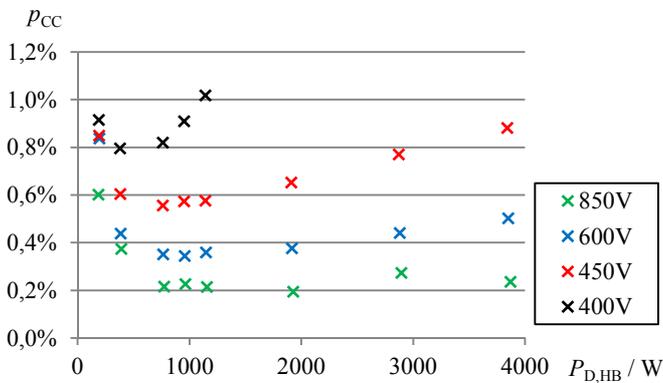


Fig. 15. Relative additional losses of the resonant charging circuit at different values of  $U_D$

## V. CONCLUSION

A new transformerless photovoltaic inverter circuit for thin-film or back-side contacted solar modules is described in detail. It requires only five transistors and is capable of providing capacitive or inductive reactive power at the AC-side. No capacitive leakage currents occur at the modules, because one pole of the solar module string is connected to the neutral conductor. The three level topology leads to low switching losses and a small AC-sided inductor. All semiconductors do not require significantly higher blocking voltages than the

voltage of the solar module string. The energy for one of both half-waves is transferred to the AC-side with a flying capacitor. Its capacitance can be chosen very small, so the usage of a film capacitor with a long lifespan is possible. A prototype has been built up and experimental results show the performance of the inverter.

Compared to a state of the art H-Bridge with three level PWM-scheme, few additional losses occur. If an H-Bridge is used with thin-film or back-side contacted solar modules, an additional isolating element is necessary, e.g. a line transformer or a high-frequency transformer at the DC side. These isolating elements also cause losses. Compared to transformer based solutions, the additional losses of the described circuit with flying capacitor are relatively low.

It has to be considered that the prototype has not been optimized for low losses yet. Therefore it is expectable that the efficiency could be further increased by the use of optimized components e.g. silicon carbide semiconductors.

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