Performance and processability of organic field effect transistors

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The fundamental laws necessary for the mathematical treatment of a large part of physics and the whole of chemistry are thus completely known, and the difficulty lies only in the fact that application of these laws leads to equations that are too complex to be solved.

— Paul Dirac

ABSTRACT

The present work addresses challenges with the performance and processability of organic semiconductors for their application in organic field-effect transistors (OFET). One fundamental issue is the inevitable presence of series resistances across interfaces between conducting and semiconducting materials. It is demonstrated that a time consuming immersion step during fabrication of injection-promoting self-assembled monolayers (SAM) can be carried out as fast as five seconds with insignificant drawbacks to the performance, if processing parameters are optimized. A novel SAM-forming molecule, featuring remarkable performance and stability, is presented and characterized. It is subsequently used to demonstrate a concept for the fabrication of unipolar n- and p-type OFETs from a single semiconductor, determined selectively by the presence or absence of an injection layer treatment. Also, the electrical decoupling of typical charge immobilization sites, provided by inorganic dielectric materials, from the delicate transistor channel via a thin polymer coating is investigated. Furthermore, an approach to prevent interlayer mixing in solution processing of multilayer stacks is presented, using novel polymers with solubility providing alkyl-chains, which can be detached and render the film insoluble by a thermal stimulus after deposition.

The results that are presented in this thesis show that combining advances in chemical material design and interface tailoring with advances in deposition and processing techniques, in order to unfold the potential of organic electronics, is a matter of engineering.

ZUSAMMENFASSUNG

Diese Arbeit befasst sich mit den Herausforderungen an Leistungsfähigkeit und Prozessierbarkeit von organischen Halbleitern für die Anwendung in organischen Feld-Effekt Transistoren (OFET). Ein grundlegendes Problem stellen hierbei unvermeidliche elektrische Widerstände an Kontakten zwischen leitenden und halbleitenden Materialien dar. Es wird gezeigt, dass ein zeitaufwändiger Herstellungsschritt bei der

Tauchbeschichtung von injektionsbefördernden selbst-organisierten Monologen (SAM) mittels optimierter Prozess-Parameter bis zu einer Dauer von fünf Sekunden beschleunigt werden kann. Ein neuartiges Molekül zur Herstellung von SAMs, welches herausragende leistungsfördernde Eigenschaften und eine hohe Stabilität aufweist, wird vorgestellt und charakterisiert. Diese SAMs werden anschließend verwendet um ein Konzept zur Herstellung von selektiv unipolaren n- und p-typ Transistoren aus dem selben Halbleiter, differenziert durch An- oder Abwesenheit der Injektionsschicht, zu demonstrieren. Außerdem wird das Entkoppeln von elektrischen Fallenzuständen, welche an Grenzflächen zwischen organischen Halbleitern und anorganischen Dielektrika entstehen, vom störungsanfälligen Transistorkanal mittels einer dünnen Polymer-Beschichtung untersucht. Darüber hinaus wird ein Konzept vorgestellt das es erlaubt ein Durchmischen an der Grenzfläche zwischen aufeinanderfolgend aus Lösung prozessierter Schichten zu verhindern. Hierfür werden neuartige halbleitende Polymere verwendet, deren löslichkeitsvermittelnde Seitenketten nach der Filmherstellung durch einen thermischen Reiz abgespalten werden können.

Die Ergebnisse die in dieser Arbeit vorgestellt werden zeigen, dass die Zusammenführung von Entwicklungen im chemischen Design neuer Materialien und Grenzflächenmodifizierungen mit Fortschritten in der Prozessierungstechnik eine entscheidende ingenieurwissenschaftliche Herausforderung darstellt, um das Potential der organischen Elektronik auszuschöpfen.

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LIST OF ABBREVIATIONS

BMBF Federal Ministry for Education and Research

FET field effect transistors

OFET organic field-effect transistors

SAM self-assembled monolayers

HOMO highest occupied molecular orbital

LUMO lowest unoccupied molecular orbital

CVD chemical vapor deposition

BCTG bottom contact top gate

TCTG top contact top gate

MOSFET metal-oxide-semiconductor field-effekt transistor

BCBG bottom contact bottom gate

BGTC bottom gate top contact

WF work function

PFDT 1H,1H,2H,2H-perfluorodecanethiol

PES photo-electron spectroscopy

SE single electron

IRRAS infrared reflection absorption spectroscopy

IR infrared

SMU source/measure unit

I/V current/voltage

XPS x-ray photo-electron spectroscopy

UPS ultraviolet photo-electron spectroscopy

HMDS hexamethyldisilazane

ParyleneC poly(chloro-p-xylylene)

OTS octadecyltrichlorosilane

RT room temperature

LED light emitting diodes

OPV organic photovoltaic

TLM transfer line method

OCI Institute of Organic Chemistry

PTAA poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine]

PDTDPP-alt-BTZ poly(diketopyrrolopyrrole-benzothiadiazole)

PEIE ethoxylated polyethylenimine

Juls julolidyl disulfide

NDI 1,4,5,8-naphthalenetetracarboxdiimide

PET polyethylene terephthalate

Part I

INTRODUCTION

1

MOTIVATION

Organic semiconductors attracted considerable attention with groundbreaking work on light emitting diodes (LED) and organic photovoltaic (OPV) cells by Tang and VanSlyke [1, 2] in the mid 1980's. Although electroluminescence of organic materials has already been reported more than 30 years earlier by Bernanose [3], organic semiconductor have been merely a matter of academic research during the silicon technology revolution because of the high operation voltage that were necessary to drive the early devices. Low operation voltages in the devices of Tang et al. were enabled by progress in the deposition techniques for ultra-thin films of organic molecules, and an arising theoretical understanding for the electrical properties of the conjugated carbon bond by Shirakawa, Heeger and MacDiarmid et al. [4, 5], awarded with the Noble Prize for chemistry in 2000. Since then, organic semiconductors have been studied with increasing intensity, and are believed by many to innovate the mass market of consumer electronics in the future, for their soft mechanical properties, as well as flexibility in material design and versatile processability [6, 7, 8, 9]. With the availability of various excellent materials [10] a multitude of electronic and photonic devices from organic semiconductors with high performance have been reported, including LED [11], field effect transistors (FET) [12], OPV [13, 14], sensors [15, 16] and batteries [17]. Also, the fabrication of thin films has been developed away from high-vaccum- and towards solution-deposition, exploiting different printing techniques with continuously improving manufacturing speed and resolution [18, 19, 20].

All these components could one day potentially be combined in ultrathin, flexible, stretchable, lightweight and semitransparent embedded systems [19] with little power consumption, printed at low cost with high throughput. At the same time, the technical challenges and issues of the transition from the lab-scale to industrial fabrication have proven to be substantial and, in some cases, fundamental [21]. Assessments about the speed and impact at which products with organic semiconductors will innovate the consumer market diverge drastically [21, 8, 9]. There is, however, already a number of commercialized organic optoelectronic applications available today [22, 12, 9], although in many cases the key advantages flexibility and/or solution-processability are not yet exploited.

The first reports of field-effect behavior in organic materials date back to 1964 (in copper-phthalocyanine) [23] and 1970 (in metal-free phthalocyanine) [24] . Functional transistor devices followed in the late 1980's [25, 26, 27]. Over the past 25 years, the mobility of charge carriers in OFETs with organic semiconductors has been increased by up to four orders of magnitude [28, 29, 9], and there is no fundamental restraint known to prevent a further increase in the future. Despite this tremendous progress, the mobility of soft van-der-Waals governed materials typically falls short to that of crystalline silicon by three orders of magnitude. Because the switching speed of transistors depends linearly on the mobility, it is beyond dispute that integrated circuits using OFETs won't be competing with single-crystalline computer chips in absolute performance. Realistically, they will be exploited for innovative application fields like low-end integrated micro-electronics [12], sensors [16] or flexible displays from electrophoretic ink, also called "e-paper". Furthermore, there is justified aspiration to implement organic semiconductors in TFT backplanes for flexible displays, as their performance is already comparable to that of amorphous silicon [9], while they possess unmatched flexible [30] and even stretchable [30] properties.

The development of technical measures and processing procedures to optimize device performance and fabrication cost will determine the future success of organic electronics just as much as deriving a fundamental theoretical understanding and new materials with improved properties.

1.1 SCOPE OF THIS WORK

The present work focuses on FET devices with organic polymeric semiconductors. It is dedicated to optimization techniques using well-known materials, as well as the development and characterization of novel materials with improved properties and innovative functionalities. These optimizations exploited in the present work are applied to the interface between metal and semiconductor, where contact resistances compromise device performance, and that between gate insulator and semiconductor, where the conductive channel is located. Furthermore, an approach to avoid interlayer mixing with solution processing of successive layers from solution, via post-deposition solubility reduction by a new class of semiconductor materials, is showcased.

The work was supported with a scholarship from Merck KGaA and carried out in the facilities of the *InnovationLab* [31] in Heidelberg. The InnovationLab was originally formed within the *Leading-Edge Cluster Forum Organic Electronics*, founded in the scope of the *High-Tech Strategy*

for Germany by the Federal Ministry for Education and Research (BMBF). The present work is associated with the BMBF-project MORPHEUS[1], in cooperation with industry- and university-partners[2]. Material synthesis was performed by Torben Aderman, Malte Jesper, Marius Kuhn and Claudia Teusch in the group of Dr. Manuel Hamburger at the Institute of Organic Chemistry (OCI) of the University of Heidelberg. Presented analytical characterizations of thin films via Infrared- and Photoelectron-spectroscopy, among other methods, was performed by Dr. Janusz Schinke, Sabina Hillebrandt and Marc Hänsel at the InnovationLab for the Universities of Braunschweig, Heidelberg and Darmstadt.

1.2 OUTLINE

The present thesis is structured as follows:

In chapter 2, an overview of the theoretical fundamentals to this work is given. Organic semiconductors and their electronic properties, as well as organic field-effect transistors (OFET) and self-assembled monolayers (SAM) are introduced and reviewed briefly. Chapter 3 presents materials and methods that are used to prepare and characterize the devices investigated in this work.

Part ii presents the obtained results, and discusses their specific implications in detail. This part is divided into chapters, according to the place within the transistor at which the investigated effects take place. Chapter 4 is dedicated to the charge injection properties, altered by SAMs, at the metal-semiconductor interface. It contains an approach to reduce the processing time of SAMs to printing relevant timescales, and an investigation of OFETs with both unipolar channel types from one single semiconductor, determined selectively by the injection layer, as a technique to realize complementary logic devices. Furthermore a novel, high performing, molecule for SAM-preparation is presented and characterized. In chapter 5, a method to optimize the chemical conformation of the transistor channel, at the interface between semiconductor and gate dielectric, is investigated. Novel semiconductors that can be casted from solution, but rendered insoluble subsequently via a thermal stimulus, are investigated in chapter 6.

A concluding summary of the results is given in part iii and their implications in context to organic electronics research and development are discussed.

1 Morphologiekontrolle für Effiziente und Stabile Bauelemente (FKZ: 13N11701-13N11706)

2 Universität Heidelberg; Merck KGaA; BASF AG; MPI für Polymerforschung; Technische Universität Braunschweig; Karlsruhe Institute of Technology

2

THEORETICAL FUNDAMENTALS

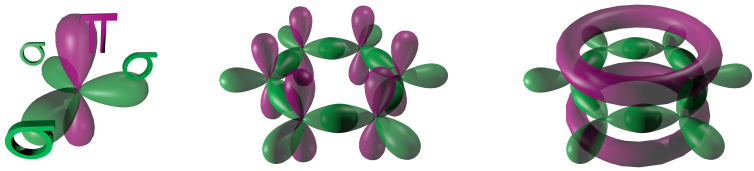
In this chapter an introduction into basic concepts of organic electronics in general and organic field effect transistors in particular is presented, and fundamental differences with respect to established material systems are discussed. The material class of SAM is described and briefly reviewed.

2.1 ORGANIC SEMICONDUCTORS

In a simplified picture, the vast majority of electrons in solid matter is bound in shells with their respective atomic nuclei. Conductive materials differ from this only in a small fraction of electrons, which are delocalized from the outer shell into an electron cloud and follow electrical fields as a current within the compound. Semiconducting materials do not exhibit delocalized charges from the outset, but they can be easily introduced (or *doped*), for example chemically, field-induced or photo-induced. This way the electrical resistance can be controlled precisely, switched in a transistor, or rectified in a diode.

Advantageous properties of soft polymeric over traditional crystalline semiconductors include flexibility, low temperature solution-processability and semi-transparency. These mechanical properties are owed to a fundamental difference in structural order, governed by relatively weak intermolecular Van-der-Waals cohesion forces. Disadvantages are a generally lower mobility and failure of the powerful established modeling approaches which are applied for traditional semiconductors: Solutions of electron quantum mechanical wave functions into eigenstates which create an electronic band structure depend on periodic boundary conditions of an underlying lattice[1]. The access on precise electronic properties of highly-crystalline materials initiated the revolution of microelectronic technology and was enabled by the fabrication of macroscopically big single crystals, which can be described on the atomic scale with a small set of lattice parameters. Essentially, a single-crystalline material is described as one infinite macromolecule and the resulting molecular orbital energies yield a continuous density of states and well defined band gaps. For materials which lack a periodic structure, like amorphous

1 These so called *Bloch waves* were originally introduced in 1928 by Felix Bloch and established the quantum theory of solids.



a) σ- and π-orbitals

b) Orbital arrangement of benzene

c) Delocalized π-electron system

Figure 1: Schematic illustration of charge delocalization in carbon based systems with conjugated bonds. For each carbon atom three localized σ-orbitals (green) are arranged in plane. Normal to this plane, the π-orbitals (purple) can overlap and form delocalized π-electron systems.

polymers in organic electronics do[2], this approach cannot be taken. The exact electronic structure in such low-order materials depends critically on the local morphology. A fully quantum mechanical handling of sufficiently extended volume fractions is practically impossible due to limited computing capacity. In the following, some important concepts on the electronic behavior of low-order semiconductors are introduced.

2.1.1 *Charge delocalization in organic matter*

In chemistry, the term *organic* refers to carbon containing compounds. Carbon has four valence electrons and is therefore well suited to be the basic building block in complex molecules. In carbon based molecules different arrangements of orbitals occupied by the valence electrons occur, yielding drastically deviating properties. The most stable configuration is formed by four equal, tetrahedrally arranged hybrid orbitals[3] of the carbon s- and p- orbitals, the *diamond*. The most important origin of delocalized charges in organic matter is the conjugated carbon-carbon bond. In this configuration, three valence electrons occupy hybrid orbitals of the carbon s- and p- orbitals. These strongly localized, covalent σ-bonds are arranged planar and connect each carbon to three neighboring carbons[4]. The fourth valence electron occupies the π-orbital, normal to the σ-plane. Due to the spatial distribution, and in lack of a bonding partner to equalize its spin, electrons in π-orbitals interact with

2 The terminology is actually more complex here and is discussed in section 2.1.2.1.

3 Mathematically, the concept of hybrid orbitals uses atomic electron orbitals as basis vectors in the vector space of molecular orbitals.

4 The σ-bonds can connect to other neighboring atoms than carbon, not always resulting in a planar arrangement and hence less overlap and delocalization of the π-orbital.

those from neighboring π-orbitals and can form a delocalized π-electron system. A schematic illustration of charge delocalization via π-electron systems in the case of a benzene ring is presented in figure 1.

2.1.2 *Charge transport and doping*

Although delocalized π-electron systems are free to follow an electrical field and should be metallic, conjugated polymers are semiconductors instead. Unlike the perfectly symmetric benzene (see figure 1), non-cyclic conjugated carbon chains of finite length in equilibrium tend to break the equidistant formation in favor of an alternating bond length in a so called *Peierls distortion* [32]. Such a configuration can result in two electron bands, one fully occupied and one unoccupied with a gap in between, and behave as a semiconductor [33, 34]. In contrast to the situation in crystalline semiconductors, these bands do not extend indefinitely but exist in every single molecule. In other words, the frontier electron states are local molecular orbitals instead of delocalized bands. Therefore, they are not called *valence-* and *conducting-band*, but instead highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO). The charge transport between adjacent molecules in low-order semiconductors is typically described as a localized so called *variable-range-hopping transport* [35]. One major difference between delocalized transport within the π-systems and localized transport between adjacent π-systems, besides the orders of magnitude in effectiveness, is the behavior with temperature. For delocalized transport, temperature behavior of the conductivity is dominantly suppressed by phonon-scattering, while hopping is thermally activated and hence temperature supports the transport. The temperature dependency of the mobility is typically put as:

$$\mu = \mu_0 \cdot exp\left[-(T_0/T)^{1/\alpha}\right] \tag{1}$$

(mobility μ; temperature T)

In the most conclusive and accepted theoretical model, charge carriers in organic semiconductors are described as distortions in the 1D lattice, so called *polarons* [5]. Basically, carbon chains with alternating bond length yield two possible lattice configurations, which in turn exist in alternating regions along the chain[5]. The inter-phases between these regions are stable quasi particles with well defined size and effective mass, so called *solitons* with either spin $S = 0$ and charge $Q = \pm e$, or $S = \frac{1}{2}$ and

5 The resulting configuration of the two phases is a trade-off between the energetically favorable single phase and entropy driven disorder.

$Q = 0$. Upon doping, solitons pair up and form polarons or *bipolarons*[6], depending on the quantum numbers of their solitons. They introduce electronic states within the band gap and carry either $S = \frac{1}{2}$ and $Q = \pm e$ (in the case of polarons) or $S = 0$ and $Q = \pm 2e$ (bipolarons). In contrast to solitons, polarons and bipolarons can be transferred between adjacent carbon chains and are suitable to motivate 3D charge transport in organic semiconductors.

2.1.2.1 *On the usage of the term "organic"*

There are examples of single-crystalline systems of organic molecules with intermolecular stacking of π-orbitals close enough for HOMOs and LUMOs of the single molecules to fuse into band behavior. This of course, comes with the sacrifice of unique selling points of organic electronics, like flexibility. The term *"organic"*, as it is used in this thesis (and in the majority of related literature), refers to flexible, or *"soft"*, materials without single-crystalline order, which are governed by van-der-Waals cohesion forces. To avoid repeatedly redundant phrasing, some statements about "organic semiconductors" implicitly exclude single-crystalline organic semiconductors.

2.2 FIELD EFFECT TRANSISTORS

The FET working principle was first patented by J.E. Lilienfeld [36] in 1930 and realized by W. Shockley in 1947 [37]. The FET is a field-controlled transistor device, as opposed to current-controlled bipolar junction transistors. FET are used as the basic logic unit in the majority of electronic applications like integrated circuits, amplifiers or sensors. Since 1960, with the introduction of the silicon-based metal-oxide-semiconductor field-effekt transistor (MOSFET) in digital microprocessors [38], FETs have become an essential part of modern technology.

2.2.1 *Working principle*

In a FET, the resistivity of a semiconducting material between two electrodes (*source* and *drain*) can be regulated by the potential at a third electrode (*gate*). The cross section of such a device is shown schematically in figure 2a. In principle, a FET combines a resistance between

6 More specifically, polarons and bipolarons consist of two solitons each. But only polarons can be created directly from solitons, while bipolarons are created in annihilation of two polarons.

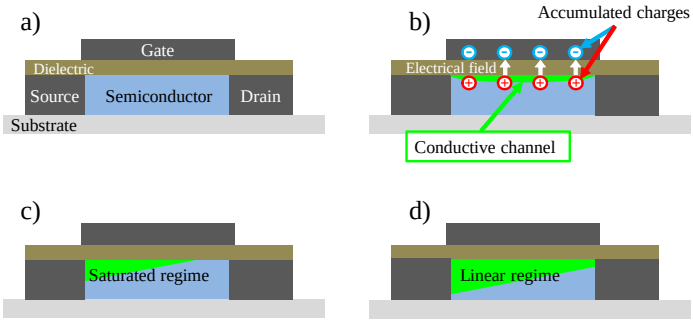


Figure 2: Schematic cross section of a FET. (a) Setup; (b) formation of a conductive channel due to an applied gate bias; (c) channel pinch-off in the saturated operation regime; (c) linear operation regime without pich-off.

source and drain with a capacitor of both to the gate. If the capacitor gets loaded by a potential at the gate electrode, mirror charges are attracted within the semiconductor and accumulate at the interface to the dielectric. The electric field in the semiconductor creates an electrochemically doped conductive *channel* at the interface, as is illustrated in figure 2b. The vertical channel dimension is in the range of a few nanometers, involving only the topmost region[7] of the semiconductor layer. The electric field in the channel is superimposed from the potentials at gate and drain. Hence, the accumulated charge density varies along the channel, depending on the lateral distance to the drain electrode. The conductive part of the channel ends, or *pinches off*, where the electric field underruns a material-specific minimum. Whether the conductive area is pinched off (figure 2c) or covers the complete channel (figure 2d), determines the operation regime to be *saturated* or *linear*.

In figure 3, the energetic alignment of electrodes and semiconductor orbitals is illustrated schematically (after Newman et al. [39]). In a simplified picture one can assume the frontier orbitals in the semiconductor to be dislocated by the resulting electric field, with respect to ground potential (figure 3b). The accumulated electrons (/holes) can access the LUMO (/HOMO) and delocalize to a mobile charge carrier cloud. With an additional potential applied at the drain electrode, a current can flow from the source (figure 3c).

7 This means the region adjacent to the dielectric which, in the example at hand, is on top of the semiconductor. Depending on the device architecture this can also be the bottommost region.

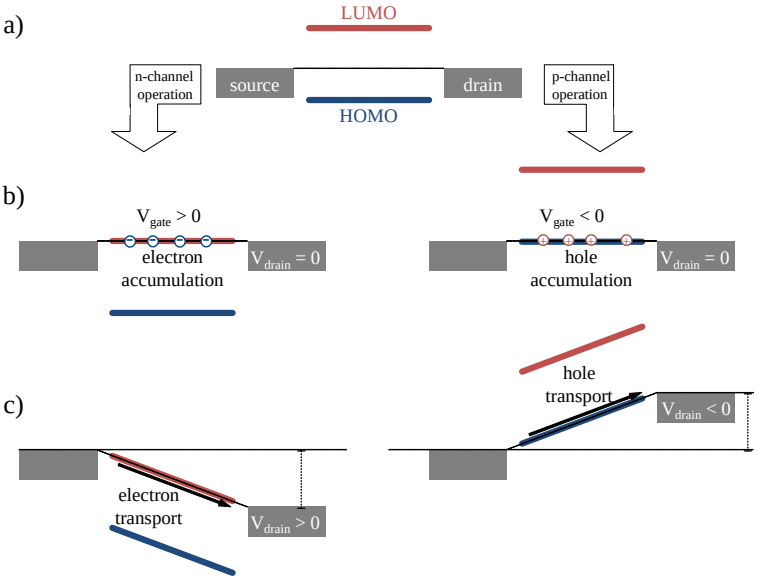


Figure 3: Schematic illustration of the working principle for OFETs in n-type and p-type operation. (a) Idealized energy level diagram in the ground state $V_{gate} = 0$, $V_{gate} = 0$; (b) energetic dislocation of frontier orbitals due to an applied potential at the gate; (c) charge carrier transport. Redrawn after [39].

2.2.2 *Modeling*

2.2.2.1 *MOSFET*

What is known as the MOSFET model today, goes back to an equivalent circuit description of silicon-based field effect transistors in the late 1960's [40, 41, 42, 43]. A new transistor model, simple enough to enable the simulation of integrated circuits by digital computers available at that time, was mandatory to meet constantly increasing circuit complexity. The remarkable advances that followed in digital computer development owe much to the MOSFET model. In organic electronics, the current-voltage equations based on the MOSFET model are commonly adopted for experimental OFET analysis [44]. Yet, not all of the concepts and terminology can be transferred readily from crystalline to soft semiconductors. In some cases, precipitous analogy between these two can actually be misleading. The following derivation of the MOSFET current/voltage (I/V) relations are reproduced after Newman et al. [39] and Kim et al. [44].

The first assumption, called *"gradual channel approximation"*, implies a linear voltage drop along the channel from the potential applied at the drain electrode to ground potential at the source $V = V(x)$. The local effective voltage $V_{eff.}$ is derived from the superposition of $V(x)$ with the potential introduced across the dielectric from the gate, corrected by the threshold voltage:

$$V_{eff.} = (V_G - V_{th}) - V(x)$$

(Gate-voltage V_G; threshold voltage V_{th}) A voltage drop across the interface from the contact to the semiconductor is neglected with this approach[8]. The spacial charge density $Q(x)$ induced in the channel is proportional to the effective local voltage across the gate dielectric:

$$Q(x) = C_i \cdot V_{eff.} = C_i \cdot [(V_G - V_{th}) - V(x)] \tag{2}$$

with the dielectric capacitance per unit area $C_i = \frac{C}{A} = \frac{\epsilon_r \epsilon_0}{d}$ (capacitance C; area A; relative dielectric constant ϵ_r; vacuum permittivity ϵ_0). The conductivity is estimated to be the product of $Q(x)$, representing the vertical thickness of the current path, and the charge carrier mobility μ. If $Q(x) > 0$ at any position along the channel, i.e. $(V_G - V_{th}) > V_D$, the device is operating in the liner regime. The current density $\frac{I_D}{W}$ (drain current I_D; channel width W) from source to drain can be put with Ohm's law as:

8 While this is a valid assumption for silicon-based FET, it is one of the reasons why the model is insufficient for many organic FET, which typically exhibit significant contact resistances.

$$\frac{I_D}{W} = Q(x) \cdot \mu \cdot \frac{dV}{dx}$$

At this point, μ is assumed to be independent of the local electrical field. Separation of the variables leads to:

$$\int_0^L \frac{I_D}{W} \cdot dx = \int_0^{V_D} Q(x) \cdot \mu \cdot dV \tag{3}$$

(channel length L; drain voltageV_D). With insertion of $Q(x)$ (equation 2), the basic I/V relation in the linear regime is derived:

$$I_{D,lin.} = \frac{W}{L} C_i \cdot \mu \left[(V_G - V_{th}) V_D - \frac{V_D^2}{2} \right]$$

If $(V_G - V_{th}) \gg V_D$ is fulfilled, it is appropriate to drop the $\frac{V_D^2}{2}$ term

$$I_{D,lin.} = \frac{W}{L} C_i \cdot \mu \left[(V_G - V_{th}) V_D \right] \tag{4}$$

and derive the *conductance* g_d, and the *transconductance* g_m as:

$$g_d = \left. \frac{\partial I_D}{\partial V_D} \right|_{V_G = const.} = \frac{W}{L} C_i \cdot \mu \cdot (V_G - V_{th}) \tag{5}$$

$$g_m = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_D = const.} = \frac{W}{L} C_i \cdot \mu \cdot V_D \tag{6}$$

With equation 6, the mobility can be determined from the slope of a V_G sweep at fixed V_D (I/V transfer characteristic, section 3.2.1).

$$\mu_{lin} = \frac{L}{W \cdot C_i \cdot V_D} \cdot g_m \tag{7}$$

Since g_m is a function of V_G, the effective field effect mobility, calculated via equation 7, in principle becomes a function of V_G as well. μ was, however, assumed earlier to be field-independent in order to solve equation 3. The unique mobility value which is commonly presented to describe the device performance is μ_{max}, the maximum of $\mu(V_G)$.

Another parameter oftentimes used to quantify OFET performance is the threshold voltage. V_{th} represents a minimum bias which needs to be applied at the gate electrode to accumulate enough charge carriers to form a conductive channel. In the linear regime, V_{th} is commonly derived from the x-axis intersect of a linear fit to I_D, although there are more sophisticated methods to extract V_{th} [45, 46, 47, 48]. With respect

to the original physical basis of V_{th} as the onset of strong inversion [49], it has been argued that the concept is generally not well defined in disordered semiconductors [50, 51].

In the saturated regime, when $(V_G - V_{th}) < V_D$, the channel is pinched off at the drain electrode and the current is assumed not to increase any further with increasing V_D. Substitution of V_D with $(V_G - V_{th})$ in equation 4 yields the current-voltage equations in the saturated regime:

$$I_{D,sat.} = \frac{W}{2L} C_i \cdot \mu \left(V_G - V_{th}\right)^2 \tag{8}$$

Similar to the case of linear operation, the field effect mobility can be calculated from equation 8. Because of the quadratic dependency on V_G, the square root must be applied:

$$g_{m,sat} = \left(\frac{\partial \sqrt{I_D}}{\partial V_G} \bigg|_{V_D = const.} \right)^2 = \frac{W}{2L} C_i \cdot \mu$$

to what could be called a *"saturated transconductance"*. The saturated mobility can now be derived from a linear fit to $\sqrt{I_D}$ versus V_G [52]:

$$\mu_{sat} = \frac{2L}{W \cdot C_i} \cdot g_{m,sat} \tag{9}$$

In analogy to the linear case, the x-axis intercept of this fit is commonly taken for the saturated threshold voltage.

In figure 4, ideal I/V curves are plotted, using equation 4 and 8.

2.2.2.2 *Transfer Line Method*

One of the decisive shortcomings of the MOSFET model for a general applicability to OFETs is, that it does not account for a voltage drop across the interface between a conductive electrode and the semiconductor. The transfer line method (TLM) is a fairly simple approach to differ between the resistance in the transistor channel, and the contact resistance. Originally, the TLM was introduced in 1964 by Goetzberger and Scarlett [53] and applied for the modeling of amorphous silicon TFT in 1992 by Luan and Neudeck [54]. The concept was transferred to OFETs by Klauk et al. [55] and Necliudov et al. [56] in 2003. It is based on the channel resistance being correlated linearly with the channel length, while the contact resistance is independent from it. Hence, the total resistance between source and drain is linearly correlated to the channel length, with the contact resistance as an offset. This idea implies, that neither the contact resistance nor the mobility depend on the electrical field. Furthermore, device operation must be in the linear regime.

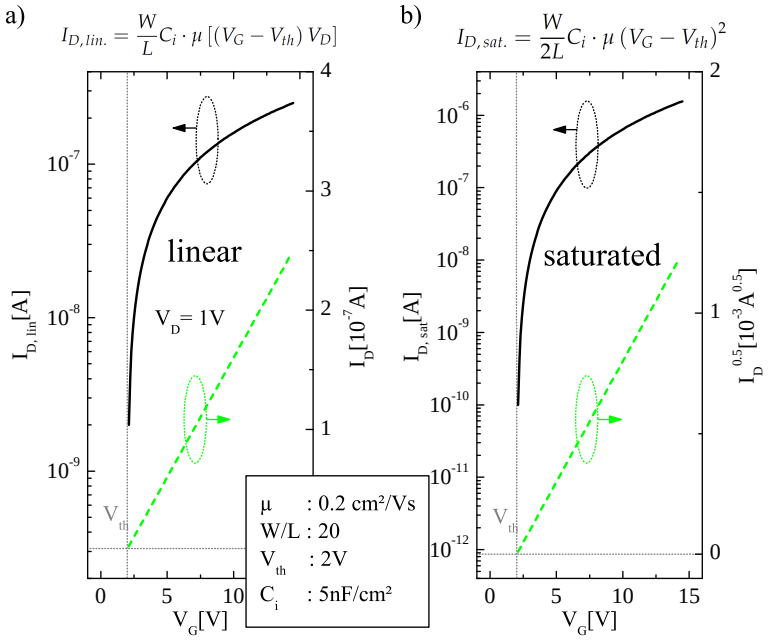


Figure 4: Idealized MOSFET behavior in the linear (a) and saturated (b) regime. Exemplary device parameters which were used for the model are shown in the black frame.

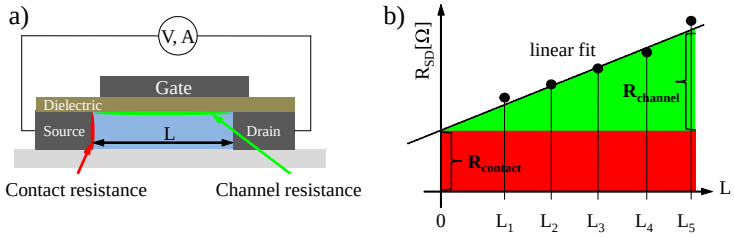


Figure 5: Working priciple of the Transfer Line Method. (a) Illustration of contact and channel resistance at a schematic OFET cross section; (b) representation of the dependency of contact and channel resistance on the channel length.

In order to apply the TLM, multiple transistors with different channel lengths, but otherwise identical architecture, need to be characterized. The concept is illustrated schematically in figure 5.

With a linear fit to the total resistance versus channel length, contact and channel resistance can be derived from the y-axis intersect and slope, respectively:

$$x(y) = a + (b \cdot y)$$

$$a = R_{cont.} \quad ; \quad b = \frac{R_{chan.}}{L} = \rho_{chan.}$$

In this form, b yields a resistivity, i.e. the channel resistance normalized by the distance between source and drain. Contact resistances presented in this thesis are multiplied by the channel width, in order to normalize them to a distance as well. Units for contact and channel resistance are therefore $[\Omega \cdot \mathrm{cm}]$ and $[\Omega / \mathrm{cm}]$. Although not thoroughly consistent, this is a common [52] representation to help the general comparability of devices with different channel widths.

As motivated in the former section, a contact resistances does not only compromise the device performance. It can also distort the evaluation via the basic MOSFET theory, because the actual electrical field in the channel is reduced against the applied external field at the contacts. Figure 6c shows the lumped element representation of series resistances at the source- and drain contacts, which lead to reduced effective voltages within the device. If the voltage drop across the electrode/semiconductor interface is known, the reduced electrical field in the channel can be accounted for, and the calculated mobility can be corrected accord-

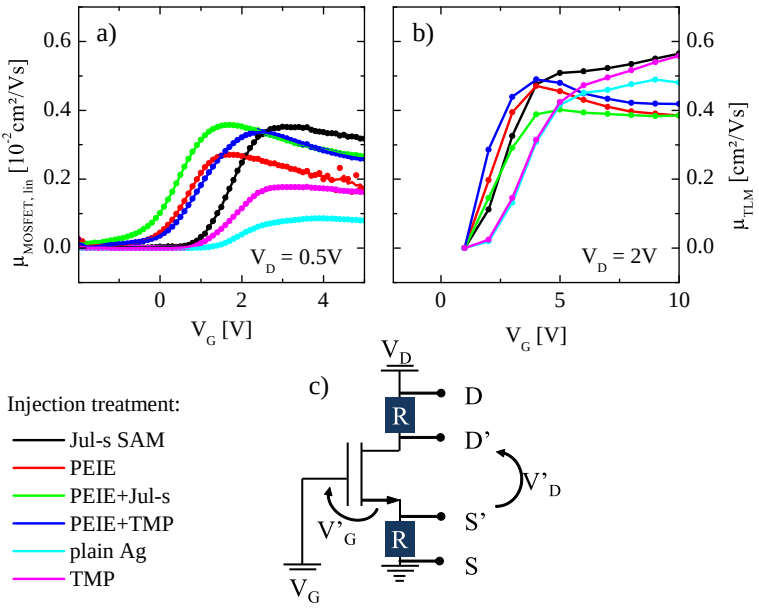


Figure 6: Example for TLM corrected mobility. Field effect mobilities of a set of OFETs with different injection treatments are determined via the MOSFET theory (a) and using TLM (b).

ingly. Using the inverse of the conductance (equation 5) for the channel resistance:

$$R_{chan} = g_d^{-1} = \frac{L}{W \cdot C_i \cdot \mu \cdot (V_G - V_{th})},$$

the corrected mobility and threshold voltage can be extracted from the derivative of R_{chan} against L [52]:

$$\frac{\partial R_{chan}}{\partial L} = \frac{1}{\mu \cdot C_i \cdot W \cdot (V_G - V_{th})}$$

An example for the corrected mobility is given in figure 6. In this figure, field effect mobilities of OFETs with different injection layers[9] are presented. In principle, the injection layer treatment is supposed to affect only the contact resistance, but leave the semiconductor in the channel and its mobility unchanged. It is clear from the direct comparison in

9 For details on injection layers in OFETs see section 2.3.3.

figure 6 that the TLM is, in this case, better suitable to extract the field effect mobility. The variance of the mobility as a function of V_G is significantly smaller for the TLM evaluation, which means that the mistaken correlation between injection properties and the conductive channel is successfully disjoint. Secondly, the absolute maximum mobility calculated via TLM for this specific semiconductor[10] agrees with literature [57], while the MOSFET-calculated value is by two orders of magnitude too low.

2.2.2.3 *More sophisticated modeling using the differential method*

While the TLM allows for a differentiation between contact and channel resistance, multiple devices must be characterized to apply the TLM, and the requirements on channel length precision are high. This can be an issue with printed electrodes. Also, from the modeling point of view, the TLM still implies the mobility to be independent of the field. With the variable-range-hopping model for charge transport in disordered semiconductors [35], the mobility can be generally described with a power-law dependence on the gate voltage:

$$\mu = \mu_0 \cdot (V_G - V_{th})^{\gamma}$$

There is a modeling approach by Natali et al. [58] that includes this power-law dependence, as well as the contact resistances. With some mathematical finesse all relevant device parameters, the contact- and channel resistances, as well as γ, μ_0 and V_{th} can be derived from the curvature of the transconductance in both, the linear and saturated regime from a single transistor, with the so called *differential method* [58]. Although this seems to be the most utile method to extract device parameters, the practical realization was found to be challenging. Unfortunately, the derived parameters exhibit such a high sensitivity on certain fitting parameters (selection of data points to include within the fit), that the results are in most cases not very reliable.

2.2.2.4 *Model comparison*

In conclusion, it can be said that the correct model to use for OFETs depends on the specific device. If the performance is dominated by injection properties, the MOSFET model alone performs poorly and the TLM poses a viable alternative, as presented in figure 6. For devices with small contact resistance, low semiconductor performance, high variance or high leakage currents on the other hand, the TLM can yield unreliable

10 N2200 (Polyera, ActiveInk).

results, or no results at all. In that case it is oftentimes better to use the classical MOSFET model and compare characteristic parameters which have less physical meaning, but can be extracted in a reliable way. The differential method represents the most sophisticated way to determine device characteristics of the ones presented here, but it could be adopted only for devices with highest performance and lowest noise.

2.3 SELF-ASSEMBLED MONOLAYERS

Ordered monolayers from small organic molecules represent a technologically important material-class in surface science. Although having a thickness of only one molecule, they can cover macroscopic lateral dimensions of a surface and alter its properties drastically. A multitude of possible applications for ordered monolayers arise from the wide range of functional groups of the small molecules, which define the chemical composition at the resulting surface. The deposition of such monolayers experienced a significant simplification with the introduction of self-assembly from solution by Nuzzo and Allara [59] in 1983. Solution deposited self-assembled monolayers (SAM) are widely used in organic electronics today, and one of the main subjects of this thesis.

2.3.1 *Structure and composition*

Small molecules for SAM formation consist in principle of three components: binding-, tail- and functional unit, as illustrated in figure 7a.

BINDING- (also called anchor- or linker-) groups can react to a specific counterpart at a suitable surface and induce a covalent bond with the small molecule. This reaction is selective in the sense that only one material class of surfaces is susceptible for a given binding group. The most studied material systems include phosphonic and carboxylic acids for oxidic surfaces, chlorosilanes for silicon and organosulfur components to bind on metal surfaces (chemical structures presented in figure 7b). Depending on the reactivity of the binding group and the stability of the resulting bond, deposition procedure and final layer properties can differ significantly. SAM preparation with phosphonic- and carboxylic- anchor groups typically include a heating step to bind and thoroughly immobilize the molecules on the surface. Organosulfur components on the other hand, are reactive enough to connect with metal

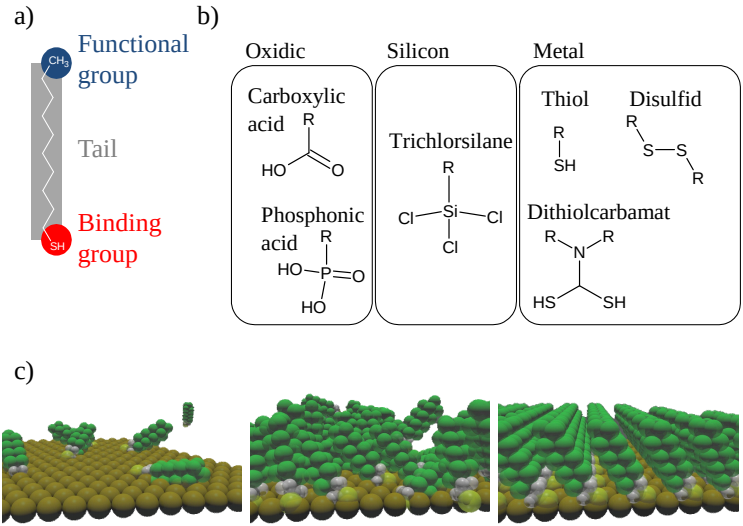


Figure 7: SAM binding mechanism. (a) Basic structure of small molecules for SAM formation; (b) the most common binding groups for different surface materials; (c) SAM accumulation sequence: nucleation, aggregation, orientation.

surfaces without external stimulus[11]. The resulting sulfur-metal bond is comparably weak and enables lateral displacement [60, 61, 62] of the bound molecules on the surface. While this facilitates post-accumulation reorganization and film formation, it renders sulfur-metal SAMs generally less stable, and also allows post-accumulation desorption of individual molecules from the completed monolayer. In the present work, organosulfur components for deposition on metal surfaces are presented.

FUNCTIONAL- (also called terminal- or head-) groups are exposed towards the adjacent layer and define the chemical composition at the SAM surface. Possible functionalities include surface wettability, chemical inertness, or interface dipoles. SAMs presented in this thesis are of the latter kind and applied to alter injection properties at interfaces between metal and semiconductor. A distinction of the functional group to the other components is not always clear-cut. Even if three different units can be distinctly distinguished within the chemical structure, they generally all contribute to the total functionality, for example the electric dipole across the molecular axis.

TAIL- (also called spacer-) groups separate the head- from the functional group. They define the molecule's rigidity and play a crucial role in the ordering process. With alkanethiols on gold, presumably the most intensely studied SAM system, it has been shown that the alkyl chains affinity towards each other cause the molecules to align parallel as an upright oriented layer [60]. But there are also rigid small molecules for SAM formation which undergo an orientation process that takes days, or even weeks [63]. The layer thickness of a SAM is determined from the length of the tail group and charge carriers generally cross the SAM via tunneling, unless π-conjugated systems are implemented within the tail [64, 65, 66, 67, 68]. Therefore, the tail plays an important role in the electrical properties of the final monolayer.

2.3.2 *Accumulation, growth and assembly*

Although formation of SAMs depends critically on the specific material system (substrate, anchor, tail, solvent), three characteristic growth phases are typically differentiated [69, 62]: island nucleation [70, 71], aggregation [72, 73, 74] and molecular orientation [75, 60, 76]. The following refinement of this classification is valid for the growth of alkanethiols, and cannot be transferred readily to all SAM systems. Many of

11 On the downside thiol-groups, as the most common sulfur-anchor, can react with oxygen under ambient conditions and must be stored under controlled atmosphere prior to deposition.

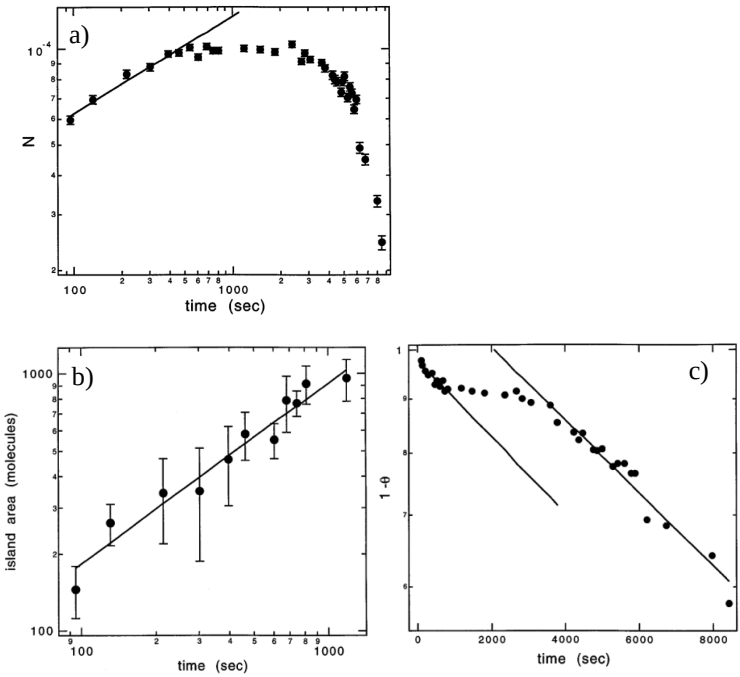


Figure 8: Nucleation and island growth behavior of SAMs. (a) Number density (normalized by the molecular area of $0.25\,nm^2$) of islands against immersion time; (b) individual island size against immersion time; (c) fraction of covered surface against immersion time. Graphics from Doudevski et al. [70].

the general concepts about SAM formation, however, are derived using alkanethiol as a model system.

The *nucleation* of single molecules is governed by the collision rate with the surface. The area density of nucleation sites can be described well with a power-law dependency while the total surface coverage is low [70, 71] (figure 8a).

In the *aggregation* regime, accumulation of molecules can be described with Langmuir isotherm behavior depending on adsorption at uncovered and resorption from covered surface [72, 73]:

$$\frac{d\theta}{dt} = k_a\,(1-\theta)\cdot c - k_d\cdot\theta$$

(covered surface fraction θ; alkanethiol concentration c; association and dissociation constants k_a and k_d). Because of the lateral mobility, adsorbed molecules agglomerate to islands, which become less mobile as they grow. In the aggregation regime, the nucleation rate goes down with increasing island size (figure 8b), and the area fraction which is covered by SAM rises. As a result, the area density of islands saturates and finally decreases when islands fuse together to form a closed layer that covers all the substrate. The different regimes of nucleation and aggregation in the growth process are visible from the slope of the surface coverage against immersion time in figure 8c.

The *orientation* of alkanethiols along each other and alignment with the surface normal, has been described by Poirier and Pylant [60] as a self-assembled phase-transition from a low density *lying down-* to a high density *upright* phase. The alignment is driven by the energetically favorable inter-chain packing over chain-surface interactions. The timescale on which this orientation takes place remains unclear. Experimental preparation usually includes immersion in solution for several hours, however, molecular dynamics simulations by Ahn et al. [76] predict horizontal orientation to assemble from initially lying down alkanethiol islands within tens of nanoseconds.

2.3.3 *Application of SAMs for injection barrier reduction*

The minimum energy which is necessary to free an electron from a metals Fermi energy (E_F) is called the work function (WF). At a metal-semiconductor contact, the energetic misalignment between the WF and the LUMO (HOMO) of the semiconductor, called *Schottky barrier*, determines a rectifying barrier for the injection of electrons (holes). In section 2.2 the performance limiting effect of such contact resistances in electrical devices is described. In figure 9a, the energetic situation at the interface is illustrated schematically[12]. In the case of established crystalline semiconductors this injection barrier is closed on the semiconductor side of the interface via highly controlled introduction of dopants, creating an *ohmic contact*. Unfortunately, this approach cannot be transferred to organic semiconductors.

Instead, SAMs can be used to alter the metals WF and narrow the energetic barrier, and with it the contact resistance [78, 77]. This is achieved via a static electric dipole along the molecular axis. Due to

12 Figure 9 shows a simplified scheme to illustrate the origin of the contact resistance at a metal-semiconductor interface qualitatively. Contact effects like energy level pinning, band bending or interface dipoles are disregarded intentionally, although they are important for the total height of the resulting injection barrier.

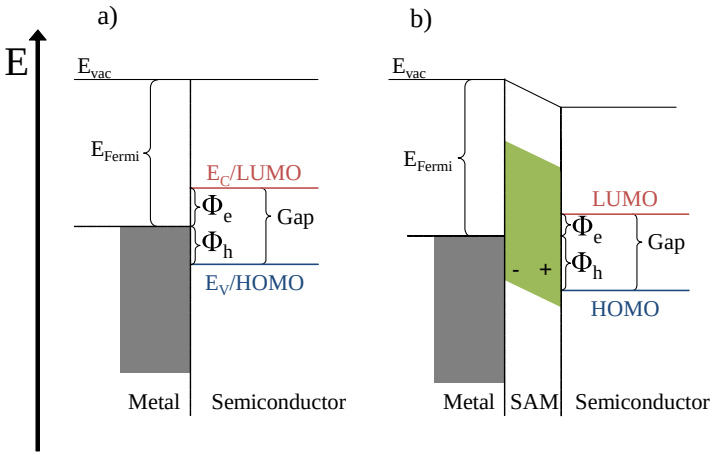


Figure 9: Schematic illustration of the injection barrier at the metal-semiconductor interface. (a) Original energetic alignament. Schottky barrier between the E_F and the E_C/LUMO for electrons (Φ_e) and E_V/HOMO for holes (Φ_h); (b) Energetic alignment after introduction of a SAM dipole layer, in this example for a reduced electron injection barrier Φ_e. Graphics redrawn after [77].

the orientation of molecules with respect to the surface in the monolayer, the dipoles align and create a potential difference from the metal to the surface, shown in figure 9b. Depending on the direction of the electric dipole, the WF can be shifted towards higher or lower values.

3 MATERIALS AND METHOD

In this chapter an overview of the preparation and characterization of thin films and devices in this thesis is presented.

3.1 SAMPLE PREPARATION

3.1.1 *Thin film deposition*

Electronic effects that can be exploited in optoelectronic or logic devices are mostly taking place at the interface to another material. Creating interfaces of thin films is a simple way to maximize the ratio of the active area to the total volume in a device. A typical film thickness for active layers in organic electronics is in the order of 100 nm, while the lateral extent can be on the order of cm or even bigger. Layers of these extreme dimensions can be fabricated most conveniently as a coating on top of a well defined substrate surface. In the following, methods which are commonly used in thin film technology, and are applied for sample preparation in the present work, are introduced briefly.

THERMAL EVAPORATION describes the thermally driven transition of a material into the gas phase and can be used for physical vapor deposition of homogenous thin layers by condensation on a suitable substrate. Materials that can be deposited in this way include metals, inorganic oxides and small organic molecules, as long as they evaporate before they decompose. In an adequately low pressure atmosphere the propagation of thermally evaporated particles can be assumed strictly ballistic, enabling lateral structuring of the deposited film by covering parts of the surface with a shadow mask. The resulting thin film depends not only on the properties and composition of the evaporated material and the employed substrate, but as well on a variety of process parameters like evaporation rate, substrate temperature or the pressure and composition of the residual atmosphere.

The film thickness can be monitored with a simultaneously coated oscillating quartz, due to its linear change in characteristic frequency with the deposited mass. A schematic illustration of a setup for thin film preparation via thermal evaporation is presented in figure 10. For the samples investigated in this work, thermal evaporation is used to

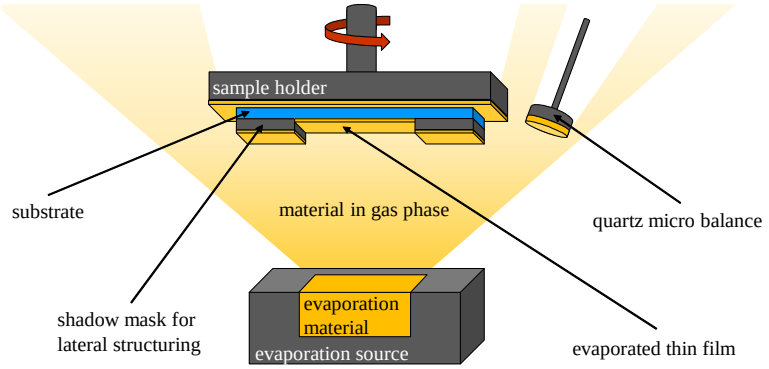


Figure 10: Schematic illustration of the setup used for thermal evaporation.

deposit structured metal electrodes. A more detailed description of thermal evaporation, along with other physical vapor deposition techniques has been summarized by John E. Mahan [79].

SPIN COATING is a comparably simple and versatile coating technique to reproducibly deposit homogenous thin layers from solution. It capitalizes on a general tendency of fluids towards uniformity under centrifugation, effectively compensating initially irregular fluid distributions [80]. In contrast to thermal evaporation, thin films of polymer materials can be deposited via spin coating without being decomposed. The only requirement on a material to be deposited, is sufficient solubility in a suitable solvent. Despite the fact that complex fluid dynamic modeling is necessary to describe the spin coating process accurately [81], a qualitative understanding can be given in a simple scheme as is shown in figure 11. First, the substrate gets completely covered with a solution containing the material which is to be casted (figure 11a). Upon well defined rotation, i.e., controlled angular acceleration and velocity, the solution is accelerated towards the edges of the substrate and jetted off until only a thin, wet film remains (figure 11b). At this point one downside of the spin coating deposition technique becomes obvious: The vast majority of used material is actually jetted off the substrate, making the process fairly wasteful material-wise. The residual solvent in the wet film is subsequently removed, typically thermally evaporated on a regulated hot plate (figure 11c). The thermal annealing parameters can have an important influence on the properties of the resulting thin film (fig-

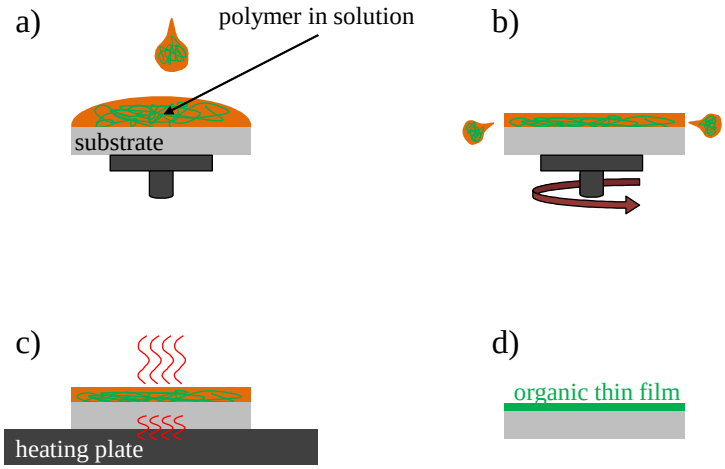


Figure 11: Schematic illustration of thin film deposition via spin coating. (a) Initial coverage of the substrate with the material in solution; (b) substrate rotation causing a flattening of the film and jetting off excessive material and solvent; (c) thermal evaporation of residual solvent; (d) resulting thin film.

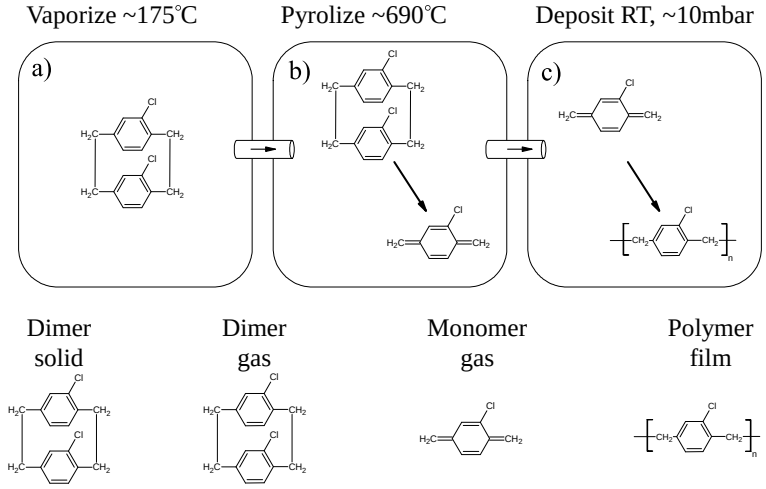


Figure 12: Schematic illustration of thin film deposition via chemical vapor deposition at the example of ParyleneC. (a) Vaporization of the solid dimer into the gas phase; (b) *cracking* of the dimer into a reactive monomer; (c) polymerization from the gas phase monomers onto the substrate.

ure 11d), for example due to thermally driven morphology changes or catalyzed chemical reactions.

CHEMICAL VAPOR DEPOSITION is a technique to deposit layers from precursors in the gas phase which react and/or decompose chemically on a specific surface. In the semiconductor industry, chemical vapor deposition (CVD) is widely used to deposit polycrystalline silicon, silicon dioxide, silicon nitride and other layers with precisely controlled properties. In contrast to physical vapor deposition, the deposit material does not propagate unperturbed through a vacuum atmosphere, but is instead transported with a gas flow. Therefore the possibilities for lateral structuring of the deposited layer via CVD are limited. On the other hand, it yields very homogenous and conformal layer growth.

In this work the deposition via CVD is used to fabricate dielectric and encapsulation layers of poly(chloro-p-xylylene) (ParyleneC). A scheme of the coating process applied for ParyleneC deposition is presented in figure 12. The setup used for deposition is a commercially available PDS2010 coating System by SCS (Specialty Coating Systems, IN, USA).

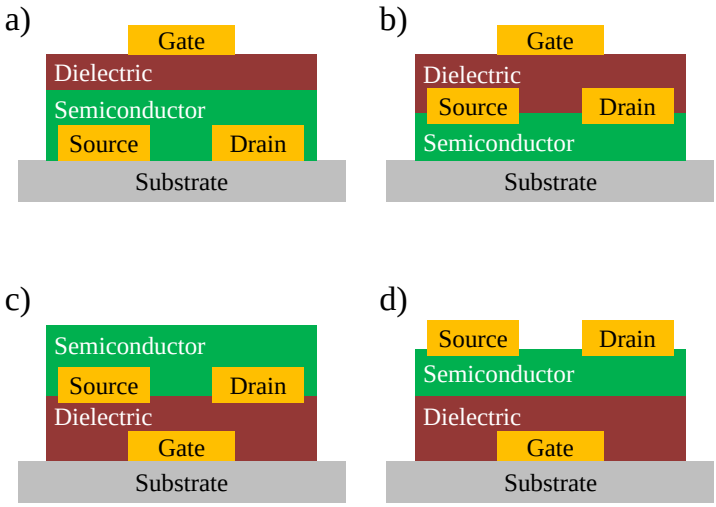


Figure 13: Principle OFET architectures. (a) Bottom contact top gate (BCTG); (b) Top contact top gate (TCTG); (c) Bottom contact bottom gate (BCBG); (d) Bottom gate top contact (BGTC).

3.1.2 *OFET architectures*

Depending on the position with respect to the active layer and the substrate, all electrodes in an FET are commonly categorized as *top* or *bottom*. In figure 13 the four principle differentiations (bottom contact top gate (BCTG), top contact top gate (TCTG), bottom contact bottom gate (BCBG) and bottom gate top contact (BGTC)) resulting from this classification are schematically illustrated. Depending on the material system, the applied architecture can play a decisive role in the device performance. One aspect of this shows at interfaces between a metal and an organic semiconductor: While this interface in the case of a semiconductor processed on top of a metal layer is generally flat and smooth, evaporating a metal electrode on top of an organic layer can cause metal atoms to penetrate into the organic layer and create mixed interfaces. These two configurations can, depending on the specific material combination, differ significantly in their charge injection properties. Another key role plays the arrangement of the contacts with respect to the dielectric layer. If there is no direct interface between those but instead a closed layer of semiconductor separating them, as is the case in figure 13a,d, the architecture is commonly referred to as *staggered*. The arrangement with

a joint interface of metal and semiconductor (figure 13b,c) is denoted as *coplanar* configuration. The electrical field distribution differs between staggered and coplanar configuration, influencing the resulting contact resistance. A more detailed study on the influence of the architecture on OFET device performance can be found in Gruber et al. [82]. The majority of OFETs in this work are prepared in bottom contact top gate configuration.

3.1.3 *Electrodes*

There are three basic electrodes in a field effect transistor: source, drain and gate[1]. The gate electrode underlies comparably little requirements besides sufficient conductivity. Throughout this work top gate electrodes consist mostly of thermally evaporated Ag, laterally structured with a shadow mask. Bottom gates are either prepared the same way or provided by a heavily doped conductive silicon substrate. The properties of source-drain contacts, in contrast, play a crucial roll in the resulting devices performance. Contacts used in OFETs investigated in this work are prepared from either Au, Ag, or in rare cases Al. The relative position of E_F of the contacts to the energy level of the destined molecular orbital in the semiconductor yields an inevitable series resistance in the device, the so called contact resistance. Commonly used metal contacts Au and Ag differ nominally by 0.8 eV in ionization energy, already causing a difference of one order of magnitude or more in the contact resistance. Contact exposition towards ambient atmosphere, lithography structuring, common electrode treatments with a solvent or plasma for cleaning, anything that causes adsorbates or reactions on the surface, can have a decisive influence on the resulting device's performance. As an example for contact sensitivity, p-type OFETs with thermally evaporated Ag contacts which were exposed to ambient air before semiconductor deposition for durations between 10 min and 2 h are presented in figure 14. Due to the fact that Ag surfaces work function rises upon oxidation, the performance of the OFETs is hereby not decreased upon electrode oxidation, but instead increased as the injection barrier is reduced.

3.1.4 *Semiconductors*

The semiconductor is often referred to as the *active layer* of a transistor. It switches from insulating to conductive behavior, when charge carri-

1 The gate is in some cases actually realized by two oppositely arranged electrodes, in order to optimize the distribution of the electrical field between them.

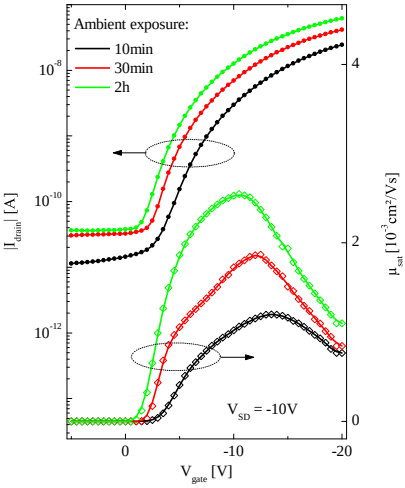


Figure 14: p-type OFETs with Ag contacts. Oxidation of the contacts was carried out by exposure to ambient atmosphere.

ers dopants are introduced. Charge carrier mobilities $\mu > 10\,cm^2/Vs$, a performance benchmark for organic semiconductors to become viable in current driven flexible OLED displays backplanes, have been reached with solution processable polymers [83]. It has been argued, however, that the methods of extracting the mobility not always reflect the true current driving capabilities if they are applied to devices with non-ideal I/V characteristic [9]. Although the development of high mobility organic semiconductors is a positive driving force in material design, reducing the complete electrical performance to a scalar number is generally an oversimplification.

All semiconductor layers in the present thesis are prepared by spin coating from chlorobenzene with 1000 rpm for 60 s. The concentration was adjusted between $6-10$ mg/ml to yield a film thickness of (80 ± 10) nm[2]. A survey over the chemical structures of polymers that are used in this work is presented in figure 15. Some semiconductors presented in this thesis were synthesized at the Institute of Organic Chemistry at the University of Heidelberg. Their chemical structures are presented in sections 4.3 and 6, along with their characterization.

2 Determined via profilometry.

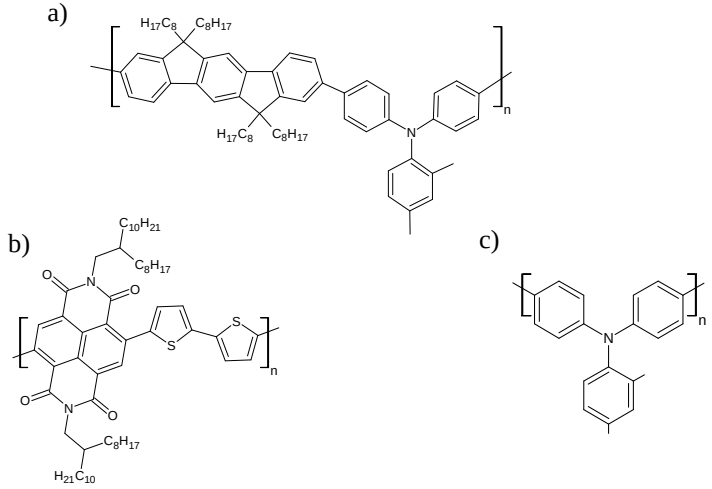


Figure 15: Chemical structures of polymeric semiconductors. (a) PIF8-TAA; (b) N2200(Polyera ActiveInk); (c) PTAA.

Comprehensive material surveys about progress and development of organic semiconductors for OFETs can be found in Mei et al. [29], Nielsen et al. [28], Holliday et al. [10].

3.1.5 *Gate dielectrics*

Despite the seemingly unspectacular job to insulate the gate electrode against the semiconductor, reliable high performing dielectric layers pose a major challenge in OFET development. The requirements on dielectrics for realistic applications are not only of electrical nature, but mechanical and chemical as well. To facilitate organic electronics main selling points, they need to be flexible and solution processable at temperatures compatible with polymer substrates ($< 200\,^{\circ}C$). Since the field effect mobility of organic semiconductors is typically orders of magnitude lower than that of their inorganic[3] counterparts, a dielectric with identical conductivity causes an accordingly higher leaking current at the gate electrode. For the design of integrated circuits from OFETs, the presence of such leakage currents has to be included within modeling approaches [84]. Additionally, as the OFET's conductive channel is located at the interface of semiconductor and dielectric layer, the chemical properties of the

3 Single crystalline Silicon

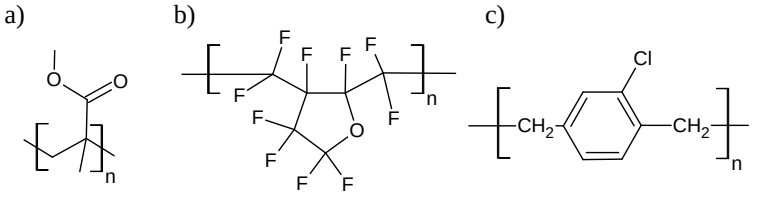


Figure 16: Chemical structures of dielectric polymers. (a) PMMA; (b) Cytop; (c) ParyleneC.

dielectrics surface are crucial. Not only for the resulting performance due to possible surface dipoles or trap sites, but in bottom gated devices for its applicability as a printing substrate, too. In figure 16a survey of all polymer dielectrics which are used in the present work is given. Furthermore SiO_2 dielectric layers are investigated, thermally grown on single-crystalline Si wafers.

ParyleneC dielectric layers in this work are fabricated using CVD and exhibit a thickness between 250 nm and 350 nm[4]. Cytop[5] dielectrics are fabricated using spin coating at 3000 rpm for 60 s and exhibit a film thickness of (650 ± 10) nm. PMMA was spin coated from solution in methyl-ethyl-ketone and exhibit a layer thickness of (40 ± 5) nm. PMMA was used in a bilayer dielectric as an adhesion promotion layer for subsequently deposited ParyleneC.

Comprehensive reviews on gate dielectric materials for OFETs are given by Veres et al. [85] and Facchetti et al. [86].

A complete overview about the material systems that are applied for transistors in this thesis is presented in table 1.

3.2 CHARACTERIZATION

3.2.1 *Electrical device characterization*

Device characterization is carried out under ambient conditions using an Agilent 4155C Semiconductor Parameter Analyzer (Agilent Technologies, CA, USA). A 3 probe setup is applied, using independent source/measure unit (SMU)s for the drain-, the source- and the gate-electrode respec-

4 Determined via profilometry.

5 Cytop solution (CTL-809M) was purchased from Asahi Glass with a concentration of 9 *wt.*% and used as received.

	Electrodes			Semiconductor				Dielectric				Injection layer			
Figure	Au	Ag	Ag print	N2200	Pif8	PTAA	other	ParC	Cytop	PMMA	SiO_2	PFDT	Juls	PEIE	PFBT
6		x		x				x					x	x	x
14		x				x		x							
17		x				x			x			x			
21	x				x			x				x			
29	x			x				x					x		
30			x	x				x					x		
31		x		x				x					x	x	
32	x					x		x				x			
33		x					x		x					x	
34		x					x		x					x	
35	x						x	x		x			x		
37	x					x		x			x				x
38	x					x		x			x				x
39	x					x		x			x				x
40	x					x		x			x				x
41	x					x		x			x				x
42	x					x		x			x				x
45	x						x	x							
47	x						x	x							
48	x						x	x							
49	x						x	x							

Table 1: Assignment of materials used in OFETs presented in this work.

tively. Each SMU can precisely force current or voltage and measure both of them simultaneously. In all measurements presented in this thesis, the voltage is set as the forced parameter, and the current is the measured variable.

There are two common I/V measurement setups for transistor device characterization, called *output-* and *transfer*-characteristic. In both cases, the source-contact is set at ground potential.

Output characteristic

For the output I/V-characteristic, the gate-electrode is fixed at a constant potential during a voltage sweep at the drain-contact. Typically, multiple sweeps at different constant gate-voltages are applied and the measured drain-current is plotted in linear scale against the applied drain-voltage. The output-characteristic can be divided into *linear* and *saturated* operation regimes from the shape of the I/V curve. The points of transition between linear and saturated regime operation of multiple gate-voltage sweeps, can be fitted in an upward curving parabola. An exemplary I/V curve is presented in figure 17a. In *bipolar junction transistors* the output characteristic can be used to determine the *Early voltage* [87]. In the research field of organic electronics, an important information most commonly extracted from output I/V curve is a quantitative measure of the contact resistance.

Transfer characteristic

For the transfer I/V-characteristic, the drain-electrode is fixed at a constant potential during a voltage sweep at the gate-contact, reverse to the output-characteristic described above. According to the MOSFET model, important performance parameters can be extracted from the transfer characteristic, including the *field effect mobility* μ and the *threshold voltage* V_{th}, as is explained in more detail in section 2.2.2.1. For performance parameter extraction, the transfer-characteristic is generally preferred over the output-characteristic throughout this work. This is a common approach for OFETs, as the transfer characteristic enables for a more precise and quantitative performance evaluation.

Graphical transfer characteristic representation

The representation which is most common for transfer I/V characteristics exhibits $|I_D|$ in dependency of the gate-voltage on a logarithmic and $|I_D|^{1/2}$ on a linear scale at two individual y-axes. Figure 17b shows the example of a p-type OFET with poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine]

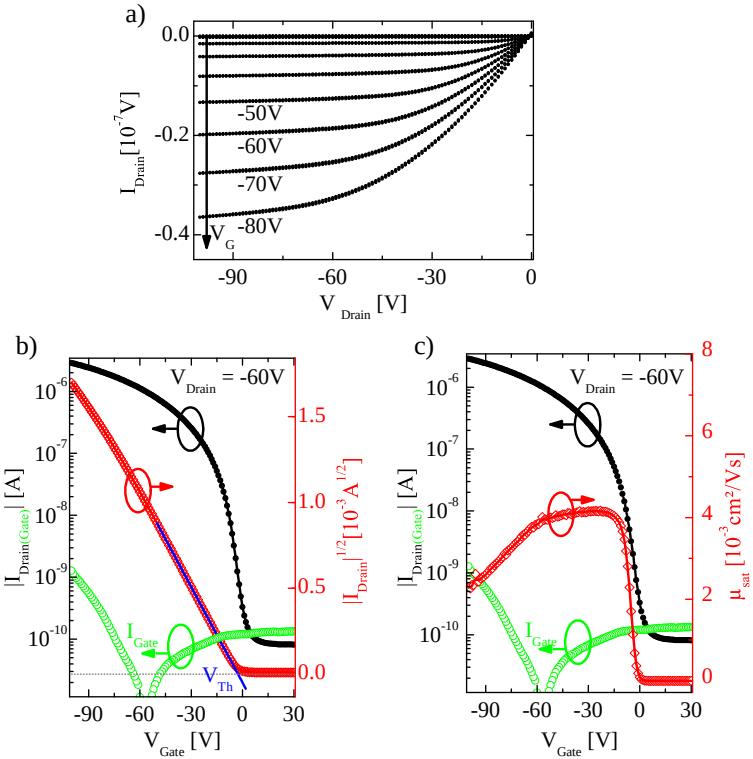


Figure 17: Expemplary p-type I/V-characteristics of an OFET. (a) Output characteristic; (b) transfer characteristic in common representation. Next to the absolute drain-current (black) in logarithmic scale, the drain-current's squareroot (red) is plotted and fitted (blue) to determine threshold voltage V_{Th} and maximum mobility μ. The current at the gate electrode is plotted on the same scale as the drain-current (green); (c) representation with gate-dependent field effect mobility on a linear scale instead of the drain-current's squareroot.

(PTAA) as the semiconductor. According to the MOSFET model V_{th} can be derived from the x-axis intercept of a linear fit to $|I_D|^{1/2}$, and is explicitly visualized in this representation[6]. An alternative representation which is in some cases throughout this thesis chosen over the traditional one is applied to the same OFET for comparison in figure 17c. Next to the usual drain-current on logarithmic scale, it exhibits the gate-dependent *effective field-effect mobility* μ on a linear scale. As μ is proportional to the *derivative* of I_D [7], it oftentimes can reveal features which are hard to identify from $|I_D|$.

The current which is leaking to the gate electrode is plotted additionally in figure 17b-c. This feature adds to the overall characterization of a single device, but is typically disregarded in favor of legibility in comparative plots of multiple transistors.

3.2.2 *Thin film characterization*

3.2.2.1 *Profilometry*

Film thicknesses of the prepared layers are determined via mechanical contact profilometry, using a DEKTAK150 Profilometer from Veeco (Veeco Instruments Incorporation, USA), if not stated otherwise. With this technique, a stylus tip rests on a sample with a mechanical force of a few milligrams, while the substrate is moved laterally beneath it. From the height profile which is recorded along the probing line across an edge from the film's surface to the substrate, the film-thickness is determined. The vertical resolution of this method is for organic layers typically dominated by the surface roughness.

3.2.2.2 *Photo-Electron Spectroscopy*

photo-electron spectroscopy (PES) is a highly sensitive characterization method in surface science which capitalizes on the quantized absorption of photons, according to the photoelectric effect, to analyze the atomic core level energies in a material. PES is widely used to investigate the chemical composition and bonding character, as well as the spectral density of states in organic semiconductors. A schematic illustration of the measurement principle is presented in figure 18. Monochromatic photons impact on the sample surface and are absorbed from electrons,

6 This is valid for device operation in the saturation regime. In the linear regime V_{th} is derived from the intercept of a linear fit to I_D, therefore I_D is typically presented in linear scale on the second axis. An inconsistency which occurs sporadically in literature, is to present $|I_D|^{1/2}$ regardless of the operation regime.

7 or respectively the derivative of $|I_D|^{1/2}$ for saturated regime operation.

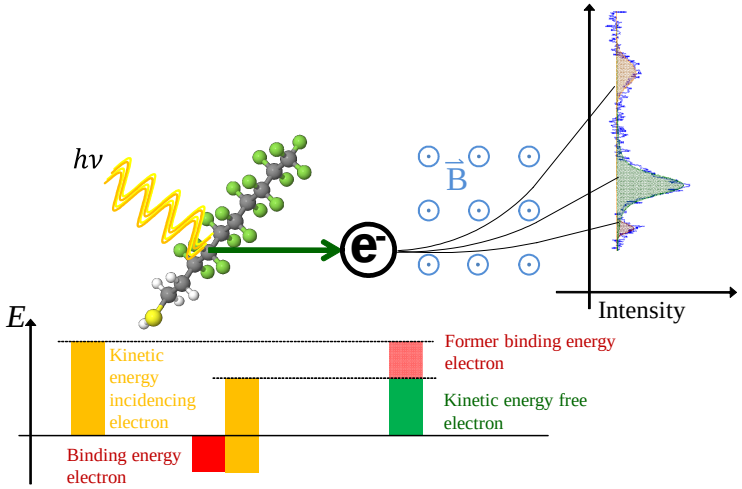


Figure 18: Schematic illustration: Photoelectron Spectroscopy

which in turn are emitted from the material if the photon energy is sufficiently high. The emitted electrons have a kinetic energy equal to the incidencing photon energy minus the former binding energy. Dispersed via a magnetic field, the spectrum of kinetic energies contains the binding energy distribution close to the sample surface.

Depending on the photon energy, PES is further specified as x-ray photo-electron spectroscopy (XPS) or ultraviolet photo-electron spectroscopy (UPS). The PES spectra presented and discussed in this work were measured and evaluated by *Janusz Schinke* and *Marc Hänsel*. Experimental details, as well as a more sophisticated description of the PES measurement technique and setup can be found in their respective dissertation and master thesis [88, 89].

3.2.2.3 *Infrared Reflection Absorption Spectroscopy*

infrared reflection absorption spectroscopy (IRRAS) is a thin film characterization technique in the infrared (IR) energy regime and therefore sensitive to intramolecular bonding-deformation excitations, including vibration, rotation and stretching-modes. IR-spectroscopy in general can be used to investigate for example the bonding configuration or the chemical composition in the bulk of a material. A schematic illustration

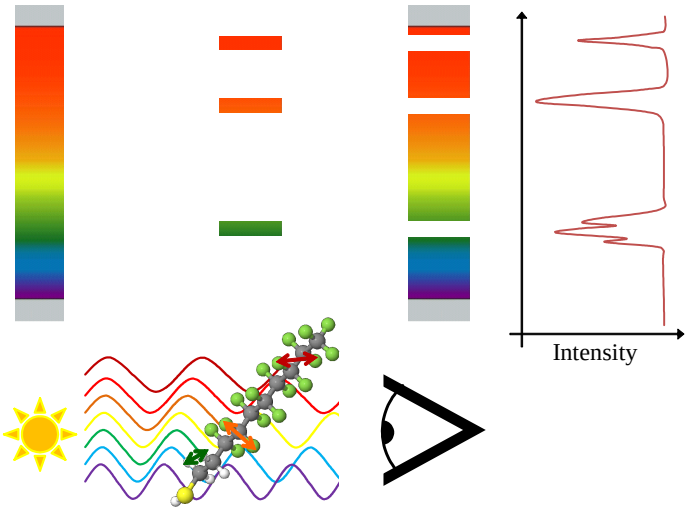


Figure 19: Schematic illustration: Infrared Reflection Absorption Spectroscopy.

of the IR-spectroscopy measurement principle is presented in figure 19. An IR-beam with continuous spectral distribution is focused on a sample which absorbs at a specific set of discrete excitation-energies. The resulting beam is missing the absorbed frequencies and exhibits intensity minima, or *peaks* in the spectrum. In IRRAS-configuration, the beam is reflected at the substrate after passing through the film, and passes it a second time in the reverse direction before being detected. As a minor benefit of this configuration, the effective film thickness is doubled, increasing the peak intensity. More importantly, the charge carriers in the reflective substrate surface are free in the lateral, but not in the vertical direction, causing a suppression of light-modes with normal polarity close to the surface, called *surface selection rule*. From the relative intensity of non-linearly oriented absorption modes, preferred molecular orientations close to the substrate surface can be determined qualitatively, and in combination with a spectrum of the amorphous phase even calculated quantitatively. All IRRAS-spectra presented in this thesis are measured and evaluated by *Sabina Hillebrandt*. A description of the experimental details, as well as a detailed derivation of the angle determination can be found in her master thesis [90].

3.2.2.4 *Wetting envelope after Owens–Wendt–Rabel–Kaelble*

The ability of a liquid to wet a solid materials surface plays an important role in solution processing, and depends in a complex way on interfacial interactions of substrate and applied solvent on a molecular level [91]. In principle, the wetting behavior of every substrate-solvent material combination needs to be characterized individually. The contact angle at the edge between substrate and liquid is an easily accessible experimental parameter for any given material combination. It can be measured via the *sessile drop technique*, basically a photo of a droplets cross section. One way to estimate a general wetting behavior of a specific surface, and roughly predict the wettability for any solvent with known properties, is the *wetting envelope* after Owens–Wendt–Rabel–Kaelble [92, 93]. Simplified, it consideres two contributions to the surface energy of a material: a polar- and a disperse fraction. Using experimentally determined contact angles of at least two known solvents, a curve in a two-axis plot of the polar and disperse surface energy fractions can be calculated: the wetting envelope. Any other known solvent with known polar and disperse fraction marks one point in the plot. If it lies within the envelope its wettability is good, and vice versa. The bigger the area of the wetting envelope of a surface, the more different solvents exhibit good wettability on it. If one surface's wetting envelope includes that of another completely, its general wettability is considered better.

3.3 PARTIALLY AUTOMATIZED EVALUATION WITH THE "EVA" ORIGIN SCRIPT

The large data volume obtained over the course of this work, and the multitude of characteristic transistor performance parameters, necessarily requires computer assisted evaluation. A significant part of this work is therefore the development of an evaluation script (*EVA*) embedded to the data analysis and graphing software Origin (OriginLab, Northampton, MA). The development of this script was done in cooperation with Arno John, PhD candidate in the group of Klaus Meerholz, University of Cologne. The script is freely accessible and additional information on the specifications and functionality, as well as the latest version can be requested from the author. The functionality includes automatized FET evaluation after the MOSFET model and TLM, and rudimentary tools for the differential method.

Part II

RESULTS AND DISCUSSION

4

CHARGE INJECTION PROPERTIES AT THE METAL-SEMICONDUCTOR INTERFACE

APPROACH

The injection of charge carriers from a conductive material into an organic semiconductor generally causes a voltage drop over the contact, and is therefore a decisive performance limiting restraint in any electrical device. Controlling and minimizing this *contact resistance* in order to optimize device performance is still one of the key challenges for the development of organic electronics technology. The size of the contact resistance depends on the relative alignment of specific energy levels on both sides of the contact. In organic electronic devices, energy level misalignment is commonly addressed by changing the WF using transition metal oxides [94, 95], polymeric dipole layers [96, 97] or SAMs. This chapter focuses on the application of solution processed SAMs in OFETs for altered injection properties. The working principle of SAM injection layers with respect to the energetic alignment at the interface is introduced in section 2.3.3 and was originally reported by Campbell et al. [78] and de Boer et al. [77].

4.1 SAM ACCUMULATION IN PRINTING-RELEVANT TIMESCALES

A decisive limitation of SAM fabrication with high throughput solution processing techniques is a time consuming immersion step which is applied to ensure optimum monolayer quality. Over the last two decades, a good understanding of the bonding mechanism, growth nucleation, initial coverage behavior and the structural properties at final equilibrium was developed, at least for the model system of alkanethiol. Despite an increasing fundamental understanding about the material class of SAMs and their positive impact on device performance, there is still a discrepancy between immersion times that are applied typically in lab scale investigations and the processing time that is realistically available in an industrial printing process. In order to estimate the optimized process speed and the actual correlation of SAM processing time to the resulting layer properties, an established, commercially available SAM forming molecule 1H,1H,2H,2H-perfluorodecanethiol (PFDT) is elected as a model system on Au [74]. PFDT exhibits a strong molecular dipole

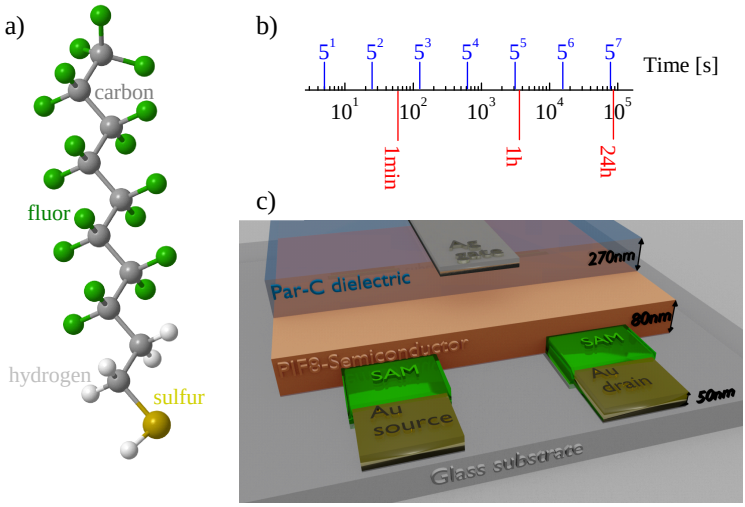


Figure 20: (a) Chemical structure of PFDT (white: hydrogen, yellow: sulfur, gray: carbon, green: fluorine); (b) overview of prepared immersion times in logarithmic scale (blue) and time markers for orientation (red); (c) schematic cross section of the BCTG OFET stack. Redrawn after [74].

and enhances the WF of a metal electrode it is applied to, supporting the injection of holes into the semiconductors HOMO. In figure 20a the chemical structure of PFDT is presented. The OFETs presented in this chapter are prepared with PIF-8-TAA semiconductor and ParyleneC dielectric. A illustration of the architecture is given in figure 20c. The performance parameter which is elected to monitor the injection functionality in these devices is the threshold voltage V_{th} (details in section 2.2.2.1). Ethanol is used as a solvent for PFDT in all experiments described here. The concentration of the precursor solution plays an important role for the pace of the SAM formation process [72]. As long as a critical *agglomeration concentration* [98] is not exceeded, the rate of SAM-molecule collisions per substrate area increases linearly with the concentration. In analogy to the *Langmuir*, the product of time and partial pressure, used as a unit for exposure in deposition from gas-phase, the parameter *exposure* is introduced here as the product of immersion time and precursor concentration.

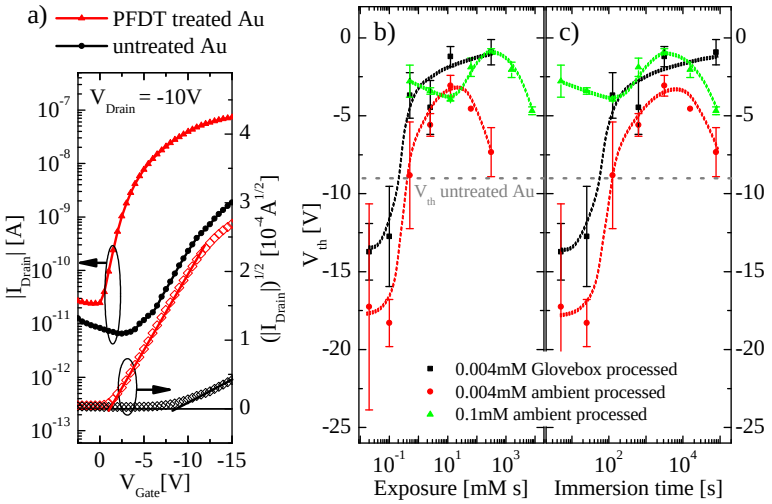


Figure 21: Transfer characteristics of OFET devices with PFDT charge injection layers. (a) I/V plot and V_{Th} of devices with and without PFDT treatment; (b) V_{Th} as function of exposure; (c) V_{Th} as function of immersion time. Lines connecting the data points are guide to the eyes. Redrawn after [74].

4.1.1 *OFET optimization with PFDT*

Three series of OFETs are prepared with varying PFDT-immersion time in seven logarithmic steps between 5 s and $\sim$ 22 h, at concentrations of 4µM and 0.1 mM. Additionally, the influence of processing in ambient atmosphere, as opposed to processing in a nitrogen-atmosphere, is investigated. The impact of a PFDT injection layer between metal and semiconductor on the transfer characteristic, and $|V_{th}|$ specifically, is demonstrated in figure 21a. Because of the shift from the oriented dipole towards higher WF, the injection barrier for holes is reduced and hence, the performance of p-type OFETs is improved. The trends of device $|V_{th}|$ as a function of contact exposure to the PFDT solution, are presented in figure 21b for three series of samples. In the regime below an exposure of 1 mM s, the injection treatment has a negative effect on the OFET and causes an increase of $|V_{th}|$, compared to the devices with untreated contacts. As the SAM coverage increases with the exposure, injection properties improve and $|V_{th}|$ is reduced until it saturates between 1 V and 2 V.

In the case of PFDT immersion in ambient conditions, however, $|V_{th}|$ reaches an optimum before it increase again for high exposure. In figure 21c the same data is plotted against the immersion time, instead of exposure. In this representation, a correlation of the functionality decrease at high exposure to the immersion time is revealed. The fact that this behavior does not occur with SAM immersion under nitrogen atmosphere, suggests a relation to ambient contaminations in the ethanol solution. Whether it is caused by a decreased effective dipole of the SAM on the surface or desorption of the molecules from the surface, possibly due to competition for bonding sites with contamination species, is out of scope for the device-based approach discussed here. The effect is addressed in detail with analytical investigations via PES in section 4.1.5.

In the short immersion regime, figure 21c shows that a significant decrease of $|V_{th}|$ to 2 V is realized, using immersion in ambient atmosphere of only five seconds with a concentration of 0.1 mM. Although this is not the highest injection barrier reduction that could be achieved with PFDT, it represents a significant improvement. While highly appreciated for high-throughput application, such short dip coating times are experimentally difficult to control for a detailed study of the SAM formation. To observe the aggregation and accumulation of SAM analytically under well-controlled experimental conditions, very low concentrations of 0.004 mM proved to be necessary for PFDT.

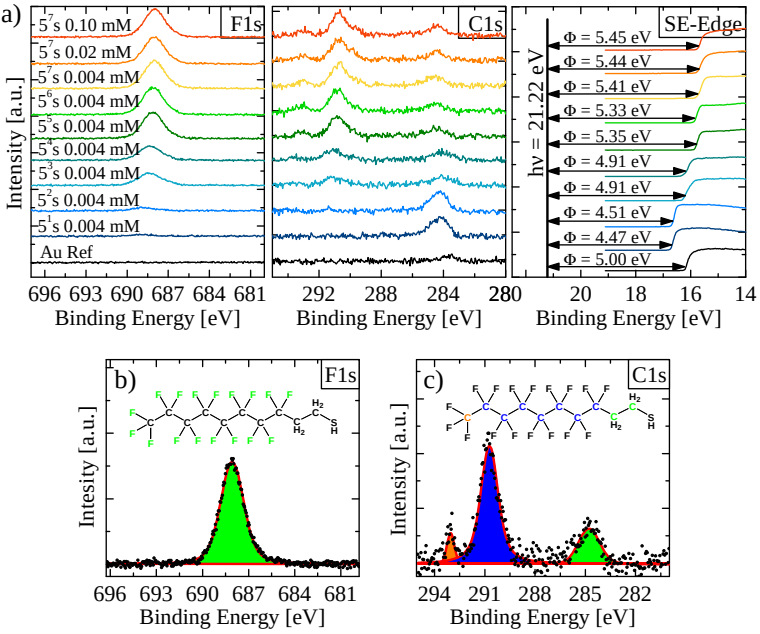


Figure 22: XPS and UPS spectra. (a) F1 s and C1 s emission and SE cutoff with and without PFDT SAM treatment, various immersion times, and different concentrations (0.004 – 0.1 mM). (b) Assignment of F1 s emission line to the molecular structure of PFDT. (c) Assignment of C1 s emission peaks to the molecular structure of PFDT. All data shown in this figure is derived from SAM prepared under N_2 atmosphere in a glovebox. (b, c): Black dots correspond to the measured spectra but with background removed. Redrawn after [74].

4.1.2 *Surface coverage, chemical surface composition and WF-shift via PES*

In order to identify the origin of the negative influence on the device performance of the SAM treatment in the regime of very low exposure, the chemical composition of the surface is investigated with PES. In figure 22 signals of the F1 s and C1 s core levels from PES measurements of PFDT SAM are presented. The increase of the F1 s peak intensity in figure 22a at the binding energy expected for PFDT (see figure 22b) illustrates the growing layer coverage with increasing exposure. From the C1 s peak-structure in figure 22a, an initial coverage with physisorbed carbon-containing adsorbates other than PFDT can be identified for very low exposure. In the nucleation regime, the surface consists of isolated

islands of accumulated PFDT, while the remaining surface is covered with these adsorbed contaminations from the ethanol solution. Because of the high WF of Au, physisorbed adsorbates generally tend to shift towards lower values, known as *pillow effect* [99, 100, 101], unless they provide a distinct oriented dipole like PFDT does. The resulting WF of the surface, as measured via the single electron (SE) cutoff energy, is superimposed from the two oppositely shifting surface coverages. Initially, the WF is shifted to lower values, dominated by the adsorbat coverage, and therefore results in an increased injection barrier in the p-type OFET devices. As the initial coverage is getting replaced successively by PFDT with increasing exposure, the WF changes in the intended direction towards higher values and leads to the observed $|V_{th}|$ -reduction. The C1 s peak structure from layers with a WF-change in the intended direction matches the assignment to the molecular structure of PFDT (see figure 22c).

4.1.3 *Angle determination via IRRAS*

The structural rearrangement of the molecules cannot be investigated from either device performance or PES measurements. Molecular absorption modes in IRRAS, in contrast, can be assigned to specific orientations with respect to the molecular axis. Due to the surface selection rule, the relative peak intensities of non-linearly aligned IR absorption modes allow for an estimation of the average molecular orientation with respect to the surface normal. A schematic illustration of this approach is given in figure 23b-c. Figure 23a displays IRRA spectra of SAM deposited with increasing exposure, along with peak position markers of orthogonal and parallel oriented modes. Generally, IRRAS is a sophisticated and challenging technique to investigate molecular monolayers reliably, due to very low absolute signal intensities from such thin layers, indicated by the scaling-arrow in figure 23a. Especially for layers in the exposure-regime below 1 mM s, where PES F1 s data suggested only little partial surface-coverage, the IR-signal intensity turned out to be too low to calculate an average orientation. The minimum exposure for which an angle could be calculated is therefore 1 mM s. All resulting average tilt angles, with respect to the surface normal are plotted against the exposure in figure 24.

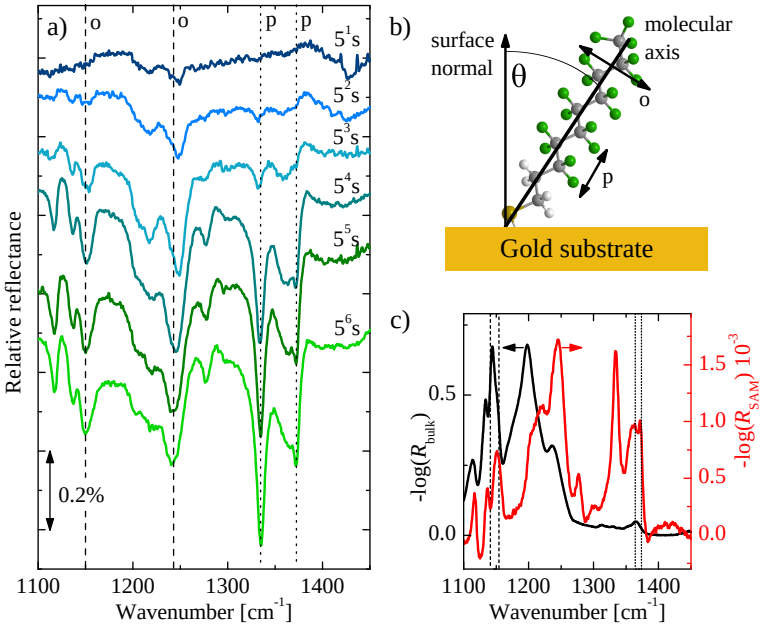


Figure 23: IRRAS data. (a) IRRA spectra of PFDT monolayers for different immersion times of the gold substrate in a 0.004 mM solution. The dotted and dashed lines mark vibrational modes with the transition dipole moment parallel (p) and orthogonal (o), respectively, to the molecular axis according to [102] and [103] (b) Schematic visualization of PFDT on the gold surface with tilt angle /theta and orientation of vibrational modes. (c) Absorbance spectra of PFDT as a SAM (measured in IRRAS geometry) and as isotropic bulk (measured in ATR geometry). The dashed and dotted lines mark the used orthogonal and parallel modes at 1150 and 1370 cm^{-1}, respectively. All data shown in this figure is derived from SAM prepared under N_2 atmosphere in a glovebox. Redrawn after [74]

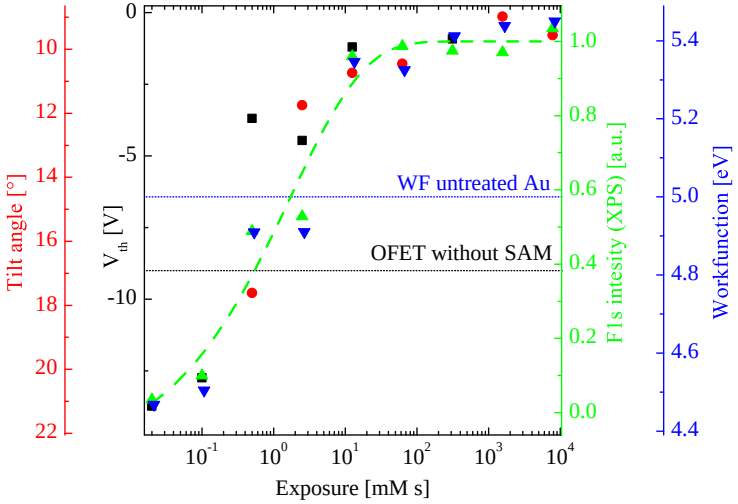


Figure 24: Compilation of measurements on the PFDT accumulation. The F1 s emission, as indicator for surface coverage, is fitted to a Langmuir isotherm adsorption behavior (dashed green line). All data shown in this figure is derived from SAMs prepared using 0.004 mM concentration under N_2 atmosphere in a glovebox. The reference values of WF and threshold voltage of untreated samples are indicated by dotted lines. Redrawn after [74].

4.1.4 *Coverage, ordering and performance*

Next to the above mentioned tilt angles from IR data, figure 24 presents the layer coverage as determined from the PES F1 s peak intensity, the WF as determined from the PES SE edge, and V_{th} of OFET devices, all plotted against the exposure. Suggested by F1 s peak intensity, the aggregation phase of molecular accumulation is finished, and the surface completely covered after $\sim$ 10 mM s. The angle to the surface normal has at this point with 10.7° almost reached its minimum value. The further orientation with the intermolecular alignment accounts only for a marginal additional erection about 1°. Additionally, the largest average angle to the surface at 1 mM s is found to be only 17.6°, a rather upright orientation, considering that this is still clearly below closed monolayer coverage. In contrast to the SAM accumulation and orientation for alkanethiols [60] (section 2.3.2), PFDT seems not to undergo an explicit "lying down phase", but is oriented surprisingly upright during the aggregation phase already. PFDT reaches almost its maximum erection with surface coverage completion[1]. It was suggested by Pellerite et al. [103] that partial fluorination can accelerate the ordering process of alkane tails in SAM accumulation. This is in accordance to the fast accumulation process which is observed here, and renders partially fluorinated alkane tails as an ideal candidate for the fabrication of hole injection layers with high throughput deposition techniques. This behavior is reflected in the OFET injection behavior, measured via $|V_{th}|$. Exposure of the contacts for 10 mM s yields the lowest $|V_{th}|$ that was achieved, also correlated to concluded surface coverage as shown in figure 24. With this insight, two different growth phases can be assigned from the trend of $|V_{th}|$ in exposure and time, presented in figure 21b-c earlier. In the aggregation regime below 10 mM s, the injection properties are governed by the fraction of SAM-covered surface and is therefore correlated to the exposure. This process can be accelerated using appropriately high concentrations, and yield injection layers with almost maximized performance very fast. The remaining difference to maximized performance, however, is associated with the final alignment of the molecules along each other, and can not be accelerated via the concentration.

1 The approach that is taken here to determine the tilt angle via IRRAS, is only sensitive to the angle with respect to the surface normal, or altitude. The respective orientation of the molecules towards each other in the azimuth angle is out of scope of this work, as it has no influence on the surface-normal fraction of the molecular dipole.

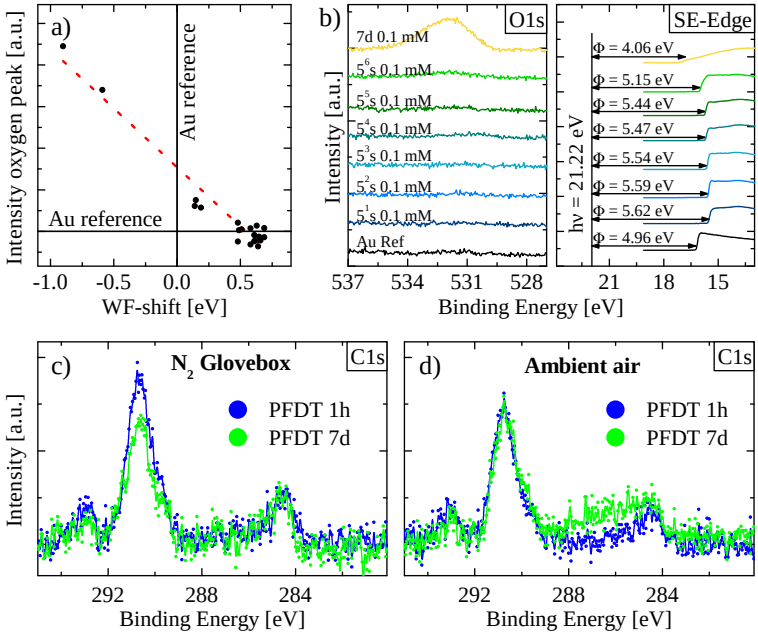


Figure 25: (a) Oxygen contamination (as measured by integrated O1 s intensity) of ambient-processed SAM against WF shift. (b) O1 s peak and respective change of the WF, measured by SE edge with PES. (c, d) C1 s signal of SAM prepared in a glovebox and under ambient condition. The dots correspond to the measured spectra but with background removed. Redrawn after [74].

4.1.5 *Influence of extensive ambient exposure*

In the regime of very long immersion time in ambient air, a time-correlated functionality decrease is observed (see figure 21), which requires an analysis of the surfaces chemical composition via PES. In figure 25a, the WF-change (as derived from the PES SE-cutoff) of several samples immersed under ambient conditions is plotted against the oxygen contamination in the according sample (derived from the integrated signal intensity of the PES O1 s peak). Clearly, there is a reverse linear correlation between the achieved change of the WF and the oxygen contamination in the PFDT layer, not only canceling out the SAM functionality, but even resulting in a strong shift of 0.9 eV in the opposite direction. Figure 25c-d displays a change in the peak structure of the C1 s signal for long time ambient processing only, suggesting a chemical reaction of the PFDT

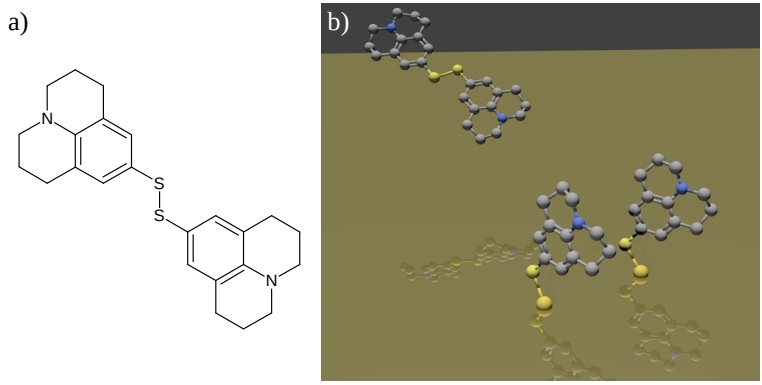


Figure 26: (a) Chemical structure of Bisjulolidyl disulfide $(Juls)_2$; (b) Schematic illustration: The Juls dimer breaks at the S−S bond and the separated monomers are attatched individually to the metal surface.

molecule with ambient oxygen. This result implies, that a commonly applied SAM immersion time of 24 h already causes a reverse WF-change in the range of 0.5 eV, canceling out the original shift completely. This is consistent with the SAM functionality loss in OFETs from exaggerated immersion time in ambient atmosphere presented above (figure 21). The negative effect is on the other hand only significant after hours of immersion, and therefore does not cause any restraints for application, since short immersion times would be preferred in an industrial fabrication anyway. It should, however, be considered for future investigations on SAM charge injection layers.

4.2 CHARACTERIZATION OF A NOVEL HIGH PERFORMANCE ELECTRON INJECTION SAM

SAM forming molecules are available with both dipole directions to promote either hole injection into the semiconductors HOMO, as was presented in section 4.1, or electron injection into the LUMO. In practice, the latter is of great interest in order to replace low WF alkaline earth metals like *Ca* (2.9 eV) or *Mg* (3.7 eV), which are chemically reactive and therefore susceptible to oxidation in ambient atmosphere. Here, a novel molecule for SAM fabrication, julolidyl disulfide (Juls), is presented and characterized[2]. If not stated otherwise, the SAM layers presented for Juls

2 Juls was synthesized by Malte Jesper in cooperation within the MORPHEUS project. Further details on the synthesis route can be found in his master thesis [104].

here are casted using immersion in ethanol for ~ 1 min inside of a nitrogen filled glovebox. All transistors presented in this section are prepared in BCTG architecture and contain N2200 (polyera™ActiveInk™) as semiconductor, as well as ParyleneC, deposited via CVD, as a dielectric layer. Juls monolayers are optimized towards short immersion times according to the findings on accumulation behavior presented in section 4.1.

The chemical structure of Juls is presented in figure 26a. Unlike the majority of SAM materials that bind to metal surfaces, including the PFDT considered earlier, Juls does not contain a thiol binding-group. The high reactivity of the thiol renders it susceptible to oxidation and severely complicates usage and handling in a realistic fabrication environment. Juls exists as dimer in disulfide configuration before deposition instead and is therefore noticeably more stable in ambient conditions. Interestingly, disulfide structures are already reported in the pioneering work on SAM by Nuzzo and Allara [59] in 1983, but were exceeded in popularity by thiol binding groups thereafter for their superior reactivity to metal surfaces.

4.2.1 *Analytical characterization of Juls SAM*

In figure 27, PES data of pristine and Juls-SAM-covered Au surfaces are presented. Figure 27a-b shows spectra of the C1 s and N1 s core level, respectively. They attest surface cleanliness prior to SAM deposition, and successful application of the SAM on the surface[3]. In figure 27c, SE cutoff energies indicate a total change of the WF of $\sim$ 1.2 eV from pristine to Juls covered Au surfaces. This is among the highest values which are published up to date. The only SAM reported with a higher total WF-change [105] exploits a dithiocarbamate binding group [106] (see section 2.3.2 for details on different binding mechanisms). The wetting envelopes after Owens–Wendt–Rabel–Kaelble [92, 93] of pristine and SAM-treated Au-surfaces, presented in figure 28, demonstrate that Juls not only changes the WF, but at the same time promotes the wetting behavior for polar and non-polar solvents. Hence, Juls treatment can also facilitate the deposition of a subsequent layer from solution.

4.2.2 *OFET optimization with Juls*

The impact of Juls SAM to the performance of an OFET device is demonstrated in figure 29. From the I/V curve in figure 29a, an increased

3 A detailed study with PES on Juls-SAM, including exposure-dependent surface coverage, is presented in Schinke [88].

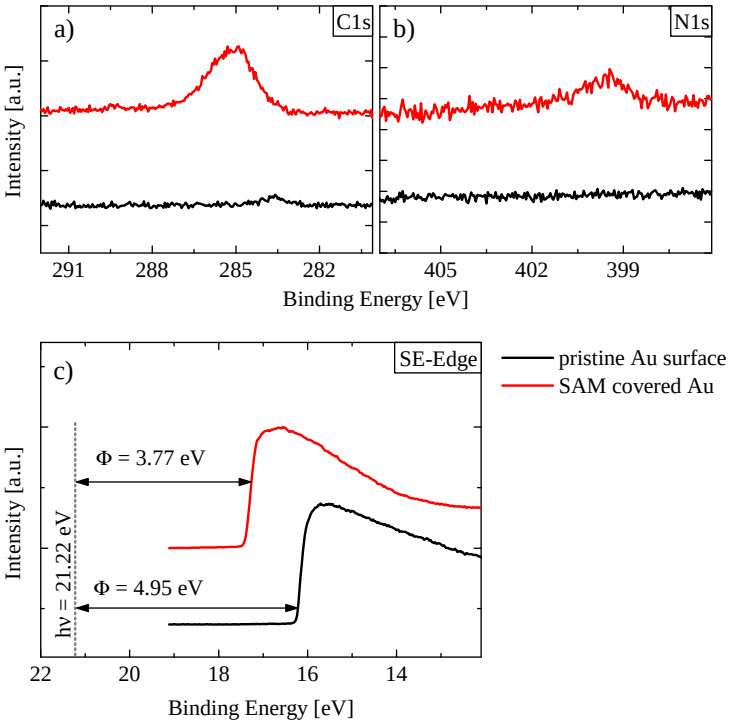


Figure 27: PES data of pristine and Juls-SAM-covered Au surfaces. Detail spectra of C1 s (a) and N1 s (b) core level; (c) SE cuttoff and absolute WF values. Monolayers presented in this figure are casted using immersion in 1 mM for 22 h to ensure optimized surface coverage.

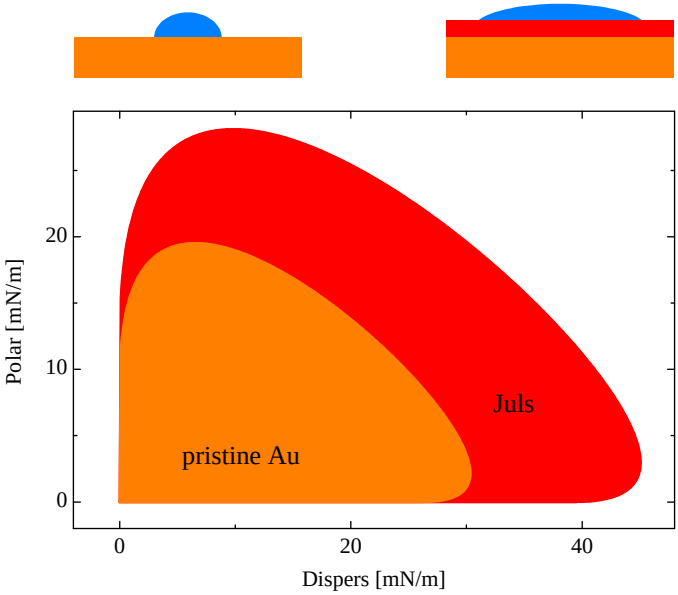


Figure 28: Wetting envelopes of pristine and Juls-SAM-covered Au surfaces, derived via the sessile drop technique after Owens-Wendt-Kaelble [92, 93]. Monolayers presented in this figure are casted using immersion in 1 mM for 22 h to ensure optimized surface coverage.

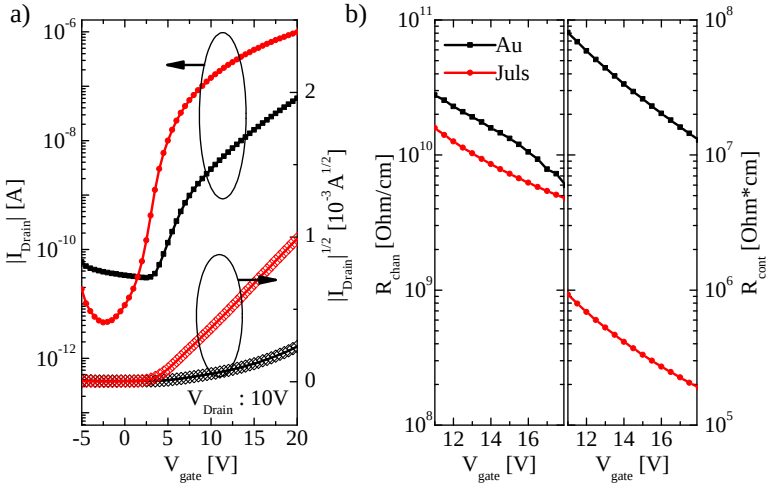


Figure 29: OFETs with Juls SAM. (a) n-type transfer I/V characteristic of devices with pristine and Juls treated Au contacts; (b) channel and contact resistance, derived via TLM.

on/off ratio by more than one order of magnitude, as well as an improved onset behavior can be recognized. Injection properties at the semiconductor/metal interface in a transistor are characterized best via TLM, as is presented in figure 29b. The channel resistance does hereby not change significantly due to the altered injection barrier reduction, as is to be expected because the semiconductor and the chemical configuration at the interface to the dielectric remain unchanged. In contrast, the contact resistance is reduced by approximately two orders of magnitude.

4.2.3 *Ambient processed OFETs with printed electrodes on flexible substrates*

Although the performance increase upon the Juls treatment is remarkable for the devices shown in figure 29, they are prepared on glass substrates, using evaporated Au contacts and SAM immersion, as well as semiconductor spin coating, under highly controlled nitrogen atmosphere. This fabrication procedure matches that of the analytical samples for comparability to the PES data and allows, due to great channel length precision, for a TLM measurement of contact and channel resistance. On the other hand, it undermines the advantageous properties of organic polymers like flexibility, lightweight and low-cost. Furthermore

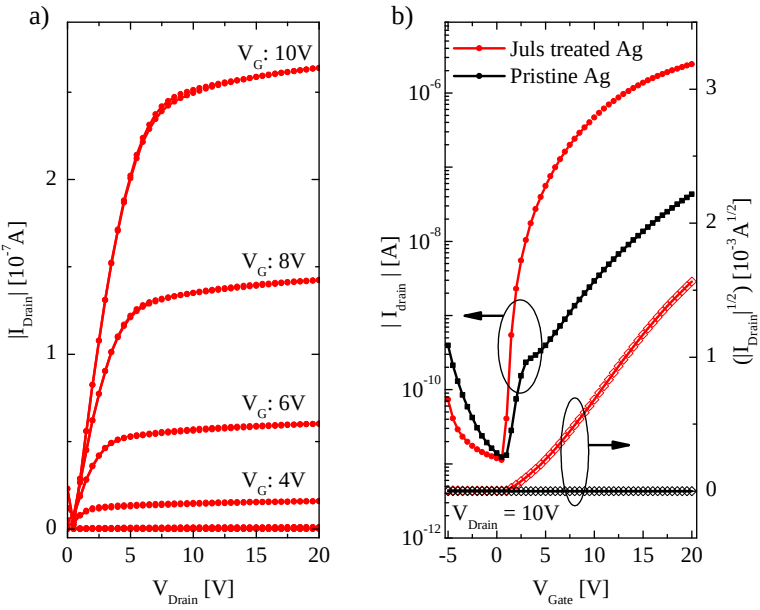


Figure 30: OFETs with and without Juls injection layer on a flexible PET substrate. (a) Output I/V characteristic (Juls treated device only); (b) transfer I/V characteristics with (red) and without (black) SAM.

it is not to be taken for granted, that successful SAM accumulation on a clean, freshly evaporated Au surface can be transferred to printed metal structures, as they typically contain a greater amount of processing-related impurities and adsorbates. In order to assess the potential of Juls under application-relevant processing conditions, OFETs are fabricated using ink-jet printed Ag electrodes on a polyethylene terephthalate (PET) substrate[4] and SAM immersion, as well as semiconductor spin coating, in ambient atmosphere. Output and transfer characteristics of the obtained transistors are presented in figure 30. For comparison, the transfer characteristic of a device with pristine printed Ag electrodes is shown in figure 30b. The performance improvement due to the charge injection promoting SAM, casted from Juls, is clearly eminent for printed Ag electrodes on flexible substrates.

4.2.4 *Protection of silver electrodes in OFETs from degradation in ambient conditions*

One downside of Ag as an electrode material in organic electronic devices is its susceptibility to oxidation under ambient conditions. The injection properties at an Ag/semiconductor interface can be severely influenced by ambient exposure within minutes, as pointed out in section 3.1.3. Even inside a device at a buried interface, contact oxidation can take place, depending on entrapped atmosphere residuals and permeability of the encapsulation. In order to estimate the impact of Juls on the susceptibility of metal contacts towards degradation, OFETs with Ag-electrodes[5] are stored under ambient conditions after characterization and measured repeatedly over the course of 3 months. Additionally to pristine and Juls-treated contacts, devices with ethoxylated polyethylenimine (PEIE)-treated contacts are fabricated for comparison. Device encapsulation is realized by the ParyleneC dielectric layer. Although ParyleneC exhibits a low permeability for oxygen and moisture [107], encapsulation from a 300 nm thin layer still enables a slow gas exchange.

A survey on the degradation in device performance is presented in figure 31. On day 1 after fabrication, the contact resistance $R_{cont.}$ is already significantly higher for untreated contacts over the Juls- and PEIE-treated ones (figure 31a left panel, determined with TLM). Within the first ten days, $R_{cont.}$ of the pristine electrodes increases further by four or-

4 Ink-jet printing of source and drain electrodes from Ag onto PET substrates was realized at the InnovationLab by Tobias Rödlmeier, PhD candidate at KIT/InnovationLab.

5 Electrodes are deposited via thermal vapor deposition to enable precise channel length for contact resistance determination with TLM.

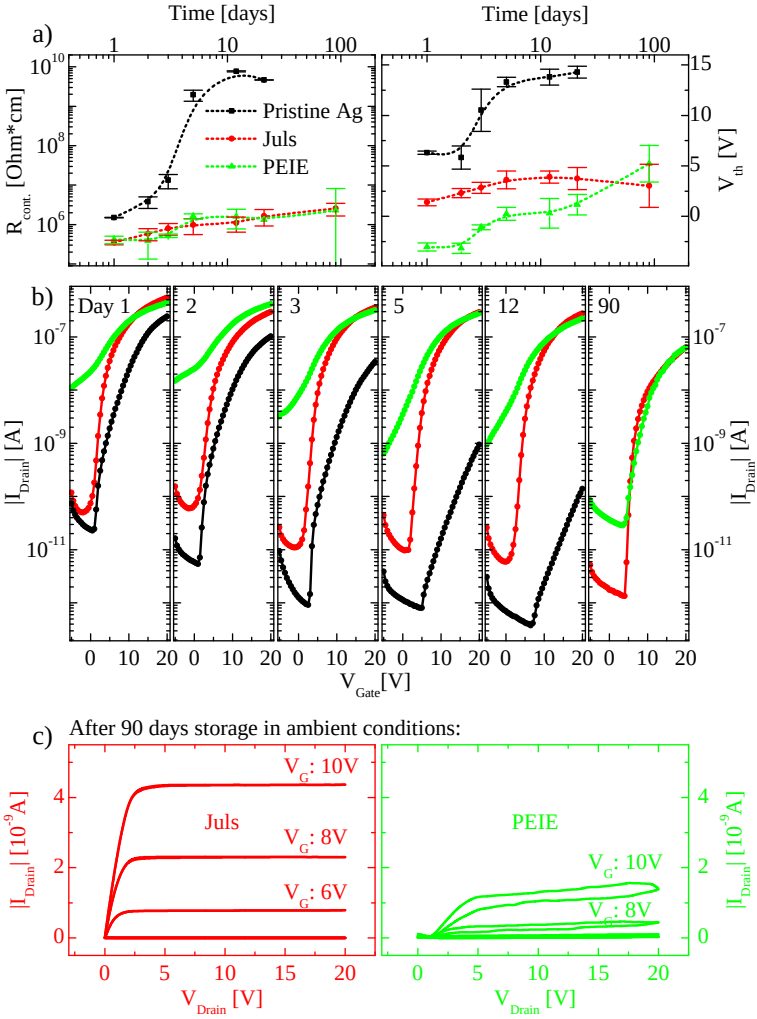


Figure 31: Degradation of ambient stored OFETs, encapsulated with a 300 nm ParyleneC coating. (a) Trend for contact resistance (left) and V_{th} (right) of pristine (black), Juls treated (red) and PEIE coated (green) devices; (b) transfer I/V curve developement, color code according to panel a); (c) output characteristics of Juls treated (red) and PEIE coated (green) devices after 90 days storage.

ders of magnitude. It is not evident from this data, that the degradation is in fact due to Ag-contact oxidation. However, it is certainly caused by an effect at the Ag-contact, since both types of injection promotion treatments prevent this drastic increase. After 90 days, the contact resistance of Juls- and PEIE-coated electrodes is increased by approximately one order of magnitude only, following a linear slope in double-logarithmic scale. Considering the remarkable analogy in the $R_{cont.}$ increase, there is likely a degradation process in the semiconductor responsible, which is identical in both cases.

Concerning the pristine contacts, the threshold voltage trend agrees with that of $R_{cont.}$, and attests a severe drop in device performance within the first ten days (figure 31a, right panel). Between Juls and PEIE, V_{th} exhibits a behavior which is not met by $R_{cont.}$. Initially after preparation, V_{th} of PEIE-treated devices is significantly lower than that of their Juls counterpart. In contrast to Juls, V_{th} of PEIE-treated devices thereafter increases steadily. This disagreement to the $R_{cont.}$ data is referred to the limitations of the MOSFET model in characterization of organic electronic devices as follows: Zhou et al. [97] reported, that PEIE layers above 1.5 nm thickness can result in a doping effect in the channel of a transistor. Although there is, due to the BCTG architecture, no mutual interface between PEIE and the OFET channel, doping of the semiconductor can explain the increased off-current for PEIE treated devices in figure 31b. V_{th} is derived from a fit to I_D in a regime of V_G, which is distorted by the doping effect. With the TLM, $R_{cont.}$ can be differentiated from the channel resistance $R_{chan.}$ and is the more reliable parameter to measure the injection properties in this case. Over time, the degree of doping in the PEIE-devices is reduced, and the I/V curve converges to that of the Juls-device. The influence of PEIE and the Juls-SAM on the injection properties at the metal-semiconductor interface are comparable, according to the absolute value and trend of $R_{cont.}$. A significant difference however, is not eminent in the logarithmic-scale representation of the transfer-characteristic, but becomes clear in the output-characteristic after 90 days (figure 31c). Here, the Juls-treated device shows significantly higher performance than the PEIE-treated one, especially in the range of low operation voltages.

4.3 SELECTIVE OFET OPERATION POLARITY FOR COMPLEMENTARY LOGIC GATE DEVICES

An additional demand for OFET application in integrated circuits, next to an optimized individual device, is the availability of transistors with n- and p-polarity of symmetric performance. Instead of applying two

different semiconductors for this cause, semiconductors with ambipolar transport properties could potentially be used to severely simplify layer stack processing. The existance of such ambipolar materials is one of the advantageous features of organic semiconductors. Ring oscillator and inverter devices from OFETs, featuring ambipolar active materials, have attracted some attention recently [108, 109, 110, 111]. However, in order to construct logic gates with low power dissipation for integrated circuits, it is inevitable to differ two unipolar OFETs with a distinct off-state. One approach to realize this with a single-component active layer, via selective charge carrier injection at the metal-semiconductor interface [112], is addressed in this chapter.

4.3.1 *Bipolar- versus selective unipolar transport*

Due to the bandgap, there is always an off-regime between n- and p-type transport of OFETs with ambipolar semiconductors. Yet, in the combined transfer characteristic this off-regime is narrowed fundamentally by the potential which is applied at the drain-electrode: Since the V_D is fixed for the complete gate-voltage sweep, its sign can be either suited for the n- or the p-type measurement, but not for both. In figure 32, a set of transfer characteristics with an applied drain-potential ranging from $-60\,\mathrm{V}$ to $+60\,\mathrm{V}$ in steps of $10\,\mathrm{V}$ is presented to demonstrate the impact of V_D sign on the I/V curve. As the active material used for the transistor in figure 32 is a p-type semiconductor (PTAA), the potential at the drain electrode is supposed to be negative in a transfer measurement. If it is negative (green curves), the value of V_D has no significant impact on the onset-behavior, as measured by V_{th} and plotted in figure 32b. In the case of positive V_D (red curves) in contrast, V_{th} is shifted with the I/V curve along the x-axis towards the off-state about the absolute value of V_D. In principle, the effect is caused by a reverse definition of source and drain, meaning that the potential at the original source is not the FET-internal ground potential, but instead the drain. Since the voltage at the gate is set with respect to the original source, the actually *effective* gate bias, now with respect to the former drain contact, is increased by V_D. There is no real shift of V_{th}, in fact in a single polarity OFET it does not change anything, except the definition of source and drain. For ambipolar semiconductors however, this effect causes a narrowing or complete quenching of the off-state regime, regardless of the applied potentials sign, because it applies only to one of the two channels. This is visualized in figure 33a: With positive V_D the p-channel is shifted towards the n-channel, which experiences no shift (figure 33a1) and vice versa with negative V_D (figure 33a2).

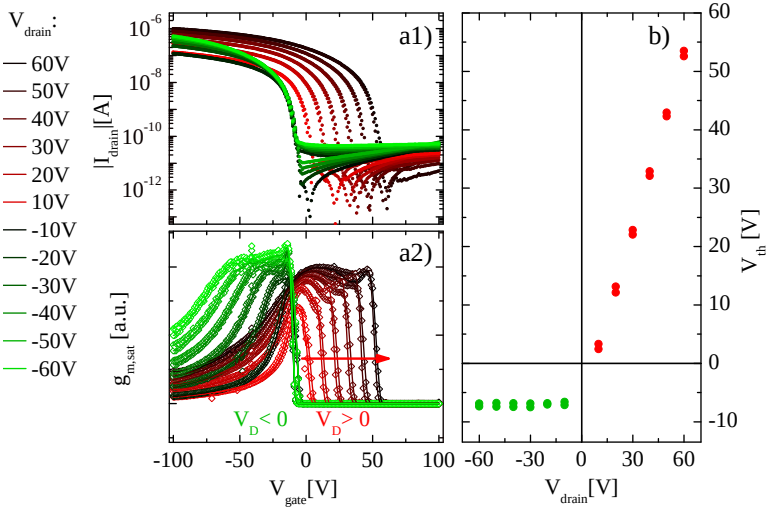


Figure 32: Effective gate voltage illustrated exemplary by threshold voltage shift of a p-type OFET. V_G sweep directions from off- to on-state and backwards are presented for each scan. (a) Transfer characteristics with p-type suited $V_D < 0\,\mathrm{V}$ and unsuited $V_D > 0\,\mathrm{V}$; (b) threshold volatges derived from transfer characteristics in a), plotted against the fix drain voltage at which they where measured.

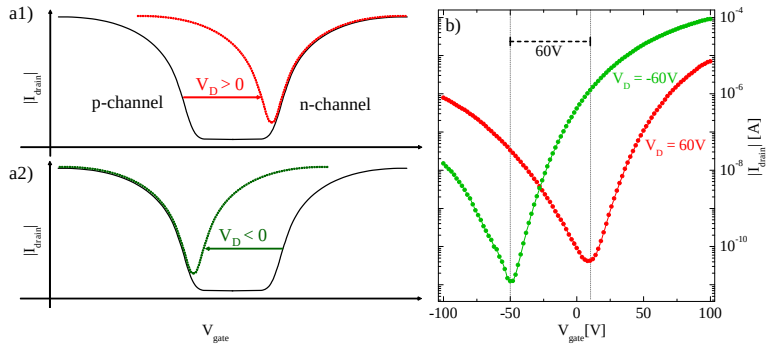


Figure 33: Off-state quenching in ambipolar FETs. (a) Schematic illustration of the impact which V_D has on the I/V curve. (b) Exemplary transfer-characteristics of OFETs with ambipolar PDTDPP-alt-BTZ semiconductor, measured with high V_D of both signs.

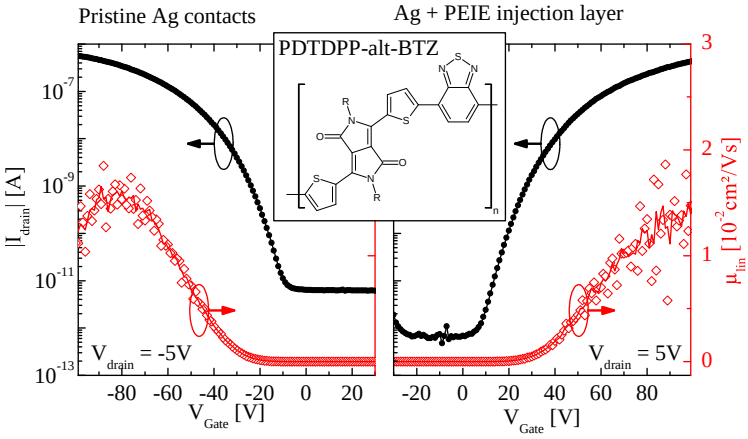


Figure 34: Selective unipolar OFETs with PDTDPP-alt-BTZ. Left: n-type behavior from Ag contacts treated with PEIE injection layer; Right: p-type behavior from pristine Ag contacts. The inset shows the chemical structure of PDTDPP-alt-BTZ.

One example of an ambipolar OFET with such behavior is presented in figure 33b, using Cytop as a dielectric layer. The semiconductor that is applied in this example is poly(diketopyrrolopyrrole-benzothiadiazole) (PDTDPP-alt-BTZ), which was reported to exhibit balanced, high performance electron- *and* hole-mobility [108][6]. The chemical structure of PDTDPP-alt-BTZ is presented in the inset in figure 34.

4.3.2 *PEIE- and Juls-treated unipolar OFETs with PDTDPP-alt-BTZ*

In order to use ambipolar semiconductors for selective unipolar FETs in complementary logic integrated circuits, the operational V_D must be sufficiently low to enable a clear off-regime. PDTDPP-alt-BTZ is in principle a valid material for this cause, as is demonstrated in figure 34. The OFETs presented in figure 34 differ in the source-drain contact injection layer treatment, and exhibit clear p- or n-type behavior with a distinct respective off-state at $V_D = \pm 5\,\mathrm{V}$. In this manner, organic complementary logic gates can be realized from a simplified layer stack layout with only one semiconductor and one contact material. There are however further requirements which are not met by the specific material combination presented here. First of all, the voltage range for the sweep at the gate

6 PDTDPP-alt-BTZ was synthesized by Marius Kuhn [113] within the MORPHEUS project.

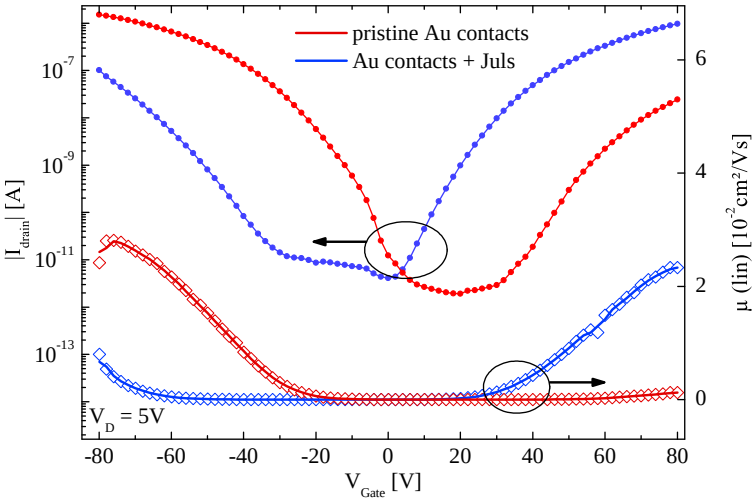


Figure 35: Selective unipolar OFETs with PDTDPP-alt-BTZ and Juls SAM. Blue: Au contacts treated with Juls injection promoting SAM; Red: pristine Au contacts.

electrode $V_G = \pm 100\,\mathrm{V}$ is too high for a realistic application. Secondly, the initial balance in p- and n-type mobility shifts towards p-type, as the n-channel shows a higher susceptibility to degradation due to electrical and environmental stress. Furthermore, the PEIE n-type injection treatment which was applied includes spin-coating at high angular velocity ($\sim 3000\,rpm$) and is therefore unsuited for lateral patterning. The first two limitations could, despite considerable effort, not be overcome and are presumably of fundamental nature. The third restriction is, however, specific to insulating polymeric injection layers like PEIE and does not apply for SAM injection layers. OFETs with PDTDPP-alt-BTZ are presented in figure 35 with pristine versus Juls-treated Au contacts. For the OFETs in figure 35, PMMA was used as an adhesion coating for ParyleneC dielectric. The concept of injection layer differentiated selective unipolar OFETs from only one semiconductor and one contact material can be demonstrated with PDTDPP-alt-BTZ. The high operation voltage (at the gate-electrode) and the low stress resistance of the n-channel are drawbacks which can not be overcome by device engineering, but rather have to be addressed in the chemical structure of the semiconductor.

5

PASSIVATION OF TRAP STATES AT ORGANIC/INORGANIC INTERFACES

APPROACH

Energetic states within the bandgap of a semiconductor can immobilize, or *trap*, charge carriers and thereby change the local electrical charge density. If occupied trap states occur in a field-effect transistor at the semiconductor-dielectric interface, the location of the conductive channel, they alter the device performance characteristic. Since the filling of trap states is assisted by electrical fields and current densities during device operation, the drift of device performance caused by trapped charges is referred to as *bias stress effect.* Considering the impressive recent progress with flexible, low temperature processable inorganic dielectric layers [114, 115, 116, 117, 118], hybrid devices of organic semiconductors and inorganic gate-dielectrics could possibly meet the multitude of requirements for future flexible TFT-applications on processability, and electrical- as well as mechanical properties better than purely organic or purely inorganic ones. Organic/inorganic interfaces are, however, notoriously known to provide charge carrier trap states and in a device with organic semiconductor and inorganic dielectric, the channel is located just at this interface. The common approaches to neutralize (or *passivate)* inorganic surfaces, via octadecyltrichlorosilane (OTS), hexamethyldisilazane (HMDS) [119] or thin fluorinated polymer coatings, render the surface strongly hydrophobic. Although the passivation functionality from these coatings is thorough, the low surface energy causes dewetting of polar solvents including alcohols, ketones or water, preventing solution processing with common industrial solvents. In this chapter, a different approach for trap passivation at organic/inorganic interfaces is described, using thin polymer layers of ParyleneC.

The effects described in this chapter occur at a buried interface and are caused by electrical stress inside an operating device. An analytical investigation of the surface via PES or IRRAS is therefore ruled out, and the approach is based on devices alone. The transistor is, in this case, serving as a gauge for the characterization of buried interfaces.

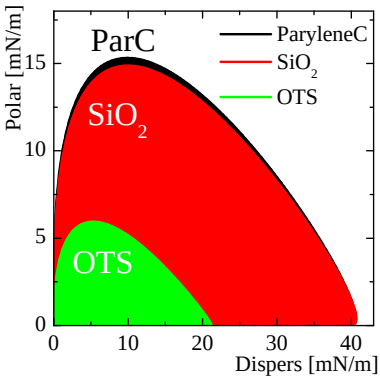


Figure 36: Wetting envelopes of pristine SiO_2, ParyleneC and a common surface passivation layer OTS in comparison.

5.1 WETTING AND PASSIVATION BEHAVIOR

Bilayer dielectric stacks with SiO_2 and ParyleneC are fabricated by deposition of a thin layer of ParyleneC via CVD onto a Si-wafer with thermally grown SiO_2. ParyleneC grows as a conformal, dense polymer film with uniform coverage and low roughness on almost any surface and is resistant to a broad range of solvents [120]. Although not considered a solution process, CVD can be performed at room temperature with moderately low pressure of 10 mbar and continuous roll-to-roll deposition was demonstrated [121, 122]. In medical engineering, ParyleneC is investigated for implant encapsulation [123, 124, 125] due to its chemical inertness and low water and oxygen permeability. ParyleneC has been used as a permeation barrier for oxygen and moisture in organic LED [107] and to improve the performance of vapor deposited OFETs by passivating the SiO_2 dielectric [126]. In order to examine the general wetting behavior of ParyleneC layers, disperse and polar fractions of the surface tension after Owens–Wendt–Rabel–Kaelble [92, 93] were determined from SiO_2 and ParyleneC surfaces with the sessile drop technique. The deduced wetting envelope, presented in figure 36, shows the wettability of ParyleneC to be very similar to that of SiO_2 and superior to that of OTS, especially for polar solvents.

The OFET stack is presented in figure 37a. PTAA as a semiconductor and Au contacts are used for all transistors in this chapter. Next to pristine SiO_2 and pure ParyleneC, a bilayer of SiO_2 and ParyleneC is investigated as a gate dielectric (stack i.-iii.), according to figure 37b. In order

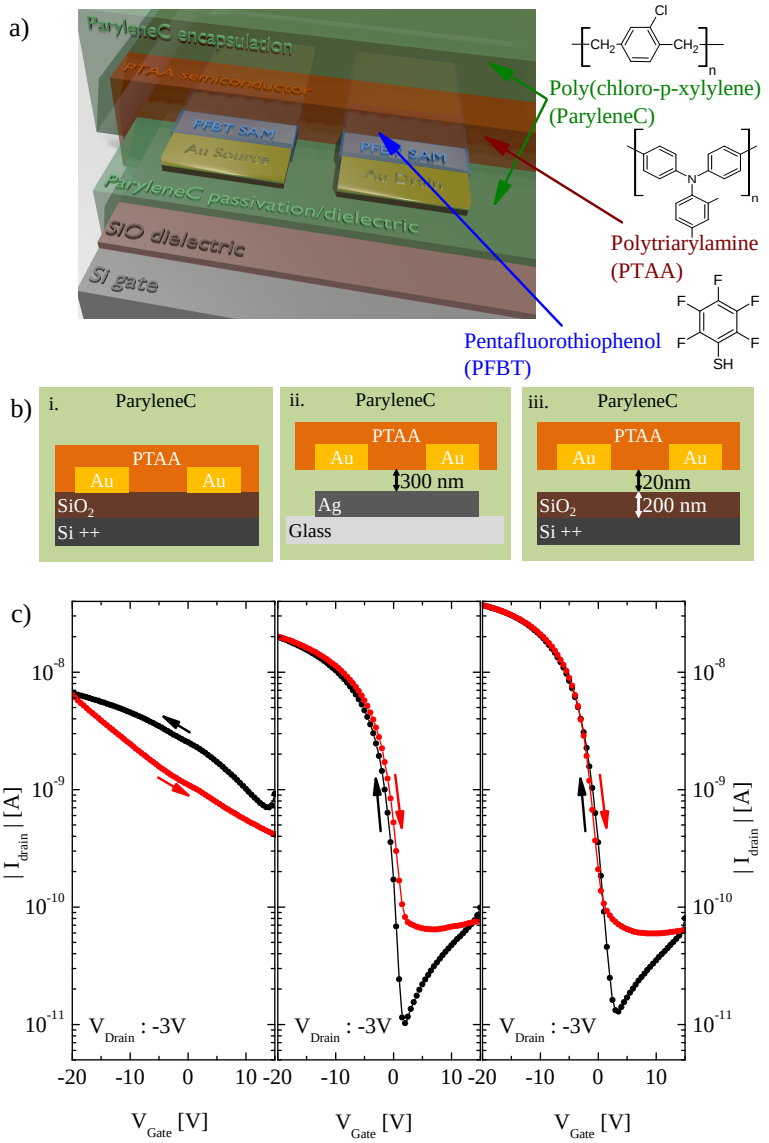


Figure 37: Transistor architecture. (a) Schematic cross section and chemical structures of applied organic materials; (b) three different transistor stacks investigated; (c) representative transfer I/V characteristics of the three transistor stacks.

to maximize direct comparability between the devices, the film thicknesses were selected in a way that the total capacitance per area differs as little as possible. In contrast to the pristine SiO_2 dielectric, both dielectric stacks with ParyleneC as topmost layer exhibit a marginal hysteresis between forward- and backward sweep and show similar performance. From this first V_G sweep it cannot be distinguished whether there is SiO_2 beneath the ParyleneC or not, the trapping sites seem thoroughly passivated.

5.2 SUCCESSIVE I/V SWEEP BIAS STRESS EFFECT

Figure 38 shows repeated gate-voltage sweeps of stack ii. and iii. in order to investigate their stability against electrical stress. The upper row of graphs in figure 38a shows transfer I/V curves and the respective transconductances g_m are plotted in the lower row. While the OFET with pure ParyleneC dielectric shows excellent stability over the course of 20 V_G sweeps, the one with ParyleneC-covered SiO_2 exhibits a steady shift in onset voltage upon electrical stress. In the according transconductances an additional shoulder in the range of the former off-state arises. Figure 38b presents the threshold voltages, derived from the I/V curves in figure 38a, plotted against the scan number. The trend of V_{th} in this graph reflects the drift of the onset voltage with successive V_G sweeps. While the bias stress effect is negligible with pure ParyleneC, it shifts V_{th} by $\sim 10\,\mathrm{V}$ in the SiO_2/ParyleneC bilayer dielectric. This suggests, that charge carriers diffuse through the ParyleneC and become trapped within the SiO_2 due to the gate bias. Apparently, that happens in such a low rate that the amount is insignificant in a single gate voltage sweep, as demonstrated in figure 37c. Accumulated over the course of successive sweeps though, the net charge in the SiO_2 causes an offset in V_G and therefore shifts the onset voltage gradually. Additional to the two data sets from figure 38a (measured with $V_D = -3\,\mathrm{V}$), the V_{th} trend of stack iii. was measured with $V_D = -10\,\mathrm{V}$ and is plotted for comparison[1]. The observed drift in V_{th} is with $\sim 20\,\mathrm{V}$ even more pronounced at higher V_D.

Because the transfer-sweep includes $-20\,\mathrm{V} < V_G < 15\,\mathrm{V}$, it gives no information if charge trapping occurs during positive or negative gate potential. Figure 38 presents devices that are not swept continuously, but stressed constantly with $V_G = \pm 15\,\mathrm{V}$ between successive measurements. The obtained I/V curves are presented in figure 39a to visualize the drift

1 The according I/V characteristics are presented in figure 40

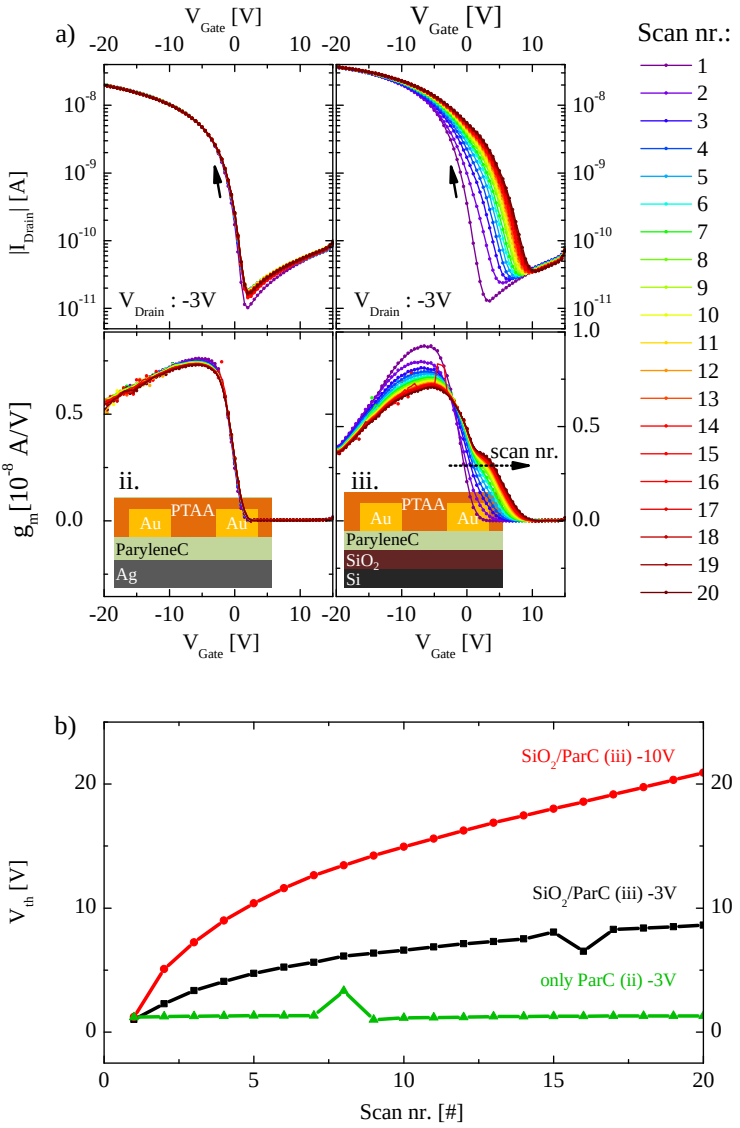


Figure 38: Gate bias stress behavior. (a) OFET transfer I/V characteristics and transconductances of 20 successive sweeps with pure ParyleneC and ParyleneC/SiO_2 bilayer dielectric; (b) threshold voltage trends of successive transfer sweeps.

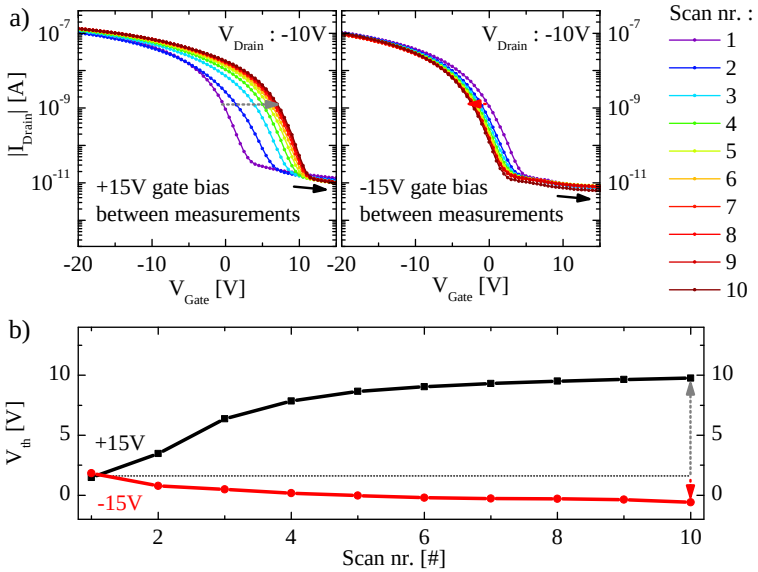


Figure 39: Constant gate potential applied between successive I/V sweeps of an OFET with ParyleneC/SiO_2 bilayer dielectric. (a) Drift of the transfer I/V curves; (b) threshold voltage trend against scan numer.

of the onset-voltage which results in a shift of V_{th}, as shown figure 39b[2]. The electrical stress behavior is clearly occurring during positive gate stress, i.e. in the depletion of holes. This result implies two conclusions: for one, the bias stress is attributed to trapping of *negative* charges in the SiO_2 and second, it occurs while the device operates in the saturated regime, when $(V_G - V_{th}) < V_D$. Considering the latter explains also that the bias stress effect is found to be more severe if the transfer-curve is derived at higher V_D, as shown in figure 38b, because the saturation regime is thereby prolonged. The bias stress effect can be reduced with an increased layer thickness of the ParyleneC coating, demonstrated in figure 40.

5.3 TEMPERATURE BEHAVIOR

In figure 41 transfer measurements derived at increasing temperatures from room temperature (RT) to 100 °C in steps of 10 °C are presented. The top row shows the I/V curves and the middle row the according g_m. Devices with pure ParyleneC and with ParyleneC-covered SiO_2 dielectric are presented for comparison. To ensure stable device performance, 400 successive transfer sweeps were performed at RT prior to the first temperature increase. After each temperature increase the devices were constantly measured again for 30 min (15 sweeps) to reach an equilibrium state. Devices with pure ParyleneC dielectric exhibit a typical increase in transconductance (figure 41a2) due to thermally activated hopping transport in organic semiconductors (equation 1). The transistor with ParyleneC/SiO_2 dielectric shows a analog increase of the maximum g_m with increasing temperature (figure 41b2). In contrast, the shoulder of g_m at positive V_G, that was assigned to trapped charges in section 5.2, decreases at high temperatures in the ParyleneC/SiO_2 devices. The explicit dependency of this shoulder on the temperature becomes apparent in the normalized g_m, presented in the bottom row of figure 41. Devices with pure ParyleneC exhibit no significant change with the temperature increase in this representation, the thermally activated transport acts mathematically as a dilation of g_m. The two features in g_m of the ParyleneC/SiO_2 bilayer, however, differ in their temperature-dependency: while the first one at negative V_G matches g_m of the pure ParyleneC, the shoulder at positive V_G changes in its relative intensity. It increases from RT up to 60 °C, and then decreases with further in-

2 The shift of V_{th} is less severe than in figure 38b, despite significant constant gate stress for 15 min between successive measurements. The measurement was performed a after thermal treatment, described in section 5.4.

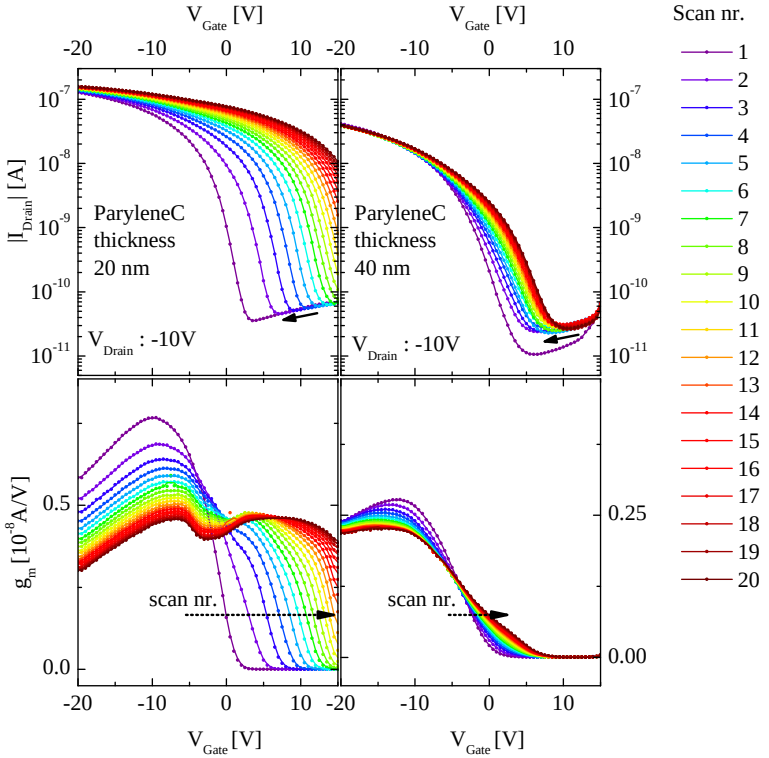


Figure 40: Influence of the ParyleneC layer thickness on the passivation properties. Left: 20 nm ParyleneC layer thickness; right: 40 nm ParyleneC layer thickness; top: absolute drain-current; bottom: transconductance g_m.

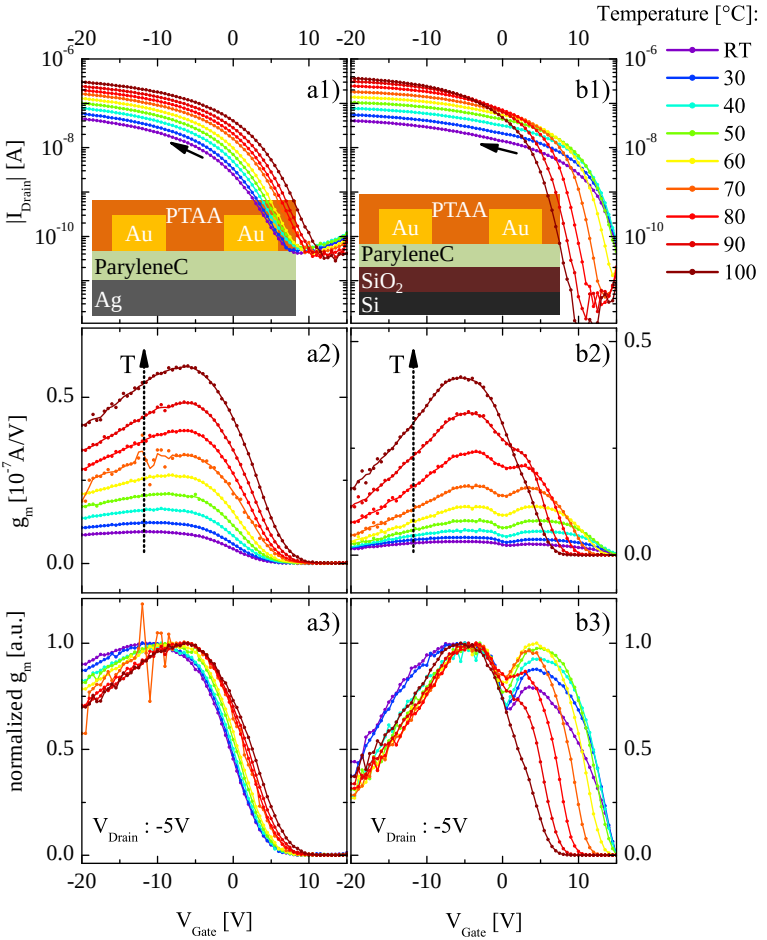


Figure 41: Temperature dependent transfer I/V characteristics of devices with pure ParyleneC (left) and ParyleneC/SiO_2 bilayer (right) dielectric. Top: absolute drain-current; middle: transconductance g_m; bottom: normalized transconductance.

creasing temperature[3]. This two-fold temperature dependency suggests two competing processes to be involved in the total quantity of occupied trap states. On the one hand, rising temperature can result in increasing seepage of charge carriers through the ParyleneC to the SiO_2. On the other hand, increasing temperature evokes thermally activated trap depopulation, therefore the lifetime of the charged defect states decreases with increasing temperature.

5.4 INFLUENCE OF THERMAL TREATMENT ON THE BIAS STRESS EFFECT

In figure 42 I/V curves and g_m from bias stress measurements of a ParyleneC/SiO_2 device before and after a heating procedure are presented. The thermal treatment was carried out, as described in section 5.3, at increasing temperatures up to 100 °C. The impact to the I/V characteristic in figure 42a is comparable in the result, but the required electrical stress load to induce the equivalent effect of 20 V_G sweeps before heating increases to 500 sweeps afterwards. To illustrate the analogous behavior before and after thermal treatment, figure 42b presents selected single I/V curves of the two series. The first scan of each series in the left graph demonstrates the remarkable stability of the device and reversibility of the trap state occupation: after several hundred transfer-measurements and a heating procedure over the course of hours, the first I/V curve is nearly unchanged. The graph on the right of figure 42b shows scan number 16 and 470 of the stress series before and after the thermal treatment, respectively. Due to the very similar I/V behavior, it can be concluded that the device is respectively in a comparable condition concerning the total amount and distribution of filled trap states. A comparison of the V_{th} trend with continuous sweeping before and after thermal annealing is presented in figure 42c. The susceptibility of the SiO_2/ParyleneC bilayer to bias stress effects is reduced considerably upon the thermal treatment.

5.5 CHARGE TRAPPING MECHANISMS IN SILICON OXIDE

Despite being extensively addressed in literature, the exact mechanisms for charge trapping in SiO_2 remain under debate. Already more than 20 years ago it was proposed that neutral electron traps in SiO_2 can be created by the energy released through the recombination of electrons

3 The reversal point from increasing to decreasing peak intensity with temperature lies close to the glass transition temperature of ParyleneC 70 °C, as measured via thermally stimulated depolarization current spectroscopy by Tewari et al. [127].

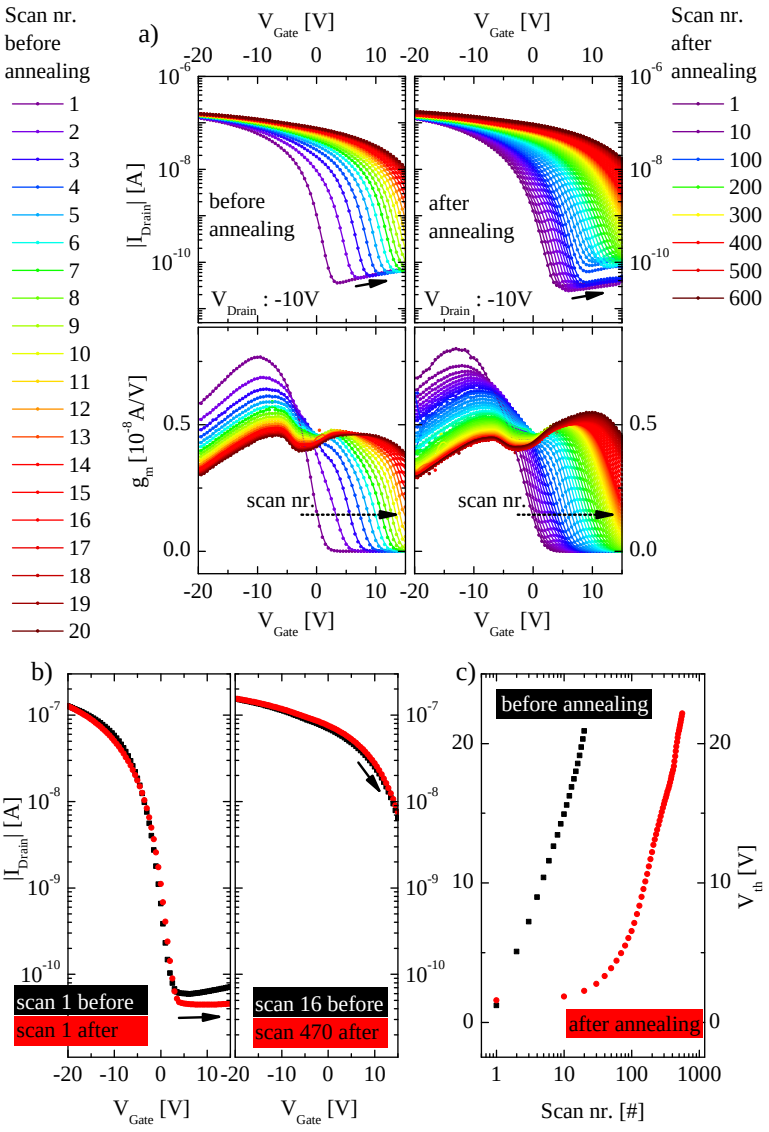


Figure 42: Change of the bias stress behavior of the ParyleneC/SiO_2 bilayer dielectric due to thermal annealing. (a) Two series of transfer I/V characteristics before and after thermal treatment; (b) comparison of single I/V curves of the respective series. (Left graph: first scan from each series. Right graph: scan nr. 16 before and scan nr. 470 after thermal treatment); (c) threshold voltages derived from transfer-characteristics in a), plotted against the scan order.

and holes [128] or associated with dipolar defects from injected holes alone, which can break Si−O bonds as they are transported in the oxide [129]. These neutral traps can subsequently become negatively charged by injected electrons. In 2008 deprotonation of hydroxyl-groups under influence of water was proposed as the origin for SiO_2-dielectric bias stress behavior according to the reaction [130]:

$$SiOH + H_2O \Leftrightarrow SiO^- + H_3O^+ \tag{10}$$

Since the Si wafers have been stored and cleaned in ambient conditions before OFET processing, one can assume the presence of SiOH hydroxyl-groups as well as residual water molecules in the SiO_2 layer. Therefore the deprotonation of hydroxyl-groups as the origin for gate bias stress behavior of OFETs [130, 131] according to equation 10 is a possible trap formation mechanism. In order to result in a negative net charge, the H_3O^+ or hydronium ions need to be either neutralized or separated from the SiO^-. Since the effect happens during positive gate bias, the extraction of H_3O^+ ions from the SiO_2 through the ParyleneC layer might be by driven by the electrical field. On the one hand this can explain why the gate bias effect is slowed down after thermal annealing: The permeability of ParyleneC for water decreases upon thermal annealing [132], resulting in slower charge seepage. On the other hand, in this case the total amount of residual water in the SiO_2 should be reduced as soon as the bias stress effect occurs. Yet, this was not observed in our experiment. Instead the gate bias behavior was found to be reversible in absence of high temperatures. Alternatively, the reduced trapping rate after annealing can result from an overall reduced amount of residual water which is needed in a trapping process after equation 10. Thermal stress can cause two hydroxyl-groups to form an Si−O−Si bond under emission of a H_2O molecule [133]. If the water molecules diffuse away from the SiO_2 the total amount of hydroxyl-groups available, and with it the cross section for electron trap creation, is reduced.

6

POLYMERS WITH THERMALLY STIMULATED SOLUBILITY REDUCTION

APPROACH

The successive deposition of multiple thin layers from solution on top of each other is one necessity for printed electronics, which causes challenges in the development of materials and processing procedures. In order to create a distinct interface of two materials, partial dissolution of a deposited layer in the solvent of the subsequently deposited material must be prevented [7]. In principle, there are two ways to approach this problem: either, the process solvents of adjacent layers are selected to be *orthogonal* to each other [134], or the solubility of a material has to be altered after deposition [135, 136]. In this chapter, an example of the latter approach, via a thermal stimulus is presented. A schematic illustration of the concept is presented in figure 43.

The semiconductors presented in this chapter are based on derivatives of 1,4,5,8-naphthalenetetracarboxdiimide (NDI) and bithiophene co-polymers, the basic building block of prominent air-stable organic n-type materials with high performance [57, 137, 10]. The alkyl side-chains which provide solubility are attached with a carbamate or carbonate linker to the NDI core and can be cleaved off thermally to alter the solubility of the remaining film. The breakup, or *pyrolysis* temperature depends on the exact chemical configuration at the link, but is generally around 200 °C for carbonate and considerably lower for carbamate groups. This amount of thermal stress is compatible with polymer substrates [138]. In figure 44, chemical structures of three NDI-based polymers[1] are presented before and after the removal process[2]. All three polymers still contain alkyl side-chains after the thermal treatment. These groups are important in order to maintain the mechanical flexibility of the film. Furthermore, the morphology, and with it the electrical performance of a film depends crucially on the length and

1 The synthesis of these materials and other NDI-bithiophene co-polymer derivatives and small molecules was developed and performed by Torben Aderman within the MORPHEUS project. The reader is referred to his PhD thesis [139] for details on the synthesis and further characterization. This work focuses on selected materials that exhibit good performance in OFET devices.

2 A detailed study on the solubility change upon heating is presented in the PhD thesis of Janusz Schinke [88].

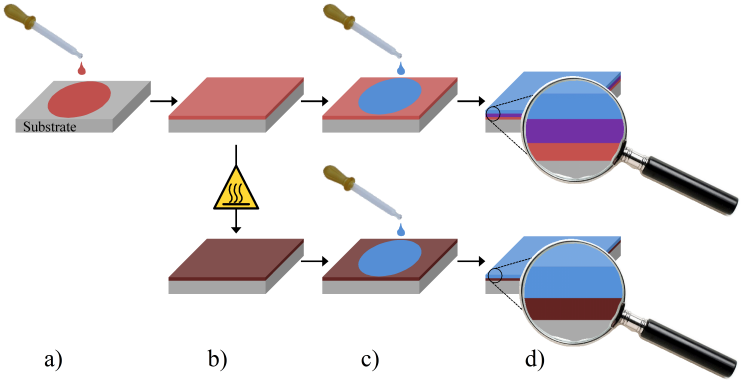


Figure 43: Schematic illustration: Multilayer processing. (a) Deposition of the first layer from solution; (b) top: film without post deposition treatment; bottom: film with post deposition pyrolysis; (c) deposition of the second layer from solution; (d) top: layer mixing at the interface; bottom: interface without layer mixing.

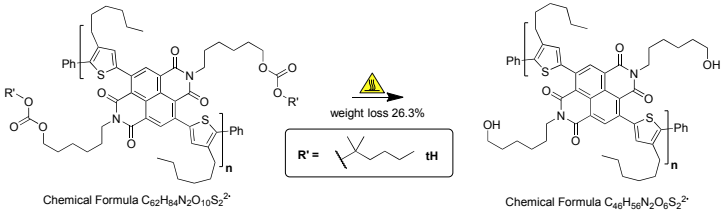
shape of the final alkyl-chain configuration [137, 140]. Although the delicate optimization between solubility reduction and beneficial morphology exceeds the scope of this work, three polymers with fundamentally different side-chain configurations on an otherwise identical backbone (see figure 44) are characterized. For simplification, the polymers are renamed "Thersol 1-3". All three exhibit excellent solubility and film-forming properties prior to thermal treatment.

All polymer films described in the following are deposited via spin coating from 10 mg/ml solution in chlorobenzene. The OFET devices presented in this chapter are fabricated in BCTG architecture, using thermally evaporated Au contacts and CVD processed ParyleneC dielectric.

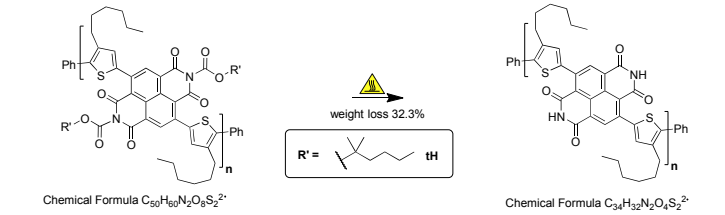
6.1 THERSOL 1-3: ANALYTIC CHARACTERIZATION AND DEVICE PERFORMANCE

6.1.1 *Thersol 1 (P(HtHC-NDI-4HT2))*

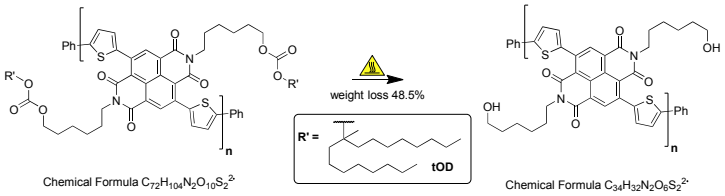
Thersol 1 (chemical structure presented in figure 44a) contains two side-chains at the NDI compound, that are cleaved off at a carbonate linker and result in a hydroxyl-capped hexyl-chain, each. Additionally, hexyl-groups are attached to each thiophene compound. The required temperature for the pyrolysis of Thersol 1 was determined with thermogravi-



(a) P(HtHC-NDI-4HT2) (Thersol 1)



(b) P(tHC-NDI-4HT2) (Thersol 2)



(c) P(HtODC-NDI-T2) (Thersol 3)

Figure 44: Chemical structures of NDI-bithiophene co-polymers with alterable solubility via cleavable side-chains.

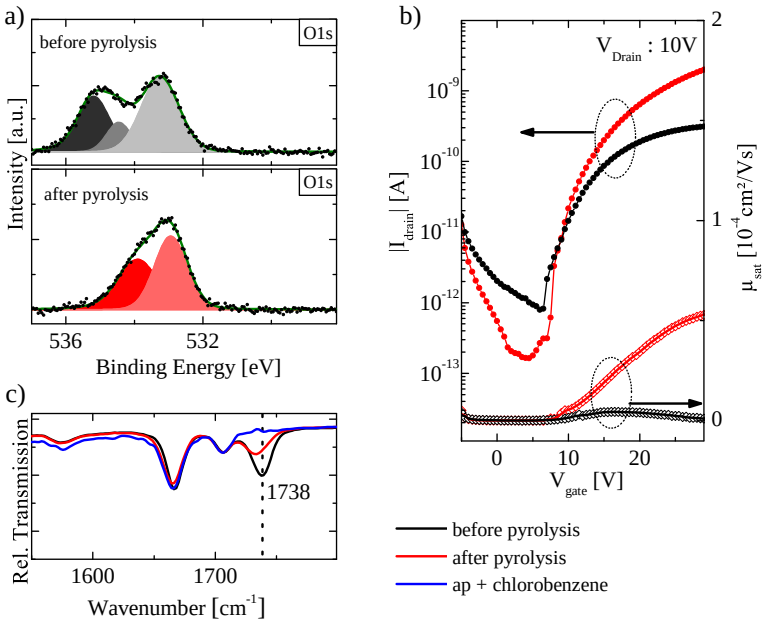


Figure 45: Data survey Thersol 1. (a) PES signal of the O1 s orbital before and after the pyrolysis procedure. (b) OFET devices with Thersol 1 semiconductor before and after the pyrolysis; (c) IRRA spectra of the C=H stretching vibrations before and after the pyrolysis, as well as after an additional washing procedure with the original solvent chlorobenzene.

metric analysis[3] to be 193 °C [139]. A pyrolysis stimulus at 220 °C was applied for 3 min in nitrogen atmosphere. In figure 45, analytical investigations via PES and IRRAS as well as OFET devices with Thersol 1 before and after pyrolysis are presented. The PES signal of the O1 s peak (figure 45a) is used as a marker for the cleavage of the carbonate group. The original carbonate O1 s signal contains three features for three different oxygen species in the structure. After pyrolysis, the O1 s signal shows two features for two oxygen species, a clear sign for completed carbonate separation. The concept is shown in more detail in figure 46, taken from [88]. Transfer characteristics of OFET devices with pristine and pyrolyzed Thersol 1 are presented in figure 45b. Due to the pyrolysis, the OFETs performance is increased significantly, rising one order of magnitude in on/off ratio and maximum mobility. IRRA spectra of

3 Onset at 157 °C; 5 %weight loss at 193 °C; inflection point 200 °C [139].

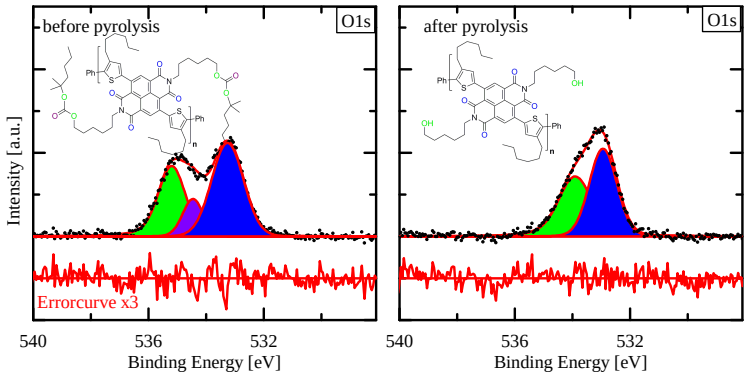


Figure 46: O1 s core level spectra (black dots represent the measured spectra with removed background) and the corresponding fits for polymer before (left side) and after (right side) pyrolysis. The colors of the fitted component are matched with the colors of the chemical structure. Redrawn after [88]

Thersol 1 (figure 45c) show the region of the C=O stretching vibrations, with that of the side-chain at 1738 cm^{-1}. Upon pyrolysis, the 1738 cm^{-1} peak is reduced significantly in intensity. However, the remaining intensity of the signal suggests, that residual side-chains, despite being cleaved off at the broken carbonate group, remain in the film. A washing procedure with the original solvent chlorobenzene was applied to the pyrolyzed film (blue spectrum in figure 45c). As a result of the washing, the residual peak at 1738 cm^{-1} dissappears, i.e. the remaining detached side-chains are washed out of the film.

6.1.2 *Thersol 2 (P(tHC-NDI-4HT2))*

Thersol 2 (figure 44b) differs in its chemical structure from Thersol 1 concerning the decomposable group which connects the hexyl-chain to the NDI unit. The carbamate linker in Thersol 2 is placed directly at the NDI, instead of being connected through an additional hexyl-chain as spacer. This way, no hydroxylgroups capping the hexyl-chains are left behind in the film. Additionally, the absence of attached alkyl-groups at the NDI units in the resulting chemical structure reduces the remaining material solubility after pyrolysis even further than in Thersol 1 [139, 88]. Furthermore, the decomposition temperature of the carbamate linker is

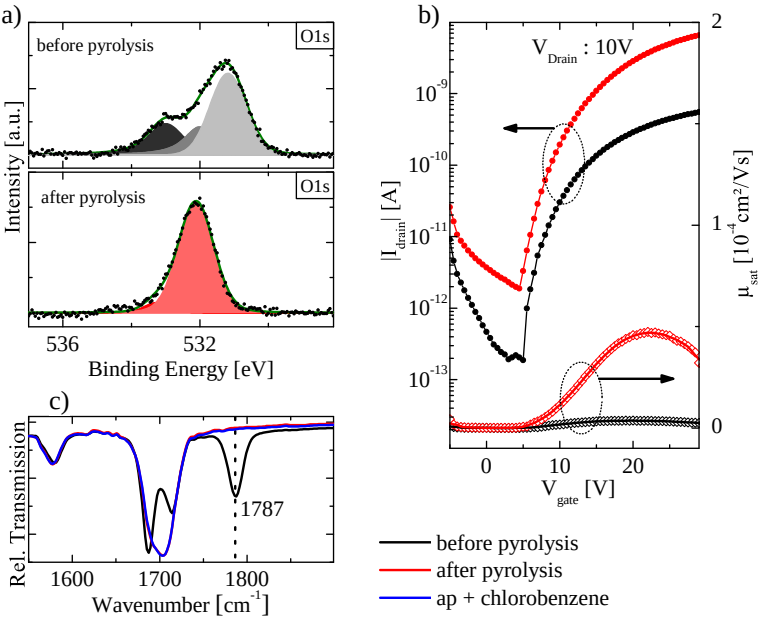


Figure 47: Data survey Thersol 2. (a) PES signal of the O1 s orbital before and after the pyrolysis procedure; (b) OFET devices with Thersol 2 semiconductor before and after the pyrolysis; (c) IRRA spectra of the C=H stretching vibrations before and after the pyrolysis, as well as after an additional washing procedure with the original solvent chlorobenzene.

with 132 °C about 60 °C lower than that of Thersol 1[4]. Pyrolysis of Thersol 2 was performed at 180 °C for 3 min in a nitrogen atmosphere. In figure 47 analytical investigations via PES and IRRAS as well as OFET devices with Thersol 2 before and after pyrolysis are presented. Comparable to Thersol 1, the PES signal of the O1 s (figure 47a) peak attests a complete decomposition of the linker groups. The electrical performance of Thersol 2 in OFET devices (figure 47b) is slightly superior to that of Thersol 1, represented in higher currents at the drain electrode and a better on/off ratio. Since devices from Thersol 1 and Thersol 2 are prepared in independent batches, processing related differences of the dielectric thickness limits the direct comparability of the I/V curves. The increase in performance of pyrolyzed over the pristine material is, however, within the same batch and therefore significant. The maximum

4 Onset at 97 °C; 5 %weight loss at 132 °C; inflection point 146 °C[139].

extracted field effect mobility is as performance parameter independent from the dielectric thickness, and very similar between Thersol 1 and Thersol 2. In contrast to Thersol 1, the IRRA spectrum of Thersol 2 exhibits no visible signal of the alkyl-chains after pyrolysis, suggesting a complete removal from the film. The position of the according C=O stretching bond of the carbamate group is at 1787 cm^{-1}. Upon a subsequently applied washing procedure with chlorobenzene, no visible change occurs in the IRRA spectrum.

6.1.3 *Thersol 3 (P(HtODC-NDI-T2))*

Thersol 3 (figure 44c) exhibits no hexylgroups at the thiophene units along the polymer backbone, but instead contains a longer, branched alkyl-group connected via a carbonate linker to maintain sufficient solubility before pyrolysis. After the side-chain cleavage, the missing hexylgroup at the thiophene unit is the only difference to Thersol 1. Thermogravimetric analysis[5] shows a pyrolysis temperature of 203 °C for Thersol 3 [139]. In figure 48 analytical investigations via PES and IRRAS as well as OFET devices with Thersol 3 before and after pyrolysis are presented. A pyrolysis stimulus at 220 °C was applied for 3 min in nitrogen atmosphere, identical to the procedure for Thersol 1. The PES signal of the O1 s orbital (figure 48a) suggests, that carbonate decomposition is initiated, but not fully completed after this procedure. This is consisted with the slightly higher pyrolysis temperature of Thersol 3 over Thersol 1. Clearly visible in the IRRA spectra (figure 48c), there are alkyl-groups left in the film after pyrolysis which become washed out by the subsequently applied washing procedure with chlorobenzene. To investigate the influence of the remaining alkyl-groups, and the influence of their removal via solvent washing, additional OFET devices were prepared with pyrolyzed and washed Thersol 3 films (figure 48b). Similar to the behavior of Thersol 1 and Thersol 2, the performance is increased significantly after the pyrolysis. Interestingly, the OFET with the semiconductor that was washed with solvent after the pyrolysis exhibits a reduced performance, not only against the pyrolyzed but also against the pristine film.

6.2 INFLUENCE OF PYROLYSIS AND SOLVENT WASHING

PES or IRRAS measurements of Thersol 2 films exhibit no signs of alkylgroups after the pyrolysis, as well as no change due to a washing proce-

5 Onset at 173 °C; 5 %weight loss at 203 °C; 2-step decomposition [139].

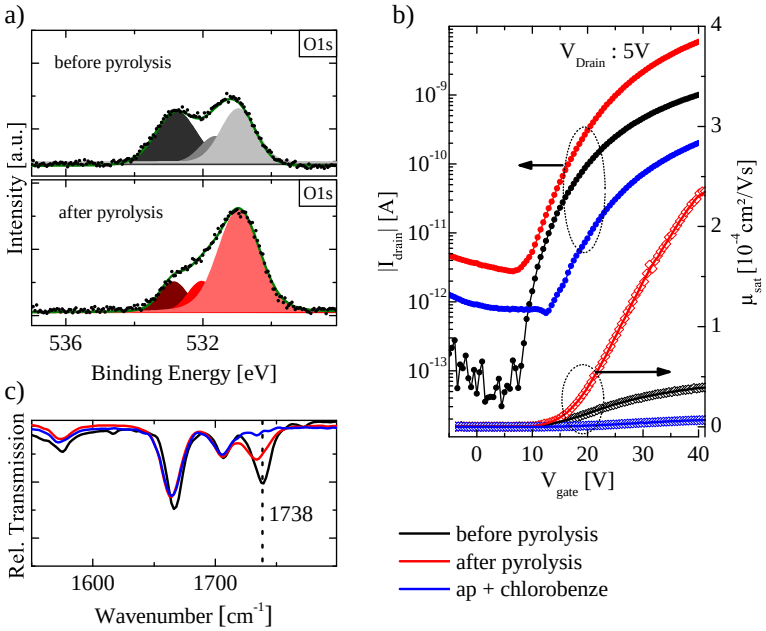


Figure 48: Data survey Thersol 3. (a) PES signal of the O1 s orbital before and after the pyrolysis procedure; (b) OFET devices with Thersol 3 semiconductor before and after the pyrolysis, as well as after an additional washing procedure with the original solvent chlorobenzene; (c) IRRA spectra of the C=H stretching vibrations before and after the pyrolysis, as well as after an additional washing procedure with the original solvent chlorobenzene.

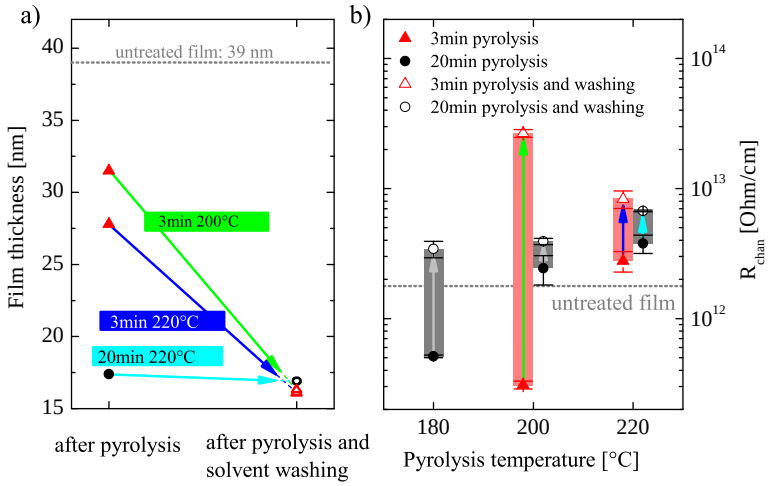


Figure 49: Thersol 3 film properties in dependence of pyrolysis parameters and influence of subsequent solvent washing. (a) Film thickness after pyrolysis and after post-pyrolysis solvent washing; (b) channel resistance of OFET devices after pyrolysis and after post-pyrolysis solvent washing, plotted against temperature of the applied pyrolysis procedure.
The arrows indicate the change due to solvent washing from closed (before washing) to open (after washing) symbols in both plots. Pyrolysis duration is indicated by the symbols shape and color. Arrow colors green, blue and light blue allow for an easier assignment of the respectively applied pyrolysis-parameters between the two graphs.

dure; apparently the outgassing of residual side-chains is completed. In contrast, Thersol 1 and Thersol 3 show remaining intensities of the side-chain associated peak in the IRRA characterization, which disappear upon a subsequently applied washing procedure. OFET devices with Thersol 3 as the semiconductor exhibit a performance increase due to the pyrolysis, but a significant decrease after the solvent washing, resulting in a lower performance than the untreated film (figure 44b). The connection of side-chain outgassing, electrical performance and heating/washing treatments are therefore investigated in more detail with Thersol 3.

6.2.1 *Thickness reduction upon pyrolysis and solvent washing*

In figure 49a, film thickness measurements via ellipsometry of equally

deposited, but differently treated Thersol 3 layers are presented. The original film thickness of 39 nm is reduced to $\sim$ 17 nm after pyrolysis and subsequent washing in all samples, regardless of duration and temperature of the pyrolysis procedure. This is consistent with IRRAS results, which suggest that all side-chains are removed after the solvent washing. Between pyrolysis and washing, however, the film thickness varies for the three different pyrolysis parameter-sets: higher temperature and longer duration causes a stronger thickness reduction. This suggests, that the decomposition of the carbonate linker group and the removal of the detached side-chains are two independent processes, which happen on different timescales. While the cleavage of the linker is completed after pyrolysis in all observed cases, temperature driven outgassing from the film is not. A schematic illustration of the stepwise thickness reduction from heating and washing is given in figure 50. Different thermal annealing results in different thickness due to the side-chain residuals (figure 50b). After subsequent washing, both films are free of residuals from the pyrolysis and exhibit the same final layer thickness (figure 50c).

6.2.2 *Channel resistance upon pyrolysis and solvent washing*

The electrical performance of the differently treated films is characterized via the channel resistance, determined with the TLM as described in section 2.2.2.2. This parameter is especially suited here, in order to determine the semiconductor's resistivity independently from potentially correlated charge injection properties. A plot of channel resistance in dependence of the pyrolysis temperature with and without post-pyrolysis washing is presented in figure 49b. The arrows in figure 49b indicate the change in channel resistance upon washing. They point upwards towards higher resistances, regardless of pyrolysis temperature and duration. With respect to the untreated reference devices, all treatment procedures result in a higher resistance after the washing, i.e. lower electrical performance. In some of the pyrolysed but unwashed devices, which according to IRRAS and thickness data still contain separated alkyl-groups, the performance is increased with respect to the untreated reference. In these devices, however, the performance drop upon subsequent washing is most pronounced. Interestingly, the performance of the semiconductor after the washing, although having the same film thickness and being completely free of side-chain residuals, varies significantly for the different pyrolysis parameters in the intermediate step. In other words, it makes a big difference whether the side-chains are removed during the thermal treatment or by the subsequent washing step.

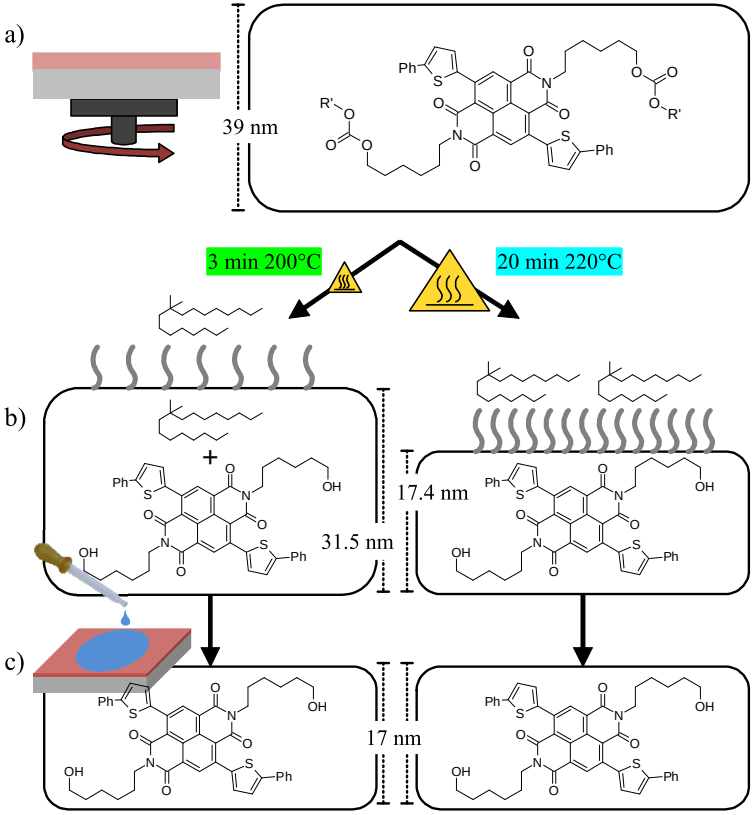


Figure 50: Schematic illustration of the detached alkyl chain residuals in the Polymer 3 films and their influence on the film thickness. (a) Untreated spin coated film; (b) films after pyrolysis with low and high thermal load; (c) resulting film without alkyl residuals after subsequent solvent washing.

6.2.3 *Morphology, π-delocalization and electrical performance*

One possible explanation for this behavior is based on morphology changes induced by the detached side-chains and their removal. Intrinsically, conjugated carbon systems tend towards a planar configuration. Distortions or kinks within the conjugated chain of a polymer disrupt the π-bonding and hence reduce the degree of intramolecular charge delocalization [141, 142, 143]. The detached alkyl-chains in pyrolyzed Thersol films can act as flexible spacers and support a relaxation of the polymer backbone towards the preferred planar configuration, facilitating electrical transport properties. Washing out the remaining chains from the film subsequently at room temperature increases the mechanical tension on the polymer's backbone, causing the device performance drop due to reduced intramolecular charge delocalization. If the thermal load is, on the other hand, sufficient to outgas the separated chains from the film, the polymer relaxes at high temperature to a stable configuration. This yields OFETs which exhibit a lower performance than those with uncompleted outgassing initially, but experience a smaller drop in performance upon subsequent solvent washing.

Furthermore, figure 49b reveals a general trend towards higher channel resistance with increasing pyrolysis temperature. Considering the comparably high temperatures up to 220 °C, this behavior presumably marks the beginning of thermal damage to the polymer backbone. For an application of such a stimulated solubility reduction material, the pyrolysis procedure must be balanced thoroughly to ensure linker group cleavage and completed side-chain removal with controlled final film morphology, but at the same time minimum thermal damage to the electrically active part.

Part III

CONCLUSION

7 SUMMARY AND CONCLUDING DISCUSSION

In the present work, solution processed FETs from organic polymers were investigated. The scope of the work included performance optimization via improved charge carrier injection by SAMs at the metal-semiconductor interface, and the passivation of trap states at the interface of organic to inorganic materials. Furthermore, novel semiconductors were characterized, which can be reduced in their solubility after deposition.

Injection barrier reduction with SAMs

THE ACCUMULATION behavior, and the connection between SAM *quality* and *functionality* as injection layer was investigated using the commercially available SAM-forming molecule PFDT. It was found, in agreement to Karpovich and Blanchard [72], that the surface coverage is correlated to both, the immersion time in solution and the precursor concentration. Increasing the concentration, the SAM reached almost full functionality in immersion time as short as five seconds, and was not compromised due to processing in ambient conditions. Such a simple and fast deposition procedure is suited to be applied at high throughput in a large scale.

The time consuming final ordering of the molecules could not be accelerated by means of an increased concentration, however, the performance benefit from it was found to be comparably small. It is important to note that the time duration of surface coverage and, even more so, that of the orientation depends on the specific chemical structure of the applied molecule, and cannot be generalized without restrictions. SAM-forming molecules with perfluorinated tail-group seem to be especially well suited for fast deposition, because they exhibit no initial "lying down phase" [60] as alkanethiols do. Instead, PFDT molecules exhibit, with an average angle of $\sim 18°$ to the surface normal as calculated from IRRAS, already a rather upright orientation at sub-monolayer coverage. At the same time, the direction of the molecular dipole is predetermined from a perfluorinated tail-group: such SAMs can shift the workfunction of metals only towards higher values.

The influence of ambient exposure during the SAM deposition was found to be insignificant for immersion times below a minute. For pro-

longed immersion under ambient conditions, a decrease in the achieved workfunction shift was observed. After one day of immersion, the resulting workfunction was shifted back to its original value, and even longer immersion leads to a strong reversal shift in the opposite direction. While this is a novel insight from a scientific perspective, it does not cause any restraints for application, since short immersion times would be preferred in an industrial fabrication anyway. The reason for this reversal shift was identified as a chemical reaction of the PFDT molecule with ambient oxygen. This reaction occurs while the molecule is already attached to the surface and does not cause its desorption, so it could potentially be exploited to tune the resulting workfunction shift to a specific value. In the unbound condition, the exposed thiol binding group is susceptible to oxidation, which destroys its ability to engage with the surface in the first place. Therefore, thiolated SAM-forming molecules and precursor solutions need to be stored in an oxygen-free environment in any case.

A NOVEL SAM-FORMING MOLECULE named Juls which is very robust against oxidation and shifts the workfunction towards higher values was presented and characterized. It contains a stable disulfide linker instead of the reactive thiol group, and was stored in solid form under ambient conditions for more than two years without recognizable loss in performance. The solubility of Juls in ethanol is comparably low and the maximum concentration is therefore fundamentally limited. Minimum immersion times of one minute were necessary to cast optimized SAMs. While this is considerably longer than the shortest times achieved with PFDT, it is still fast with respect to common standard SAM procedures. The workfunction shift that was achieved with Juls is among the strongest reported for SAMs up to date, and matches that of widely used PEIE, without its drawbacks. Another beneficial feature which has been demonstrated for Juls and PEIE alike, is the protection of coated silver electrodes from degradation, caused by storage of the devices in ambient atmosphere and reflected in an increasing contact resistance. Although the contact resistance exhibits the same trend for these two injection layers over the course of three months, the Juls treated transistor performed much more stable after such long storage.

The Juls SAM was also used to investigate unipolar transistors from a single active material, determined via the presence or absence of an injection-layer. For now, the choice of semiconductors that exhibit balanced and high mobility for charge carriers of both polarities is limited. PDTDPP-alt-BTZ, a material that shows great promise in this regard [108], was used in OFETs with pristine- and Juls-treated metal contacts.

It was found that equivalent p- and n-type transistors with a distinct off-state for sufficiently low operation voltages, and low threshold voltage can both be realized with PDTDPP-alt-BTZ, differentiated by the injection treatment. On the other hand, the high operation voltages of ± 60 V, that were used by Cho et al. [108], proved to be necessary to fully exploit the field-dependent maximum mobility. Additionally, the electron mobility of PDTDPP-alt-BTZ decreased upon electrical stress during operation, rendering this exact polymer rather a proof of concept than a viable option for industrial application. Yet, these shortcomings in performance and stability are not of fundamental nature and it seems realistic that they can be overcome, considering recent progress in the design of ambipolar semiconductors [144, 145] and the virtually unlimited variety of molecules.

Interface trap state passivation

The usage of ParyleneC as a highly controlled, easily processable interlayer with exceptional film-forming properties at the interface between inorganic and organic layers was investigated for the example of PTAA and SiO_2. Energy states at this interface, which can immobilize charge carriers and severely compromise device performance, were successfully passivated against the OFET channel by a thin, conformal ParyleneC coating. In contrast to surface treatments with OTS and HMDS, that are typically applied for this purpose, thin layers of ParyleneC exhibited a good wettability for polar and non-polar solvents, facilitating the deposition of a subsequent layer from solution.

A steady drift of the onset voltage was, however, observed with persistent electrical stress at the gate electrode. It was found that this behavior results from negative charges which diffuse through the ParyleneC and become trapped in the SiO_2, at a rate too slow to be observable in a single gate-voltage sweep. An increasing number of immobilized charges in the SiO_2, accumulated over the course of several successive sweeps, can attract enough mirror-charges inside the transistor channel to cause an offset in the electrical field, and therefore a visible shift in the onset voltage. The severity of this effect was reduced with increasing film thickness of the ParyleneC passivation layer.

It was found in an investigation of the behavior with rising temperature, that the onset voltage shift increased initially, up to a temperature of $\sim$ 60 °C, and decreases again with further increasing temperature. The latter effect is consistent with thermal depletion of filled trap states in the SiO_2 layer. The initial rise in the amount of trapped charges with temperature, on the other hand, could reflect a reduced permeation bar-

rier of the ParyleneC. After this thermal treatment, however, the rate of charge accumulation upon electrical stress was reduced dramatically.

In conclusion, the usage of ParyleneC seems certainly viable for its chemical composition at the interface to an organic semiconductor and offers beneficial wetting behavior for solution processing at the same time. On the downside, its permeability for charge carriers is finite. The resulting slow and steady bias stress effect can be suppressed by an adequate film-thickness and thermal curing. Potentially, however, the effect might even be exploited for its memory effect on both, the electrical and the thermal history.

Thermally induced solubility reduction

Furthermore, semiconducting polymers with thermally induced solubility reduction were investigated. The functionality was realized via cleaveable carbamate- or carbonate linker-groups at which solubility providing alkyl side-chains are connected to the polymer backbone. Three derivatives (Thersol 1-3), differing in the placement and composition of side chains at the backbone after linker decomposition, were processed in OFET devices in both forms, before and after the thermal pyrolysis. It was found that in all three cases the device performance increased with respect to the untreated films. Analytical investigations of the thin films by IRRAS and PES suggests, that residual contaminations of loose detached alkyl-chains remain within the film in two of the three studied examples. These contaminations could be removed completely by a subsequent washing procedure applied to the pyrolyzed films, however, associated with a severe degradation in electrical performance.

A detailed investigation with varied pyrolysis parameters time and temperature, probing for the impact of subsequent solvent washing, was performed with Thersol 3. It was found that it plays a decisive role for the channel resistance in the device, whether the detached side-chains are removed during the pyrolysis or during washing, despite the fact that chemical composition and film thickness were found to be identical via IRRAS and PES. An explanation that is consistent with all the data in this work is related to morphology changes upon side-chain removal. Loose side-chain contaminations in the film can act as spacers and facilitate the polymers relaxation at pyrolysis temperatures to align with a planar backbone, which is energetically favored and provides intramolecular charge delocalization [141, 142, 143]. Their removal via solvent washing at room temperature, however, can cause a porous framework with high internal mechanical tension, limiting intramolecular charge delocalization. Thorough side-chain removal in a prolonged

pyrolysis procedure on the other hand, enables a relaxed backbone configuration at high temperatures in absence of loose alkyl spacers. Although this configuration is less optimized, it is comparably unaffected by subsequent exposure to the original solvent.

Purely morphological variations can cause the channel resistance of an OFET to differ by an order of magnitude. This outlines the complicated connection between morphology and charge transport in soft van-der-Waals governed materials. At the same time, it illustrates that the development of organic semiconductors has plenty of ground left to cover.

Conclusion

In the present thesis, different ways to alter and optimize the performance and processability of TFT from organic semiconductors have been applied and investigated. The well established technique of injection barrier treatment with SAMs was found to be applicable with drastically reduced processing times of five seconds, in order to meet industrial requirements on processing speed if process parameters are chosen carefully. A novel SAM-forming molecule with a strong molecular dipole was introduced, that changes the WF of metals by 1.2 eV towards lower values and prevents the degradation of electrodes inside a device. It was shown that injection layers from this SAM can be used to produce selective unipolar transistors from a single ambipolar organic semiconductor. Transistors with SiO_2 dielectric layers, covered by a ParyleneC coating, were investigated. It was demonstrated that the resulting chemical composition in the channel is determined by the ParyleneC, and charge carrier traps from the SiO_2 are passivated. A slow, but steady bias stress effect due to permeation of charges into the SiO_2 could be adjusted via ParyleneC layer thickness and thermal curing. Furthermore, novel semiconducting polymers with reduceable solubility were implemented in OFET devices. Such materials enable successive solution-processing of multiple layers from the same solvent. It was found that the channel resistance of OFET devices can differ by one order magnitude, depending on the removal process of the detached side-chains.

The example of the Thersol polymers showed how critically the electrical performance of organic semiconductors depends on the morphology, which in turn depends in a complex way on the processing. The performance of a transistor device at the same time, depends not only on properties of the single materials, but also on the interfaces between them, since they can provide contact resistances and charge trapping sites. Additionally, all layers in a thin film device, including electrodes,

semiconductors, gate dielectrics and surface coatings that address certain interface issues, represent at the same time a printing substrate for the subsequent layer. The wetting properties and processing compatibility of these films therefore need to be considered additionally to the original purpose. In order to exploit the potential of organic electronics, advances in material design and interface tailoring, as well as their interconnection to deposition and processing have to be considered as entangled fields of research. It was demonstrated in this work that bringing them together is a matter of engineering.

APPENDIX

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PUBLICATIONS

JOURNAL PUBLICATIONS (STATUS 19. NOV. 2015)

- M. Alt, J. Schinke, S. Hillebrandt, M. Hänsel, G. Hernandez-Sosa, N. Mechau, T. Glaser, E. Mankel, M. Hamburger, K. Deing, W. Jaegermann, A. Pucci, W. Kowalsky, U. Lemmer, R. Lovrinčić: *Processing follows function: Pushing the formation of self-assembled monolayers to high throughput compatible timescales;* ACS Applied Materials & Interfaces [74].
- S. Hengen, M. Alt, G. Hernandez-Sosa, J. Giehl, U. Lemmer, N. Mechau: *Modelling and simulation of gate leakage currents of solution-processed OTFT;* Organic Electronics [84].
- M. Alt, C. Melzer, F. Mathies, K. Deing, G. Hernandez-Sosa, U. Lemmer: *Adjustable passivation of SiO_2 trap states in OFETs by an ultrathin CVD deposited polymer coating;* Applied Physics A - submitted.
- M. Jesper, J. Schinke, M. Alt, S. Hillebrandt, I. Angelova, V. Rohnacher, A. Pucci, U. Lemmer, W. Jaegermann, W. Kowalsky, T. Glaser, E. Mankel, R. Lovrinčić, F. Golling, M. Hamburger, U. Bunz: *Dipolar SAMs Reduce Charge Carrier Injection Barriers in n-Channel Organic Field Effect Transistors;* Langmuir [146].
- S. Hillebrandt, T. Adermann, M. Alt, J. Schinke, T. Glaser, E. Mankel, G. Hernandez-Sosa, W. Jaegermann, U. Lemmer, A. Pucci, W. Kowalsky, K. Müllen, R. Lovrinčić, M. Hamburger: *Naphthalene tetracarboxydiimide based n-type polymers with thermally cleavable side chains*; Applied Materials & Interfaces - submitted.
- M. Alt, M. Jesper, J. Schinke, S. Hillebrandt, P. Reiser, T. Rödlmeier, I. Angelova, K. Deing, T. Glaser, E. Mankel, W. Jaegermann, A.Pucci, U. Lemmer, U. Bunz, W. Kowalsky, G. Hernandez-Sosa, R. Lovrinčić, M. Hamburger, : *The Swiss-Army-Knife Self-Assembled Monolayer: Improving Electron Injection, Stability, and Wettability of Metal Electrodes with a One-Minute Process;* Advanced Materials - submitted.

PATENTS

- Thermische Abspaltung von löslichkeitsvermittelnden Gruppen bei Polymeren. (filed)
- Austrittsarbeitsänderung durch selbst assoziierte Monolagen polarer Moleküle. (filed)

PRESENTATIONS

- M. Alt, J. Schinke, S. Hillebrandt, M. Hänsel, N. Mechau, G. Hernandez-Sosa, T. Glaser, E. Mankel, W. Kowalsky, A. Pucci, W. Jägermann, K. Deing, U. Lemmer, R. Lovrincic: *Solution processing of self-assembled monolayers in printing relevant timescales*; Talk; LOPEC München 2014.
- M. Alt, J. Schinke, S. Hillebrandt, M. Hänsel, E. Mankel, T. Glaser, R. Lovrinčić, W. Jaegermann and W. Kowalsky; *Multianalytical investigation of SAM formation on printing relevant timescales III: OFET devices*; Talk; DPG Dresden 2014.
- M. Alt, J. Schinke, S. Hillebrandt, M. Hänsel, N. Mechau, G. Hernandez-Sosa, T. Glaser, E. Mankel, W. Kowalsky, A. Pucci, W. Jägermann, K. Deing, U. Lemmer, R. Lovrincic*: Solution processing of self-assembled monolayers as charge injection layers in organic FETs*; Poster; Swiss ePrint 2014.
- M. Alt, J. Schinke, M. Hänsel, G. Hernandez-Sosa, I. Levine, M. Jesper, E. Mankel, M. Hamburger, K. Deing, W. Kowalsky, U. Lemmer, N. Mechau.: *SAM as charge injection layers in OFET - The correlation of accumulation parameters and functionality*; Talk; MRS Spring Meeting San Francisco 2013.

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The only source of knowledge is experience.

— Albert Einstein

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Ich versichere wahrheitsgemäß, die Dissertation bis auf die dort angegebene Hilfe selbständig angefertigt, alle benutzten Hilfsmittel vollständig und genau angegeben und alles kenntlich gemacht zu haben, was aus Arbeiten anderer und eigenen Veröffentlichungen unverändert oder mit Änderungen entnommen wurde.

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