40 GBd 16QAM Signaling at 160 Gbit/s in a Silicon-Organic Hybrid (SOH) Modulator

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***Abstract* — We demonstrate for the first time generation of 16-state quadrature amplitude modulation (16QAM) signals at a symbol rate of 40 GBd using silicon-based modulators. Our devices exploit silicon-organic hybrid (SOH) integration, which combines silicon-on-insulator slot waveguides with electro-optic cladding materials to realize highly efficient phase shifters. The devices enable 16QAM signaling and quadrature phase shift keying (QPSK) at symbol rates of 40 GBd and 45 GBd, respectively, leading to line rates of up to 160 Gbit/s on a single wavelength and in a single polarization. This is the highest value demonstrated by a silicon-based device up to now. The energy consumption for 16QAM signaling amounts to less than 120 fJ/bit – one order of magnitude below that of conventional silicon photonic 16QAM modulators.**

***Index Terms*— Electro-optic modulators, photonic integrated circuits, nonlinear optical devices**

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I. Introduction

FAST and efficient in-phase/quadrature-phase (IQ) modulators are key elements for high-speed links in telecom and datacom networks. [1]. To maximize the data rate that can be transmitted on a single wavelength channel, both large symbol rates and the ability to use higher-order modulation formats are essential [2]. At the same time, minimizing the power consumption of the devices is of utmost importance regarding high-density integration and scalability of interconnect counts.

Silicon photonics is a particularly attractive platform for realizing electro-optic modulators, leveraging mature complementary metal-oxide-semiconductor (CMOS) processing and enabling high-density integration of photonic devices along with electronic circuitry. However, the inversion symmetry of the silicon crystal lattice inhibits electro-optic effects, thereby making high-performance IQ modulators challenging. As a consequence, conventional silicon modulators have to rely on carrier depletion or carrier injection in pn, p-i-n or metal-oxide-semiconductor (MOS) structures [3]–[6]. Using a depletion-type device, generation of quadrature phase shift keying (QPSK) signals was recently shown at a symbol rate of 56 GBd resulting in a total line rate of 112 Gbit/s [7]. However, when using more advanced modulation formats, the achievable symbol rates are still significantly lower – record values amount to 28 GBd demonstrated for dual-polarization 16-state quadrature amplitude modulation (16QAM) [8], which leads to a line rate (net data rate) of 112 Gbit/s (93.3 Gbit/s) encoded on each polarization. The performance of these devices is inherently limited by the underlying depletion-type phase shifters, which exhibit rather low efficiencies with typical voltage-length products $U_\pi L$ of 10 Vmm or more. As a consequence, large drive voltages, on the order of several volts, have to be used, leading to high energy consumption – for 16QAM modulation at 28 GBd, the modulation energy amounts to approximately 1.2 pJ/bit at a peak-to-peak drive voltage of 5 V_{pp} [8]. In addition, phase modulation based on the plasma dispersion effect is inevitably linked to amplitude modulation due to free-carrier absorption. This may eventually hamper the generation

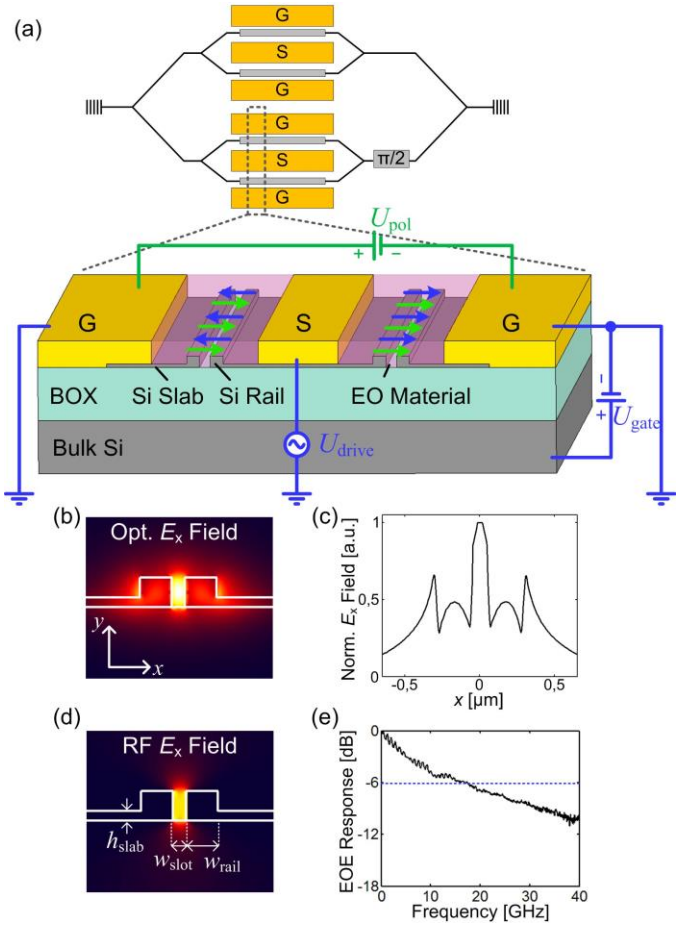

Fig. 1. Silicon-organic hybrid (SOH) modulator. (a). Schematic of the IQ modulator and cross-section of a single SOH Mach-Zehnder Modulator (MZM). The slot waveguides have a rail width of w_{rail} = 240 nm and a slot width of w_{slot} = 80 nm. As an EO cladding, a mixture of the chromophores YLD124 (25 wt.%) and PSLD41 (75 wt.%) is deposited via spin coating. Thin *n*-doped silicon slabs with (h_{slab} = 70 nm) are used to electrically connect the rails to the metal strips of an RF transmission line in a ground-signal-ground configuration. A poling process is used to align the chromophores in both waveguides along the same direction. Operating the device via the GSG transmission line results in opposite phase shifts in the two arms of the MZM (push-pull operation). The π-voltage at DC is U_π = 0.9 V. A gate voltage U_{Gate} between the Si substrate and the SOI device layer improves the conductivity of the silicon slab, resulting in an electro-optic bandwidth of the device of 18 GHz. (b) Contour plot of the normalized E_x component of the optical field in the slot waveguide. (c) Plot of the E_x-component of the optical mode field as a function of the horizontal position x at half the waveguide height (y = 110 nm). Discontinuities of the E_x-component at the slot sidewalls lead to strong field enhancement in the slot. (d) E_x component of the electrical RF drive signal below the *RC* limit. The silicon slabs are doped such that the applied RF voltage drops predominantly across the slot. As a consequence, the RF mode and the optical mode are both well confined to the slot, resulting in strong interaction and hence in an efficient modulation. (e) Measured frequency response of a 1.5 mm-long MZM. The 6 dB electrical-optical-electrical (3 dB electro-optic) bandwidth amounts to 18 GHz.

of advanced modulation formats with high order, where phase and amplitude of the signals have to be controlled independently of one another.

In this paper we show that silicon-organic hybrid (SOH) integration can overcome these limitations. We use silicon-on-insulator (SOI) slot waveguides [9] and combine them with electro-optic (EO) cladding materials to realize Pockels-type phase shifters [10]–[13] . SOH integration enables remarkably small voltage-length products of down to 0.5 Vmm measured

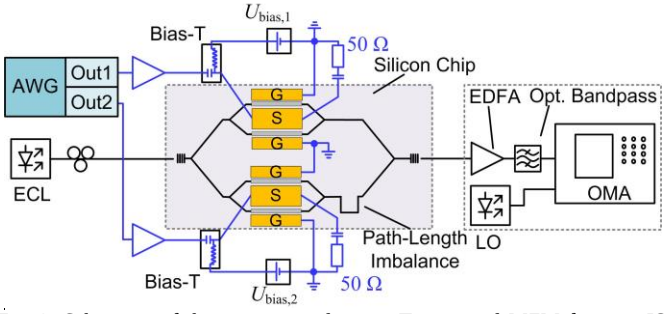

Fig. 2. Schematic of the experimental setup. Two nested MZM form an IQ modulator. An intentional imbalance allows for adjusting the π/2 phase offset of the in-phase (I) and the quadrature-phase (Q) component by wavelength tuning. Electrical multilevel drive signals are generated by a Keysight M8195A arbitrary waveform generator (AWG) operating at 65 GSa/s, the outputs of which are amplified and coupled to the silicon chip via RF probes. Bias-Ts are used to connect a DC voltage for controlling the operation point. The optical output is amplified by an EDFA, bandpass filtered and subsequently fed into an optical modulation analyzer (OMA) for intradyne detection. Standard digital post processing is performed at the OMA for equalization.

at DC [14], and at the same time avoids unwanted amplitude-phase coupling and thereby enables higher-order modulation formats [15], [16]. We demonstrate 16QAM and QPSK signaling at symbol rates of 40 GBd and 45 GBd, respectively, leading to line rates (net data rates) of up to 160 Gbit/s (133.3 Gbit/s) on a single polarization [17]. This is the highest value achieved by a silicon-based modulator up to now. The energy consumption of our 16QAM device is estimated to be 120 fJ/bit at 40 GBd – one order of magnitude better than for best-in-class 28 GBd 16QAM all-silicon modulators. The work builds upon and expands our earlier experiments, where we have demonstrated energy-efficient on-off-keying [18], generation of multi-level amplitude modulation at symbol rates of up to 84 Gbit/s [15] and 16QAM modulation at 28 GBd [19].

II. Silicon-Organic Hybrid Modulator

SOH modulators exploit interaction of the guided light with the electro-optic cladding material under the influence of a modulating RF field. A cross section of an SOH Mach-Zehnder modulator (MZM) is depicted in Fig. 1(a). Each phase shifter consists of a silicon slot waveguide which is covered by the organic EO material. Fig. 1(b) and 1(c) show the optical E_x field. The discontinuity and the high refractive index contrast at the silicon – slot interface leads to a field enhancement within the slot and therefore to a large interaction of the light with the organic EO material [12]. The rails of the slot waveguide have a width of w_{rail} = 240 nm and are connected to a coplanar ground-signal-ground (GSG) transmission line via thin (h_{slab} = 70 nm), slightly conductive, *n*-doped silicon slabs. A voltage applied to the transmission line will drop predominantly across the w_{slot} = 80 nm wide slot, thereby generating a large electric field. A plot of the E_x component of the electrical field can be seen in Fig. 1(d). This configuration ensures excellent overlap between the modulation field and the optical fields, leading to high modulation efficiency. The RF transmission line comprises the metal traces and the silicon slot waveguides and is designed

for a wave impedance of 50 Ω. This is confirmed by measurements – at RF signals of up to 40 GHz, we find wave impedances of 50 ± 5 Ω.

The device was fabricated on an SOI wafer with a 220 nm-thick device layer and a 3 µm-thick buried oxide (BOX) using electron beam lithography for defining the silicon waveguides and optical lithography for the metallization. The chip is coated with a mixture of the electro-optic multi-chromophore dendritic molecule PSLD41 (75 wt.%) and the chromophore YLD124 (25 wt.%) [14], [20]. The cladding material is poled by heating it close to its glass transition temperature while applying a poling voltage across the two floating ground electrodes of each MZM. Half of the voltage drops across each slot, resulting in an orientation of the chromophores in the slot which is antisymmetric with respect to the signal electrode, as indicated in Fig. 1(a) by green arrows. The blue arrows indicate the RF field applied to the GSG electrodes after poling, which results in opposite phase shifts in the two arms of the MZM and enables push-pull operation. For DC fields, the π-voltage of one push-pull MZM amounts to 0.9 V. Taking into account the device length of 1.5 mm, this corresponds to a voltage-length product of $U_\pi L$ = 1.35 Vmm. This is higher than previously published values of SOH devices [14] and is attributed to different device geometry and the resulting difference in poling efficiency. The bandwidth of the SOH devices is dictated by the RC time constant of the slot waveguide: The slot corresponds to a capacitor which is charged and de-charged via the resistive silicon slabs. To increase the conductivity of the slab by a charge accumulation layer and hence to increase the bandwidth, a static gate voltage U_{gate} is applied between the substrate and the top silicon layer [21], Fig. 1(a). A bandwidth measurement of the current MZM results in a 6 dB electrical-optical-electrical (3 dB electro-optic) bandwidth of 18 GHz, see Fig. 1(e), with significant potential for further improvement [22]. The roll-off is relatively smooth and resembles that of an RC low-pass, thereby still allowing 40 GBd 16QAM and 45 GBd QPSK signaling using root-raised-cosine Nyquist pulses.

For practical applications of SOH devices, the long-term stability of the organic cladding is of high importance. Recently novel materials have become available, featuring glass transition temperatures of more than 130 °C while maintaining electro-optic coefficients in excess of 100 pm/V [23]. The investigation of aging and temperature stability of organic EO materials is subject to ongoing research. It can be expected, that the stability of the materials can be further improved by synthetically modified chromophores that bear specific crosslinking agents for post-poling lattice hardening or by increasing the molar mass of the chromophores. The viability of the first approach has been demonstrated for similar EO compounds [24], [25] where material stability of up to 250 °C has been achieved.

III. Experiment

The setup for the modulation experiments is depicted Fig. 2. Two MZM are nested in an on-chip IQ configuration. The parent Mach-Zehnder interferometer features a path length imbalance, which is used to adjust the π/2 phase shift between the I and the Q signal via wavelength tuning. The drive signals for QPSK and 16QAM modulation are generated by a Keysight M8195A arbitrary waveform generator (AWG) operated at 65 GSa/s. We use root-raised-cosine pulses with a roll-off factor of $\beta = 0.35$ to reduce the occupied spectral bandwidth and to exploit the benefits of a matched filter at the receiver. The transmitted data are derived from a pseudo-random bit sequence with a length of 2^{11}-1. After the AWG, the analog signals are amplified to peak-to-peak voltages of approximately 1.8 V_{pp} by two linear RF-amplifiers, which drive the GSG-electrodes of the on-chip IQ-modulator via microwave probes. A 50 Ω termination is used at the end of each transmission line to avoid back-reflection of the RF signal. For each MZM a DC voltage is applied to the device via bias-Ts to set the operating point of the modulator. To improve the bandwidth of the device, a static gate field of E_{Gate} = 0.1 V/nm is applied between the silicon substrate and the device layer. Grating couplers are used to couple laser light at λ = 1550 nm from an external cavity laser (ECL) to the silicon waveguide. After the device, the light is amplified by an erbium doped fiber amplifier (EDFA), followed by an optical band-pass filter (2 nm passband) to suppress out-of-band amplified spontaneous emission (ASE). An optical modulation analyzer (OMA) with two real-time oscilloscopes (80 GSa/s) serves as a receiver. A second ECL is used as a local oscillator (LO) for intradyne reception. Digital post-processing comprising polarization demultiplexing, phase recovery, compensation of the frequency offset between signal and LO, and channel equalization is performed by the OMA. The insertion loss of the silicon chip amounts to 27 dB, where 10 dB – 12 dB are caused by fiber-chip coupling losses. This rather high loss can be significantly reduced in future devices: By employing optimized grating coupler [26] or photonic wirebonds [27], [28] the coupling loss to the fibers can be reduced from 10 dB to less than 4 dB. The current losses of 5 dB in the 9 mm long access strip waveguide can be reduced to below 1 dB by improving the sidewall roughness and reducing the length. The strip-to-slot converters and multimode interference couplers (MMI) are already optimized and contribute only 1 dB to the total loss. To reduce the 11 dB losses of the 1.5 mm long slot waveguide to below 3 dB, asymmetric slot waveguide geometries can be used [29] together with an optimization of the doping profile of the phase shifter sections. We estimate that these measures will permit reducing the total on-chip excess loss of the device to less than 5 dB and the fiber-fiber insertion loss to less than 9 dB.

For testing the performance of the devices, we use QPSK signals up to a symbol rate of 45 GBd and 16QAM signals up to 40 GBd. Measurement of the bit error ratio (BER) allows for direct assessment of the signal quality. However, within our memory-limited record length of 62.5µs, we can only measure a maximum of 2.8×10^6 symbols, which does not allow a measurement of BER smaller than 1×10^{-6}. As a complementary measure of the signal quality, we therefore use the error vector magnitude (EVM_m), which describes the

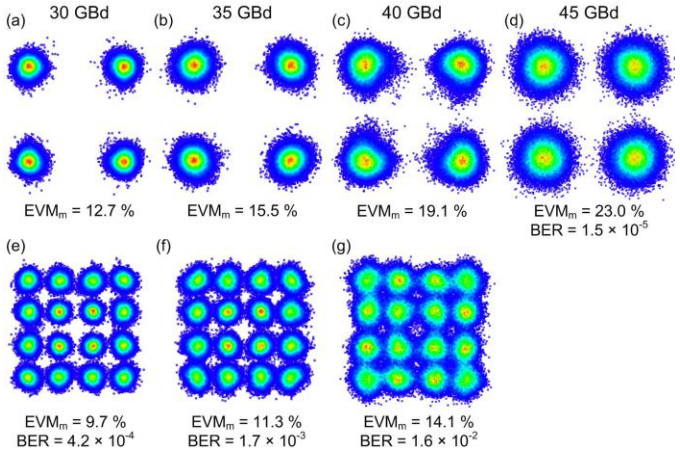

Fig. 3. Optical constellation diagrams. (a) – (d): QPSK signals at 30 GBd, 35 GBd, 40 GBd, and 45 GBd. No bit errors were detected within our record length of 62.5 µs for symbol rates of 30 GBd and 35 GBd, and the error vector magnitude (EVM_m) indicate error free signals with BER < 10^{-9}. QPSK signals at 40 GBd and 45 GBd are well below the threshold for hard-decision FEC with 7 % overhead. At 40 GBd the number of measured errors was not sufficient for a reliable BER estimation, at 45 GBd the measured BER amounts to 1.5×10^{-5}. (e) – (g): 16 QAM signals for 30 GBd, 35 GBd, and 40 GBd. At data rates of up to 35 GBd the measured BER is below the hard-decision FEC threshold. For 40 GBd 16QAM signals, the BER is below the threshold for soft-decision FEC with 20 % overhead.

effective distance of a received complex symbol from its ideal position in the constellation diagram, using the maximum length of an ideal constellation vector for normalization. The EVM_m can be directly translated into a BER assuming the signal is impaired by additive white Gaussian noise only [30]. In our experiment we find a very good agreement between BER values calculated from the EVM_m and the measured BER, supporting our assumption that the channel is limited by Gaussian noise.

Fig. 3 shows constellation diagrams for the various generated signals. In Fig. 3(a) - (d), received QPSK constellation diagrams at data rates between 30 GBd and 45 GBd are depicted. At 45 GBd the EVM_m amounts to 23 % and the measured BER is 1.5×10^{-5}, well below the limit of 4.5×10^{-3} for second-generation hard-decision forward error correction (FEC) with 7 % overhead [31]. At 40 GBd the number of measured errors was not sufficient for a reliable BER estimation. At symbol rates of 35 GBd and below, the QPSK signals can be considered error free: No errors were measureable, and the EVM_m corresponds to a BER well below 1×10^{-9}. The constellation diagrams for 16QAM are depicted in Fig 3(e) - (g). 16QAM signaling is demonstrated up to a symbol rate of 40 GBd. At symbol rates of up to 35 GBd, the measured BER is below the threshold for hard-decision FEC. For 40 GBd, the BER increases significantly, but is still below the threshold of 2.4×10^{-2} for third-generation soft-decision FEC with 20 % overhead [32]. The results of the signal generation experiments are summarized in Fig. 4, where the EVM_m is plotted for different symbol rates. The horizontal dashed lines in Fig. 4 indicate the calculated EVM_m [30] of the various BER threshold levels. For QPSK signals in Fig. 4(a), the dashed line corresponds to the BER of 1×10^{-9}, below that the signals can be considered error free. This applies to the signals measured at 30 GBd and 35 GBd. All other measured

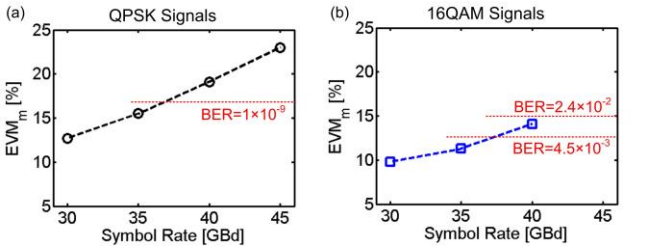

Fig. 4. EVM_m plotted over the symbol rate, in red the corresponding BER [20] is indicated. (a) Plot for QPSK signals. Up to 35 GBd the signal can be considered error free with a corresponding BER < 10^{-9}. The BER limit for hard-decision FEC corresponds to an EVM_m of 38.3 %, outside the range of the plot. (b) Plot for 16QAM signals. The horizontal dashed lines indicate the EVM_m that correspond to the BER thresholds for soft-decision and hard-decision FEC in the case of 16QAM.

QPSK signals are well below the hard-decision FEC limit which corresponds to an EVM_m of 38.3 % and is outside the scale of the vertical axis. For 16QAM signals in Fig. 4(b), the horizontal lines indicate the EVM_m corresponding to the BER thresholds for hard-decision and soft-decision FEC, requiring 7 % and 20 % overhead, respectively. For symbol rates up to 35 GBd the EVM_m is below the threshold for hard-decision FEC; for 40 GBd it is still below the soft-decision threshold, consistent with the directly measured BER indicated in Fig. 3(e)-(g). Using 35 GBd 16QAM signals with hard-decision FEC, the line rate amounts to 140 Gbit/s, and the net data rate amounts to 130.8 Gbit/s. For 16QAM at 40 GBd, the line rate is 160 Gbit/s – the highest value hitherto achieved by a silicon photonic modulator on a single polarization with measured BER figures comparable to those achieved in reference experiments [8]. Taking into account the 20 % overhead for soft-decision FEC coding, the net data rate amounts to the record value of 133.3 Gbit/s. The signal quality in the 40 GBd experiment is limited by the device bandwidth of 18 GHz. We expect that by optimization of the waveguide geometry and of the doping profile in the slabs, the bandwidth of future SOH devices can be significantly increased [22], leading to considerably lower BER.

When using a short SOH modulator at low symbol rates, the device can be operated without a terminal resistance and hence treated as a lumped capacitive load [33]. This is not possible for the high-speed data signals investigated here, for which the symbol duration is of the same order of magnitude as the propagation delay of the RF wave in the device. In this case, we need to model the modulator as a transmission line with a 50 Ω wave impedance, which is fed by a 50 Ω probe and terminated by a matched 50 Ω resistor, Fig. 5. This configuration is equivalent to a single 50 Ω load resistor, which is directly connected to the drive amplifier. The power

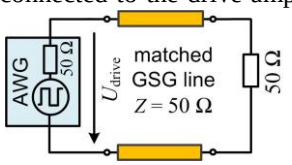

Fig. 5. Equivalent-circuit diagram of one MZM for calculation of the energy consumption. The AWG which drives the MZM is represented by an ideal voltage source and an internal resistance of 50 Ω. The GSG line of the MZM is matched to the 50 Ω output of the DAC and terminated by an external 50 Ω impedance. To estimate the energy consumption, the transmission line and its termination is replaced by an equivalent resistor of R = 50 Ω.

consumption of a single MZM is then given by the power dissipation in this resistor. The output port of the drive amplifier is represented by an ideal voltage source with an internal generator impedance of 50 Ω. The energy per bit for the IQ modulator is obtained by adding the power consumptions of the two MZM and dividing by the total data rate. For 16QAM generation, the electrical drive signal for each MZM consists of two amplitude levels, which differ by a factor of 1/3. Assuming equal probability of the various symbols, the mean power consumption for each MZM can be calculated by averaging over the dissipated power of both amplitude levels. The energy per bit $W_{\mathrm{bit,16QAM}}$ is then obtained by taking into account the power consumption of both MZM and by dividing by the data rate. Denoting the peak-to-peak voltages at the input of the $R = 50\ \Omega$ device as U_{d}, this leads to

$$W_{\mathrm{bit,16QAM}} = 2\times\frac{1}{2}\left[\left(\frac{U_{\mathrm{d}}}{2}\right)^2\frac{1}{R}+\left(\frac{1}{3}\frac{U_{\mathrm{d}}}{2}\right)^2\frac{1}{R}\right]\times\frac{1}{r_{\mathrm{16QAM}}}. \quad (1)$$

For $U_{\mathrm{d}} = 1.80$ V and a data rate of $r_{\mathrm{16QAM}} = 160$ Gbit/s, the energy consumption of the modulator is hence found to be 113 fJ/bit. This is one magnitude below current all-silicon 16QAM modulators [8], but still significantly higher than the energy consumption of a 28 GBd, 16QAM SOH device, for which 19 fJ/bit have been demonstrated [19]. It is the goal of ongoing research activity to further decrease the power consumption at high symbol rates.

IV. Summary

We experimentally demonstrate that SOH integration is capable of boosting data rates and energy efficiency of silicon-based IQ modulators to unprecedented values. We show 16QAM modulation at 40 GBd, resulting in line rates (net data rates) of 160 Gbit/s (133.3 Gbit/s), and QPSK modulation at 45 GBd, leading to 90 Gbit/s (84 Gbit/s). For 16QAM, the energy consumption is as low as 113 fJ/bit - an order of magnitude below that of comparable all-silicon devices.

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