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An Ultra-Efficient Maximum Power Point Tracking Circuit for Photovoltaic Inverters

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***Abstract*—This paper deals with a new ultra-efficient circuit for the individual maximum power point (MPP) tracking of an unlimited number of photovoltaic strings. The circuit generates a DC output voltage and can be combined with common DC-AC solar inverter circuits. The necessary blocking voltages of the transistors are far below the maximum string voltages, which yields to low losses and small passive components. An appropriate controller structure is developed and a prototype is built up, that reaches a maximum efficiency of 99.85 percent.**

Keywords—DC-DC power converters; Maximum power point trackers

I. Introduction

Large photovoltaic installations are often built up with central inverters that are fed by several strings. If the DC lines are combined with string diodes or fuses [1], every string runs at the same voltage and partial shading can lead to a significant power loss of the affected string. The usage of multiple boost converters or electrically isolated converters [2] at the DC-side allows an individual MPP-tracking of every string but causes additional costs and losses. Further solutions are multiple-input-single-inductor buck converters [3], multiple-input-single-inductor buck-boost converters [4, 5] or multiple-input flyback converters [5].

Indeed, a converter input voltage range down to 0V is usually not necessary for a reasonable operation. Fig. 1 shows exemplary power curves of three strings with the same electrical configuration. One of them is unshaded and two are partially shaded. Assuming, that the strings are combined with a three-input DC-DC converter, an input voltage range that reaches from $u_{G,min}$ to $u_{G,max}$ is absolutely sufficient to operate all strings at their MPP.

This paper investigates a new circuit (Fig. 2), which is basically described in [6]. In this circuit, the switched voltages are reduced to about $u_{G,max} - u_{G,min}$. This leads to very low losses and small passive components. Additionally, the circuit allows the buffering of 100Hz / 120Hz components at the DC-side, when a single-phase inverter is connected [6].

Another circuit with similar function is described in [7]. The voltages that have to be switched in that circuit are also below the maximum string voltage $u_{G,max}$ at its MPP, but not as low as in the proposed circuit of Fig. 2.

The proposed circuit contains N input half-bridges that are built up with two MOSFETs T1x and T2x ($x \in \{1..N\}$). Furthermore, every input needs a capacitor C4x and an inductor L1x. The MOSFETs T3 and T4 of the output half-bridge, as well as the capacitor C1, are only needed once. The input voltages u_{Gx} can be controlled in the range $\overline{u}_H \le u_{Gx} \le \overline{u}_H + u_{C1}$, where $\overline{u}_H$ is the mean value of the pulsed voltage u_H during one pulse-period. $\overline{u}_H$ can be chosen freely, what allows a movement of the voltage range, that is marked gray in Fig. 1. An inverter that is connected between the terminals A+ and A- is fed by the circuit with a DC voltage u_A. Neglecting losses, the mean value of the voltage u_A is always between the lowest string voltage $u_{G,min}$ and the highest string voltage $u_{G,max}$.

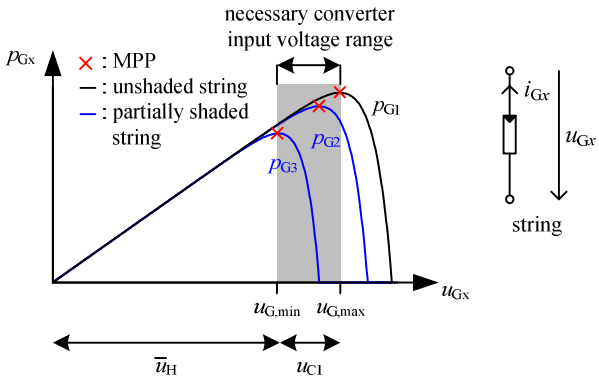


Fig. 1. Power of unshaded and partially shaded strings and necessary converter input voltage range; Model parameters are taken from Table 2 of [8]

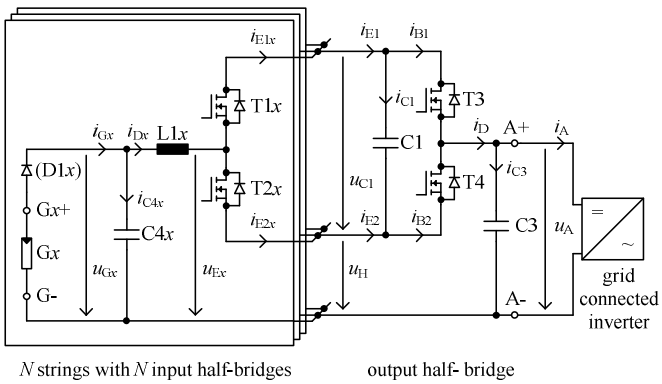


Fig. 2. The new MPP tracking circuit (see also [6])

The circuit is compared with conventional boost converters in Section II and described in detail in Section III. A cascaded control scheme is developed in Section IV. Prototype measurements show the proper function and the very high efficiency in Section V.

II. Comparison with conventional boost converters

The total switched power P_{sw} of the proposed circuit (Fig. 2) is calculated with equation (1) by summing the products of drain-source voltage and drain current of every transistor. The inductor currents i_{Dx} are assumed as DC currents without ripple and $i_{G,max}$ is the maximum expected current of the strings. The voltage at the capacitor C1 is set to $u_{C1} = u_{G,max} - u_{G,min}$.

$$P_{sw,MPPTC} = N \cdot 4 \cdot \left(u_{G,max} - u_{G,min}\right) \cdot i_{G,max} \qquad (1)$$

The proposed circuit is now compared to a conventional solution with boost converters for the individual control of N string voltages (Fig. 3).

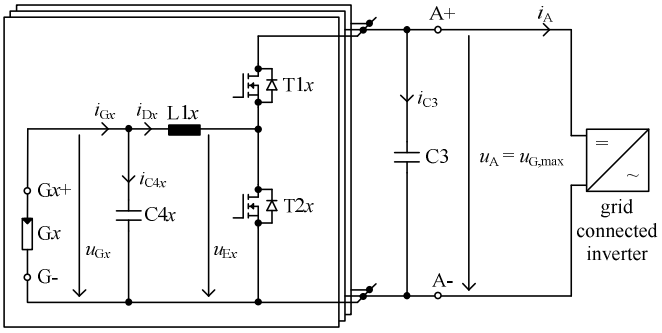


Fig. 3. Conventional solution with boost converters

The total switched power of the conventional circuit (Fig. 3) is given by the following equation:

$$P_{sw,boost} = N \cdot 2 \cdot u_{G,max} \cdot i_{G,max} \qquad (2)$$

A low value of P_{sw} usually leads to low losses and low semiconductor costs. As long as the difference $u_{G,max} - u_{G,min}$ is smaller than 50% of $u_{G,max}$, the total switched power of the proposed MPP tracking circuit is lower than the total switched power of the conventional circuit with boost converters. This condition is usually fulfilled in photovoltaic applications.

III. Function of the new MPP tracking circuit

The transistors T1x and T2x (Fig. 2) are controlled by a pulse width modulation (PWM) with a duty cycle of a_{Dx} and a switching frequency of f_{sw}:

$$T_{T1x} = a_{Dx} \cdot \frac{1}{f_{sw}} \quad | \quad T_{T2x} = (1 - a_{Dx}) \cdot \frac{1}{f_{sw}} \qquad (3)$$

The input current i_{Gx} of each half-bridge is split into the currents i_{E1x} and i_{E2x} by T1x and T2x. Their mean values during one pulse-period are:

$$\bar{i}_{E1x} = a_{Dx} \cdot i_{Gx} \quad | \quad \bar{i}_{E2x} = (1 - a_{Dx}) \cdot i_{Gx} \qquad (4)$$

All N input half-bridges can be modeled as one equivalent input half-bridge according to Fig. 4 with the equivalent voltage u_G and the equivalent currents i_G and i_D. These values are needed later in the control system. The current i_G is the sum of all input currents i_{Gx}, while i_D is the sum of all inductor currents i_{Dx}.

$$i_G = \sum_{x=1}^{N} i_{Gx} \quad | \quad i_D = \sum_{x=1}^{N} i_{Dx} \qquad (5)$$

The equivalent voltage u_G, which is always between the lowest string voltage $u_{G,min}$ and the highest string voltage $u_{G,max}$, is determined with the assumption that all powers $p_{Gx} = u_{Gx} \cdot i_{Gx}$ sum up to the equivalent power $p_G = u_G \cdot i_G$:

$$u_G = \frac{p_G}{i_G} = \frac{\sum_{x=1}^{N} p_{Gx}}{i_G} = \frac{\sum_{x=1}^{N} u_{Gx} \cdot i_{Gx}}{i_G} \qquad (6)$$

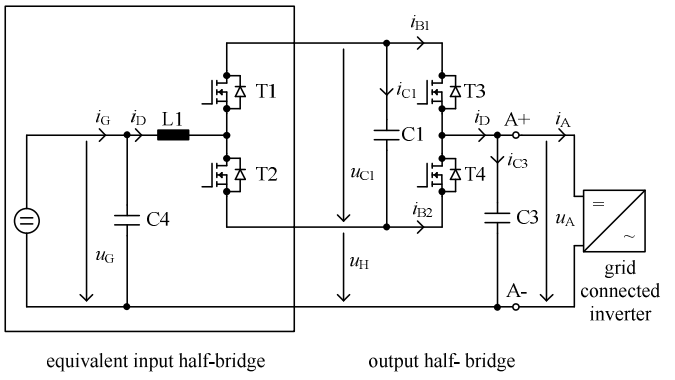


Fig. 4. Equivalent circuit with equivalent input half-bridge

The currents i_{B1} and i_{B2} are combined by the output half-bridge, consisting of T3 and T4. The two MOSFETs are controlled by a PWM modulation with the duty cycle a_F:

$$T_{T3} = a_F \cdot \frac{1}{f_{sw}} \quad | \quad T_{T4} = (1 - a_F) \cdot \frac{1}{f_{sw}} \qquad (7)$$

In stationary operation, the mean output power $\overline{p}_F = u_A \cdot \overline{i_D}$ is the input power $p_G = u_G \cdot i_G$ minus the circuit losses. The output current i_A equals the mean value of i_D and equals i_G. Therefore, the output voltage u_A is approximately u_G.

$$i_A = \bar{i}_D = i_G \quad | \quad u_A \approx u_G \qquad (8)$$

As consequence, the inverter is fed with a voltage u_A, that can vary approximately between the lowest string voltage $u_{G,min}$ and the highest string voltage $u_{G,max}$. Boosting above $u_{G,max}$ is not possible. This is no disadvantage, as most inverter topologies can be operated with variable DC input voltages.

The voltage u_{C1} can be controlled to approximately $u_{G,max} - u_{G,min}$ when the circuit is operating. This leads to low switching losses at T1x - T4 due to the low switched voltages [9] and to small inductors L1x.

Basically, the semiconductors T1x - T4 and the capacitor C1 can be dimensioned for lower voltages than the maximum

expectable string voltages [6]. This allows the usage of fast-switching MOSFETs with very low $R_{DS(on)}$. Furthermore, semiconductors with lower blocking voltage and same current capability are often cheaper than types with higher blocking voltage. However, measures against overvoltage of u_{C1} have to be taken in this case. When the strings are connected between G*x*+ and A- before the control system is active, C1 and C3 act as capacitive voltage divider. Therefore, the ratio of C1 and C3 has to be chosen considering the maximum voltage u_{C1}. The control system of the inverter can be supplied directly from the strings (G*x*+ / G-) and not from A+ / A- to prevent C1 from charging by discharging C3. Alternatively, T2x or T3 could be realized as depletion MOSFETs that are conducting as long as the control system is not active. If external short circuits between G*x*+ and G- can occur, measures against negative currents i_{Gx} have to be taken. This can be done e.g. by string interrupting relays or diodes D1*x*. Since only DC currents are flowing through D1*x*, cheap and slow rectifier diodes with low forward voltage are advantageous.

The semiconductors T1*x* - T4 and C1 can also be dimensioned for the maximum expectable string voltages. In this case, no additional measures against overvoltage of u_{C1} are needed. Nevertheless, the voltage u_{C1} can be controlled to approximately $u_{G,max} - u_{G,min}$ when the circuit is operating, which is advantageous for low switching losses and small inductors L1x.

Additionally, the circuit is capable of buffering pulsating energy, which occurs when a single-phase inverter is connected. The input voltages u_{Gx} can be held constant, while a high voltage ripple on u_A is permissible. This allows the use of a small film capacitor C3 with long lifetime. The voltage u_A can temporarily exceed $u_{G,min}$ and $u_{G,max}$ if u_{C1} is chosen higher than $u_{G,max} - u_{G,min}$.

IV. Cascaded Control Scheme

A cascaded control scheme has been developed for the MPP tracking circuit. The circuit contains $2N + 2$ components that store energy:

- *N* capacitors C4*x*
- *N* inductors L1*x*
- Capacitor C1
- Capacitor C3

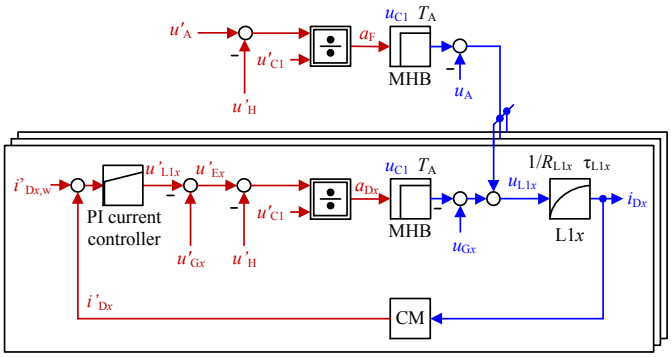
For control purposes, the following values need to be measured:

- *N* input voltages u_{Gx}
- *N* inductor currents i_{Dx}
- Capacitor voltage u_{C1}
- Output voltage u_A

The cascaded control scheme requires the following reference values:

- *N* input reference voltages $u_{Gx,w}$
- Reference capacitor voltage $u_{C1,w}$

The currents i_{Dx} of the inductors L1*x* are set with *N* inner current controllers. The currents i_{Dx} are used to control the *N* string voltages u_{Gx} in an outer voltage control loop. The output voltage u_A is controlled with the active power component of the inverter. Last, the capacitor voltage u_{C1} is controlled by an outer voltage control loop, which uses the output voltage u_A as degree of freedom. The *N* inner control loops for the currents i_{Dx} are shown in Fig. 5. Values that occur physically are drawn in blue. Values that occur in the control system are drawn in red and marked with ‘. All values are mean values during one pulse-period.



MHB: MOSFET half-bridge
CM: current measurement

Fig. 5. Inner current control structure for i_{Dx}

The *N* inductors L1*x* are modeled as first order lag element, which allows the consideration of a series resistance R_{L1x}. The voltages u_{L1x} at the inductors L1*x* are given by:

$$u_{L1x} = u_{Gx} - a_{Dx} \cdot u_{C1} + a_F \cdot u_{C1} - u_A \qquad (9)$$

The upper part of Fig. 5 calculates the duty cycle a_F for the output half-bridge and is only needed once. a_F depends on the reference value u'_H, which equals the mean value $\overline{u}_H$ of u_H. The condition $u'_H \leq u_{G,min}$ has to be maintained when u'_H is chosen. The *N* output values u'_{L1x} of the current controllers influence the duty cycles a_{Dx}. The values u_{Gx}, u_{C1} and u_A are measured and fed-forward. A delay time of T_A is caused by the calculations in the control system.

Standard PI current controllers are usually sufficient for three phase inverters. For higher dynamic requirements or single phase inverters with pulsating voltages u_A, state controllers according to Fig. 6 [10, 11] are advantageous. Measures against wind-up have to be considered in all controllers with integrating component.

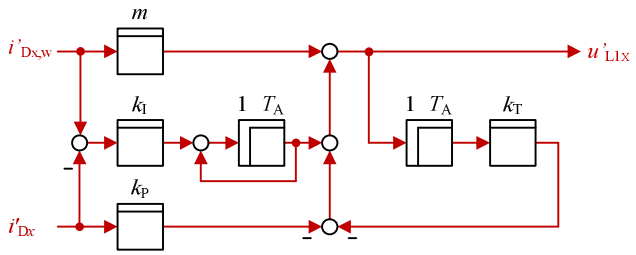


Fig. 6. Current state controller with integrating component for i_{Dx} [10, 11]; simplified diagram; parameters can be found in [11]

The string voltages u_{Gx}, which occur at the capacitors C4x are controlled with N outer voltage controllers according to Fig. 7. The capacitor currents i_{C4x} are given by:

$$i_{C4x} = i_{Gx} - i_{Dx} \tag{10}$$

As the input currents i_{Gx} are not measured, they cannot be fed forward. This leads to PI voltage controllers.

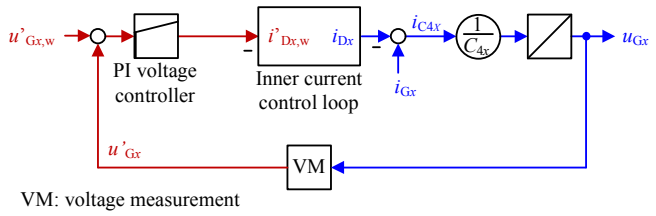


Fig. 7. Outer voltage control structure for u_{Gx}

The PI voltage controllers are fed with reference values $u'_{Gx,w}$ from standard MPP tracking algorithms (Fig. 8, e.g. perturb and observe algorithms).

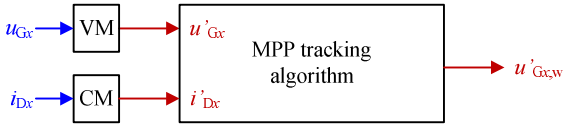
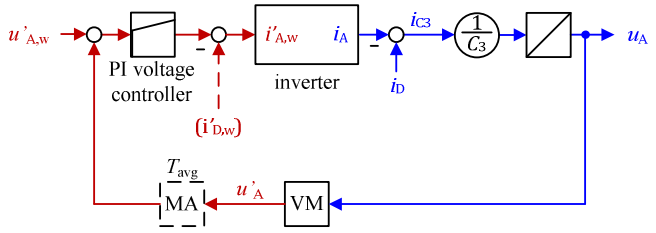


Fig. 8. MPP tracking algorithm

The output voltage u_A is controlled with the active power component, delivered to the grid by the inverter. An appropriate controller structure is shown in Fig. 9. The reference value $i'_{A,w}$ of the DC current i_A is used within the inverter for the control of the active AC current at the output. The value $i'_{D,w}$ can be calculated with (11) and fed forward. Single-phase inverters lead to a voltage ripple on u_A with double output frequency. An optional moving-average filter with an averaging time of $T_{avg} = 1 / (2 \cdot f_{grid})$ suppresses this ripple.



MA: moving average filter

Fig. 9. Control structure for u_A

$$i'_{D,w} = \sum_{x=1}^{N} i'_{Dx,w} \tag{11}$$

Last, the capacitor voltage u_{C1} has to be controlled. The sum power p_D at the input of the MPP tracking circuit is given by:

$$p_D = u_G \cdot i_D \tag{12}$$

The power p_F at the output of the circuit is:

$$p_F = u_A \cdot i_D \tag{13}$$

Neglecting losses, the difference of these powers occurs at the capacitor C1:

$$p_{C1} = p_D - p_F \tag{14}$$

The capacitor current i_{C1} and therefore p_{C1} have to be zero at stationary operation:

$$u_{C1} = \frac{1}{C_1} \int i_{C1} dt = \frac{1}{C_1} \int \frac{p_{C1}}{u_{C1}} dt \tag{15}$$

The output voltage u_A is a degree of freedom and can be used to control u_{C1}. An appropriate control structure is shown in Fig. 10.

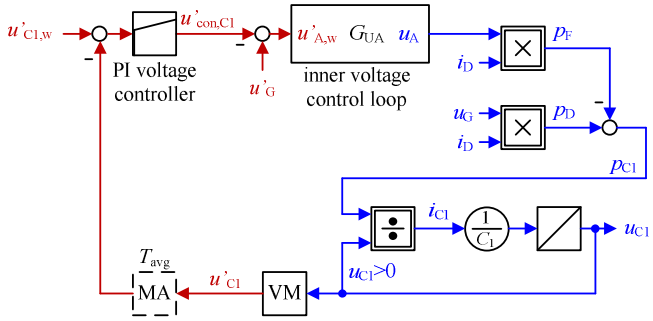


Fig. 10. Outer voltage control structure for u_{C1}

The power p_{C1} can be expressed by:

$$p_{C1} = \underbrace{u_G \cdot i_D}_{p_D} + \underbrace{G_{UA} \cdot u'_{con,C1} \cdot i_D - G_{UA} \cdot u'_G \cdot i_D}_{-p_F} \tag{16}$$

Here, $G_{UA} = u_A / u'_{A,w}$ describes the behavior of the inner voltage control loop. The Laplace-transformed transfer function from the controller output $u'_{con,C1}$ to the voltage u_{C1} is as follows:

$$\frac{u_{C1}(s)}{u'_{con,C1}(s)} = G_{UA}(s) \cdot \frac{i_D}{u_{C1}} \cdot \frac{1}{C_1} \cdot \frac{1}{s} \tag{17}$$

The gain of the transfer function depends on i_D and u_{C1}. This has to be considered, when controller parameters are calculated. Single-phase inverters lead to a voltage ripple on u_{C1} with double output frequency, which can be suppressed by a moving average filter in the measuring path. The voltage u_{C1} can be changed dynamically during operation and should be kept as low as possible to minimize the switching losses.

V. Experimental Results

A prototype for three strings has been built up to verify the function of the MPP tracking circuit. Fig. 11a shows one of two identical printed circuit boards with two MOSFET half-bridges. The circuit feeds a single-phase IGBT H-bridge inverter, shown in Fig. 11b. Values and part names of

important components are listed in Table I. The maximum output current is 25A, the switching frequency of T1*x* - T4 has been set to 16kHz.

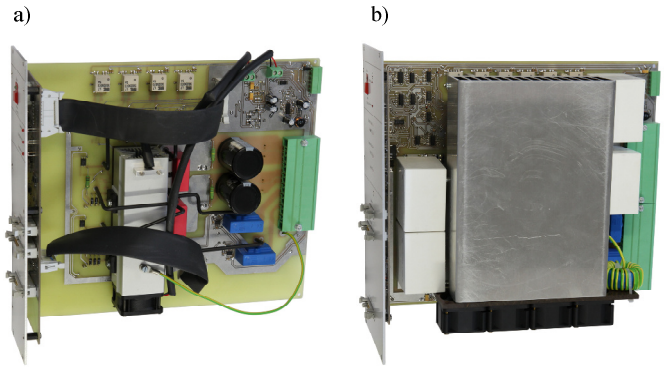


Fig. 11. Prototype printed circuit boards

TABLE I. COMPONENT VALUES AND NAMES

Part	Value / Part Name
C1	8800µF / 160V electrolytic capacitors
C3	500µF / 900V film capacitors (MPP tracking circuit + inverter)
C4*x*	50µF / 900V film capacitor
L1x	1.9mH
D1*x*	not used; string relays are used instead
T1x - T4	Infineon IPP110N20N3 (200V / 10.7mΩ)

A. Operation

Measurements have been performed with three strings of "MQ36" photovoltaic panels, see Fig. 12. The individual string voltages u_{Gx} are set to different values. The currents i_{Dx} are

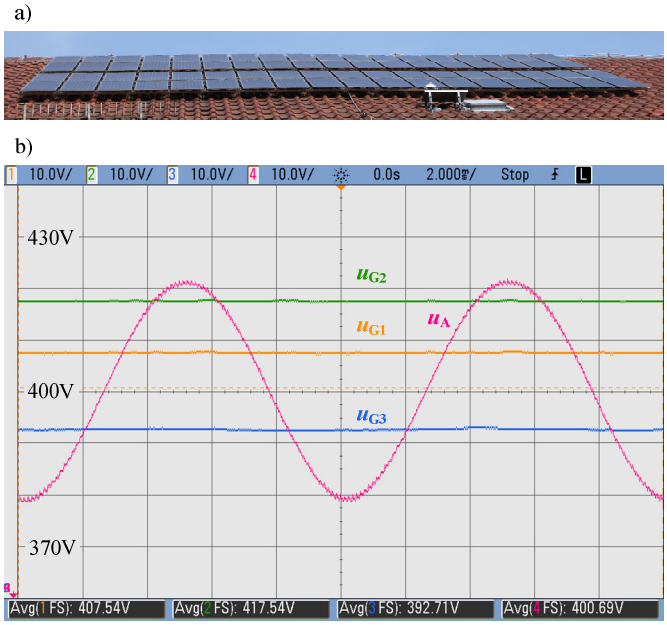


Fig. 12. a) Photovoltaic panels (three strings)
b) Experimental results: string voltages u_{Gx} and output voltage u_A

controlled with state controllers according to Fig. 6. As the single-phase inverter sinks a pulsating power with double grid-frequency at its DC-side, the voltage u_A is pulsating with 100Hz. The pulsating energy is buffered in C1 and C3. The output capacitor C3 is realized as film capacitor with only 500µF. The voltage ripple Δu_A is 42V at a DC power of p_D = 2.7kW and a grid frequency of f_{grid} = 50Hz.

When solar panels are connected directly to a single-phase inverter with 100Hz input voltage ripple, the operating point on the power curve (Fig. 1) moves around the MPP with the same frequency. This reduces the mean power, delivered by the panels. The MPP tracking circuit holds the string voltages u_{Gx} constant (Fig. 12), which increases the mean power of the solar panels.

B. Efficiency

Efficiency measurements usually lead to relatively high tolerances when the measured output power of a circuit is divided by the measured input power ($\eta = p_{out} / p_{in}$). Therefore, a special measurement setup according to Fig. 13 is used, that leads to more accurate results due to lower voltage measuring ranges of the used power analyzer.

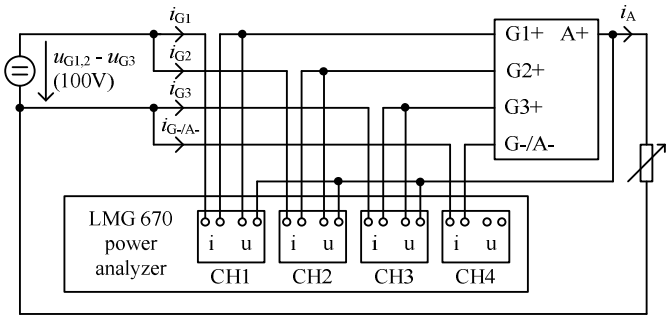


Fig. 13. Efficiency measurement setup

The DC-currents at the capacitors C4*x* and C3 (Fig. 2) are zero at stationary operation, so the DC-current $i_{G-/A-}$ at the terminal G-/A- (Fig. 13) is also zero. Therefore, the losses depend on the voltage differences between u_{G1} .. u_{G3} and on the currents i_{Gx}, but not on the absolute values of u_{Gx}, that occur between the terminals G*x*+ and G-.

Below, the efficiency of the circuit is investigated for the following operating condition: two strings G1 and G2 are operated with a higher voltage $u_{G1} = u_{G2} = u_{G1,2}$ and one string G3 is operated with a lower voltage u_{G3} of $u_{G3} = u_{G1,2} - 100V$. All string currents are equal ($i_{G1} = i_{G2} = i_{G3}$).

The voltage $u_{G1,2} - u_{G3} = 100V$ is provided by a laboratory power supply (Fig. 13). Terminal G-/A- is connected to G3+. The output current i_A is set by a resistor. The control system, which is powered externally, ensures that all currents i_{Gx} are one third of i_A. The capacitor voltage u_{C1} is set to 110V and the voltage u'_H is set to -5V. This ensures, that all transistors T1*x* - T4 are switching with 16kHz. The losses p_V of the circuit are calculated by adding the three powers p_{CH1} .. p_{CH3}, that are measured by a LMG670 precision power analyzer from ZES Zimmer.

The fourth channel is used to verify that no DC current occurs at the terminal G-/A-. The losses p_V are plotted in Fig. 14 at different output currents i_A. p_V contains no losses in relays, gate-units, discharging resistors and in the control system. No diodes D1x are used. The maximum uncertainty $\Delta p_V = \Delta p_{CH1} + \Delta p_{CH2} + \Delta p_{CH3}$ of the LMG 670 power analyzer is calculated according to [12] and plotted with dashed lines. Typical uncertainties of the LMG670 are usually about 2..5 times below the calculated maximum uncertainties [12].

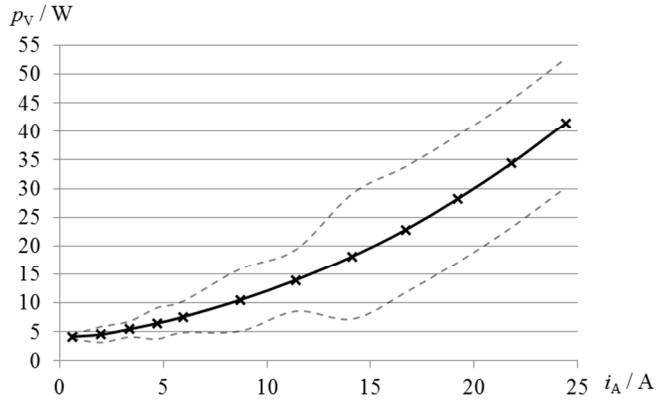


Fig. 14. Measured losses; lines interpolated; dashed line: maximum measurement uncertainity of the power analyzer

The efficiency can now be calculated for different string voltages $u_{G1,2}$. This is done with the following equation, where u_{CH1} is the measured voltage of channel 1:

$$\eta = \frac{p_{out}}{p_{in}} = \frac{p_A}{p_A + p_V} = \frac{u_A \cdot i_A}{u_A \cdot i_A + p_V} = \frac{(u_{G1,2} - u_{CH1}) \cdot i_A}{(u_{G1,2} - u_{CH1}) \cdot i_A + p_V} \quad (18)$$

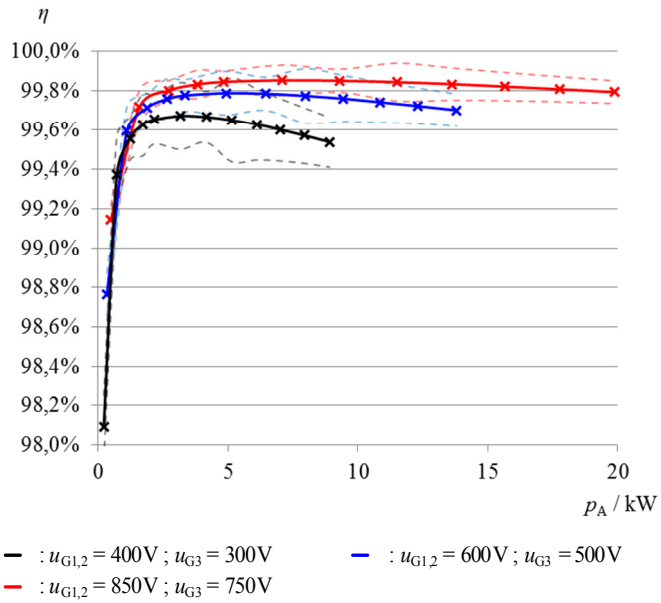


Fig. 15. Calculated efficiency at different string voltages; lines interpolated; dashed line: maximum measurement uncertainity of the power analyzer

The calculated efficiency is shown in Fig. 15. The resulting maximum measurement uncertainty $\Delta\eta$, caused by the power analyzer, is calculated with the total derivative (19) and plotted in dashed lines.

$$\Delta\eta = \left|\frac{\partial\eta}{\partial p_V}\right| \cdot \Delta p_V + \left|\frac{\partial\eta}{\partial u_A}\right| \cdot \Delta u_A + \left|\frac{\partial\eta}{\partial i_A}\right| \cdot \Delta i_A \quad (19)$$

The efficiency increases with increasing string voltages and reaches a peak value of 99.85%.

VI. Conclusion

An ultra-efficient MPP tracking circuit, that allows the connection of an unlimited number of strings to a solar inverter is described and investigated. All string voltages can be controlled independently. A limited difference between the individual string voltages is usually sufficient for a reasonable operation. This allows the use of transistors with reduced blocking voltages and smaller inductors, which leads to low losses. Furthermore, the circuit can buffer the pulsating energy that occurs when a single-phase inverter is used. A cascaded control scheme is developed and a prototype is built up. The circuit is tested with real photovoltaic panels. Loss measurements are performed and the resulting efficiency is calculated at different operating points. The prototype reaches a maximum efficiency of 99.85%.

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