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Institute:	Karlsruhe Institute of Technology (KIT) Elektrotechnisches Institut (ETI)
Type:	Conference Proceedings
Published at:	IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society, Yokohama, Japan, November 9-12, 2015 Publischer: IEEE, Piscataway (NJ) ISBN: 978-1-4799-1761-7 Year: 2015 Pages: 1276 - 1281
Hyperlinks:	10.1109/IECON.2015.7392276

A Novel Modulation Scheme for a Modular Multiphase Multilevel Converter in a Power Hardware-in-the-Loop Emulation System

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***Abstract*—This paper presents a novel modulation strategy for a Modular Multiphase Multilevel Converter especially for the usage in Power Hardware-in-the-Loop Emulation Systems. The proposed modulation scheme generates the required voltage time area by means of an integrator in a quasi continuous operation mode. Therefore, the fixed modulation period is disestablished to achieve a minimum response time of the emulation converter. The switching states of the parallel half-bridges are selected by a sorting algorithm, dependent on the instantaneous branch currents, to avoid saturation in the flux compensated chokes of the converter. The performance of the modulation scheme is verified at a three phase, seven level multilevel converter, with a PWM-frequency up to 120 kHz and an output power of more than 100 kW.**

I. Introduction

In modern drive inverter development processes the desire for more and more advanced test benches increases rapidly. Thus, besides various state of the art computer simulation tools (software-in-the-loop - SIL - simulation), real-time hardware-in-the-loop (HIL) test benches were developed. However, HIL test benches are not suitable to test the manufacturing processes, the reliability or the behavior of the entire device under various fault conditions. Therefore, conventional motor load test benches are used for that purpose. Unfortunately, there are several drawbacks and disadvantages inherent to conventional motor load testbeds. Due to the fact that there are numerous different applications that drives can be used for, various motor load combinations are required to test the drive system. Furthermore, as a result of fabrication tolerances, the test conditions can vary between actually identical motor load combinations. Therefore, it is desirable to connect the inverter to a power hardware-in-the-loop (PHIL) emulation test bench to evaluate its proper function under equal and reproducible test conditions.

Figure 1. shows a typical PHIL emulation test bench. At this type of test bench, the HIL real-time simulation system is extended by an emulation converter which is connected to the device under test (DUT) by means of an inductive coupling network. Since the DUT commonly controls the machine currents, the PHIL-emulation system should control the counter voltages $v_{x,\mathrm{CV}}$ at the coupling network to avoid problems

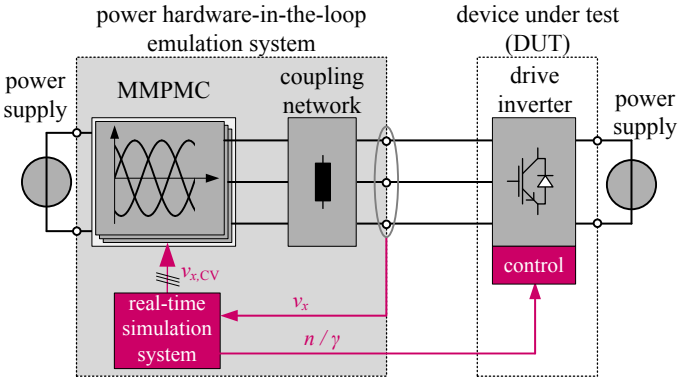

Fig. 1. Schematic diagram of a typical power hardware-in-the-loop emulation test bench equipped with a Modular Multiphase Multilevel Converter (MMPMC).

caused by a second current controller within the PHIL [1]. Therefore, the counter voltages have to be calculated by the real-time simulation system and provided for the emulation converter as reference value. However, to emulate the machine behavior at the best rate, it is preferable to feed the coupling network by a high-precision 3AC voltage source. The most important requirements to this voltage source are a low total harmonic distortion (THD), high dynamics, high precision and a low internal resistance. The Modular Multiphase Multilevel Converter (MMPMC) which has been proposed in [2] fulfills these requirements. The main advantages of this converter are, compared to other proposals like [1], [3]–[6], that the converter is easy scalable, consists only of standard components like half-bridges and two winding flux compensated chokes and has no critical operation points due to internal cell balancing tasks.

The fundamentals of the MMPMC in conjunction with a direct differential current measurement are introduced in Section II. Afterwards, the new modulation scheme which is especially suitable for a PHIL application is derived in Section III. The hardware setup of the converter as well as the specifically designed high performance signal processing system is described in Section IV. Measurements are per-

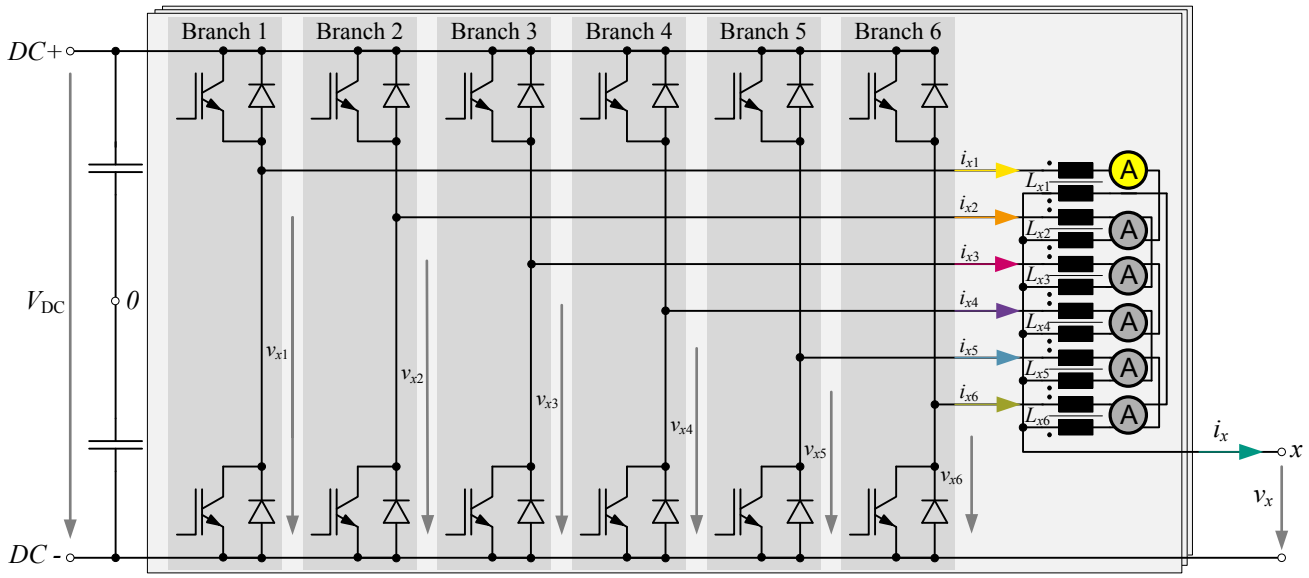

Fig. 2. Schematic diagram of the Modular Multiphase Multilevel Converter (MMPMC) with $n = 6$ branches per phase.

formed to evaluate the performance of the converter as well as the modulation schemes and are discussed in Section V. Conclusions are stated in Section VI.

II. Fundamentals of the MMPMC

Figure 2. shows the equivalent circuit of a three phase Modular Multiphase Multilevel Converter with six branches per phase [2]. The basic idea of this converter is the construction of an inductive voltage divider to generate a multilevel voltage waveform. The principle of the multilevel voltage generation is illustrated in Fig. 3. The inductive voltage divider is composed of n flux compensated chokes and n standard half-bridges ($n \in \mathbb{N} \mathrel{\widehat{=}}$ number of parallel branches and $y \mathrel{\widehat{=}}$ branch number, $y \in \{1, 2, ..n\}$). For this reason, the resulting output voltage v_x has $n + 1$ constant voltage levels ($x \mathrel{\widehat{=}}$ output phase number, $x \in \{\mathrm{u}, \mathrm{v}, \mathrm{w}\}$). Furthermore, the coupling network is connected as cyclic cascade [7]. Therefore, the resulting effective inductance $L_{x,\mathrm{DM,res}}$ for the output currents i_x is only determined by the leakage inductance of the flux compensated chokes $L_{xy,\sigma}$. Thus, the load dependent change of the output voltages v_x is negligible and the converter has the performance of a voltage source. A more detailed description of the operation principle can be found in [2].

The switching states of the particular branches are selected by means of a sorting algorithm in the modulator. The advantage of this modulation, compared to other proposals (e.g. [8], [9]), is that no additional current controllers are required to ensure a symmetrical distribution of the load currents i_x to the branches. Furthermore, the entire modulation scheme which generates the multilevel voltage waveform as well as the sorting algorithm for the current balancing is carried out directly into an FPGA. For this reason, it is not necessary to consider the MMPMC in the overlaying control algorithms since the modulator generates just the required voltage time area without affecting the control unit. The use of a sorting

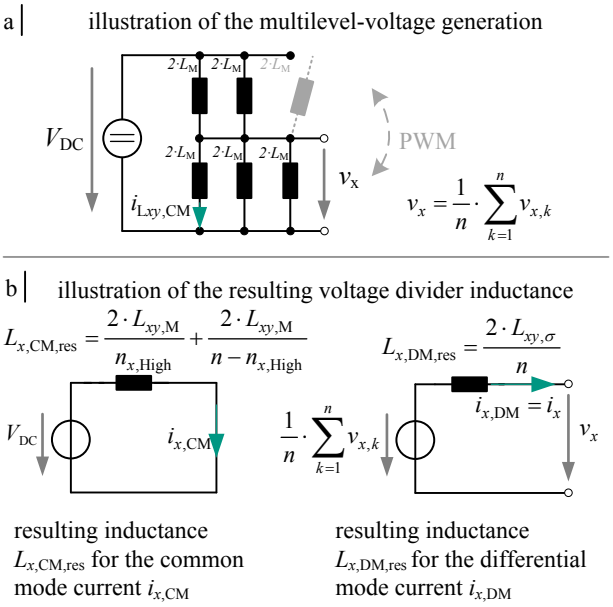

Fig. 3. Illustration of the multilevel-voltage generation and the resulting output inductance of the MMPMC.

algorithm for the selection of the switching states is similar to the modulation of the Modular Multilevel Converter (MMC) [10] and has been adapted to this application.

A. Direct Differential Current Measurement

As mentioned above, flux compensated chokes are used for the cyclic cascade. It is advantageous to use flux compensated chokes with a high common mode inductance $L_{xy,\mathrm{CM}}$ (e.g. some mH) to minimize the additional stress for the semiconductors caused by the inner circulating current of the

inductive voltage divider. Thus, the common mode currents are very small and negligible compared to the load current. Indeed, a precise measurement of the common mode currents, or rather the magnetic effective currents $i_{\mathrm{L}xy,\mathrm{CM}}$, is necessary to avoid saturation in the flux compensated chokes. Due to the strongly limited resolution of the inverters branch current measurement, which is designed for the whole branch current i_{xy}, the MMPMC in this paper was equipped with a direct differential current measurement for the currents $i_{xy,\mathrm{diff}}$ (gray current measurement in Fig. 2.):

$$i_{xy,\mathrm{diff}} = i_{xy} - i_{x(y-1)} = i_{\mathrm{L}xy,\mathrm{CM}} \tag{1}$$

This measurement is feasible, since the relative currents related to one arbitrary branch are sufficient for the correct operation of the sorting algorithm. The output currents i_x are necessary for an optional overlaying current controller only. Indeed, the measurement of one arbitrary branch current i_{xy} (e.g. yellow current measurement in Fig. 2.) is sufficient as well. Due to the junction rule, the output currents i_x can be calculated if one branch current i_{xy} and (n-1) differential currents $i_{xy,\mathrm{diff}}$ are measured.

III. Modulation Strategy

In this Section, a modulation strategy for the MMPMC is derived, which is especially suited for the MMPMC as emulation converter within a Power Hardware-in-the-Loop test bench. According to [11] the set values $v_{x,\mathrm{CV}}$ for the emulation converter have to be calculated with a very high frequency (e.g. 1.5 MHz). Additionally, the phase inductance of the coupling network does not correspond to the phase inductance of the emulated machine due to saturation or the magnetic anisotropy of synchronous machines. Therefore, the counter voltages $v_{x,\mathrm{CV}}$ at the coupling network have to be changed very dynamically, to ensure the correct current slopes of the emulated machine in the coupling inductance of the PHIL test bench. For this reason, the requirements to a modulation scheme for a MMPMC within a PHIL test bench are:

- precise realization of the required voltage time area
- high modulation frequency f_{c}
- low total harmonic distortion (THD)
- minimal dead times
- symmetrical distribution of the load currents i_x to the single branches i_{xy}
- minimization of the common mode currents $i_{\mathrm{L}xy,\mathrm{CM}}$ in the flux compensated chokes
- prevention of saturation in the flux compensated chokes
- low average switching frequencies f_{s} within the single branches

A. Complete Sorting Modulation (CSM)

The origin of the proposed modulator is the complete sorting modulation. This scheme is nearly identical to a typical modulation of the MMC [12]. Fig. 4. depicts a modulation cycle of this method. The differential current $i_{xy,\mathrm{diff}}$ in every branch is measured and the currents i_{xy} are calculated at the

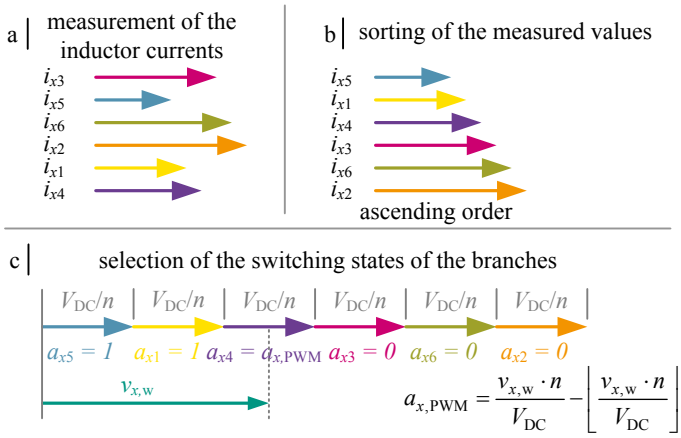

Fig. 4. Modulation cycle of the complete sorting modulation

beginning of the pulse-period (Fig. 4.a). Subsequently, the sorting algorithm sorts the branch currents in ascending order (Fig. 4.b). Afterwards, the number of switches $n_{x,\mathrm{High}}$, which have to be switched to $DC+$ during the entire modulation period as well as the duty-cycle $a_{x,\mathrm{PWM}}$ of the PWM-switch is calculated according to the desired output voltage $v_{x,\mathrm{w}}$, with:

$$n_{x,\mathrm{High}} = \left\lfloor \frac{v_{x,\mathrm{w}} \cdot n}{V_{\mathrm{DC}}} \right\rfloor \tag{2}$$

$$a_{x,\mathrm{PWM}} = \frac{v_{x,\mathrm{w}} \cdot n}{V_{\mathrm{DC}}} - n_{x,\mathrm{High}}. \tag{3}$$

Finally, the branches with the lowest currents are selected and switched to DC+ according to the calculated duty cycles (Fig. 4.c) [2]. The advantage of this modulation scheme is, that it ensures the best distribution of the output currents i_x to the branches and therefore, it has the lowest common mode currents in the chokes. Indeed, for this reason the single branches have the highest switching frequency f_{s} compared to the modulation frequency f_{c}.

B. Single Switching Modulation (SSM)

The single switching modulation is the first advancement of the complete sorting modulation to minimize the switching frequency of the particular branches. This modulation scheme is also very similar to a proposal from [10]. Fig. 5. shows a modulation cycle of the single switching modulation. At this modulation scheme the measurement as well as the calculation of $n_{x,\mathrm{High}}$ and $a_{x,\mathrm{PWM}}$ is identical to the complete sorting modulation. Indeed, the switching states of the branches from the previous modulation cycle are now taken into account. Therefore, the sorting algorithm forms two groups (group $DC+$ and group $DC-$) of branches dependent on their actual switching state. Subsequently, the branches are sorted within their group in ascending order (Fig. 5.b). Afterwards, the modulation cycle is partitioned into the three following states: T_{F1}, T_{A}, T_{F2} (see Fig. 5.c). In case that the reference value of the output voltage $v_{x,\mathrm{w}}$ stays within the same voltage level ($n_{x,\mathrm{High},k} = n_{x,\mathrm{High},k-1}$) the switching state $T_{\mathrm{F1}k}$ is

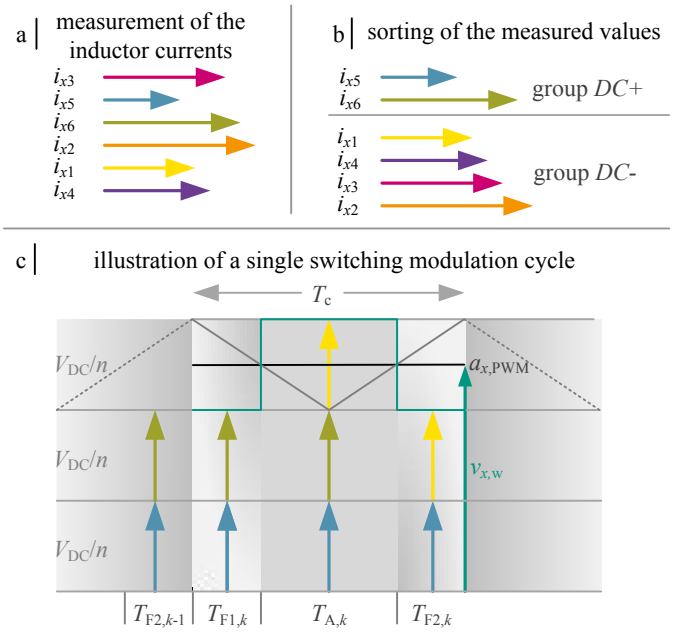

Fig. 5. Modulation cycle of the single switching modulation

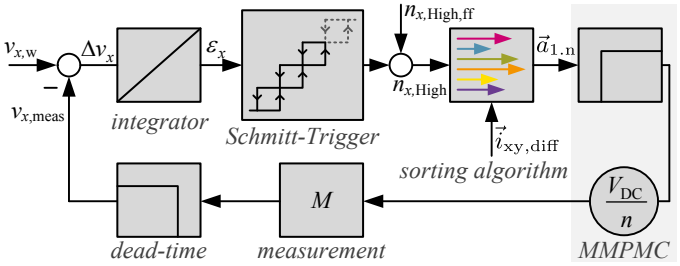

Fig. 6. Modulation cycle of the direct self-modulation

inherited from T_{F2k-1} so that there are no switching events at the beginning of the modulation period. Afterwards, at the beginning of $T_{A,k}$ the branch with the lowest current of group $DC-$ (yellow branch) is switched to $DC+$. Finally, at the end of $T_{A,k}$ the branch of group $DC+$ with the highest branch current (green branch), is switched to $DC-$ to generate the pulse width modulation (see Fig. 5.c). Therefore, the swapping of the branches, which is necessary for the current balancing, is done within the PWM-modulation and does not cause additional switching cycles. The theoretical lower limit for the switching frequency f_s of one branch with single switching modulation is:

$$f_s = \frac{f_c}{n} + \frac{n_{vlc}}{2 \cdot n} \cdot f_{x,vw} \tag{4}$$

whereby:

- $f_{x,vw}$ = frequency of the output voltage waveform
- n_{vlc} = number of voltage level changes within one period of the output voltage waveform

Though, it has to be considered that due to manufacturing tolerances of the chokes, the current slopes of the common mode currents $i_{Lxy,CM}$ in every branch can differ from each other and the branch switching frequencies f_s can be unequally distributed. Furthermore, the common mode currents $i_{Lxy,CM}$ in the chokes are naturally higher compared to the complete sorting modulation.

C. Threshold Modulation (THM)

Due to the fact, that the single switching modulation has strongly reduced switching losses compared to the complete sorting modulation, this kind of modulation should be preferred for the MMPMC. Though, the saturation of the flux compensated chokes has to be avoided in any case. Therefore, the single switching modulation was extended by a threshold monitoring for the common mode currents $i_{Lxy,CM}$. Thus, the threshold modulation combines the advantages of the complete sorting and the single switching modulation. In case that the common mode currents exceed a specific threshold value, a complete sorting cycle is inserted. This avoids the saturation of the flux compensated chokes in any case without increasing the switching frequency f_s of the single branches significantly.

D. Direct Self-Modulation (DSM)

Up to now, the modulation scheme considers only the requirements of the MMPMC. Hence, a further improvement is necessary to consider the requirements of the PHIL system as well. Therefore, the THM was extended by a control loop to the direct self-modulation. The functionality of the direct self-modulation is illustrated in Fig. 6. The basic idea of the DSM is very similar to the realization of the flux controller of the direct self-control (DSC) which was proposed in [13]. Analogous to the DSC, the DSM has no fixed modulation period. Instead, there is now an integrator which integrates the difference of the reference voltage $v_{x,w}$ and the measured voltage $v_{x,meas}$. The DSM integrator and the sorting algorithm are realized quasi continuous with the same frequency as the machine model in the PHIL test bench (1.5 MHz [11]) and are directly connected to the machine model. Due to the quasi continuous integration of the reference voltage $v_{x,w}$, the DSM avoids the additional dead time T_c for the duty-cycle calculation. Therefore, the response time of the voltage time area generation is only limited by the maximum switching frequency of the branch semiconductors, the dead-time of the MMPMC (signal propagation delay, switching delay time and interlock times) and the dead-time of the output voltage measurement. Subsequently, the integrator output ε_x is evaluated by means of a Schmitt-Trigger. In case that the integrator exceeds or rather falls below a reference value ε_{ref}, an additional switch is switched to $DC+$ respectively to $DC-$. Thereby, the reference value ε_{ref} of the integrator can be used to tune the average modulation frequency f_c of the output voltage waveform. Additionally, the number of branches $n_{x,High,ff,}$ is calculated according to eq. 2 and fed forward to increase the dynamic of the modulation scheme. Furthermore, errors in the desired voltage time area due to interlock times of the semiconductor switches as well as

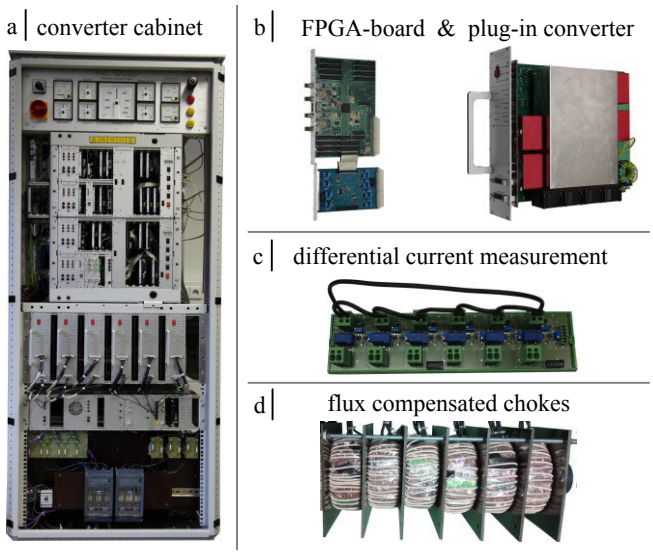

Fig. 7. Hardware setup of the MMPMC

minimum turn on times etc. are directly corrected, since the output voltages v_x are measured and directly controlled. In addition, the common mode currents $i_{\mathrm{L}xy,\mathrm{CM}}$ of the chokes are monitored analogous to the THM to ensure a symmetrical distribution of the load current to the branches. In case that the common mode currents exceeds a specific threshold the active requested switching configuration is newly set by a complete sorting without effecting the output voltage.

IV. Hardware Setup

A three phase prototype ($U_\mathrm{N} = 400$ V, $I_\mathrm{N} = 150$ A) is built up to evaluate the performance of the proposed converter as well as the new modulation scheme (Fig. 7.a). The prototype has $n = 6$ branches per phase and consists of a specifically designed modular power converter (six-pulse bridge, Fig. 7.b). The power converter is based on the FS75R12KT4-B15 IGBT-module from Infineon, has double euroboard format and is built as plug-in unit for a 19" rack to get a scalable test bench. A specifically designed high-performance signal processing unit is used to implement the modulator. The core of the signal processing unit is an FPGA-board with a Cyclone 4 FPGA (EP4CE40F23C6) from Altera. The FPGA-board is directly connected to THS1206 A/D-Converters from Texas Instruments with a sample rate of 1.5 MS/s to measure the differential currents $i_{xy,\mathrm{diff}}$ as well as the output voltages v_x. The direct differential current measurement was built up with CAS6-NP current sensors from LEM. The interconnection of the cyclic cascade is directly done at the differential current measurement board (Fig. 7.c). The flux compensated chokes of one phase are depicted in Fig. 7.d. The chokes consist of a stack of two L2130 - W587 ring shaped strip-wound cores per branch. The core is made of the nanocrystalline material Vitroperm 500F from VAC. Furthermore, the single chokes are designed for a common mode current of $\hat{i}_{xy,\mathrm{diff}} = \hat{i}_{\mathrm{L}xy,\mathrm{CM}} = 680$ mA and a differential mode current of $I_{\mathrm{L}xy,\mathrm{DM}} = 30$ A.

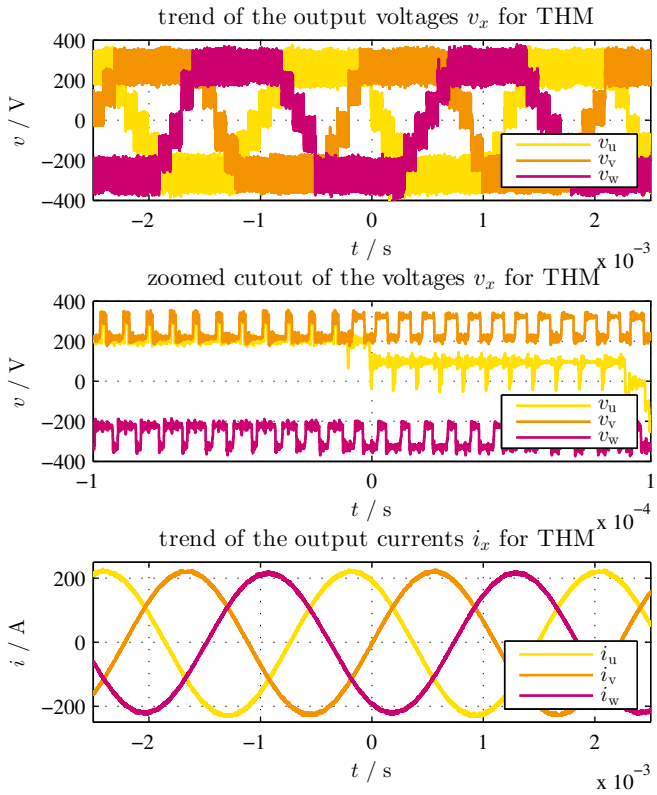

Fig. 8. Measurement results for the threshold modulation

TABLE I
SWITCHING FREQUENCIES FOR THE DIFFERENT MODULATION SCHEMES

n	$f_{\mathrm{s,SSM}}$/ kHz	$f_{\mathrm{s,THM}}$/ kHz	$f_{\mathrm{s,CSM}}$/ kHz	$f_{\mathrm{s,DSM}}$/ kHz
1	19.53	19.47	29.66	17.19
2	22.26	22.52	34.24	16.27
3	21.91	22.16	36.29	17.16
4	19.75	19.74	35.68	17.19
5	19.51	19.72	30.58	17.43
6	19.57	19.86	33.72	16.96
Σ	122.53	123.47	200.17	102.20

V. Measurements

Figure 8. shows a measurement of the output voltage waveforms v_x of the three phase MMPMC. The load current was measured at a passive RL-load with an inductance of 0.5 mH, an ohmic resistance of 10 mΩ and a frequency of $f_{x,\mathrm{vw}} = 450$ Hz. Agilent MSOX3024A oscilloscopes with Tektronix P5200 differential probes and Tektronix A6304XL current probes were used to measure the output voltages and currents. Furthermore, the THM was used at a DC-Link voltage of 650 V. The modulation frequency f_c was set to 120 kHz. A zoomed cutout of the output voltages is depicted in Fig. 8, second plot. In the third plot, the load current is shown to demonstrate the performance of the test bench. It can be seen that the steps of the multilevel voltage waveforms are clearly formed even at an output current $\hat{i}_x$ of more than 200 A. Additionally, Tab. I. shows the measured switching frequencies f_s of the MMPMC branches for the different modulation schemes at a modulation frequency of

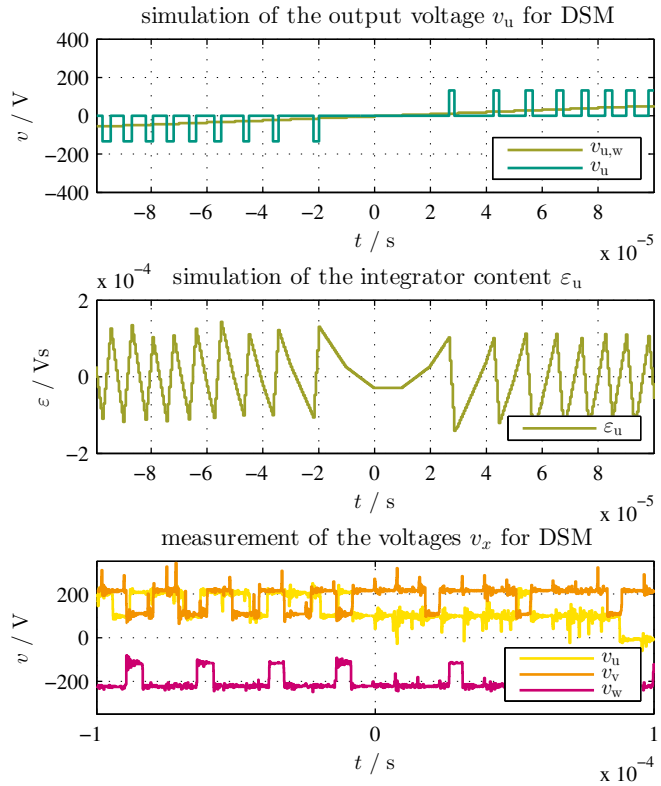

Fig. 9. Simulation and measurement results for the direct self-modulation

$f_c = 120$ kHz. As can be seen from Tab. I. the switching frequencies of the THM and the SSM are nearly identical. Only the CSM increases the switching frequency of the particular branches significantly. Figure 9. shows simulation and measurement results of the DSM. In the first plot it can be noted that there is no longer a fixed modulation period. The second plot depicts the integrator content of the simulation which adjusts the modulation frequency f_c of the simulated output voltage waveform v_u to approximately 120 kHz. The third plot shows a measurement result. Indeed, there are a lot of spikes in the output voltage waveforms. This spikes are caused by the branch swapping of the threshold monitoring, since the swapping is not perfect synchronous in every branch due to different signal propagation delays as well as switching delay times of the IGBTs. Additionally, it can be seen that the resulting modulation frequency f_c of the output voltages v_x are lower compared to the THM or the simulation. This can be explained with the dead-time of the used A/D-Converter (2.2 µs), the switching delay of the plug-in converter ($\approx$ 0.7 µs) and the necessary interlock times of the IGBTs ($\approx$ 1 µs). These effects limit the maximum possible modulation frequency f_c to approximately 65 kHz. Indeed, these limitations can be easily eliminated if e.g. SIC or GaN seminconductors or an A/D-converter with a better performance are used.

VI. Conclusion

This paper has introduced a novel modulation strategy for a Modular Multiphase Multilevel Converter especially for the usage in Power Hardware-in-the-Loop emulation systems. The proposed modulation scheme generates the required voltage time area, without additional dead times, by means of an integrator in a quasi continuous operation mode (1.5 MHz). A sorting algorithm selects the optimal switching states of the particular branches dependent on the instantaneous branch currents to avoid saturation in the flux compensated chokes. Measurements were performed to verify the performance of the modulation scheme as well as the performance of the converter of 100 kW at a seven level output voltage waveform and a modulation frequency up to 120 kHz.

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