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# A multi-string photovoltaic inverter for thin-film or back-side contacted solar modules

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## Abstract

Photovoltaic inverters are widely used to feed solar generated power into the public grid. Inverter topologies have to be carefully chosen, depending on the type and on the power of the solar generator. A new transformerless, three-level photovoltaic inverter circuit for multiple strings is investigated in this paper. It allows an individual MPP tracking of each string without needing a full scale boost converter for each input. Furthermore, either the positive poles or the negative poles of the strings can be connected to the neutral conductor N. Therefore, the topology is especially suited for thin-film or back-side contacted solar modules.

## 1 Introduction

Depending on the configuration of the solar generator, photovoltaic inverters have to fulfill several requirements. If partial shading occurs in multi-string systems, an individual maximum power point (MPP) tracking of every string is very advantageous to maximize the energy yield. Furthermore, it may be required to connect one pole of the strings to the neutral conductor N. Connecting the negative poles to N can prevent thin-film solar modules from corrosion of the transparent conductive oxide (TCO) [1]. Connecting the positive poles to N can lead to a higher efficiency if back-side contacted solar modules are used [2]. Last but not least some grid codes, e.g. [3] require, that certain photovoltaic inverters must be able to deliver reactive power. A new transformerless circuit, which fulfills these requirements is shown in Fig. 1. A basic description can be found in [4]. This contribution presents a detailed circuit description, an appropriate control system and experimental results.

## 2 Function of the circuit

The circuit of Fig. 1 consists of $M$ input half-bridges and a common inverter section [4]. They are interconnected at X1-X3 with a split DC-link, consisting of the capacitors C1 and C2. Another capacitor C3 can be added optionally. The input half-bridges are built up with two transistors T1$x$ and T2$x$ ($x \in \{1,2..M\}$). They are used to control the string voltages $u_{Gx}$ in the range $u_{C2} < u_{Gx} < u_{C1} + u_{C2}$. Furthermore, they spilt the string currents $i_{Gx}$ into the currents $i_{E1}$ and $i_{E2}$. The inverter section on the right side of Fig. 1 is built up with the transistors T3-T7 and is similar to the single string topology of [5-7]. The positive poles of the solar generator can be connected to N if all power semiconductors are connected in opposite direction.

Fig. 2 shows the switching states of the inverter section, which are chosen by a pulse with modulation (see also [5-7]). During the positive half-wave, the switching states 1 and 3a

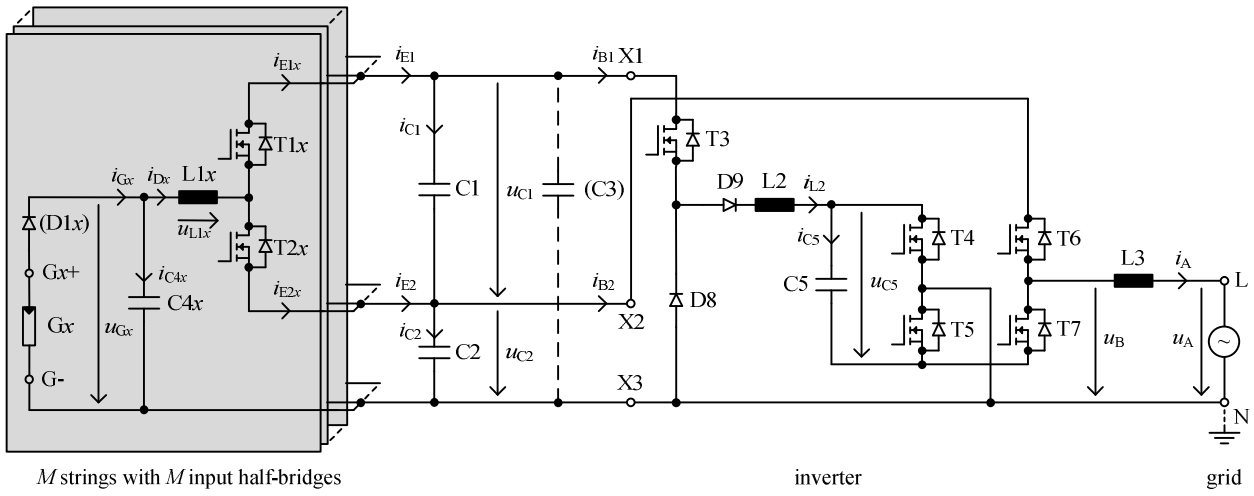
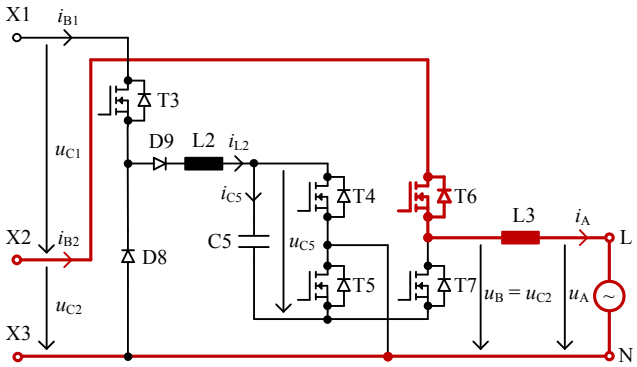
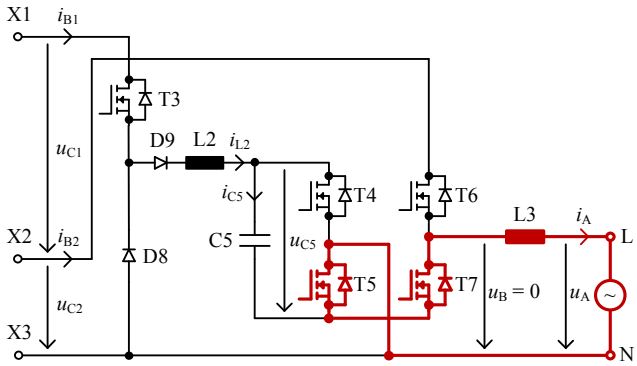


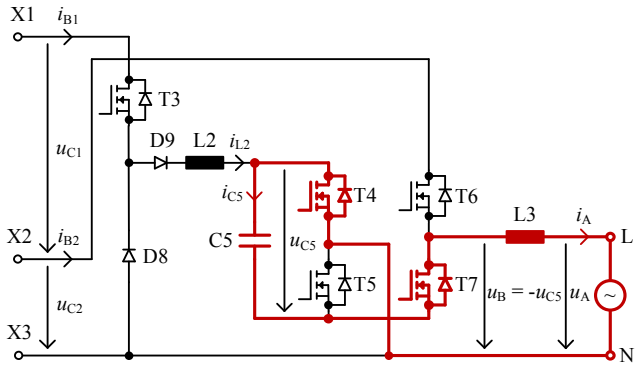

Fig. 1: The new inverter circuit (see also [4])



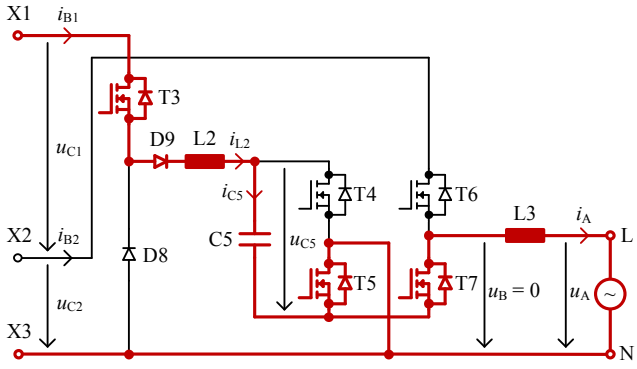

State 1 (positive half-wave)




State 3a (positive half-wave)




State 2 (negative half-wave)




State 3b (negative half-wave)

Fig. 2: Switching states (see also [5-7])

are used alternately. This operation mode is similar to a buck converter. The state durations depend on the set value $u'_B$:

$$T_1 = \frac{1}{f_{sw}} \cdot \frac{u'_B}{u_{C2}} \qquad T_{3a} = \frac{1}{f_{sw}} \cdot \left(1 - \frac{u'_B}{u_{C2}}\right) \qquad (1)$$

During the negative half-wave, the switching states 2 and 3b are used alternately. In state 2, the voltage $u_{C5}$ of the flying capacitor C5 is applied to the AC side and C5 gets discharged. In the free-wheeling state 3b, C5 is recharged resonantly via T3, D9, L2 and T5. The durations of the switching states are as follows:

$$T_2 = \frac{1}{f_{sw}} \cdot \frac{-u'_B}{u_{C5}} \qquad T_{3b} = \frac{1}{f_{sw}} \cdot \left(1 - \frac{-u'_B}{u_{C5}}\right) \qquad (2)$$

The resonant charging process is shown in Fig. 3 (see also [5-7]). The charging current $i_{L2}$ is switched off by the diode D9 at a value of zero. The diode D8 protects the transistor T3 from overvoltage, if T3 switched off, before $i_{L2}$ has reached zero [4]. Due to parasitic resistances in the charging path, the current $i_{L2}$ is a damped sine half-wave (see also [7, 8]). Note, that the energy for the positive half-wave of $u_A$ is taken from X2 / X3, while the energy for the negative half-wave is taken from X1 / X3 [4].

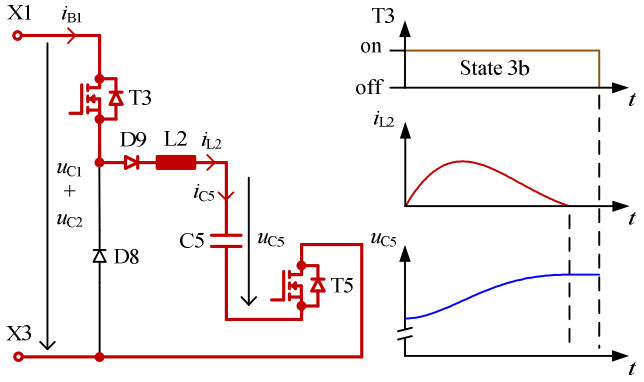



Fig. 3: Resonant charging process (see also [5-7])

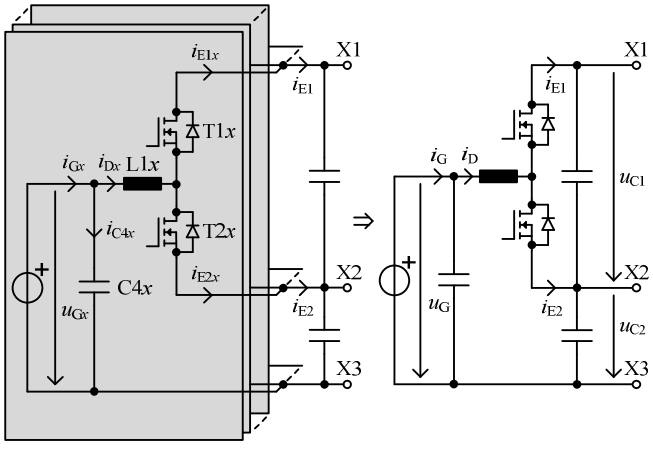



Fig. 4: Equivalent input section (see also [9])

The input section, consisting of $M$ half-bridges, can be modelled as one equivalent half-bridge according to Fig. 4 (see also [9]). The equivalent currents $i_G$ and $i_D$, as well as the equivalent voltage $u_G$ are calculated as follows [9]:

$$i_G = \sum_{x=1}^{M} i_{Gx} \qquad i_D = \sum_{x=1}^{M} i_{Dx} \tag{3}$$

$$u_G = \frac{\sum_{x=1}^{M} u_{Gx} \cdot i_{Gx}}{i_G} \tag{4}$$

The transistors T1$x$ and T2$x$ are controlled by a pulse width modulation. They split the input currents $i_{Gx} \approx i_{Dx}$ into the currents $i_{E1x}$ and $i_{E2x}$ (Fig. 4). These currents sum up to $i_{E1}$ and $i_{E2}$. Neglecting losses, their mean values per pulse-period $\overline{i}_{E1}$ and $\overline{i}_{E2}$ are calculated with the mean current per pulse-period $\overline{i}_D$ (see also [10]):

$$\overline{i}_{E1} = \frac{u_G - u_{C2}}{u_{C1}} \cdot \overline{i}_D \tag{5}$$

$$\overline{i}_{E2} = \left(1 - \frac{u_G - u_{C2}}{u_{C1}}\right) \cdot \overline{i}_D \tag{6}$$

The mean input currents per grid-period of the inverter section depend on the active power $P_A$ delivered to the grid. Assuming, that $u_{C1} = \overline{u}_{C1}$ and $u_{C2} = \overline{u}_{C2}$ are constant, they can be calculated as follows (see also [10]):

$$\overline{i}_{B1} = \frac{1}{2} \cdot \frac{P_A}{\overline{u}_{C1} + \overline{u}_{C2}} \tag{7}$$

$$\overline{i}_{B2} = \frac{1}{2} \cdot \frac{P_A}{\overline{u}_{C2}} \tag{8}$$

In stationary operation, the mean values of the capacitor currents $i_{C1}$ and $i_{C2}$ shall be zero. This leads to [10]:

$$\overline{i}_{B1} = \overline{i}_{E1} \qquad \overline{i}_{B2} = \overline{i}_{E2} \tag{9}$$

The mean capacitor current $\overline{i}_{C2}$ and therefore the voltage at the capacitor C2 (Fig. 1) can be controlled with the active power component $P_A$ of the inverter section. Due to a natural balancing effect, the mean voltage $\overline{u}_{C1}$ at the capacitor C1 automatically reaches a stable value under the following conditions [10]:

$$\frac{1}{2} \cdot u_G < u_{C2} < u_G \quad | \quad u_{C1} + u_{C2} > u_G \tag{10}$$

$$\overline{i}_D > 0 \tag{11}$$

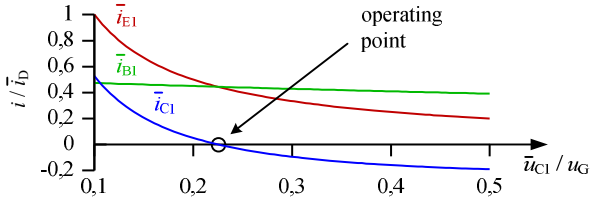



Fig. 5: Capacitor current $\overline{i}_{C1}$ over capacitor voltage $\overline{u}_{C1}$

Fig. 5 shows a graphical example for $\overline{u}_{C2} = 0.9 \cdot u_G$ and $\overline{i}_{C2} = 0$. The capacitor current $\overline{i}_{C1} = \overline{i}_{E1} - \overline{i}_{B1}$ crosses zero at the following operating point [10]:

$$\overline{u}_{C1} = \frac{2 \cdot (u_G - \overline{u}_{C2}) \cdot \overline{u}_{C2}}{2 \cdot \overline{u}_{C2} - u_G} \quad \text{for} \quad \frac{1}{2} \cdot u_G < \overline{u}_{C2} < u_G \tag{12}$$

The capacitors C1 and C2 buffer the pulsating energy, that occurs due to the usage of a single-phase inverter section [4]. Therefore, the voltages $u_{C1}$ and $u_{C2}$ are pulsating. The amplitudes of the pulsations around the operating points $\overline{u}_{C1}$ and $\overline{u}_{C2}$ depend on the capacitance values of C1 and C2, as well as on the apparent power at the AC-side [10]. Generally, the capacitor voltages have to fulfill the following conditions:

$$\hat{U}'_B < u_{C2} < u_{G,min} \tag{13}$$

$$u_{G,max} < u_{C1} + u_{C2} \tag{14}$$

$\hat{U}'_B$ is the amplitude of the set value $u'_B$ at the AC-side. The values $u_{G,min}$ and $u_{G,max}$ are the minimum and maximum voltages of the different strings at their maximum power point (see example in Fig. 6). It is advantageous to keep $u_{C1}$ as low as possible. This reduces the switching losses in the input half-bridges and allows the usage of small input inductors L1$x$ [10]. A low value of $\overline{u}_{C1}$ is achieved by choosing a high reference value for $\overline{u}_{C2}$ (see eq. (12)).

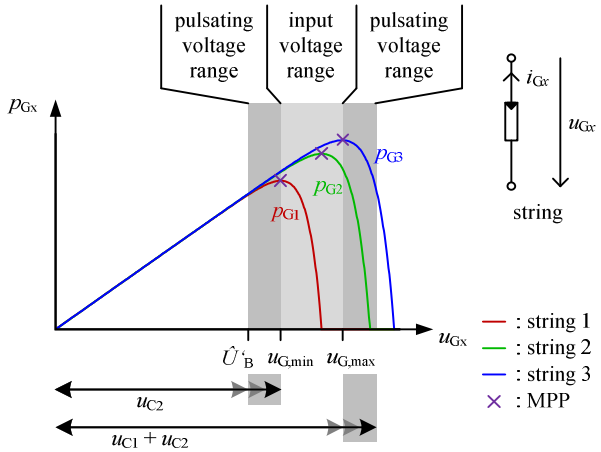



Fig. 6: voltage ranges; model parameters are taken from Table 2 of [11]

The transistors T1$x$ and T2$x$ only have to block voltages in the range of the maximum voltage at the capacitor C1, which is usually a fraction of the input voltages $u_{Gx}$. Therefore, T1$x$, T2$x$ and C1 can be dimensioned for a fraction of $u_{Gx}$. This leads to low losses and low costs. However, measures against overvoltage of $u_{C1}$ have to be taken. For example, overvoltage due to external short circuits at one of the strings can be prevented by additional diodes D1$x$ (Fig. 1). [4]

The circuit of Fig. 1 could also be realized with three inverter sections, connected in parallel to X1-X3. This allows an operation at three-phase grids.

## 3 Cascaded control scheme

The circuit contains $2M + 5$ components, that store energy:

- $M$ input capacitors C4$x$
- $M$ inductors L1$x$
- Capacitor C1
- Capacitor C2
- Charging inductor L2
- Flying capacitor C5
- AC inductor L3

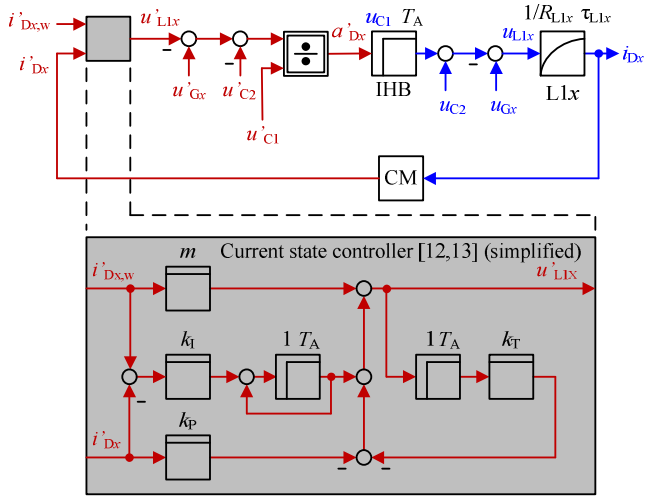
A cascaded control scheme is proposed. It requires, that the following values are measured:

- $M$ input voltages $u_{Gx}$
- $M$ inductor currents $i_{Dx}$
- Capacitor voltage $u_{C1}$
- Capacitor voltage $u_{C2}$
- Flying capacitor voltage $u_{C5}$
- AC voltage $u_A$
- AC current $i_A$

As the charging current $i_{L2}$ for the flying capacitor C5 is automatically switched off at a value of zero, there is no need to measure that current (see also [6]). The control scheme requires the following reference values:

- $M$ reference input voltages $u'_{Gx,w}$
- Reference capacitor voltage $u'_{C2,w}$

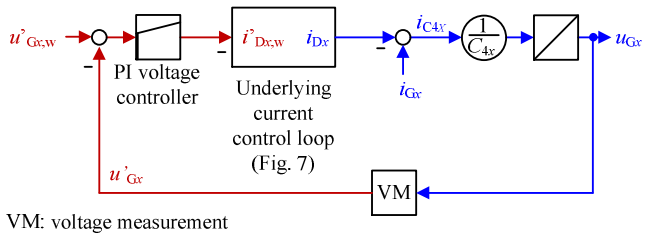
The currents $i_{Dx}$ at the inductors L1$x$ are set with $M$ underlying control loops according to Fig. 7. Values, that occur physically are drawn in blue. Values that occur in the control system, are drawn in red and marked with an apostrophe ( ' ). All values are mean values during one pulse-period. The inductors L1$x$ are modeled as first order lag elements, which allows the consideration of a series resistance. A dead time of $T_A$ occurs due to the pulse width modulation of the input half-bridges with the duty cycle $a'_{Dx}$. For high dynamic capabilities, state controllers according to [12, 13] are used. Controller parameters can be found in [13]. The voltages $u_{Gx}$, $u_{C1}$ and $u_{C2}$ are measured and fed-forward.




IHB: input half-bridge
CM: current measurement

Fig. 7: Underlying control structure for the inductor currents $i_{Dx}$

The inductor currents $i_{Dx}$ are used to set the $M$ input voltages $u_{Gx}$ in an overlying control loop (Fig. 8, see also [9]). For this purpose, standard PI-controllers are sufficient. Controller parameters can be calculated according to the symmetrical optimum [12]. The reference values $u'_{Gx,w}$ are set by standard MPP tracking algorithms, e.g. by perturb and observe algorithms.




VM: voltage measurement

Fig. 8: Overlying control structure for the input voltages $u_{Gx}$ (see also [9])

The AC current $i_A$ is controlled in an underlying loop, that sets the switching states from Fig. 2. The amplitude $\hat{I}_{A,w}$ of the AC current depends on the reference value $P'_{A,w}$ of the active power component and on the desired phase shift $\varphi'_{UI}$ between voltage and current (Fig. 9).

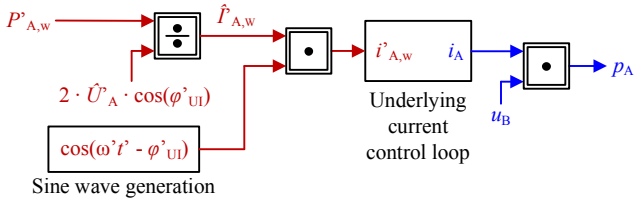



Fig. 9: Calculation of the reference AC current $i'_{A,w}$

The current $i_{C2}$ at the capacitor C2 equals the difference between the sum input current $i_D$ and the sum of the currents $i_{B1}$ and $i_{B2}$ at the inverter section:

$$i_{C2} = i_D - i_{B1} - i_{B2} \tag{15}$$

The mean inverter input currents during one pulse-period depend on the instantaneous power $p_A$ at the AC side:

$$\bar{i}_{B1} + \bar{i}_{B2} = \frac{p_A}{u_{IA} = \begin{cases} u_{C2} & \text{for } u'_B > 0 \\ u_{C1} + u_{C2} & \text{for } u'_B \le 0 \end{cases}} \tag{16}$$

Therefore, the voltage at C2 can be set with the active power component $P_A$ in an overlying control loop according to Fig. 10. The ripple on the measured value $u'_{C2}$ is suppressed by a moving average filter with an averaging time of

$T_{MA} = 1 / f_{grid}$. The sum of the reference input currents $i'_{D,w} = \sum_{x=1}^{M} i'_{Dx,w}$ is smoothened by another moving average filter and fed-forward.

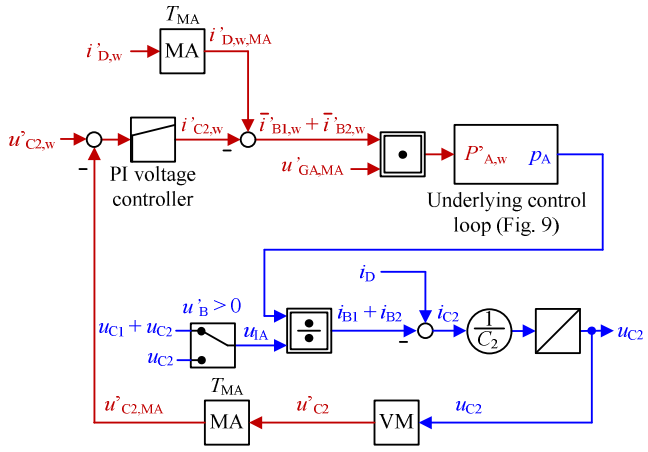



Fig. 10: Overlying control structure for the capacitor voltage $u_{C2}$

The reference value $P'_{A,w}$ is finally calculated with:

$$P'_{A,w} = \left(i'_{D,w,MA} - i'_{C2,w}\right) \cdot u'_{GA,MA} \qquad (17)$$

$$u'_{GA,MA} = \frac{2 \cdot u'_{C2,MA} \cdot (u'_{C1,MA} + u'_{C2,MA})}{2 \cdot u'_{C2,MA} + u'_{C1,MA}} \qquad (18)$$

$u'_{GA,MA}$ is a kind of mean value of $u_{IA}$. It can be calculated with the averaged voltages $u'_{C1,MA}$ and $u'_{C2,MA}$ at the capacitors C1 and C2. Moving average filters with $T_{MA} = 1 / f_{grid}$ suppress the ripples, caused by the pulsating power at the AC side (Fig. 11).

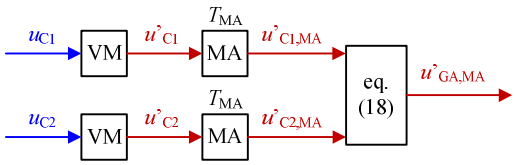



Fig. 11: Calculation of $u'_{GA,MA}$

## 4 Experimental results

A modular 3.7kW prototype for a grid voltage of 230V has been built up. Fig. 12a) shows a printed circuit board (PCB) with two input half-bridges. Fig. 12b) shows the PCB with the inverter section. Values and names of important components are listed in Table 1. The input half-bridges, consisting of T1*x* and T2*x*, are built up with low voltage silicon MOSFETs. Their $R_{DS(on)}$ is only 32mΩ, which leads to low losses. The inverter section is built up with silicon carbide MOSFETs. As the voltage at the transistor T6 can be approximately twice as high as the voltages at T3-T5 and T7, two MOSFETs are connected in series (see also [4]). A small film capacitor C3 is added to provide a current path with low inductance between X1 and X3.

a) b)

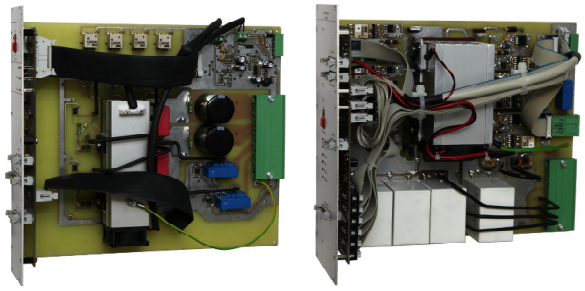


Fig. 12: Prototype printed circuit boards

| *Component* | *Value / Part Name* | *Comment* |
|---|---|---|
| T1*x*, T2*x* | Infineon IPP320N20N3G | $U_{DSmax}$ = 200V<br>$I_{D@100°C}$ = 22A |
| T3, T5 | CREE C2M0025120D | $U_{DSmax}$ = 1200V<br>$I_{D@100°C}$ = 60A |
| T4, T7 | CREE C2M0040120D | $U_{DSmax}$ = 1200V<br>$I_{D@100°C}$ = 40A |
| T6 | 2x CREE C2M0040120D in series | $U_{DSmax}$ = 1200V<br>$I_{D@100°C}$ = 40A |
| D9 | IXYS DSEI60-02A | $U_{RRM}$ = 200V<br>$I_{FAVM@85°C}$ = 69A |
| C1 | 8850µF / 160V | Electrolytic + Film |
| C2 | 450µF / 900V | Film |
| C3, C4x, C5 | 50µF / 900V | Film |
| L1x | 720µH | |
| L2 | Coilcraft SER2011-501ML (500nH) | + additional parasitic inductance |
| L3 | 5mH | |

Table 1: Values and names of components

Fig. 13 shows corresponding measurement results. The investigated prototype is equipped with three DC inputs. All three strings were replaced by a single 620V laboratory power supply. Every input G*x*+ is connected with a series resistance of 50Ω to the plus pole of the power supply. The AC-side is connected to the 230V / 50Hz grid. The switching frequency of the inverter section is set to 12kHz, while the switching frequency of the input half-bridges is set to 24kHz. The power at the AC-side is $P_A$ = 3.7kW. Additional measures against wind-up are taken in all controllers.

The first two plots show the grid voltage $u'_A$ and the grid current $i_A$, which is controlled sinusoidally. The power factor is set to $\cos(\varphi_{UI}) = 1$. The three input voltages $u_{Gx}$ in the third plot are held constant by the control system. The voltages $u_{C2}$ and $u_{C1} + u_{C2}$ are pulsating due to the single phase conversion. A high ripple on these voltages is permissible, which allows the usage of small film capacitors C2 and C3. The voltage $u_{C5}$ of the flying capacitor C5 is overlayed with a 12kHz ripple during the negative half-wave of $u_A$. The forth plot shows the currents $i'_{Dx}$ at the inductors L1*x*, that were sampled by the control system. The current ripple at one of the inductors L1*x*

can be seen in the fifth plot, as this measurement was taken with an oscilloscope. The proposed control structure leads to a stable system.

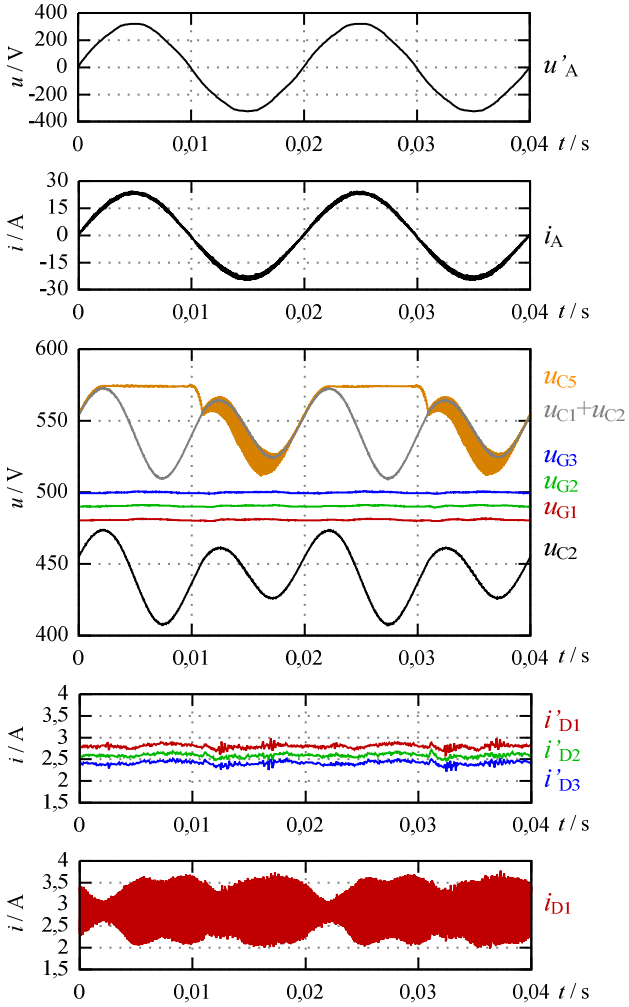



Fig. 13: Experimental results; Values with apostrophe (') are sampled values of the control system; Values without apostrophe are measured with an oscilloscope

## 5 Conclusion

A new transformerless photovoltaic inverter circuit is described in detail. It allows an individual MPP tracking of several strings, without needing a full scale boost converter for each string. Either the plus-poles or the minus-poles of all strings are connected to the neutral conductor N. Therefore, it is especially suited for thin-film or back-side contacted solar modules. The circuit generates a three level output voltage and is capable of delivering reactive power. An appropriate control scheme is presented. Experimental results proof the proper function of the circuit and of the control system.

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