Karlsruhe Institute of Technology

FAKULTÄT FÜR PHYSIK
Institut für Prozessdatenverarbeitung
und Elektronik (IPE)

Development of active CMOS sensors for particle physics experiments

Masterarbeit
von

Felix Ehrler

am Institut für Prozessdatenverarbeitung
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Referent: Prof. Dr. Marc Weber
Korreferent: Prof. Dr. Ivan Perić

Karlsruhe, den 10. November 2015

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1. Introduction

Around 2025 the Large-Hadron-Collider (LHC) is planned to receive an upgrade to increase its integrated luminosity to 3000 fb^{-1}, which is ten times the value of the original design. The high luminosity upgrade of the Large Hadron Collider (HL-LHC) will make accessible very rare processes, extend the search reach for so far unknown physics and enable precision measurements.

It is commonly accepted that the Standard Model of Particle Physics is not able to explain all observations in particle physics [1]. Therefore it needs to receive an extension or modification to describe all experimental results. The main issues of the Standard Model are:

- Gravity is not included in the Standard Model.
- Dark matter and dark energy are an explanation of astronomical observations, but are not represented in the Standard Model.
- It has been shown that neutrinos have a rest mass, however the exact number is not known yet. In the Standard Model neutrinos are considered massless. A new attempt to weigh neutrinos is the KATRIN experiment at KIT [2].
- The asymmetry of matter and antimatter in the universe can not be exclusively explained by the asymmetry effects in the Standard Model [3].

So it is obvious that the discovery of the Higgs Boson in 2012 [4] marks not the end of particle accelerators. On the contrary the detector experiments have to be further improved in order to discover more exotic particles with high mass or low generation probability. The goal is nothing less than finding the theory of everything that explains and unifies all physical aspects of the universe [5].

Improvement means in this context higher particle energy, higher spacial resolution and higher collision rate. To achieve all these requirements the respective collaborations have to improve existing technologies or develop new options with potentially better performance. In general improving a technology comes along with higher cost. A new approach on the other hand may promise a better or easier solution, however success can not be guaranteed.

High-voltage CMOS (HV CMOS) summarizes technologies which combines the usage of both voltages above 5 V and CMOS electronics on the same chip. The purpose of this thesis is to explore for which applications in high energy physics the HV CMOS AMS H35 technology is suitable and what it is capable of. Possible experiments to use HV CMOS are not only the LHC experiments, but also the proposed experiment Mu3e at the Paul Scherrer Institute (Switzerland) and the Belle II experiment at KEK (Japan).

The key properties and issues of HV CMOS sensors are:

a) The working principle of combining sensor diode and electronics on the same chip (MAPS). This leads to a reduction of material in the detector and grants higher

spacial resolutions, as it is not necessary anymore to have a bond connection per pixel.

b) The costs for HV CMOS chips are rather low, because these chips can be produced in a standard commercial process.

c) Detector chips have to be radiation tolerant. Radiation hardness has to be proven for HV CMOS chips.

d) HV CMOS chips are expected to consume more power than other technologies. It has to be shown that the power consumption stays within boundaries, even after irradiation. Excessive power consumption may lead to thermal runaway.

e) The HL LHC is planned to have a collision frequency of 40 MHz. This means that the detector chips have to have a time resolution of at least 25 ns.

Chapter 2 introduces the HV CMOS technology. Basic concepts and their usage in particle detectors are briefly discussed.

The main content of this thesis is the discussion of the measurement results in chapters 3, 4 and 5. Each chapter concentrates on a specific chip with individual properties. The used methods are explained when first occurring. Some results presented in these sections have already been published in [6] and [7]. Very specific information about certain topics can be found in the appendix section.

2. Basic Information on High-voltage CMOS Sensors

2.1 Silicon

Most semiconductor detectors use silicon sensors. Silicon is the semiconductor most used in any electronics, because it is easy to handle and well-understood. Silicon dioxide can be easily grown on silicon wafers and serves as both insulator and protection layer. Silicon's band structure (allowed electron states) can be determined by using the time-independent Schrödinger equation

$$\hat{H}\Psi\left(\vec{r}\right) = E\Psi\left(\vec{r}\right), \tag{2.1}$$

where the Hamiltonian is given by

$$\hat{H} = -\frac{\hbar}{2m}\nabla + V\left(\vec{r}\right). \tag{2.2}$$

where $V\left(\vec{r}\right)$ is a periodic potential caused by a silicon crystal lattice with periodicity $\vec{R}$:

$$V\left(\vec{r}\right) = V\left(\vec{r} + \vec{R}\right) \tag{2.3}$$

From this Bloch deduced the form of the solutions of the time-independent Schrödinger equation to be

$$\Psi\left(\vec{r}\right) = e^{i\vec{k}\cdot\vec{r}} \cdot u_{\vec{k}}\left(\vec{r}\right), \tag{2.4}$$

where $u_{\vec{k}}\left(\vec{r}\right)$ is a periodic function with the same periodicity $\vec{R}$ as $V\left(\vec{r}\right)$ [8] and $\vec{k}$ is the crystal wave vector. These solutions of this Schrödinger equation are called Bloch-waves.

The silicon band structure is shown in Fig. 2.1 as a reduced zone scheme. The band structure in the elementary cell of the three dimensional momentum space (Brillouin zone), is displayed in two dimensions by showing the dispersion relation along paths between certain points of high symmetry. Therefore it is important in which orientation a silicon crystal is cut into wafers, because different orientations have different electrical properties. Examples of such orientations are {110}, {100} or {111}.

Between the upper edge of the valence band labeled E_V and the lower edge of the conduction band E_C is the band gap

$$E_G = E_C - E_V. \tag{2.5}$$

Silicon is a group IV (group IV in the periodic table) semiconductor, because the Fermi level is located in the band gap and the band gap is small. For an insulator, the Fermi level is between two bands too, but the energy gap E_G is much bigger. The Fermi level of a metal is inside a band (Fig. 2.2). The band gap of a semiconductor is usually less than 4 eV. Silicon has a band gap of 1.107 eV at room temperature. Silicon is an indirect semiconductor. This means that the minimum of conduction band and the maximum

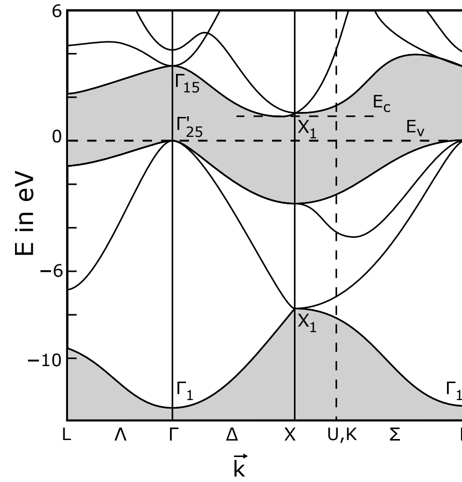


Figure 2.1: Band structure of silicon showed as reduced zone scheme, with the wave vector $\vec{k}$ on the x-axis and the energy on the y-axis. The upper edge of the valence band is labeled E_V, the lower edge of the conduction band E_C. In between the band gap is located. From [9], after [10]

of valence band are not at the same wave vector $\vec{k}$. For transition of an electron from the valence to the conduction band either a higher excitation energy than the band gap is necessary or a phonon has to participate in the transition process, to compensate the difference in wave vector $\Delta\vec{k}$.

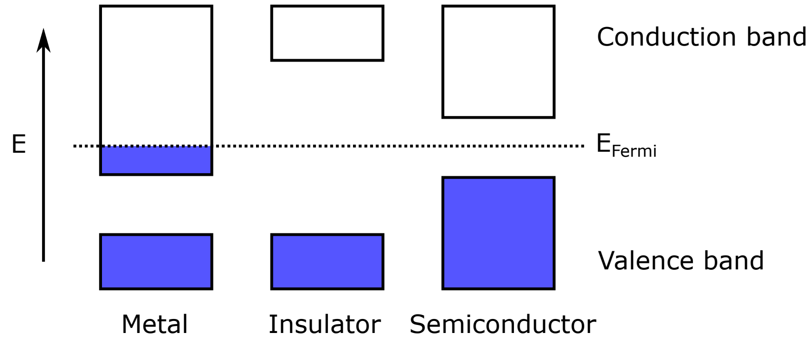


Figure 2.2: Simplified scheme of the band structure of a metal, an insulator and a semiconductor.

For $T = 0$ K a semiconductor behaves like an insulator, because there are no free electrons in the conduction band. Free electrons are not bound to a specific atom, but can move freely through the solid. For $T > 0$ K thermal excitation enables some electrons to move to the conduction band. These electrons, as well as the resulting holes, can participate in a possible current.

The fraction of electrons as a function of temperature in the conduction band, is given by the Fermi distribution:

$$f(E) = \frac{1}{\exp\left((E - E_F)/k_B T\right) + 1} \tag{2.6}$$

For $T = 0$ K this is a step function, which means that below a certain energy E_F all electron states are occupied, while above all are empty. For finite temperatures the step softens, resulting in empty states below and occupied states above E_F. Fig. 2.3 shows the Fermi distribution for several temperatures.

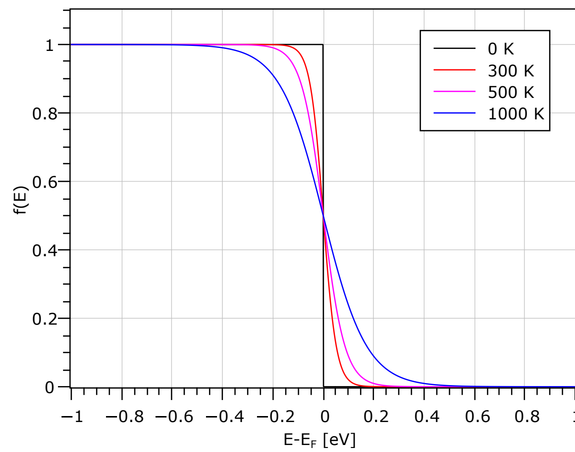


Figure 2.3: The Fermi distribution displays the fraction of occupied electron states over their energy for several temperatures.

2.1.1 PN Junction

As mentioned above silicon is an element of group IV in the periodic table. In other words it has four unpaired electrons in the outermost shell. In a crystal structure these electrons bond to neighbor atoms and form a tetrahedral lattice.

The electrical properties of a semiconductor can be varied by doping. Doping is the introduction of atoms other than silicon into the silicon crystal. Often elements of the III'rd or V'th group are used for doping. They fit in the silicon lattice, but cause a defect: In case of group III elements a hole occurs (p-doping, Fig. 2.4a), called electron acceptor; in case of group V elements an uncoupled electron occurs (n-doping, Fig. 2.4b), called electron donator. Typical doping concentrations are one impurity atom per 10^7 to 10^4 silicon atoms.

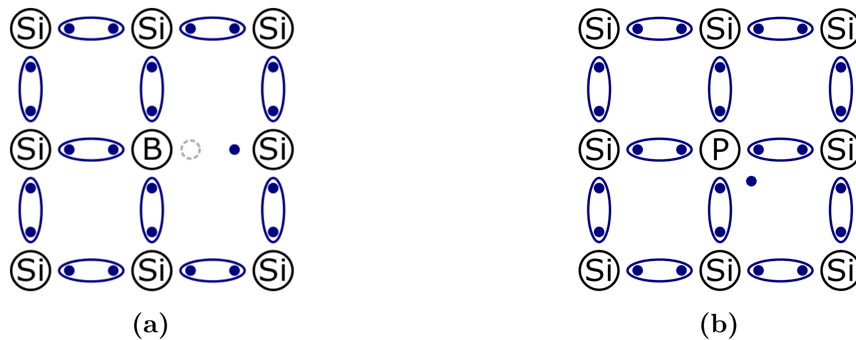


Figure 2.4: 2D representation of the defects induced by doping atoms.
a) Boron, a group III element, causes a hole.
b) Phosphorus, a group V element, causes a weakly bound electron.

How these defects change the Fermi energy is shown in Fig. 2.5 a). The weakly bound electrons of n-doped semiconductors need only little energy for transition to the conduction band, the Fermi energy is close to the conduction band. Electron conduction is made easy possible.
P-doping causes unoccupied electron states with energy levels close to the valence band. This moves the Fermi level close to it. Electrons from the valence band can easily occupy these states, leaving holes at their original position, which can be occupied themselves by other electrons again. With an externally applied bias voltage, it seems as if not the electrons, but the hole is traveling: a current with positive charge carriers identified as

holes is enabled. Silicon wafers have a typical resistivity of ρ = 10 Ωcm to 10^4 Ωcm. Doped silicon has a typical resistivity of ρ = 0.001 Ωcm to 1 Ωcm.

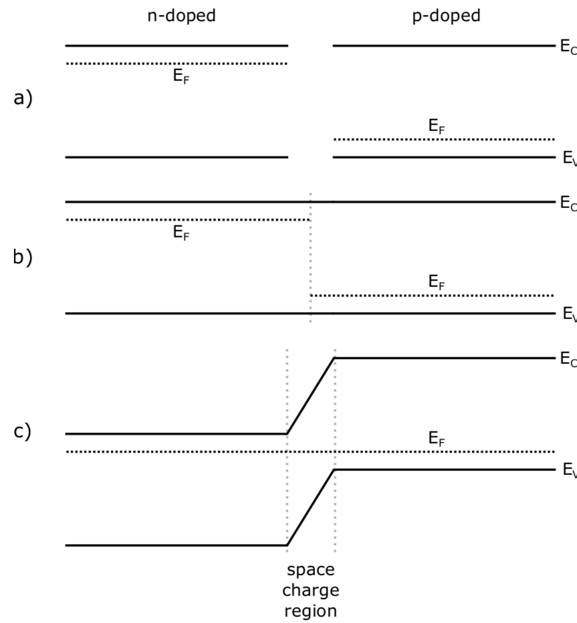


Figure 2.5: Fermi levels for n-doped and p-doped silicon.

Bringing a p- and an n-doped semiconductor into contact, as shown in Fig. 2.5 b), leads to a problem: the Fermi level should be constant in the whole material, but the distance to the bands is also fixed. As a consequence the bands are bent as shown in Fig. 2.5 c). The weakly bound electrons of the n-doped area diffuse into the p-doped area and 'fill' the holes there. This has two effects:

- An electrical field builds up, because the p region is charged negatively and the n region positively.
- The amount of free charge carriers drops both in the n and the p region near the interface. The area nearly without free charge carriers is called "depletion region".

The diffusion process continues until the Fermi levels are equal. Positive charge carriers have moved to the n-doped area and negative charge carriers have moved to the p-doped area. Now the n- and p-type region close to the connection are charged. Thus the depletion region is also called: space charge zone. The diffusion process is finally stopped by the electrical field, caused by these charges.
An externally applied bias voltage increases or decreases the width of the depletion zone depending on the polarity.

2.1.2 Metal-Oxide-Semiconductor Field Effect Transistor

A Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is a voltage-controlled resistor. The resistance between source and drain is controlled by the voltage applied to the gate. If the resistivity is low enough, an applied source-drain voltage leads to a current from source to drain. Fig. 2.6a shows the schematic of a simple n-type MOSFET, with an applied gate voltage U_{GS} below the threshold voltage U_{th}. In case of a p-type MOSFET, everything is inverted. Source and drain are n-doped implants with high donator density. At their interface to the p-doped substrate they form a depletion zone (cf. chapter 2.1.1). This depletion zone blocks the current between source and drain. The gate electrode is separated from the substrate by an insulating oxide layer. Source, drain and gate are contacted by a metal layer.

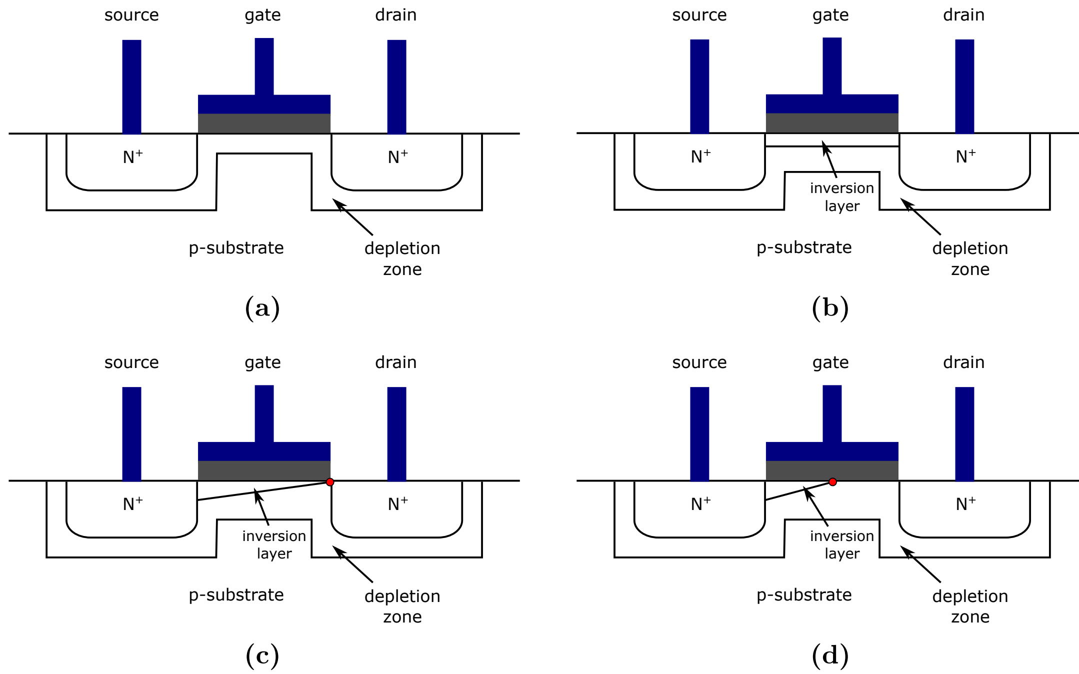


Figure 2.6: The different operation states of a MOSFET. (After [11])

We distinguish three operation regions: If a gate voltage $U_{GS} \geq U_{th}$ is applied, a conducting channel below the gate electrode is formed (Fig. 2.6b). This channel is n-conducting, even though it is in p-type substrate. Because of the inversion of the majority charge carrier, this layer is also called inversion layer. A voltage between source and drain $U_{DS} < U_{GS} - U_{th}$ causes a current I_{DS} proportional to U_{DS}. This operation region is called ohmic or linear region, because the transistor behaves like a resistor.

Higher U_{DS} change the shape of the inversion layer. The charge carriers are pulled towards the source and the inversion layer becomes rather wedge-shaped. At a critical voltage $U_{DS} = U_{GS} - U_{th}$, the tip of the wedge is right at the drain (red dot in Fig. 2.6c). This effect is called pinch-off and the source-drain current I_{DS} saturates. This operation region is therefore called saturation region.

For $U_{DS} > U_{GS} - U_{th}$ the pinch-off point moves toward the source (Fig. 2.6d). The current stays constant.

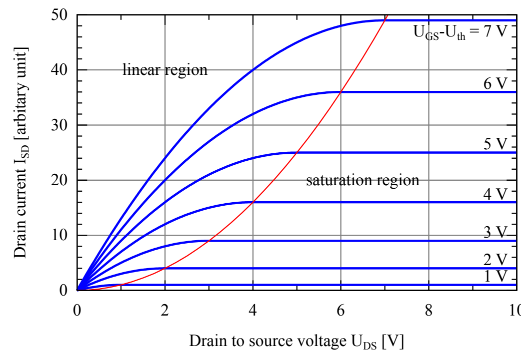


Figure 2.7: MOSFET behavior for several settings. (From [12])

Fig. 2.7 shows the characteristic I-V-curves for several U_{GS}. The slopes of these curves in the saturation region are called transconductance g_m. The transconductance can be calculated:

$$g_m = \frac{2I_{DS}}{U_{GS} - U_{th}} \tag{2.7}$$

2.2 Detector Functionality

The signal path is the same in all silicon detectors: The signal is generated as mobile charges in silicon, the charge is collected, converted to a voltage, amplified and finally read out (Fig. 2.8).

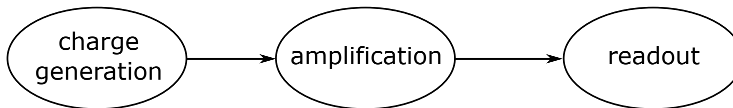


Figure 2.8: Basic idea of silicon particle detectors.

2.2.1 Charge Generation in Silicon

The working principle of a silicon detector is charge generation in silicon. Electron-hole pairs are generated when energy is deposited by particles in the silicon substrate.

Photons are annihilated when hitting an atom in the substrate. This means all energy is deposited in one point and all charges are created there (Fig. 2.9).

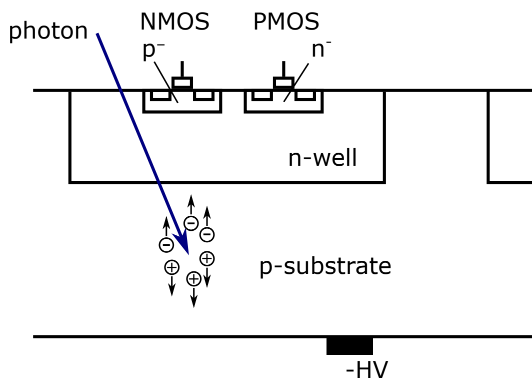


Figure 2.9: Charge generation by photons or X-rays in silicon. A photon is annihilated on hit and deposits all energy in one spot. The generation of electron-hole pairs takes 3.6 eV per pair.

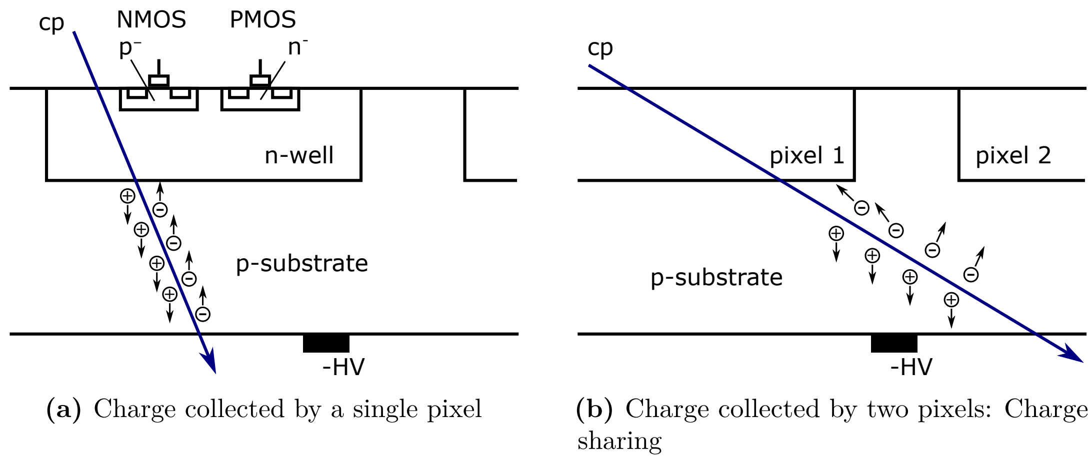
Charged particles interact with the atoms along their path (Fig. 2.10). This means that the generated charges are distributed over a larger area. Furthermore the total amount is not only dependent on the energy of the incoming particle, but also on the path it takes.

The energy loss per traveled distance $-\frac{dE}{dx}$ is given by the Bethe-Bloch formula [13, 14]:

$$-\frac{dE}{dx} = \frac{4\pi n z^2}{m_e c^2 \beta^2} \cdot \left(\frac{e^2}{4\pi\varepsilon_0}\right)^2 \cdot \left[\ln\left(\frac{2m_e c^2 \beta^2}{I \cdot (1-\beta^2)} - \beta^2\right)\right] \tag{2.8}$$

with $\beta = v/c$, the particle speed v, vacuum speed of light c, particle energy E, traveled distance x, particle charge $z \cdot e$, vacuum permittivity ε, electron density of the material n, electron mass m_e and excitation potential I. This function has a minimum for a certain particle and material. A particle with this minimum energy is often referred to as a minimum ionizing particle (MIP). A handy source for MIPs is ^{90}Sr [15, 16], because:

- it has a long half-life of 28.5 years,
- its decay sends out β particles with an energy of 0.546 MeV, which is close to the MIP energy, and



(a) Charge collected by a single pixel

(b) Charge collected by two pixels: Charge sharing

Figure 2.10: Charge generation by charged particles (cp) in silicon using a MAPS as an example. The electron-hole pairs are generated along the particle path. The configuration of a MAPS sensor used here will be explained in the next section.

- neither ^{90}Sr, nor the secondary decay of ^{90}Y produce photons, which could disturb the measurement.

The ionization energy of silicon is 3.6 eV, this means that per 3.6 eV deposited energy one electron-hole pair is generated. The charge generated by a MIP is thereby 75 electron-hole pairs per μm path length in silicon [17]. This amount can be reduced further by the effect of charge-sharing between two pixels, illustrated in Fig. 2.10b.

The total charge generated in the collection region of the detector is dependent on its thickness. The collection region is the depletion zone between p-substrate and n-well. Charges generated in other regions recombine and can not be collected. The electric field in the depletion region separates the electrons and holes, so most do not recombine. On the back side of the detector chip a high bias voltage can be applied, both for widening the depletion zone and improving the charge collection efficiency.

To sum up: The hardest particle to detect is a MIP, which traverses the detector vertically, exactly in the middle of two pixels. This means it generates a signal of

$$\frac{75\ e}{\mu m}/2 = \frac{37.5\ e}{\mu m}, \tag{2.9}$$

which needs to be detected by the electronics.

2.2.2 Monolithic Active Pixel Sensors

The monolithic active pixel sensor (MAPS) concept combines pixel diode and readout electronics on a single chip (cf. Fig. 2.10). It often uses 'smart pixels', which means that the signal is not only generated, but also processed in the pixels. Further electronics on the periphery of the chip are used to process the signal [18].

All chips investigated in this thesis are HV CMOS MAPS produced in the AMS H35 (350 nm) technology. HV stands for 'high voltage', which refers to the usage of a depletion voltage of up to 120 V. CMOS means that both NMOS and PMOS transistors are used. The used substrate has a resistivity of 20 Ωcm.

This combination of technologies brings many advantages:

- MAPS require less material in the detector than approaches with multiple chips. Further MAPS can have a higher spacial resolution, because the hit signals can be

digitized on the MAPS itself. That means that a digital bus with few connections is sufficient for communication between involved chips. Designs without on-chip signal processing require a connection for each pixel. This defines a minimum pixel size. The signals are processed on-chip and only the relevant information is sent to readout. The smart pixels of CMOS MAPS amplify the and can even conduct first steps in the readout process. CMOS means that both NMOS and PMOS transistors can be used. This makes it possible to design small and efficient in-pixel circuits.
In case of detector chips without readout electronics the hit signals of each pixel has to be transmitted to a readout chip (ROC). The output of the in-pixel amplification is strong enough to transmit the hit signal capacitively to the ROC [19]. This grants a higher spacial resolution than the conservative bump bond connection, even if a separate readout chip has to be used.

- Charge signals can be collected by drift in a large depletion zone, if high voltage is used. Collection by drift is faster and more efficient than diffusion.
- The count of electron-hole pairs generated in the sensor diode is proportional to the way length in the depletion zone. The width of the depletion zone depends on the depletion voltage. This means that a high depletion voltage leads to a strong signal.
- The AMS H35 process is a commercial 350 nm standard technology, which is cheaper than highly specialized technologies needed for other approaches. AMS H35 is also used for "applications in the automotive and industrial segment" [20].

All together HV CMOS is an interesting technology enabeling innovative designs. It brings the advantages in material budget, spacial resolution and price. However it brings also challenges, which have to be dealt with:

- The power consumption is expected to be higher in detectors using HV CMOS technology. The power consumption is limited by the cooling capacity of the detector.
- Detectors for high energy physics have to be radiation tolerant, because the detected particles are also damaging the detectors. The radiation hardness of HV CMOS sensors in AMS H35 has not yet been proven.
- Most detector experiments operate at a very high rate, LHC for example has only 25 ns between two bunch crossings. This means that the time resolution of all used detector systems has to be better than 25 ns. Basic HV CMOS circuits in AMS H35 do not meet this requirement, however there are approaches to solve this problem. One of these approaches is investigated in chapter 3.6.3 and 5.2.

2.2.3 Signal Amplification

In order to convert the generated small charge into a strong voltage signal, a charge sensitive amplifier (CSA) is used. An enclosed source follower strengthens the signal (Fig. 2.11). In case of a simple CSA, the feedback is just a capacitor. A better design is to use a variable additional coupling between output and input. This is realized by a feedback transistor, which continuously resets the signal. The state of this feedback transistor can be adjusted to a changed behavior of the chip after irradiation by changing VNFB.

The circuit diagram of amplifier, feedback and source follower is shown in Fig. 2.12. The amplifier itself is an advanced cascode with variable settings. Its main bias current is set by transistor T_2, the input is connected to transistor T_1. The voltage VPload sets the load transistor current. The voltage Vcasc is a constant external voltage.
The feedback capacity is not shown, because it is not a separate component. The feedback capacity occurs between the implants of the VPload transistor and the sensor diode, above

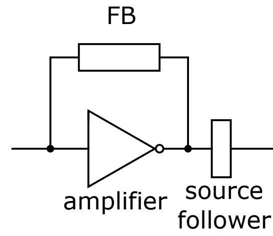


Figure 2.11: Amplifier and source follower as block diagram.

which this transistor is located. The continuous reset is realized by the transistor T_{FB} which is controlled by VNFB.
A source follower is connected to the amplifier's output. It serves as impedance converter. The baseline voltage BL and baseline resistance BLR define the comparator's input baseline, which is in case of hits modulated by the source follower's output.
The supply voltages are set to Vdda = 3.3 V and Vssa = 2.5 V.

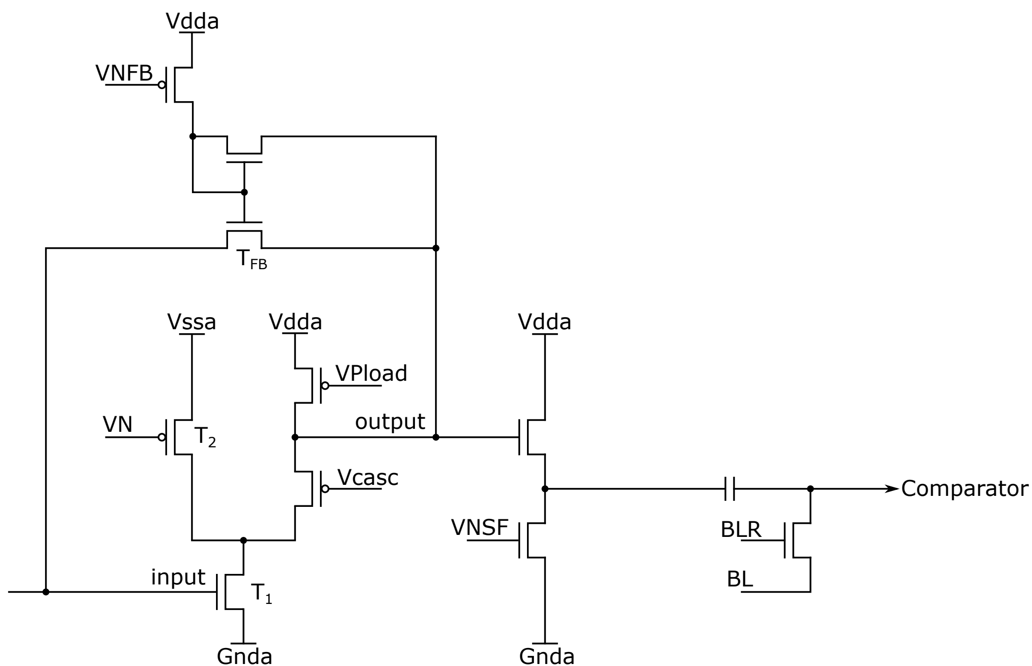


Figure 2.12: Circuit diagram of amplifier and source follower on transistor level.

2.2.4 Signal Readout

The prototype HVStripV1 discussed in the following chapter offers the possibility of a digital readout. The capacitively coupled pixel detector discussed in chapter 4 CCPDv1 sends its analog hit signals to a separate readout chip. A different version named CCPDv2 generates boolean time walk compensated hit information.

Both HVStripV1 and CCPDv2 generate boolean hit information per pixel by comparing the analog signal to a set threshold. Is the signal strong enough (above the threshold), a logical 1 is generated (Fig. 2.13). In case of the HVStripV1 this information is processed further to obtain a digital output containing the hit pixel's address or hit pixels' addresses.

The output signal of the source follower modulates the baseline (set by BL in Fig. 2.12). The adjacent comparator compares the modulated baseline voltage to a set threshold Th. Is the input signal higher than this threshold, the comparator's output is high, otherwise

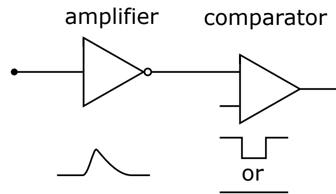


Figure 2.13: The comparator translates an analog signal into a boolean signal.

low. The common source stage strengthens the output signal. Fig. 2.14 shows the layout of a normal comparator on transistor level.

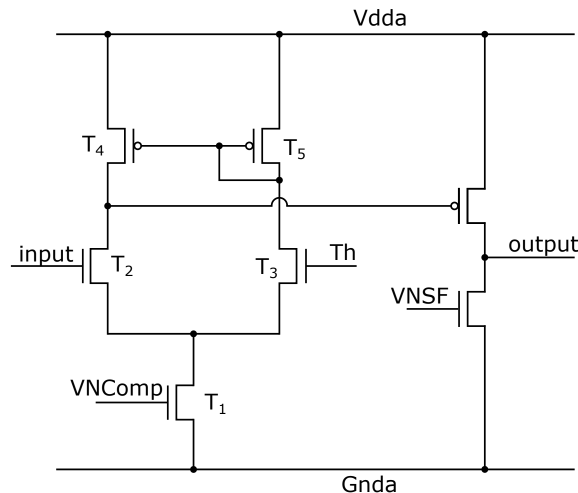


Figure 2.14: A normal comparator compares the input to a set threshold. A common source stage strengthens the output.

At this point the signal is translated into either high or low. This means we have a digital signal now, which can be combined in a readout block with hit information, like pixel number or timing.

The comparator is actually a differential amplifier, with its positive input (T_2) connected to signal input and its negative input (T_3) connected to threshold (Th). The current through the comparator is biased by T_1. The current mirror (T_4 and T_5) stabilizes the current in the arms of the differential amplifier. The common source finally stage strengthens the output.

2.3 Radiation Damage in Silicon

One challenge detectors in collider experiments have to meet is the high radiation field close to the interaction point. The expected hadronic fluence in the tracker of ATLAS for example is up to $1 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$ and additional 600 kGy ionizing dose. This radiation causes damage in the silicon structures, which changes the the performance of the detector.

We distinguish two radiation types cause different defects: Hadrons create both bulk and surface damage, while γ-rays cause only surface damage.

2.3.1 Bulk Damage

Particles passing through the detector generate not only electron-hole pairs, which are the wanted signal, but also interact with the atomic lattice. If the interaction is strong enough to knock off atoms, it leaves defects behind: An unoccupied lattice position is called

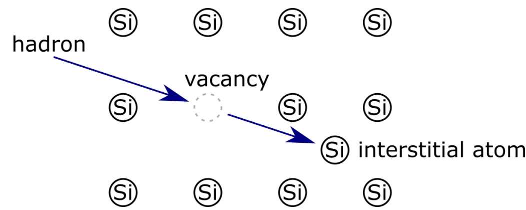


Figure 2.15: Point defect generation by hadrons.

vacancy, an additional atom in between lattice-atoms is called interstitial atom (Fig. 2.15). If interstitial atom and vacancy stay close together, this defect is called Frenkel defect [21].

A single particle may generate several of such point defects along its path, if it carries sufficient energy. Furthermore knocked off atoms can cause additional damage to the lattice as well. Often such atoms cause cluster defects at the end of their path (Fig. 2.16).

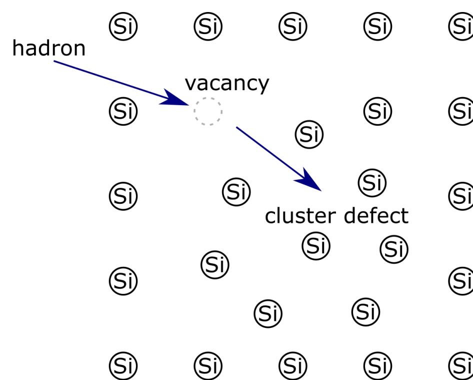


Figure 2.16: Cluster defect generation by hadrons.

Even though both protons and neutrons are hadrons, their effect on silicon is not the same. Protons interact mostly by Coulomb interactions, while neutrons have to hit atoms to interact. Coulomb interaction can transmit arbitrary energies. Weak interaction (hits) transfers a big amount of energy to the hit atom, which most likely ends up causing a cluster defect. This is why neutrons cause rather cluster defects than point defects, while protons cause both point and cluster defects.

For comparison of the damage caused by diverse particle types the NIEL-scaling hypothesis is used. The assumption made is that in Non-Ionizing-Energy-Loss (NIEL) processes the damage induced is proportional to the deposited energy. A hardness factor κ depending on particle energy and particle type is introduced:

$$\kappa = \frac{\text{Damage caused}}{\text{Damage caused by 1 MeV neutrons}} \tag{2.10}$$

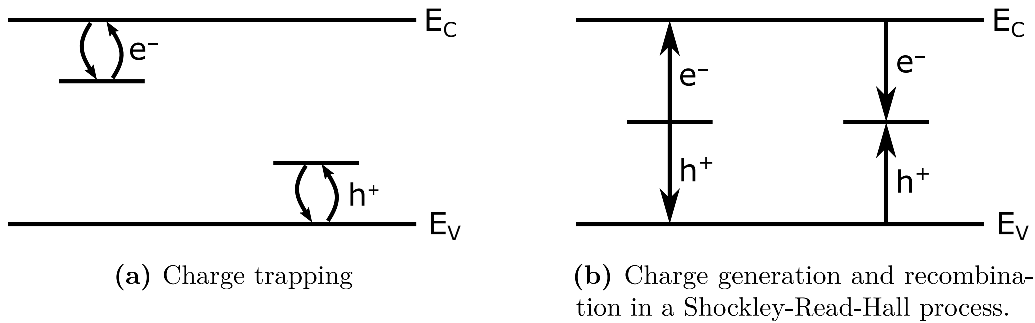
All together the neutron equivalent fluence of an irradiation can be calculated and has the unit $\mathrm{n_{eq}/cm^2}$.

The described defects in the silicon bulk have three main effects:

Shallow traps: The different defects create energy levels in the band gap of silicon. If those energy levels are close to either valence or conduction band, charge carriers can be trapped in them (Fig. 2.17a).
This means for a particle detector that its signal is reduced. The thicker a detector is, the longer is the path of charges to the electrodes, and thereby the probability of getting trapped.

Generation current: Energy levels in the middle of the band gap serve as generation/recombination centers (Fig. 2.17b). This means that charges can be generated by an applied voltage and cause a generation current. This bipolar process is called Shockley-Read-Hall process [22].
This current is measured as a leakage current of a pixel diode. A rise in leakage current causes increased shot noise, which is amplified by the detector's electronics.

Change in effective doping: The new defects can serve either as electron acceptors or donors. This effect can change the effective doping. Depending on the relation of the created acceptors and donors even the type of effective doping can be changed by irradiation. If an n-type (p-type) region changes to become p-type (n-type), the term type-inversion is used.
Type inversion changes the depletion voltage (respective depletion thickness) is the result in case of sensor diodes. Type-inversion can prevent depletion of the pixel diode at all, which leads to much reduced signal and a big leakage current.



(a) Charge trapping

(b) Charge generation and recombination in a Shockley-Read-Hall process.

Figure 2.17: Bulk defects in silicon act as shallow traps (a) or generation/recombination centers (b), depending on their energy level.

2.3.2 Surface Damage

Surface damage is caused by ionizing radiation, photons and charged particles. Here surface damage by the example of X-ray irradiation is discussed. The surface consists of silicon dioxide, in which electron hole pairs are generated by the incoming radiation. These pairs do either recombine, diffuse or cause one of the following effects:

Oxide trapped charge: Charges are trapped in the oxide layer. This effect anneals quickly.

Fixed oxide charge: The electrons leave the SiO_2, while the holes are trapped close to the Si-SiO_2 interface. This region has many deep hole-traps, because the atoms there are highly disordered. The holes are strongly bound, which slows down the annealing process. The resulting electrical field affects the electronics (Fig. 2.19).

Interface traps: The interface of Si and SiO_2 has dangling bonds, because the lattices do not fit to each other. In production these interface traps are passivated by H-atoms. Irradiation removes the H-atoms and leaves the dangling bonds behind. Interface traps cause energy levels in the middle of the band gap, which contribute to the surface current.

One result of those effects is the appearance of surface currents:

- A surface current can connect two pixels and thereby cause crosstalk.
- Usually the collection region of the sensor-diode is separated from other structures by a guard ring. If surface currents are present, not all charges generated in the active area are collected, but instead diffuse to other structures (Fig. 2.18). Further some charges are caught by interface traps. This reduces the signal and increases the noise.

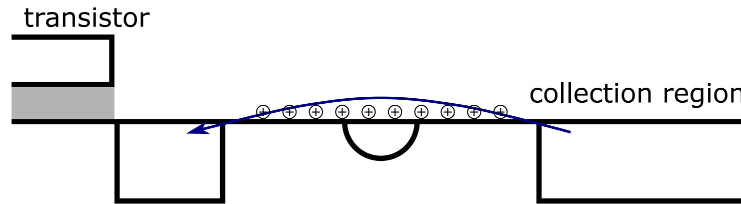


Figure 2.18: Surface charges can make surface currents possible from the sensor-diode's surface connector to transistors past guard rings.

- Transistors show increased leakage currents, because they feature Si-SiO_2 interfaces in the region of the gate (gate-oxide). As a result the transistor can not be turn off properly anymore (Fig. 2.19).

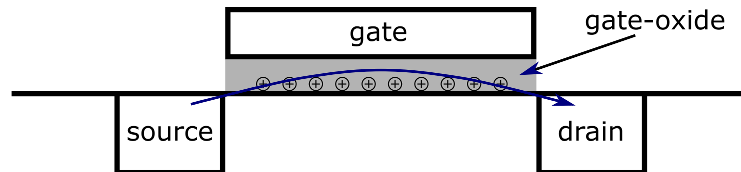


Figure 2.19: Radiation induced charges in the gate oxide of transistors cause a leakage current.

2.3.3 Annealing

As mentioned before, some radiation defects of the silicon chip are reversible. Some annealing effects happen immediately, like the recombination of electron-hole pairs in the Si-SiO_2 interface. The remaining defects are often mobile and the mobility is highly dependant on temperature. Radiation-induced defects can only anneal when they are mobile. As the mobility of all defects depends on temperature, the annealing is also depending on the temperature. While low temperatures are desirable with respect to leakage current, a high temperature accelerates annealing. For the LHC, the silicon detector chips are cooled while in operation, but could be warmed up while maintenance. This means the leakage current is minimized when taking data, but annealing is possible between measurement cycles.
Annealing is not always beneficial. Oxygen enriched silicon shows reverse annealing after long annealing times [23].

3. Characterisation of the HV CMOS Sensor HVStripV1

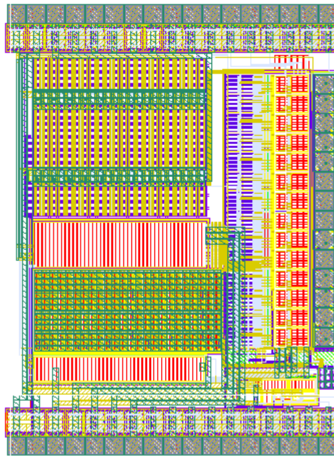


Figure 3.1: Layout of the HVStripV1 chip

Silicon strip detectors are in use at almost any particle physics experiment for example at ATLAS or CMS at CERN. The HVStripV1 chip is a CMOS test chip. It is produced in AMS H35 technology, designed to evaluate the high-voltage CMOS (HV CMOS) technology for detector experiments in high energy physics. This chip is meant to demonstrate both radiation hardness and overall performance of the HV CMOS technology. In case of success, HV CMOS is an alternative option for upcoming upgrades of existing detectors and the detectors of new experiments.

As HV CMOS technology is new to experiments of this scale, the design has to be optimized to meet all requirements and grant the best performance. This is accomplished by compiling different designs for most functions along the signal path (Fig. 3.2). The test chip serves to clarify which design detail, at its respective position along the signal path, is best to cope with the conditions in a high-energy physics experiment.

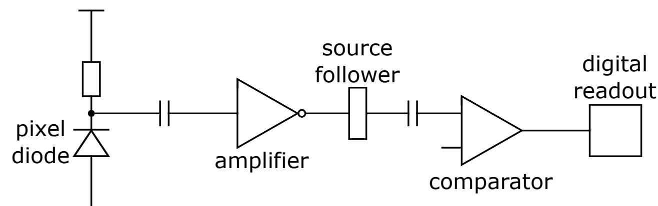
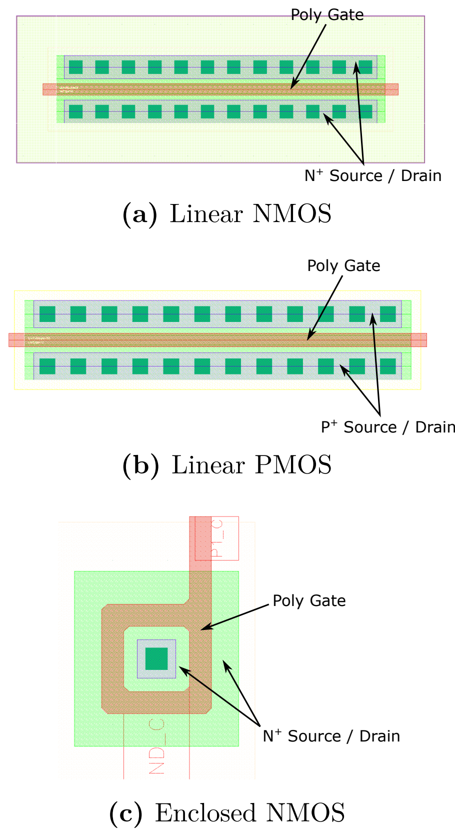


Figure 3.2: Simplified signal path of HVStripV1

The signal is generated in the pixel diode by charged particles passing through the active area. A charge-sensitive amplifier and a source follower convert the generated charges to a

voltage signal and shape it. This analog signal is digitized by a comparator. Signals can be injected electronically into the pixel diode (analog injection) or after the comparator into the readout part (digital injection). The signal can be read out after the amplifier (analog readout) or digitally. The digital readout is possible directly after the comparator of a pixel via HitBus. The HitBus can be connected to the digital output of an arbitrary pixel for external signal analysis. This options monitors only a single, predefined pixel. The second option is to read out from the readout block. This option monitors the whole chip. Up to three simultaneous hits can be read out in this mode.

The first question to be investigated is if linear or enclosed NMOS transistors in the amplifier perform best. Linear NMOS transistors are smaller and grant a higher gain, because they can have small transconductance g_m as well, but are not as radiation tolerant as enclosed NMOS transistors. Fig. 3.3 shows the layout of the different transistor types. Linear NMOS transistors are used in the amplifiers of pixels no. 0-7 and no. 22-29. Enclosed NMOS transistors are used in the amplifiers of pixel no. 8-21 and no. 30-43.



(a) Linear NMOS

(b) Linear PMOS

(c) Enclosed NMOS

Figure 3.3: Layout comparison of the three basic transistor types.

An issue for big detector experiments is the timing. For example, the time resolution required for ATLAS experiment is 25 ns or less. This can not be achieved with a standard design because of the time walk effect. The time walk effect is caused by the amplifier, which shows different slopes of the signal's rising edge for different signal heights (cf. chapter 3.6.3). This chip offers a dedicated time walk compensating comparator (TWCC) as a solution to this problem. For direct comparison and evaluation each chip has a normal comparator and a TWCC.

A scheme of the HVStripV1 chip is shown in Fig. 3.4. The chip is organized in 22 × 2 strip-style pixels (red). The amplifier of each pixel is located inside its pixel, therefore we speak about active pixels. The further electronics (comparators, readout, etc.) are placed

outside the pixels in a digital block (yellow, grey, green). The test structures are displayed in blue.

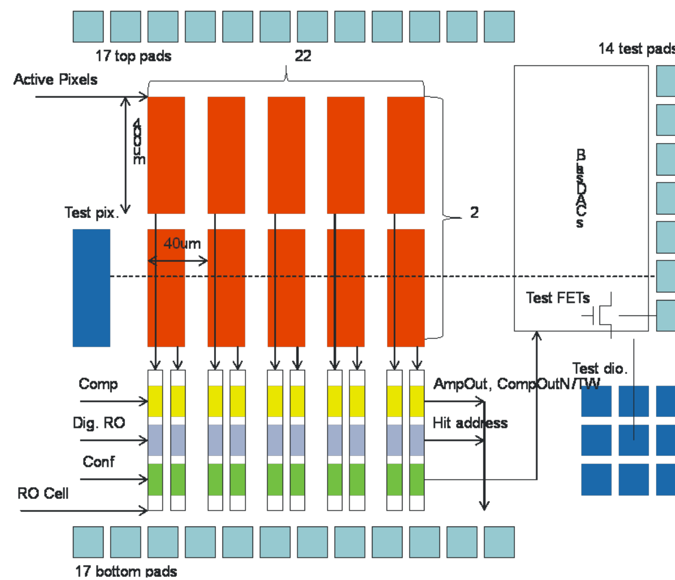


Figure 3.4: Schema of the HVStripV1 chip (Graphic: I. Perić)

Each strip style pixel consists of five diodes on each side of a bigger diode, which contains the electronics (Fig. 3.5). The total diode fill-factor is 34%. The fill-factor states the ratio between sensitive and total sensor area.

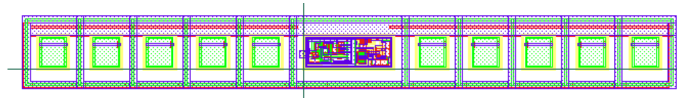


Figure 3.5: Layout of a single strip style pixel. (Graphic: I. Perić)

Further the HVStripV1 chip offers test structures to investigate the impact of radiation on a HV CMOS systems:

Array of pixel type diodes
An independent passive array of 3×3 pixel type diodes. Each diode's size is $33\ \mu m \times 33\ \mu m$. These diodes can be measured in groups to simulate the effect of a guard ring.

Big diode
By the size of $40\ \mu m \times 400\ \mu m$ this diode is much bigger than the ones mentioned above. It has the same size and shape as the active pixels. However this test pixel lacks the electronics inside the deep n-well. On the big diode the effect of radiation damage on the leakage current can be measured.

Test transistors
To evaluate the radiation hardness of CMOS electronics there are three single MOSFETs located on the chip. One of each type:

- linear NMOS
- enclosed NMOS
- PMOS

Each input characteristic can be measured independently.

The following chapters 'follow' the hit signal from being created in the pixels to being read out.

3.1 Pixel Diode

The number of electrons generated by a charged particle passing through the pixel diode is directly proportional to the thickness of the depletion zone. More electrons cause a stronger signal and therefore higher signal-to-noise ratio. The thickness is given by

$$d = \sqrt{\frac{2\varepsilon}{q}\frac{N_A + N_D}{N_A \cdot N_D}\Delta U} \tag{3.1}$$

with

$$\Delta U = U_{ext} + U_D \tag{3.2}$$

$$\Delta U = U_{ext} + \frac{k_B \cdot T}{q}\ln\left(\frac{N_A \cdot N_D}{n_i^2}\right) \tag{3.3}$$

3.1.1 Leakage Current

An un-irradiated diode array shows a very low leakage current. This keeps both power consumption and shot noise (see App. C.1) low. Power consumption should be always taken into account when designing a chip, as high power consumption leads to an increase in temperature, which has to be dealt with. The heat loss must not exceed the cooling capability of the detector, which is limited.

It is very important to keep a low noise generation at first amplification stage. Any noise generated at this stage will be amplified in the same way as the signal by the following amplifier stages.

Fig. 3.6 shows the measured leakage current over the applied bias voltage. A fresh un-irradiated chip shows only a very small bias-leakage current of 17 nA (< 0.4 nA per strip). After being irradiated with X-rays[1] to a total dose of 600 kGy, the leakage current increases to 128 nA (2.9 nA per pixel, ≙ ×7.5 current of an un-irradiated chip). In case of proton irradiation[2] to $2 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$ the bias current increases to 61000 nA (1386 nA per pixel, ≙ ×3600 current of an un-irradiated chip). The generated bulk defects act as generation/recombination centers, which are able to establish a current through the depletion zone (cf. Fig. 2.17b).

As the effect of proton irradiation on the diode structure turned out to be so significant it requires further investigation. A way to reduce leakage current in semiconductors is to cool them. By cooling the chip down to −20 °C the leakage current can be reduced by a factor of 38 to 1600 nA (36 nA per pixel).

The leakage current in diodes is mostly caused by charge generation [24]. The temperature dependency for generation in silicon is therefore given by

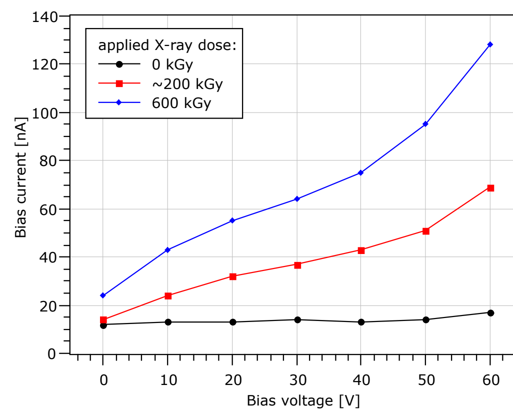
$$I(T) \propto T^2 \exp\left(-\frac{1.21\ eV}{2k_B T}\right) \tag{3.4}$$

with T being the temperature and k_B the Boltzmann constant. This formula has been fitted to the data in Fig. 3.7 in the following form:

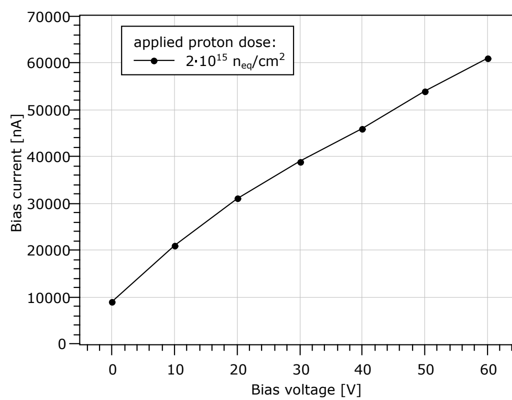
$$I(T) = a \cdot T^2 \exp\left(-\frac{b}{T}\right) \tag{3.5}$$

[1] Irradiation conducted at the IEKP irradiation facility. Most probable energy of the X-rays is 35 keV. For details see appendix B.

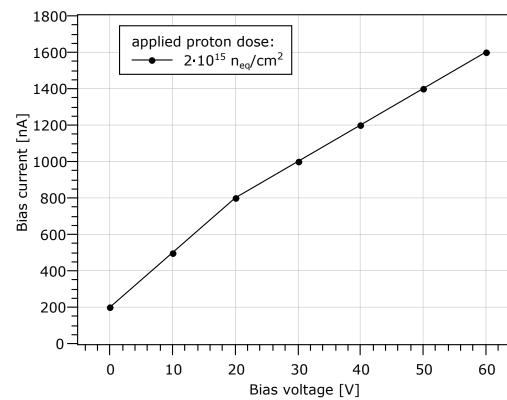
[2] Irradiation conducted at the ZAG Zyclotron AG with 23 MeV protons. For details see appendix B.



(a) X-ray irradiated diodes



(b) Proton irradiated diode at 20 °C



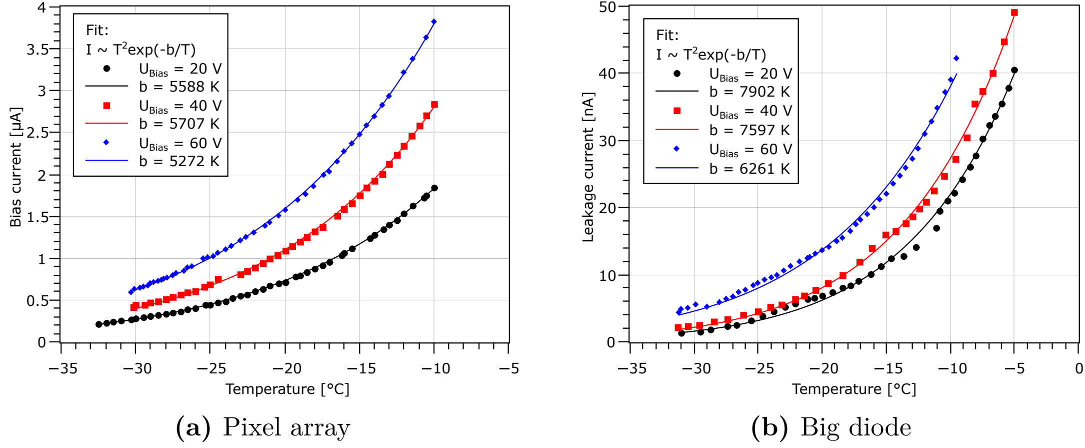
(c) Proton irradiated diode at −20 °C

Figure 3.6: The leakage current of the diodes in the pixel array as a function of bias voltage.

In this form is

$$b = \frac{1.21\ eV}{2k_B} = 7019\ K. \tag{3.6}$$

Overall the measured data fit this theory well. The measured band gaps of silicon E_g (included in b) are in the same order as the calculated value. The leakage current was measured also on the test structure big diode. The results from measuring the big diode are closer to the theoretical value than the results from the pixel diodes. This is obvious, because the pixel array has attached electronics and periphery, which influence the measurement. Nevertheless the shapes of the $I\,(T)$-curves of both measurements are in agreement with Eq. (3.4).



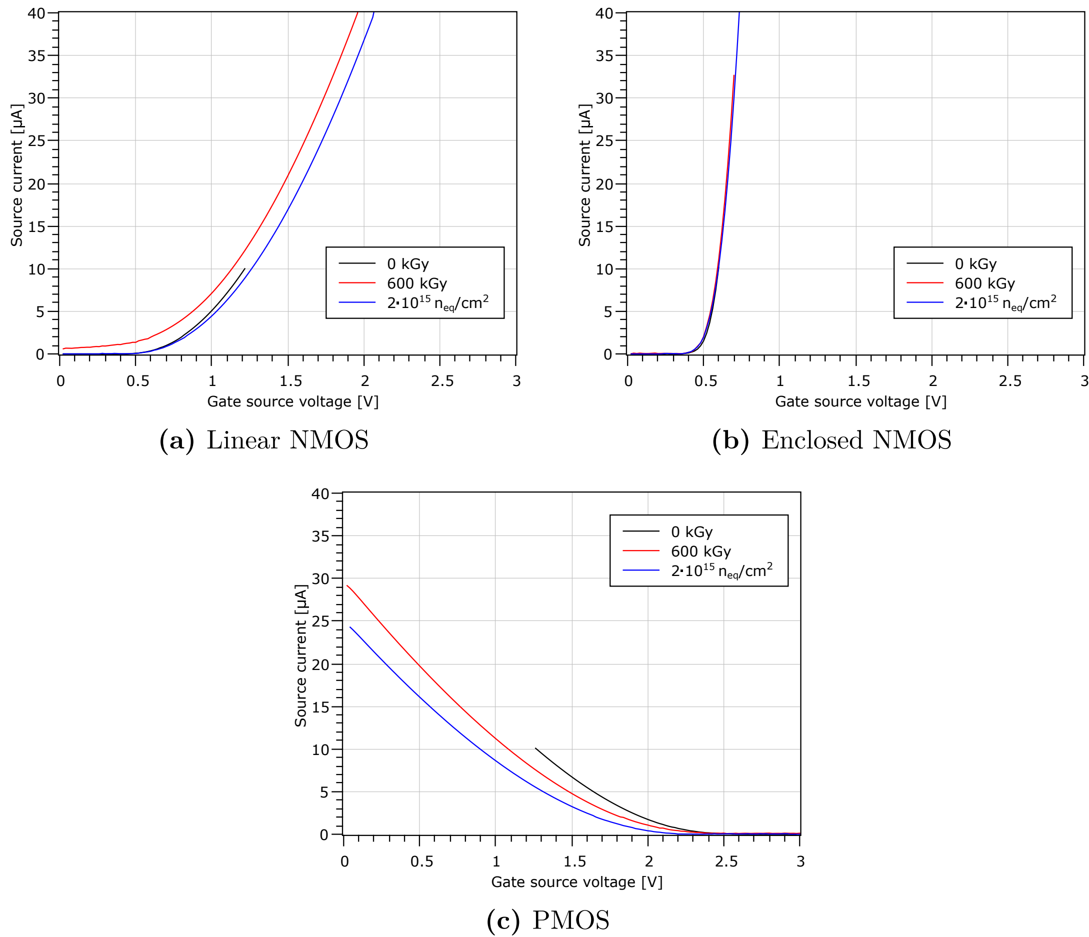
(a) Pixel array **(b)** Big diode

Figure 3.7: Leakage current as a function of temperature for $U_{Bias} = 20$ V, 40 V, 60 V. The uncertainty in temperature of each measurement point is ±2°C, which is not shown in the diagram to retain clarity.

3.2 Transistor Input Characteristics

CMOS technology offers two basic types of transistors. The NMOS transistor conducts electrons, PMOS holes. NMOS is open for positive U_{GS}, PMOS for negative U_{GS}. PMOS transistors are considered radiation tolerant whereas linear NMOS transistors tend to suffer from radiation damage. As CMOS uses both types, this problem led to the development of enclosed NMOS transistors. The enclosed version of NMOS transistors is meant to be very radiation tolerant. However the new design has also some issues. The gain of amplifiers using this design is reduced, because the transconductance g_m is always high. Furthermore enclosed transistors require much more space on a chip than their linear counterparts (cf. Fig. 3.3).

In order to evaluate the advantages and disadvantages of each design the source current I_{DS} has been measured while varying the gate-source voltage U_{GS}. The drain-source voltage was kept constantly at $U_{DS} = 3.3$ V. After the chips were exposed to a certain radiation dose these measurements were repeated. One chip was irradiated with an X-ray tube in several steps to a total dose of 600 kGy. Another chip was irradiated with protons to a dose of $2 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$ in a single irradiation session. The curves obtained by this measurement are shown in Fig. 3.8.



(a) Linear NMOS

(b) Enclosed NMOS

(c) PMOS

Figure 3.8: The input characteristics of the three transistor types before and after irradiation. One chip was irradiated with an X-ray tube in several steps to a total dose of 600 kGy. Another one was irradiated with protons to a dose of $2 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$ in a single step.

The PMOS transistor was affected by the irradiation, but only in matters of slope. The transistor still blocks the source-drain current I_{DS} at about the same U_{GS}, as it did in the un-irradiated state (Fig. 3.8c).

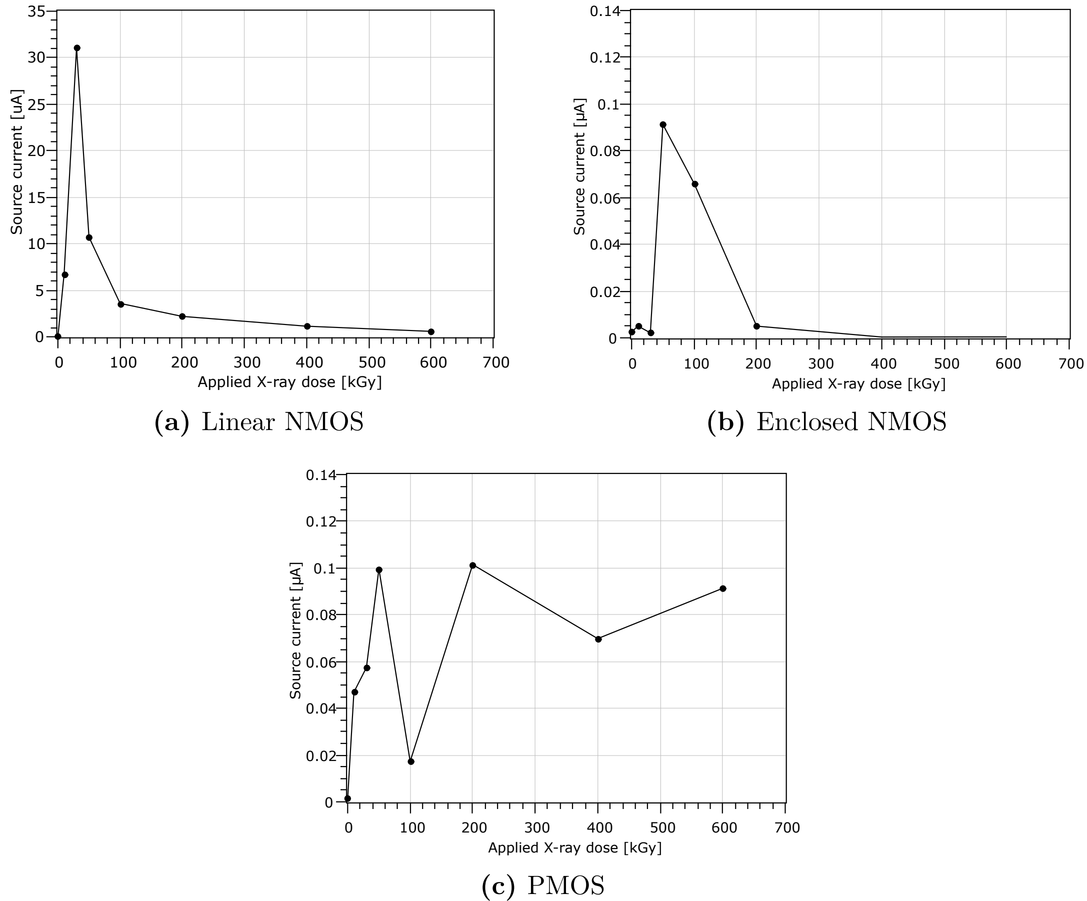
The input characteristics of the enclosed NMOS transistors remain unchanged after both X-ray and proton irradiation (Fig. 3.8b).

Proton irradiation leads to a slightly decreased slope for the linear NMOS transistor only. However after X-ray irradiation the curve is shifted significantly up. This means linear NMOS transistors are not able to block I_{DS} anymore for positive U_{GS} (Fig. 3.8a). This results in increased noise (shot noise) and power consumption.

Even after high radiation doses all types of transistors remain functional. However the linear NMOS transistors have some problems after X-ray irradiation. As the enclosed NMOS transistors are too big to replace all linear ones, future designs should use the enclosed version on all crucial positions like in first stage amplifiers or in places where a current has to be blocked properly.
Some circuits can be designed with both NMOS and PMOS transistors. In these circuits PMOS transistors might be the better choice. Linear NMOS transistors are still a good and also inevitable choice for digital circuits, in which a high density of transistors is needed and the problems caused by not properly shutting transistors is negligible.

The observation of a distinct y-offset after X-ray irradiation requests further investigation.

As mentioned above the irradiation was not applied at once but in several steps. Several measurements were taken between consecutive steps. The taking of the test transistors' input characteristics is one of those measurements performed after each irradiation step. From this data the y-offset of the current can be read out: the drain-source current I_{DS} for U_{GS} = 0 V (Fig. 3.9). Annealing between the irradiation steps was minimized by freezing the chip to less than −20 °C. The analysis of the obtained data shows that the y-offset of the linear transistor is not continually increasing with applied dose, but has a maximum around 30 kGy and decreases for higher doses (Fig. 3.9a).



(a) Linear NMOS

(b) Enclosed NMOS

(c) PMOS

Figure 3.9: The source-drain-current I_{DS} is shown as a function of the applied X-ray dose for a gate-voltage of U_{GS} = 0 V and a drain-source-voltage of U_{DS} = 3.3 V.

The increase of the leakage current may be caused by the generation of surface charges, which are above 30 kGy compensated by the generation of interface traps [25].

The enclosed transistor shows similar behavior (Fig. 3.9b) with the maximum located around 50 kGy, which however does not exceed 0.1 μA and is thereby more than 300 times smaller than the effect on the linear transistor.

The PMOS transistor does not have such maximum, the leakage current (taken at a gate voltage U_{GS} = 3 V) swings around 0.1 μA (Fig. 3.9c).

3.2.1 Annealing Effects on Transistors

The X-ray irradiation campaign has been conducted in about two weeks. To prevent the chips from annealing the chip was stored at temperatures below −20 °C whenever possible. However the requirements of a strip detector, for example in ATLAS, are not 600 kGy in two weeks but 600 kGy in about two years. This means that the structures have much

time to anneal. This annealing process was investigated after the irradiation campaign was finished. In order to obtain information about an extensive annealing process the chip has been stored at 20 °C for many weeks. The input characteristics of the transistors have been measured regularly. The results can be seen in Fig. 3.10. The y-offset decays over few days exponentially. The remaining y-offset is less than 0.05 μA. Right after the last irradiation step it was about 0.6 μA.

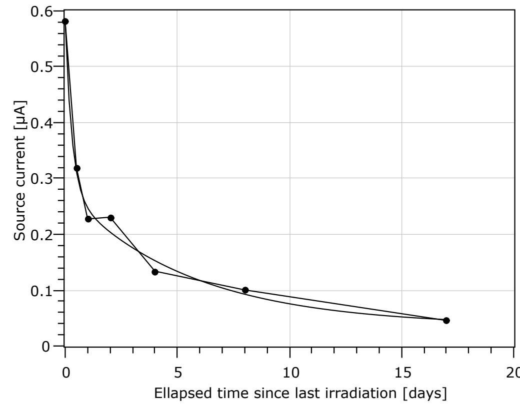


Figure 3.10: Y-offset of the linear NMOS transistor characteristic after some days of annealing (originally irradiated to 600 kGy). The offset sinks from about 0.6 μA right after the last irradiation step to less than 0.05 μA after 17 days annealing at room temperature (20 °C).

The behavior seems to be an exponential decay. Though a fit of the form

$$y(x) = y_0 + A \cdot \exp\left(-x/t\right) \tag{3.7}$$

is not successful. A fit of the form

$$y(x) = y_0 + A_1 \cdot \exp\left(-x/t_1\right) + A_2 \cdot \exp\left(-x/t_2\right) \tag{3.8}$$

however converges. This means that at least two effects with different lifetimes t_1 and t_2 are involved in the annealing process. Lifetime t_1 is about 5.5 days, t_2 is only 0.3 days. The weighting of both is about equal.

It has been shown that the y-offset after 600 kGy anneals over time. This result is not necessarily transferable to the peak region at about 30 to 50 kGy in Fig. 3.9a, as there a different effect seems dominant which probably does not anneal in the same way over time. That is why another chip was irradiated with X-rays to 40 kGy to find out if the annealing works in the same way in the peak region, as it does after 600 kGy.

Fig. 3.11 shows that annealing after 40 kGy is possible, too. However the decrease of the y-offset is slower after 40 kGy than after 600 kGy. After 9 days it is about 32% of the maximum value, in case of 600 kGy it was about 15%. Further it turned out that the dose, which leads to maximum offset, is less than 40 kGy, because the offset at 30 kGy is higher than the one after 40 kGy.

3.3 Calibration

The charge sensitive amplifier generates a voltage output, which is proportional to the number of electrons on the pixel capacitor. This output voltage of each pixel can be monitored by an attached oscilloscope. For multiple purposes the HVStripV1 chip has the option to inject a certain charge into the pixel capacity. The amount of electrons injected is well defined by the externally set injection voltage. This gadget makes it possible to test

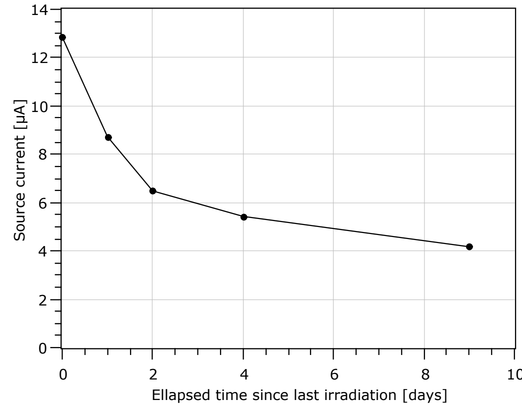


Figure 3.11: Annealing behavior of the y-offset of the linear NMOS transistor, irradiated to 40 kGy.

the signal path from the very beginning to any viable output without the need of actual particles. This is beneficial for many measurements, e.g. timing evaluations or output calibration.

The amplifier's response to an 1.0 V injection is shown in Fig. 3.12. A short rise-time ($\ll 1\ \mu$s) is followed by a linear decrease with a duration of some μs. Both rise- and fall-time are variable and can be influenced by certain DAC-settings.

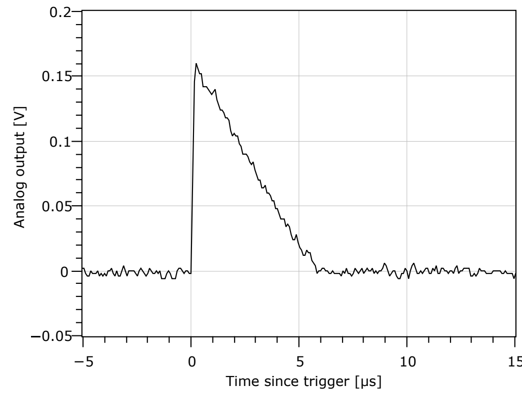


Figure 3.12: The amplifier's response to an 1.0 V injection pulse.

The signals generated by an injection pulse are a linear function of the injection voltage (Fig. 3.13). Injections with a set injection voltage generate electrons which are amplified by the CSA. The output is monitored by an oscilloscope.

$$U_{Inj} \propto U_{Out} \tag{3.9}$$

Only for injections above 2.5 V the output is not proportional to the injection voltage anymore. We are especially interested in small signals. Injection voltages above 2.0 V are not needed, so the nonlinearity will not cause any problems.

A calibration has to be performed, because it is not exactly known yet, what charge on the pixel sensor (caused by particle or injection) leads to what output voltage. It depends on various factors how many electron-hole pairs are generated by a charged particle passing through the detector, so charged particles are not suitable for calibration.

Photons deposit all energy in one spot, which means a photon with a certain energy generates a quite precise amount of charges in silicon. The transition of an electron from the L-shell to the K-shell of an atom emits an X-ray photon, with energy depending on the

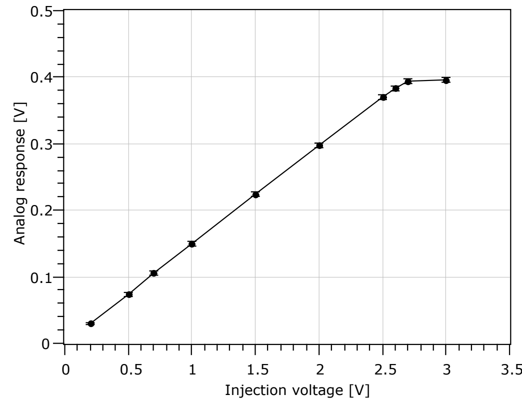


Figure 3.13: The signals generated by injections are a linear function of the injection voltage.

element of the emitting atom. This means also that a spot in the K-shell has to be vacant in the first place. We obtain such excited atoms by illuminating a target with high energy X-rays from an X-ray tube.

Another source of photons with precise energy dispersion are radioactive decays. A decay which emits only a photon (+ a neutrino) is the decay of ^{55}Fe. The iron isotope ^{55}Fe decays to ^{55}Mn by K-electron capture.

$$^{55}_{26}\mathrm{Fe} + e^{-} \longrightarrow ^{55}_{25}\mathrm{Mn} + \nu_e \tag{3.10}$$

This decay leaves a vacancy in the K-shell of the newly created ^{55}Mn which is quickly filled by an electron of an outer shell. The most probable origin of this electron is the L-shell. The transition of an electron from the L-shell to the K-shell emits an X-ray photon with about 5900 eV [26].

A ^{55}Fe γ-source placed right above the pixel matrix creates hits in the pixel matrix. As all energy of a hit is deposited in one spot, charge sharing between adjacent pixels is very unlikely (cf. Fig 2.10). Each hit of a ^{55}Fe X-ray generates 1639 electrons in silicon.

The analog response to a X-ray photon has the same shape as the analog response to an injection pulse (cf. Fig. 3.12). The height of the triangle-shaped signal is determined by the X-ray's energy. In order to measure an X-ray spectrum, the analog output is connected to an oscilloscope. The oscilloscope accepts a signal as a hit, if the signal crosses a certain threshold level. The threshold is set right above the baseline noise. For every hit the signal's height is taken to fill a histogram. Such histogram can be seen in Fig. 3.14a. Theoretically the peak should be very sharp (however not δ-distribution like), but is widened by noise. Fitting a normal-distribution (Gaussian-distribution), minimizes statistical mistakes and the most probable value (MPV) is found (Fig. 3.14b). That means also that the width of the Gaussian-distribution is a measure for the noise in the system, usually given as the standard deviation σ.

The analog response of every pixel is read out one by one individually. The difference in pulse height is shown in Fig. 3.15, even though all pixels have been illuminated with X-rays of the same energy. The difference in pulse height between pixels with linear and enclosed feedback transistor is clearly visible. Linear pixels (column 0 to 7) show an output signal about 20% bigger than enclosed pixels. But there are also significant differences between the pixels of each group. To deal with such production induced differences a tuning function in the analog-digital-converter (ADC) is implemented (see chapter 3.6.2).

With this information a first calibration can be conducted. Every pixel has a different response to the ^{55}Fe signal, as seen in Fig. 3.15, even though in every hit the same charge

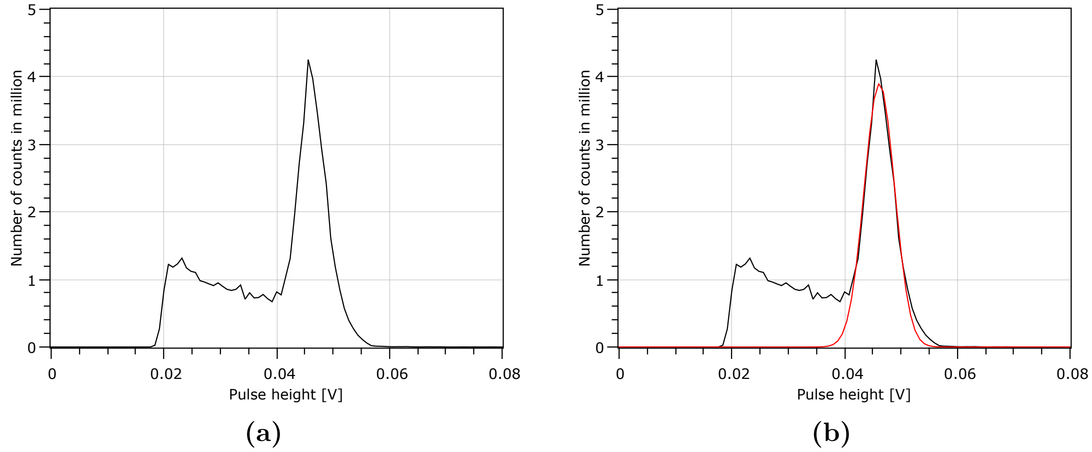


Figure 3.14: The histogram of a ^{55}Fe signal (a). Smaller pulse heights (left) are cut off. To find the most probable value a Gaussian-distribution has been fitted in (b).

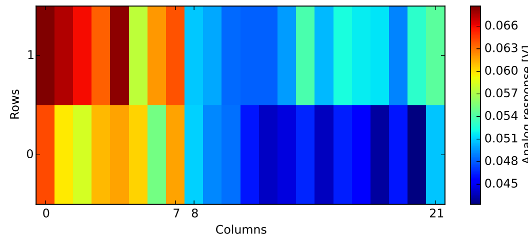


Figure 3.15: Analog response of all pixels to ^{55}Fe. The amplifiers of pixels in columns 0 to 7 have linear NMOS feedback transistors, all others use the enclosed version.

is generated. This means that every pixel needs its own calibration.
Pixel 0 shows an analog response of 64 mV to the ^{55}Fe signal (1639 e). A linear relation between number of electrons N_e and output voltage U_{Out} is assumed. Further an injection setting of 0 V is expected to result in a 0 V output signal.

$$U_{Out} \propto N_e \tag{3.11}$$

$$U_{Out}\,(0e) = 0\ mV \tag{3.12}$$

$$\Rightarrow U_{Out}^{Pix0}\,(N_e) = N_e \cdot 39\ \frac{\mu V}{e} \tag{3.13}$$

Same calculation and assumptions can be made for other pixels (Tab. 3.1). While Eq. (3.11) should be a good assumption for a wide signal range, Eq. (3.12) might be not.

So far only one data-point was used for calibration. More data-points make the calibration independent of the assumptions above. Characteristic X-rays of several elements deliver a set of data-points for a precise calibration. The used X-rays are emitted by targets illuminated by an X-ray tube. The used targets with their dominant X-ray energies are shown in Tab. 3.2.

Every target results in a spectrum similar to Fig. 3.14a, each with a different peak position, which refers to a different amount of electrons. Spectra of all seven used targets are combined in one plot in Fig. 3.16.

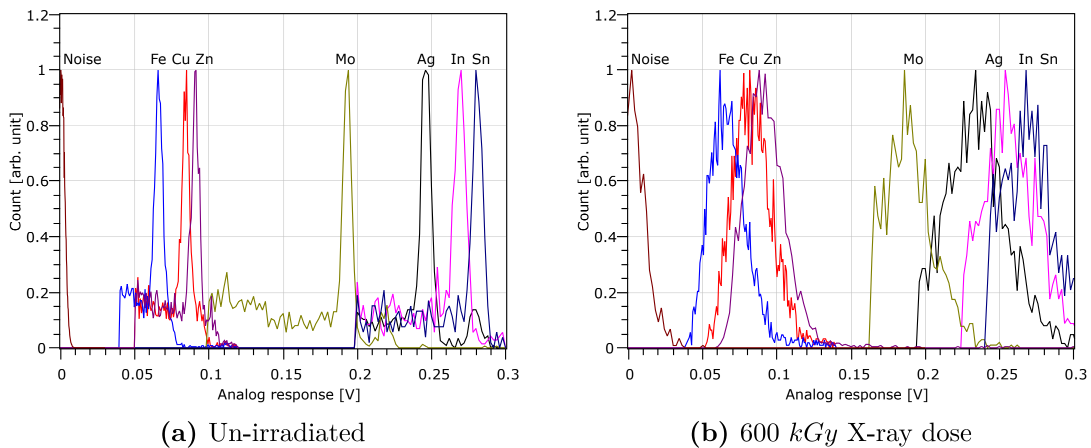
These peak positions are set in relation to the amount of electron-hole pairs generated by incoming X-rays (cf. Tab. 3.2) for calibration. This is shown in Fig. 3.17. The ^{55}Fe calibration showed already that every pixel needs its own calibration. The difference in gain is especially big between pixels with linear and enclosed transistors.

Pixel	$\frac{\mu V}{e}$	**Pixel**	$\frac{\mu V}{e}$	**Pixel**	$\frac{\mu V}{e}$	**Pixel**	$\frac{\mu V}{e}$
0	39	8	31	22	42	30	31
1	36	9	30	23	41	31	30
2	36	10	30	24	40	32	29
3	37	11	28	25	39	33	29
4	38	12	27	26	42	34	29
5	37	13	27	27	35	35	30
6	34	14	28	28	38	36	33
7	38	15	27	29	39	37	31
		16	28			38	32
		17	28			39	32
		18	26			40	31
		19	28			41	30
		20	26			42	32
		21	31			43	33

Table 3.1: Gain of all pixels on HVStripV1 chip 1. Column 1 and 3 have linear, 2 and 4 have enclosed feedback transistors.

Target element	**X-ray energy [eV]**	**Electron-hole pairs**
Fe	6403	1778
Cu	8048	2235
Zn	8639	2399
Mo	17479	4855
Ag	22163	6155
In	24210	6724
Sn	25271	7019

Table 3.2: Used targets for X-ray-calibration. In silicon an X-ray generates one electron-hole-pair per 3.6 eV incoming energy.

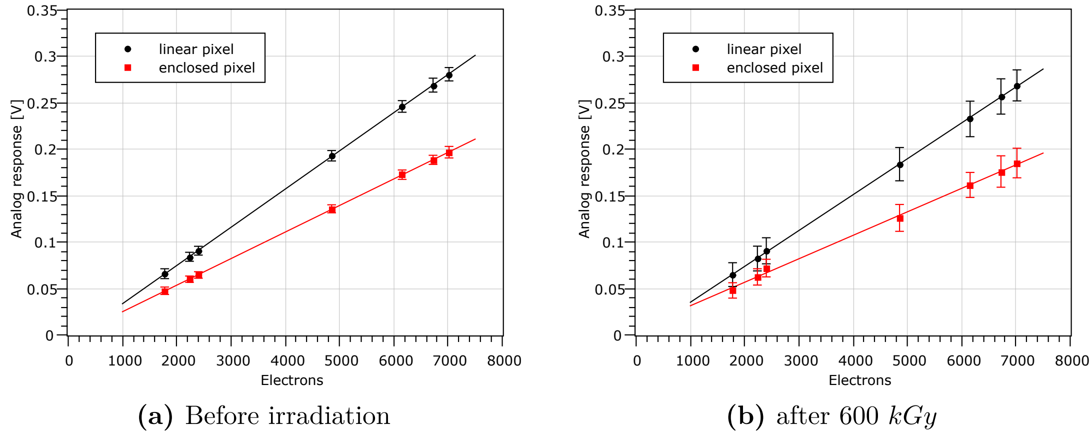


(a) Un-irradiated **(b)** 600 kGy X-ray dose

Figure 3.16: Spectra of seven elements combined. The target element used for a specific spectrum is written above the respective peak. In addition the baseline noise is shown. Each data set is standardized so all peaks have the same height. After irradiation the spectra have been shifted towards lower energies and the peaks are widened.

A line fit through all points of one pixel is conducted to prove linearity. As all data points are perfectly on the fit line, linearity of gain in the relevant range is actually given. Assumption (3.12) however turns out to be not correct. The linear fits do not intersect the y-axis at $y = 0$. This means that for a reliable calibration more than one measure point is needed. The reason for this y-offset can not be found necessarily on the chip. It might be also an effect of the long signal path from the experimental setup to the oscilloscope or of the oscilloscope itself.

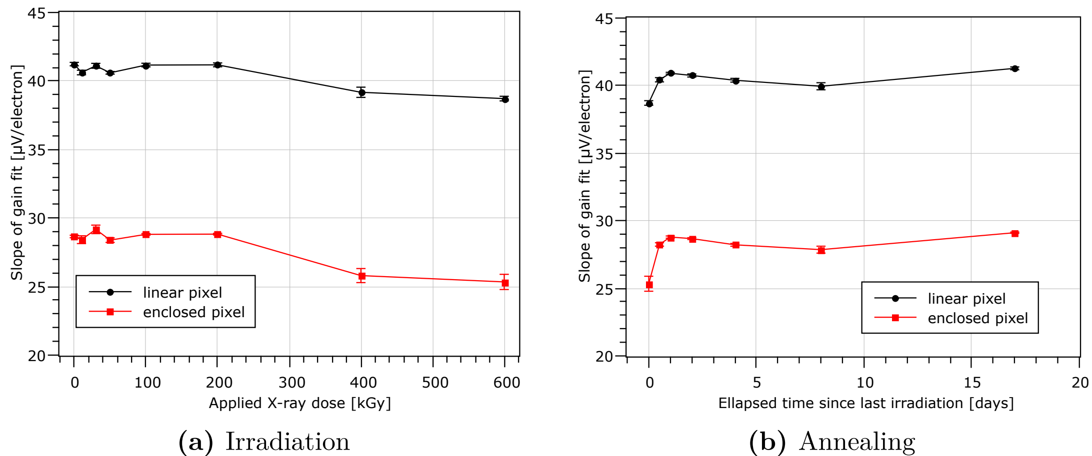
Once the chip has been irradiated by direct X-ray illumination to 600 kGy, the seven spectra are taken again (Fig. 3.17b). After irradiation the gain is slightly reduced. The increased uncertainty of each data point is caused by widened peaks of each spectrum. This means that there is more noise in the system after irradiation.



(a) Before irradiation **(b)** after 600 kGy

Figure 3.17: Pixel calibration using characteristic X-rays from seven different targets.

The calibration, including the line fitting, was conducted after every irradiation step. The resulting slopes are shown in Fig. 3.18a. The slope remains nearly unchanged after the first steps up to 200 kGy. Between 200 and 600 kGy the slope is slightly reduced. These observations are the same for both linear and enclosed pixels.



(a) Irradiation **(b)** Annealing

Figure 3.18: The slope of the energy calibration while irradiating and annealing.

After the irradiation campaign has been completed, the slope is measured while annealing (Fig. 3.18b). Already after one day of annealing the slope is close to its value before irradiation.

The combined pieces of information about injection behavior (Fig. 3.13) and X-ray calibration (Fig. 3.17) determine the amount of electrons created by a certain injection

voltage. The X-ray calibration brings:

$$U_{Out} = A_1 \cdot N_e + B_1 \tag{3.14}$$

Where U_{Out} is the analog response and N_e the number of of electrons generated. The injection calibration has a similar form:

$$U_{Out} = A_2 \cdot U_{Inj} + B_2 \tag{3.15}$$

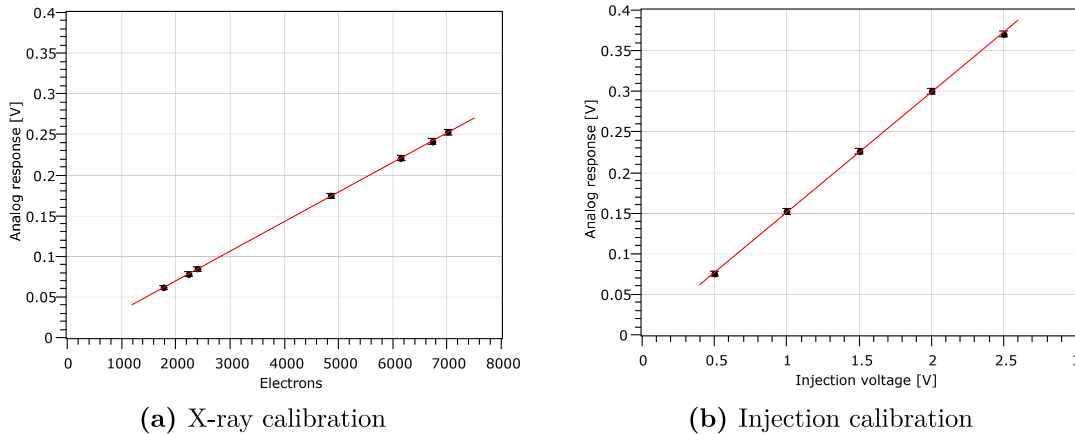
With U_{Inj} being the injection voltage. Together we obtain:

$$N_e = \frac{A_2 \cdot U_{Inj} + B_2 - B_1}{A_1} \tag{3.16}$$

$$N_e = \frac{A_2}{A_1} \cdot U_{Inj} + \frac{B_2 - B_1}{A_1} \tag{3.17}$$

The fit parameters of a linear pixel from Fig. 3.19 are used to calculated the conversion formula:

$$N_e = (4061 \pm 58)\,\frac{e}{V} \cdot U_{\text{Inj}} + (166 \pm 114)\,e \tag{3.18}$$



(a) X-ray calibration **(b)** Injection calibration

Figure 3.19: Calibrations needed to determine an equation for the number of electrons generated by injection pulses. Here by the example of a linear pixel.

Data of an enclosed pixel from Fig. 3.20 calculates to:

$$N_e = (4178 \pm 57)\,\frac{e}{V} \cdot U_{\text{Inj}} + (51 \pm 120)\,e \tag{3.19}$$

Even though pixels of different type were used, the results are nearly the same. This was expected, because the injection mechanism is the same for all pixels.

3.3.1 Calibration Summary

It has been shown that a charge is correctly amplified and the output voltage is proportional to it. The generation of charges has been tested in two ways:
X-ray signals of different energies cause an output voltage proportional to those energies.
Direct injections create a precise signal proportional to the injection voltage. The proportionality factor between U_{Inj} and N_e has been calculated for some pixels and turned out to be more or less universal.
Signal shapes have been observed for several pixels. The analog response to the same charge is quite different for different pixels, which makes tuning necessary.
High irradiation doses have a minor effect on the gain, which vanishes after a short annealing time.

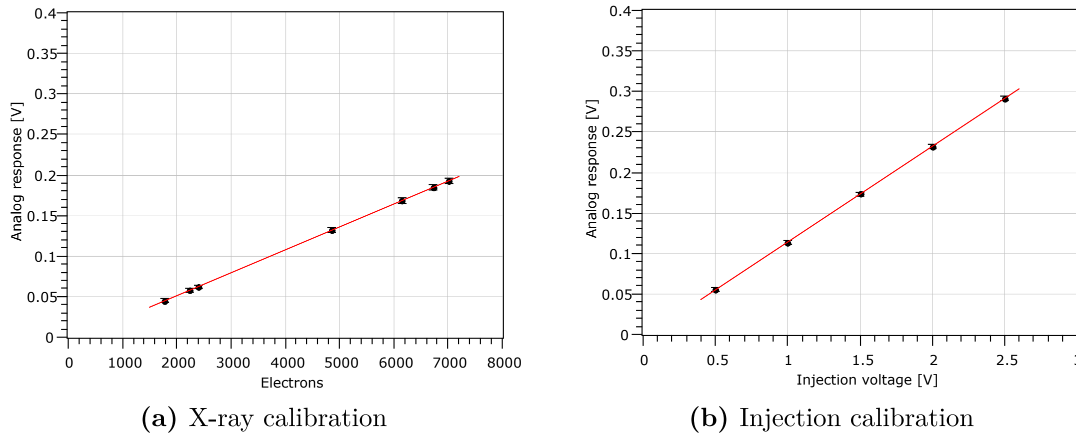


Figure 3.20: Calibrations needed to determine an equation for the number of electrons generated by injection pulses. Here by the example of an enclosed pixel.

3.4 Charged Particle Detection

The usual purpose of semiconductor sensors is to track the path of charged particles. When a charged particle passes through the active material electron-hole pairs are generated, which can be detected. So far the source of the detected electrons was not a charged particle, but X-rays or analog injections. As the generation of charges by charged particles differs from others, this has to be investigated separately.

A handy source of charged particles is ^{90}Sr. It undergoes a β^- decay:

$$^{90}_{38}\mathrm{Sr} \longrightarrow ^{90}_{39}\mathrm{Y} + e^- + \bar{\nu}_e \tag{3.20}$$

Yttrium decays further to ^{90}Zr, which is stable and remains in the source. Neutrinos do not interact with the sensor material and therefore do not disturb the measurement. The generated free electron is the desired charged particle. Some of these electrons pass through the active area of the detector chip, but not every electron leaves the same amount of electron-hole pairs behind. The amount depends on several factors, like trajectory, particle energy and thickness of the depletion zone. The probability for a certain amount of electron-hole pairs generated is described by the Landau-distribution:

$$p(x) = \frac{1}{2\pi i} \int_{c-i\infty}^{c+i\infty} e^{s \ln s + xs} ds \tag{3.21}$$

The expected output signal is a convolution of this Landau- and a Gaussian-distribution, the Landau-Gaussian-distribution, because all signals get a Gauss-like uncertainty by passing through the detector electronics. (Cf. Fig. 3.14 which is a convolution of a δ-distribution and a Gaussian-distribution.)

While a ^{90}Sr source is placed on the chip, the analog response of a single pixel is monitored and histogrammed by an oscilloscope (Fig. 3.21). The noise peak is very close to the Strontium peak, because the measurement setup makes it impossible to trigger by scintillator. That is why it is not possible to exclude low energy β-rays from direct hits by ^{90}Sr-β-rays from the data. These low energy β signals appear as additional noise peak.

A Landau-Gaussian-function has to be fit to the obtained data to find the most probable value (MPV). As before the MPV [V] can be converted to electrons.

As mentioned above the charged particles generate electron-hole pairs along their path through the active area of the detector chip. The active area is the depleted zone of each

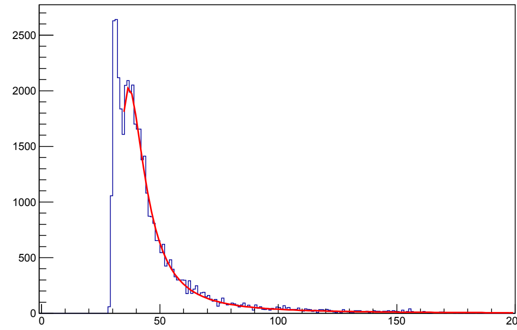


Figure 3.21: A histogram filled with data by a ^{90}Sr source on the chip. The count as a function of output voltage in arbitrary units (channels). A convoluted Landau-Gaussian-distribution in red has been fitted to the relevant data. The MPV is 77 mV ≙ 2060 e. More to the left the beginning of the noise peak is visible.

pixel-diode. The thickness of the depletion-zone w is given by

$$w\left(U_A\right) = \sqrt{\frac{2\varepsilon\varepsilon_0}{e}\frac{n_A + n_D}{n_A n_D}\left(U_D + U_A\right)} \tag{3.22}$$

Where n_A/n_D are the concentrations of acceptors/donators, $\varepsilon/\varepsilon_0$ are the relative/vacuum permittivity and U_D/U_A are the diffusion/applied voltage.

The easiest way to vary the thickness of the depletion zone is to vary the bias voltage, because

$$U_A = U_{DD} - U_{Bias} \tag{3.23}$$

$$U_A = 3.3\ V - U_{Bias} \tag{3.24}$$

U_{DD} is the supply voltage of the chip on one side of the pixel-diode, whereas U_{Bias} is the extra applied (negative) voltage on the substrate to increase the depletion zone width.

The analog response to ^{90}Sr illumination of a linear and enclosed pixel has been measured for different bias voltages. Fig. 3.22a shows the obtained data. As seen before the signal of linear pixels is higher than the one of enclosed pixels. The output voltage of both pixels is translated into electrons generated in the pixel-diode using an X-ray calibration. As the pixel of all types have the same diode layout, the calculations show a similar amount of electrons for both types.

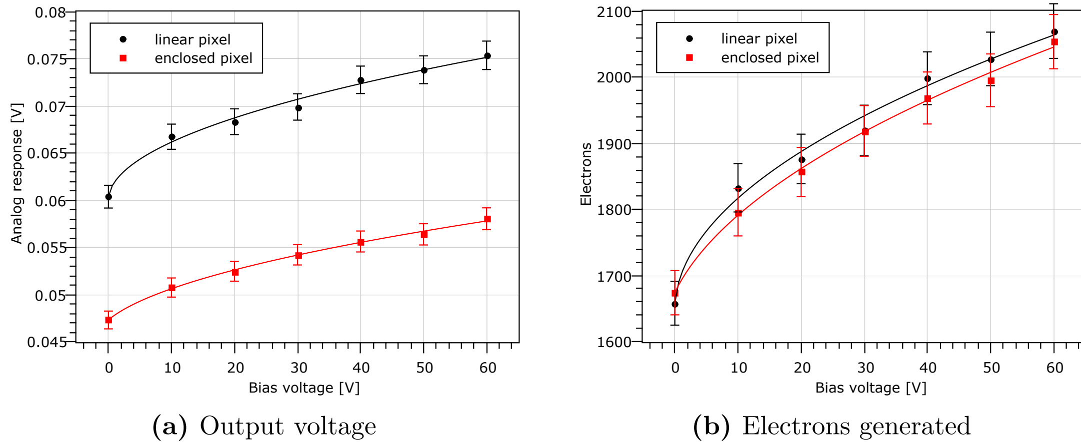
The number of electrons collected in the pixel diode is proportional to the thickness of the depletion zone. So Eq. (3.22) can be used to form a fit-function:

$$f\left(x\right) \propto A \cdot \sqrt{x - x_0} \tag{3.25}$$

This function can be adapted to all points in Fig. 3.22. The obtained curves fit to the points which fortifies the made assumptions.

3.4.1 Irradiation

It has been shown in chapter 3.3 that X-ray irradiation reduces the analog response (output voltage of the amplifier) to γ- and injection-signals. The same observation is made for β-signals. However the count of collected electrons remains the same. Both before and after being irradiated with the X-ray tube, about 2000 to 2100 electrons are collected, irrespective of the pixel type. This is an expectable result, because the used X-ray radiation has not enough energy to damage the crystal lattice. The X-rays generate only electron-hole



(a) Output voltage

(b) Electrons generated

Figure 3.22: The β-rays from a ^{90}Sr-source cause output voltages in the pixels. The output voltage in a linear pixel is higher than in an enclosed pixel (a). Using X-ray calibration the number of electron-hole pairs generated in the pixel diode is obtained (b).

pairs which either recombine or diffuse out of the active area. Either way the pixel-diode remains unaffected.

The situation is different when the chip has been exposed to proton radiation. After a chip has been irradiated to $2 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$, the ^{90}Sr signal has been measured again. Using a ^{55}Fe output calibration the amount of electrons collected can be determined to 3500 - 3600. This is a significant increase compared to the un-irradiated case. This means that proton irradiation increases the thickness of the active area. The 23 MeV protons used in this irradiation campaign carry enough energy to cause damage to the silicon lattice. The newly created vacancies and interstitial atoms serve as electron acceptors, respectively donors. So the effective doping is decreasing which causes a thicker depletion zone (cf. Eq. (3.22)).

3.5 Noise

So far only various signals at different conditions have been discussed. But low noises are as important as strong signals. The common used signal-to-noise ratio (SNR) is a measure for the quality of an output. A high SNR indicates a good, easy to read and process signal.

$$\mathrm{SNR} = \frac{\text{Signal } S}{\text{Noise } N} \tag{3.26}$$

Here S is the average pulse hight of signals; noise N is the standard deviation σ of the signal or the baseline.

For a first overview the noise of all pixels was extracted from the ^{55}Fe measurement (Fig. 3.14). The value of the noise as standard deviation σ is included in the Gaussian-fit. Higher noise means wider peak. The noise for each pixel is shown color-coded in Fig. 3.23. The signals of the linear pixels have been bigger compared to the enclosed ones (Fig. 3.15). The noise values show the same behavior: Linear pixels have a higher noise than the enclosed ones. However the noise is also not homogeneous within one type.

3.5.1 Bias Voltage

Low noise is always a desirable property for electronic systems. It turned out that a simple way to lower the noise is to apply a higher bias voltage. The noise at the amplifier's output, while 60 V bias voltage is applied, is about 1/3 lower compared to the noise, while bias voltage is set to 0 V (Fig. 3.24).

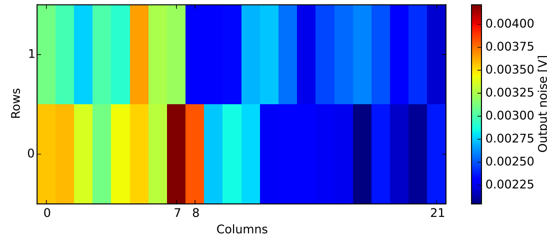


Figure 3.23: A map of noise for all pixels. Linear pixels (column 0 to 7) show a higher noise than enclosed pixels.

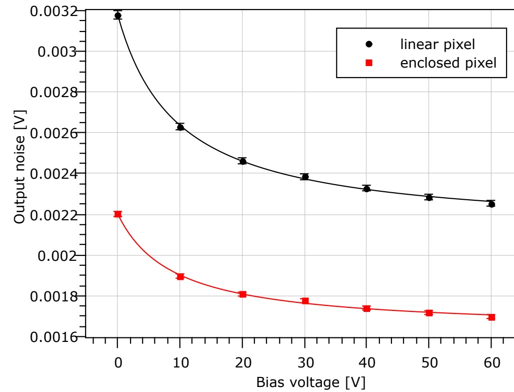


Figure 3.24: The noise on the analog output as a function of the bias voltage for a linear pixels (black) and an enclosed pixel (red).

Fig. 3.25 shows the SNR as a fucntion of the bias voltage. It has been calculated using Eq. (3.26), with data from ^{90}Sr-signal and baseline noise of the same pixel (cf. Fig. 3.22 and Fig. 3.24). The SNR for both pixel types rises from about 22 (U_{Bias} = 0 V) to over 39 (U_{Bias} = 60 V). Although the difference between the two pixel types is not big, the SNR of linear pixels is in advantage for higher applied voltages.

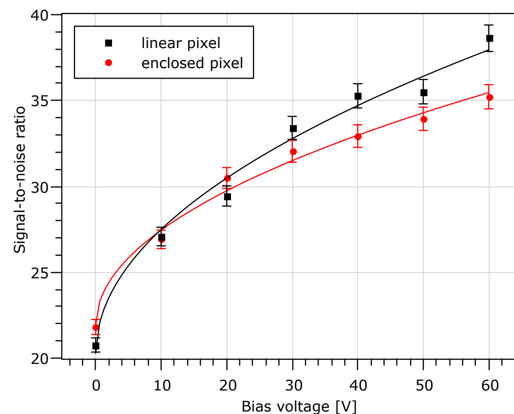
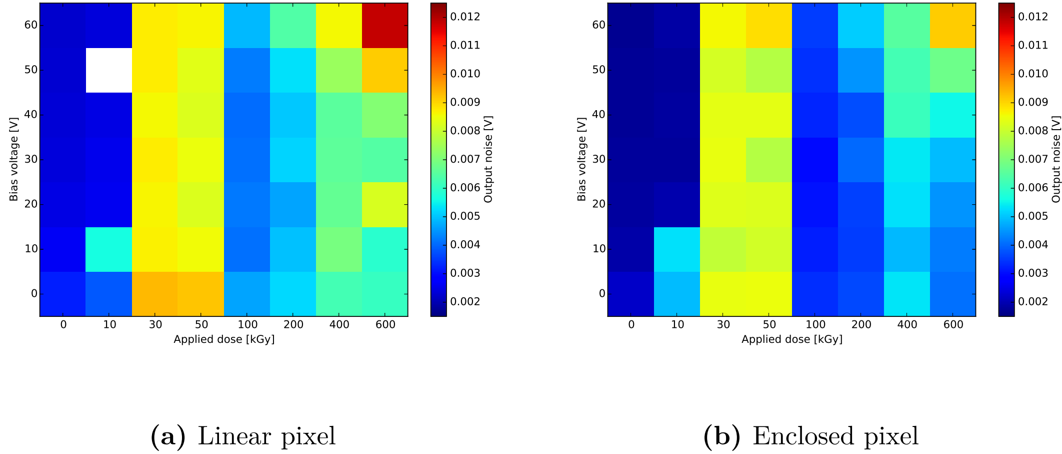


Figure 3.25: Signal-to-noise ratio of a ^{90}Sr-signal. The chip has not been irradiated yet.

3.5.2 Noise after X-irradiation

Before being irradiated the noise at common bias voltages was about 2.3 mV for linear pixels, respectively 1.7 mV for enclosed pixels. As mentioned above a chip has been irradiated with X-rays in several steps to a total dose of 600 kGy. The bias-dependency of the noise has been measured after each step (Fig. E.9 and Fig. 3.26).



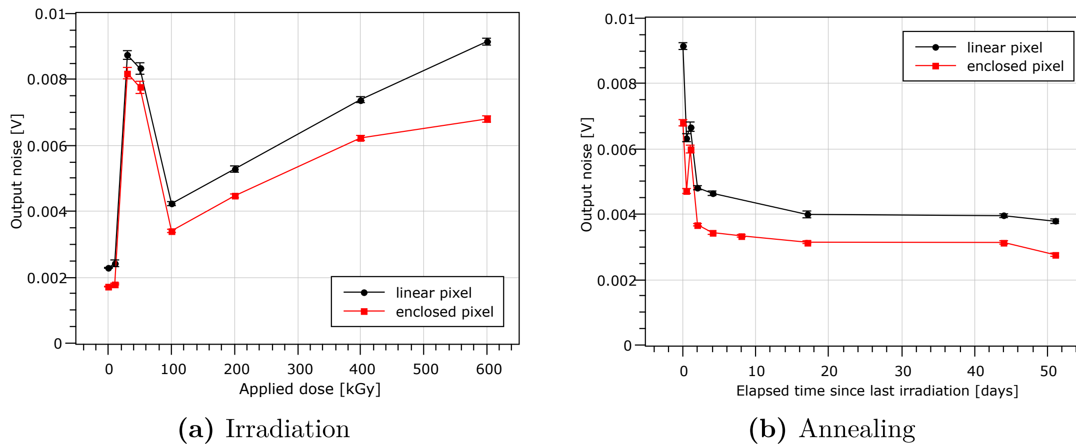
(a) Linear pixel

(b) Enclosed pixel

Figure 3.26: Color map showing the noise on the amplifier's output line for several bias voltages and doses.

Before irradiation the shape of the data is $^1/_x$-like (Fig. E.9 a). This shape remains for low doses (Fig. E.9 b), however the overall noise is slightly increased after 10 kGy. A first maximum of noise is reached after 30 to 50 kGy (Fig. E.9 c and d). The noise is 3-5 times as high as before irradiation. Also the shape changed from $^1/_x$ to a rather U-like shape. The increase of noise for high bias voltages is caused by an increase in leakage current. Higher doses up to 200 kGy lead to a reduced over all noise (Fig. E.9 e and f). Compared to the un-irradiated state the noise is only about doubled. The shape is rather independent of the bias voltage with a tendency to U-like shape. From this local minimum the noise rises again (Fig. E.9 g and h). The shape shows an exponential behavior.

It has been shown that X-ray irradiation increases the overall noise, for high bias voltages in particular. The arising of a local noise maximum around 40 kGy seems correlated with the y-offset of transistors while irradiation (cf. Fig. 3.9). The high noise after a full dose is crucial, as for the usage of this chip a high bias voltage is necessary. Fig. 3.27a shows the noise with an applied bias voltage of U_{Bias} = 50 V. The local maximum around 30-50 kGy is clearly visible. Higher doses cause a linear (or probably square root) increase of noise till the end of the irradiation campaign.



(a) Irradiation

(b) Annealing

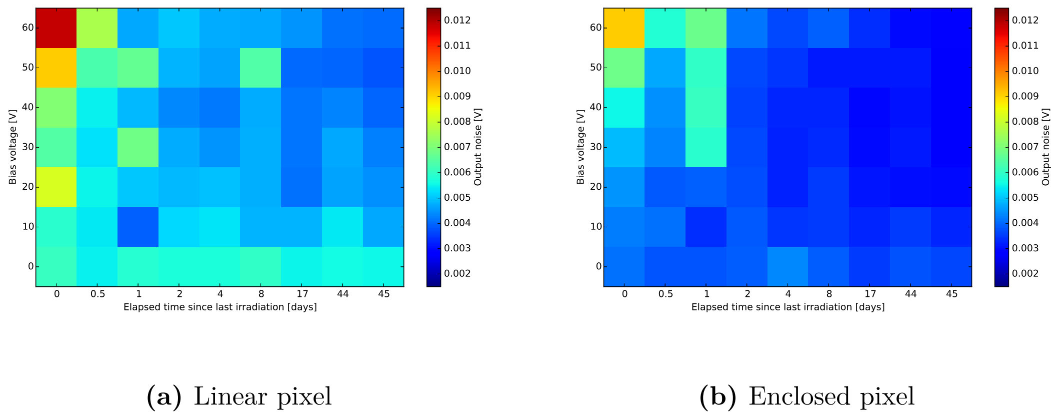
Figure 3.27: The noise on the amplifier's output line for a bias voltage U_{Bias} = 50 V

3.5.3 Noise after Annealing

It has been shown before that annealing might play an interesting role and has to be taken into account (Fig. 3.10). An annealing campaign has been started after the last irradiation step (total dose of 600 kGy). The noise is repeatedly measured after certain time steps. The chip is kept at 20°C in between the measurements.

Only two days of annealing are enough for the noise of the enclosed pixels to drop to less than 4 mV (Fig. 3.27b) for a bias voltage of 50 V. This is about twice the noise as before the irradiation. After 17 days the noise of both types have reached a plateau, which is less then twice the pre-irradiation value. After 44 days annealing with higher temperature has been tested, as the noise has not significantly dropped anymore. A time of 30 minutes at 60°C lead to an additional reduction in noise.

Bias dependent measurements show the reverse behavior as described in chapter 3.5.2, just without a local maximum (Fig. E.10). The color-coded diagram in Fig. 3.28 shows the effect of annealing on the noise. The color-coding is the same in all four diagrams in Fig. 3.26 and Fig. 3.28. This allows easy and direct comparison of the colors and shapes: Annealing of linear pixels appears to be slower than annealing of enclosed ones. In the end of the annealing campaign, the noise of both pixel types is reduced by high bias voltages, like it has been before irradiation.



(a) Linear pixel

(b) Enclosed pixel

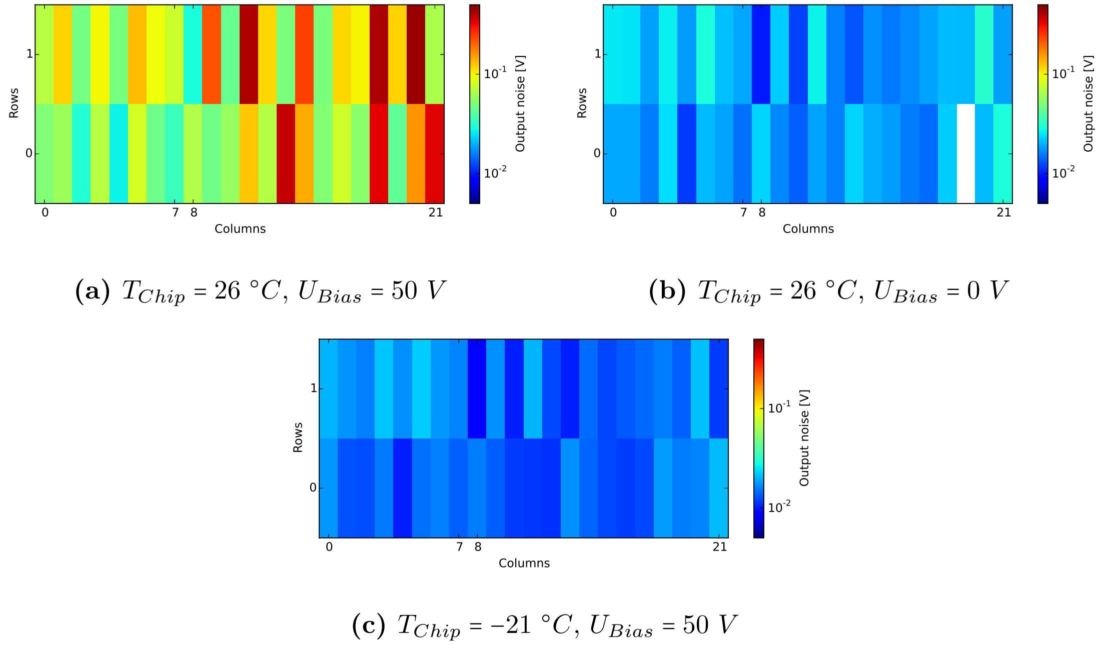
Figure 3.28: Color map showing the noise on the amplifier's output line for several bias voltages and annealing times.

3.5.4 Noise after Proton Irradiation

One chip has been irradiated to a total of $2 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$ using 23 MeV cyclotron protons. For radiation protection reasons only un-bonded chips can be irradiated. But this means also that no pre-irradiation measurements can be performed on those chips. That is why the comparison of pre- and post- irradiation measurements are always performed on different chips.

A total dose of $2 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$ has been applied. This is about twice the dose such a detector chip has to be able to handle in its lifetime. Fig. 3.29a shows the noise on the analog output line of all pixels for an applied bias voltage of 50 V. Some pixels show extreme noise. It is impossible to see signals with such background noise, assuming that the chip still works at all.

A lower bias voltage reduces the noise by far (Fig. 3.29b). This is a hint where the main source of noise is originated. Checking the leakage current confirms this assumption (Fig.



(a) $T_{Chip} = 26\ °C$, $U_{Bias} = 50\ V$

(b) $T_{Chip} = 26\ °C$, $U_{Bias} = 0\ V$

(c) $T_{Chip} = -21\ °C$, $U_{Bias} = 50\ V$

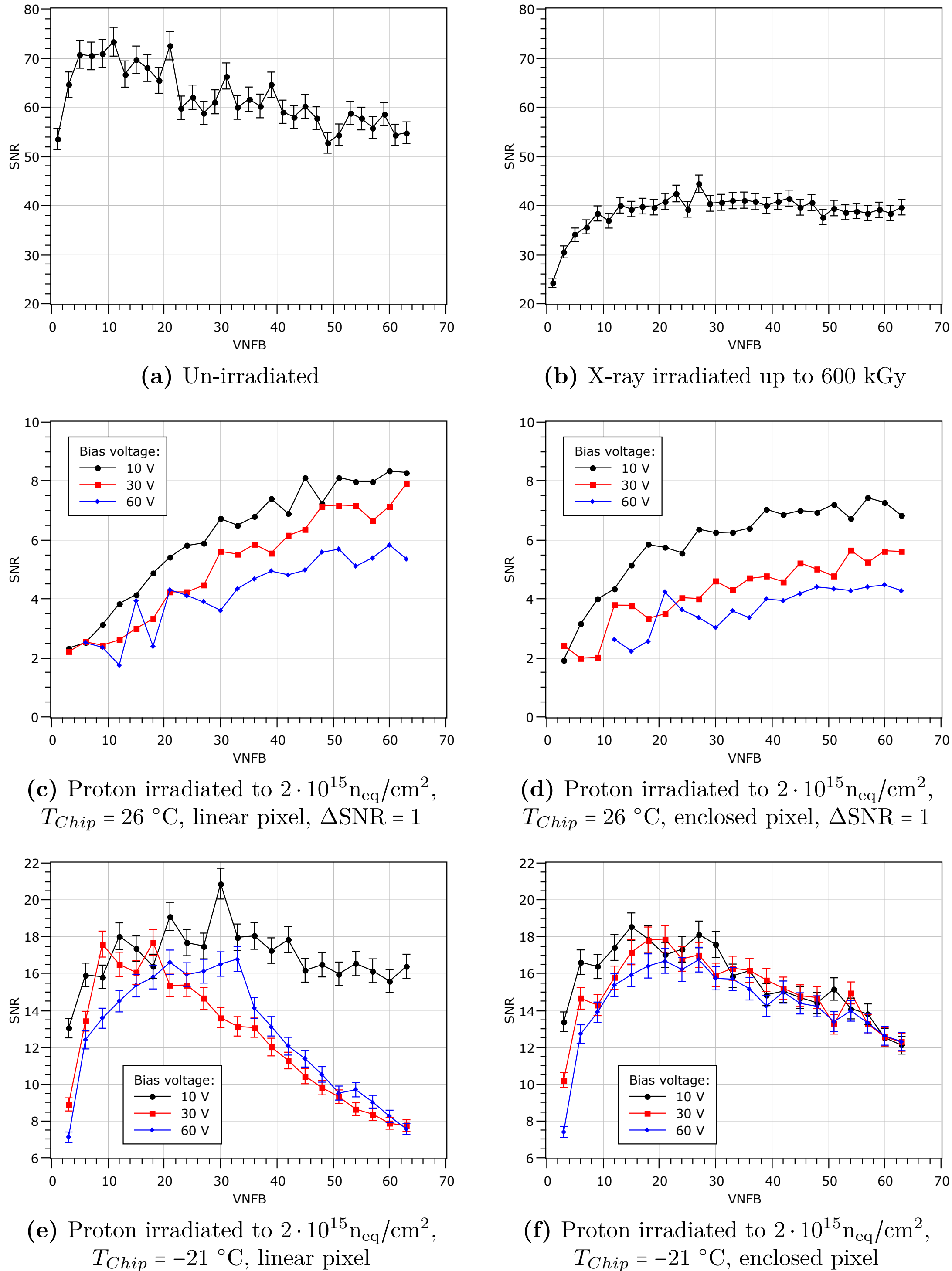
Figure 3.29: The noise of all pixels color coded under several conditions. The chip has been irradiated to $2 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$. Note the logarithmic scale!

3.6): An un-irradiated chip shows a leakage current of less than 20 nA. After irradiation with X-rays to 600 kGy the leakage current was increased to about 130 nA, while proton irradiation ($2 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$) causes bias currents up to 60000 nA at room temperature. The shot noise caused by this bias leakage current is considered to be the main source of noise here.

For further testing the leakage current, and thereby the noise, has to be reduced. The bias current is caused by the effect of charge generation, as described in chapter 3.1.1. Eq. (3.4) shows that the current is highly dependent on the temperature. This is confirmed by Fig. 3.29c, which shows the noise of the proton irradiated chip at a reduced temperature. Also another improvement has been made in this measurement: It has turned out that the setting of the feedback transistors has to be adjusted for certain doses in order to obtain the best possible signal-to-noise ratio.

The feedback transistors are controlled by a 6-bit DAC called VNFB. To find the best value of VNFB, a charge in the pixel is generated with a fix injection voltage for several values of VNFB. From the obtained histograms the SNR for each setting can be calculated. The result of such VNFB scan is shown in Fig. 3.30.

An un-irradiated chip shows best SNR of over 70 for VNFB = 5 – 10 (Fig. 3.30a). After being illuminated by X-rays to a total dose of 600 kGy (and 25 days of annealing), the SNR is still over 40, if VNFB has been set to over 15 (Fig. 3.30b). As mentioned before the analog output shows a strongly increased noise after being irradiated with protons up to $2 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$. Therefore the SNR is not even reaching 10, even at the maximum value for VNFB of 63 (Fig. 3.30c). For reasonable bias voltages the SNR is even smaller. The SNR values of enclosed pixels are slightly smaller than those of linear pixels. Cooling reduces the noise and at the same time increases the SNR. With an applied bias voltage of $U_{Bias} = 60$ V, SNR reaches about 17 for both linear (Fig. 3.30e) and enclosed pixels (Fig. 3.30f). These SNR values are obtained for VNFB = 20.



(a) Un-irradiated

(b) X-ray irradiated up to 600 kGy

(c) Proton irradiated to $2 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$, T_{Chip} = 26 °C, linear pixel, ΔSNR = 1

(d) Proton irradiated to $2 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$, T_{Chip} = 26 °C, enclosed pixel, ΔSNR = 1

(e) Proton irradiated to $2 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$, T_{Chip} = −21 °C, linear pixel

(f) Proton irradiated to $2 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$, T_{Chip} = −21 °C, enclosed pixel

Figure 3.30: Signal-to-noise ratio of 1 V injections into the pixel diode for varying settings of VNFB. Each figure shows SNR as a function of VNFB for different doses, bias voltages and temperatures.

3.5.5 Noise Summary

The last results have shown that the noise is highly dependent on various factors. Before irradiation noise is no problem for the signal at the analog output.

Illumination with X-rays to high doses causes increased noise on the amplifiers output. Furthermore a higher bias voltage does not decrease the noise anymore, but increases it. This is problematic for the detection of charged particles passing through the detector, because for a high signal a high bias voltage is needed. However even short times of annealing result in a sufficient reduction of noise.

Irradiation with protons causes bulk damage in the pixel diode, which leads to an increased bias current. The resulting shot noise is strong enough to make particle detection impossible. Cooling and adjusted chip settings improve the SNR enough to make even small signals distinguishable from background noise.

For the usage as detectors HV CMOS chips should be kept at low temperatures and the chip settings have to be checked and adjusted in regular cycles. Both linear and enclosed pixels show similar signal-to-noise ratios, however have certain advantages and disadvantages. In future designs a good combination of linear and enclosed transistors should be used.

3.6 Digital Readout

In the preceding chapters the analog signal generation and handling was discussed. But the HVStripV1 chip does not only offer analog logic, but also digital logic. For the transition from analog to digital part two different comparators can be used. A normal comparator (NC) compares the analog signal coming from the amplifier with an externally set threshold Th1. As second option for digitization the time walk compensating comparator (TWCC) compares the analog signal with two thresholds to compensate the time walk effect.

For readout purposes the address of the hit pixel is sent. To handle two simultaneous hits the chip has two address busses. Further the chip features a hitbus which can be connected to arbitrary pixels, allowing external signal analysis.

3.6.1 S-Curve Measurements

An S-curve measurement can picture the analog noise and signal height from the digital point of view. Therefore the detection efficiency as a function of injection voltage is measured. For each data point 128 injections are sent into the pixel diode. The pulses crossing the set threshold of the comparator are counted. So the efficiency is given by

$$E = \frac{\text{\# signals detected by comparator}}{\text{\# injections sent}} \tag{3.27}$$

The threshold is fixed for each S-curve. A lower threshold shifts the S-curve left, a higher shifts it right (Fig. 3.31). It is desirable to have a low threshold, in order to detect small signals. A too small threshold however will confuse noise with hits. In this case the efficiency seems to be > 1.

A noiseless system would cause a step function, noise causes an uncertainty in the signal height which results in the characteristic S-curve. The shape of these S-curves contains information about original signal strength and noise (Fig. 3.32). The noise can be calculated (horizontal double arrow) from the width of the S. The noise is calculated by fitting a Gaussian distribution to the derivation of the S-curve (for details see appendix A). The position of the S-curve corresponds to the original signal strength (vertical arrow).

Between amplifier output and comparator input is an optional low pass filter located, which can be switched on and off. The expected effect of this low pass is a reduction of noise on

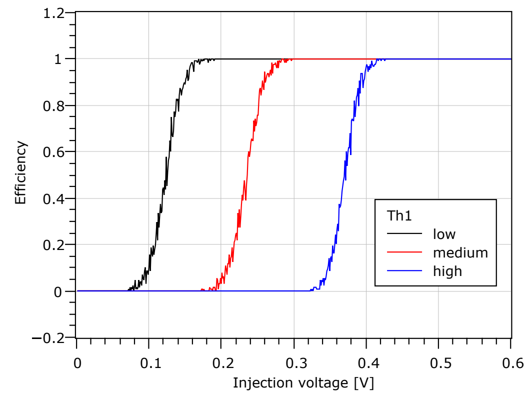


Figure 3.31: Detection efficiency as a function of injection voltage form S-curves. Each S-curve is taken for a different threshold.

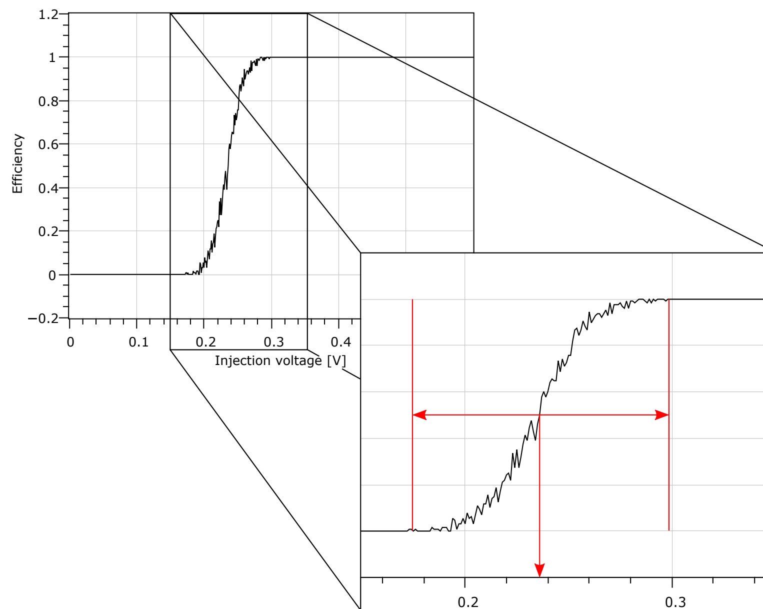


Figure 3.32: Information about noise and signal strength can be obtained from S-curves. A measure for noise is the width of the transition zone (horizontal double arrow). The position of the S-curve determines the analog signal strength.

the cost of increasing the rise time. A bigger rise time means a stronger time walk effect, as well.

In order to inspect this behavior, S-curves with and without extra low pass filter are measured and their noise compared. Fig. 3.33 shows the data obtained from S-curve measurements. The extra filter reduces the noise of an un-irradiated chip by about 5 - 15%. The effect is more significant on irradiated chips.

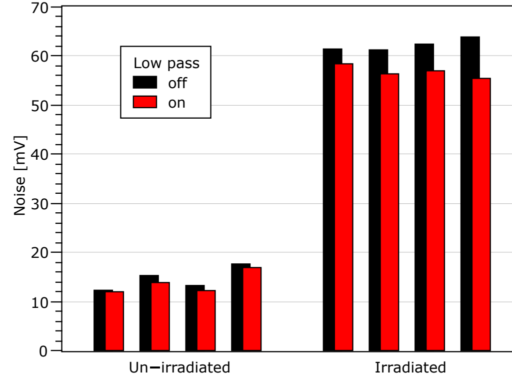


Figure 3.33: The effect of an extra low pass filter on the noise of four pixels. The measurement has been performed before irradiation and after a total X-ray dose of 200 kGy. The red bars show the situation with, the black ones without extra low pass filter.

3.6.2 Tuning of Threshold Th1

It has been shown already in chapter 3.3 that the signal height is not homogenous. Neither for pixels of one type, nor for pixels of one chip and obviously not for pixels of different types. The noise of the pixels show inhomogeneity as well. This means that if the comparators had all the same settings, either low signals would get lost in some pixels or noise would be detected as hits in others. Further the comparators show mismatch. That means that they do not react uniformly to a threshold due to imperfect production.

Tune DACs can be used to cope with this situation. The externally set global threshold can be adjusted for each comparator by the use of them. This means that the local threshold is the sum of the externally set threshold and an individual offset. If those DACs are set properly, the signals of all pixels show the same behavior, once they have been digitized by the comparator.

Before tuning, the optimal threshold of each pixel has to be found. Fixed bunches of 128 injections are sent repeatedly while the threshold is varied until the threshold is found at which 50% of the injections are detected (cf. 50% point of S-curves). These critical thresholds are shown in Fig. 3.34. After the tuning process has been completed, the same threshold works for all pixels. The local threshold is influenced by three global setting and an individual 4-bit Tune-DAC:

$$\mathrm{Th}_{\mathrm{local}} = \mathrm{Th1} - \mathrm{TDAC}_{\mathrm{normal}} \cdot \frac{\mathrm{VN}_{\mathrm{TuneNor}}}{\mathrm{ThRes}} \tag{3.28}$$

The $\mathrm{TDAC}_{\mathrm{normal}}$ can have 16 possible settings. They are multiplied with another value which is defined by global settings $\mathrm{VN}_{\mathrm{TuneNor}}$ and ThRes. In other words $\mathrm{TDAC}_{\mathrm{normal}}$ is the number of 'steps' and $\mathrm{VN}_{\mathrm{TuneNor}}/\mathrm{ThRes}$ is the step width. For a precise tuning the step width must not be too big, but big enough to bring all local thresholds to the same global threshold level.

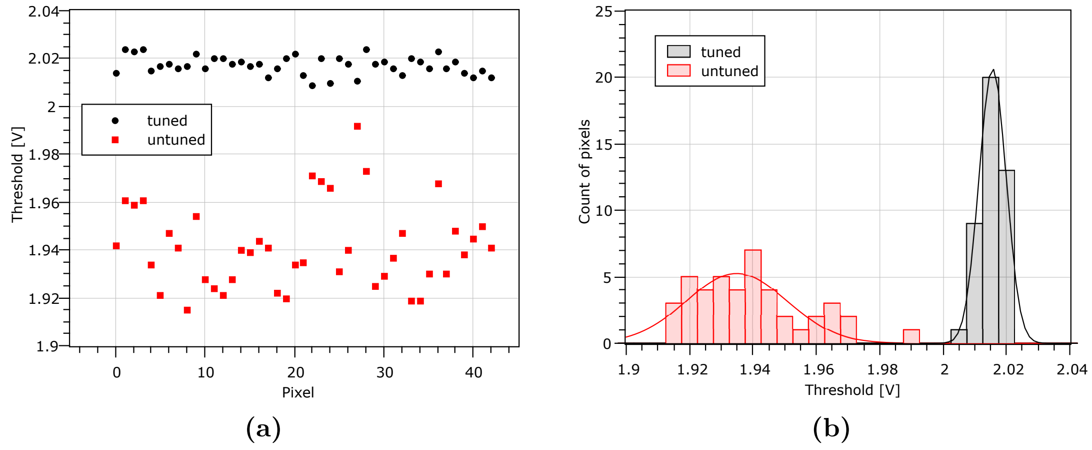


Figure 3.34: Threshold for which the detection probability of 0.3 V injections is 50%, before (red) and after (black) the thresholds have been tuned. The value of each pixel is shown in a) and the distribution of those threshold in b)

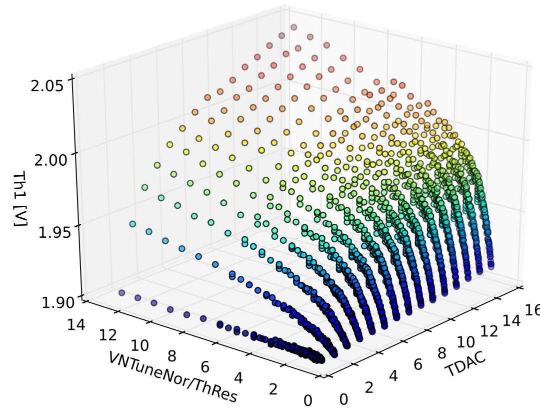


Figure 3.35: Lowest possible thresholds as a function of $\mathrm{TDAC_{normal}}$, $\mathrm{VN_{TuneNor}}$ and ThRes

A measurement of Th1 while varying $\mathrm{VN_{TuneNor}}$, ThRes and $\mathrm{TDAC_{normal}}$ (Fig. 3.35)shows that Eq. (3.28) has to be adjusted. Applying fits to data with a certain $\mathrm{TDAC_{normal}}$ value lead to the following empirically found equation:

$$\mathrm{Th_{local}} \approx \mathrm{Th1} - 2 \cdot \mathrm{TDAC_{normal}} \cdot \ln\left(\frac{\mathrm{VN_{TuneNor}}}{\mathrm{ThRes}}\right) \tag{3.29}$$

The fraction $\mathrm{VN_{TuneNor}}/\mathrm{ThRes}$ has to be set in a way that varying $\mathrm{TDAC_{normal}}$ can cover the differences of the individual thresholds. Because of the logarithmic behavior the lowest $\mathrm{TDAC_{normal}} = 0$ should not be used. The best value for $\mathrm{VN_{TuneNor}}/\mathrm{ThRes}$ is found by using the boundary conditions[3]

$$\mathrm{Th_{max}} \approx \mathrm{Th1} - 2 \cdot 1 \cdot \ln\left(\frac{\mathrm{VN_{TuneNor}}}{\mathrm{ThRes}}\right) \tag{3.30}$$

$$\mathrm{Th_{min}} \approx \mathrm{Th1} - 2 \cdot 15 \cdot \ln\left(\frac{\mathrm{VN_{TuneNor}}}{\mathrm{ThRes}}\right) \tag{3.31}$$

$$\mathrm{Th_{max}} \stackrel{!}{=} \mathrm{Th_{min}} \tag{3.32}$$

[3]This defines only the relation between $\mathrm{VN_{TuneNor}}$ and ThRes. To minimize the current flow, low values for both settings are desirable.

Where Th_{max} is the highest threshold and Th_{min} is the lowest threshold that has been measured for an individual pixel. With these settings the $TDAC_{normal}$ settings for each pixel can be found.

Repeating the 50% search with the found settings reduces the difference between the highest and the lowest threshold by 80% (Fig. 3.34). Another way to review the success of the tuning procedure is the comparison of S-curves before and after the tuning process in Fig. 3.36. If good values for all variables are found[4], the S-curves are all close together, in contrast to the S-curves before tuning.

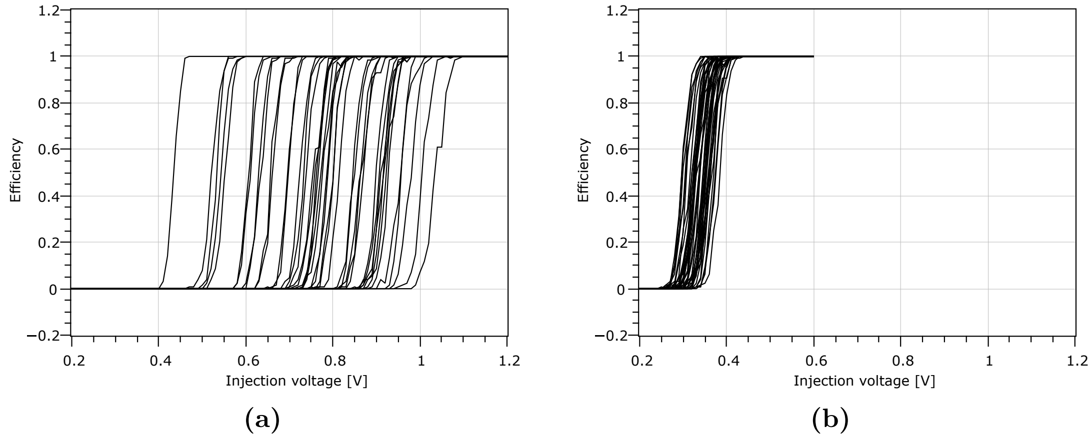


Figure 3.36: S-curves of all pixels for a constant global threshold. In a) for an un-tuned chip are the curves spread over a large range, after tuning in b) are all close together.

It turned out in several test runs that the lowest injection voltage for this chip is 0.08 V ($\hat{=}$ 500 e^-), for which the tuning is successful.

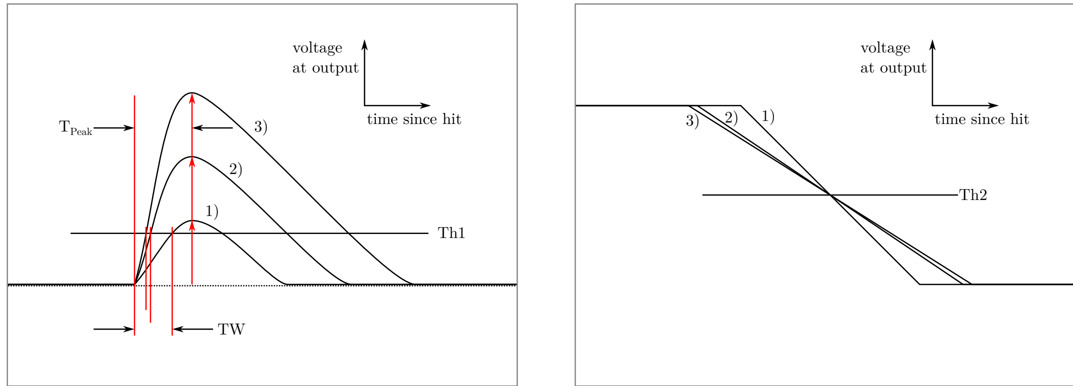
3.6.3 Time Walk Compensating Comparator

Most detector projects require a good time resolution. The LHC experiments for example have to work with a frequency of 40 MHz. That does not mean that hit data has to be processed within 25 ns, but that the time uncertainty must not exceed this time. Amplifiers however have a different threshold crossing time for different pulse heights (Fig. 3.37a). The difference between small and big pulses can exceed 100 ns. There are basically two options to cope with this time walk effect. One is to reduce the rise time of the amplifier, which is possible but increases the power consumption and noise. Another more elegant way is the implementation of a comparator which compensates the time walk effect, the time walk compensating comparator (TWCC). Such comparator is implemented in the HVStripV1 chip.

Fig. 3.38 shows the simplified circuit diagram of the TWCC used in the HVStripV1. The left side is a normal comparator (cf. Fig. 2.14) which compares the input to Th1. The clue is the right half. This common source stage has a double input. Wire 1) is the output of what a normal comparator would be. The transistor with gate 2) gets the same setting as the comparator's PMOS transistors. The output timing of the TWCC is depending on how fast the output capacity is loaded, thus on the voltages at 1) and 2).

For explanation we look at the cases of very small and very strong signals:

[4] In this example 0.3 V was the predefined injection voltage at which the 50% point of the S-curves should be. The following values were found: $Th_{global} = 2.024\ V$, $VN_{TuneNor} = 40$ and ThRes = 5.
First tuning runs took many hours. Improving the procedure and using binary search instead of linear search reduced the needed time to about 3:30 minutes.



(a) A normal comparator compares the signal to a fixed local threshold Th1 (cf. chapter 3.6.2). This causes a time walk effect.

(b) A second comparator compares the output of the first one to a second threshold Th2.

Figure 3.37: The signal passes through two comparators. The response of the first one is slow for high signals (3) and fast for low signals (1). The second comparator has its threshold Th2 set in the intersection point of the first comparator's output signals.

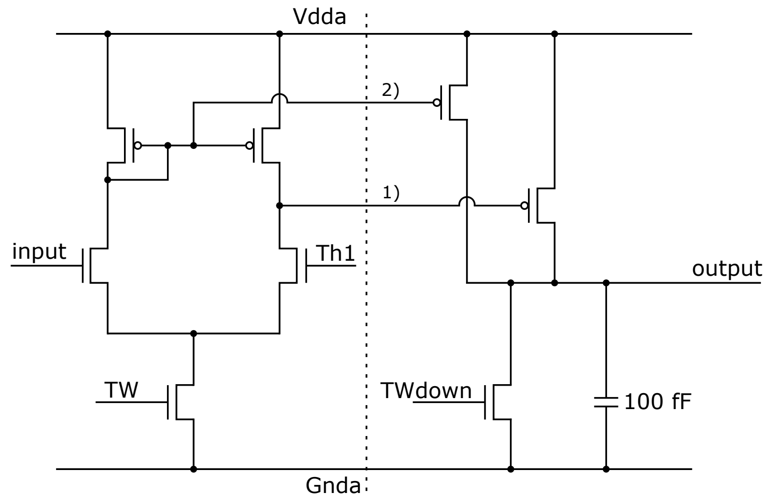


Figure 3.38: The circuit diagram of the time walk compensating comparator is similar to a normal comparator (Fig. 2.14). The output has to be connected to a normal comparator.

- Signals below Th1 do not lead to an output signal, because the input transistor is not conducting and thereby both transistors with gate 1) and 2) do not conduct as well. The output capacitance remains charged.
- For small signals right above the threshold, transistors with gate input and Th1 are equally conductive. That means each of them conducts $1/2\ I_{\mathrm{TW}}$. This current is copied by the transistor with gate 2). The PMOS transistor with gate 1) is the output of a normal not inverting differential amplifier and does not contribute to the unloading current, because its U_{GS} becomes zero.

$$I_{\mathrm{unload}} = I_{\mathrm{TWdown}} - 1/2 I_{\mathrm{TW}} \tag{3.33}$$

  The output capacitance unloads quickly, the response is fast.
- Big signals make the input transistor more and the Th1 transistor less conductive. The bias current I_{TW} flows completely through the input arm. This current is copied to the transistor with gate 2). The transistor with gate 1) does not contribute. In this case the loading current is

$$I_{\mathrm{unload}} = I_{\mathrm{TWdown}} - I_{\mathrm{TW}} \tag{3.34}$$

The output capacitance unloads slowly, the response is slow.

So we see that the TWCC reacts slower to signals with higher amplitudes and faster to signals with lower amplitudes. This is the opposite behavior of the amplifier. In result the TWCC's output signals intersect all in one point independent of the original pulse height. A second normal comparator with its threshold Th2 set in this crossing point (Fig. 3.37b) has an output with fixed delay, so every hit signal can be assigned to a specific event.

Two additional TuneDACs are needed for time walk compensation: The TuneDAC VNTW defines the main current of the TWCC and thereby how far the lines 1) to 3) in Fig. 3.37b are separated from each other. The TuneDAC VNTWdown defines the pull down current and thereby the slope of the signals. These two global settings can be locally adjusted by TuneDACs for an optimal time resolution (cf. chapter 3.6.2).

Simulations suggest that several combinations of VNTW and VNTWdown lead to an intersection point as shown in Fig. 3.37b. To prove this in an experiment, all free variables

- main current DAC (VNTW),
- pull down current DAC (VNTWdown),
- threshold of the second comparator (Th2) and
- Injection voltage U_{Inj}

have been varied and the delay between injection and time walk compensating comparator response has been measured for each combination. The first trial runs delivered information to reduce the amount of possible combinations from about 4.5 million to about 0.2 million promising combinations. When plotted for fixed VNTW and VNTWdown the remaining data should form figures similar to Fig. 3.37b. An example for such plot is Fig. 3.39[5]. The delay between injection and TWCC response is measured by the chip controlling FPGA. The precision of the delay time is only 10.4 ns, because the FPGA works on 96 MHz. It can be seen that the intersection point is independent of the injection voltage. In this example the second comparator's threshold Th2 should be set to 1.5 V for full time walk compensation. Note that the fit functions are exponential decays, not line fits.

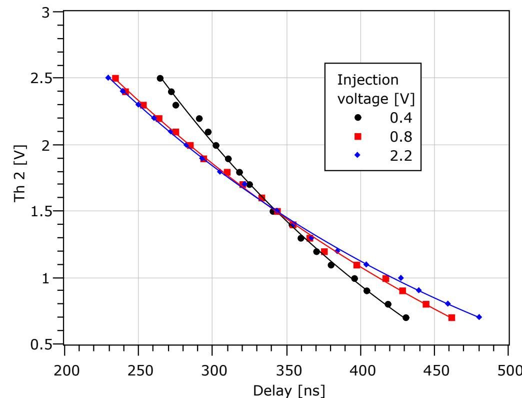
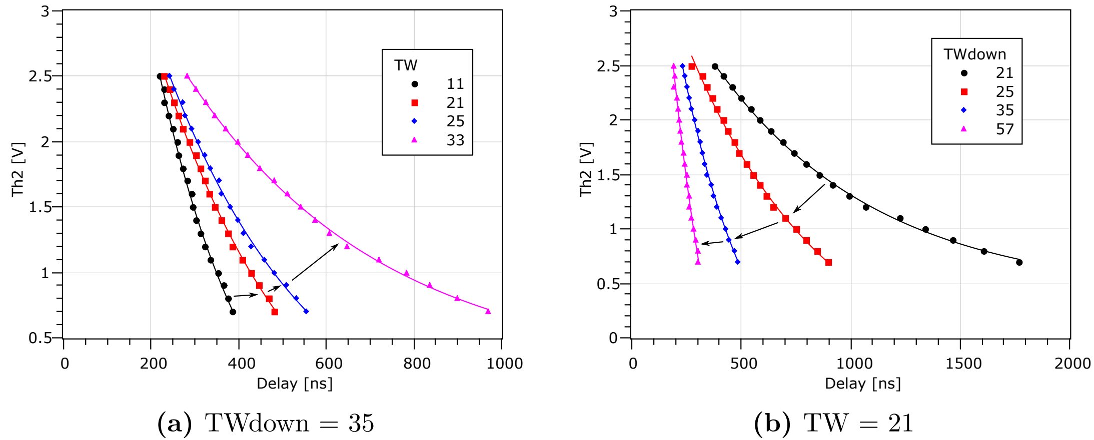


Figure 3.39: Threshold Th2 as a function of delay of the time walk compensating comparator. For this setting of VNTW and VNTWdown the delay is independent of the signal height. ΔDelay = 10.4 ns, ΔTh2 = 0.05 V

It has to be known how the tunable variables VNTW and VNTWdown influence the point of equal delay for proper tuning. The effects of varying TW(TWdown) on the Th2/delay-curve

[5]Here are only three different injections displayed. The total measurement had 15 different injection voltages (0.2 V ... 3.0 V). All intersect in the same point. Values for Th2 above 2.5 V and below 0.7 V cause invalid data.

is shown in Fig. 3.40. Increasing TW moves the curve rightwards and increases the slope. A higher TWdown on the other hand decreases the slope.



(a) TWdown = 35 (b) TW = 21

Figure 3.40: The Th2 (Delay)-curves and by that the equal-delay point can be influenced by adjusting TW and TWdown. Increasing TW moves the curve rightwards and increases the slope. A higher TWdown decreases the slope. The uncertainties are ΔDelay = 10.4 ns and ΔTh2 = 0.05 V.

Actually the point without delay variance for different injections is wanted. And also the influence TW and TWdown have on it. To gain this information a wide range of settings has been tested and the intersection points, also known as equal-delay points, have been read from the plots (cf. Fig. 3.39). The intersection points both for Th2 and delay are displayed in Fig. 3.41a and 3.42a. In several steps, including the results from simulations, plane equations have been found:

$$\mathrm{Th2}\left(\mathrm{TW},\mathrm{TWdown}\right) = a + b\cdot\ln\left(\mathrm{TW}\right)\cdot\mathrm{TWdown} + c\cdot\ln\left(\mathrm{TW}\right) + d\cdot\mathrm{TWdown} \tag{3.35}$$

$$\mathrm{Delay}\left(\mathrm{TW},\mathrm{TWdown}\right) = a + b\cdot\exp\left(-\frac{\mathrm{TW}}{c\cdot\mathrm{TWdown}+d}\right) \tag{3.36}$$

The free parameters a, b, c, d are obtained by fitting these functions to the data points. The results are displayed in Fig. 3.41b and 3.42b. Note that only settings TW/TWdown are represented here that lead to an intersection point. Some settings lead to theoretical intersection points above the maximum value for Th2, others cause no sharp discrimination between hit signal and noise which results in random delay measures. The allowed values are about:

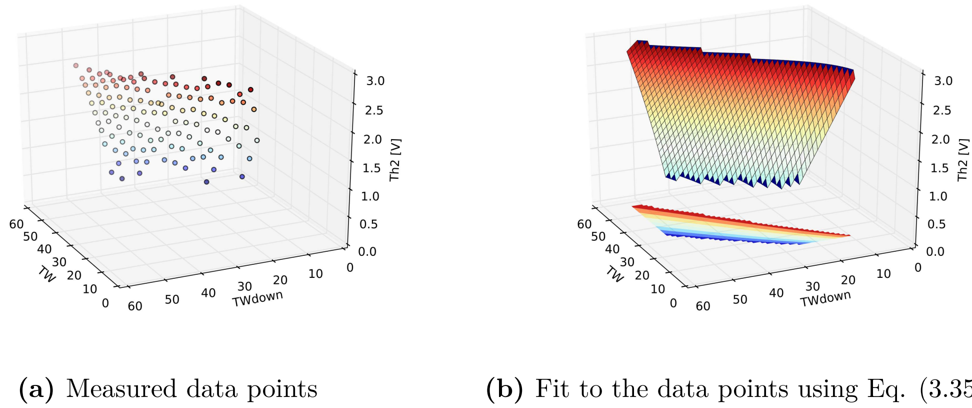
$$10 \le \mathrm{VNTW} \le 50 \tag{3.37}$$

$$15 \le \mathrm{VNTWdown} \le 50 \tag{3.38}$$

$$U_{\mathrm{Inj}} \ge 0.3\ V \tag{3.39}$$

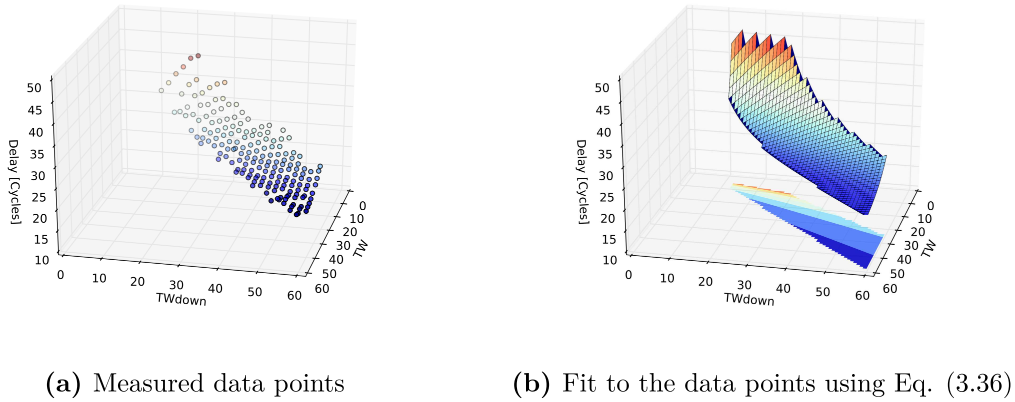
$$0.7\ V \le \mathrm{Th2} \le 2.5\ V \tag{3.40}$$

With these pieces of information a tuning process is possible, however not easily to conduct. Maybe it is possible in future designs to change the tuning procedure of the time walk compensating comparator: Instead of having tunable TW and TWdown to obtain a uniform delay for all pixels, those values could be set globally for all pixels. The only requirement would be the existence of equal-delay points. This means that each pixel has an individual intersection point with own delay and Th2. Th2 can be easily tuned on the detector chip (TuneDAC) and a time offset for each pixel can be added in an readout chip to gain time uniformity.



(a) Measured data points **(b)** Fit to the data points using Eq. (3.35)

Figure 3.41: Th2 of equal-delay points for various TW and TWdown. a) data points and b) plane fit.



(a) Measured data points **(b)** Fit to the data points using Eq. (3.36)

Figure 3.42: Delay of equal-delay points for various TW and TWdown. a) data points and b) plane fit.

3.6.4 Digital Logic after Irradiation

So far all measurements of the digital part of the chip have been performed on un-irradiated chips. As the digital logic uses, among others, linear NMOS transistors (cf. chapter 3.2), irradiation might affect the functionality. The biggest effect on a single transistor was observed at 40 kGy X-ray dose. Therefore it is reasonable to check the digital logic after this dose as worst case scenario.

After the irradiation, the first step is to check on the comparator. Injections are sent into the pixel and the response of the time walk compensating comparator is monitored. However the response of the comparator showed permanent hits, no matter how the threshold was set. This means that either the digital logic is not working at all anymore or the signal is somewhere corrupted on the path from injection to digital output. As the analog output is still working fine (cf. chapter 3.3), the problem should be searched at the comparator or the digital readout.

The HVStripV1 chip offers the possibility to measure the actual threshold at the comparator. Th1, the set threshold, and ThT, the measured threshold, are displayed in Fig. 3.43. The measured threshold is a bit lower than set, however linearity in the relevant range is given:

$$\mathrm{ThT} = \mathrm{Th1} \cdot 0.96 - 0.1\ V \tag{3.41}$$

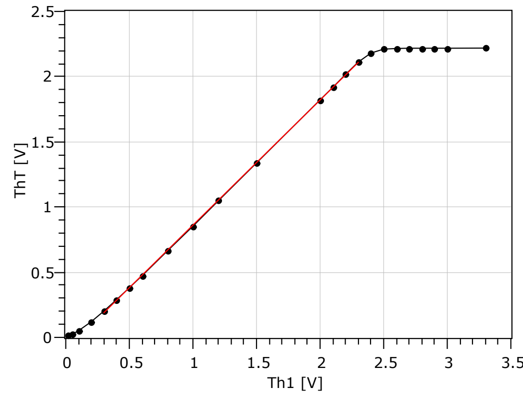


Figure 3.43: Measured threshold ThT as a function of set threshold Th1. The measured threshold is a little bit lower than set, however linearity in the relevant range is given.

In Fig. 3.44 the relation between Th1 and ThT was measured, but Th1 is a tunable value. In order to exclude any effects of the TuneDAC on the result of the measurement, the TuneDAC has been separated from the threshold. This is achieved by switching off an enclosed transistor, which controls the connection between TuneDAC logic and threshold. Switching off the TuneDAC however had another effect. The main current depends on the set threshold and has increased after irradiation. Switching off the TuneDAC results in a significantly decreased main current. This means a current of about 1 mA flows through a device, through which only a marginal current should flow. This current may be the reason that the threshold can not be set anymore and thereby the digitization of the hit signal fails.

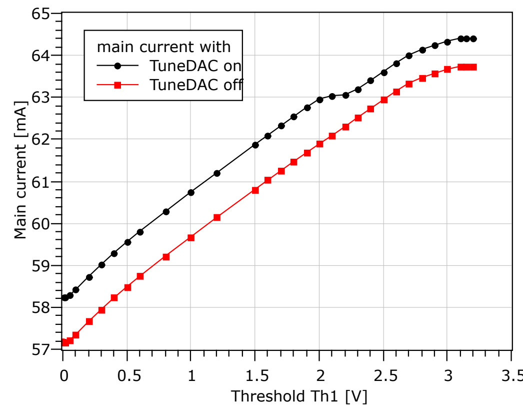


Figure 3.44: Main current with enabled and disabled TuneDAC as a function of set threshold Th1.

Closer investigation of the TuneDAC layout holds the reason why it does not block the current anymore after irradiation: It consists of linear NMOS transistors which are unable to block current anymore. Future designs may use PMOS transistors to solve this problem. After the TuneDACs have been switched off, the digitization works again and the chip sends hit signals as before irradiation.

The increased power consumption of the chip's digital section is not limited to the TuneDACs. The current flow through the digital section has been monitored while irradiating with X-rays to a total dose of 600 kGy. After each irradiation step the digital supply current has been measured, while the analog part was switched off. The digital current as a function of dose is shown in Fig. 3.45. The digital part has to use linear transistors, enclosed ones

would take too much space. Therefore it is no surprise that the behavior of the power consumption is similar to the one of a single linear NMOS transistor (cf. chapter 3.2).

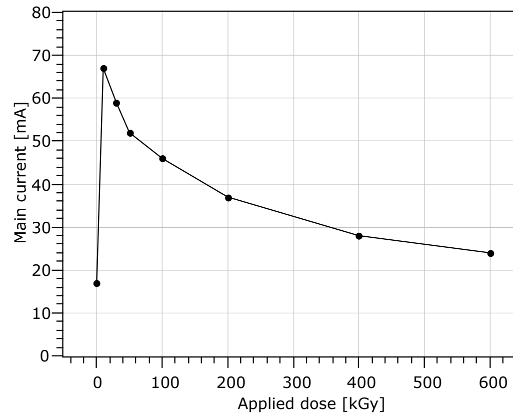


Figure 3.45: Power consumption of the digital section as a function of applied dose.

3.6.5 Summary

The digital readout part of the HVStripV1 brings promising and innovative features.

The time walk compensating comparator (TWCC) is able to digitize a hit signal without the time walk effect of a normal comparator. However the tuning process for the TWCC requires high effort for this chip. An exchange of tunable and chip-wide set values may simplify the tuning process.

Tuning the chip in a way that all pixels respond to the same signal in the same way turned out to work as expected.

Radiation hardness of the digital section is not fully given. The digital logic works only with disabled TuneDACs. The general functionality is still present, only the tuning does not work anymore. A small design modification of the TuneDACs (usage of PMOS logic instead of NMOS logic) is going to solve this problem.

4. Characterisation of the HV CMOS Sensor CCPDv1

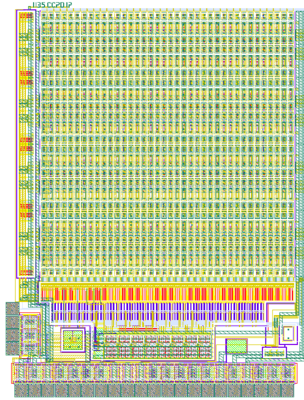


Figure 4.1: Layout of the CCPDv1 chip

The CCPDv1 is an experimental pixel detector chip, which can be capacitively coupled to readout chips. It uses the AMS H35 technology. Classic designs rely on bump- or wire-bonds to connect readout chips (ROC) and sensors. Capacitive transmission of hit information allows smaller pixels and thereby a higher spatial resolution. However this chip is not primary designed to evaluate the bondless signal transmission, but to learn more about several pixel features.

The chip has a 8 rows $\times$ 38 columns pixel matrix. Each pixel measures 50 μm $\times$ 250 μm, so the active area is about 2 mm $\times$ 2 mm. The pixels of each row have a different layout. By comparing the performance of the different rows individually, we can learn which option for each key feature leads to best results. In Tab. 4.1 the properties of each pixel row are shown.

Row	**Bump bond pad**	**Feedback transistor type**	**Input transistor type**	**Input transistor size**	**Guard ring width**	**Extra guard ring**
0	⊠	enclosed	NMOS		big	□
1	□	enclosed	NMOS		big	□
2	□	linear	NMOS		big	□
3	□	linear	PMOS	0.6 μm	big	□
4	□	linear	PMOS	0.4 μm	big	□
5	□	enclosed	PMOS	0.4 μm	small	□
6	□	enclosed	PMOS	0.4 μm	big	⊠
7	⊠	enclosed	PMOS	0.4 μm	big	□

Table 4.1: Differences in design of the eight rows of CCPDv1

The differences of the mentioned features require further explanation:

Feedback transistor type

The feedback transistor T_{FB} controls the feedback of the in-pixel amplifier as shown in Fig. 4.2. It is implemented as linear or enclosed transistor.

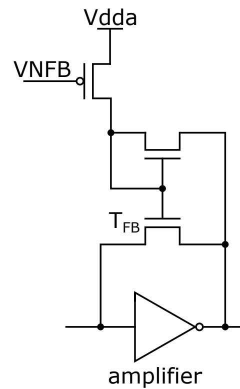
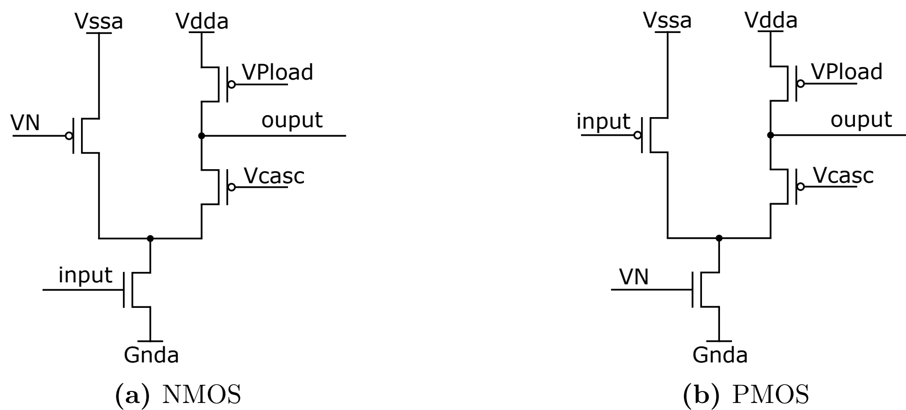


Figure 4.2: Layout of the feedback configuration. Rows 2 to 4 feature an linear feedback transistor T_{FB}, others have the enclosed version.

Input transistor type

There are two versions of the amplifier. Fig. 4.3a shows the one with NMOS input transistor, Fig. 4.3b the one with PMOS input transistor.



(a) NMOS **(b)** PMOS

Figure 4.3: The in-pixel amplifier is implemented either with a NMOS or a PMOS input transistor.

Guard ring width

The guard ring is supposed to block possible leakage current between n^{+}-diffusion and n-well (Fig. 4.4). It is implemented as a p^{+}-implant of different widths (top-view in Fig. 4.5).

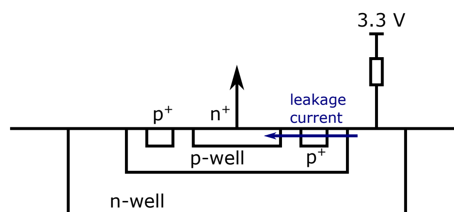


Figure 4.4: Cut through a chip showing the guard ring. The guard ring is supposed to block leakage current between n^{+}-diffusion and n-well

Extra guard ring

The extra guard ring is shown in Fig. 4.5.

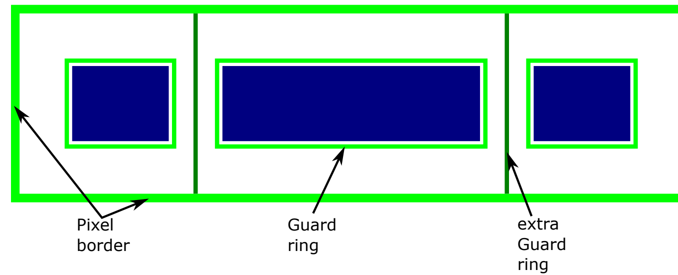


Figure 4.5: Schematic of a pixel. The electronics have a guard ring, as well as the pixel in total. The extra guard ring is only implemented in row 6.

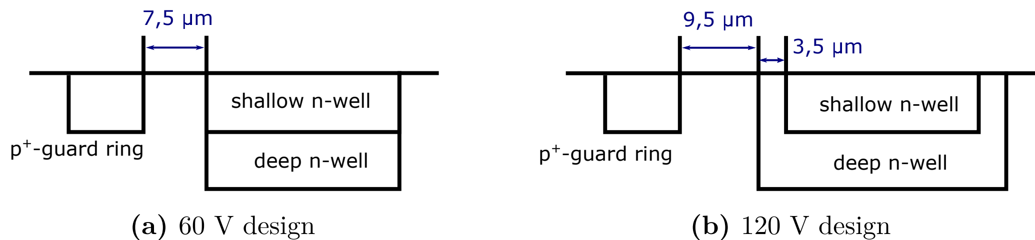
These features might have several effects on the overall performance of the chip. To make a decision on each feature, if option 1 or option 2 is more suitable, two rows can be compared which only differ in this single feature. The expected effects of these features are shown in Tab. 4.2. There may be effects on other properties as well, this will be investigated in the following chapters.

Feature	Expected influence on
Bump bond pad	no effect
Feedback transistor type	signal, noise, radiation hardness
Input transistor type	signal, noise, Radiation hardness
Input transistor size	speed, noise
Guard ring width	noise, leakage current
Extra guard ring	noise, leakage current

Table 4.2: Feature details of CCPDv1 and their expected effect on the chip's behavior

In contrast to HVStripV1 the CCPDv1 has no digital part. This chip has a second amplifier, instead of a comparator for digitization or digital readout.

Furthermore the maximum bias voltage as been doubled from 60 V to 120 V. This was achieved by leaving the guard rings floating and increasing the distance between the guard ring and the deep n-well. Fig. 4.6 shows the differences in layout. Higher bias voltage means thicker depletion zone, which is beneficial for the signal strength of charged particles (cf. Eq. (3.22)).

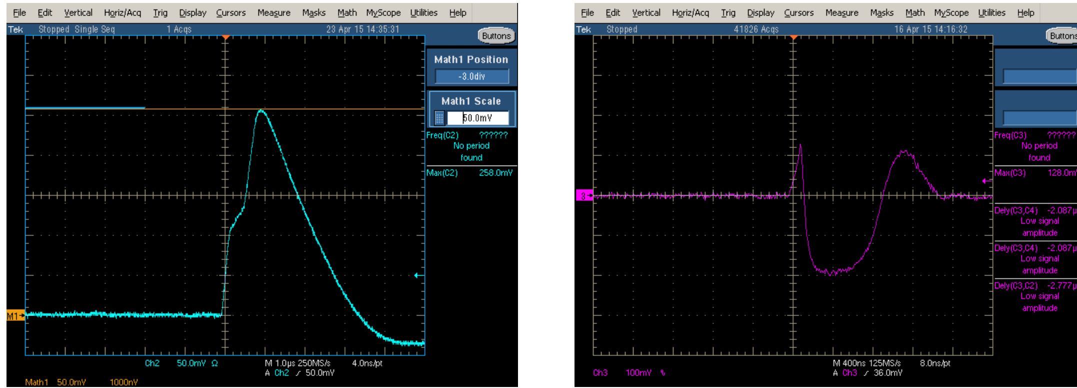


(a) 60 V design **(b)** 120 V design

Figure 4.6: Figure a) shows the layout of a 60 V proof design. Figure b) shows the 120 V proof design: The deep n-well is wider than the shallow one and the distance between n-well and p-guard ring is increased.

4.1 Initial problems

At first we have to check if the CCPDv1 works as expected. Therefore injections are sent into the pixel and the response is displayed on an oscilloscope. At the beginning the best



(a) Analog response of the first stage amplifier to a Sn-X-ray hit. The signal shape shows an unexpected ’step’.

(b) Crosstalk caused by input signals.

Figure 4.7: Irregularities shown by the CCPDv1 during the first tests.

settings for the chip were searched. However the results were not satisfying. The signal was much smaller than expected and showed an unexpected shape (Fig. 4.7).

The chip offers the option to inject a signal with well defined voltage directly into the amplifiers output. In this way we found that the source follower has an attenuation of 55%. The attenuation has been reduced to 25% by exchanging the output resistor on the PCB-board.

It turned out that the unexpected signal shape is caused by extensive crosstalk. Two sources of crosstalk were identified:
Sending signals to the chip, like a configuration sequence, leads to big signals on the chips output line (Fig. 4.7b). This is only a problem if signals are created by injections. As this problem could not be solved easily, this version of the chip should be used for external signal detection only.
The second source of crosstalk is the second stage amplifier. The signal of the first amplifier shows a more or less distinct step, dependent on the power supply of the second amplifier. We turned off the second stage amplifier whenever measuring the first stage to walk around this problem.

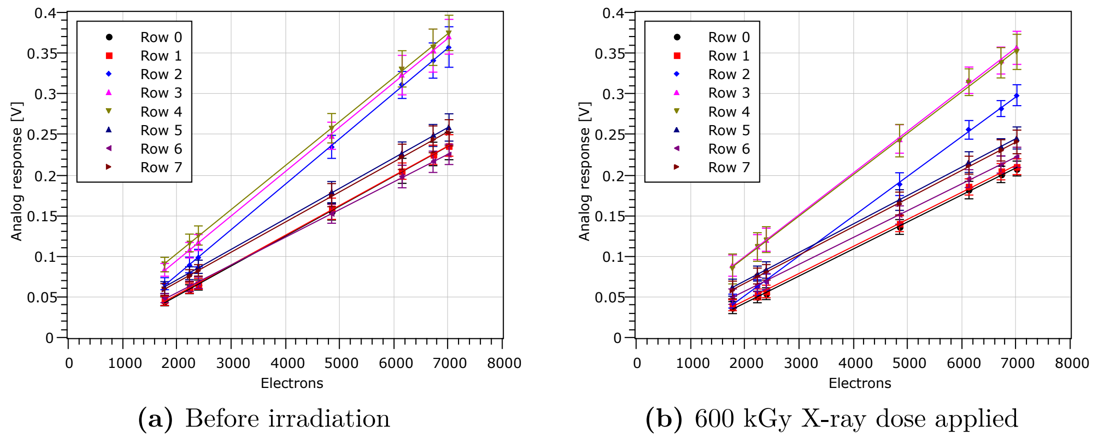
4.2 Signal

4.2.1 Calibration

We performed an X-ray calibration for each of the different rows, like we did for the strip chip HVStripV1 (chapter 3.3). Both first and second stage amplifier's output have been calibrated. The first stage amplifier shows a linear response to the number of created electrons (Fig. 4.8a). The second stage amplifier shows a linear behavior only for low energy X-rays (Fig. 4.9a). All rows show already signs of saturation for medium X-ray energies (K_α emission of Molybdenum).

These calibrations have been repeated after the chip had been irradiated with X-rays up to 600 kGy. The first amplifier shows a slightly reduced gain (Fig. 4.8b), whilst the second stage amplifier reaches saturation later (Fig. 4.9b).

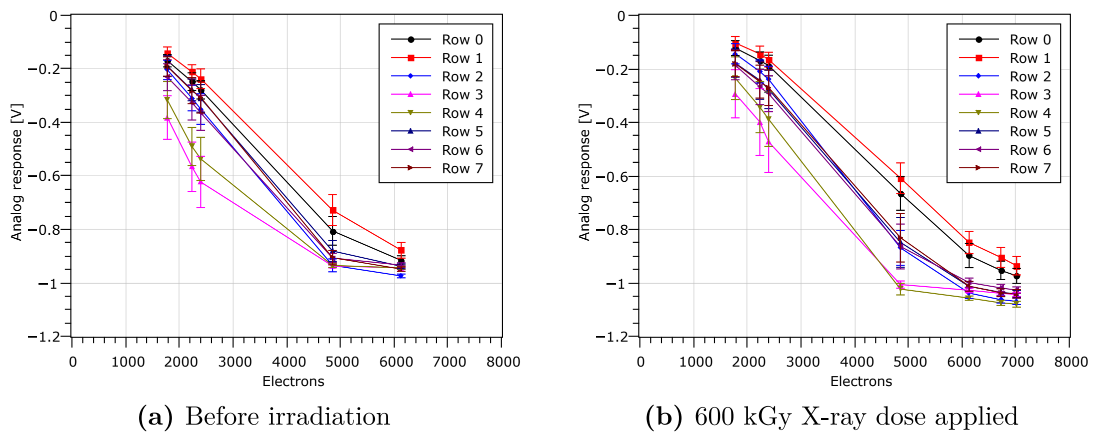
If we just plot the output of the second amplifier, we cannot be sure, whether the second stage amplifier is affected by irradiation or maybe just the first one. However we can disentangle the effects in first and second amplifier in the following way:



(a) Before irradiation

(b) 600 kGy X-ray dose applied

Figure 4.8: X-ray calibration before and after X-ray irradiation: Analog output as a function of electrons generated. Each row is affected differently by the irradiation.



(a) Before irradiation

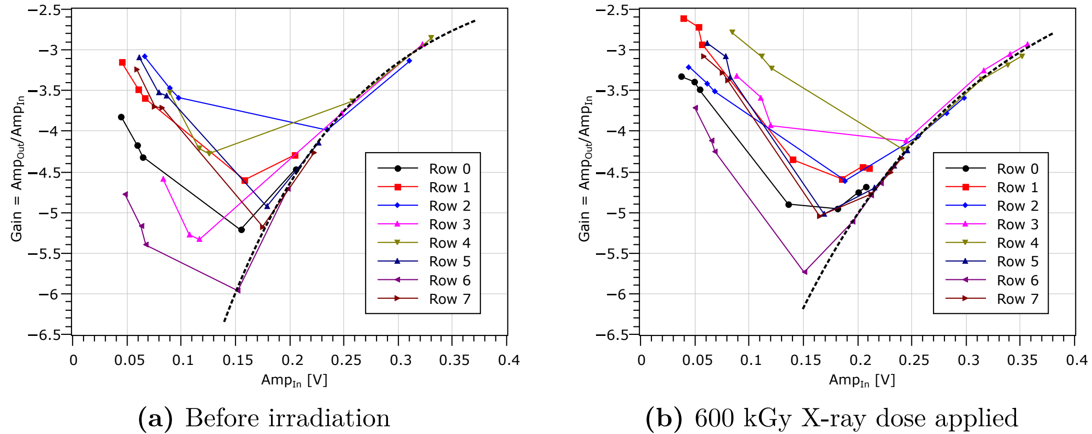
(b) 600 kGy X-ray dose applied

Figure 4.9: The response of the second stage amplifier as a function of electrons generated. It reaches saturation quickly.

Fig. 4.10 shows the gain of the second amplifier over its input signal, the first amplifier's output. Gain is here the ratio of the input and output amplitudes:

$$\text{Gain} = \frac{\text{Amp}_{\text{Out}}}{\text{Amp}_{\text{In}}} \tag{4.1}$$

By that we obtain pure information about the second stage amplifier, independent of the first stage amplifier. As the output voltage can not exceed the ground level, for high signals the gain has to decrease. For what signal strength the saturation effect occurs, is shown by the dotted line. After irradiation this line is shifted towards higher input signals, this means the amplifier reaches saturation a little bit later than before irradiation.



(a) Before irradiation **(b)** 600 kGy X-ray dose applied

Figure 4.10: Gain of the second stage amplifier as a function of its input signal. The dotted line marks the saturation effect.

For smaller signals the gain increases with increasing signal. This behavior was not expected. Usually it is assumed that the gain of an amplifier is constant in a certain range and then decreases. As this behavior could be the result of incorrect measuring, it needs further attention. In order to verify or falsify this result, a simulation was conducted. The responses of both amplifiers to input signals of different strengths are simulated (Fig. 4.11).

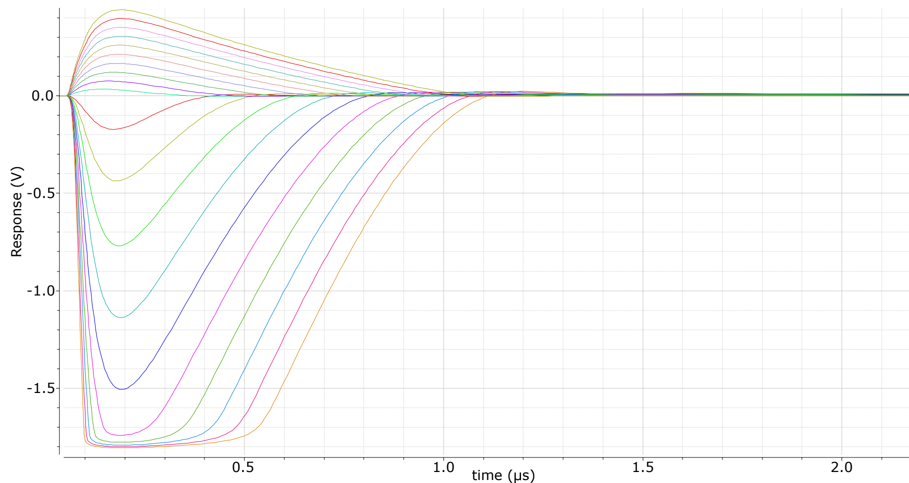


Figure 4.11: Simulation of the responses of both amplifiers to signals of different strength. Above the baseline are the responses of the first stage amplifier, below the ones of the second stage amplifier.

The maximum points of each simulated output line are used to plot the gain-over-input graph like Fig. 4.10. The resulting Fig. 4.12 shows the same behavior as the measurement.

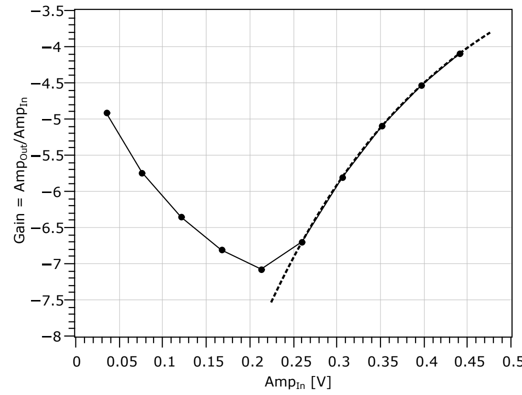


Figure 4.12: The simulated gain-over-input graph shows the same behavior as the measured one above.

However the numbers are not the same. Overall the simulated gain is a bit bigger than the measured one. Also saturation is reached for higher input signals. These differences are most likely due to the fact that the simulation was performed on schematics and not on netlist extracted from the layout. Also the simulation displays the voltage directly at the output, whilst the measured data is taken after an additional signal path to the oscilloscope.

For the comparison of the eight rows, the second stage amplifier is not important. Therefore only the calibration lines of the first stage amplifiers are used. To obtain them, lines were fitted to the data points:

$$f(x) = a \cdot x + b \tag{4.2}$$

We call a the gain and b the y-axis intersection point (y-offset). However the differences in y-offset are most likely not a property of the different designs, but of the oscilloscope or readout PCB.

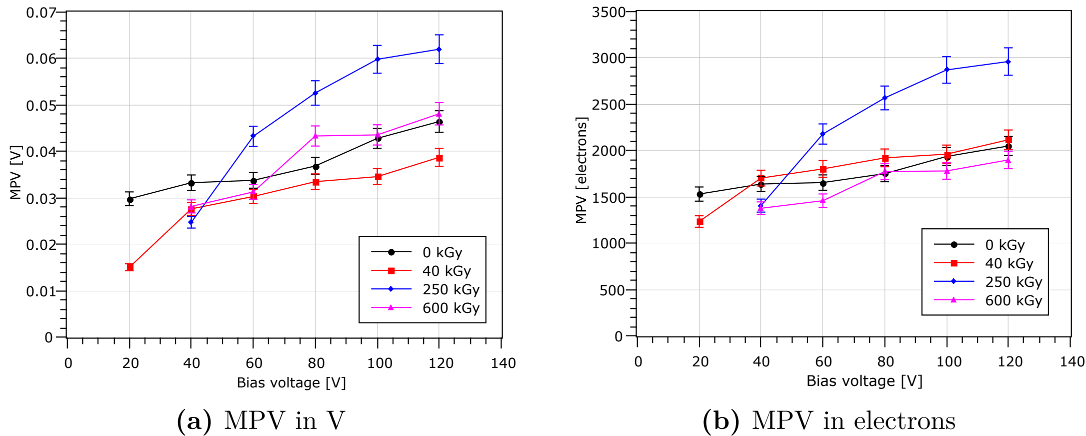
All lines are similar, but not identical. By comparing pairs of two thoroughly picked lines, the effect of isolated features on the calibration can be determined. The results of these comparisons are shown in Tab. 4.3.

Feature	**Measured difference**
Bump bond pad	no effect
Feedback transistor type	Linear feedback transistors cause a 50% higher gain than enclosed ones. After irradiation this value is only slightly reduced.
Input transistor type	Before irradiation no significant difference could be observed. However afterwards the gain of NMOS-type input transistors show a 5% smaller gain than the ones using a PMOS transistor.
Input transistor size	no effect
Guard ring width	no effect
Extra guard ring	With an extra guard ring the gain is 10% reduced. After irradiation it is still 5% reduced.

Table 4.3: The measured effect of the different features on the gain of the calibration line of CCPDv1.

4.2.2 Strontium

Charged particles generate signals differently than X-rays. As before on the HVStripV1 chip, the response of the CCPDv1 chip to charged particles has to be measured. Electrons coming from a ^{90}Sr-source pass through the detector and generate electron-hole pairs. The electrons are gathered and amplified by a charge sensitive amplifier. The signal strength is Landau-Gaussian-distributed. The most probable value (MPV) depends on the width of the depletion zone (cf. Eq. (3.22)). However the results do not form a clear picture (Fig. 4.13). Neither a square root dependency on the bias voltage can be observed, nor is the number of generated electrons as expected.
Several reasons for this outcome of the measurement have been found. However only repeating the measurement can clarify the situation.



(a) MPV in V

(b) MPV in electrons

Figure 4.13: The most probable value (MPV) of the ^{90}Sr signal is Landau-Gaussian-distributed. This figure displays the MPV from a pixel in row 0 as a function of bias voltage in either V (a) or electrons (b).

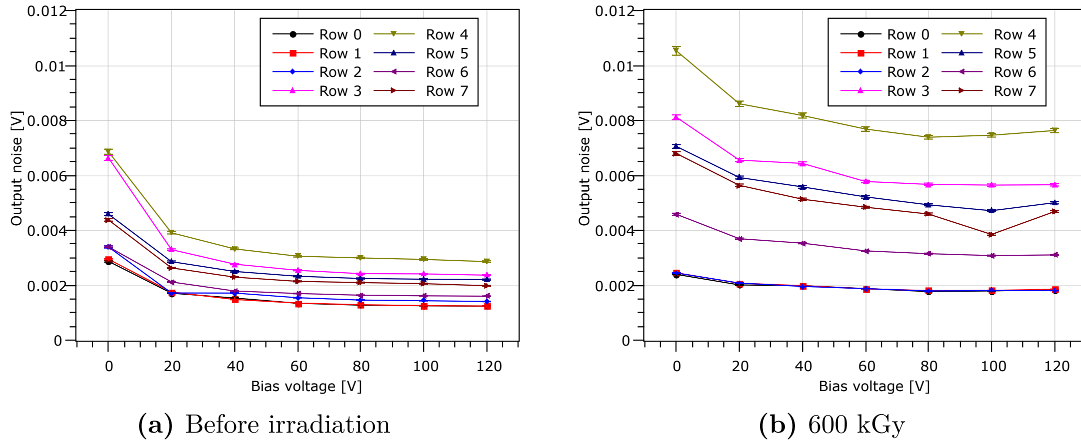
4.3 Noise

The noise of the first amplifier is shown in Fig. 4.14. As we have already seen from the HVStripV1 measurements, an increased bias voltage leads to a decreased noise. This behavior is the same for all rows and even after irradiation with X-rays up to 600 kGy. The HVStripV1 chip showed an increase of noise for increased bias voltage after X-ray irradiation. While the noise of CCPDv1 is very similar for all rows before irradiation, the spread is much bigger after irradiation.

The noise at the output of the second amplifier is higher, than the noise at the first amplifier's output (Fig. 4.15), which can be addressed to additional gain. However the increase in noise after irradiation is smaller than the increase in signal compared to the first stage amplifier. Therefore the second stage amplifier is beneficial for the signal-to-noise ratio.

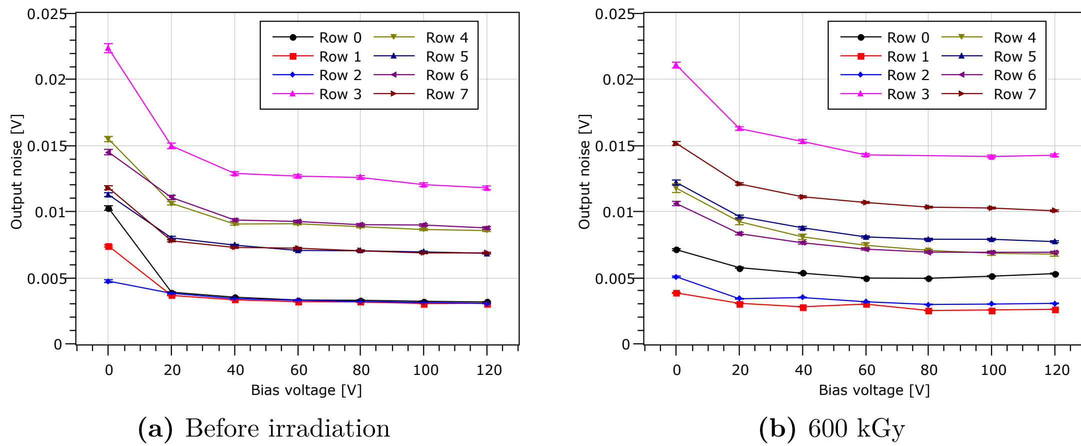
We have to decide again which feature has a positive effect on the noise. Therefore we compare the first stage amplifier's output noise of different rows.

The results of Tab. 4.4 are obtained by the comparison of only one pixel per row. The difference between the pixels of the same row can be up to 12%. This means that not all made conclusions are due to differences in layout of certain rows, but can be also statistical effects caused by mismatch.



(a) Before irradiation **(b)** 600 kGy

Figure 4.14: Noise on the output line of the first stage amplifier as a function of bias voltage. All rows show similar noise.



(a) Before irradiation **(b)** 600 kGy

Figure 4.15: Noise on the output line of the second stage amplifier as a function of bias voltage.

Feature	Measured difference
Bump bond pad	no effect
Feedback transistor type	Linear feedback transistors seem to cause a higher noise on the output. However the effect varies between 15 and 90%.
Input transistor type	The pixels with NMOS input transistors show a significant smaller noise than the ones using PMOS transistors, both before and after irradiation. The reduction is about 50%.
Input transistor size	A bigger input transistor causes a reduction of noise of about 20%.
Guard ring width	A wider guard ring has a negative effect on the noise of about 10%.
Extra guard ring	The extra guard ring is beneficial for the noise on the output line. An extra guard ring reduces the noise by 20%.

Table 4.4: The measured effect of the different features on the noise of the first stage amplifier's output of CCPDv1.

4.3.1 Signal-to-Noise Ratio

We can calculate the signal-to-noise ratio (SNR) for each row (Fig. 4.16) with the data from the last chapters. The results are summarized in Tab. 4.5. This is the most important property of a detector chip. Before irradiation the SNR is between 27 and 69. Irradiation with X-rays up to 600 kGy reduces the SNR of all rows by about 15.

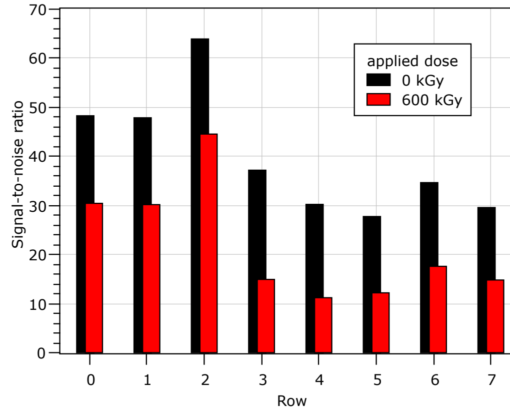


Figure 4.16: The signal-to-noise ratio of the first stage amplifier before (black) and after (red) being illuminated with X-rays.

The best SNRs are observed on rows using NMOS input transistors (rows 0, 1, 2). The highest values among those are measured for row 2, which features a linear feedback transistor.

Feature	Measured difference
Bump bond pad	no effect
Feedback transistor type	Linear feedback transistors in combination with NMOS input transistors seem to have a positive effect on the SNR of 30 - 40%. In combination with PMOS input transistor is no benefit observed.
Input transistor type	The usage of NMOS input transistors improves the SNR both before (+80%) and after irradiation (+150%).
Input transistor size	A bigger input transistor improves the SNR by 20%.
Guard ring width	The SNR of a pixel with wider guard ring is about 10% smaller than the SNR of pixels with a normal guard ring.
Extra guard ring	The reduced gain of a pixel with extra guard ring is overcompensated by the reduction of noise. This leads to an increased SNR of nearly 20%

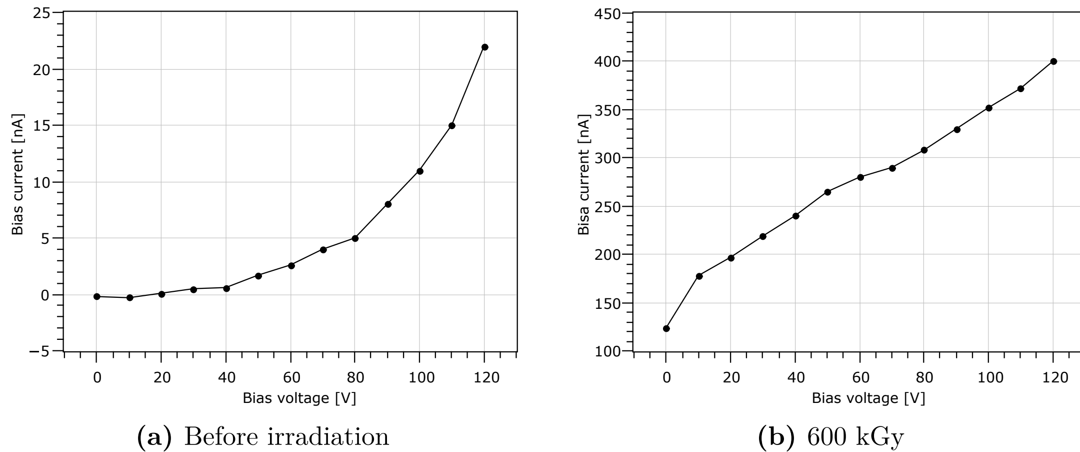
Table 4.5: The previous results about signal and noise merge into the important signal-to-noise ratio.

4.4 Bias Current

The CCPDv1 chip has a maximum bias voltage of -120 V. The resulting bias current can be measured either on the p^+ substrate contact or on the pixel's n-well contact. The

p-substrate one I_{Bias} and the n-well one I_{SensBias}. The bias current I_{Bias} measures not only the generation current in the pixel diode, but also a current consisting of charges coming from the pixel electronics. However there is no possibility to measure the current of a single pixel but only of the whole chip. This means it is impossible to evaluate the behavior of isolated rows or pixels.

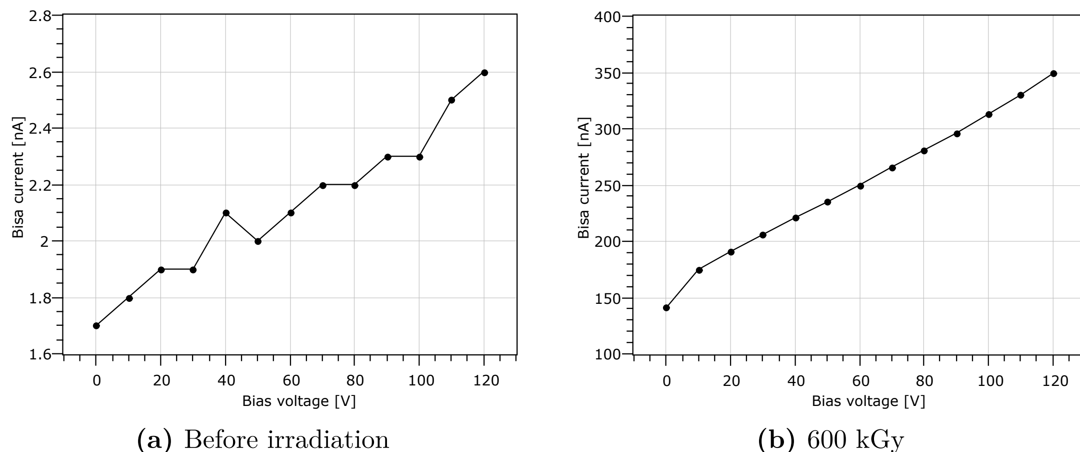
In Fig. 4.17 the total bias current is shown before and after irradiation. For the maximum bias voltage $U_{\text{Bias}} = 120$ V the total bias current is $I_{\text{Bias}} = 22$ nA. This means that 72 pA flow through each pixel diode, as the chip has 304 pixels. After X-ray illumination to a total dose of 600 kGy, the bias current per pixel has grown to 1.3 nA.



(a) Before irradiation **(b)** 600 kGy

Figure 4.17: The bias current measured at the p^{+}-substrate contact as a function of bias voltage. After irradiation it is about 20 times bigger.

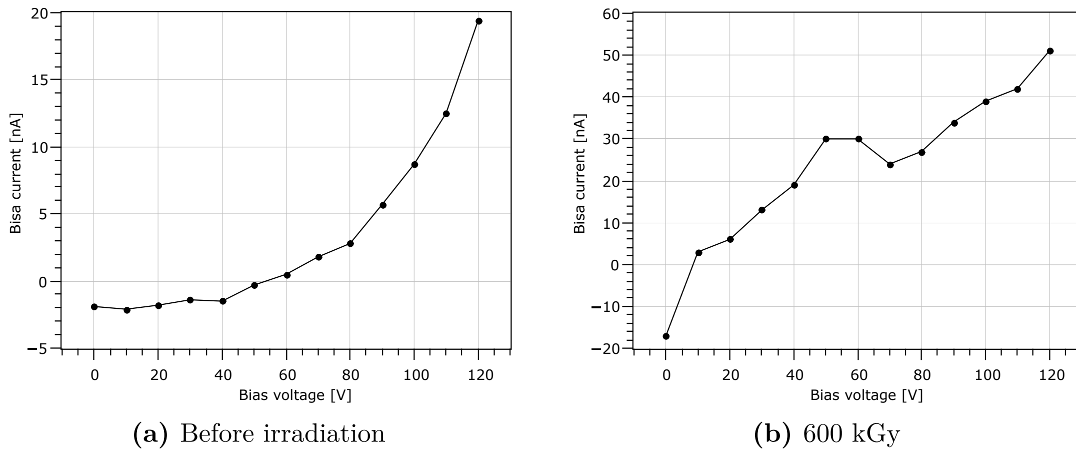
Fig. 4.18 shows the bias current measured at the n-well contact. This measurement is not affected by the in-pixel electronics. Before irradiation the measured current is 2.6 nA (8.5 pA per pixel), after irradiation these values are over 130 times increased: 349 nA in total, 1.1 nA per pixel.



(a) Before irradiation **(b)** 600 kGy

Figure 4.18: The bias current measured on the n-well contact as a function of bias voltage. It does not include the charges coming from the periphery.

We can deduct from this measurement that the periphery contributes significantly to the bias current. The calculated values are shown in Fig. 4.19. The contribution from the electronics increases after irradiation as well, but only by the factor 2.6 from 19.4 nA (64 pA per pixel) to 51 nA (167 pA per pixel).



(a) Before irradiation **(b)** 600 kGy

Figure 4.19: The current as a function of bias voltage with its origin in the pixel electronics is calculated as the difference of I_{Bias} and I_{SensBias}

4.5 Summary

The duty of the CCPDv1 chip is to determine which pixel features are beneficial for HV CMOS pixel sensors in high energy physics. It has some minor issues, which can be worked around. The different row types show significant differences in signal-to-noise ratio.

Bump bond pad

A significant difference between pixels with and without bump bond pad could not be observed.

Feedback transistor type

Linear feedback transistors increase both noise and signal in comparison to enclosed transistors. In combination with an NMOS input transistor the signal growth is bigger than the noise growth; with a PMOS input transistor the growth is equal. This can be explained by higher open loop gain of the NMOS version.

Input transistor type

The input transistor type had the biggest influence on the signal-to-noise ratio in this measurement series. NMOS input transistors show a much better performance than PMOS ones both before and after irradiation. This is probably caused by better transconductance g_m of NMOS transistors.

Input transistor size

The effect of a bigger input transistor size on the SNR is an improvement of 20%. The size of the input transistor is only variable for (linear) PMOS transistors. We saw that an enclosed NMOS transistor shows an SNR-benefit bigger than 80%. In result the NMOS transistor is the better option than a PMOS transistor of increased size.

Guard ring width

A wider guard ring brings no benefit in terms of SNR. If it helps to reduce leakage current can not be measured, because only the combined bias current of the whole chip can be measured.

Extra guard ring

The extra guard ring reduces both noise and gain. Bottom line a SNR benefit of 20% remains. Further the leakage current may be positively affected.

The conducted measurements on the rows of CCPDv1 recommend some design details over others. And thereby CCPDv1 fulfils its duties. Further we learned that the second stage amplifier is capable of improving the signal-to-noise ratio.

Future measurements should be done with bigger statistics (measuring all pixels of a row) and should include a proton or neutron irradiation campaign. Furthermore a delay measurement (time between hit and response) for diverse signal strengths might be interesting to learn more about the timing of the chip.

5. Characterisation of the HV CMOS Sensor CCPDv2

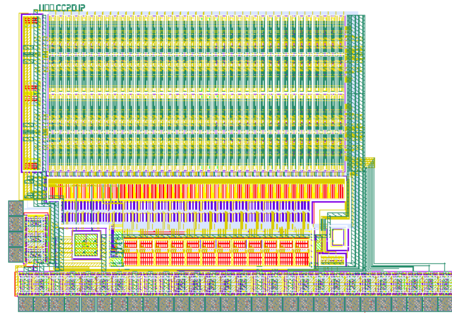


Figure 5.1: Layout of the CCPDv2 chip

CCPDv2 is the name of another pixel chip in AMS H35 technology. Like the previous discussed CCPDv1, it is a pixel chip with a 4 rows × 38 columns pixel matrix, where each pixel measures 50 μm × 250 μm. In contrast to CCPDv1 this chip is not primarily designed to evaluate different layout details. The main feature is that not only the amplifier, but also a time walk compensating comparator (TWCC) is located inside each smart pixel. The HVStripV1 has all digital electronics including the TWCC in a separate digital block outside the pixels. This difference makes it necessary to adjust the TWCC's layout slightly. All pixels have the same layout except for row 0. This row reacts faster, on the cost of smaller gain and higher noise. This is achieved by a different feedback design of the amplifier (Fig. 5.9).

The goal of the following experiments is to check on the in-pixel TWCC, compare the faster and slower rows and of course have a look at the overall performance.

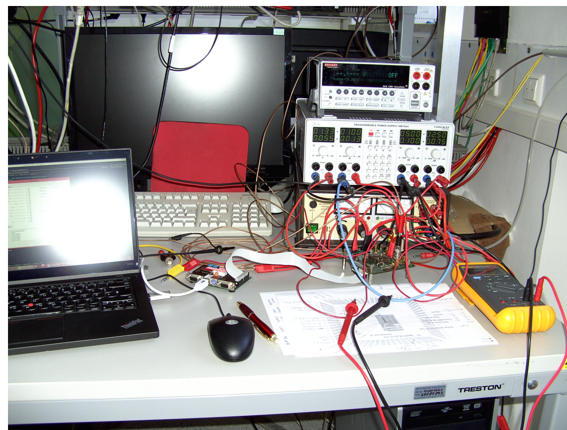


Figure 5.2: The setup of CCPDv2 needs many externally set voltages.

Getting started with this chip turned out to be more complicated, than with previous ones. The PCB, on which the chip is mounted, needed some revision and requires many externally set voltages (Fig. 5.2).

First tests showed that this chip has the same crosstalk issue as the CCPDv1: Whenever the electronics after the amplifier is powered, the amplifier is affected. We cope with this problem in the same way as at the CCPDv1 and just turn off the adjacent electronics, whenever measuring the analog output.

5.1 Signal Detection

5.1.1 Fe55 X-rays

The setup for this chip is more complicated than for the already examined chips. This makes calibration with the X-ray tube very difficult, so the calibration was performed using the X-rays from a ^{55}Fe-source only (Fig. 5.3).

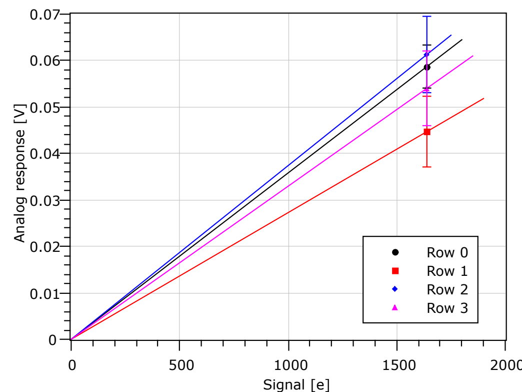


Figure 5.3: Output calibration using a ^{55}Fe X-ray-source.

The noise measurement was not successful, because the readout chip had an issue, which caused the output line to have a big additional noise. Whenever the oscillator of the FPGA board is running, it has a big effect on the chip's output. At this time a replacement for the FPGA board was not available.

5.1.2 Injections

We are going to test the time walk compensation on this chip. For this purpose injections with known charge and timing are necessary. As we are going to trigger on the injection signal, only the injected charge has to be determined. This is accomplished by calibrating the injection signals with the signals of ^{55}Fe.

Fig. 5.4 shows the output signals of five different injection voltages. The most probable values of those Gaussian-fits are used for calibration (Fig. 5.5a). Together with the ^{55}Fe-calibration, the electrons generated by a certain injection pulse can be calculated (Fig. 5.5b).

5.1.3 Strontium Electrons

In order to measure the signals of charged particles passing through the pixel-diode, a ^{90}Sr source is placed above the chip. The analog response of the chip is measured by an oscilloscope. The maximum of each signal is sorted by energy into a histogram (Fig. 5.6). The most probable value of the Landau-Gaussian distribution is shown in Fig. 5.7.

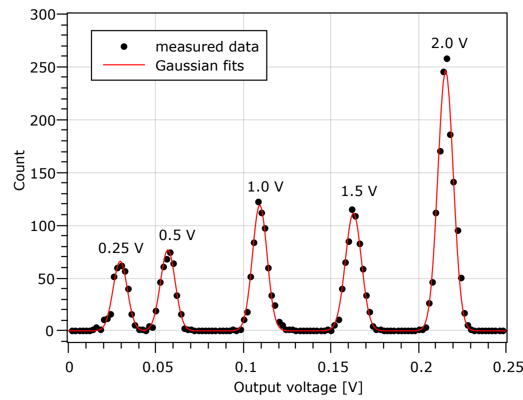
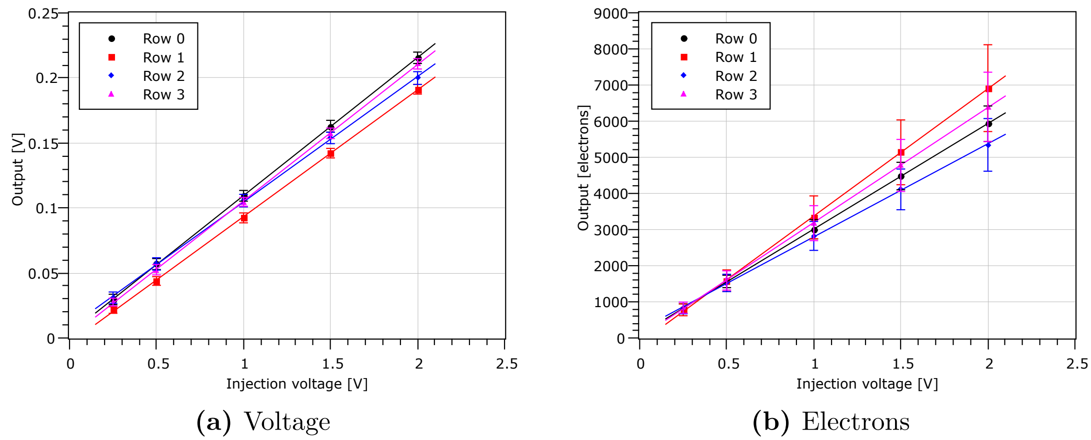


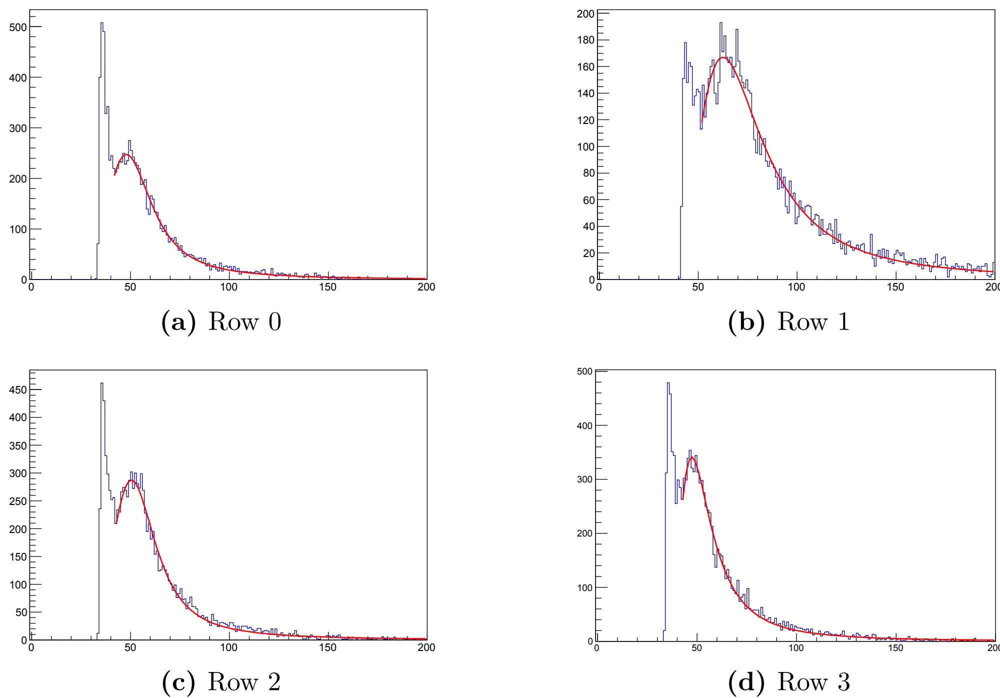
Figure 5.4: Injections with different injection voltages cause different output signals.



(a) Voltage

(b) Electrons

Figure 5.5: Output signal as a function of injection voltage for calibration of the second pixel of each row.



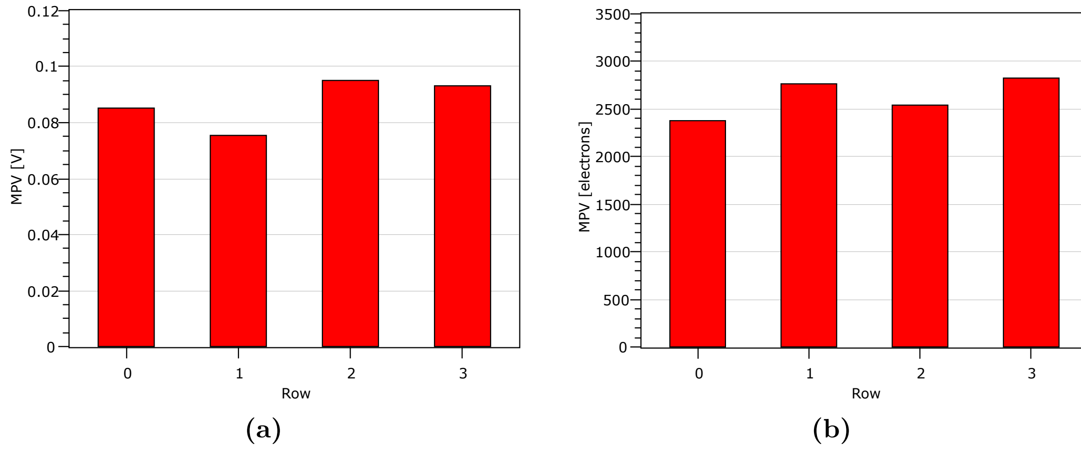
(a) Row 0

(b) Row 1

(c) Row 2

(d) Row 3

Figure 5.6: The strontium spectrum, count over energy (channel). It consists of a peak caused by passing electrons (right) and a background peak caused by low energy electrons (left).



(a) **(b)**

Figure 5.7: The most probable value of ^{90}Sr β-rays.

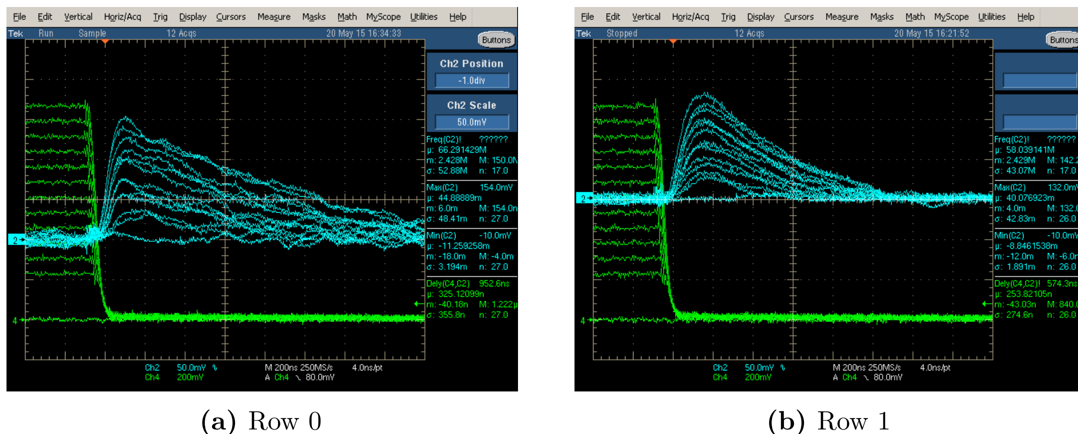
5.1.4 Signal Summary

The CCPDv2 chip detects all three types of signals as expected: X-rays, charged particles and injections. A significant effect of the feedback design on the output signal could not be observed. Most likely the effect is too small to be seen without sufficient statistics. However the speedup and increased noise caused by the changed feedback design could be measured.

5.2 In-Pixel Time Walk Compensation

This chip features time walk compensating comparators, which are located inside each pixel. This in-pixel design requires a different layout than the out-pixel design of the HVStripV1 chip, however the functional principle remains the same.

With the knowledge obtained in the experiments on the HVStripV1 TWCC and simulations, we could quickly find good settings for the required DACs. Each measurement consists of a series of injections, each with a different injection voltage. The different signal strengths cause the time walk effect (cf. Fig. 3.37a). The amplifier's output was monitored for such injection sweeps to get an idea of how big the time walk effect is expected to be (Fig. 5.8).



(a) Row 0 **(b)** Row 1

Figure 5.8: The amplifier's response to a set of injections of different strength. The time walk effect is up to 100 ns.

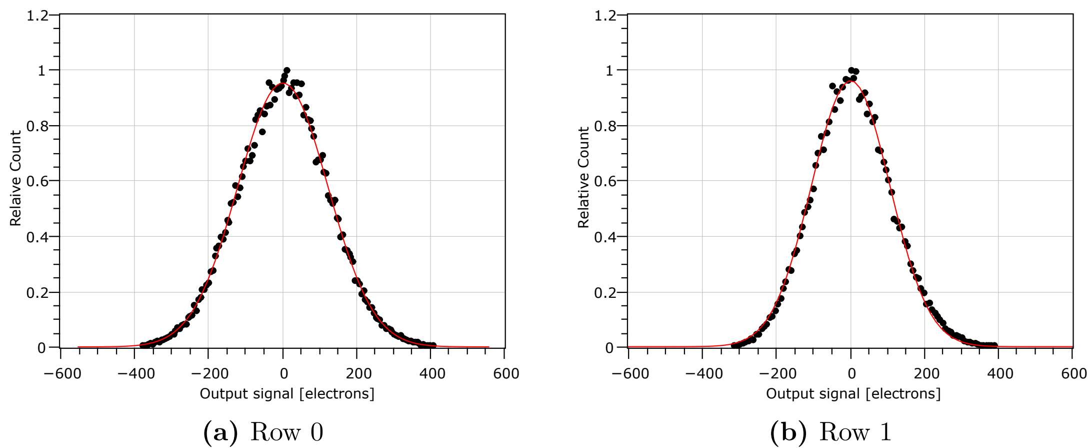
For further experiments Row 1 is used, because the smoother signal shape makes measurements easier. As the settings for both pictures in Fig. 5.8 are the same, the noisier output of Row 0 might be a result of the different amplifier's feedback setups (Fig. 5.9).

(a) Row 0 **(b)** Row 1

Figure 5.9: Row 0 has a new, faster feedback setting. The shorter reaction time is at the cost of increased noise. Row 1 features the standard design.

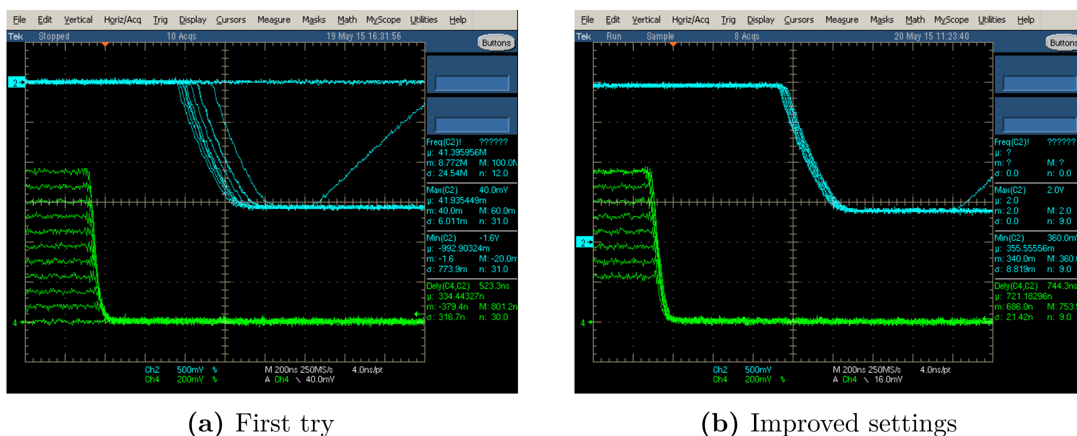
Both rows do not only differ in noise, but also in signal height and timing. The output of Row 0 reacts after about 100 ns to input signals, Row 1 needs about 150 ns. In return the signal of Row 1 is stronger and the noise is lower.

The baseline noise has been measured without the readout FPGA to exclude external noise. The result has been translated to electrons for better comparability (Fig. 5.10). The classic design shows an equivalent noise of 106 electrons, while the noise of the faster design is 122 electrons which is 15% higher.



(a) Row 0 **(b)** Row 1

Figure 5.10: The noise of the fast row (a) is 15% higher, than the noise of the row with classic feedback design (b).



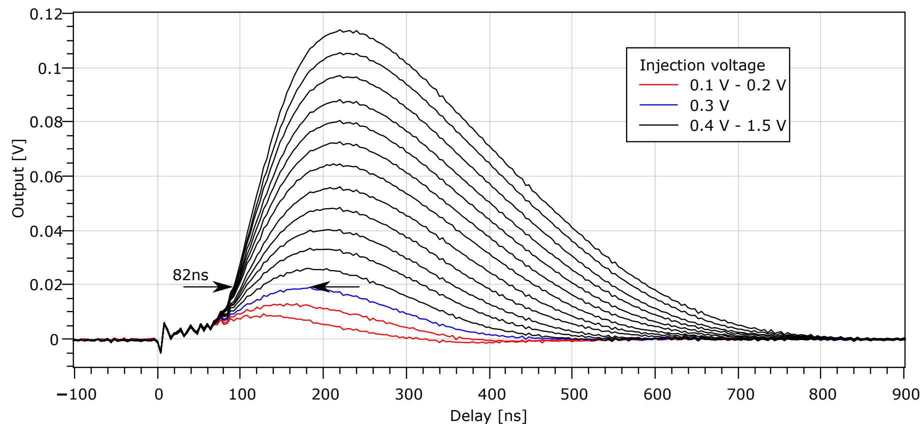
(a) First try **(b)** Improved settings

Figure 5.11: Waveforms of injection pulse (green) and comparator (blue). The output of the TWCC with the settings of the HVStripV1 shows a time walk of 200 ns. Improved settings reduce the time walk effect to less than 50 ns.

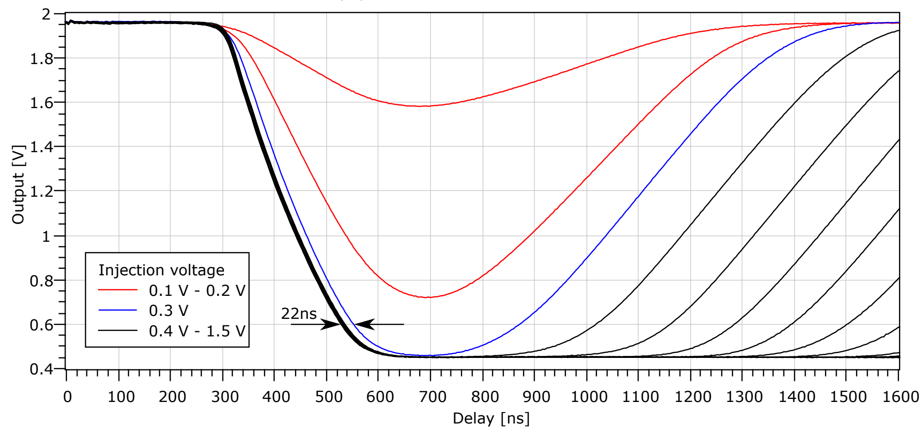
Now the output of the time walk compensating comparator is monitored while an injection sweep. For the first attempt the best settings of the HVStripV1 experiments were used

(Fig. 5.11a). The result was not satisfying, but variation of the settings quickly reduced the time walk to less than 50 ns.

The waveforms taken by the oscilloscope were read out to a computer, for fine tuning of the settings (Fig. 5.12). Further the triggering was improved. The injection sweep reaches from 0.1 V to 1.5 V in 0.1 V steps. This means about 250 to 3800 electrons.



(a) Amplifier's output



(b) TWCC's output

Figure 5.12: Responses of amplifier and TWCC to injections of various strengths.

A time walk of less than 22 ns is given for injection voltages of 0.3 V and above. This corresponds to a signal of 700 electrons. A normal comparator would show a time walk of 82 ns. To exclude such small signals, the first threshold has to be set in an appropriate way.

5.3 Summary

We were able to prove that the time walk compensating comparator with adjusted design for in-pixel usage works as well as the out-of-pixel design (cf. chapter 3.6.3). The TWCC is hardly improvable. The remaining time walk originates mainly from the amplifier.

The comparison of rows with slow and fast pixels requires more statistics for reliable results. However we see the expectation confirmed by the observations made by now.
Only the TWCC of a slow pixel has been tested. A comparison with a fast pixel should be conducted in future measurements.

In order to measure noise and signal more precisely, the readout PCB has to be replaced or repaired. Further the PCB on which the chip is mounted has to be replaced. The need of too many external set voltages prevents measurements and irradiation using an X-ray tube. These measurements however are necessary for a valid calibration and radiation hardness test.

6. Conclusion and Outlook

6.1 Summary

Future detector experiments come with new challenges and have to cope with limited budget, while the expectations towards performance are high. Radiation tolerance, power consumption, costs, efficiency, precision in time and space are key properties of detectors for particle physics experiments. The HV CMOS technology has been recognized as a promising technology even for large scale detector experiments.
In this thesis three demonstrator chips using the HV CMOS AMS H35 technology have been investigated.

The over all functionality, especially of the innovative time walk compensating comparator, has been monitored. The in-pixel signal amplification works very well on all chips. It shows a signal-to-noise ratio for minimum ionizing particles of > 30.
Both TWCC in the periphery of HVStripV1 and inside each pixel of CCPDv2 have shown time walk compensation for a wide range of signal strengths. Once the settings of the TWCC are well chosen, the uncertainty in timing is less than 25 ns. The remaining uncertainty is nearly exclusively caused by the first stage amplifier's jitter.

The radiation hardness has been tested for high X-ray (up to 600 kGy) and proton ($2 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$) doses. The effects of irradiation have been investigated for isolated structures (sensor diode and single transistors) and complex electronics.
As expected the sensor diode suffers only from proton irradiation, not from X-ray illumination. The used X-rays do not carry enough energy to dislocate atoms of the silicon bulk. Proton irradiation induces bulk defects, which cause an increase in leakage current and thereby an increase of noise. But also the amount of charges generated by a MIP grows as the depletion zone grows due to the change in doping.
X-ray irradiation affects mainly the electronics. Though the effect on linear NMOS transistors is significant, the effect on power consumption and output SNR can be kept to a minimum by a good combination of PMOS transistors with both linear and enclosed NMOS transistors.
The CCPDv1 chip has been used to identify beneficial design details for overall performance and radiation hardness.
It is remarkable that no irradiation campaign conducted in the making of this thesis caused a chip to quit working. However it turned out that chips after irradiation require different settings than pre-irradiation ones.

It has been shown that the HV CMOS in 350 nm technology is able to fulfil all expectations.

6.2 Outlook

Not all aspects of the investigated chips have been tested yet. Further information could be gained by a test-beam measurement of HVStripV1. Both the digital readout and the

TWCC could be tested in a setup environment closer to the conditions in a final application. The diverse feature details of the pixels of CCPDv1 require further investigation. The information from a larger data set could suggest more precisely which feature details bring benefit to the overall performance. Further the effect of those details on the performance of a proton irradiated chip has not yet been measured.
A new test board for the CCPDv2 chip would simplify measurements. This would allow irradiation and better calibration. The difference of fast and slow pixels could be determined with higher accuracy from a larger data set.

Designers of future demonstrator chips may profit from the results presented in this thesis in a way, whether linear or enclosed NMOS transistors are to be used for a specific purpose. Furthermore the measurements on the diverse rows of the CCPDv1 chip may help to find an optimal layout for future HV CMOS detector chips. The measurement on the TWCC of HVStripV1 suggests that the choice, which settings should be set chip wide and which individually tunable, can have a significant impact on the time a tuning procedure consumes.

We plan to conduct measurements on chips of a larger scale (2 cm × 2 cm) to prove the scalability of this technology. Also the usage of substrate with higher resistivity is planned, in order to reduce time walk by increasing the signal amplitude [7].

Appendix

A S-Curve Analysis

The measurement of noise on a digital signal is not as simple as it is on an analog signal. The noise measurement on a digital signal is performed by taking an S-curve. An S-Curve describes the detection efficiency over signal strength. It is taken by sending signals into the pixel and count the amount of signals at the comparator's output (Fig. A.1). The signal strength is reduced until the detection efficiency is zero. Strong signals show a detection efficiency of 100%, low signals of 0% and medium signals are in between. A perfect signal would show a step-function, but as the input signal is convoluted with noise, the outcome is an S-curve (Fig. A.2).

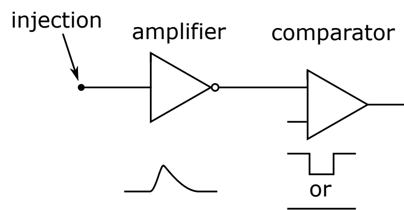
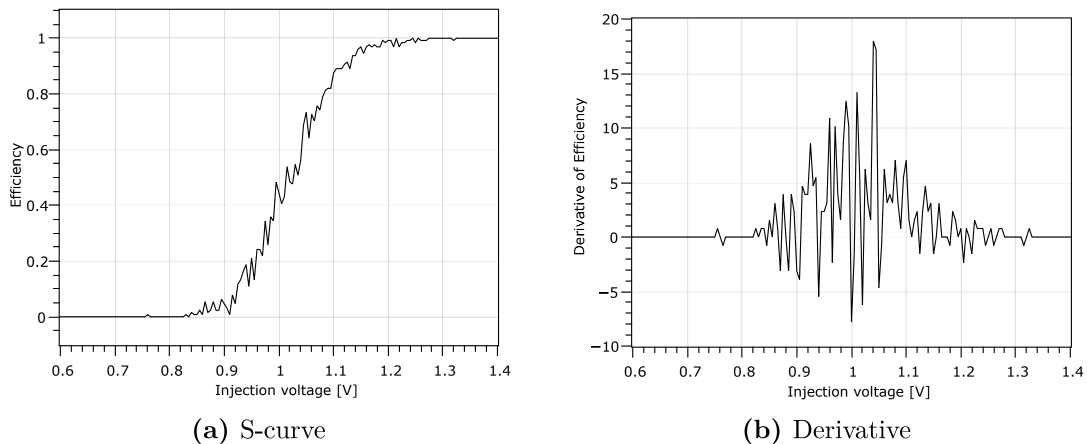


Figure A.1: The response of the charge sensitive amplifier to an injected charge is digitized by a comparator. If the signal (plus noise and uncertainties) is high enough, a hit is detected.



(a) S-curve **(b)** Derivative

Figure A.2: The originally measured S-curve shows a statistical distribution. This distribution causes its derivative to be very noisy.

For the signal analysis the derivative of the S-curve is important. It can only be determined properly for a sufficient smooth S-curve. However the S-curve is usually not really smooth for statistical reasons. This can be improved by either increasing the number of injections per data point, or by mathematical smoothing. Higher statistics requires longer measuring

time, which would not allow taking S-curves for a whole pixel-matrix with hundreds of pixels.

We used the mathematical smoothing method called 'Simple Moving Average' (SMA). Each data point η_i is replaced by the average of its own value and the value of its neighbors. The smoothing effect depends on the amount of neighbors included. The new efficiency η_i^{new} for each injection voltage is given by:

$$\eta_i^{\text{new}}\left(U_{\text{Inj}}\right) = \frac{1}{2n+1} \cdot \left(\eta_{i-n} + \ldots + \eta_{i-1} + \eta_i + \eta_{i+1} + \ldots + \eta_{i+n}\right) \tag{A.1}$$

Fig. A.4 shows the result of SMA using next neighbors ($n = 1$). If more values are used, the result becomes more and more smooth: Fig. A.5 with $n = 2$, Fig. A.6 with $n = 3$.

Once the derivative is smooth enough, a Gaussian-distribution can be fit to it (Fig. A.3), from which the noise of the signal in form of the standard deviation σ can be extracted:

$$f\left(x\right) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{x-\mu}{\sigma}\right)^2} \tag{A.2}$$

The noise σ in this example is 77 mV.

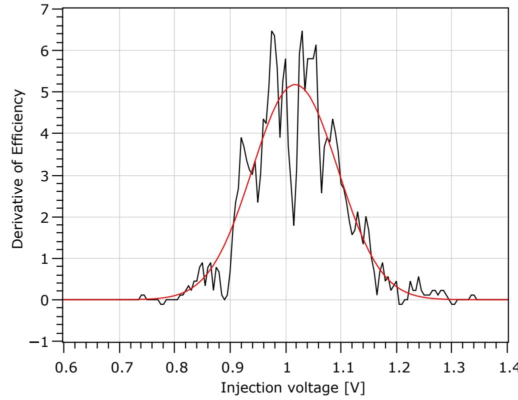
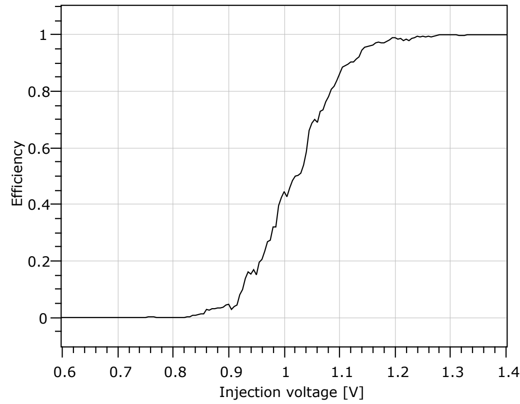
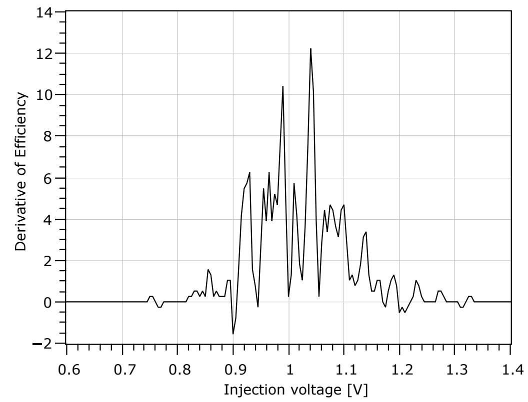


Figure A.3: SMA with $n = 3$ is sufficient for fitting a Gaussian distribution to the derivative.

Treating the S-curve with the 'Simple Moving Average' algorithm is also useful to read out the 50%-efficiency point, which is necessary for tuning. The 50%-point x can easily be read from the Gaussian function. Without smoothing the S-curve might cross the 50% point several times. In this example the point of 50% efficiency is 1.025 V.

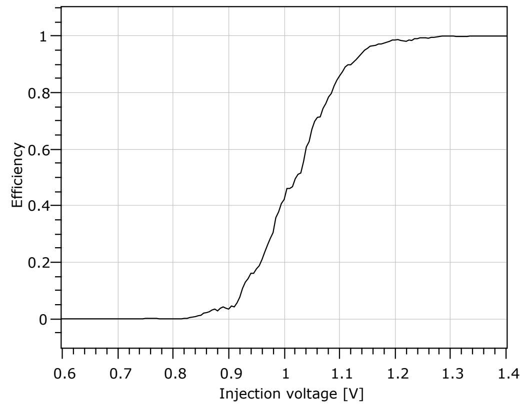


(a) The measured S-curve shows efficiency as a function of injection voltage.

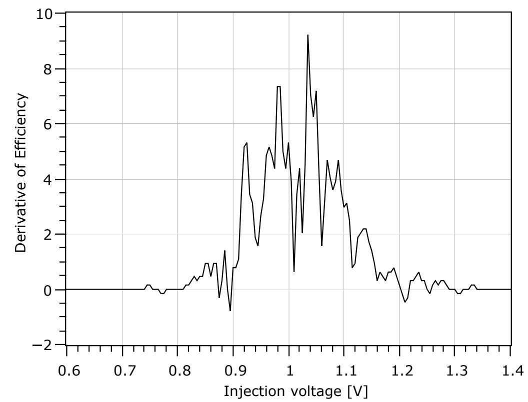


(b) The derivative of the S-curve on the left.

Figure A.4: Only 3 values ($n = 1$) are used for SMA

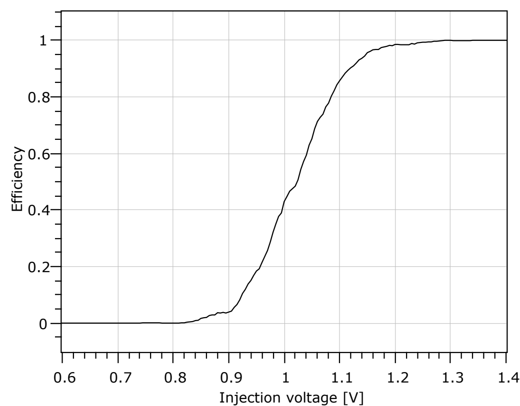


(a) The measured S-curve shows efficiency as a function of injection voltage.

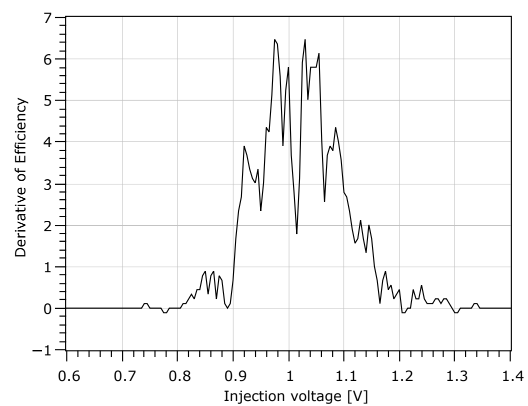


(b) The derivative of the S-curve on the left.

Figure A.5: The result with $n = 2$.



(a) The measured S-curve shows efficiency as a function of injection voltage.



(b) The derivative of the S-curve on the left.

Figure A.6: $n = 3$ makes the outcome quite smooth.

B Irradiation

B.1 Proton-Irradiation

Proton irradiation is used to cause bulk damage in detector chips. The protons are accelerated in a cyclotron to an energy of 23 MeV and are then lead onto the target. The proton current is about 2 μA. However proton irradiation causes also a big ionizing

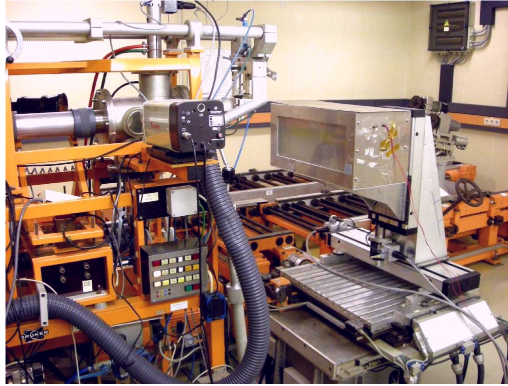


Figure B.7: The cyclotron setup for proton irradiation at KIT. (photo [27])

dose. We applied a dose of $2 \cdot 10^{15} \mathrm{n_{eq}/cm^2}$, which caused an additional ionizing dose of approximately of 1.5 MGy (the maximum ionizing dose willingly applied to a chip was 600 kGy!).

The cyclotron is operated by the private company ZAG Zyklotron AG on the premises of KIT.

B.2 X-ray Irradiation

X-rays are needed in the experiments described in this thesis for both signal source and evaluation of the effect of high ionizing doses on detector chips.

X-rays are emitted by nuclear decays, an example is the decay of ^{55}Fe (cf. chapter 3.3). For irradiation experiments such sources have not a sufficient decay rate. Further the emitted radiation can not be focused. Another disadvantage is that they can not be switched off, which makes it dangerous to work with radioactive sources.

The better option is an X-ray-tube. The Institute of Experimental Nuclear Physics (IEKP) at KIT owns an X-ray irradiation setup. Fig. B.8 shows the configuration of the X-ray-tube

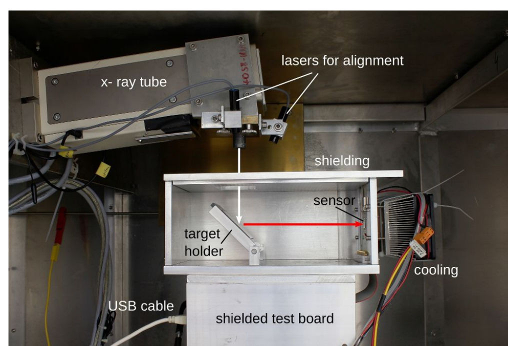


Figure B.8: The X-ray setup for irradiation and calibration. The shown configuration has been used for calibration. The different targets are placed in the target holder, while the detector chip is located on the right. For irradiation the target holder is replaced with the chip to be irradiated. (photo [27])

for calibration.
For irradiation, the box with the target holder is removed and the chip can be placed below for direct illumination.
Either way the accelerating voltage is set to 60 kV, with the X-rays having a most probable energy of 35 keV. During irradiation the electron current is set to 30 mA for a fast finish. An hourly dose of 10 kGy can be applied. Calibration requires a current of about 10 mA, which results in a handy hit-rate.
The beam spot's diameter is about 6 – 30 mm wide, depending on how far the target is located from the X-ray tube.

C Main Sources of Noise

The most important forms of noise in electronics are shot noise, thermal noise and 1/f-noise [28]. In comparison to shot and thermal noise, 1/f-noise is expected to be negligible for the systems described in this thesis.

C.1 Shot Noise

Shot noise appears whenever charge carriers cross a potential barrier. In case of a sensor this barrier is usually the depletion zone of the pixel diode. As charge carriers are discrete objects, there is a statistical probability for each charge carrier, independent from each other, to cross the barrier. The result is a modulation of the over all current [29]. The fluctuation in current is given by

$$\frac{\langle i^2 \rangle}{\Delta f} = 2eI. \tag{C.1}$$

Where $\langle i^2 \rangle$ is the squared current variance, Δf the bandwidth, e the elementary charge and I the mean current.

This source of noise is independent from the temperature. However the measured noise is highly dependent on the temperature, because the current I is a generation current $I(T)$ in a semiconductor (cf. Eq. (3.4)), which depends on the temperature.

The shot noise is Poisson-distributed:

$$F_\lambda(n) = e^{-\lambda} \sum_{k=0}^{n} \frac{\lambda^k}{k!} \tag{C.2}$$

With $\lambda > 0$ and $k = 0, 1, 2, \ldots$. This distribution is for many parameters similar to the Gaussian-distribution. For fitting to data points the Gaussian is much more handy. In this thesis always Gaussian fits were used to measure and evaluate noise.

C.2 Thermal Noise

Thermal or Johnson-Nyquist noise is generated by thermal agitation of charge carriers. This effect was discovered by John B. Johnson [30] and explained by Harry Nyquist [31]. The charge carriers, usually electrons, participate in the thermal movement of the atomic lattice. The resulting, measurable noise is mostly white noise. It can be characterized by a Gaussian-distribution with mean $\mu = 0$. The voltage variance measured on a resistor is given by

$$\frac{\langle u^2 \rangle}{\Delta f} = 4k_B T R. \tag{C.3}$$

Where $\langle u^2 \rangle$ is the squared voltage variance, Δf the bandwidth, T the Temperature and R the resistors resistance. This result can be used to obtain power

$$\frac{P}{\Delta f} = \frac{\langle u^2 \rangle}{R \Delta f} = 4k_B T \tag{C.4}$$

and current noise

$$\frac{\langle i^2 \rangle}{\Delta f} = \frac{4k_B T}{R}. \tag{C.5}$$

D Measurement and Source Units

The device information is extracted from the respective manuals.

D.1 Measurement Units

Keithley 6485 Picoammeter This device is used in all current measurements. The resolution is 10 fA or 5½ digit. Due to the high precision the current uncertainties are not shown in any diagrams.

Tektronix TDS 5104B This oscilloscope (5 GHz bandwidth and 5 GS/s sampling rate) was used in making all histograms, voltage measurements and some timing measurements. DC vertical gain accuracy is given as 1.5%.

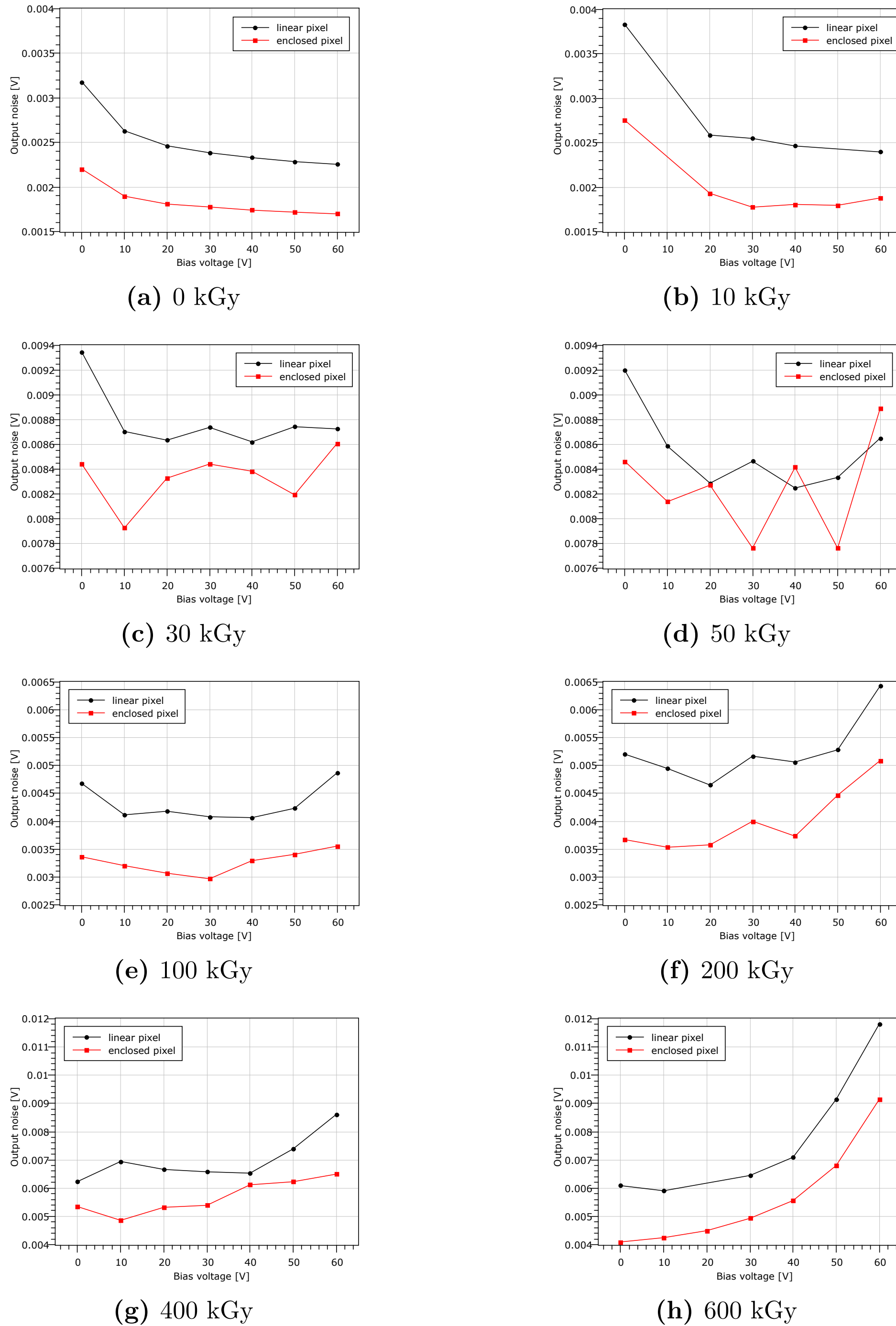
D.2 Source Units

HAMEG 7044 Most supply voltages were generated by one of the four outputs of this unit. The uncertainty of each output line is 10 mV or 1 mA.

Keithley 2410 High-Voltage SourceMeter This device was used as high voltage source, the bias voltage. For precise bias current measurement the Keithley 6485 was used.

E Bias dependant Noise

Additional noise measurements on the HVStripV1 chip as a function of dose and bias voltage or as a function of dose and annealing time. For additional information and discussion see chapter 3.5.2.



(a) 0 kGy

(b) 10 kGy

(c) 30 kGy

(d) 50 kGy

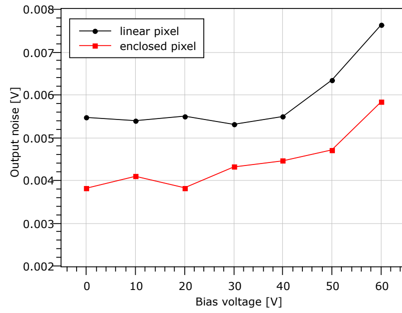
(e) 100 kGy

(f) 200 kGy

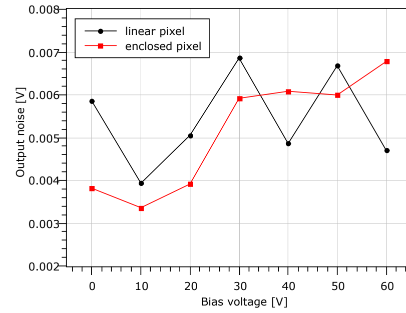
(g) 400 kGy

(h) 600 kGy

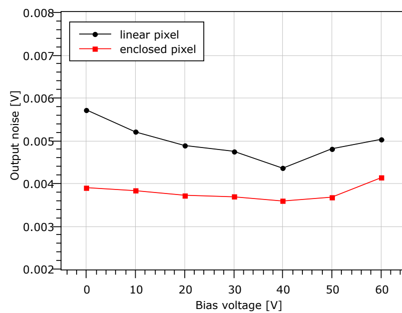
Figure E.9: Noise of HVStripV1 as a function of bias voltage after certain X-ray doses have been applied.



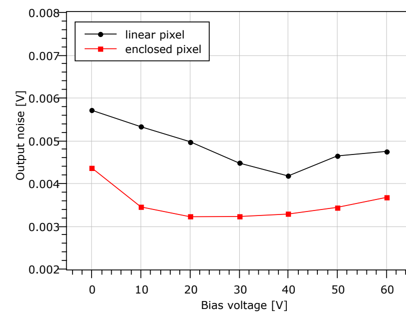
(a) 48h frozen



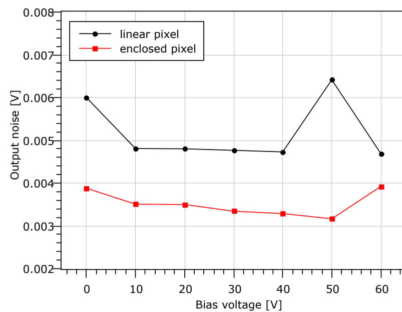
(b) 1 day of annealing



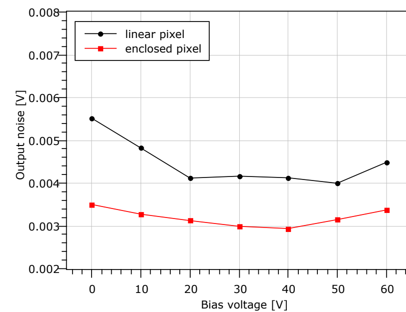
(c) 2 days of annealing



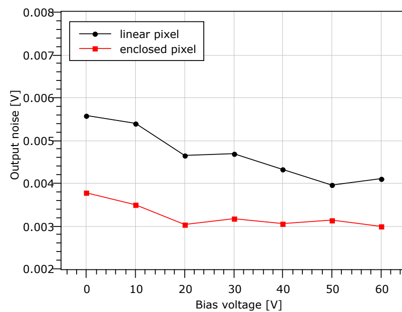
(d) 4 days of annealing



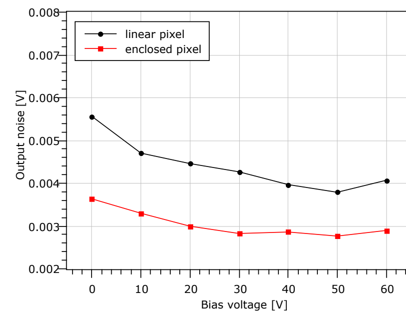
(e) 8 days of annealing



(f) 17 days of annealing



(g) 44 days of annealing



(h) 45 days of annealing, plus 30 minutes at 60°C

Figure E.10: Noise of HVStripV1 as a function of bias voltage after 600 kGy X-ray dose and a certain annealing time. The elapsed annealing time is given below each figure.

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