Multiple ink-jet printed zinc tin oxide layers with improved TFT performance

Benedikt Sykora,[1] Di Wang,[2] and Heinz von Seggern[1,a)]
[1] *Material Science Department, Technische Universität Darmstadt, Darmstadt 64287, Germany*
[2] *Institute of Nanotechnology and Karlsruhe Nano Micro Facility (KNMF), Karlsruhe Institute of Technology, Eggenstein Leopoldshafen 76344, Germany*

In the last two decades, metal-oxides, like zinc tin oxide (ZTO), are widely studied semiconductors for transistor applications. This study presents a simple, non-toxic, stable, and cost efficient precursor route for ZTO deposition by ink-jet printing. Such fabricated thin films are composed of an amorphous phase with embedded ZnO nanocrystals. The saturation mobility of ink-jet printed transistors increases from 0.05 $cm^2 V^{-1} s^{-1}$ for a single semiconducting layer to 7.8 $cm^2 V^{-1} s^{-1}$ for a transistor composed of 8 layers. This constitutes the highest saturation mobility of an ink-jet printed ZTO transistor reported so far. The devices exhibit large output currents (up to 38.7 mA) and high on/off ratios (exceeding 10^8). The large improvement in transistor performance with the number of layers is ascribed to an improved degree of substrate coverage confirmed by AFM investigations.

In 2004, Nomura *et al*. reported that In-Ga-Zn-O exhibits good transistor properties even if processed at room temperature.[1] This publication led to an increased interest in the scientific community to continue working on transparent conducting oxides (TCOs) for flexible electronics. The main drawback of such indium-based TCOs is the insufficient sustainability due to insufficient resources.[2] An alternative metal oxide is zinc tin oxide (ZTO), which has been widely studied as a possible semiconductor for field-effect transistor applications because of its preferential band transport.[3] Currently, ZTO films are processed by sputtering[4–7] or spin-casting techniques[8–11] which are both associated with a large material consumption. In contrast, the ink-jet printing process is more favorable because the ink is mainly supplied to the area of interest. No additional post processing like patterning with masks or photolithography is necessary, thereby leading to a reduction of potential production costs of 64%.[12] This implies that production waste can be minimized and the scale of the process can be increased.[13] Most of the TCOs possess an amorphous structure, thus avoiding electron scattering at grain boundaries during charge transport and the creation of trap states that is normally observed in polycrystalline films.[14] In contrast to the rigid sp^3 orbital system of silicon that is deteriorated from the crystalline to the amorphous phase, transition metal oxides show comparable Hall mobilities in the crystalline phase and the amorphous phase. This effect is due to the metal-oxygen-metal bonding between the large metal *s*-orbitals and the small oxygen *p*-orbitals, which is not extensively altered at the crystalline to amorphous transition.[1] Amorphous TCOs can also be easily adapted to a large scale production process by applying the knowledge of the a-Si:H technology.[2,12] ZTO based transistors have been introduced recently by ink-jet printing, reporting mobilities between 0.6 and 5.11 $cm^2 V^{-1} s^{-1}$.[15–17] Unfortunately, most of them use the widely applied but toxic 2-methoxyethanol as a solvent, which is not suitable for industrial production.

In the present letter, a precursor route using the non-toxic and cost efficient ethanol as a solvent is introduced which is similar to a route reported recently by Branquinho *et al*.[18] It will be shown that the repeated application[19] of the developed ink during ink-jet printing results in ZTO transistors with a mobility of up to 7.8 $cm^2 V^{-1} s^{-1}$ and a high on/off ratio exceeding 10^8. The reason for the improved transistor performance with increasing number of applied layers can be seen in the layer quality investigated by AFM analysis.

A precursor route to produce transparent, amorphous, and smooth ZTO layers was elaborated. The solution was produced by dissolving zinc nitrate hydrate ($Zn(NO_3)_2 \cdot x\ H_2O$) 99.999% and tin(II) chloride ($SnCl_2$) 99.99% both obtained from Sigma-Aldrich in 99.8% pure ethanol (Carl Roth). This solution exhibits precipitation, since the basidic tinchlorid is not stable under hydrophilic conditions.[20] To avoid the formation of tinhydroxidechlorid (Sn(OH)Cl), 1 vol. % hydrochloric acid (HCl) 34 wt. % (Merck) was added in order to oxidize the tin^{2+} to tin^{4+}. The complete oxidation of the tin ions was confirmed by a UPS analysis of the valence band onset. The corresponding result can be found in Figure S1 of the supplementary material.[21] This solution was then stirred for at least 14 h at room temperature. Before usage, it was filtered through a 0.2 μm polytetrafluoroethylene (PTFE)-filter in order to remove any residuals. The final precursor solution turns out to be stable for up to 12 months stored in ambient atmosphere. To build transistors, the precursor solution with a concentration of 0.1 mol/l was printed on prestructured and commercially available substrates from Fraunhofer IPMS (Dresden, Germany). The substrates consist of highly n-doped Si ($n \sim 3 \times 10^{17}\ cm^{-3}$) exhibiting a thickness of 675 μm and acting as the gate of the transistor, covered by a 90 nm thick thermally grown SiO_2 used as an gate insulator, followed by interdigitated source/drain electrodes composed of 10 nm of ITO as an anchor layer and 30 nm of Au. From the 16 prestructured transistors, only four with a channel length

a)Electronic mail: seggern@e mat.tu darmstadt.de

$L = 20\,\mu$m and a width of 10 mm ($W/L = 500$) were analyzed to avoid short channel effects. The substrates were cleaned by ultrasonication in acetone and propanediol for 15 min each. Subsequently, they were treated in an air plasma (70 W) for 60 s in a home made vacuum chamber in combination with the RF-generator PFG 300 RF by Trumpf Hüttinger GmbH & Co KG. For the ink-jet printing, a Dimatix DMP2831 desktop printer was used with the following settings: cartridge frequency 5 kHz, cartridge voltage 20 V, and cartridge head and stage temperature 20 °C. In this letter, the cartridges with 10 picoliters (pl) drop volume instead of 1 pl are used to achieve a faster processing of the predefined printing pattern. In addition, an optimized waveform for the above described ink of low viscosity was applied.[22] The printed films were annealed at a temperature of 500 °C on a preheated hot-plate in air for 10 min after each printing step. The electrical characterization was performed in a nitrogen filled glovebox. The *I-V* curves were measured with an Agilent 4155C semiconductor parameter analyzer. The saturation mobility μ_{sat} was extracted from the square root plot $\sqrt{I_D}$ (V_{GS}) of the transfer curve at a source-drain voltage of $V_{DS} = 30$ V utilizing the following equation:

$$\mu_{sat} = \frac{2L}{WC}\left[\frac{\partial I_D^{0.5}}{\partial V_{GS}}\right]^2, \quad (1)$$

where L and W represent the channel length and width, respectively, and C the areal capacitance. It is calculated by $C = \epsilon_0\epsilon_r d$ [1], where $\epsilon_r = 3.9$ for SiO_2 and d is the thickness of the dielectric layer which was 90 nm for all transistors in this publication. Cross section transmission electron microscopy (TEM) and grazing-incident X-ray diffraction (GIXRD) studies were performed using a FEI Talos F200X microscope at 200 kV and a Seifert PTS 3003 X-ray machine utilizing Cu K_α radiation, respectively. TEM and XRD studies were performed on thin printed ZTO films composed of 8 and four layers deposited onto Si/SiO_2 (90 nm) substrates.

The results of both measurements are displayed in Figure 1 and show an amorphous phase where nanocrystallites are embedded. The inset on the left side of Figure 1 indicates the GIXRD diffractogram obtained after a very long measurement time of 59 h. Apart from dominant peaks from the Si substrate and the glass holder, also four small peaks at 31.6°, 34.2°, 36.3°, and 38.2° can be detected in the enlarged section of the diffractogram (right inset). These peaks can be attributed to the (100), (002), and (101) diffraction peaks from ZnO reported at 31.9°, 34.4°, and 36.3° (Ref. 23) and the (200) diffraction peak of SnO_2.[24] From the enlarged section of one of the crystalline particles, the lattice spacing could be determined to be 0.28 nm. This value is in good agreement with the lattice spacing of the (100) planes of the hexagonal wurtzite structure of ZnO.[25,26] The GIXRD measurement of thin films composed of two, four, 8, and 12 printed ZTO layers can be found in Figure S2 of the supplementary material.[21] All diffractograms show a broad peak between 30° and 38° which includes the diffracted signal of the ZnO and the SnO_2 phase. Figure S3 of the supplementary material also shows the nanocrystalline structure of the printed and annealed ZTO solution.[21] In this case, the crystalline areas could be identified to be SnO_2. One possible explanation of the different crystalline phase could be that in this case a very thin film of one drop was analyzed.

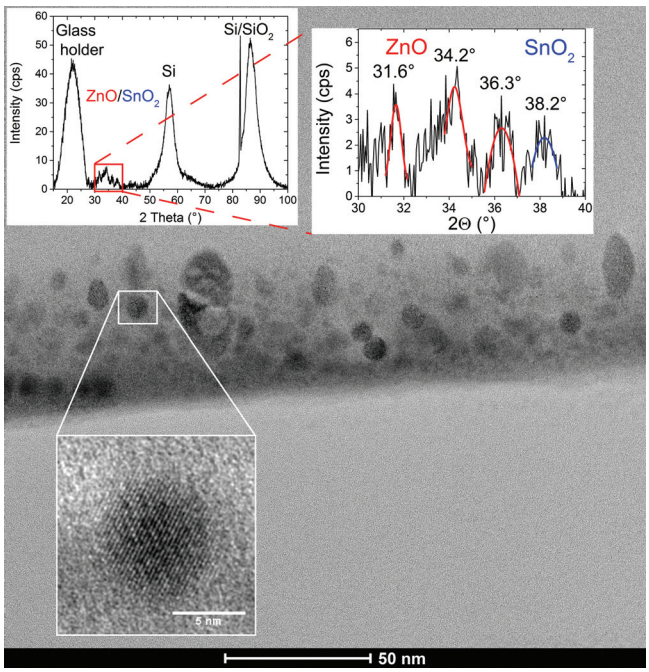

FIG. 1. Cross sectional TEM image of a printed ZTO film composed of 8 layers showing an amorphous phase with embedded nanocrystallites (one particle is enlarged). The insets show the GIXRD diffractogram of a thin printed ZTO film obtained after a grazing angle measurement under Ω 0.7° (left) and an enlarged section of it (right).

In order to investigate the electrical properties of such nanocrystalline films, field-effect transistors were processed whose layout is shown in the inset of Figure 2 displaying in addition typical results for five transistors with a different number of sequentially deposited ZTO layers. The transfer characteristics clearly demonstrate an improvement of the transistor properties with increasing number of ZTO layers. The better performance is visualized by the increasing amplitude and slope of the drain currents, the growing on/off ratio, and the decreasing hysteresis indicated by the decrease of the difference between forward and backward sweeps (arrows). All these indicate an improved functional layer with an

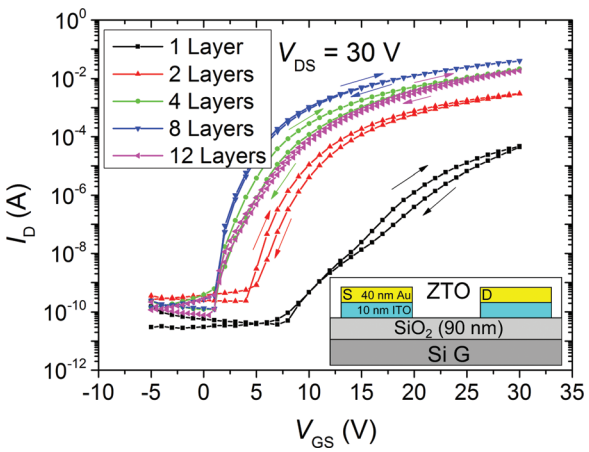

FIG. 2. Transfer curves of transistors based on increasing number of ZTO layers measured at a source drain voltage V_{DS} 30 V. The inset shows a sketch of the transistor layout.

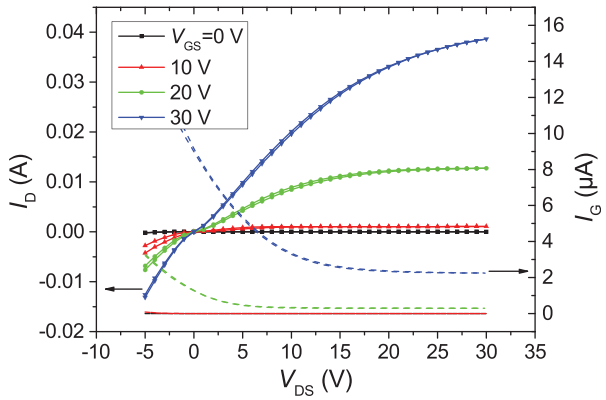

FIG. 3. Output characteristics of the transistor based on 8 ZTO layers measured at source gate voltages V_{GS} of 0, 10, 20, and 30 V. The solid lines display the drain currents I_D and the dashed lines the corresponding gate currents I_G.

increasing number of printed ZTO layers. The only drawback is the increasing off-current which demonstrates a higher conductivity of the channel which is due to the larger thickness and probably a better coverage of the SiO_2 channel area. The optimized transistor performance could be achieved for 8 layers. Printing of additional ZTO layers leads to a slight decrease in transistor performance which could be related to the additional heating steps following the 8th layer. We believe that after 8 layers, the additional application of ZTO does not improve the dielectric/semiconducting SiO_2/ZTO interface anymore and still present voids, and inhomogeneities may even deteriorate due to the additional heating.

Figure 3 displays the output characteristics of the transistor composed of 8 printed ZTO layers. The solid lines display the drain currents I_D and the dashed lines the corresponding gate currents I_G. It shows a clear gate modulation and saturation behavior. The large drain current of up to 38.7 mA at $V_{DS} = 30$ V and $V_{GS} = 30$ V can be attributed to the good ZTO film quality and the large W/L ratio. The contact resistance can be explained by the fact that via the printing process also the contact pads of the source and drain electrodes are covered with ZTO. The gate currents indicated by the dashed lines are about 20 000 times smaller than the corresponding drain currents. The output characteristics of the transistors if one, two, four, and 12 ZTO layers are applied can be found in Figures S4 S7 of the supplementary material.[21]

The extracted transistor properties are displayed in Table I which comprehends the thickness of the printed layers determined by profilometry (Bruker Dektak XT), saturation mobility (μ_{sat}), the threshold voltage (V_{th}), the subthreshold swing value (S.S.), and the ratio between the on/off current for one, two, four, 8 and, 12 layers of the printed semiconductor.

TABLE I. Layer thickness, saturation mobility (μ_{sat}), threshold voltage (V_{th}), subthreshold swing value (S.S.), and the on/off ratio (I_{on}/I_{off}) for transistors composed of one, two, four, 8, and 12 applied ZTO layers.

Number of layers	Thickness (nm)	μ_{sat} ($cm^2 V^{-1} s^{-1}$)	V_{th} (V)	S.S. (V/decade)	I_{on}/I_{off}
1	3	0.05	19.6	1.79	1.3×10^6
2	10	0.82	10.0	0.88	1.3×10^7
4	27	6.62	11.9	0.47	1.7×10^8
8	34	7.76	7.0	0.35	3.2×10^8
12	43	6.21	12.3	0.51	2.4×10^8

All reported values of Table I reveal that the single layer shows clearly inferior properties to those with multiple layers. The transistors exhibit current values I_D increasing by almost 3 orders of magnitude and mobilities μ_{sat} increase by a factor of 150 with the largest calculated value of 7.8 $cm^2 V^{-1} s^{-1}$ which is to the best of the author's knowledge the highest reported value for an ink-jet printed ZTO transistor. In addition, these transistors exhibit high on/off ratios I_{on}/I_{off} exceeding 10^8. The decreasing subthreshold swing value with increasing number of layers is also remarkable. The value of 350 mV/decade for the best transistor is still large compared to common values reported for inorganic MOSFETs of about 70 mV/decade and indicates the presence of trap states at the ZTO/SiO_2 interface. This interpretation can also be seen in the observed threshold voltage V_{th} which decreases from 19.6 V to 7.0 V comparing one layer with 8 layers. These values also indicate the presence of trap states even for the best transistors with 8 layers. This transistor shows the best performance because the application of another four layers leads to a decrease in mobility and on/off ratio and to an increase of the threshold voltage and the subthreshold swing value. This peak in the saturation mobility as a function of applied layers was already reported by Walker *et al.*[19]

In order to understand the morphology of the printed ZTO films, AFM images within the channel region of the corresponding transistors were taken using an Asylum research MFP-3D microscope and HQ:NSC19/AlBS tips. Figure 4(a) shows the morphology of a single layer. One can observe a grain-like structure with small agglomeration tendency. It can also be said that the film is not dense or the substrate coverage degree is small. This structure can explain the inferior transistor properties of the single layer device, because electrons face difficulties to find a conducting path between the source and drain electrode. This results in a rather small electron mobility of around 0.05 $cm^2 V^{-1} s^{-1}$. The corresponding rms roughness is 3.68 nm. This value can be attributed to the insufficient substrate coverage. Figure 4(b) shows the topography of the printed film with 8 layers. Whereas the rms roughness of 2.77 nm is still in the same order of magnitude than the single layer device, the substrate is, however, completely covered by ZTO. This indicates that the good coverage is most probably responsible for the high saturation mobility of up to 7.8 $cm^2 V^{-1} s^{-1}$ and also for the above discussed increased conductivity of the transistor channel. The small ring structure in Figure 4(a) is due to spilling of small drops during the printing process. The larger rings in Figure 4(b) occur because the hydrophilic ink is printed on the hydrophobic ZTO surface. Its hydrophobicity could be confirmed by contact angle measurements with a contact angle of 89°. The AFM images of the two, four, and 12 layers transistors can be found in Figure S8 of the supplementary material.[21] Figures S8(a) and S8(b) show an improved substrate coverage compared to the AFM image for a one layer device (Figure 4(a)) but the substrate is not completely covered with printed ZTO. The 12 layer image

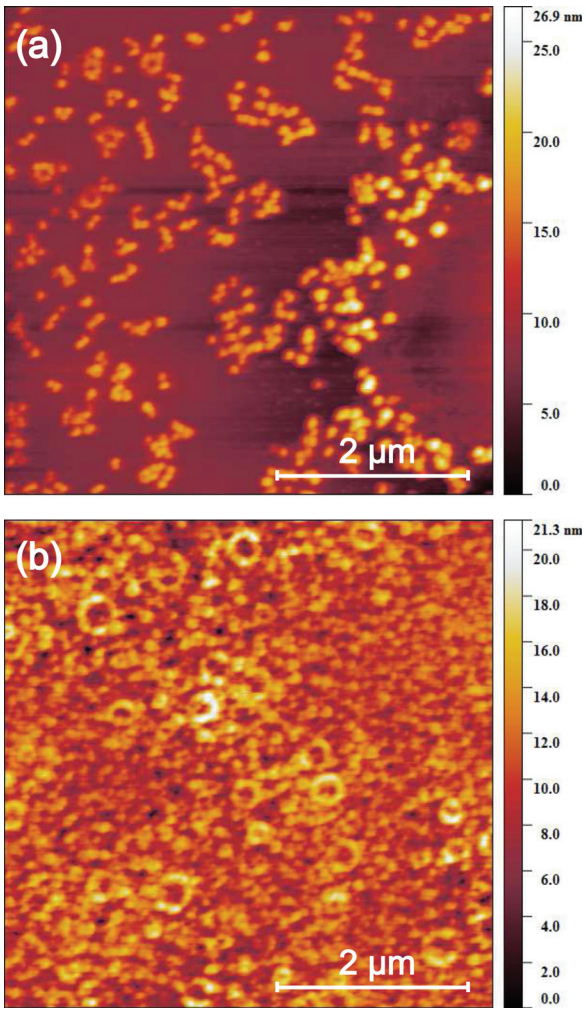

FIG. 4. AFM images of the printed ZTO for one (a) and 8 layers (b) recorded within the channel region of the corresponding transistors.

shows a complete substrate coverage but also a larger roughness compared to the film with 8 layers.

In summary, we have introduced a simple, non-toxic, stable, and cost efficient precursor route for the preparation of ZTO based transistors. Films of this semiconductor show an amorphous phase with embedded ZnO nanocrystallites, confirmed by TEM and GIXRD analysis. Field-effect transistors fabricated with multiple layers of ink-jet printed precursor solution reveal good device characteristics. The saturation mobility increases from $0.05\,cm^2\,V^{-1}\,s^{-1}$ for a single layer device to $7.8\,cm^2\,V^{-1}\,s^{-1}$ for a device composed of 8 layers which to the best of the author's knowledge is the highest saturation mobility reported for an ink-jet printed ZTO transistor. The decreasing threshold voltages combined with the decreasing subthreshold swing values as well as the increasing on/off ratios with increasing number of layers indicate a strong improvement of the ZTO layer quality as well as the channel coverage responsible for the transistor improvements. The reason for these improved transistor properties is confirmed by AFM results, indicating a drastically improved dielectric/semiconductor interface. These transistor properties and the low costs/toxicity of the developed precursor route could be an alternative to the toxic solvent and indium containing TCOs.

B.S. would like to thank Dr. Bonrad and Dr. Schwall of the Merck Lab at the Technische Universität Darmstadt for access to the Dimatix ink-jet printer and Joachim Brötz of the Technische Universtität Darmstadt for the XRD measurement. B.S. would further like to thank Subho Dasgupta from the Institute of Nanotechnology at Karlsruhe Institute of Technology for discussion of the results and Alla Sologubenko of the Laboratory for nanometallurgy and ScopeM of the ETH Zürich for FIB/TEM measurements. This work was funded by the Helmholtz Association through the Helmholtz Virtual Institute VI-530.

[1]K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, Nature **432**, 488 (2004).
[2]J. F. Wager, B. Yeh, R. L. Hoffmann, and D. A. Keszler, Curr. Opin. Solid State Mater. Sci. **18**, 53 (2014).
[3]C. G. Lee, B. Cobb, and A. Dodabalapur, Appl. Phys. Lett. **97**, 203505 (2010).
[4]D. L. Young, H. Moutinho, Y. Yan, and T. J. Coutts, J. Appl. Phys. **92**, 310 (2002).
[5]H. Q. Chiang, J. F. Wager, R. L. Hoffman, J. Jeong, and D. A. Keszler, Appl. Phys. Lett. **86**, 013503 (2005).
[6]J. S. Rajachidambaram, S. Sanghavi, P. Nachimuthu, V. Shutthanandan, T. Varga, B. Flynn, S. Thevuthasan, and G. S. Herman, J. Mater. Res. **27**, 2309 (2012).
[7]M. Fakhri, M. Theisen, A. Behrendt, P. Gorrn, and T. Riedl, Appl. Phys. Lett. **104**, 251603 (2014).
[8]S. J. Seo, C. G. Choi, Y. H. Hwang, and B. S. Bae, J. Phys. D: Appl. Phys. **42**, 035106 (2009).
[9]T. J. Ha and A. Dodabalapur, Appl. Phys. Lett. **102**, 123506 (2013).
[10]P. K. Nayak, M. N. Hedhili, D. Cha, and H. N. Alshareef, ACS Appl. Mater. Interfaces **5**, 3587 (2013).
[11]H. J. Jeon, K. B. Chung, and J. S. Park, J. Electroceram. **32**, 319 (2014).
[12]E. Fortunato, P. Barquinha, and R. Martins, Adv. Mater. **24**, 2945 (2012).
[13]M. Singh, H. M. Haverinen, P. Dhagat, and G. E. Jabbour, Adv. Mater. **22**, 673 (2010).
[14]T. Kamiya and H. Hosono, NPG Asia Mater. **2**, 15 (2010).
[15]D. Kim, Y. Jeong, K. Song, S. K. Park, G. Cao, and J. Moon, Langmuir **25**, 11149 (2009).
[16]Y. H. Kim, K. H. Kim, M. S. Oh, H. J. Kim, J. I. Han, M. K. Han, and S. K. Park, IEEE Electron Device Lett. **31**, 836 (2010).
[17]S. H. Lee and W. S. Choi, Electron. Mater. Lett. **10**, 737 (2014).
[18]R. Branquinho, D. Salgueiro, A. Santa, and A. Kiazadeh, Semicond. Sci. Technol. **30**, 24007 (2015).
[19]D. E. Walker, M. Major, M. B. Yazdi, A. Klyszcz, M. Haeming, K. Bonrad, C. Melzer, W. Donner, and H. V. Seggern, ACS Appl. Mater. Interfaces **4**, 6835 (2012).
[20]E. Riedel, *Anorganische Chemie*, 2nd ed. (Walter de Gruyter, Berlin, 1990), p. 504.
[21]See supplementary material at http://dx.doi.org/10.1063/1.4958701 for UPS, XRD, TEM, AFM thin film characterization and output characteristics, Supplementary material L 16 02693, Technische Universtitat Darmstadt, 2016.
[22]D. E. Walker, "Improving performance in metal oxide field effect transistors," PhD thesis, Technische Universtitat Darmstadt, 2013.
[23]S. Ong, C. Li, Y. Li, Y. Wu, and R. Loutfy, J. Am. Chem. Soc. **129**, 2750 (2007).
[24]D. F. Zhang, L. D. Sun, J. L. Yin, and C. H. Yan, Adv. Mater. **15**, 1022 (2003).
[25]P. Sharma, A. Gupta, K. V. Rao, F. J. Owens, R. Sharma, R. Ahuja, J. M. O. Guillen, B. Johansson, and G. A. Gehring, Nat. Mater. **2**, 673 (2003).
[26]H. Zhang, X. Ma, J. Xu, J. Niu, and D. Yang, Nanotechnology **14**, 423 (2003).