Karlsruhe Institute of Technology

Elektrotechnisches Institut (ETI)
Prof. Dr.-Ing. Michael Braun
Prof. Dr.-Ing. Martin Doppelbauer
Prof. Dr.-Ing. Marc Hiller
Kaiserstr.12. 76131 Karlsruhe

Elektrotechnisches Institut

Title:	Cell Design of a Square-Wave Powered 1AC-3AC Modular Multilevel Converter Low Voltage Prototype
Authors:	Mathias Schnarrenberger, Felix Kammerer, Dennis Bräckle, Michael Braun
Institute:	Karlsruhe Institute of Technology (KIT) Elektrotechnisches Institut (ETI)
Type:	Conference Proceedings
Published at:	Proceedings 2016 European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), Karlsruhe, Germany, 2016 Publisher: IEEE Year: 2016 ISBN: 978-9-0758-1524-5
Hyperlinks:	DOI: 10.1109/EPE.2016.7695373

Cell Design of a Square-Wave Powered 1AC-3AC Modular Multilevel Converter Low Voltage Prototype

Mathias Schnarrenberger, Felix Kammerer, Dennis Bräckle, Michael Braun
Karlsruhe Institute of Technology (KIT)
Elektrotechnisches Institut (ETI) - Electrical Drives and Power Electronics
Kaiserstr. 12, 76131 Karlsruhe, Germany
mathias.schnarrenberger@kit.edu, www.eti.kit.edu

Acknowledgments

The authors would like to thank the DFG (German Research Foundation) which finances this research project under grant BR 1780/11-1.

Keywords

≪Modular Multilevel Converter≫, ≪Design≫, ≪MOSFET≫, ≪Low Voltage Prototype≫

Abstract

This paper presents a novel design calculation scheme for low voltage Modular Multilevel Converters. One of the most important design values is to estimate the lifetime of the electrolytic cell capacitor. Therefore, a novel calculation method for the arm capacitor root mean square current is presented. Additionally, a new algorithm to estimate the power losses without a detailed simulation of the switching events is introduced. The results from these calculations are used to construct a low voltage Modular Multilevel Converter with 8 cells per arm.

Introduction

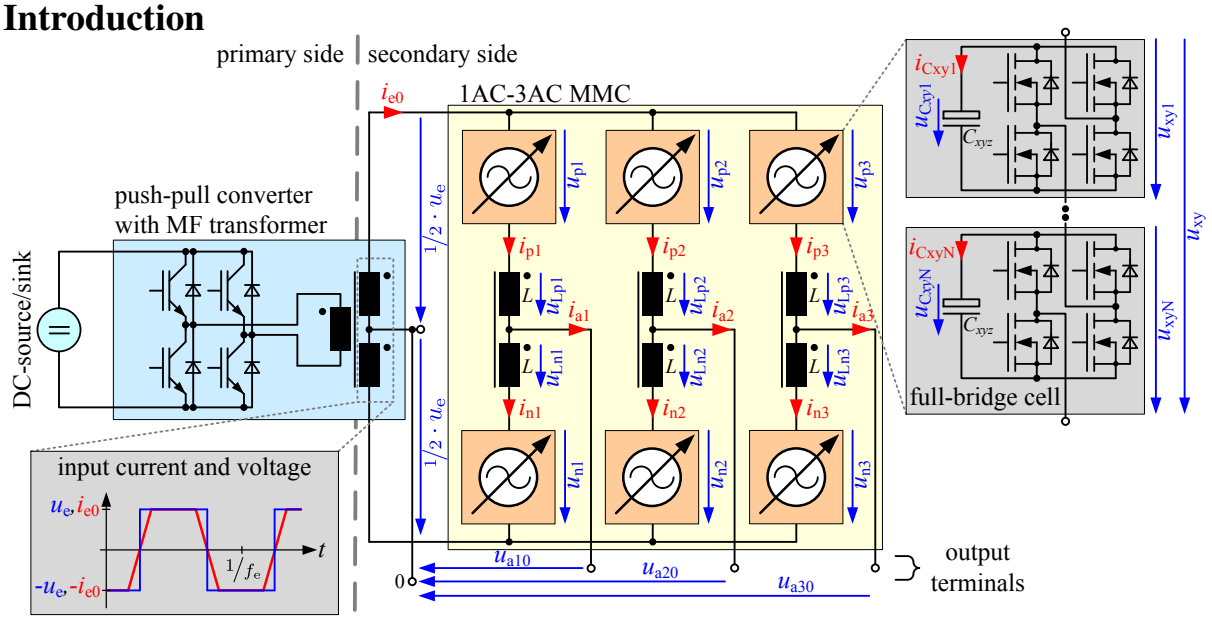


Fig. 1: Modular Multilevel Converter (MMC) with series connected full-bridge MMC cells fed by a push-pull converter [1]

Fig. 1 shows the square-wave powered 1AC-3AC Modular Multilevel Converter (MMC) [1]. This topology is used as a universal 3AC voltage source from 0 Hz up to 1 kHz and its applications are e.g. power

grid emulation [2] and Power Hardware-in-the-Loop emulation [2]. The MMC is fed by a push-pull converter with a square-wave voltage via a medium frequency (MF) transformer for galvanic isolation. The input current of the MMC is controlled in a trapezoidal manner to achieve zero current switching at the push-pull-converter. The MMC converts the power into a three phase output voltage with adjustable amplitude and frequency. The output voltage contains very low harmonics due to the multilevel topology and is well-suited for generating sinusoidal output voltages.

The core component of a square-wave powered 1AC-3AC Modular Multilevel Converter is a full-bridge cell (see Fig. 1). The cell for a low voltage prototype consists of the following power electronic parts: A cell capacitance implemented as an electrolytic capacitor and an H-bridge built with MOSFETs. The main task is to determine the capacitance and the root mean square (RMS) current of the cell capacitor to select the components. Furthermore, the currents and voltages of the MOSFETs must be determined to estimate the cooling effort. The referred values will be calculated in this paper over the complete output operating area.

In [3] the MMC for HVDC transmission is investigated regarding the arm energy variations with fixed voltages at the DC and AC side. For asymmetric grid voltages the arm energy variations are studied in [4]. For varying output voltages and phase angles the arm energy variations are calculated in [5]. In the literature, to the best knowledge of the author of this article, no RMS current of the cell capacitor for MMCs has been calculated. In [6] an average loss calculation for MMCs with a high cell number per arm is presented.

The fundamentals of the operation of the MMC are shown in Section 1. The calculation of relevant cell quantities is explained in Section 2. Comparison between calculation and simulation are presented in Section 3. Section 4 shows the designed cell and Section 5 summarizes the calculation scheme.

1 Fundamentals

The MMC consists of three phases [1]. Each phase has an upper arm p, a lower arm n and a coupled inductor L. Every arm consists of N series-connected cells (z = cell number, $z \in \{\mathbb{N} | 1 \leq z \leq N\}$). All cells contain an H-bridge with a cell capacitor C_{xyz} and can generate the voltages $0\,\mathrm{V}$, $+u_{\mathrm{C}xyz}$, $-u_{\mathrm{C}xyz}$ (upper or lower arm: $x \in \{p,n\}$, number of phase: $y \in \{1,2,3\}$). Every arm is able to generate a variable arm voltage u_{xy} within the following range utilizing pulse-width modulation (PWM):

$$-u_{\mathrm{C}xy} = -\sum_{z=1}^{N} u_{\mathrm{C}xyz} \leq u_{xy} \leq \sum_{z=1}^{N} u_{\mathrm{C}xyz} = u_{\mathrm{C}xy} \tag{1}$$

$u_{\mathrm{C}xy}$ is the arm capacitor voltage of the arm xy which equals the sum of all cell capacitors in this arm. Each arm capacitor voltage can be converted to a corresponding arm energy $w_{\mathrm{C}xy}$ using eq. (2)

$$w_{\mathrm{C}xy} = \frac{1}{2} C_{xy} \cdot u_{\mathrm{C}xy}^2 \tag{2}$$

$$w_{\mathrm{C}xy} = \bar{w}_{\mathrm{C}} + \tilde{w}_{\mathrm{C}xy} = \bar{w}_{\mathrm{C}} + \int p_{xy}\,\mathrm{d}t \tag{3}$$

with $C_{xy} = {}^{C_{xyz}}/_{N}$ as resulting arm capacitance. Since there are only capacitors and no power sources in each arm, the arm energy $w_{\mathrm{C}xy}$ can only be influenced by the arm power $p_{xy} = u_{xy} \cdot i_{xy}$. The arm energy $w_{\mathrm{C}xy}$ can be split according to eq. (3) into a constant average value $\bar{w}_{\mathrm{C}}$ and a time-dependent value $\tilde{w}_{\mathrm{C}xy}$. The average of p_{xy} must be zero to keep a constant average arm energy and, therefore, a constant arm capacitor voltage $u_{\mathrm{C}xy}$. For energy balancing a cascaded control system is implemented, see [1].

Each arm is described by its arm voltage u_{xy} and arm current i_{xy} because each arm is a two terminal network regarding the power connections. To perform the cell dimensioning the analytical expressions of the arm voltage u_{p1} and arm current i_{p1} for the upper arm in phase 1 are given:

$$u_{\mathrm{p1}} = \frac{\hat{u}_{\mathrm{e}}}{2} \cdot f_{\mathrm{S}} - u_{\mathrm{Lp1}} - u_{\mathrm{a1}} - u_{\mathrm{a0}} \tag{4}$$

$$i_{\mathrm{p1}} = \frac{\hat{i}_{\mathrm{e0}}}{3} \cdot f_{\mathrm{T}} + \frac{i_{\mathrm{a1}}}{2} + i_{\mathrm{e}\alpha} \cdot f_{\mathrm{T}} \tag{5}$$

$\hat{u}_{\mathrm{e}}$ represents the amplitude of the MMC input voltage, u_{Lp1} is the arm inductor voltage, u_{a1} is the output voltage of phase 1, u_{a0} is the output voltage zero component. $\hat{i}_{\mathrm{e0}}$ is the amplitude of the MMC input

current, i_{a1} is the output current of phase 1 and $i_{e\alpha}$ is an internal balancing current, see [1].

The function f_S defines a square wave with amplitude of 1 and the function f_T defines a trapezoidal wave with the amplitude of ξ_T, see Fig. 2. φ_T defines the duration for the current reversal and depends on the dynamic performance of the current control. ξ_T is a correction factor to compensate the transferred power due to the trapezoidal current and depends on φ_T, see [1]. $\gamma_e = 2\pi \cdot f_e \cdot t$ is the angle of the input voltage.

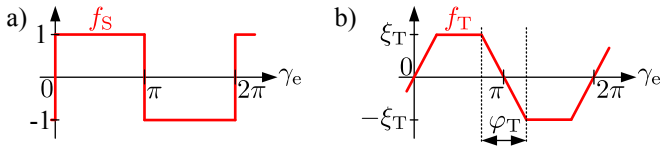


Fig. 2: Definition of f_S as a square wave (a) and f_T as a trapezoidal wave (b)

2 Cell Dimensioning

This Section presents a calculation method for designing cells for MMCs. First, the arm energy variation is calculated. This is the most essential quantity during the operation of the MMC because this specifies the amount of the arm capacitance that is needed for operation. Then the occurring arm capacitor RMS current is calculated which defines the lifetime of the capacitor. For power loss estimation in the switches the arm RMS current and a new calculation scheme for switching losses is given.

For the prototype the parameters in Table I are chosen. The parameters which define the cells are calculated over the complete output operating area, which means that $\hat{u}_a$, $\hat{i}_a$, φ_a and f_a are free to choose and independent from each other.

Table I: Parameters for prototype

Symbol	Value	Description
$\hat{u}_e$	700 V	input voltage
f_e	1.25 kHz	input frequency (square wave)
S_a	0 kVA .. 50 kVA	range of output apparent power
$\hat{u}_a$	0 V .. 325 V	range of output voltage amplitude
$\hat{i}_a$	0 A .. 102 A	range of output current amplitude
f_a	-1 kHz .. $+1$ kHz	range of output frequency
φ_a	$-\pi$ .. $+\pi$	range of angle between output voltage and current
φ_T	$\pi/2$	angle for current reversal
ξ_T	$4/3 = 1.\bar{3}$	correction factor for trapezoidal quantities

The following assumptions for the calculations are made: The resistor voltages are neglected, the output voltages and currents are sinusoidal and symmetric and no zero voltage component u_{a0} at the output is used. Additionally, a cascaded control system for energy balancing is assumed, see [1].

For cell dimensioning it is sufficient to consider only one arm of the six arms due to symmetrical reasons: First, the upper and lower arms are equally loaded due to the AC input voltage. Second, all three phases are identically loaded but displaced by 120°. Due to the cell balancing algorithm it is ensured that each cell in the arm is loaded equally and the calculations can be performed with arm quantities.

The output side for arm p1 is defined with the following equations:

$$u_{a1} = \hat{u}_a \cdot \cos(\gamma_a) \quad (6) \qquad i_{a1} = \hat{i}_a \cdot \cos(\gamma_a - \varphi_a) \quad (7) \qquad \gamma_a = 2\pi \cdot f_a \cdot t \quad (8)$$

$\hat{u}_a$ is the amplitude of the output voltage, $\hat{i}_a$ is the amplitude of the output current, γ_a is the angle of the output voltage and φ_a is the angle between the output voltage and output current.

Two different modes, a low frequency (LF) output mode and a high frequency (HF) output mode, must be distinguished depending on the output frequency. During low frequency output an additional internal balancing current $i_{e\alpha}$ is needed to limit the occurring arm energy variation of the second harmonic of the output frequency, see [1]:

$$i_{e\alpha} = \begin{cases} 0\,\mathrm{A} & |f_a| \gg 0\,\mathrm{Hz} \quad \text{high frequency (HF) output mode} \\ \frac{\hat{u}_a \cdot \hat{i}_a \cdot \cos(2\cdot\gamma_a - \varphi_a)}{2\cdot\hat{u}_e} & \text{otherwise} \quad \text{low frequency (LF) output mode} \end{cases} \tag{9}$$

The input current $\hat{i}_{e0}$ is chosen according to eq. (10) to maintain the overall energy balance of the MMC:

$$\hat{i}_{e0} = \frac{3}{2\cdot\hat{u}_e} \cdot \hat{u}_a \cdot \hat{i}_a \cdot \cos(\varphi_a) \tag{10}$$

The subsequent results are shown for full apparent power of the converter because this leads to the worst-case values of each design value.

2.1 Peak arm values

In this Section the peak arm current and voltage is calculated. These values represent the arm design parameters and are needed subsequently.

2.1.1 Peak arm current

The peak arm current $\hat{i}_{xy}$ is calculated according to eq. (11) by applying a worst case calculation with eq. (5), (9) and (10) during low frequency output mode and values from Table I:

$$\hat{i}_{xy} = \frac{\hat{i}_{e0}}{3} \cdot \hat{f}_T + \frac{\hat{i}_{a1}}{2} + \hat{i}_{e\alpha} \cdot \hat{f}_T = \frac{\hat{u}_a \cdot \hat{i}_a}{\hat{u}_e} \cdot \hat{f}_T + \frac{\hat{i}_{a1}}{2} = \frac{325\,\mathrm{V}\cdot 102\,\mathrm{A}}{700\,\mathrm{V}} \cdot \frac{4}{3} + \frac{102\,\mathrm{A}}{2} \approx 114\,\mathrm{A} \tag{11}$$

2.1.2 Peak arm voltage

In this Section the peak arm voltage $\hat{u}_{xy}$ is identified and the average arm capacitor voltage $\bar{u}_C$ is determined.

The peak arm voltage $\hat{u}_{xy}$ is calculated according to eq. (13) by applying a worst case calculation with eq. (4) and values from Table I. The peak inductor voltage $\hat{u}_{Lxy}$ is calculated using eq. (12) with $\hat{i}_\mu$ representing the coupled inductor maximum magnetizing current and T_r as time span to reach 0 A during input current reversal:

$$\hat{u}_{Lxy} = L \cdot \frac{\mathrm{d}\hat{i}_\mu}{\mathrm{d}T_r} \text{ with } \hat{i}_\mu = \frac{\hat{u}_a \cdot \hat{i}_a}{\hat{u}_e} \cdot \hat{f}_T \text{ and } T_r = \frac{\varphi_T}{4\pi} \cdot \frac{1}{f_e} \tag{12}$$

$$\hat{u}_{xy} = \frac{\hat{u}_e}{2} \cdot \hat{f}_S + \hat{u}_{Lxy} + \hat{u}_a + \hat{u}_{a0} = \frac{700\,\mathrm{V}}{2} \cdot 1 + 57\,\mathrm{V} + 325\,\mathrm{V} + 0\,\mathrm{V} = 732\,\mathrm{V} \tag{13}$$

The arm capacitor voltage u_{Cxy} must not fall below the peak arm voltage to ensure proper function of the converter. The average arm capacitor voltage $\bar{u}_C$ is set to 960 V due to a generic control reserve [1] and the arm voltage variation $\tilde{u}_{Cxy}$.

2.2 Arm Energy Variation

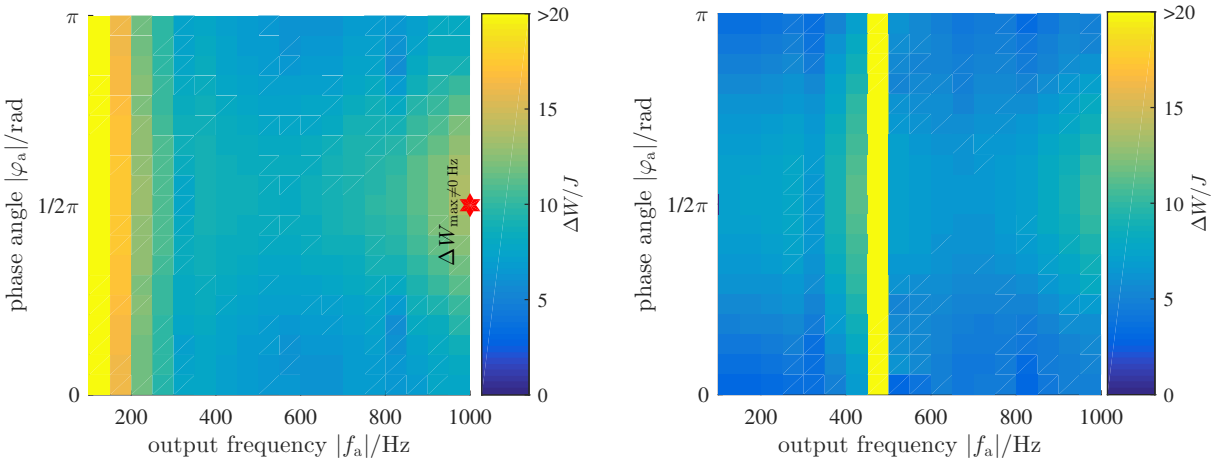
In this Section the maximum arm energy variation over the entire operating area is calculated using eq. (3). A numerical integration is used due to the discontinuities in f_S and f_T and, therefore, in the arm power p_{xy} (see. Fig. 2). The arm energy variation ΔW is defined as:

$$\Delta W = w_{Cxy,\max} - w_{Cxy,\min} \tag{14}$$

2.2.1 Output frequency unequal zero

The results for the arm energy variation with $\hat{u}_a = 325\,\mathrm{V}$ and $\hat{i}_a = 102\,\mathrm{A}$ are shown without (Fig. 3a) and with (Fig. 3b) additional balancing current. Without an internal balancing current an increase of

the arm energy variation ΔW is clearly seen for low output frequencies ($|f_a| < 300\,\text{Hz}$). In contrast, with an internal balancing current no significant increase for low output frequency occur but in the area of $|f_a| \approx f_e/3$ an increase of the arm energy variation is noticed. This occurs due to an active power component in the according arm with a singularity at $|f_a| = f_e/3$, see [7]. The highest arm energy variation of $\Delta W_{\text{max},\neq 0\,\text{Hz}} \approx 16\,\text{J}$ is reached at an output frequency of $f_a = 1\,\text{kHz}$ and an output phase angle of $\varphi_a = \pm\pi/2$ during high frequency output mode. This operating point can occur e. g. during the voltage recovery of a low voltage ride-through (LVRT) test.



(a) without internal balancing current $i_{e\alpha}$
high frequency output mode

(b) with internal balancing current $i_{e\alpha}$ (see eq. (9))
low frequency output mode

Fig. 3: Arm energy variation ΔW over output frequency f_a and phase angle φ_a with $\hat{u}_a = 325\,\text{V}$ and $\hat{i}_a = 102\,\text{A}$

2.2.2 Output frequency zero

Fig. 4 shows the arm energy variation at standstill with $f_a = 0\,\text{Hz}$, $\hat{u}_a = 325\,\text{V}$ and $\hat{i}_a = 102\,\text{A}$ depending on the output voltage angle γ_a and phase angle φ_a. The highest arm energy $\Delta W_{\text{max},0\text{Hz}} \approx 7.2\,\text{J}$ variation is observed if the output voltage of the phase is 0 V and the current is in its maximum: $\gamma_a = \pm\pi/2$ and $\varphi_a = \pm\pi/2$. The other extreme case is an arm energy variation of 0 J if the output current is 0 A in the according phase.

In this Section the maximum arm energy variation is calculated and the worst-case operating point is determined over the complete operating area of the square-wave powered MMC and occurs at the highest output frequency with a phase angle of $\pm\pi/2$. The overall worst case arm energy variation is set to $\Delta W_{\text{max}} = \Delta W_{\text{max},\neq 0\,\text{Hz}} \approx 16\,\text{J}$.

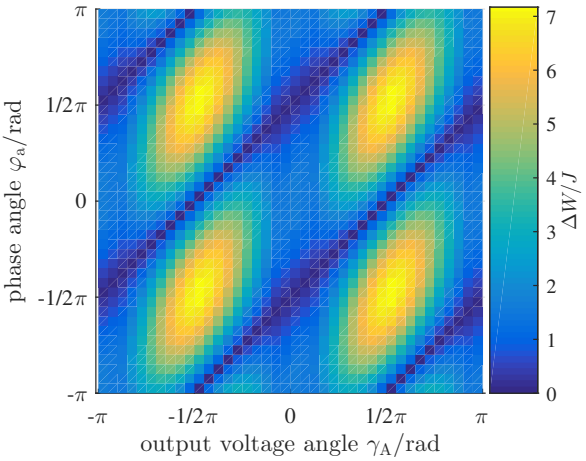


Fig. 4: Arm energy variation depending on the output voltage angle γ_a and phase angle φ_a at 0 Hz output frequency with $\hat{u}_a = 325\,\text{V}$ and $\hat{i}_a = 102\,\text{A}$

2.3 Arm capacitor RMS current

As shown in Table I the prototype will be used for low voltages. As stated in [8], the minimum foil thickness of polypropylene is $> 4\,\mu\text{m}$ and the dielectric strength of polypropylene is $> 100\,\text{kV}\,\text{mm}^{-1}$ which results in a dielectric strength $> 400\,\text{V}$ for the capacitors. Conversely, this means that low voltage capacitors have a high volume with respect to the capacitance. For this reason the prototype will be built

with electrolytic capacitors and, therefore, the root mean square (RMS)-current of the capacitor must be calculated to estimate its lifetime.

The RMS capacitor current for one cell is determined using the cell schematic, see Fig. 5a. The switches T1-T4 represent the H-bridge. u_{Cxyz} defines the cell capacitor voltage, i_{Cxyz} the cell capacitor current, i_{xy} the arm current and u_{xyz} the cell voltage at the power connections. To generate an arbitrary output voltage u_{xyz} a pulse-width modulation (PWM) is utilized which leads to the cell capacitor current i_{Cxyz} depending on the arm current i_{xy} and the duty cycle $d = \frac{t_{on}}{T_p} = \frac{|u_{xyz}|}{u_{Cxyz}}$, see Fig. 5b. The RMS current of the

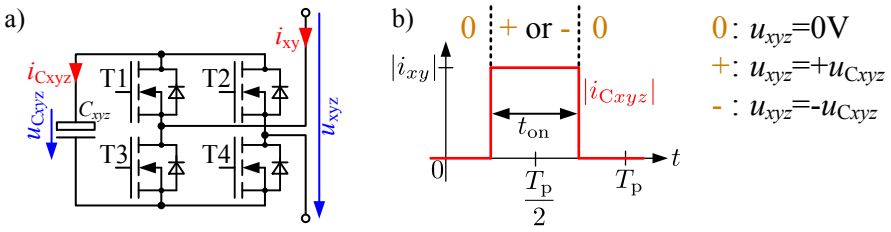


Fig. 5: a) Schematic of one cell, b) capacitor current i_{Cxyz} depending on duty cycle and arm current i_{xy}

cell capacitor during one switching period T_p is calculated according to eq. (15) assuming i_{xy} is constant during the switching period.

$$I_{Cxyz} = \sqrt{\frac{1}{T_p} \cdot \int_0^{T_p} i_{Cxyz}^2 \, dt} = \sqrt{\frac{1}{T_p} \cdot \int_{\frac{T_p - t_{on}}{2}}^{\frac{T_p + t_{on}}{2}} i_{xy}^2 \, dt} = \sqrt{i_{xy}^2 \cdot \frac{|u_{xyz}|}{u_{Cxyz}}} \tag{15}$$

The RMS capacitor current $\bar{I}_{Cxyz}$ over a complete output period T is determined using eq. (16)

$$\bar{I}_{Cxyz} = \sqrt{\frac{1}{T} \int_0^T I_{Cxyz}^2 \, dt} = \sqrt{\frac{1}{T} \cdot \int_0^T i_{xy}^2 \cdot \frac{|u_{xyz}|}{u_{Cxyz}} \, dt} \tag{16}$$

The transition from cell quantities to arm quantities can be conducted under the following two prerequisites: First, a cell balancing algorithm is used and second, all cells have an identical design. This prerequisites leads to a equally distributed cell capacitor burden, see [9]. The RMS current of the arm capacitor $\bar{I}_{Cxy}$ is then calculated according to eq. (17) with the output period T:

$$\bar{I}_{Cxy} = \sqrt{\frac{1}{T} \cdot \int_0^T i_{xy}^2 \cdot \frac{|u_{xy}|}{u_{Cxy}} \, dt} \approx \sqrt{\frac{1}{T} \cdot \frac{1}{\bar{u}_C} \cdot \int_0^T i_{xy}^2 \cdot |u_{xy}| \, dt} \tag{17}$$

Assuming that $\bar{w}_C \gg \tilde{w}_{xy}$ and, therefore, $\bar{u}_C \gg \tilde{u}_{Cxy}$ (see Section 4), the arm capacitor voltage variation can be neglected and eq. (17) is approximated.

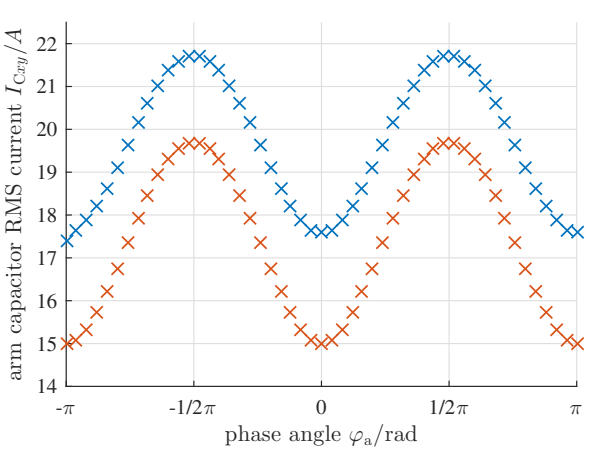
The resulting arm capacitor RMS currents are shown in Fig. 6. For an output frequency unequal zero the RMS current can be read from Fig. 6a with its maximum RMS current of $\approx 22\,\mathrm{A}$ if no balancing current is used and only reactive power is transferred. The overall maximum RMS current is $\approx 31\,\mathrm{A}$ during standstill (see Fig. 6b) at $\gamma_a = \pm\pi/2$ and $\varphi_a = \pm\pi/2$.

2.4 Arm RMS current

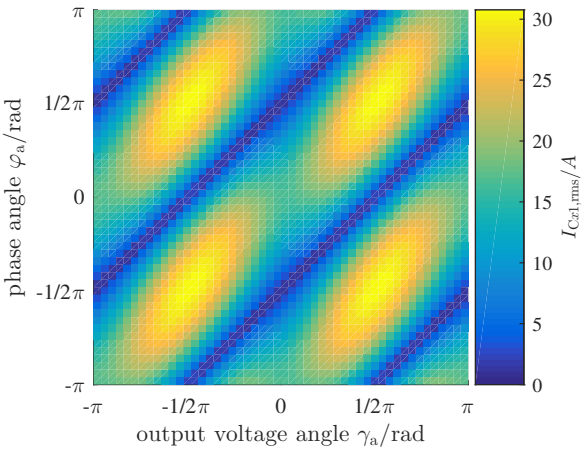
In this Section the arm RMS current is calculated which is needed to design the required cable cross-section, fuses and conduction losses. The arm RMS current i_{xy} is calculated according eq. (18):

$$I_{xy} = \sqrt{\frac{1}{T} \int_0^T i_{xy}^2 \, dt} \tag{18}$$

The resulting arm RMS currents are shown in Fig. 7. The maximum arm RMS current is $I_{xy,max} \approx 48\,\mathrm{A}$ and occurs at $f_a \neq 0\,\mathrm{Hz}$ and enabled balancing current, see Fig. 7a. During standstill the maximum arm



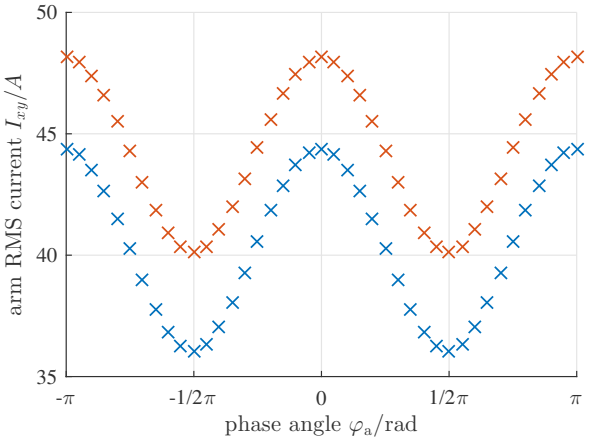
(a) arm capacitor RMS current depending on the phase angle. Results for no balancing current (blue) and with balancing current (red) is shown for $f_a \neq 0\,\text{Hz}$.



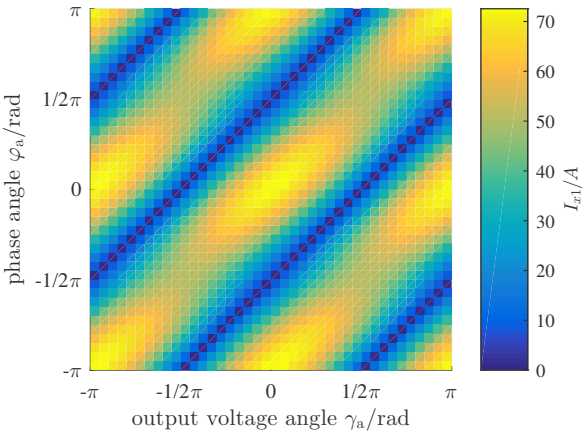
(b) arm capacitor RMS current depending on the output voltage angle and phase angle with balancing current for $f_a = 0\,\text{Hz}$.

Fig. 6: Arm capacitor RMS current with $\hat{u}_a = 325\,\text{V}$ and $\hat{i}_a = 102\,\text{A}$

RMS current rises up to $I_{x1,\max} \approx 72\,\text{A}$, see Fig. 7b.



(a) arm RMS current depending on the phase angle. Results for no balancing current (blue) and with balancing current (red) is shown for $f_a \neq 0\,\text{Hz}$.



(b) arm RMS current depending on the output voltage angle and phase angle with balancing current for $f_a = 0\,\text{Hz}$.

Fig. 7: Arm RMS current with $\hat{u}_a = 325\,\text{V}$ and $\hat{i}_a = 102\,\text{A}$

Comparing Fig. 6a and 7a it is clearly seen, that an additional internal balancing current leads to an increase of the arm RMS current but also to a decrease of the arm capacitor RMS current.

2.5 Cell losses

In this Section a calculation scheme for cell losses is given. The approach is separated into the calculation of conduction losses and switching losses. The results are used to estimate the cooling effort of the cell.

2.5.1 Conduction losses

Within this Section the occurring conduction losses in the cell is calculated. As this prototype will be used for low voltages, MOSFETs will be used as cell switches (see Fig. 5a). During steady state, only one MOSFET per half-bridge is switched on, e. g. either T1 or T3. During deadtime both MOSFETs in a half-bridge are off and the diode is conducting. This case is neglected because the deadtime is relatively short compared to the pulse period. For the calculation it is assumed, that always exactly one MOSFET per half-bridge is conducting. The conduction losses $P_{M,\text{cond}}$ are then calculated using eq. (19) with the

RMS drain current I_{D}^2 and the MOSFET dependent drain-source resistance $R_{\mathrm{DS,on}}$:

$$P_{\mathrm{M,cond}} = I_{\mathrm{D}}^2 \cdot R_{\mathrm{DS,on}} \tag{19}$$

Due to the series connection of the cells in each arm the drain RMS current I_{D} equals the arm RMS current I_{xy}.

2.5.2 Switching losses

This Section describes a novel switching loss calculation method for modular multilevel converter arms without the need for a switching model. To determine the switching losses, first the four different switching energies (MOSFET turn-on energy $E_{\mathrm{M,on}}(u_{\mathrm{DS}}, i_{\mathrm{D}})$, turn-off energy $E_{\mathrm{M,off}}(u_{\mathrm{DS}}, i_{\mathrm{D}})$, diode turn-on energy $E_{\mathrm{D,on}}(u_{\mathrm{DS}}, i_{\mathrm{D}})$ and turn-off energy $E_{\mathrm{D,off}}(u_{\mathrm{DS}}, i_{\mathrm{D}})$) must be calculated from the MOSFET datasheet values depending on the switch voltage u_{DS} and current i_{D}, see [10]. Due to the fact, that at each switching instance either a MOSFET is switched on and a diode is switched off or a diode is switched on and a MOSFET is switched off, the energies can be summarized to $E_1(u_{\mathrm{DS}}, i_{\mathrm{D}}) = E_{\mathrm{M,on}}(u_{\mathrm{DS}}, i_{\mathrm{D}}) + E_{\mathrm{D,off}}(u_{\mathrm{DS}}, i_{\mathrm{D}})$ and $E_2(u_{\mathrm{DS}}, i_{\mathrm{D}}) = E_{\mathrm{M,off}}(u_{\mathrm{DS}}, i_{\mathrm{D}}) + E_{\mathrm{D,on}}(u_{\mathrm{DS}}, i_{\mathrm{D}})$.

Each change of the cell output voltage leads to a switching energy, summarized in Table II. State describes the transition from the previous state to the new state: State 0 occurs if the switches T1 and T2 or T3 and T4 are switched on which leads to $u_{xyz} = 0\,\mathrm{V}$. State + occurs if the switches T1 and T4 are switched on which leads to $u_{xyz} = +u_{\mathrm{C}xyz}$. State − occurs if the switches T2 and T3 are switched on which leads to $u_{xyz} = -u_{\mathrm{C}xyz}$. The number of the occurring switching energy is shown in the columns E_1 and E_2 and, if applicable, a condition depending on the current sign.

Table II: Number of switching energy (E_1 and/or E_2) depending on the switch event and current sign

state	E_1	E_2	state	E_1	E_2	state	E_1	E_2
$0 \to 0$	0	0	$+ \to 0$	1; $i_{xy} > 0$	1; $i_{xy} < 0$	$- \to 0$	1; $i_{xy} < 0$	1; $i_{xy} > 0$
$0 \to +$	1; $i_{xy} < 0$	1; $i_{xy} > 0$	$+ \to +$	0	0	$- \to +$	2; $i_{xy} < 0$	2; $i_{xy} > 0$
$0 \to -$	1; $i_{xy} > 0$	1; $i_{xy} < 0$	$+ \to -$	2; $i_{xy} > 0$	2; $i_{xy} < 0$	$- \to -$	0	0

Table II is used in conjunction with the cell output voltage from the previous and the actual control period. To obtain the cell voltages, a complete modular multilevel converter arm must be considered due to the impact of the sorting algorithm. The sorting and selection algorithm is responsible for choosing the specific cells in a converter arm during each control period. As there are different types of sorting algorithms, for this consideration the algorithm presented in [9] is used: In case of a positive arm power the sorting algorithm selects the cells with the lowest voltage first and vice versa during each control period. This leads to a continuous balancing of the cell voltages per arm and obtains the best homogenization of the cell voltages but also the highest amount of switchings in each cell occurs. This leads to a worst-case estimation of the switching losses. The cell voltages for the sorting algorithm are provided by the cell model in eq. (20) with u_{xyz} as the cell output voltage, $\bar{w}_{\mathrm{C}xyz}$ as the average cell capacitor energy and C_{xyz} as the cell capacitance:

$$u_{\mathrm{C}xyz} = \sqrt{\frac{2}{C_{xyz}} \cdot \left(\int u_{xyz} \cdot i_{xy}\, \mathrm{d}t + \bar{w}_{\mathrm{C}xyz} \right)} \tag{20}$$

The selection algorithm then chooses the required number of cells depending on the output of the sorting algorithm and the arm voltage. $N-1$ cells are either completely switched off ($u_{xyz} = 0\,\mathrm{V}$) or on ($u_{xyz} = \pm u_{\mathrm{C}xyz}$). One cell generates an arbitrary output voltage utilizing a PWM. The overview of the arm model is shown in Fig. 8.

Using the set point cell voltage u_{xyz} from the previous and actual control period the occurring switching transitions in each control period are derived by using Table II and are converted into the switching energy by accumulating $E_{\mathrm{M,sw}} = E_1(u_{\mathrm{DS}}, i_{\mathrm{D}}) + E_2(u_{\mathrm{DS}}, i_{\mathrm{D}})$ over a complete output period T. The average power loss is then calculated with $P_{\mathrm{M,sw}} = {}^{E_{\mathrm{M,sw}}}/_{T}$.

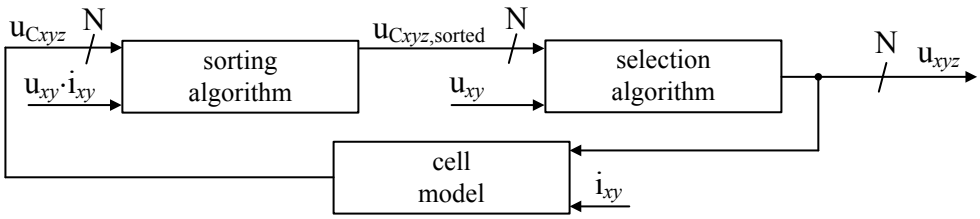
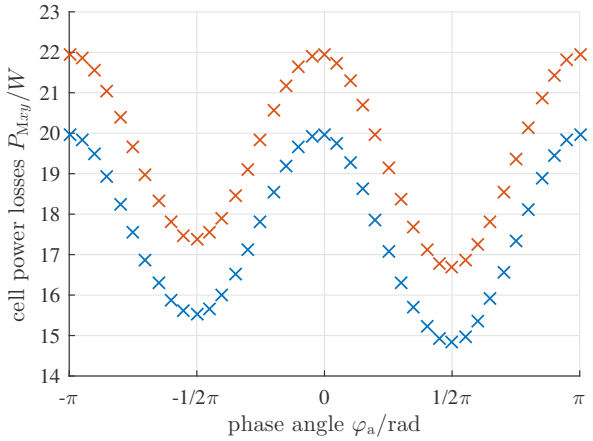


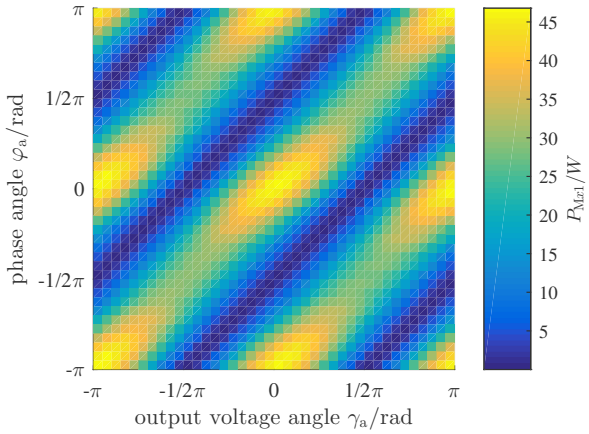
Fig. 8: Schematic of the sorting and selection algorithm including cell model

2.5.3 Results

In this Section the overall losses of one cell are shown. The MOSFET IPP075N15N3 G from Infineon [11] is chosen to calculate specific losses. Due to the peak arm current of $\hat{i}_{xy} \approx 114\,\mathrm{A}$, 2 MOSFETs are paralleled which leads to a total of 8 MOSFETs per cell. The results from the loss calculations are shown in Fig. 9. The losses for an operation with $f_a \neq 0\,\mathrm{Hz}$ are shown in Fig. 9a. It is observed that there are different losses for a capacitive respectively inductive load. The reason for this is that the switching losses are differently splitted between E_1 and E_2 depending on the phase angle φ_a. During standstill the overall highest loss of $\approx 47\,\mathrm{W}$ per cell occur.



(a) cell losses depending on the phase angle. Results for no balancing current (blue) and with balancing current (red) is shown for $f_a \neq 0\,\mathrm{Hz}$.



(b) cell losses depending on the output voltage angle and phase angle with balancing current for $f_a = 0\,\mathrm{Hz}$.

Fig. 9: Cell losses with $\hat{u}_a = 325\,\mathrm{V}$ and $\hat{i}_a = 102\,\mathrm{A}$

3 Simulation results

The prototype is under construction and, therefore, the calculations are compared with a simulation model built in MATLAB/SIMULINK, see [1]. The comparison is shown in Table III. The following operating points are chosen: Row 1 is the operating point at the highest arm energy variation during high frequency (HF) output mode. The operating point with the highest arm capacitor RMS current is depicted in row 2 and row 3 shows an ohmic load at European grid conditions during low frequency (LF) output mode.

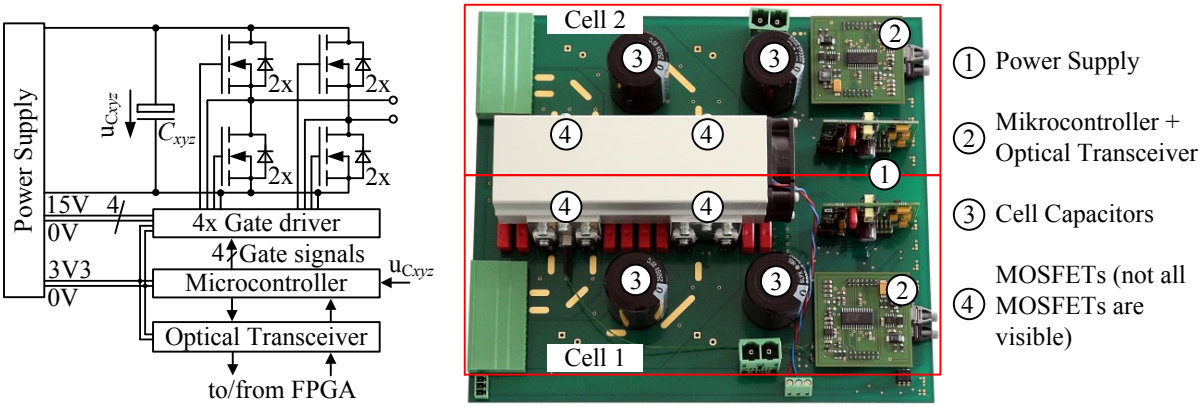
Table III: Comparison between calculation and simulation for selected operating points

Row	f_a or γ_a	$\hat{u}_a$	$\hat{i}_a$	φ_a	mode	ΔW calc.	ΔW sim.	I_{Cxy} calc.	I_{Cxy} sim.
1	$f_a = 1000\,\mathrm{Hz}$	325 V	102 A	$\pi/2$ rad	HF	16.1 J	16.8 J	21.8 A	21.7 A
2	$f_a = 0\,\mathrm{Hz}$; $\gamma_a = \pi/2$ rad	325 V	102 A	$\pi/2$ rad	LF	7.2 J	7.1 J	30.8 A	30.7 A
3	$f_a = 50\,\mathrm{Hz}$	325 V	102 A	0 rad	LF	3.1 J	3.1 J	15.0 A	15.1 A

Table III shows that the calculated and simulated results are well matched and only small deviations occur despite neglecting the arm inductances and arm resistances in the calculations.

4 Cell Design

The results from Section 2 were used to design the cell (see Fig. 10) for a low voltage MMC prototype according to Table I. The block diagram of one cell is shown in Fig. 10a. Each cell has a cell capacitance C_{xyz} and one H-bridge with MOSFETs. Each MOSFET is driven by a gate driver which in turn is controlled from a microcontroller per PWM. The microcontroller receives its set point voltage via an optical receiver from a FPGA and sends the actual cell voltage via an optical transmitter to a FPGA. The gate drivers, microcontroller and the optical transceivers are self-supplied from the cell capacitor using an isolated switching power supply.



(a) Block diagram of one cell

(b) Final PCB design with 2 cells per PCB

Fig. 10: Designed Cell

The most crucial parts of the cell design are the cell capacitors, MOSFETs and the cooling effort. Assuming that standstill is a rare operating point, the average of the arm capacitor RMS current is set to 20 A (see Fig. 6a, no balancing current). The selected cell capacitors SLPX222M200H9P3 (2200 µF, 200 V) have a lifetime of 3000 h at 45 °C ambient temperature and a RMS current of ≈ 9.5 A at 1 kHz [12]. For this reason, two capacitors are paralleled to reach a lifetime of ≈ 3000 h under full load. This results in a total of $C_{xyz} = 4400\,\mu\text{F}$ cell capacitance respectively to a resulting arm capacitance of $C_{xy} = 550\,\mu\text{F}$ with the number of cells per arm $N = 8$. This in turn results with $\Delta W_{\max} \approx 16\,\text{J}$ in a maximum arm voltage variation of $\tilde{u}_{Cxy,\max} \approx 15.3\,\text{V}$ at an average arm capacitor voltage of $\bar{u}_C = 960\,\text{V}$. This confirms the assumption of $\bar{u}_C \gg \tilde{u}_{Cxy}$ in Section 2.3. The results show that for a low voltage MMC cell it is crucial to consider the occurring arm capacitor RMS current rather than the arm energy variation if electrolytic capacitors are chosen. As MOSFETs IPP075N15N3 G from Infineon are chosen, see Section 2.5.3. As shown in Fig. 10b, 2 cells are assembled per PCB and the MOSFETs are sharing one heat sink. This leads to a worst-case total power loss of $\approx 94\,\text{W}$ which must be considered for the cooling design. As heat sink a LAM 5 K with 24 V fan from Fischer Elektronik (see [13]) with $\approx 0.3\,\text{K/W}$ is used which leads to a decent temperature rise of $\approx 28\,\text{K}$. The fan is temperature controlled and is supplied using an external power supply.

5 Conclusion

In this paper the calculation of the arm energy variation, arm capacitor root mean square (RMS) current and power losses in the MOSFETs are shown to design a cell for a low voltage Modular Multilevel Converter (MMC). The cell capacity is determined according the arm energy variation. To estimate the lifetime of the electrolytic cell capacitors of the low voltage MMC prototype a novel calculation method for the arm capacitor RMS current is introduced. The calculation show that it is necessary to pay extra attention to the arm capacitor RMS current to estimate the cell capacitor lifetime rather than only looking at the arm energy variation. The power losses to estimate the cooling effort are calculated

using a novel method without the need for a detailed simulation of the switching events. The planned applications, like a Power Hardware-in-the-Loop emulator, require a wide operating range with various output frequencies including standstill. For this, the results of the arm energy variation, arm capacitor RMS current and power losses are shown for full output apparent power of the square-wave powered 1AC-3AC MMC. The results were used to design a cell for the square-wave powered 1AC-3AC MMC low voltage prototype with 50 kVA output apparent power and an output frequency range from -1 kHz to $+1$ kHz.

References

[1] M. Schnarrenberger, F. Kammerer, M. Gommeringer, J. Kolb, and M. Braun, "Current control and energy balancing of a square-wave powered 1ac-3ac modular multilevel converter," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, Sept 2015, pp. 3607–3614.

[2] J. Kolb, F. Kammerer, A. Schmitt, M. Gommeringer, and M. Braun, "The modular multilevel converter as universal high-precision 3ac voltage source for power hardware-in-the-loop systems," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*, May 2014, pp. 1–8.

[3] K. Ilves, S. Norrga, L. Harnefors, and H.-P. Nee, "On energy storage requirements in modular multilevel converters," *Power Electronics, IEEE Transactions on*, vol. 29, no. 1, pp. 77–88, Jan 2014.

[4] M. Vasiladiotis, N. Cherix, D. Siemaszko, and A. Rufer, "Operation of modular multilevel converters under grid asymmetries," in *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, Nov 2013, pp. 6281–6286.

[5] H. Barnklau, A. Gensior, and S. Bernet, "Submodule capacitor dimensioning for modular multilevel converters," *Industry Applications, IEEE Transactions on*, vol. 50, no. 3, pp. 1915–1923, May 2014.

[6] T. Modeer, H. P. Nee, and S. Norrga, "Loss comparison of different sub-module implementations for modular multilevel converters in hvdc applications," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, Aug 2011, pp. 1–7.

[7] A. J. Korn, M. Winkelnkemper, P. Steimer, and J. W. Kolar, "Direct modular multi-level converter for gearless low-speed drives," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, Aug 2011, pp. 1–7.

[8] "Technical Infomarion Polypropylene," http://www.wima.com/EN/polypropylene.htm, accessed: 2015-11-01.

[9] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, vol. 3, June 2003, pp. 6 pp. Vol.3–.

[10] D. Graovac, M. Pürschel, and A. Kiep, *MOSFET Power Losses Calculation Using the Data-Sheet Parameters*, Infineon, 2006.

[11] "IPP075N15N3 G," http://www.infineon.com/dgdl/Infineon-IPP075N15N3_G-DS-v02_06-en.pdf?fileId=db3a30432313ff5e012399f743143bad, accessed: 2016-05-24.

[12] "Type SLPX 85 °C Snap-In Aluminum Electrolytic," http://www.cde.com/resources/catalogs/SLPX.pdf, accessed: 2015-11-01.

[13] "LAM 5 K," http://www.fischerelektronik.de/web_fischer/en_GB/heatsinks/D02/Miniature%20cooling%20aggregates/PG/LAM5K/search.xhtml, accessed: 2016-05-24.