

Sub-50 nm Channel Vertical Field-Effect Transistors using Conventional Ink-Jet Printing

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The rapid progress in printed electronics^[1–8] can be further accelerated by developing advanced architectures that may overcome fundamental limitations of the conventional printing techniques. At present, the performance of the printed field-effect transistors (FETs) and logic devices is severely impeded by the low printing resolution, which at best lies in the micrometer range.^[9,10] In contrast, here we demonstrate an alternative, fully printable vertical FET (vFET) geometry with ≤ 50 nm channel lengths. In our printed vFETs, this critical device dimension is not defined by the printing resolution, but determined by the thickness of a printed porous semiconductor layer that is sandwiched between the vertically stacked drive electrodes. Infiltration of the porous channel with a printable composite solid polymer electrolyte (CSPE)^[6,8,11,12] leads to fully 3D charge accumulation in the porous percolating semiconductor network and results in an unprecedented current density on the order of MA cm^{-2} , thereby paving the way for printed power transistors.

In silicon electronics, advancements in lithographic techniques have resulted in a continuous miniaturization of device dimensions, and this scaling process alone, without major material developments, has driven technological progress for decades.^[13] In contrast, intensive research efforts over the past years have produced a large number of solution-processable and high-performance semiconductors in printed electronics.^[1,2,6,8,14–19] As a result, the DC characteristics of printed FETs, be it organic or inorganic semiconductor based,

have long-time outperformed amorphous silicon. However, the resolution of the present printing techniques, being in the micrometer range, fundamentally limits the channel length and thereby device performance. In addition, typically encountered low intrinsic mobility of printed semiconductors requires devices with even larger channel widths to attain appreciable current output, thereby further increasing the device capacitance. This fundamental geometrical constraint has severely impeded the development of fully printed radio-frequency identification tags^[1] or light-emitting diode^[2] display backplanes.

Here we show a printed vertical transistor (vFET) that overcomes both of these fundamental limitations: we investigate a vertical channel geometry, which decouples the channel length from the printing resolution and permits printing of transistors with channel lengths of 50 nm or lower, more than two orders of magnitude lower than conventional printed FETs. The printable vFETs combine a porous semiconductor channel with 3D electrolyte gating mechanism. The solid polymer electrolyte used as a gate insulator exerts strong local fields throughout the interpenetrating channel/insulator geometry and accumulates charge carriers at every interface with the semiconductor material. This approach goes beyond prior investigations of vertical field-effect transistors,^[20–24] which either have reported a 90° rotation of the standard thin film transistor geometry,^[20–22] or achieved vertical electronic transport in vertically aligned nanowire transistors,^[23] or utilized a pseudo-vertical geometry, where one of the drive electrodes is prepared extremely thin so that the applied field can penetrate the metal electrode and polarize the semiconductor.^[24] While electronic transport is vertical in all of these devices, the semiconductor geometry is analogous to the classical thin film geometry, and they retain the general idea of an interface-controlled, 2D device. In contrast, in the present bulk vFET, not only the electronic transport is vertical, but also the current flow is fully 3D. Consequently, we observe a staggeringly high current density, almost reaching MA cm^{-2} level, which is at least two orders of magnitude higher than the highest reported current density during vertical transport (e.g., involving a polarization-transparent monolayer graphene electrode and MoS_2 semiconductor films),^[24] along with a large field-controllable current modulation of up to eight orders of magnitude (10^8).

A representative schematic showing the geometry of the vFET is presented in **Figure 1a–d**. The details of the device fabrication are described in the Experimental Section. We have used a metal–organic precursor ink, which transforms upon annealing into a mesoporous oxide semiconductor (here we have used SnO_2 ; see Movie S1 in the Supporting Information for details of the semiconductor morphology). The size of the

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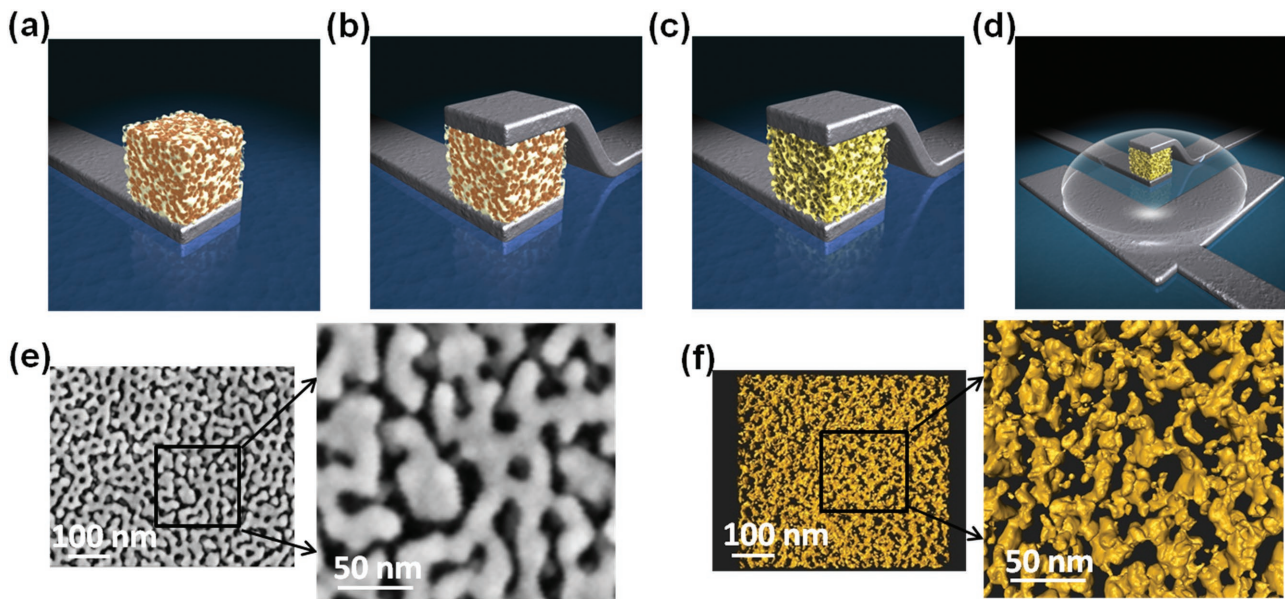


Figure 1. a) System comprising the bottom drive electrode along with the printed metal–organic precursor ink that would form the mesoporous semiconductor layer upon annealing. b) After structuring and placing the top drive electrode. c) After the annealing process that removes the polymer and opens the pores; the porous semiconductor channel layer is now sandwiched between the drive electrodes. d) The final vFET geometry after printing the polymer electrolyte (gate dielectric) that covers the porous channel and the displaced gate electrode. e) SEM image showing the actual porous SnO₂ surface morphology; the bright white phase represents the material and the dark regions show the pores. f) 3D surface rendering of the reconstructed STEM tomography showing the 3D structure of SnO₂. All the images were generated from the sample annealed at 550 °C for 5 min.

oxide ligaments/domains can be tailored either by the choice of the polymer or by varying the annealing routine (see Section III in the Supporting Information for details). This specially designed metal–organic precursor provides a mesoporous network with numerous current percolation paths, and the closely spaced ligaments offer sufficient strength to the structure to sustain the semi free-standing top metal electrode and avoid interelectrode electrical contact; simultaneously, the interconnected pores allow the printable dielectric (CSPE) to have sufficient access to the entire porous mesostructure.^[6–8,11]

The morphology of the printed and annealed semiconductor layer perpendicular to the current direction is shown in Figure 1e. The representative scanning electron microscopy (SEM) images reveal the surface morphology of the printed mesoporous semiconductor layer. The reconstructed and surface-rendered 3D scanning transmission electron microscopy (STEM) tomography of the printed layer shows near-identical feature sizes (Figure 1f). The partially interconnected oxide ligaments are 20–35 nm in width and the height of the printed layer is ≤ 50 nm (see Section V in the Supporting Information for details). Consequently, the vast majority of these semiconductor domains contribute to the vertical electronic transport. On the other hand, the pores are well-interconnected (Movie S2, Supporting Information), allowing the electrolyte to surround the SnO₂ domains completely.

The measured electrical characteristics of a typical vFET are shown in Figure 2. To ensure a low off-current (pA) and a high on–off ratio (10^8), the width of the drive electrodes is chosen to be 0.25 μm , resulting in an overlapping channel area of 0.25 $\mu\text{m} \times 0.25 \mu\text{m}$. For devices with a larger overlap area, the on–off ratio gets reduced to 10^5 (see Section VI in the Supporting Information). However, as shown in the next section,

the on–off ratio and saturated channel current ($I_{D,\text{sat}}$) are strong functions of the initial doping concentration of the semiconductor and can be controlled either by tuning the oxygen vacancies or by the selection of a suitable alternative material. Nonetheless, irrespective of the overlap area, the devices behave as typical accumulation-mode (threshold voltage, $V_T = 0.6$ V) metal oxide semiconductor FETs (MOSFETs) with an exceedingly high current density of 0.35 MA cm^{-2} . The calculated subthreshold swing turns out to be 121 mV per decade. An on-current pushing to MA cm^{-2} may be three to four orders of magnitude larger than any printed FETs reported till date.^[21,24] It is to be noted that the observed huge on-current is clearly the result of the device architecture, where about a thousand of semiconductor domains per square micrometer can be switched on with one applied gate voltage. Interestingly, despite tremendous current densities, we observe ideal MOSFET output characteristics with a clear current saturation (Figure 2b) and the classical quadratic relationship between the respective output currents at different V_{GS} . In addition, the accumulation layer thickness inside the semiconductor and the dielectric layer thickness at the semiconductor/electrolyte interface (which can be approximated as the thickness of the diffused double layer and is in the range of 1–2 nm; see discussion below)^[25] are rather small compared to the channel length of 50 nm. As a result, the gate field is always stronger than the drain–source field, and the gradual channel approximation holds; thus, no indication of short channel effect has been noticed.

In order to rationalize the performance of the present device architecture and to estimate the control of the electrical properties as a function of the device parameters, we have developed a computational model for the vFET device geometry that is subsequently used to compute the electrical device characteristics.

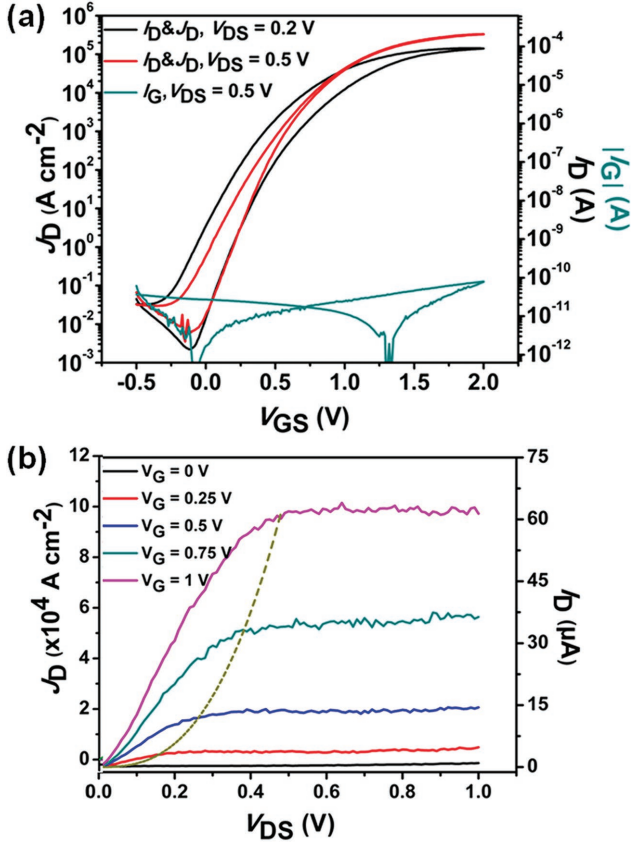


Figure 2. a) Transfer characteristics of a vFET showing a drain current density (J_D) approaching MA cm^{-2} level; the butterfly curve represents the leakage current. b) The corresponding output curves have been measured at different gate bias voltages (V_{GS}); the dashed line indicates the locus of the saturation drain current ($I_{D, sat}$) at different drain voltages (V_{DS}).

Next, we have performed Monte Carlo simulations to generate representative device morphologies with sub-nanometer resolution, which mimic the experimentally observed channel morphology shown in Figure 1e,f. We then performed drift-diffusion simulations of the electrical properties to quantitatively elucidate the impact of the overall channel geometry (overlap area), morphological aspects (ligament and pore size and their densities), and material aspects (doping concentration and carrier mobility of the chosen semiconductor) to model and optimize the FET characteristics.

The experimental and simulated transfer characteristics at $V_{DS} = 0.5 \text{ V}$ are shown in Figure 3a, which is described by a drift-diffusion model with a gate electrode work function $\Phi = 5.95 \text{ eV}$, where experimental values of $\Phi = 5.65 \text{ eV}$ have been reported.^[26] The doping concentration considered in the model is $n_0 = 5.4 \times 10^{18} \text{ cm}^{-3}$ which lies at the higher end of the previously reported values for SnO_2 ($1 \times 10^{17} - 1 \times 10^{19} \text{ cm}^{-3}$).^[27,28] The electron mobility $\mu_e = 3.0 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ is at the lower end of the experimentally determined range of $5 - 30 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$,^[28] due to the lack of order in the metal-organic ink derived extremely small nanocrystals. The effective dielectric constant of the electrolyte, $\epsilon = 4$, is about an order of magnitude smaller than the bulk value due to local microscopic effects.^[29,30] Using these values, the simulated current follows the experimental curve for nearly

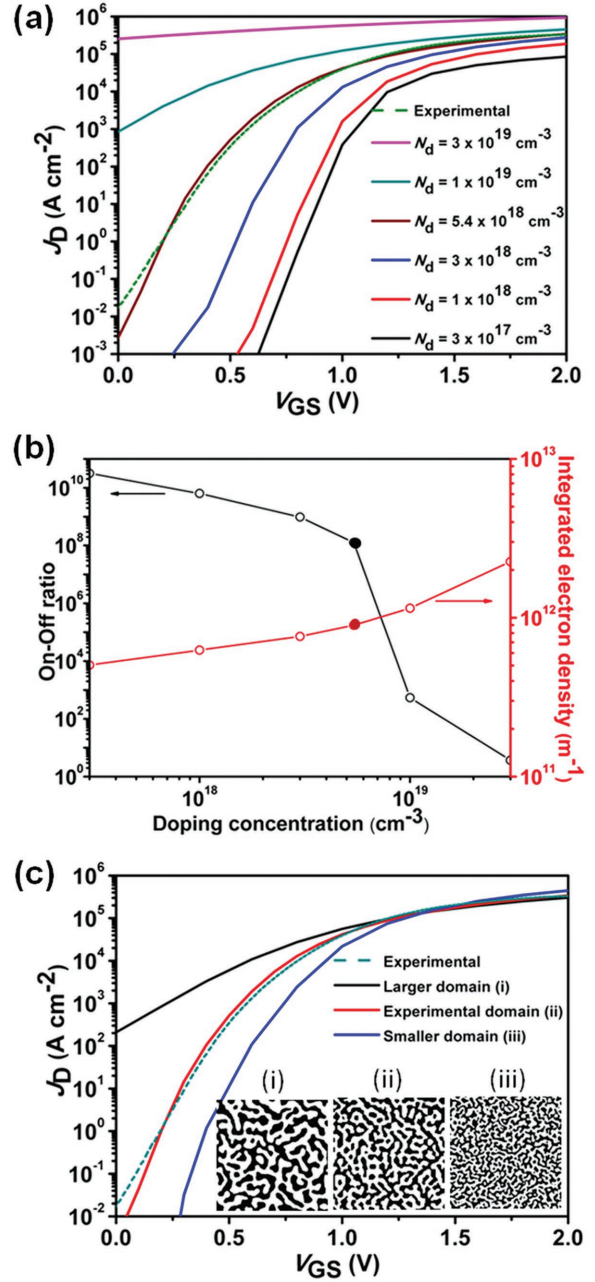


Figure 3. a) Modeled transfer characteristics (solid lines) as a function of the doping concentration show good agreement with the experimental data (dashed line) for $N_d = 5.4 \times 10^{18} \text{ cm}^{-3}$. All other parameters of the modeled curves are given in the text. b) On-off current ratio (black line) and integrated electron density (n) at a height of 25 nm (red line) as a function of the initial doping concentration, n_0 . The solid symbols represent the experimental values. c) The influence of morphology on transfer characteristics: smaller domains decrease the off-current and improve the on-off ratio, whereas larger domains increase the off-current and decrease the on-off ratio.

the entire range of the current modulation (approximately eight orders of magnitude). Thus, the chosen model describes all the relevant effects except the gate leakage, which may be responsible for the observed deviation at low gate voltages. As

shown in Figure 3b, the doping concentration of the chosen semiconductor can influence the on–off ratio; e.g., decreasing the doping concentration may further increase the already large value of 10^8 . The integrated electron density at a height of 25 nm increases as a superlinear function of the doping concentration, leading to a superlinear behavior of the on-current at higher gate voltages (Figure 3a at a gate voltage of 2 V).

Further optimization of the current density and the on–off ratio can be achieved by modulation of the doping concentration and the semiconductor–electrolyte interface area via the semiconductor domain size. The latter can be varied by the choice of the polymer used in the metal–organic precursor ink or by adjusting the annealing protocol accordingly. Figure 3c shows the dependence of the transfer characteristics on the semiconductor structure at a constant semiconductor volume. First, the smaller domain sizes result in larger interface areas between the semiconductor and the electrolyte, thereby increasing the fraction of the semiconductor volume that can be controlled by the gate bias and thus enhancing the on-currents. However, the off-current at zerogate is mainly determined by the intrinsic charge density of the bulk semiconductor. At the interface, the difference in work functions leads to a depletion of the charge carriers and an increase of the interface area enlarges the depletion volume and, therefore, reduces the off-current (Figure 3c).

Consequently, both the on-current and the on–off ratio can be improved by decreasing the domain size of the semiconductor material. However, it should be noted that at very small domain sizes, the cross-talk between the domains and the corrections to the drift-diffusion model may become relevant.

We find that the device will operate at an optimum efficiency when a surface charge double layer forms at every available semiconductor–electrolyte interface; i.e., interdomain cross-talking should be minimized. Therefore, the decay length of the diffused double layer at the semiconductor–electrolyte interface, which is a function of the ion concentration and the gate voltage, must be small compared to the distance between individual domains, which is governed by the pore size. To test the assumption of lack of cross-talking domains, first a 3D drift-diffusion model is used to obtain the local charge density in the semiconductor ligaments only (Figure 4a). Next, a typical semiconductor domain, as shown in Figure 4b, is modeled in a drift-diffusion/Poisson–Boltzmann simulation (see the Experimental Section for details) for the charge density in the semiconductor domain as well as in the electrolyte. Using the charge concentration in the semiconductor from the drift diffusion model (Figure 4a) we find a diffuse double-layer thickness in the electrolyte of 0.180 ± 0.006 nm (Figure 4c); within 1 nm from the interface, the concentration becomes numerically

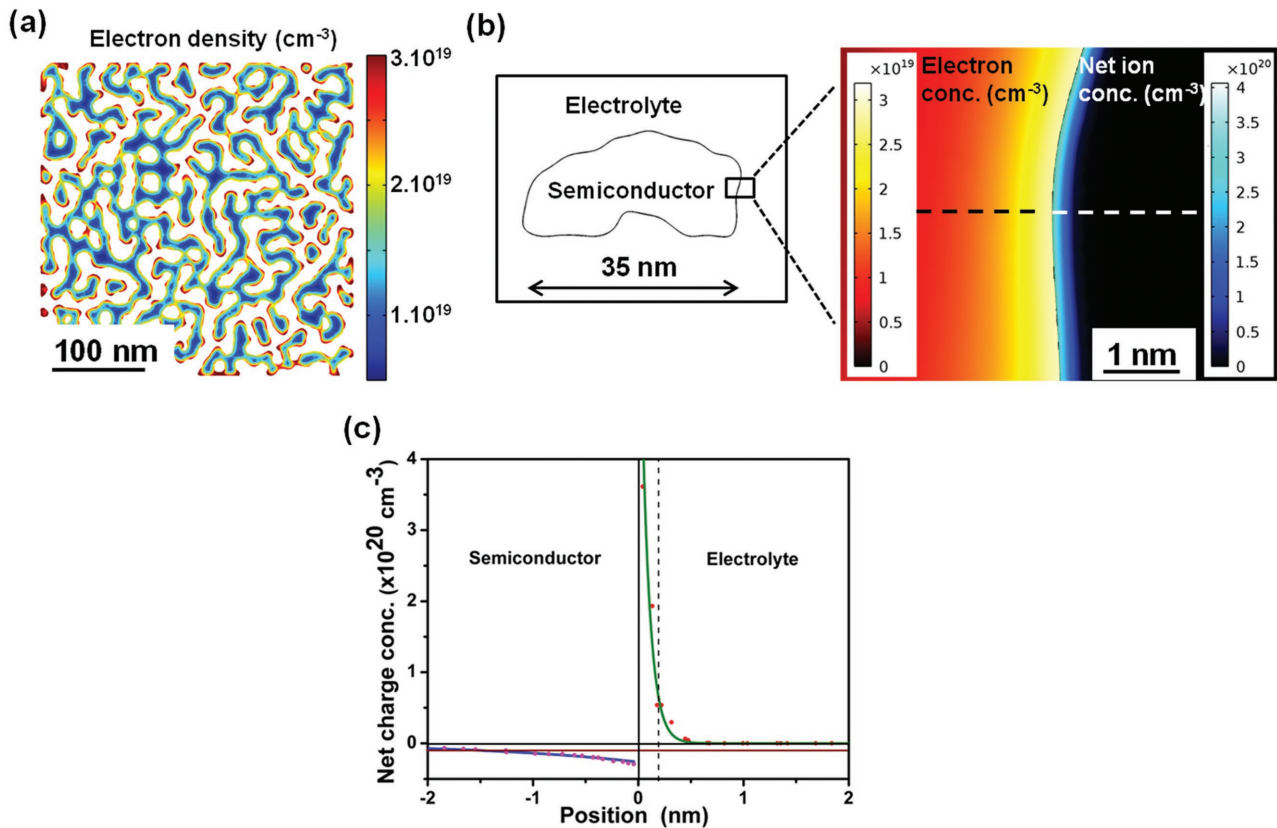


Figure 4. a) The modeled electron density distribution within the semiconductor at $V_{GS} = 2$ V and $V_{DS} = 0.5$ V. b) Schematic of a semiconductor domain and the surrounding electrolyte; the magnified section shows the net electron concentration in the semiconductor (left) and the net ionic concentration in the electrolyte (right). c) A cross-section through (b) is shown, where the solid points represent the results of simulation, on the simulation mesh, and the solid lines stand for the exponential fits. The decay length in the electrolyte is 0.180 ± 0.006 nm. The sign of the charge carrier concentration represents the sign of the respective majority carrier. The doping concentration in the semiconductor ($N_d = 5.4 \times 10^{18}$ cm⁻³) is plotted as a reference.

indistinguishable from the bulk value. As expected, the net charge in the semiconductor and electrolyte cancel each other out and we find a stable mean electron density at the electrolyte–semiconductor interface (Figure 4b). Because the Poisson–Boltzmann equation is a mean-field approach and neglects the explicit Pauli repulsion between the ions, the computed ion density at the electrolyte–semiconductor interface constitutes an upper bound of the decay length. Nevertheless, the simulations show that the charge distribution does not depend on the local curvature of the interface. Molecular dynamics simulations including explicit Pauli repulsion performed by Bourg and Sposito^[25] with a similar ion concentration also found that the ion concentration deviates from the bulk value no further than 1.5 nm from the interface. These distances are substantially smaller than the typical pore size of ≈ 15 –20 nm; consequently, one may expect no interference between the neighboring semiconductor domains and no suppression of the gating effect.

In summary, we have experimentally demonstrated and quantitatively modeled printable vFETs with channel lengths of less than 50 nm, which decouples the channel length from the printing resolution. The simulations permit extraction of key device parameters in agreement with complementing experimental data. Unlike traditional thin film field-effect devices, the 3D bulk-channel vFET geometry allows charge accumulation in bulk volume of the porous semiconductor materials, resulting in orders of magnitude higher saturated on-currents than typical printed FETs. Consequently, this device type may find novel applications beyond those conventionally considered for printed FETs, e.g., all-printed power electronics useful for balancing circuits associated with energy-storage devices. Moreover, because of the enormous surface area of its active component and a short distance of electronic transport, the printable vertical device architecture can be quite attractive for a range of novel devices, where an amplification of the output signal or an improved sensitivity toward various analytes is of interest, for example, ion-sensitive FETs, high precision sensors, and biosensors.

Experimental Section

Ink Preparation: A specially designed metal–organic precursor ink was developed to print the porous semiconductor layer that combines a selectively chosen polymer with typical metal oxide semiconductor precursors. The selected polymer with the formula $[(\text{CH}_2\text{CH}_2)_{0.67}(\text{CH}_2\text{CHCH}_2\text{CH}_3)_{0.33}]_{89}(\text{OCH}_2\text{CH}_2)_{79}\text{OH}$, known as poly(ethylene-co-butylene)-*block*-poly(ethylene oxide) (referred to as P(E/B)-*b*-PEO), was chosen because it forms a regularly ordered mesoporous nanostructure with average ligament and pore widths of 15–20 nm. The formation process of the oxide layer after printing, during the evaporation of the solvent, is closely related to the so-called evaporation-induced self-assembly process as described elsewhere. The polymer was prepared by the anionic polymerization of ethylene oxide using a “Kraton Liquid”-type ω -hydroxypoly(ethylene-co-butylene) precursor polymer as a macroinitiator as described elsewhere.^[31] For the printable ink, a homogeneous solution was first prepared by dissolving SnCl_4 (285.5 mg) and 75 mg of P(E/B)-*b*-PEO-polymer in (3.2 mL) of ethanol. Subsequently, after adding (0.3 mL) of water (to initiate the hydrolysis reaction) under stirring, the resulting mixture was aged for ≈ 24 h before being used for printing. The entire process was conducted under ambient conditions.^[32]

Characterization of the Printed Mesoporous Semiconductor Layer: A Dimatix 2831 ink-jet printer was used to print the semiconductor

layers for characterization and device fabrication. The height of the printed layers after the annealing steps was examined with a Dektak 6M stylus profilometer equipped with the N-Lite low-force package (Veeco) (see Section V in the Supporting Information). The surface morphology of the printed and annealed porous semiconductor layer was investigated with a Leo 1530 SEM. The metal–organic precursor ink was printed on precleaned Si/SiO₂ substrates, and different annealing routines were followed to optimize the preferred porosity and morphology. Transmission electron microscopy (TEM) characterization was performed using an aberration-corrected Titan 80–300 TEM (FEI Company) operated at an acceleration voltage of 300 kV and equipped with a US1000 slow scan charge-coupled device camera (Gatan) for TEM imaging and a high-angle annular dark field (HAADF) detector (Fischione) for STEM imaging. The tomographic analysis was performed in HAADF-STEM mode with a nominal beam diameter of 0.14 nm using the Xplore3D package (FEI Company). A series of STEM images were collected with one-degree steps over a tilt angle range of $\pm 60^\circ$ with a pixel size of 0.23 nm. The images were aligned by cross-correlation using IMOD V4.7 and reconstructed using 20 iterations of the simultaneous iterative reconstruction technique algorithm implemented in Inspect3D (FEI Company). The resulting image stack was de-noised using the nonlinear anisotropic diffusion implemented in IMOD and rebinned by a factor of two. The final data analysis was performed using Amira 5.6 (FEI Company) by manually segmenting the data stack. The resulting binarized volume was visualized by surface rendering and centerline tree analysis to reveal the pore connectivity. Additional material characterization is presented in Section IV in the Supporting Information.

Device Fabrication and Characterization: To create an accurately defined overlap region to facilitate precise parameter calculations, e-beam lithography was used to structure the drive electrodes (5 nm indium-tin-oxide/100 nm Pt). The metal–organic ink was printed on top of the bottom drive electrode (i.e., the source), and then the top drive electrode (drain) was structured. As the semiconductor channel area was not prestructured, the printed metal–organic ink actually got spread over a larger area than the cube-shaped form shown in Figure 1. As a result, the stray currents along the edges had to be considered. This has been calculated and presented in Section VII in the Supporting Information. After the top electrode was placed, the complete assembly was annealed at 550 °C for 5 min to oxidize the polymeric Sn-precursor and to open the pores. After the annealing step, the mesoporous semiconductor layer was ready to be infiltrated with our electrolytic dielectric; accordingly, as the last step of device fabrication, the CSPE was printed carefully on the porous channel while minimizing the overlap with the drive electrodes (to reduce parasitic capacitive currents). The synthesis procedure of the CSPE was explained in the previous publications.^[33,34] The electrical characterization was conducted using an Agilent 4156C semiconductor parameter analyzer and SüssMicroTec EP6 probe station. All the electrical measurements were performed under ambient conditions.

Morphology Generation for the Drift-Diffusion-Model Solver: To generate the 2D domain/ligament structure of the porous SnO₂ network, a Metropolis Monte-Carlo-based simulated annealing algorithm was used. The ratio of the semiconductor to the pore area, extracted from the STEM tomography, was used as an input for the simulation. The simulated annealing algorithm was based on the minimization of the interface area between the semiconductor and the pores. The cooling rate utilized in the simulated annealing process determined the final domain size of the mesoporous structure.

3D Drift-Diffusion Model: The 2D images generated by the Monte Carlo algorithm or directly extracted from the SEM images were extruded to a layer thickness of 50 nm to construct a 3D geometry, which was then used as the geometry for a numerical 3D drift-diffusion-model solver based on the semiconductor equations and the finite volume method (COMSOL 5.1). The upper and lower surfaces of the semiconducting particles were assumed to be connected to the electrodes through ohmic contacts.^[28] As the initial input, an n-type doping concentration of n_0 (bulk carrier concentration) and an electron mobility of μ_e were considered for the porous semiconductor channel region. The accumulation/current of

minority carriers (holes) is considered negligible for the gate and drain-source voltages applied in the study. The electrolyte was modeled as a thin (2 nm) insulator layer with a dielectric constant, ϵ ; the gate electrode was assigned a work function, Φ .

2D Drift-Diffusion Model Coupled to Poisson–Boltzmann Solver. To simulate the charge density in the electrolyte, the electrolyte was modeled by a Poisson–Boltzmann solver connected to the drift-diffusion model, which solves the electron density and the electric potential within the semiconductor. The electrolyte was connected to the gate electrode with a work function (Φ) from outside. Here, the electrolyte was simulated with a coupled Poisson–Boltzmann drift-diffusion model. Two types of singly charged ions (Li^+ and ClO_4^-) were assumed to be present in the electrolyte region at a concentration of 1 mol L^{-1} . A negative space charge density was assigned to the semiconductor domain and relaxed in the presence of positive ion density, which accumulated at the electrolyte–semiconductor interface. All the calculations were performed using COMSOL Version 5.1.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

T.T.B. and M.R. contributed equally to this work. The authors acknowledge financial support from the Helmholtz Association in the form of Helmholtz Virtual Institute VI-530.

- [1] A. Dodabalapur, *Mater. Today* **2006**, *9*, 24.
- [2] H. Sirringhaus, N. Tessler, R. H. Friend, *Science* **1998**, *280*, 1741.
- [3] B. W. An, K. Kim, H. Lee, S.-Y. Kim, Y. Shim, D.-Y. Lee, J. Y. Song, J.-U. Park, *Adv. Mater.* **2015**, *27*, 4322.
- [4] J.-U. Park, M. Hardy, S. J. Kang, K. Barton, K. Adair, D. k. Mukhopadhyay, C. Y. Lee, M. S. Strano, A. G. Alleyne, J. G. Georgiadis, P. M. Ferreira, J. A. Rogers, *Nat. Mater.* **2007**, *6*, 782.
- [5] P. Galliker, J. Schneider, H. Eghlidi, S. Kress, V. Sandoghdar, D. Poulidakos, *Nat. Commun.* **2012**, *3*, 890.
- [6] S. Dasgupta, R. Kruk, N. Mechau, H. Hahn, *ACS Nano* **2011**, *5*, 9628.
- [7] K. Hong, S. H. Kim, K. H. Lee, C. D. Frisbie, *Adv. Mater.* **2013**, *25*, 3413.
- [8] T. T. Baby, S. K. Garlapati, S. Dehm, M. Häming, R. Kruk, H. Hahn, S. Dasgupta, *ACS Nano* **2015**, *9*, 3075.
- [9] B. D. Gates, Q. Xu, M. Stewart, D. Ryan, C. G. Willson, G. M. Whitesides, *Chem. Rev.* **2005**, *105*, 1171.
- [10] M. Geissler, Y. Xia, *Adv. Mater.* **2004**, *16*, 1249.
- [11] S. K. Garlapati, T. T. Baby, S. Dehm, M. Hammad, V. S. Chakravadhanula, R. Kruk, H. Hahn, S. Dasgupta, *Small* **2015**, *11*, 3591.
- [12] L. Herlogsson, X. Crispin, S. Tierney, M. Berggren, *Adv. Mater.* **2011**, *23*, 4684.
- [13] G. E. Moore, *Electronics* **1965**, *38*, 114.
- [14] H. Sirringhaus, *Adv. Mater.* **2014**, *26*, 1319.
- [15] K. K. Banger, Y. Yamashita, K. Mori, R. L. Peterson, T. Leedham, J. Rickard, H. Sirringhaus, *Nat. Mater.* **2011**, *10*, 45.
- [16] W. J. Hyun, E. B. Secor, G. A. Rojas, M. C. Hersam, L. F. Francis, C. D. Frisbie, *Adv. Mater.* **2015**, *27*, 7058.
- [17] B. Kim, S. Jang, M. L. Geier, P. L. Prabhuram, M. C. Hersam, A. Dodabalapur, *Nano Lett.* **2014**, *14*, 3683.
- [18] M. P. Klinger, A. Fischer, F. Kaschura, R. Scholz, B. Lüsse, B. K. Boroujeni, F. Ellinger, D. Kasemann, K. Leo, *Adv. Mater.* **2015**, *27*, 7734.
- [19] T. Schmaltz, A. Y. Amin, A. Khassanov, T. M. Friedrichsen, H. G. Steinrück, A. Magerl, J. J. Segura, K. Voitchovsky, F. Stellacci, M. Halik, *Adv. Mater.* **2013**, *25*, 511.
- [20] D. E. Johnston, K. G. Yager, C. Y. Nam, B. M. Ocko, C. T. Black, *Nano Lett.* **2012**, *12*, 4181.
- [21] M. G. Lemaitre, E. P. Donoghue, M. A. McCarthy, B. Liu, S. Tongay, B. Gila, P. Kumar, R. K. Singh, B. R. Appleton, A. G. Rinzier, *ACS Nano* **2012**, *6*, 9095.
- [22] N. Stutzmann, R. H. Friend, H. Sirringhaus, *Science* **2003**, *299*, 1881.
- [23] L. Chen, W. Y. Fung, W. Lu, *Nano Lett.* **2013**, *13*, 5521.
- [24] W. J. Yu, Z. Li, H. Zhou, Y. Chen, Y. Wang, Y. Huang, X. Duan, *Nat. Mater.* **2013**, *12*, 246.
- [25] I. C. Bourg, G. Sposito, *J. Colloid Interface Sci.* **2011**, *360*, 701.
- [26] D. E. Eastman, *Phys. Rev. B* **1970**, *2*, 1.
- [27] D. F. Crabtree, R. N. S. M. Mehdi, D. A. Wright, *Br. J. Appl. Phys. (J. Phys. D: Appl. Phys.)* **1969**, *2*, 1503.
- [28] A. Oprea, E. Moretton, N. Bârsan, W. J. Becker, J. Wöllenstein, U. Weimar, *J. Appl. Phys.* **2006**, *100*, 033716.
- [29] L. J. Yang, X. Q. Yang, K. M. Huang, G. Z. Jia, H. Shang, *Int. J. Mol. Sci.* **2009**, *10*, 1261.
- [30] P. G. Dzhavakhidze, A. A. Kornyshev, A. Liebsch, M. Urbakh, *Phys. Rev. B* **1992**, *45*, 9339.
- [31] A. Thomas, H. Schlaad, B. Smarsly, M. Antonietti, *Langmuir* **2003**, *19*, 4455.
- [32] T. Brezesinski, A. Fischer, K. -i. Iimura, C. Sanchez, D. Grosso, M. Antonietti, B. M. Smarsly, *Adv. Funct. Mater.* **2006**, *16*, 1433.
- [33] S. Dasgupta, G. Stoesser, N. Schweikert, R. Hahn, S. Dehm, R. Kruk, H. Hahn, *Adv. Funct. Mater.* **2012**, *22*, 4909.
- [34] B. Nasr, D. Wang, R. Kruk, H. Rösner, H. Hahn, S. Dasgupta, *Adv. Funct. Mater.* **2013**, *23*, 1750.