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Direct Flux Linkage Control Scheme for Highly Utilized DC/DC Converters with Simple Interleaving Method

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***Abstract*—In this contribution, a control scheme for n-leg interleaved DC/DC converters is presented, allowing dead beat current control. Accurate average current control is ensured even for nonlinear filter components such as iron powder inductors or ferrite core inductors used near their saturation limit.**

Furthermore, the control scheme features a common measurement instant for all measured values. The effectiveness of the proposed control scheme is shown with a three leg bidirectional DC/DC converter.

I. Introduction

Many high power applications need bidirectional power flow between DC voltages of different magnitude. For applications like the adaption of battery voltages in electric vehicles or the connection of stationary energy storage systems to a common DC-link potential galvanic isolation is not necessary. In these cases interleaved DC/DC buck converters (Figure 1) are favorable due to a reduced filter expense [1], low output current ripple [2] and high efficiency [3]. With the interleaving, high current ripples per inductor are possible, which additionally enables very high dynamics of this converter type.

To utilize these advantages, a current control scheme is necessary, which enables high dynamic current control and accuracy. To reach these goals, many control schemes are presented in literature, e.g. *predictive control* [4], [5], *sliding mode control* [6], [7] or *evolution control* [8]. Further specialized control concepts like *projected cross point control* [9]–[11] or *synchronized zero crossing control* [12]–[15] are interesting solutions for DC/DC converters.

Still, most of these control schemes rely on constant inductivity of the used filter elements. As shown in this contribution, this is not always true, for example if iron powder inductors are chosen as filter elements or ferrite core inductors are operated near their saturation limit.

Even current control schemes like [16], [17], which are able to adapt for a varying inductance, are not necessarily applicable for high current ripples. These schemes make the assumption $\Delta i_\mathrm{k} = \Delta i_\mathrm{k+1}$, which is violated, if the current trajectory is no straight line segment.

To accomplish the objectives of high current quality and high control dynamics, this contribution presents a predictive direct flux linkage control method. This control scheme allows precise average current control, even if the used inductors show nonlinear behavior like saturation. This is an advantageous property for short overload conditions and allows space- and cost optimized design of filter inductors. The effectiveness of flux linkage control was presented before for electrical machines showing strong saturation effects [18] and for active front end converters utilizing iron powder inductors [19].

Furthermore, the implementation of an optimized interleaving scheme is described. It allows to take the necessary measurements in one common sampling instant per fundamental clock cycle, so the control algorithm is calculated only once per fundamental clock cycle even for n-leg converters, which allows simple integration in complex power electronic systems.

The paper is organized as follows: Section II introduces the necessary modeling for nonlinear inductors. In Section III the principle of direct flux linkage control for DC/DC converters is presented. Section IV describes the interleaving scheme. The prototype setup and measurements demonstrating the effectiveness of the control scheme are then presented in Section V and Section VI.

II. Modeling of Power Inductors

Figure 1 shows the hardware setup, that is reviewed in this contribution. It consists of n parallel half bridges, each one

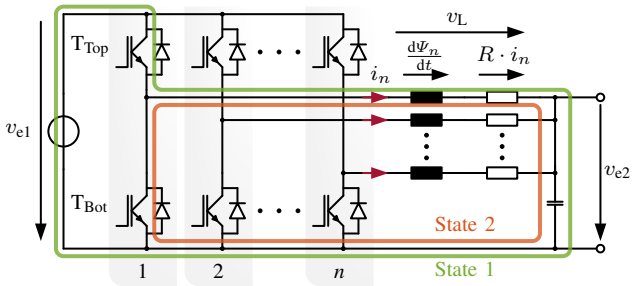


Figure 1. Schematic of the investigated DC/DC-converter. In green color, the path around the mesh for activated top switch and in orange the path for activated bottom switch is drawn.

connected to a single filter inductor and a common output capacitor. The input voltage is denoted with v_{e1}, whereas the output voltage across the common output capacitor is denoted with v_{e2}.

Without loss of generality, in this contribution only iron powder inductors and ferrite core inductors are reviewed, since both materials are widely used in DC/DC converters. Power inductors are assumed to be ideal and have a constant inductance for deduction of most control schemes. As stated earlier, this is not necessarily true. To investigate the characteristics of the two core materials, measurements with an iron powder core and a ferrite core inductor were carried out.

Figure 2 shows the measured flux linkage trajectory $\Psi(i)$ and the respective differential inductance $L_{\text{diff}} = {}^{\mathrm{d}\Psi(i)}/_{\mathrm{d}i}$ for the two prototype inductors used in the later presented measurements. Since the values of the two inductor types differ, the measurements are normalized to their rated values for easier comparison.

Even though a nonlinear connection of flux linkage Ψ and current i is not immediately visible for the measured iron powder inductor (marked with orange circles [—o—]), the differential inductance shows a significant constant decay, so no fixed inductance can be given for this kind of inductor. Therefore, current control schemes based on fixed inductance are likely to show inferior performance, when incorporating iron powder inductors in the hardware setup. Regarding Figure 2 iron powder inductors are especially interesting for high power applications, since they feature high differential inductance under large bias magnetization, which is the normal operation condition for DC/DC converters. Furthermore, iron powder inductors allow output currents exceeding their nominal current rating, since no sudden saturation occurs.

Regarding ferrite core inductors (marked with blue squares [—□—]) the differential inductance shows a constant range, indicating a linear relationship between flux linkage and current. Above this range, the ferrite core inductor shows a quick decay in differential inductance. Should this inductor type be utilized in this range, for example during short overload conditions, here too, a fixed inductance value can not be given.

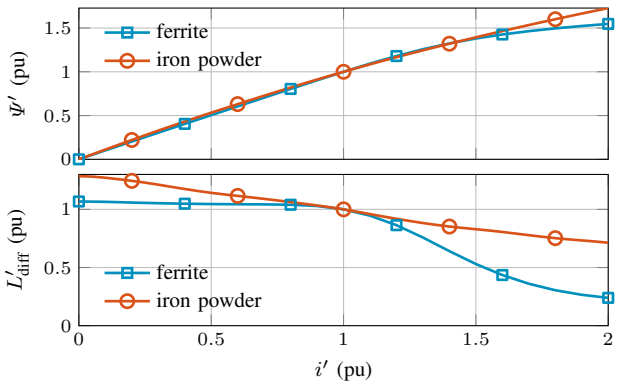


Figure 2. Measurements of flux linkage and differential inductance for iron powder core and ferrite core inductors. The measurements are normalized to their nominal values for easier comparison

Nevertheless, the properties of the inductors are fully characterized by the knowledge of $\Psi(i)$, and since for technically realized inductors every current value i can be assigned to a single-valued flux linkage Ψ, the inverse function $i(\Psi)$ exists. This correlation will be utilized in the next sections, to develop a current control scheme for nonlinear or highly utilized inductors.

III. Control Scheme

As introduced in the previous section, in general cases no fixed inductance value L can be given. Therefore, in this contribution the flux linkage Ψ is controlled in a direct manner. If the characteristics $\Psi(i)$ and $i(\Psi)$ are known, the output current of the converter is controlled implicitly by controlling the flux linkage.

Figure 3 shows a block diagram, representing the implementation of the control scheme for a single phase leg on a digital signal processor. The components of this block diagram are introduced and explained in the following sections. To derive the control scheme, only a single phase leg is regarded. The interleaving scheme is introduced in Section IV.

A. Simplifying assumptions

To derive the control scheme following simplifying assumptions are made:

- the voltages v_{e1} and v_{e2} remain constant during the prediction horizon of the control scheme
- the resistive voltage drop $R \cdot i$ is assumed to be constant during one clock cycle
- power switches are ideal
- characteristics of the power inductors are not temperature dependent

These assumptions can easily be made, because in common hardware setups, the capacitors used for filtering current ripples at the DC-link and at the output of the converter prevent rapid changes in voltages.

Regarding the second assumption, it is always desirable to minimize the resistive voltage drop regarding losses so the resistive voltage drop $R \cdot i$ is magnitudes smaller than the inductive voltage drop ${}^{\mathrm{d}\Psi}/_{\mathrm{d}t}$ (see Figure 1 for definition).

B. Direct flux linkage control for small signal steps

Regarding Figure 1, only two active states of the converter system have to be distinguished:

state 1: the top switch is *closed* and the bottom switch *opened* (outer, green loop in Figure 1)

state 2: the top switch is *opened* and the bottom switch *closed* (inner, orange loop in Figure 1)

A change in flux linkage Ψ can directly be calculated

$$\frac{\Delta\Psi}{\Delta t} = \begin{cases} v_{e1} - v_{e2} - R \cdot i & \text{state 1} \\ -v_{e2} - R \cdot i & \text{state 2} \end{cases} \tag{1}$$

To reach a specific change in flux linkage, one can combine the two states and calculate the necessary times for each state

$$\Delta\Psi_{\text{setpoint}} = \left.\frac{\Delta\Psi}{\Delta t}\right|_{\text{state1}} \cdot t_{\text{state1}} + \left.\frac{\Delta\Psi}{\Delta t}\right|_{\text{state2}} \cdot t_{\text{state2}} \tag{2}$$

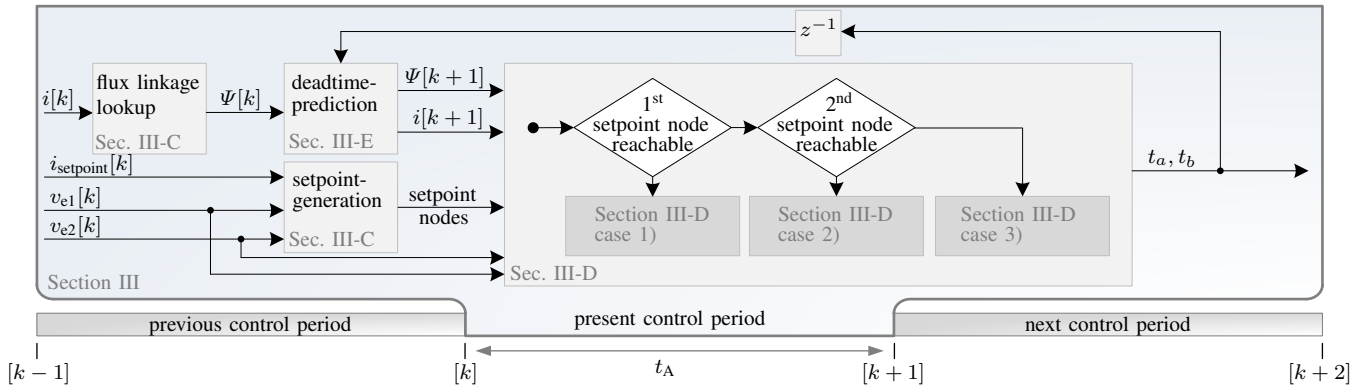


Figure 3. Control implementation on a digital signal processor

Equation (2) is used to control the flux linkage trajectory. Therefore, specific points are defined (further called *setpoint nodes*), through which the flux linkage trajectory is directed by switching the converter between state 1 and state 2. These setpoint nodes are defined by a tuple, consisting of flux linkage setpoint Ψ_{setpoint} and time t_{node}

$$\text{setpoint node} = \{\Psi_{\text{setpoint}}, t_{\text{node}}\} \tag{3}$$

Figure 4 shows an exemplary flux linkage trajectory for the proposed control scheme. The setpoint nodes (marked with help of blue dots [◓]) are distributed equally with a constant time interval of t_{node}. With t_{node} also follows that

$$t_{\text{node}} = t_{\text{state1}} + t_{\text{state2}} \tag{4}$$

Equation (2) and Equation (4) show that the trajectory of flux linkage can normally be commanded through the set point nodes with a single switching action of the phase leg, so the clock frequency of the converter is set with

$$f_{\text{clock}} = \frac{1}{t_{\text{A}}} = \frac{1}{2 \cdot t_{\text{node}}} \tag{5}$$

Obviously the flux linkage value Ψ_{setpoint} of the set point nodes allows to control the average flux linkage and hence control the average output current of the phase leg, as will be shown in Section III-C.

For effective flux linkage control, only the switching times t_a and t_b need to be calculated in such a manner, that the setpoint nodes are met by the flux linkage trajectory. The time t_a is calculated, depending on the inverter state at the beginning of the control period, to

$$t_a = \begin{cases} \dfrac{(v_{\text{e2}} + R \cdot i) \cdot t_{\text{node}} + \Delta\Psi_{\text{setpoint}}}{v_{\text{e1}}} & \text{state 1} \\ \dfrac{(v_{\text{e1}} - v_{\text{e2}} - R \cdot i) \cdot t_{\text{node}} - \Delta\Psi_{\text{setpoint}}}{v_{\text{e1}}} & \text{state 2} \end{cases} \tag{6}$$

$\Delta\Psi_{\text{setpoint}}$ denotes the necessary change in flux linkage which accounts for new flux linkage setpoints or errors in the measured flux linkage trajectory. Flux linkage measurement is done by measuring the output current i and lookup with $\Psi(i)$, see Section III-C for details.

In Figure 4 the measurement instants are marked with purple crosses [⊗]. The flux linkage values are measured, when the converter is in state 1 and at the same time as a setpoint node is given. This is not mandatory, since the measurements can also be made in state two or even to an arbitrary time. This property is used later, to introduce the interleaving scheme in Section IV.

Until now, only the switching time t_a is calculated, which is necessary to reach the first given setpoint node for the control period. In principle, a next measurement can be made at the time of the next occuring setpoint node and the calculation can be repeated. But since the average flux linkage value $\overline{\Psi}$ and hence the average output current $\bar{i}$ is not realized until the second consecutive set point node, it is practical to insert an additional prediction step to calculate the switching time t_b.

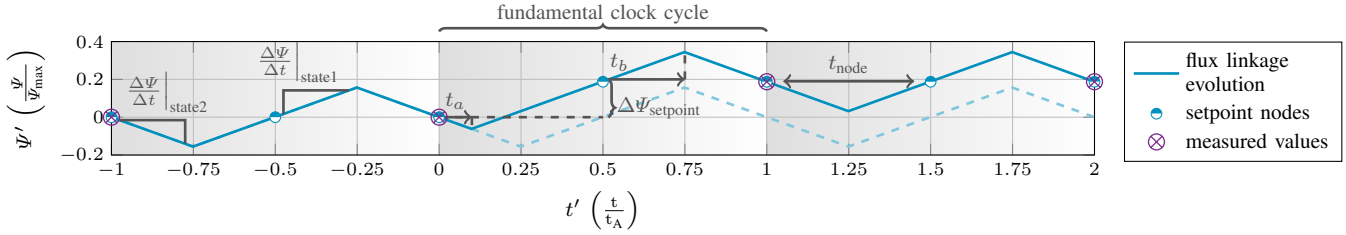


Figure 4. Evolution of flux linkage Ψ for a single phase leg.

This additional prediction step can be calculated – assuming that the set point node at time t_a was met – to

$$t_b = \begin{cases} \dfrac{(v_{e2} + R \cdot i) \cdot t_{node}}{v_{e1}} & \text{state 1} \\ \dfrac{(v_{e1} - v_{e2} - R \cdot i) \cdot t_{node}}{v_{e1}} & \text{state 2} \end{cases} \quad (7)$$

For correct calculation, the converter state at the time of the second setpoint node must be regarded.

C. Flux linkage lookup and setpoint generation

Since the flux linkage Ψ is controlled in a direct manner, but only the output current is easily measurable (and also is the desired output value of the converter), a mapping between measured current i and flux linkage Ψ and vice versa must be made. For the measured values of the system, this mapping is done with a look-up-table, representing the functions $\Psi(i)$ and $i(\Psi)$ using the beforehand measured data presented in Figure 2.

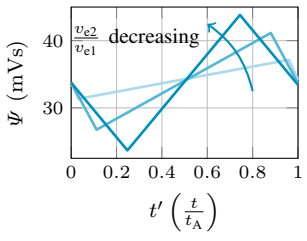
Besides the measured values, also the set point values have to be mapped from a desired average output current value $\bar{i}_{setpoint}$ to the corresponding flux set point $\Psi_{setpoint}$. As shown in Section III, the average flux linkage value can be set by the control scheme, but the flux linkage ripple during one clock period is depending on the voltage v_{e1} and the ratio v_{e2}/v_{e1}.

Regarding Equation (1), the flux linkage trajectory during the switching states of the converter can be assumed to increase or decrease linearly. This is not true for the trajectory of the output current, since it is linked to the flux linkage with help of $i(\Psi)$.

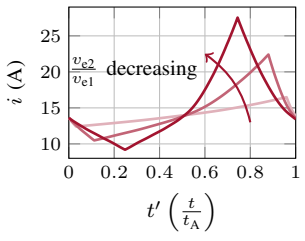
Figure 5a exemplarily demonstrates the flux linkage trajectory for different factors v_{e2}/v_{e1}. Figure 5b gives the resulting current. Here, a ferrite core inductor was assumed, working near its saturation region. Due to the nonlinearity of the inductance, the average output current is depending on the flux linkage $\Psi_{setpoint}$, voltage v_{e1} and voltage v_{e2}. So, the needed lookup table for setpoint generation is defined by three independent variables

$$\Psi_{setpoint} = f(i_{setpoint}, v_{e1}, v_{e2}) \quad (8)$$

This look-up table is generated by a time step analysis for all possible flux linkage set points $\Psi_{setpoint}$ and voltages

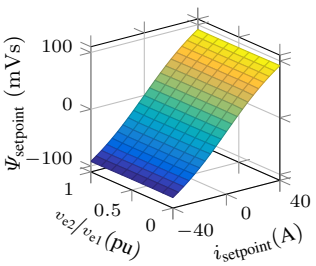


(a) Trajectory of of flux linkage for different values of v_{e2}/v_{e1}

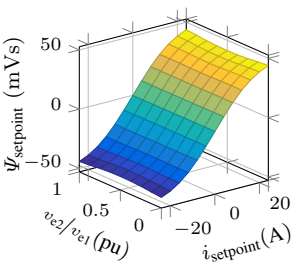


(b) Trajectory of current for different values of v_{e2}/v_{e1}

Figure 5. Flux linkage and current trajectory for a ferrite core inductor, working near its saturation range



(a) Setpoint map for iron powder core inductor



(b) Setpoint map for ferrite core inductor

Figure 6. Setpoint maps for the used prototype inductors

v_{e1}, v_{e2} using measurement data for the used inductor. The resulting current trajectory is averaged over one clock cycle to gain the average output current $\bar{i}$. The desired function $\Psi_{setpoint}(i_{setpoint}, v_{e1}, v_{e2})$ is then generated with help of this simulation data and later used for the control scheme.

The generated set point lookup maps for the two inductor types used in the prototype are shown in Figure 6 . The voltage v_{e1} was set to 650 V, so only the desired average output current $i_{setpoint}$ and the voltage ratio v_{e2}/v_{e1} remain as independent variable.

Figure 6a shows the setpoint map for the iron powder inductor. The flux linkage setpoint dependence on the desired average output current closely resembles the characteristic given in Figure 2. A dependence on v_{e2}/v_{e1} is not visible. This is as expected, since the differential inductance is changing very slowly and no sudden saturation occurs.

In contrast, the setpoint map for the ferrite core inductor presented in Figure 6b shows stronger deviations in respect to the desired output current. Additionally slight deviations in respect to v_{e2}/v_{e1} are observable. Even though these deviations seem very small, they can have large impact due to the nonlinear relationship between flux linkage and current (see Figure 5a and Figure 5b).

D. Handling of large signal steps

Beside small signal steps presented in Section III, also large signal steps of the flux linkage reference have to be handled by the control scheme, to ensure correct operation. Therefore, the maximum possible flux linkage which can be realized at the first setpoint node is calculated with help of Equation (1)

$$\Psi_{max,node1} = \Psi_{start} + (v_{e1} - v_{e2} - R \cdot i) \cdot t_{node} \quad (9)$$

$$\Psi_{min,node1} = \Psi_{start} + (-v_{e2} - R \cdot i) \cdot t_{node} \quad (10)$$

Maximum flux linkage at the second node is derived by

$$\Psi_{max,node2} = \Psi_{start} + 2 \cdot (v_{e1} - v_{e2} - R \cdot i) \cdot t_{node} \quad (11)$$

$$\Psi_{min,node2} = \Psi_{start} + 2 \cdot (-v_{e2} - R \cdot i) \cdot t_{node} \quad (12)$$

Ψ_{start} denotes the measured flux linkage at the start of the control period, see Figure 7 for definition. With the calculated maximum possible flux linkages, following cases can be distinguished:

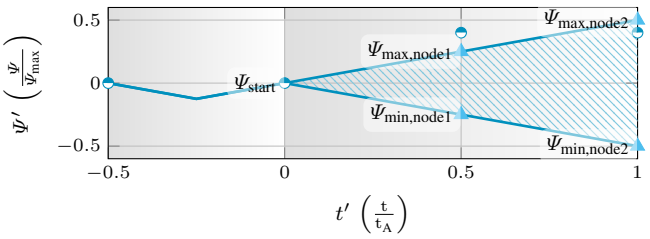


Figure 7. Flux linkage trajectory for state one and state two of the converter.

case 1) $\Psi_{\text{max,node1}} > \Psi_{\text{setpoint}} > \Psi_{\text{min,node1}}$
case 2) $((\Psi_{\text{max,node1}} < \Psi_{\text{setpoint}})$ or $(\Psi_{\text{min,node1}} > \Psi_{\text{setpoint}}))$
and $(\Psi_{\text{max,node2}} > \Psi_{\text{setpoint}} > \Psi_{\text{min,node2}})$
case 3) $(\Psi_{\text{max,node2}} < \Psi_{\text{setpoint}})$ or $(\Psi_{\text{min,node2}} > \Psi_{\text{setpoint}})$

Case 1) represents a small signal change, where the next set point node is reachable. Calculation is carried out with help of Equation (6) and Equation (7).

In *case 2)* the first set point node can not be reached due to limitation of the control plant, but the second consecutive set point node is reachable (Figure 7). To minimize the control error, a switching action is carried out immediately or it is omitted, depending on the current converter state. Afterwards, time t_b is calculated with help of Equation (6) to meet the second setpoint node with a small signal step.

Regarding *case 3)*, the change in set points is so large, that none of the setpoint nodes are reachable. In this case, the control error is minimized as already described in case 2).

The control implementation uses a state machine to ensure correct calculation of switching times.

E. Prediction of dead time

Implementation in a digital signal processor implies computational time, which leads to a dead time. The flux linkage trajectory during that dead time can easily be predicted, since the needed switching time values t_a and t_b are known from the previous control period. The flux linkage value $\Psi[k+1]$ for the next control period is calculated to

$$\begin{aligned}\Psi[k+1] = \Psi[k] + \left.\frac{\Delta\Psi}{\Delta t}\right|_{\text{state}\{1,2\}} \cdot t_a + \\ \left.\frac{\Delta\Psi}{\Delta t}\right|_{\text{state}\{1,2\}} \cdot (2 \cdot t_{\text{node}} - t_b - t_a) + \\ \left.\frac{\Delta\Psi}{\Delta t}\right|_{\text{state}\{1,2\}} \cdot (t_{\text{node}} - t_b) - R \cdot i[k]\end{aligned} \tag{13}$$

To ensure the correct calculation of $\Psi[k+1]$, the state of the converter during the respective intervals has to be regarded by choosing the corresponding $\Delta\Psi/\Delta t$. Since the converter state is known, this imposes no further problems.

IV. Interleaving Scheme

The concept of set point nodes, presented in the last sections, is well suited to interleave multiple phase legs. Figure 8 shows the process of interleaving exemplarily for a three leg inverter. In blue, marked with blue dots [—o—], flux linkage trajectory and set points for leg one are shown (compare to Figure 4). Flux linkage trajectories for leg two and leg three are given in red [—o—] and yellow [—o—] respectively. To establish the desired interleaving, the set point nodes of the single legs are arranged with a time offset

$$t_s = \frac{t_{\text{A}}}{2 \cdot n} \tag{14}$$

where t_{A} denotes the fundamental clock cycle duration of the inverter and n the number of active phase legs.

In comparison to the already derived control scheme for a single phase leg (Section III) two minor additions are necessary to guarantee correct interleaving:

A. Prediction horizon and switching time calculation

Until now, instants of setpoint nodes and measurements coincided. This ensured that all necessary calculations and

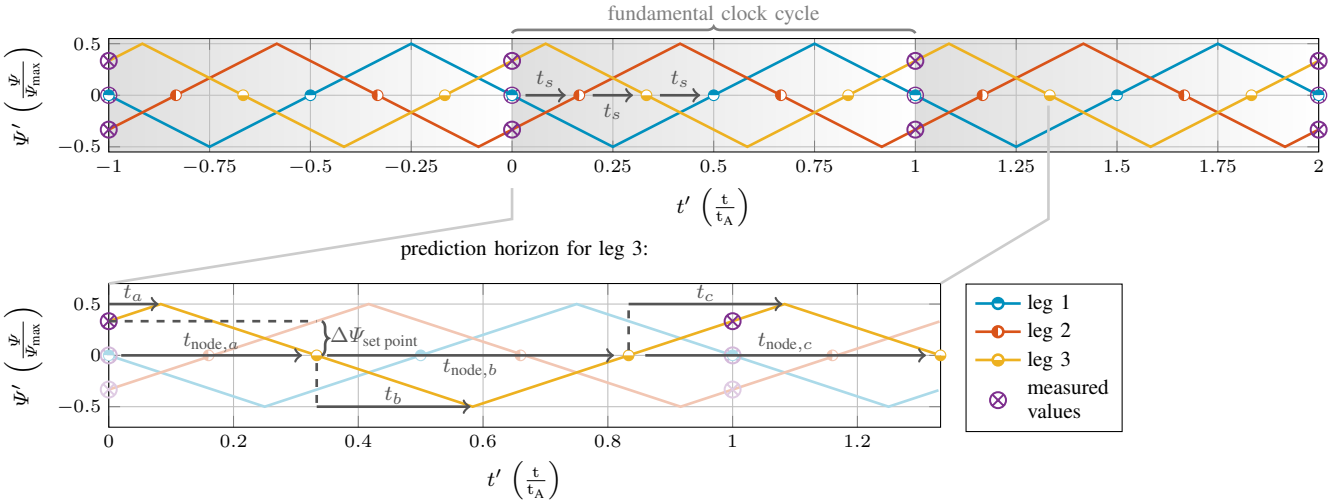


Figure 8. Exemplary implementation of interleaving with shifted set point nodes for a three leg DC/DC-converter

predictions take place between two consecutive measurement instants (see the gray shades in Figure 4 and Figure 8, representing the fundamental clock cycle used for control calculation). This is a special case, which is not valid for interleaved implementation of the direct flux control.

The zoomed cut out of Figure 8 presents the calculation of switching times for leg three of a three leg converter system, demonstrating this circumstance. At the time of the measurement instance, here no setpoint node is given. Nevertheless, the needed switching times t_a and t_b can be calculated with the readily given Equation (6) and Equation (7).

Like observable in the zoomed cutout of Figure 8, the second setpoint node is located some time before the second measurement instant. Since a switching state transition of the converter must take place between the second and the third node, it is possible, that this commutation is necessary before the next measurement and therefore before the next control period. So, to ensure correct results, a third prediction step is needed to calculate the switching time t_c. This is also done with help of Equation (7).

Furthermore, it must be ensured that a switching action did not already happen right before the beginning of the control period. If no further measures are taken, this might lead to a false commutation of the converter, resulting in two switching actions between two consecutive setpoint nodes. Nevertheless, this case can be handled during dead time prediction, since here all switching time instants are known, and switching actions can be prohibited until the next set point node is reached, so no second commutation is possible.

This shows, that the current controller, presented in Figure 3 can be implemented for an arbitrary number of legs with shifted setpoint nodes (Equation (14)). Yet, all control algorithms can be triggered in the same control interrupt and calculated in parallel, so no interleaved triggering is needed.

B. Desired gradient of flux linkage

For the single leg direct flux linkage control, Equation (3) defines set point nodes as tuple of flux linkage value and node time. For interleaved implementation this is not sufficient, since the flux linkage trajectory is not fully defined, because the sign of flux linkage gradient $^{\Delta\Psi}/_{\Delta t}$ at the instants of the setpoint nodes is left as one degree of freedom.

The correct sign is important after large signal steps in particular. Figure 9 gives an example of a large signal step, where only the second node can be reached. The dashed blue line demonstrates the flux linkage trajectory, utilizing the algorithm presented in Section III-D. Even though the second setpoint node is reached in a dead beat manner, the flux linkage gradient in the second set point node is wrong, leading to false interleaving.

The solid line presents a possible procedure to preserve correct sign of the flux linkage $^{\Delta\Psi}/_{\Delta t}$ at the second set point node and enforce correct interleaving. Here, an immediate switching action is introduced, if a violation of the sign of $^{\Delta\Psi}/_{\Delta t}$ is detected. This results in two switching actions to meet the second set point node, by which correct interleaving is ensured.

Finally, for interleaved implementation set point nodes are defined by

$$\text{setpoint node} = \left\{\Psi_{\text{setpoint}}, t_{\text{node}}, \frac{\Delta\Psi}{\Delta t}\right\} \tag{15}$$

Needed adaptions to the state-flow in Figure 3 are trivial, since only a third prediction step is needed and the large signal detection need simple modification.

V. Prototype Setup

The described control scheme was tested with a laboratory prototype inverter, consisting of an active front end inverter and a three leg DC/DC converter (Figure 10). This inverter is used to interface a stationary energy storage system to the grid, therefore, as load a double layer capacitor (DLC) is connected. Technical data is given in Table I.

The usage of the DLC needs a careful design. Since only the terminal voltage is measurable, an observer was implemented to deliver the internal capacitor voltage. The internal resistance R_{DLC} is regarded by setting the resistance value in Equation (6) and Equation (7) for every current controller to

$$R = R_{\text{L}} + 3 \cdot R_{\text{DLC}} \tag{16}$$

The factor 3 is needed, since R_{DLC} is effective for the sumed current of all phases. Even though it seems as if the assumptions made in Section III are violated due to the high resistance value, one has to keep in mind, that the resulting current ripple for the DLC is very low due to the interleaving and the filter capacitor connected to the output inductors. So, regarding R_{DLC} in this way is allowed and increases accuracy of the control scheme considerably.

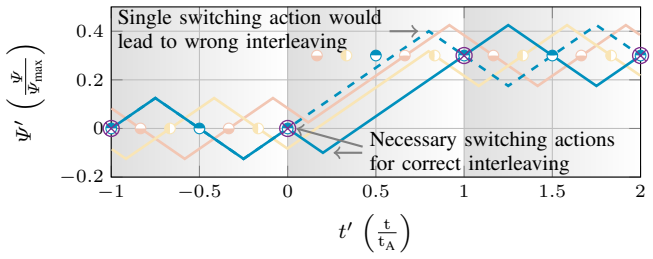


Figure 9. Necessary switching action to ensure interleaving after large signal changes

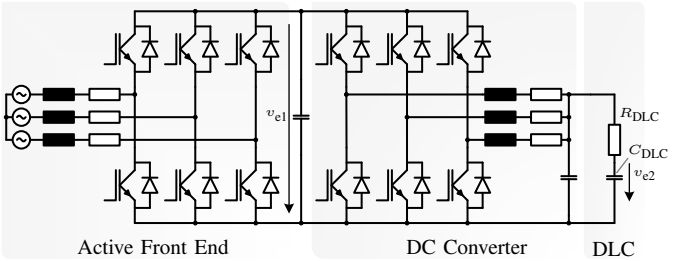


Figure 10. Schematic of the prototype inverter, consisting of active front end and three leg DC/DC-converter with connected double layer capacitor.

Table I
KEY DATA OF THE PROTOTYPE SETUP

inverter		switching frequency	8 kHz
		v_{e1}	650 V
filter inductor	iron powder	i_{nom}	20 A
		L_{nom}	2 mH
		R_L	80 mΩ
	ferrite	i_{nom}	10 A
		L_{nom}	0.9 mH
		R_L	160 mΩ
double layer capacitor		v_{e2}	0 V – 450 V
		C_{DLC}	2 F
		R_{DLC}	440 mΩ

A flexible control system incorporating a digital signal processor from Texas Instruments and a field programmable gate array from Altera was used to implement the control scheme. Besides the DC/DC control also the active front end control runs on the same processor, nevertheless a switching frequency of 8 kHz is reached, demonstrating the low computational requirements of the control scheme.

VI. MEASUREMENTS

All measurements presented here were made with the algorithm for the interleaved control, introduced in Section IV. Therefore in the single phase measurements switching actions are present, according to Section IV-B. Comparison with the measurement of the three leg inverter will show that this switching actions are desired.

A. Single leg measurements

Figure 11 demonstrates different different set point changes, ranging from small signal to large signal. The measurements are taken with iron powder inductors and a DLC-voltage of $v_{e2} = 325\,\text{V}$ resulting in a voltage ration $v_{e2}/v_{e1} = 0.5$.

In addition to the measurements of current trajectories, the averaged currents are shown (dashed lines). For the latter a moving average filter with a length of one fundamental clock cycle was used. The new setpoint values are reached with good accuracy and in a deadbeat manner. Comparison of current ripple shows the effects of lower differential inductance L_{diff} for larger magnetic bias, as expected.

Similar measurements were carried out for a ferrite core inductor (Figure 12). In this case the DLC-voltage was set to $v_{e2} = 100\,\text{V}$, leading to a voltage ratio of $v_{e2}/v_{e1} \approx 0.15$.

The suddenly beginning saturation is clearly visible for currents over approx. 15 A. Nevertheless, due to the setpoint look up presented in Section III-C the commanded average output current is set correctly, even for highly saturated cores. The oscillation observable for the 20 A setpoint can be ascribed to a suboptimal implementation of the DLC-voltage observer. Nevertheless, the current trajectory is stable and accurate after only two clock cycles.

B. Three leg measurements

Finally, measurements for a three leg interleaved converter were carried out. The DLC-voltage was set to $v_{e2} = 325\,\text{V}$. Figure 13 demonstrates an exemplary trajectory of the three output currents. Additionally, the setpoint values are given. After the dead time of one control period, each current trajectory approaches the setpoint as fast as possible, while interleaving is ensured. The zoomed cutouts magnify a small signal and two large signal setpoint changes. As described in Section IV, the average currents for all legs are traced with a single measurement instant, coinciding with the tick marks of the plot.

Regarding the left cutout, a small signal step is show, made within one fundamental clock cycle and good accuracy.

The middle cutout, shows a large signal step and demonstrates correct phase interleaving and necessary switching actions, according to Section IV-B.

The right cutout demonstrates another large signal step. Here, no further switching actions for correct interleaving are needed. The average output current value per inductor is approx. 40 A, which is the double rated current for the inductor (Table I). The higher output current ripple due to a lower differential inductance is also visible, but is tolerable due to the interleaving. So the converter enables short time overload, if necessary.

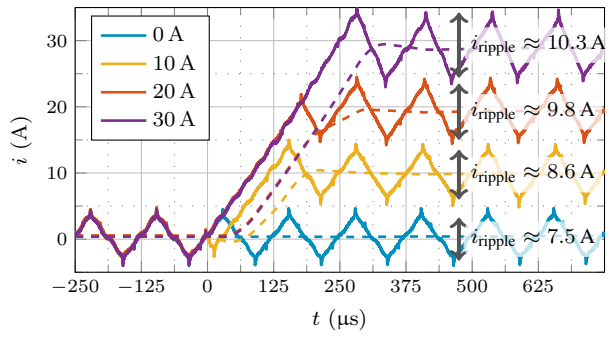


Figure 11. Different setpoint values for the converter, equipped with iron powder inductors. Dashed lines represent the averaged output current. Clearly visible is the increasing current ripple with higher output currents (see also Figure 2)

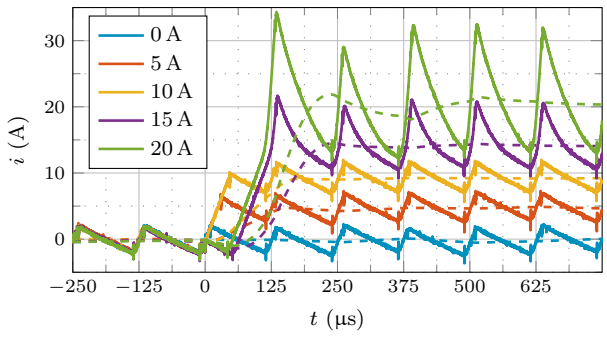


Figure 12. Different set-point values for the converter, equipped with ferrite core inductors. In contrast to the measurements with iron powder inductors (Figure 11), the current ripple stays constant for the nominal operating range. Despite excessive saturation above 15 A, the control scheme remains stable.

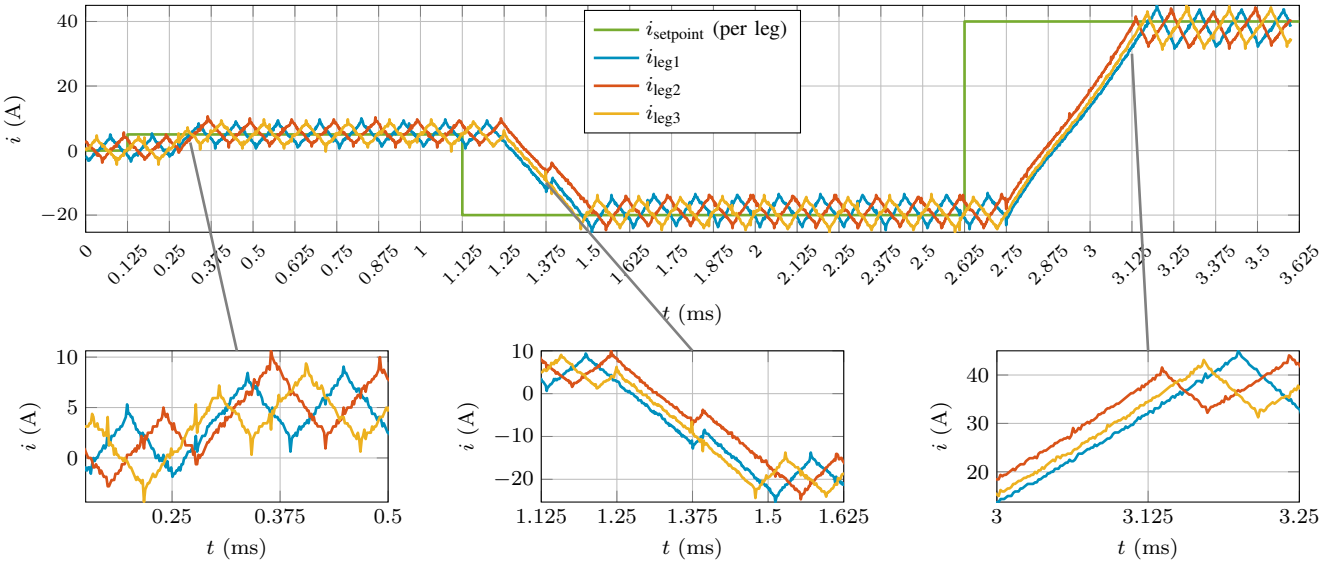


Figure 13. Measurement for 3-leg inverter equipped with iron-powder inductors.

VII. Conclusion

In this paper, the principle of the direct flux linkage control for DC/DC converters is presented. The special feature of this control method is the ability of precise dead beat current control for nonlinear or even saturating inductive filter elements.

Furthermore, due to a special control implementation, n-leg interleaved DC/DC converters are controllable with a single measurement instance per fundamental clock cycle. Effectiveness of the control scheme is shown with a laboratory prototype setup and high filter utilization for different inductor types is demonstrated.

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