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Efficiency Map Computation of Arbitrary Converter Topologies in EV Powertrains

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***Abstract*—Traction converters in automotive applications benefit from various emerging technologies like semiconductor-materials such as SiC or converter topologies like multilevel converters. As especially novel topologies often lack an analytic way to determine their power losses or efficiency, comparability is often hard to achieve until each converter is built up and measured. With the proposed procedure of time-domain simulation, efficiency and loss maps can be calculated, visualizing possible impacts on the cruising range of arbitrary converter topologies. The simulation takes the drive train into account by including the electric machine in form of a standardized parameter set and the battery as fixed voltage source. Even machines with nonlinear magnetics or cross-coupling do not raise a problem, as the parameter set is entirely based on lookup tables. Moreover, simulation results as well as an experimental validation are presented.**

I. Introduction

Electric vehicles gain more and more ground in today's individual and public transportation. One of the main problems that still slow down this development, is the smaller cruising range, compared to similar vehicles with combustion engines. Following the principle that the best energy is energy that is not used, the efficiency of the whole traction chain needs to be optimized. Measures can be taken to quantify and improve the efficiency of the different subsystems, such as machines, inverters or batteries. However, individual efficiency optimization of a single element can lead to deterioration in others. One example is discontinuous modulation, which on the one hand lowers the converter's switching losses but on the other hand increases current harmonics in the driven machine [1], thus increasing iron losses.

In EV propulsion systems, mainly three-phase bridges are used to drive the traction motor. Its converter losses and thus converter efficiency can be quite easily computed, as analytical solutions exist for high pulse rates [2]. If novel topologies shall be evaluated, it is not always possible to straightforwardly compare their efficiency to existing topologies. If known formulas and solutions can not be used or adapted, practices exist that allow fast and easy topology comparison like the Component Load Factor [3], Component Stress Factor [4] or the Switch Utilization Ratio [5]. But they all feature a more superficial result in form of a quality factor. This contribution proposes a time-domain simulation, in which arbitrary topologies can be evaluated in interaction with a given electric machine and DC source. The only information needed about the topology is the schematic and the modulation logic, i.e. how to create the switching signals in dependence of the output-voltage set value. The result is an efficiency map of the particular topology and modulation strategy, dependent on torque and speed of the assumed machine. This map then can be used to identify the total converter losses of a topology e.g. within a complete drive cycle.

In the following section, the loss mechanisms and calculation of power semiconductors will be described, as they are already known from e.g. [2]. After that, the time domain simulation, the associated power loss models and the machine's lookup tables will be described. Subsequently, the simulation results of three different converter topologies (a common three-phase bridge [6], a 3-level I-Type converter [7] and a SiC three-phase bridge [8]) will be shown and compared. To cross-check the simulation results, the last section provides an experimental validation of the simulation tool by comparing simulation results to measured data from a three-phase bridge with connected machine. A conclusion and outlook finish the contribution.

II. Losses in Power Semiconductors

As is known, there are four different kinds of losses in power semiconductors:

- conduction losses,
- switching losses,
- blocking losses and
- driving losses.

In low voltage and low frequency applications blocking and driving losses usually are small, compared to other losses, so they can can be neglected.

A. Conduction Losses

The conduction losses of a semiconductor are (like the blocking losses) part of the so called static losses. As current flows through the semiconductor, a voltage drop occurs. Generally, the voltage drop is not linear dependent on the current as can be seen exemplary in Fig. 1.

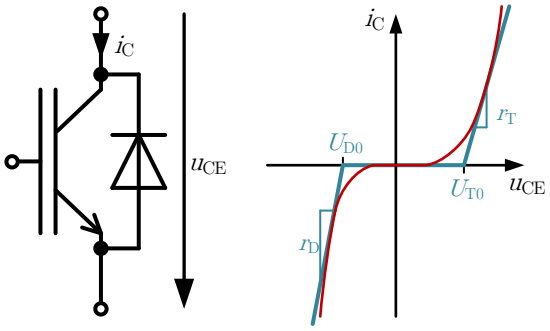

Fig. 1. Exact and approximated forward characteristic of an IGBT and its included free wheeling diode.

The time continuous conduction losses are the product of voltage and current of the considered component:

$$p_{\mathrm{cond}}(t) = u_{\mathrm{CE}}(t) \cdot i_{\mathrm{C}}(t) \tag{1}$$

According to [2], a good approximation to the nonlinear forward characteristic can be done by

$$u_{\mathrm{CE}}(i_{\mathrm{C}}) = U_{\mathrm{T0}} + r_{\mathrm{T}} \cdot i_{\mathrm{C}} \tag{2}$$

which brings (1) to its known form

$$p_{\mathrm{cond}}(t) = U_{\mathrm{T0}} \cdot i_{\mathrm{C}}(t) + r_{\mathrm{T}} \cdot i_{\mathrm{C}}^2(t) \tag{3}$$

The same approach applies just as to diodes, and with $U_{\mathrm{T0}} = 0\,\mathrm{V}$ and $r_{\mathrm{T}} = R_{\mathrm{DS,on}}$ for MOSFETs instead of IGBTs. If synchronous rectification is used, a superposition of the diode and MOSFET forward characteristics results, often referred to as the *3rd quadrant characteristic*. [2] also gives an approach for i_{C} and i_{C}^2 for three-phase bridges with a symmetrical load and thus the resulting total conduction losses. Besides the semiconductors forward characteristics, one only needs the modulation index M, the current amplitude $\hat{I}$ and the phase shift φ (all referred to a fundamental period) to compute all conduction losses in a good approximation:

$$P_{\mathrm{cond,3ph}} = 6 \cdot \left(\frac{\hat{I}}{\pi}(U_{\mathrm{T0}} + U_{\mathrm{D0}}) + \frac{M\,\hat{I}}{4}(U_{\mathrm{T0}} - U_{\mathrm{D0}})\cos\varphi + \frac{\hat{I}^2}{4}(r_{\mathrm{T}} + r_{\mathrm{D}}) + \frac{2\,M\,\hat{I}^2}{3\pi}(r_{\mathrm{T}} - r_{\mathrm{D}})\cos\varphi \right) \tag{4}$$

B. Switching Losses

For power modules, usually datasheet curves of the switching energies exist that show measurement results for certain operating points, as it can be seen exemplary in Fig. 2. At switch-over, the given energy is converted to heat inside the semiconductor. As switching operations are discrete events, a resulting power can be obtained by calculating the average over a certain period of time:

$$P_{\mathrm{sw}} = \frac{1}{T} \cdot \sum_{\mathrm{T}} E_{\mathrm{sw}} \tag{5}$$

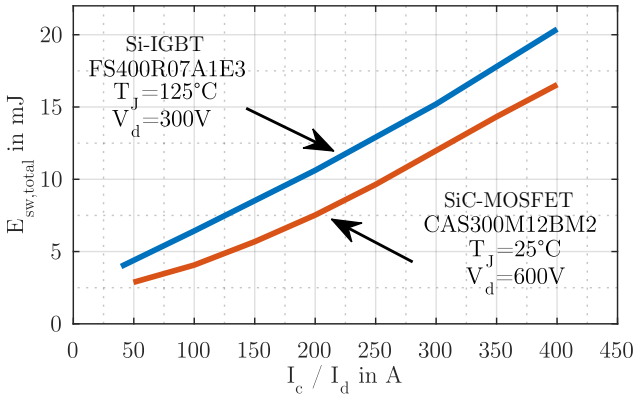

Fig. 2. Comparison of total switching energies. Top: Si-IGBT *Infineon FS400R07A1E3* [6], Bottom: SiC-MOSFET *Cree CAS300M12BM2* [8].

A derivation for a three-phase bridge is introduced in [2], in which these switching energies are originally considered as quadratically dependent on the phase current. Mostly, a linear dependency seems sufficient and is thereby used today [9]. Hence, datasheet values can be adapted to the current operating point:

$$P_{\mathrm{sw,3ph}} = 6 \cdot \frac{1}{\pi} \cdot f_{\mathrm{P}} \cdot (k_{\mathrm{T}} + k_{\mathrm{D}}) \cdot \hat{I} \tag{6}$$

with

$$k_{\mathrm{T}} = \frac{1}{i_0} \cdot \left(E_{\mathrm{on}}|_{i_0,u_d} + E_{\mathrm{off}}|_{i_0,u_d} \right) \tag{7}$$

$$k_{\mathrm{D}} = \frac{1}{i_0} \cdot \left(E_{\mathrm{rec}}|_{i_0,u_d} \right) \tag{8}$$

According to [10], MOSFETs raise a problem, as their switching energies, especially for low currents, exceed the linear approach. The quadratic approximation is better suited here, but an offset in switching energy remains for little or no current, caused by the higher output capacity. [10] expands the approximation of switching losses by a current-dependent correction-factor $cf(I_{\mathrm{D,eff}})$. When looking at the curves of switching energies of IGBTs (e.g. Fig. 2) and extrapolating them to zero current, one can recognize that these also create switching losses (mainly E_{off}) so that a correction-factor for IGBTs could be conceivable, too.

III. Simulation Setup

The whole simulation setup is depicted in Fig. 3. The simulation is processed within Matlab/Simulink, making use of the PLECS Blockset. This is a special extension to Matlab/Simulink that supports the simulation of power electronic systems, and among others their semiconductor losses. PLECS presents a WYSIWYG-Interface to the user, in which schematics and semiconductor characteristics can be fed in.

The input parameters to the Simulink simulation are the DC link voltage V_{DC}, pulse frequency f_{P}, torque T and rotational speed n of the machine. A standardized machine parameter set, which can be gained by measurement or finite elements calculation, is fed with the desired torque and rotational

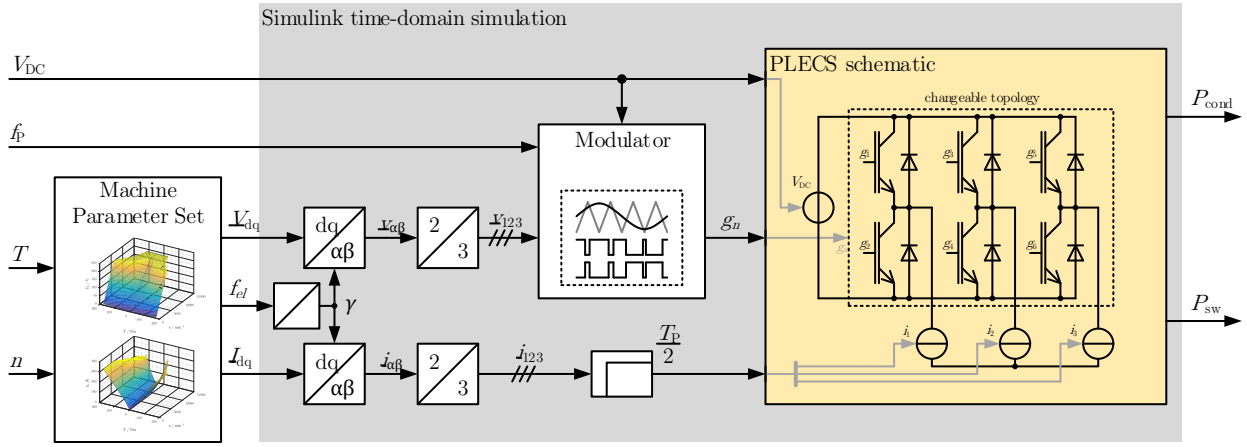

Fig. 3. Signal flow diagram of the simulation tool. The voltages and currents that come from the machine's parameter set first get transformed. The set-point voltage is fed to the modulation-subsystem, the set-point current must be delayed by half a pulse period to remain the correct phase angle. The gate-signals and the delayed currents are then forwardesd to PLECS, which computes conduction and switching losses of the particular inverter topology. Exemplary, a three-phase bridge is depicted as topology to be analyzed.

speed. The machine's parameter-set consists of lookup tables, containing all electrical and mechanical operating data in dependence on the (T, n) operating point, so nonlinearities can be taken into account up to a certain point. The data for these lookup-tables can either be gained by measurement of a real machine, or by finite element calculation. This has the advantage, that – in cooperation with simulations of battery, machine, gearbox etc. – a whole drivetrain of an electric vehicle can be evaluated.

Two of the mentioned lookup tables from the machine's parameter set are needed here, that of the stator voltage space vector $\underline{V}_{\mathrm{dq}}$ and that of the stator current space vector $\underline{I}_{\mathrm{dq}}$, which are both oriented in the d/q reference-frame. In real machines, a position sensor (e.g. resolver) identifies the direction of the d- and q-axes. For the stationary determination of semiconductor-losses, only the angle between voltage and current is relevant, which becomes clear when looking at (4) for three-phase bridges. So stator voltages and currents get transformed to their phase magnitudes $\underline{v}_{123}$ and $\underline{i}_{123}$ by inverse Park- and Clarke-Transformation. Multi-phase machines can be considered, but then these transformations need to be adapted accordingly. As the machine's number of pole-pairs is also known from the parameter set, the rotational speed of the machine n can be converted to the rotational frequency f_{el} of the stator magnitudes. This limits the simulation to synchronous machines at first, but induction machines could be considered, if e.g. the (stationary) slip in each operating point is known.

The modulator's system boundary comprises the inputs of the set-point values v_n, the pulse frequency f_{P} and the DC-link voltage V_{DC} and the output of the gate signals g_n that drive the semiconductors in the PLECS subsystem. The inputs and outputs have vector-format, their widths basically depend on the number of phases, voltage sources and controllable semiconductors. So the modulator subsystem always has to be designed with the particular topology. This usually does not raise a problem, as publications of novel topologies normally include the modulation scheme. The transformed voltages gained from the machine parameter set are fed into this modulation subsystem. To reduce simulation time, it is advantageous to use special MATLAB functions to reduce computation time, as they are introduced in [11].

Instead of a machine model, current sources are implemented to impress the wanted current into one phase leg. So the phase currents i_{123} are fed directly into the underlying PLECS schematic, eliminating the need for a computationally intensive current controller. This is valid, because an ideal controller would keep the actual phase currents nearly identical to those of the machine's parameter set, neglecting current ripple. Besides, the delay time of the modulator must be taken into account, because the mean value of the output-voltage is not valid before half a pulse period. As it is no closed loop control, the impressed currents must be delayed by this half a pulse period to maintain their correct phase angle.

The evaluation of conduction and switching losses is done by PLECS, so adequate data must be gained about the used semiconductor's forward characteristics and switching energies, e.g. from the datasheet or by measurements. These are stored as lookup-tables. By means of these lookup-tables the losses are computed and averaged for every pulse-period. This is performed by quasi-continuous evaluation of (1) and (5) for each semiconductor. The simulation is run for every (T, n)-tuple, that is reachable by the machine. The conduction and switching losses are recorded separately. The simulation time is one electrical period, as after that every possible distribution of power losses inside the inverter has occurred at least once. For no rotational speed ($n = 0$), a maximum simulation time must be set. As the machine's electrical input power is known from its parameter set, the efficiency for every operating point can be identified.

TABLE I
MACHINE PARAMETERS USED FOR SIMULATION

Parameter	Nominal value
Voltage	230 V
Current	340 A
Shaft power	86 kW
Speed	4800 min^{-1}
Torque	172 Nm
Ohmic stator resistance	55 mΩ
Number of pole pairs	3

IV. SIMULATION RESULTS

Currently, interesting questions are the use of multilevel converters or SiC semiconductors in electric vehicles. So three simulation results will be presented and discussed, that show possible chances and problems. In all cases, the forward characteristics of transistors and diodes as well as switching energies were taken directly from the datasheet. As switching losses depend strongly on the mechanical composition of the inverter, all simulations can be seen as best-case scenarios. Furthermore, additional losses arise from parasitic capacities, that are immanent to the cable between converter and machine and the machine itself, which have to be recharged by the converter in every pulse period. It is inherent to the simulation that these parameters are unknown, as the inverters, cables, machines or meachanical setups usually do not really exist.

In the following, a permanent magnet synchronous machine is assumed as traction machine with its key properties listed in table I. All parameters of the machine were merely calculated with a 2D finite elements method. The total battery voltage is fixed to $V_{\mathrm{DC}} = 400\,\mathrm{V}$.

First, as a reference, a single three-phase bridge *FS400R07A1E3* by *Infineon* is simulated. The used schematic is shown in Fig. 4 a). This bridge is automotive qualified and specially designed for electric vehicles. The used modulator subsystem produces a symmetrical PWM scheme without locking- or minimum-on-times at a pulse rate of $f_{\mathrm{P}} = 8\,\mathrm{kHz}$. Fig. 4 shows b)-d) the obtained simulation results. Fig. 4 b) and c) show the conduction respectively the switching losses. Fig. 4 d) shows the resulting efficiency map for this kind of converter. It can be observed, that the efficiency converges to zero for no torque respectively no rotational speed. This is obvious as the output power of the machine and thus the output power of the converter become nearly zero in these cases.

The second examined topology is a 3-level I-type converter (NPC). Suitable modules exist, that allow for an easy and compact construction. One of these modules is the *F3L400R07ME4* by *Infineon*. It is comparable to the three-phase bridge, regarding the peak blocking voltage and peak current, but is not automotive-qualified. Regarding electric drivetrains, a third switchable level is advantageous, as the smaller voltage steps create less harmonics and thus should

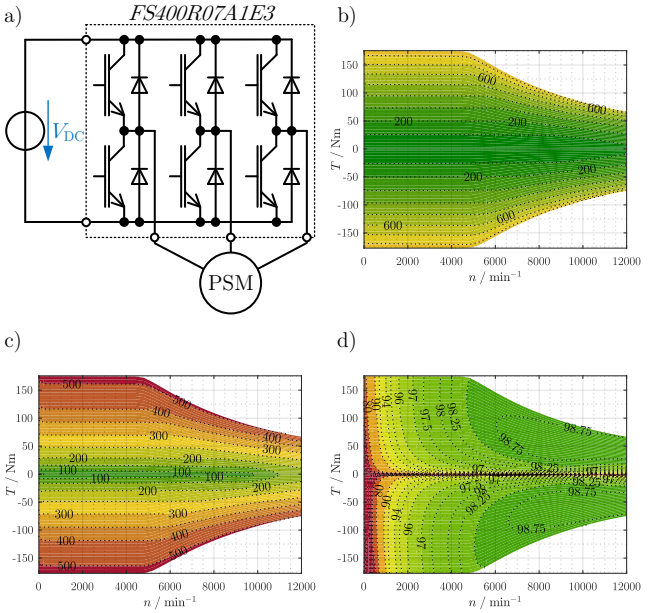

Fig. 4. Simulation results of the three-phase bridge *FS400R07A1E3*. a) Simplified schematic of the two-level topology. b) Conduction losses of all semiconductors. c) Switching losses of all semiconductors. d) Resulting efficiency map of the 3-phase bridge.

reduce iron losses in the connected machine. A single phase schematic is shown in Fig. 5. Since a drivetrain is assumed, it is eligible (but not essential) to split the battery in two halves with $\frac{V\mathrm{DC}}{2} = 200\,\mathrm{V}$ each, so that a center tap results. This tap provides the third switchable level. A double-carrier-based modulation is used to create the gate signals with a pulse period of $f_{\mathrm{P}} = 8\,\mathrm{kHz}$, also neglecting locking- and minimum-on-times. As before, Fig. 5 b) shows the simulative obtained conduction losses, Fig. 5 c) shows the switching losses. In 5 d) the resulting efficiency map is shown.

In comparison to the three-phase bridge the efficiency map hardly changed, but the composition of the semiconductor losses changed noticeably. In the 3-level converter, the conduction losses approximately doubled. This is obvious, as the total number of semiconductors more than doubled and the load current always flows through two semiconductors instead of one. On the other hand, the switching losses remain nearly constant, as the individual semiconductor only has to block half of the total battery voltage, but there are twice as much semiconductors now.

As a third topology, a three-phase bridge is examined, now equipped with SiC-MOSFETs instead of IGBTs and corresponding SiC-Diodes. The loss data were taken from the *Cree CAS300M12BM2* datasheet. As MOSFETs are capable of reverse conduction (i.e. synchronous rectification), special care must be taken to model the third-quadrant characteristic. All other parameters were adopted from the first three-phase IGBT bridge, i.e. $V_{\mathrm{DC}} = 400\,\mathrm{V}$ and $f_{\mathrm{P}} = 8\,\mathrm{kHz}$ without locking- or minimum-on-times. Fig. 6 shows the simulation

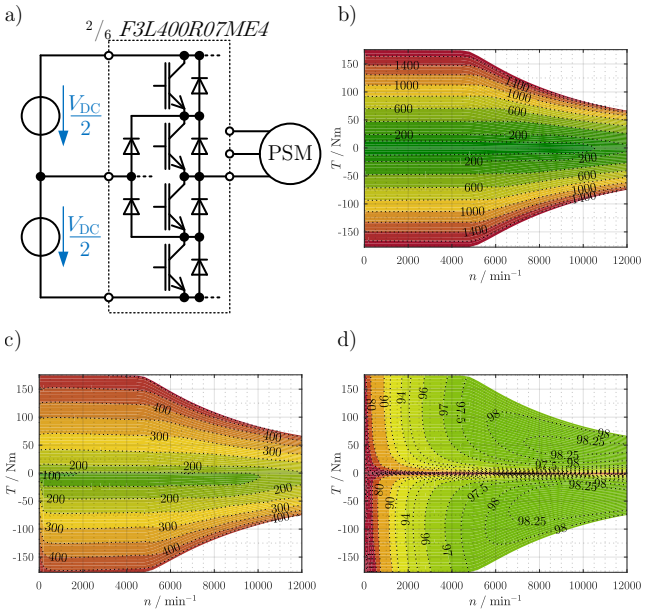

Fig. 5. Simulation results of the three-level NPC *F3L400R07ME4*. a) Simplified schematic of the three-level topology (only one leg shown). b) Conduction losses of all semiconductors. c) Switching losses of all semiconductors. d) Resulting efficiency map of the 3-level converter.

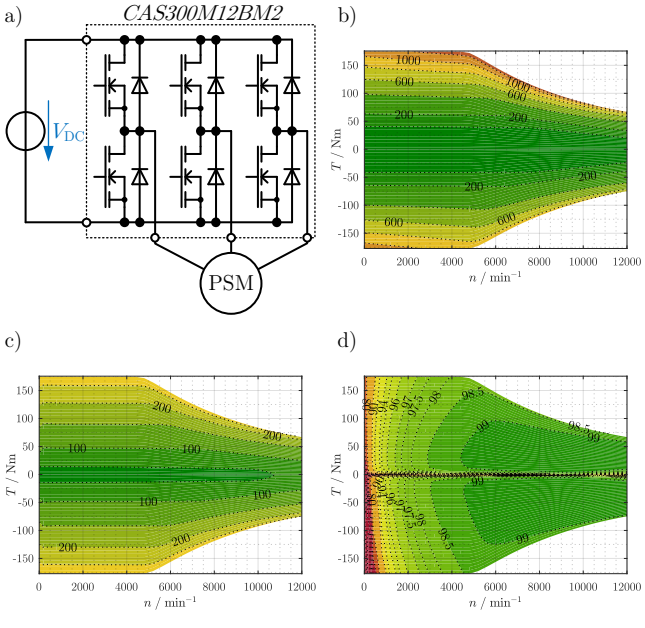

Fig. 6. Simulation results of the SiC three-phase bridge *CAS300M12BM2*. a) Simplified schematic of the two-level topology, equipped with SiC-MOSFETs and diodes. b) Conduction losses of all semiconductors. c) Switching losses of all semiconductors. d) Resulting efficiency map of the SiC three-phase bridge.

results as before.

The switching losses (Fig. 6 c) are about half the amount of those created by the IGBT-based two-level-converter, which

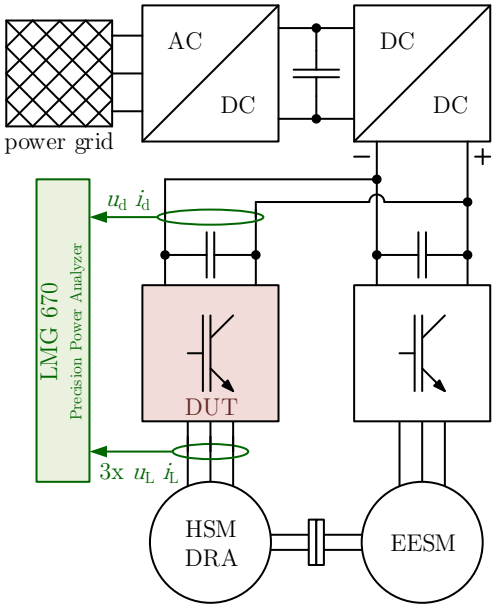

Fig. 7. Schematic of the experimental setup.

corresponds to Fig. 2. On the contrary, the conduction losses increased by about 20%. To sum it up, the total losses are still reduced, which is reflected in a higher peak efficiency. In contrast, it would not be sensible to equip the three-level NPC with those semiconductors, because the doubled conduction losses could not be counterbalanced by the reduced switching losses.

V. Experimental Validation

To evaluate the conformity of the simulation with real semiconductor losses, a setup according to Fig. 7 was built up and measured. An active frontend is connected to a 400 V/50 Hz grid. Via a DC/DC-Converter, a fixed DC-link voltage of 730 V is provided. All power converters are custom Power Electronics Building Blocks, equipped with *Infineon FS75R12KT4* three-phase bridges.

One of these three-phase bridges is the device under test that will be compared to the simulation results from above. It drives a *Hybrid Synchronous Machine with displaced Reluctance Axis* (HSM-DRA) that was developed in [12]. This machine is electrically excited by an auxiliary power supply that is no further considered. The load machine is an electrically excited synchronous machine (EESM). A *Zimmer LMG670 Precision Power Analyzer* measures both the DC input power P_{DC} such as the AC output power P_{AC} of the device under test. All converter control algorithms are executed by a custom digital signal processing system [13] with a control and pulse rate of 8 kHz.

The measured inverter power losses $P_{DC} - P_{AC}$ in the predefined (T,n)-Points are shown in Fig. 8 a). As the electric output-power of the inverter is measured, the efficiency of the inverter can be computed, which can be seen in Fig. 8 b).

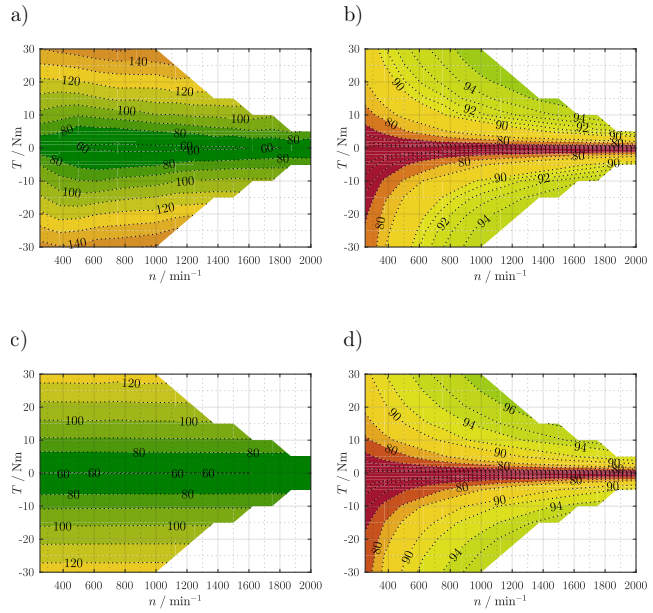

Fig. 8. Results from experimental verification. a) Measured total power losses in device under test (DUT) *FS75R12KT4*. b) Calculated efficiency of the DUT, based on measurement results. c) Simulated power losses. d) Calculated efficiency of the DUT, based on simulation results.

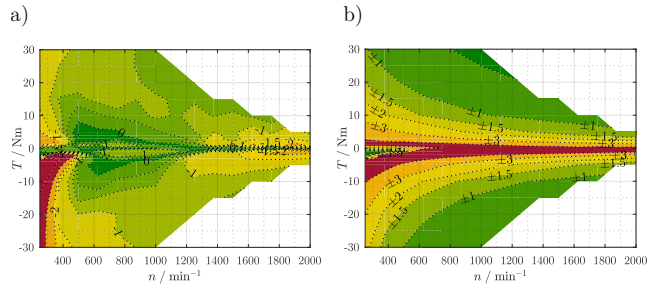

Fig. 9. a) Absolute error between simulated and measured efficency in percentage points. b) Absolute measurement uncertainty of the used power analyzer in percentage points.

The machine's parameter set, gained by measurement, and the semiconductor's loss parameters from the datasheet were fed into the proposed simulation tool and the power losses were simulated. Fig. 8 c) shows the simulated power losses and Fig. 8 d) the resulting efficiency map.

In Fig. 9 a) the absolute difference between the simulated and measured efficiency is shown. The efficiency gained by simulation is always below the the measured efficiency. This accords with the fact, that the simulation can not take additional losses into account (e.g. wires, circuit boards or bus bars). Fig. 9 b) shows the measurement uncertainty of the used power analyzer, which was calculated, using the measurement uncertainties of the individual power measurements. As the uncertainty of the measurement device is bigger than the difference between simulation and measurement, the simulation tool is proven to be adequate to predetermine the efficiency of power converters.

VI. Conclusion

A software tool was presented that allows for creation of efficiency maps of arbitrary traction converters in electric vehicles. By evaluating a standardized dataset, machine voltage and currents are fed into a time-domain simulation. So, for every torque/speed operating point of the machine, the converter efficiency can be gained, which in turn can be used e.g. for estimation of the specific consumption of a car in a drive cycle. Because of its WYSIWYG-interface and special approach in simulation, the tool is an ideal solution to compare different converter-topologies in terms of power losses respectively efficiency. Neither is it needed to deeply analyze current flows nor to built up, control and measure each topology explicitly. A comparison of simulation results was made, regarding different topologies as well as semiconductor materials. In an experimental validation, the simulation results were cross-checked to real measurements.

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