Simple Gate-boosting Circuit for Reduced Switching Losses in Single IGBT Devices

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Abstract

Rise and fall time of current and voltage across an IGBT determine the switching losses under hard switching conditions. Due to parasitic inductances in the gate drive circuit and the device leads, gate charging is delayed and hence switching speed is limited. The simple gate-boosting circuit under investigation enables fast charging of the gate capacitance by applying 80 V external gate drive voltage while not exceeding the specified maximum voltage across the internal gate capacitance. Under hard switching conditions at a collector current of 80 % of the maximum rated pulse current, reduction of turn-on speed and turn-on losses in the order of 90 % could be achieved.

1. Introduction

Under hard switching conditions, current and voltage occur across the switch at the same time, causing switching losses. Switching losses, as product of voltage and current, can be decreased by decreasing the switching time. One method is to employ inherently fast switching elements such as MOSFETs. However, their conduction losses are comparably high. One alternative are IGBTs exhibiting lower conduction losses. The switching speed of IGBTs (and as well of MOSFETs) might be increased by the application of increased voltage to the gate terminal (so called gate boosting), [1]. While other researchers ([1], [2]) employ complex gate drive circuits, the proposed gate drive circuit in this work has been designed without additional active elements to operate at a driver voltage of up to 80 V for single IGBT devices.

2. Gate drive circuitry

One major challenge in fast switching of IGBTs is the fast charging of the gate capacitance. The parasitic inductance of the device leads and gate drive circuit hinders the charging process and reduces the switching speed [3]. For faster charging, a higher voltage at the gate terminal is necessary. However, for operation within the datasheet limits, the maximum voltage across the internal gate capacitance must not be exceeded. As a result, the upper limit for the charge delivered to the gate is the value given in the datasheet. The gate drive circuit under investigation as shown in fig. 1 is basically a damped capacitive divider with damping resistors R_D, dividing the driver voltage V_{GD} between the coupling capacitor C_C and the internal gate capacitance C_G of the IGBT. In the circuit diagram, the IGBT is considered to be an ideal component, whereas its internal components such as gate capacitance C_G, parasitic lead inductance L_P and internal gate resistor R_P are displayed in gray. To compensate charge loss for longer pulses, additional

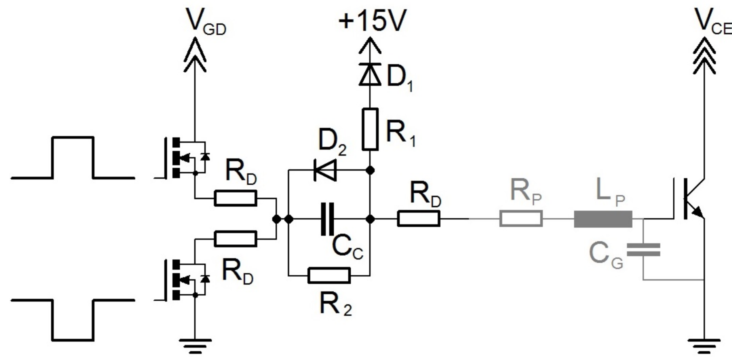

Fig. 1: The gate-boosting circuit under investigation, using drive voltages V_{GD} of up to 80 V. The IGBT's internal/parasitic components are shown in gray.

charge is supplied via resistor R_2 (several kΩ). Diode D_1 and resistor R_1 ensure that the gate voltage settles to approximately 15 V in steady on-state. To prevent gate charging during off-state, diode D_2 offers a low resistance path to ground when the low-side driver is switched on.

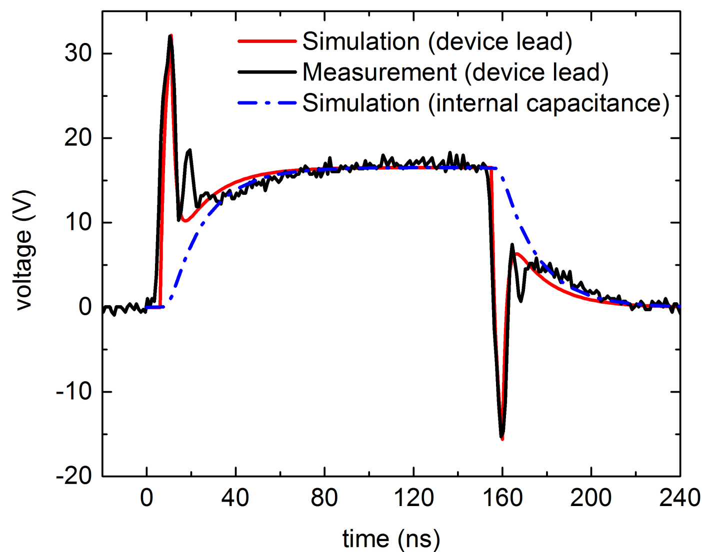

Fig. 2: SPICE simulation results together with measurements on the device leads. Parasitic inductances cause a voltage overshoot which does not affect the internal gate capacitance.

The black trace in figure 2 shows the measured gate signal at the device leads using a gate drive voltage of 80 V. The voltage overshoot of around 30 V as seen in the measurement is caused by the parasitic inductance of the circuit. For reliable operation of the device, however, the voltage across the internal gate capacitance must be limited to the value given in the datasheet($<$20 V, [4]) at all times to prevent damage to the device. To estimate the voltage across the internal gate capacitance, a SPICE simulation based on ideal components as shown in fig. 1 has been performed. The value of capacitance C_G was derived from measurements to

be 18 nF. Values for R_P and L_P have been iteratively adjusted such, that the simulated voltage across the device leads (red solid line in fig. 2) matched the measurement(black solid line in fig. 2). A good agreement was achieved for 8 nH and 0.8 Ω. Under this assumption, the voltage across the internal gate capacitance (blue dashed line in fig. 2) can be derived from the simulation. As can be seen, it stays well within the specified limits. Therefore, the proposed gate drive circuit is considered to be suitable for operation even at high driving voltage.

3. Experimental results

The following results were obtained for a standard IGBT in a TO-247 housing. To ensure hard switching conditions, the total inductance of the test circuit was kept below 60 nH. As the IGBT showed a pronounced increase of rise time for high currents, the measurements were conducted at 25 %, 50 % and 80 % of the maximum rated pulse current in single pulse operation (the device under test: 320 A, [4]). The different currents were achieved by adjusting the load resistance, while the collector-emitter voltage was kept constant at 1 kV. Figure 3 shows collector-emitter current as well as collector-emitter voltage across the IGBT during switching. As both curves coincide, the inductance of the pulse circuit can be neglected.

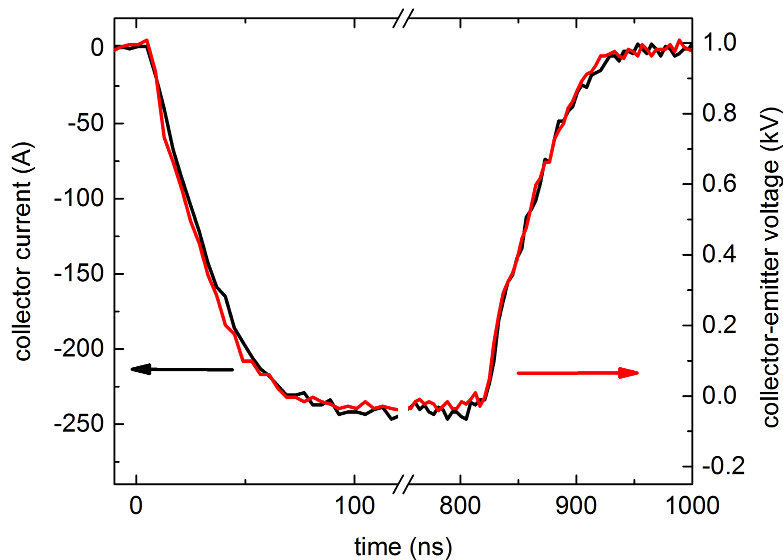

Fig. 3: Collector current and collector-emitter voltage across the IGBT during the pulse. The low inductance of the pulse circuit ensures hard switching conditions.

The driver voltage has been increased up to 80 V. As reference, the coupling capacitor C_C was shorted for applying a driving voltage of 15 V, representing the standard gate drive. In figure 4, the collector current for different driver voltages is shown. From the graph it becomes evident that the switching time significantly decreases for higher driver voltage. Figure 5(a) shows the rise time dependence on the driver voltage for different collector currents. As can be seen, the rise time is strongly increased for higher currents. However, with high driver voltage it is possible to speed up switching by approximately the same order of magnitude for high and low currents. For 80 % maximum pulsed current (256 A) a reduction from 400 ns to 50 ns

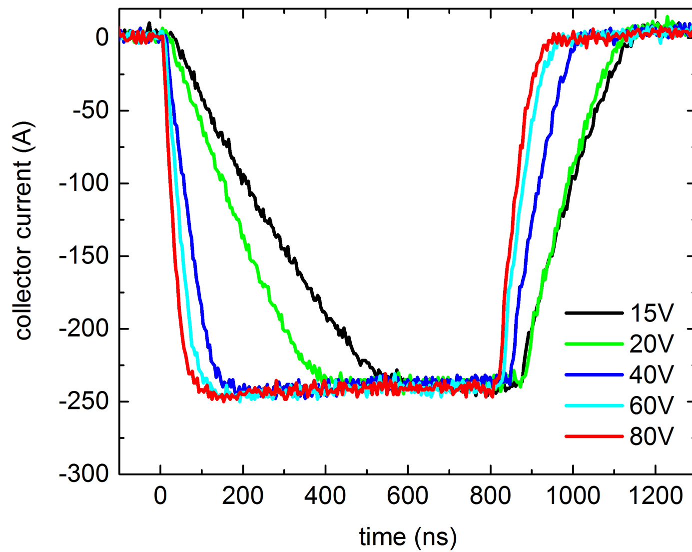

Fig. 4: Collector current for different boosting voltages. A strong increase in switching speed is visible.

was achieved, which is comparable to the reduction from 125 ns to 18 ns for 25 % maximum pulsed current (80 A). The decrease in fall times, however, as displayed in fig. 5(b) is not as pronounced as for the rise times. In addition, the turn-off times are less susceptible to the magnitude of the gate drive voltage for low currents.

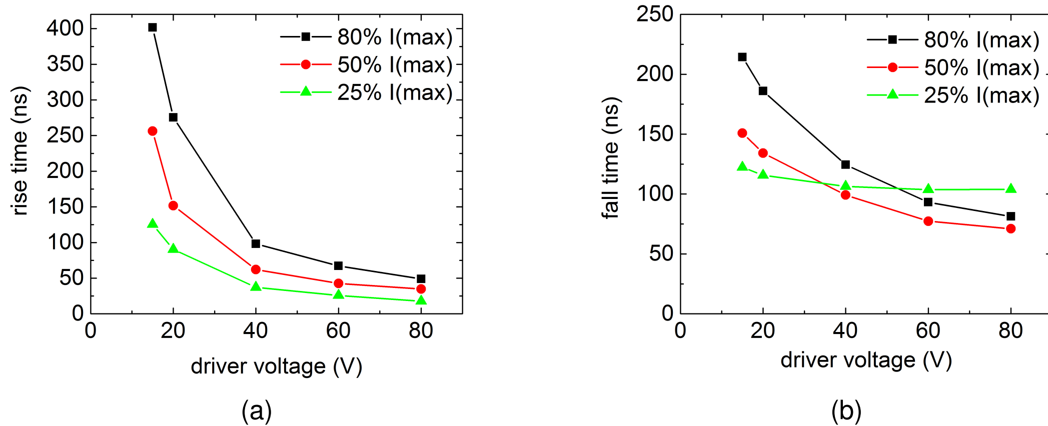

Fig. 5:
(a): Collector current rise time and
(b): fall time for different gate drive voltages at 25 %, 50 % and 80 % of the maximum rated pulse current. The rise time can be influenced to a greater extend by high gate drive voltages.

The resulting switching losses at 80 % maximum rated pulse current are shown in fig. 6(a) for different driver voltages. This data was obtained using a low inductance shunt resistor (as presented in [5]) and a fast high voltage probe. Both measurements were synchronized within 2 ns. Figure 6(b) displays the loss energy normalized to the losses using the standard gate drive. As could be expected from the huge decrease in switching time, the turn-on losses are

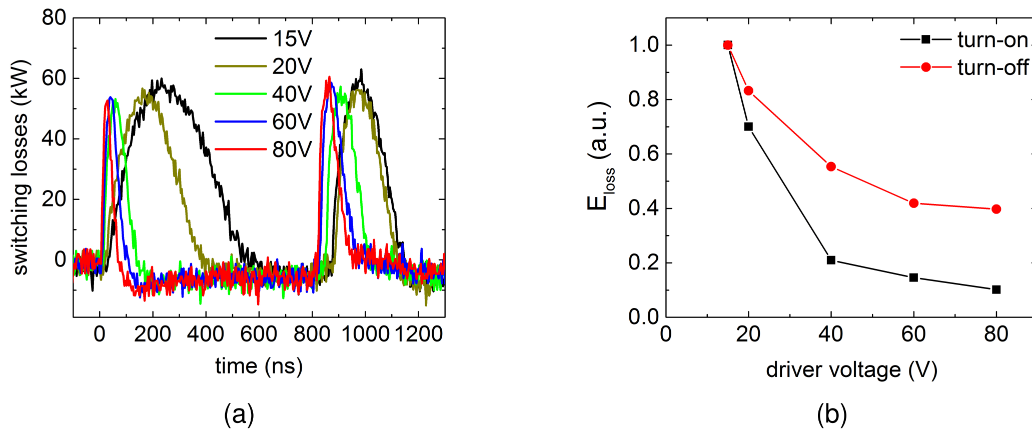

Fig. 6:
(a): Switching losses at 80 % maximum rated pulse current (256 A) for different driver voltages.
(b): Dependence of normalized switching losses on the driver voltage during turn-on and turn-off.

decreased by 90 % for a driver voltage of 80 V. In agreement with the slower fall time, the turn-off losses can be influenced to a smaller extend as compared to the turn-on losses. However, the reduction of turn-off losses of about 50 % is possible for 80 V driver voltage.

4. Summary and Conclusion

To overcome the limitations of IGBTs under hard switching conditions with respect to switching speed and switching losses, a simple gate-boosting circuit has been investigated. It allows fast gate charging by the application of up to 80 V driver voltage. Single trench IGBT devices have been operated at up to 80 % maximum rated pulse current in a low-inductance pulse circuit in single pulse mode. SPICE simulations revealed, that even at 80 V driver voltage, the specifications for the internal gate capacitance were not exceeded. For 80 % maximum rated pulse current it was possible to achieve a reduction of current rise time from 400 ns to 50 ns and accordingly a reduction of turn-on losses in the order of 90 %. It was found that the turn-off losses are not as strongly dependent on the driver voltage. Hence, a decrease of turn-off losses by 50 % was achievable for high currents only. Further work will be devoted to in-depth analysis and optimization of the resulting gate signal with respect to switching speed and reliable operation. Another focus will be the applicability of the proposed circuit to different switching elements.

5. References

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