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Design of a Programmable Passive SoC for Biomedical Applications Using RFID ISO 15693/NFC5 Interface

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Abstract: Low power, low cost inductively powered passive biotelemetry system involving fully customized RFID/NFC interface base SoC has gained popularity in the last decades. However, most of the SoCs developed are application specific and lacks either on-chip computational or sensor readout capability. In this paper, we present design details of a programmable passive SoC in compliance with ISO 15693/NFC5 standard for biomedical applications. The integrated system consists of a 32-bit microcontroller, a sensor readout circuit, a 12-bit SAR type ADC, 16 kB RAM, 16 kB ROM and other digital peripherals. The design is implemented in a 0.18 µm CMOS technology and used a die area of 1.52 mm × 3.24 mm. The simulated maximum power consumption of the analog block is 592 µW. The number of external components required by the SoC is limited to an external memory device, sensors, antenna and some passive components. The external memory device contains the application specific firmware. Based on the application, the firmware can be modified accordingly. The SoC design is suitable for medical implants to measure physiological parameters like temperature, pressure or ECG. As an application example, the authors have proposed a bioimplant to measure arterial blood pressure for patients suffering from Peripheral Artery Disease (PAD).

Keywords: RFID (radio frequency identification); NFC (near field communication); sensor readout; ADC (analog to digital converter); microcontroller; passive; biotelemetry

1. Introduction

Inductive powered biomedical systems brought in complete new dimension in the medical field over the last century. A bioimplant to consider excitable regions in the nervous systems is presented in [1], where the experimental study was conducted on Rhesus monkeys as early as 1949. A similar discussion is also done in the paper [2]. The work [3] demonstrates a pressure sensitive radio transmitting capsule for the study of motility in the gastrointestinal environment as early as 1957.

From the 1950s and 60s onward, the RFID (radio frequency identification) technology is extensively utilized for the design of the remotely powered systems. Since it was first patented in 1973 [4], RFID technology became more and more popular over the succeeding decades. A considerable insight into the evolution track of RFID is mentioned in [5]. The typical operating frequency of RFID varies from a

low frequency range 100 kHz, HF (high frequency) range of 13.56 MHz to ultra-high frequency range of 860–960 MHz and 2.45–5.8 GHz. Biotelemetry systems using RFID have persisted around for years where it is utilized for sensing and wireless identification [6–8].

From 2000 onward, along with the growth of RFID technology, a fresh band of communication protocols was introduced based on the existing RFID standards which is usually known as NFC or near field communication. Unlike RFID, it merely goes on one band of a frequency of 13.56 MHz as it is only functional over a maximum length of 4 centimeters. The telemetry applications have been revolutionized by the introduction of NFC, as a handheld smart device can be utilized to interact. There are five different kinds of available standards for NFC which are type1&2-ISO/IEC 14443 A, type 3-JIS X 6319-4 (Felica), type4-ISO/IEC 14443 A/B and type5-ISO/IEC 15693 (18000-3). The proposed SoC (system-on-chip) is developed based on ISO 15693 standard which corresponds to the standard type 5 or simply NFC 5.

The first SoC appeared in an electronic watch in 1974 [9]. Since then, along with the advancement of silicon technology, SoCs had become an integral lot of electronic devices used in our day to day life. Our smartphones, tablets, laptops or artificial intelligence gadgets, all of them have dedicated SoCs. Complex circuitries can be included in a more limited area which includes analog circuits and digital logic, including memory devices and integrated computational platforms. So biotelemetry is no exception as it requires modest size and lower power consumption.

Table 1 presents an overview of the state-of-the-art SoCs for bio-medical applications. The NFC and RFID enabled ICs [8,10,11] are specifically used for glucose measurement. The SoC presented in [12] is reconfigurable and provides a possibility to integrate a wide range of sensor types (temperature, glucose, pH value and protein concentration) but it does not have an NFC communication interface. A batteryless body sensor node is recorded in [13] is suitable for acquiring, processing and transmitting electrocardiogram (ECG), electromyogram (EMG) and EEG (EEG). This is the only SoC among all which includes an 8-bit microcontroller without NFC communication capability. Thus, a batteryless (passive) SoC which includes RFID/NFC interface, PMU (power management unit), sensor readout interface, integrated ADC (analog to digital converters), integrated microcontroller and is unspecific to a particular application lacks. Our study demonstrates a passive, programmable SoC which includes all these features which are hashed out in detail subsequently.

Table 1. State-of-the-art SoCs for biomedical applications.

Year [Ref]	CMOS (µm)	Wireless comm.	Power Source	PMU	Sensor readout	Integ. ADC	Re-config. /Prog	Integ. µC	Internal memory	Application
2017 [14]	0.13	Bluetooth	Battery	Yes	TIA, INA, CA	14-bit SAR ADC	Yes	No	No	PPG and ECG meas.
2016 [10]	0.6	13.56 MHz NFC, ISO 15693	Battery-less	Yes	MUX, TIA	11-bit sigma-delta	Yes	No	Yes	Glucose meas.
2015 [8]	0.13	13.56 MHz NFC, ISO 15693	Battery-less	Yes	Pstat, MUX	10-bit sigma-delta	N.A	No	No	Cont. glucose monitoring
2015 [15]	0.18	N.A	Battery	No	CA, PGA, INA	9-bit SAR ADC	Yes	No	No	Cochlear implant
2014 [12]	0.35	403 MHz OOK	RF-DC energy harvester	Yes	MUX, TIA, VA, PGA	10-bit SAR ADC	Yes	No	No	Glucose, temp., pH and protein conc. meas.
2013 [16]	0.13	MICS band, OOK receive/ FSK transmit	N.A	No	PA, PGA	8-bit SAR ADC	Yes	16-bit RISC	Yes	Wireless ECG meas.
2013 [13]	0.13	400/433 MHz Freq-multiplying transmitter	RF/Th. energy harvester	Yes	LNA, VA, MUX	8-bit SAR ADC	Yes	8-bit	Yes	ECG, EMG and EEG meas.
2012 [11]	0.18	13.56 MHz carrier freq.	Ind. power	Yes	Integrator, SC	10 bit SAR ADC	No	No	No	Blood flow monitoring

Abbreviations: µC—microcontroller; PMU—Power management unit; SAR—Successive approximation register; ADC—Analog to digital converter; ECG—Electrocardiogram; EEG—Electroencephalogram; EMG—Electromyogram; MICS—Medical implant communication service; FSK—Frequency shift keying; OOK—On-off keying; RF—Radio frequency; PGA—Programmable gain amplifier; TIA—Trans impedance amplifier; INA—Instrumentation amplifier; CA—Capacitive amplifier; VA—Voltage amplifier; LNA—Low noise amplifier; SC—Switch capacitor; Res—Resistive; temp.—temperature; Freq—frequency; Integ.—Integrated; Pstat—Potentiostat; PA—Pre-amplifier; Th.—Thermal; Ind.—Inductive; Meas.—measurement; Conc.—Concentration; N.A—Not available; Re-config.—Reconfigurable; Prog—Programmable; RISC—Reduced instruction set computer.

The mixed signal SoC presented in this paper is designed for low power passive sensor system applications first proposed in [17,18]. The key features included by the state-of-the-art SoC presented in this paper are:

- Battery-less system (completely passive)
- RFID (ISO-15693) /NFC (NFC5) communication interface
- Power management unit
- Sensor readout unit including 12-bit ADC
- 32-bit microcontroller
- RAM (Random Access Memory)
- ROM (Read Only Memory)

The sensor readout unit is capable to acquire ECG data using electrodes, resistive sensor measurements, such as pressure and temperature. Low power design techniques and architecture are used to reduce the overall power consumption. By using the firmware the SoC can be programmed according to the requirement of the application.

The analog part of the SoC is responsible for energy management, RF communication, and sensor data readout. A 32-bit microcontroller, internal RAM, and ROM along with other peripherals are included in the digital part of the design. A much larger circuit complexity is included in a smaller area which makes it low power and cost-effective design. The external components required are memory devices, such as flash or FRAM, sensors, antenna and some passive components. An NFC capable smart device like a smartphone or a tablet can be used to communicate with a sensor tag developed with the proposed SoC.

Organization of the Paper

An application example of the SoC is presented in Section 2. Section 3 discusses in detail the ultra-low power design techniques applied to the design. The system architecture and the design details of the SoC are elaborated in Section 4. In Section 5, the complete layout of the SoC is presented, whereas in Section 6 the functional verification of the SoC is illustrated. Lastly, Section 7 manifests the overall conclusion of the work.

2. SoC Application Example and Advantage of 13.56 MHz Frequency Range in Biomedical Applications

Although the intended application for the SoC is open and can be employed in industrial applications or as a medical implant to measure physiological parameters, such as temperature, ECG or blood pressure. One of the possible applications could be to develop a bioimplant to monitor blood pressure in the femoral arterial system for the patients suffering from Peripheral Artery Disease (PAD). Most of us are aware of arterial blockages in the heart or in the brain; a similar kind of blockage can also occur in places like arteries in the legs. PAD is commonly referred to the arterial blockage of the legs, but it can affect the other arteries (except heart and brain) too. A detailed discussion about the disease is done in the works [19,20]. The work [21] presents in detail the global distribution of the disease based on high-income and low-income countries. As per [21], in 2010 there were 202 million living with the disease, where it also asserts about the occurrence of the disease depending on sex and age of the individual. The idea of the proposed passive implant is to monitor the blood pressure within the blocked artery through invasive method. The particular individual can monitor the arterial condition by using his or her smart device. Figure 1 shows a simplified diagram of the implant realized by using the proposed SoC.

A bioimplant placed inside the human body operates in an environment consisting mostly of bone, skin, fat, blood and muscle. So there is a certain amount of energy loss as the dielectric constant

of these body tissues are much greater than that of air. The relationship in between relative permittivity (ε_r), wavelength of the material (λ_m) and that in free space (λ_f) is given by the equation:

$$\lambda_m = \frac{\lambda_f}{\sqrt{\varepsilon_r}}. \quad (1)$$

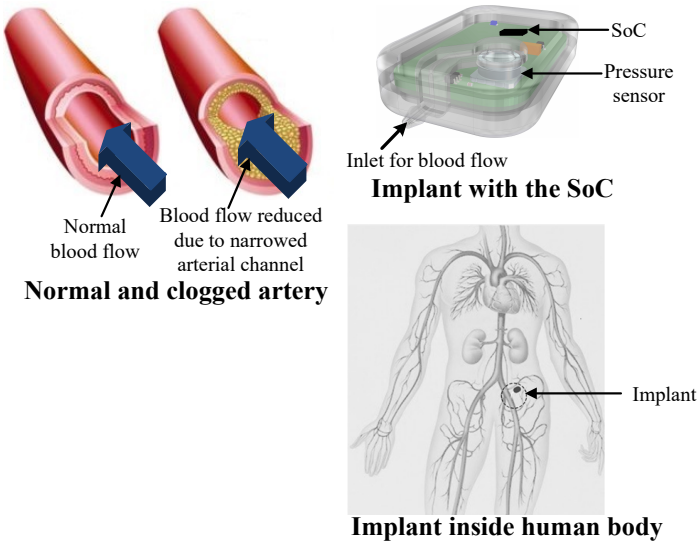


Figure 1. PAD implant realized using the proposed SoC.

The value of ε_r depends on the frequency, Table 2 provides an overview of the value of ε_r and conductivity σ for different body tissues at the frequency range of 13.56 MHz, where λ_f = 22.12 m. The values are obtained from the Federal communications commissions (FCC) document where body tissue dielectric parameters are listed for 10 to 6000 MHz [22]. As the permittivity increases, the wavelength of the material decreases. The variation in the permittivity changes the direction of incident waves from one medium to the other (Snell's law). However, this deviation is inversely proportional to the wavelength, at higher frequencies i.e., 800 MHz and above this deviation is much larger. The frequency range of 13.56 MHz provides a good tradeoff in-between wavelength deviation, read range and data rate.

Table 2. Tissue dielectric parameters for 13.56 MHz [22].

Body Tissue	ε_r (F/m)	σ (S/m)	$\lambda_m(m)$
Blood	210.67	1.12	1.52
Fat	11.83	0.03	6.43
Skin (dry)	285.25	0.23	1.31
Skin (wet)	177.13	0.38	1.66
Avg. Muscle	132.07	0.65	1.92
Avg. Brain	208.23	0.25	1.53
Avg. Skull	44.93	0.09	3.3

3. Ultra Low Power Design Techniques

In modern-day electronics systems, low power design techniques are used to reduce the overall power consumption, of the system, whether it is a battery powered or a battery-less passive system. In this context, numerous methods are embraced by the designers to keep the power consumption as low as possible. A considerable insight into the ultra-low power circuit design is provided in the work [23], which explains the design details at the architectural, physical and system levels. The work

presented in [24] illustrates "The Low-Power Hand" which is fundamentally a tradeoff in between precision, speed, topology, technology, and task for an energy efficient low power design. The work presented in [25] yields a thorough insight of the main design tradeoffs in between the supply voltage, delay, robustness due to technology scaling and variability. Low power designs in the context of wearable and implantable devices are discussed in [26].

3.1. Digital Power Consumption

First, we take a look into the digital power consumption; it can be observed that it is a sum of standby power or the leakage power $(V_{DD}I_{leak})$, short circuit power $\left(C_{sc}V_{DD}^2\right)$ and dynamic power $\left(\frac{1}{2}\alpha C_L V_{DD}^2 f_{clk}\right)$ consumption as given by the equation:

$$P_{dig} = V_{DD}I_{leak} + C_{sc}V_{DD}^2 f_{clk} + \frac{1}{2}\alpha C_L V_{DD}^2 f_{clk} \tag{2}$$

where V_{DD} is the power supply, I_{leak} is the leakage current, C_{sc} is the equivalent short circuit capacitance, C_L is the capacitive load for the digital circuit, f_{clk} is the system clock frequency and α (where $0 \leq \alpha \leq 1$) indicates activity factor which is a function of circuit topology and activity of input signals. From Equation (2), it can be concluded that the power consumption of the digital circuits can be reduced if the supply voltage, clock frequency and the capacitive load are kept at bare minimum. A deeper insight into the same is provided in [23,24,26]. For the SoC, a system clock of 6.78 MHz is used, generated by the internal clock regenerator circuit. Slower clock and absence of an external clock source helps to keep the power consumption low. No wake-up unit manager is provided for the digital part as it is a battery-less system.

3.2. Analog Power Consumption

To reduce the power consumption of the analog circuits, weak inversion or sub-threshold region of operation is used [23,24]. The current equation for the device operating in sub-threshold region $I_{DSub-th}$ can be given as:

$$I_{DSub-th} = I_{D0}\frac{W}{L}e^{\frac{(V_{GS}-V_{th})}{n \cdot v_t}}\left(1 - e^{-\frac{V_{DS}}{v_t}}\right), \tag{3}$$

where I_{D0} is the technology dependent sub-threshold current obtained for $V_{GS} = V_{th}$, where V_{GS} is the gate-source voltage and V_{th} is the threshold voltage, v_t is the thermal voltage, W/L is the aspect ratio and n is the sub-threshold factor [27]. For $V_{GS} = V_{th}$, equation 3 can be further simplified as:

$$I_{DSub-th} \approx I_{D0}\frac{W}{L}e^{\frac{V_{GS}}{n \cdot v_t}} \tag{4}$$

If W/L and V_{GS} are kept constant, $I_{DSub-th}$ only depends exponentially on v_t, resulting in a much smaller current in compare to the saturation or strong inversion region. A vivid description about sub-threshold operation is provided in [27–29]. For the design of the analog part, weak-inversion region of operation is used extensively which is discussed in detail for some of the circuits.

Multiple supply voltages (VDD) can be used to reduce the overall power consumption. Some of the analog circuits are driven by the supply rail VDDI = 1.2 V and digital block, as well as the rest of the external circuits required for the design, are driven by the supply rail VDDE = 1.4 V to 1.8 V. All the analog signals interfacing with the digital block are level shifted to the voltage level of VDDE.

The parts of the analog block, which are unrequired to be always active, are kept switched off and are only activated whenever required for sensor data reading. This helps to reduce the overall power consumption to a great extent. The low threshold voltage transistor is another means to cut the overall power consumption, which is employed in some of the analog circuits.

4. System Architecture and Design Details of the SoC

A simplified system overview is shown in Figure 2 for the passive tag system developed with the SoC. The reader device is an NFC capable smart device, but it can also be a standard RFID reader conforming to the ISO 15693 standard. The antenna shown is responsible for RFID/NFC communication as well as receiving energy from the reader device via inductive coupling. The energy available from the reader field is stored for a very limited period of time, by using a temporary storage device, such as a ceramic or a tantalum capacitor. The external memory device in the form of Flash or FRAM contains the application specific firmware. This makes an enormous flexibility in conditions of usability, as the SoC can be configured and the application program can be altered as per the demand. This is why the SoC is referred as GAPSIC which stands for General Application Passive Sensor Integrated Circuit.

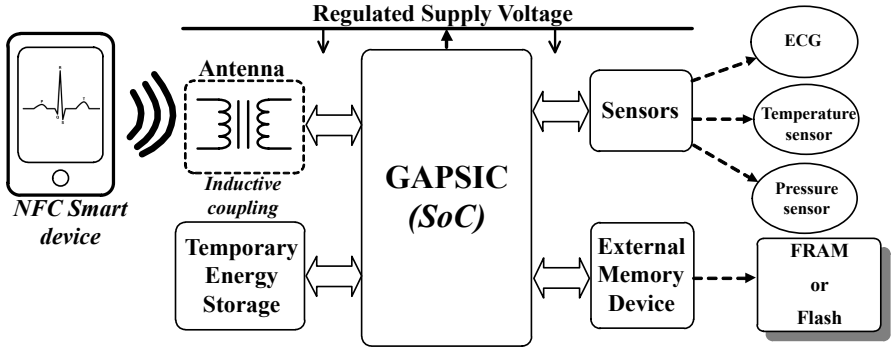


Figure 2. System overview of a passive tag developed using GAPSIC-SoC along with some external components.

Figure 3 exhibits the internal architecture of the SoC, which consists of analog block, digital block, and internal memory devices. The analog block can be further split into two categories RFID/NFC communication and power management unit and sensor readout unit. The digital block consists of a 32-bit integrated microcontroller and digital peripherals. The internal memory devices include 16 KB RAM and 16 KB ROM.

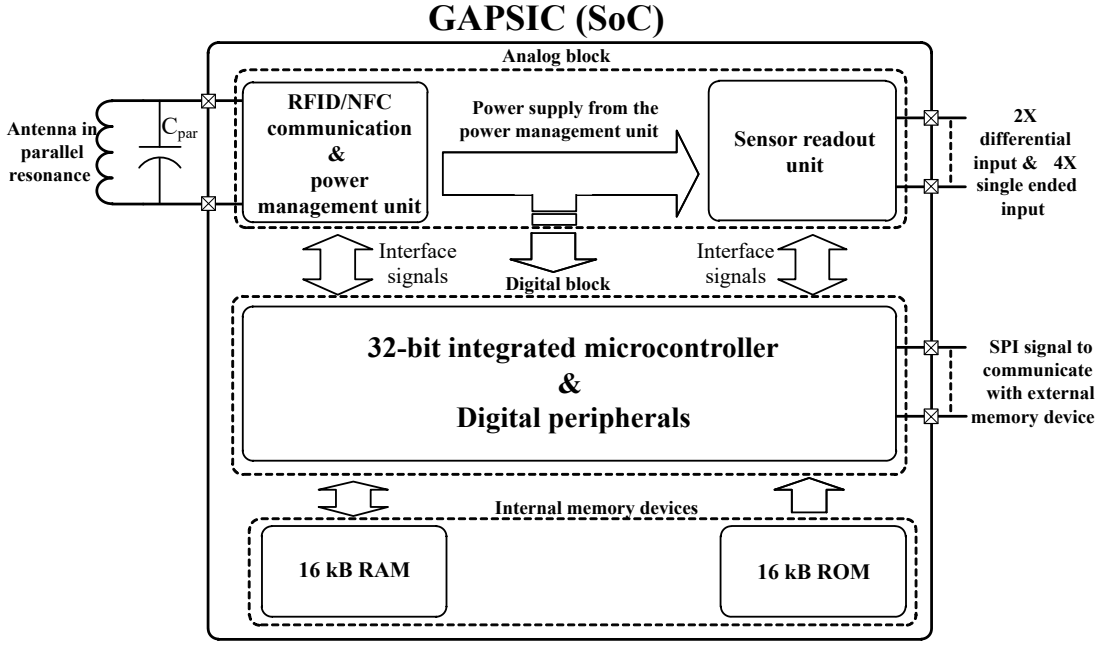


Figure 3. Simplified system architecture of the proposed SoC-GAPSIC.

4.1. RFID/NFC Communication and Power Management Unit

This block is responsible for RFID/NFC communication and also for handling the entire power supply of the chip. Based on the functionalities, this block can be categorized into four different units, such as a power supply management unit, RF communication unit, field detector unit and clock regenerator unit.

In this section, only a brief overview is given, where some of the circuits are discussed in detail. This part is realized as a stand-alone chip which is tested for all of its functionalities. Figure 4 shows the system level block diagram of the RFID/NFC communication and the power management unit where all four functional blocks are shown.

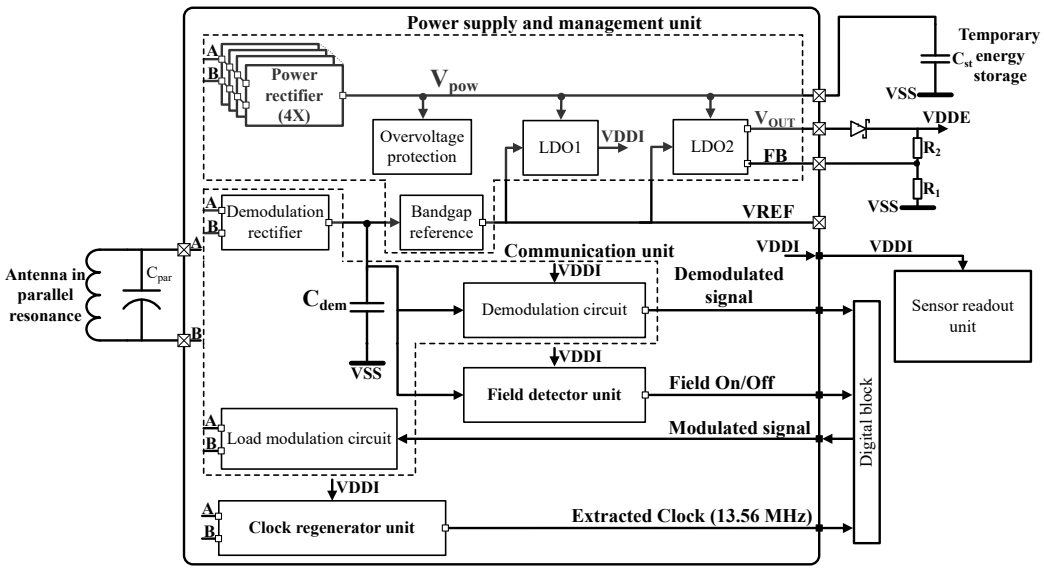


Figure 4. System level architecture for RFID/NFC communication and power management unit.

4.1.1. Power Supply Management Unit

The power supply management part consists of over-voltage protection circuit, power rectifiers, bandgap reference and LDOs (low drop out regulators).

Over-Voltage Protection Circuit

The over-voltage protection circuit and the ESD (Electro Static Discharge) diodes protect the chip from over-voltage conditions. The over-voltage protection circuit consists of a bleeder circuit as discussed in detail in the works [30–33]. The maximum allowed limit for the over-voltage protection circuit is set by the technology which is 3.6 V.

4.1.2. Power Rectifier Unit

Figure 5 shows the power rectifier circuit which supplies both the LDO regulators to fulfill the entire energy requirement of the microchip. Some of the state-of-the-art power rectifiers are presented in recent times are presented in the works [34–36]. In this case, four gates, cross-connected NMOS passive rectifier is used in parallel. The working of a gate, cross-coupled NMOS rectifier is in detail discussed in [33], hence further explanation is avoided here. The phase inverse antenna inputs (A and B) switch on even and odd-numbered transistors in respective clock cycles. The power rectifier can support a maximum load of 8.5 mW and has a maximum power conversion efficiency of 45% for a load of 1 kΩ and an input power of 8 dBm.

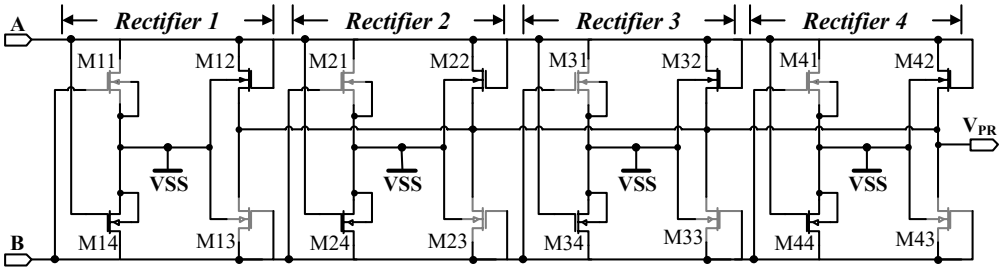


Figure 5. Circuit schematic of the NMOS cross coupled rectifier.

Bandgap Reference

The bandgap reference circuit is used to generate a temperature and supply independent reference voltage which is further used by the LDOs. The basic working principle of the bandgap reference circuit is provided in [37–41]. The work presented in [42] discusses about a bandgap reference circuit for RFID applications similar to the one presented here. The bandgap circuit is powered by the rectified voltage V_{DR} provided by the demodulation rectifier as shown in Figure 4. The average value of $VREF \approx 1.215$ V for nominal temperature of 25 °C. The minimum value of V_{DR} required to turn on the circuit is 1.7 V. The supply voltage sensitivity is 152 µV/V at 25 °C for V_{DR} = 1.7 V to 2.5 V and has a start-up time of 5 µs.

Low Drop out Regulators—LDO1 and LDO2

Two LDOs provide the regulated power supply for the SoC including all the external components. LDO1 provides a fixed supply voltage VDDI of 1.2 V for the internal analog blocks. LDO2 provides the supply voltage in the range of 1.2 V to 2.1 V for all the external components and the internal digital block. The output voltage of LDO2 can be fixed by choosing the resistors R_1 and R_2 as shown in Figure 4. Only LDO1 is discussed here as both the LDOs are similar. The LDOs presented in the works [43–46] analyzes the LDO fundamentals including different kinds of implementation. The LDO1 presented here is very similar to the one presented in the work [46] and is initially proposed in [47].

Figure 6 shows the schematic of the LDO1, where M3-6 forms the first stage, M7-11 forms the second (inverting) stage and the pass element MPa is the third stage. The devices M12-14 form a common source stage with source degeneration. This provides the gate voltage for the load device M16, which acts as an active resistor to set the output voltage at 1.2 V. To achieve a good phase margin and stability, a pole splitting capacitor C_{m1} in the form of Miller compensation is provided along with a resistor R_{m1}. Including only C_{m1} would have caused a right half plane zero (RHP), resulting in a stability issue.

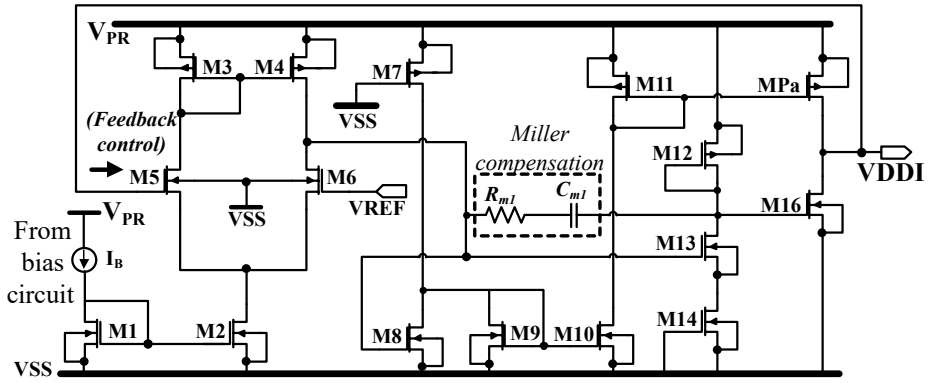


Figure 6. Low dropout regulator 1 (LDO1).

The transconductance, output capacitance and the output resistance for each of the stages are denoted as G_{mx}, C_{ox} and R_{ox} respectively, where the subscript x indicates the respective number of the stage. The transfer function for the proposed LDO1, which is also the loop gain frequency response, is given as $H(s)$, which is further expressed by the following equation:

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{k\left(1+\frac{s}{Z_0}\right)}{\left(1+\frac{s}{\omega P_1}\right)\cdot\left(1+\frac{s}{\omega P_2}\right)\cdot\left(1+\frac{s}{\omega P_3}\right)}, \tag{5}$$

where $V_o(s)$ is the output and the $V_i(s)$ is the input voltage, k indicates the DC gain, Z_0 is the zero and P_1, P_2, P_3 are number of poles for each stage. LDO1 never operates in a no load condition and has to support a minimum load of the communication unit, field detector unit and the clock regenerator unit and the maximum load is for the sensor readout unit. The transfer function is given for the maximum load condition, where the $G_{m3} \gg G_{m1}$ and G_{m2}. The $H(s)$ for LDO1 is given as:

$$H(s) = \frac{-G_{m1}G_{m2}G_{m3}R_{o1}R_{o2}R_{o3}\left(1+s\frac{C_{m1}(1-G_{m1}G_{m2}R_{m1})}{G_{m2}G_{m3}}\right)}{\left(1+\frac{s}{(C_{m1}G_{m2}G_{m3}R_{o1}R_{o2}R_{o3})}\right)\cdot\left(1+s\frac{G_{m2}}{C_{gdPa}}\right)\cdot\left(1+s\frac{G_{m3}C_{gdPa}}{(C_{gdPa}+C_{O2})\cdot C_L}\right)} \tag{6}$$

$$H(s) = \frac{-G_{m1}G_{m2}G_{m3}R_{o1}R_{o2}R_{o3}\left(1+s\frac{C_{m1}(1-G_{m1}G_{m2}R_{m1})}{G_{m2}G_{m3}}\right)}{\left(1+\frac{s}{(C_{m1}G_{m2}G_{m3}R_{o1}R_{o2}R_{o3})}\right)\cdot(1+A\cdot s+B\cdot s^2)}, \tag{7}$$

where A = $\left[\frac{G_{m3}C_{gdPa}}{(C_{gdPa}+C_{O2})\cdot C_L}+\frac{G_{m2}}{C_{gdPa}}\right]$ and B = $\left[\frac{G_{m2}G_{m3}C_{gdPa}}{(C_{gdPa}+C_{O2})\cdot C_L}\right]$. For a large load current G_{m3} will be large and hence the pole P_3 has no effect on the stability. However, a minimum value of G_{m3} is required to maintain for stability reason in case of a smaller load current which is obtained from the loop gain simulation as shown in Figure 7. The differential pair of the first stage is kept in weak inversion region, second and third stage are kept in saturation. Some of the important design parameters are G_{m1} = 66 µA/V, G_{m2} = 4.24 µA/V and G_{m3} = 6.4 mA/V, R_{m1} = 120 kΩ and C_{m1} = 5 pF. M12-14 are kept in cut off region, which drives the device M16 having an equivalent resistance of 3.6 MΩ. The pass transistor MPa is designed with a channel resistance of 432 Ω and gate-drain capacitance of 216.3 fF.

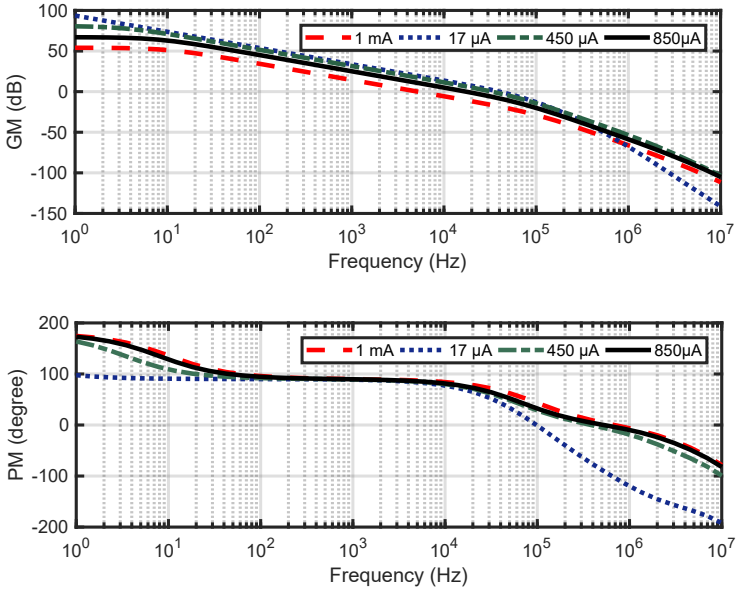


Figure 7. Loop gain simulation. GM = Gain Margin; PM = Phase Margin.

The minimum and maximum load that the LDO1 needs to support ranges in between 17 µA and 450 µA respectively, however it is designed to support a maximum load of 1 mA. The line regulation for minimum and maximum load is 197 µV/V and 92 µV/V respectively. It has a minimum load regulation of 984 µV/mA for a V_{PR} = 1.45 V and 364 µV/mA for a V_{PR} = 1.85 V. For the temperature range of −30 °C to 85 °C and a maximum load of 1 mA it has a dropout voltage of 240 mV. For a V_{PR} = 1.45 V, it consumes a power of 11 µW. An output capacitor of 2.2 µF is sufficient to provide stability for all possible load conditions i.e., from 17 µA to 1 mA. The average PSR (power supply rejection) is 60 dB for all possible load conditions. Table 3 shows the stability analysis for different load conditions.

Table 3. Loop gain parameters for different load conditions for V_{PR} = 1.45 V and at nominal temperature condition of 27 °C.

I_L (µA)	GM (dB)	PM (degree)	UGF (kHz)
17	18	57	23.1
450	31.4	46	46
550	33.1	47	45
850	37.2	49	42
1000	38.8	50	40

Note: I_L is load current; GM is gain margin; PM is phase margin; UGF is unity gain frequency.

4.1.3. RF Communication Unit

The demodulator circuit consists of an envelope detector circuit, first order high pass filter, and a comparator. The demodulation rectifier used is a passive rectifier similar to the one implemented for the power rectifier, but with much smaller device dimension as it needs to support a maximum load of 85 µW. The envelope detector circuit is used to extract the message sent by the reader, which is further given to the comparator circuit to generate the digital bit sequence. The rectifier provides the DC level of the envelope signal, the capacitor C_{dem} stores the charge for a short period of time, which is then discharged through the resistive load which is the bandgap reference circuit itself. The current consumption of the bandgap reference circuit is used as the current load for the envelope detector circuit. For C_{dem} , a 5 pF capacitor is used where the average minimum and maximum discharge time is 1.34 µs and 1.8 µs respectively.

4.1.4. Field Detector Unit

A digital Schmitt trigger circuit is applied to detect the RF field, similar to the one explained in [48]. When the field is detected, the output goes high or else it is low. The low pass filter has a cutoff frequency of 24 kHz as it prevents the Schmitt trigger to alter its state instantaneously in case the RF field is on or off for a very brief period of time. The field on/off signal is further used as the system reset signal by the digital block. The switching on and off time for the circuit is 150 µs and 200 µs respectively.

4.1.5. Clock Regenerator Unit

The clock regenerator unit extracts the clock from the RF field. An RS (set-reset) logic latch is used which is implemented using two NAND gates. The extracted clock pulse has a frequency of 13.56 MHz and a duty cycle of 50 ± 2%. This clock is further divided by half (6.78 MHz) to be used as the system clock. All other clocks required by the SoC are further generated from this clock and no external clock source is used.

4.2. Sensor Readout Unit

The sensor readout unit is initially proposed in [47,49], which is further modified. Figure 8 shows the system architecture of the sensor readout unit proposed here, which consists of channel

selector, virtual ground generator, PGA (programmable gain amplifier) and a 12-bit SAR (successive approximation register) type ADC (analog to digital converter). In the following sections, the design of some of the circuits is discussed in details.

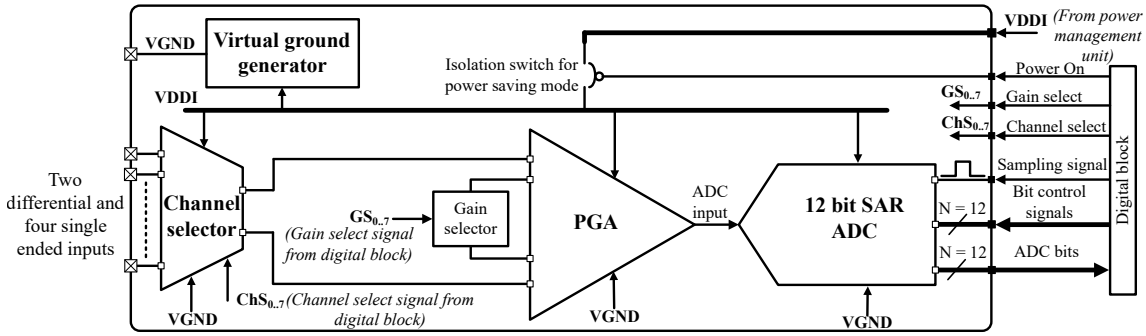


Figure 8. System level architecture for sensor readout unit.

4.2.1. Channel Selector, Bias Generator Circuit and Virtual Ground Generator

The channel selector is realized as a multiplexer which is programmable and can be selected by the digital block. It has two differential and four single-ended inputs.

The bias generator is responsible for generating the bias voltages V_{B1} = 663 mV, V_{B2} = 888 mV and V_{B3} = 242 mV at nominal (27 °C) conditions.

The virtual ground generator fulfills two purposes. Firstly, it provides the reference voltage VGND for the channel selector, PGA and the comparator for the SAR ADC. Secondly, as it is compatible with the human body model, it can be used as the reference potential by the reference electrode for the ECG measurement. Figure 9 shows the simplified circuit diagram of the virtual ground amplifier circuit which is a voltage follower circuit configuration. In the figure, the human body model is characterized by a resistive load R_B = 1.5 kΩ and a capacitive load C_B = 100 − 300 pF, which forms a low pass filter. The output stage of the virtual ground generator shall be able to source and sink current. For this, a PMOS differential amplifier is used as the first stage, which is followed by two common source amplifier stages CS1 and CS2 consisting of PMOS (M6) and NMOS (M9) devices respectively. Both the CS stages provide the voltage headroom close to both the rails for the class AB output stage. Class AB amplifier is ideal to drive larger load capacitances as the push-pull output stage can both sink and source current. M2, M3, M10, and M11 are kept in saturation, M6 and M9 are in weak inversion region. The transconductance (G_m) for each of the stages is given as follows: $G_{m-stage1}$ = 11 µA/V, for CS1: G_{m-CS1} = 9.3 µA/V and for CS2: G_{m-CS2} = 2.8 µA/V.

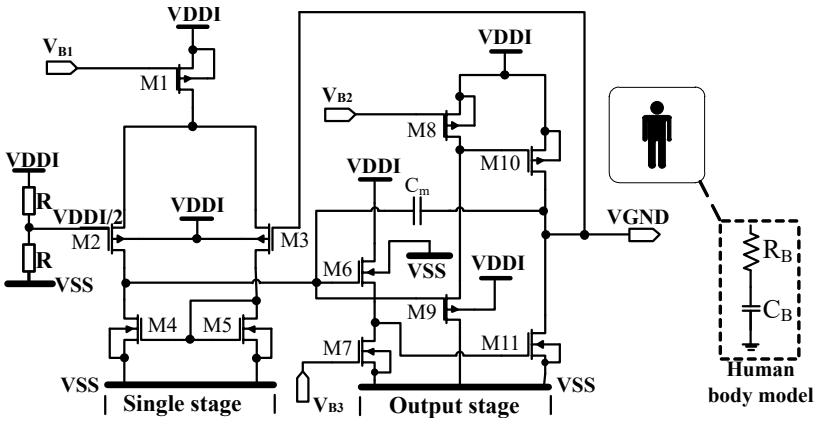


Figure 9. Input buffer amplifier used to generate virtual ground potential VGND.

With a decoupling capacitor of 100 nF, it has a slewing time of 69 µs, settling time of 170 µs and an error band of 4 mV for a temperature of 37 °C which is the normal human body temperature. The closed-loop bandwidth at 37 °C is 10 kHz and has a closed-loop output resistance of 10 Ω. At no load condition, VGND = 606.7 mV and has a load regulation of 20 µv/µA. It has a total power consumption of 172 µW and a minimum and maximum settling time of 160 µs (at 85 °C) and 180 µs (at −30 °C) respectively depending on the temperature. For this design, low threshold voltage transistors are used to keep the overall power consumption, low in comparison to the high threshold voltage transistors.

4.2.2. Programmable Gain Amplifier—PGA

The PGA is implemented using a three op-amp IA (instrumentation amplifier). There are different topologies which can be used to implement an IA some of which are presented in the works [50–52]. In this topology, no offset cancellation technique is provided rather the offset voltage is measured prior to every measurement, which is stored digitally. The stored offset value is then canceled from the measured sensor data.

Figure 10, shows the schematic diagram of the IA used here, where the input stage op amps A_1 and A_2 act as the voltage follower for the inputs V_{in1} and V_{in2}. The input resistance of the op amps A_1 and A_2 is desired to be as large as possible (ideally infinite) so that the signal to be measured remains undistorted. The input stage amplifies the differential signal but allows the common mode signal to pass through without any amplification.

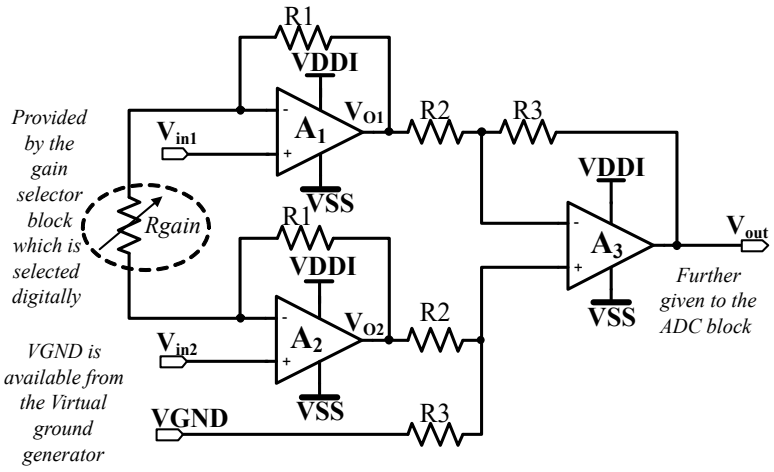
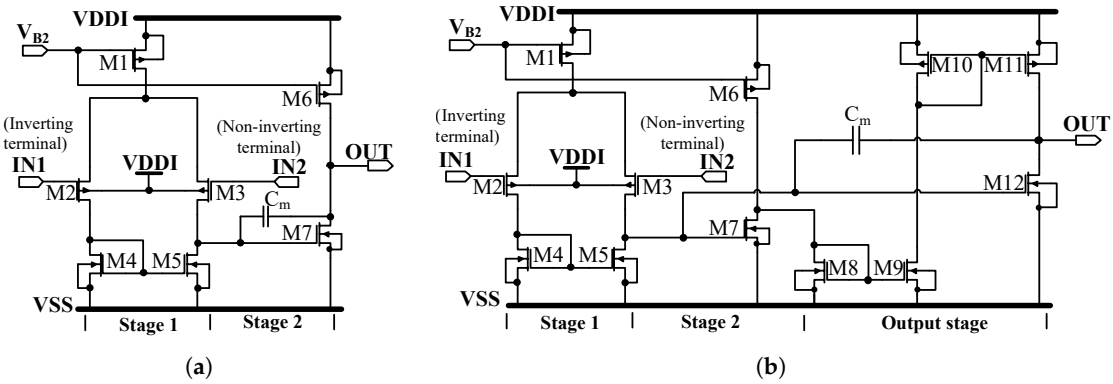


Figure 10. Programmable gain amplifier configuration used where $R_1 = R_2 = R_3 = R = 120\,k\Omega$.

Figure 11 shows the input stage op-amp A_1 and A_2 used, which are identical for the design. A two-stage amplifier is used for this purpose with a small compensating capacitor C_m. It has a loop gain of 54 dB and an offset voltage ranging from −490 µV (−30 °C) to 640 µV (+85 °C), having an offset drift due to temperature by 10 µV/°C. It has a closed loop trans-impedance of 61.4 Ω and a closed loop gain of 46.63 dB in the frequency range of 10 kHz. It provides a CMR of 55 dB at unity gain configuration and has a power consumption of 143.3 µW.

The difference amplifier A_3 is a three-stage amplifier, where first stage amplification is provided by the M2-5, M7 and M6 provide the second stage amplification and the current buffer M8-12 provides the third stage amplification. The topology is very similar to the one used for the LDO1 (Section 4.1.2) hence further explanation is avoided. The difference amplifier has an offset value ranging from 650 µV to −1.4 mV depending on temperature and process variations and has a value of 192 µV at nominal conditions (27 °C).



(**a**) (**b**)

Figure 11. (**a**) Input buffer stage (A1 and A2) operational amplifier for the IA; (**b**) Difference amplifier used for the IA.

The resistor R_{gain} as shown in Figure 10, is used to adjust the overall gain of the PGA, which is selected digitally by using the gain selector. The amplification of the PGA can be adjusted from $1\times$, $2\times$, $10\times$, $20\times$, $40\times$, $50\times$, $80\times$ and $100\times$. The op-amp A_3 is arranged in the difference amplifier configuration involving the resistors R_2 and R_3.

The output of the difference amplifier is given as:

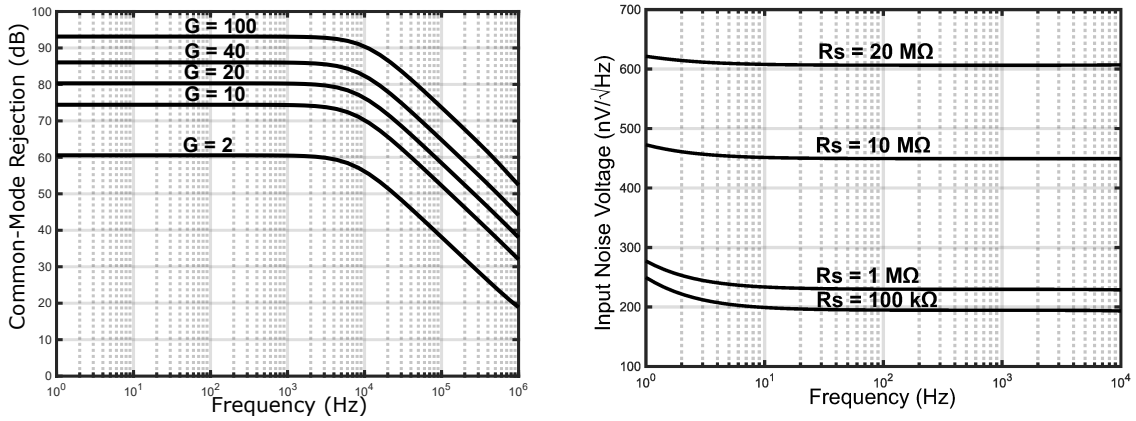
$$V_{out} = G \cdot (V_{in2} - V_{in1}) + VGND \tag{8}$$

where V_{in2} and V_{in1} are the inputs and the G is the gain which is given as:

$$G = \left(\frac{R_3}{R_2}\right) \cdot \left(1 + \frac{2R_1}{R_g}\right) \tag{9}$$

In this case $R_1 = R_2 = R_3 = R = 120\,\text{k}\Omega$. Hence the gain factor G can be given as:

$$G = \left(1 + \frac{2R}{R_g}\right) \tag{10}$$



(**a**) (**b**)

Figure 12. (**a**) Simulated CMR (Common mode rejection) for the PGA; (**b**) Simulated input referred noise of the PGA for different input source resistances.

The common mode signal is removed by the difference amplifier stage. CMR (Common mode rejection) provides an idea about how the PGA will behave in the presence of common mode input

voltage. The CMR of the difference amplifier largely depends on the matching of the R_2 and R_3 resistors which are of the same value and in layout inter digitization is used for better matching. Figure 12 shows the CMR for different gain factor over the frequency range. For a gain of 100×, PGA has a CMR above 90 dB, which is a good figure-of-merit. In case of physiological signal measurement like ECG, the source impedance is in megohm range. Figure 12 yields an estimate of the effect of source resistance on the input noise figure in the measurement process which ignores the noise contribution of the source itself. For better noise immunity, a guard ring is provided in the layout around all the structures of the PGA. The differential pair of A_3 is realized by using common centroid layout to avoid variation due to temperature and process gradient. As obtained from the simulation for the PGA, for unity gain configuration, the closed loop output impedance is 45 Ω, a CMR of 50.6 dB and a power consumption of 157 µW. For a load resistance of 100 kΩ and a load capacitance of 18 pF, the average SR (slew rate) of the PGA varies in between 0.97 V/µs to 1.1 V/µs. The input impedance is 2 MΩ at 100 kHz while the closed loop output impedance varies from 54 Ω to 1 Ω for gain 1× and 100× respectively. The gain margin is 4.5 MHz for a load capacitance of 18 pF and the 3 dB roll-off frequency is at 1 MHz.

4.2.3. 4.2.3 SAR (Successive approximation register) type ADC (analog to digital converter)

A comparative study of different SAR architectures based on power consumption and linearity is provided in [53]. A 10-bit SAR ADC for medical implant devices with a novel switching scheme to improve the energy efficiency is presented in [54]. Some other state-of-the-art designs presented in recent times are [55,56]. The SAR ADC discussed here is based on the architecture provided in the work [57] which is again based on the work [58]. The basic architecture of the proposed SAR ADC is shown in Figure 13. The ADC module strictly comprises of a sample switch, comparator, capacitive array and SAR logic implemented in the digital block. In this architecture, the power consumption is less as each bit gets selected by the SAR logic, which is further added to the sampled input, which is the principal difference between this scheme and the conventional SAR ADC. For each addition of the input signal, the ΔVDAC is compared by the comparator with the reference voltage VGND, in case it is greater than the reference, the comparator gives a digital output of '1' else '0'.

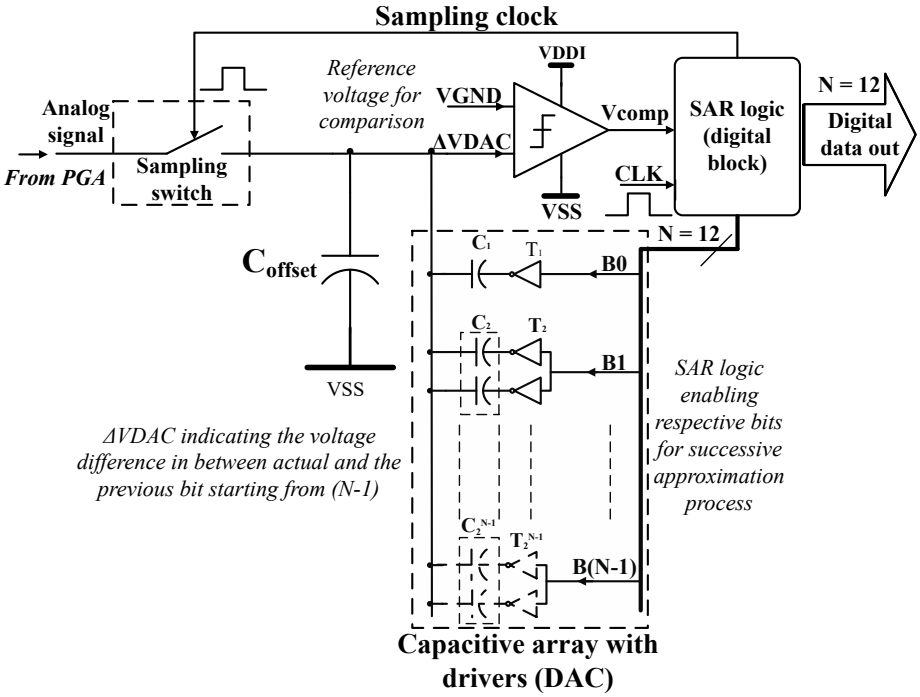


Figure 13. Schematic diagram of the 12-bit SAR ADC.

Sample and Hold Circuit

The process of sampling is controlled by the SAR logic module which is part of the digital block and depends on the mode selected for the ADC conversion. In case the only single conversion mode is selected, it is activated by using an active low signal and again deactivated after single conversion is over, but in case of continuous conversion mode, the process continues till it is stopped explicitly. The sampling switch is accomplished by using a transmission gate. In general, for each of the components used in the signal path, the input capacitance and the effective channel resistance shall be kept as low as possible. The transistors used in the transmission gate are divided into equal numbered fingers. This diminishes the effect of the gate capacitances in the input signal value.

R_{sa} is the equivalent resistance of the sample switch and C_{sa} is the equivalent load capacitance for the sampling switch. The time constant T_{DAC} for the DAC (digital to analog converter) circuit can be given as:

$$T_{DAC} = R_{sa} \cdot C_{sa} \tag{11}$$

The relationship in between sampling time T_{sa} and T_{DAC} is given as:

$$T_{sa} = 3 \cdot T_{DAC} \tag{12}$$

The designed maximum value of R_{sa} is 1.4 kΩ and that of C_{sa} is ∼18 pF, the value of T_{DAC} obtained is 25.2 ns which is much faster than the maximum T_{sa} which is 10.4 µs with 96 kHz sampling frequency. The voltage spikes originating due to gate capacitances of the sampling switch, the comparator and the DAC circuit itself is damped out through the low resistive path provided by the output stage of the PGA which is able to sink current due to its low output impedance which is 1 kΩ ± 10% as obtained from the simulation.

ADC Comparator

Comparators are the key components for an ADC as it sets the accuracy in terms of resolution and the working range of the ADC. The ADCs use either continuous time comparators or latch comparators. Most of the designs incorporate the latch comparator as it is less sensitive to noise distortion in comparison to the continuous time comparators as presented in the works [58–65]. This is due to the separation of the input and output stages but they have a discrete time operation. The work [66], presents a mathematical model for using multiple comparators to reduce the overall power consumption of the SAR ADC.

In this case, a low noise, low offset open loop comparator is used for sensing the voltage difference between each byte and the reference voltage VGND. The input capacitance plays an important role as it adds up to the stray capacitance affecting the overall accuracy of the capacitive array of the ADC.

The practical realization of the comparator is shown in Figure 14, where a two-stage operational amplifier is used. The first stage is realized by using a PMOS differential pair M7-8 with cascode load comprising of M9-12. The sensitivity of the comparator largely depends on the gain of the differential pair which in turn depends on the transconductance and the output resistance. As the output resistance of the 'Stage 1' is increased due to cascoding, the differential stage has an increased gain at the expense of limited output voltage swing. This is again compensated by 'Stage 2' which provides the voltage swing. Higher loop gain ensures good CMR value and lower input offset voltage. In order to have higher transconductance values for the input differential pairs, wide channel transistors are chosen in parallel in order to reduce the gate resistance. Multiple fingers are used to design each of the transistors as it reduces the effect of the input gate capacitances. The use of fingers can only minimize the effect of the gate capacitance mostly the gate-source capacitance C_{gs} but cannot eliminate it completely. The input voltage difference will result in large voltage spikes due to voltage transition caused by the input capacitances. The gate-drain capacitance C_{gd} will generate this spikes/edges to be translated back to both the input nodes. So a lower input capacitance is necessary, along with it the output stage

of the PGA and the sample switch shall be able to sink sufficient amount of current in order to reduce the time constant required to discharge the capacitances. The designed input gate capacitance of the differential pair is 19 fF, gate-drain capacitance is 18 fF, drain junction capacitance is 44 fF and source junction capacitance is 53 fF.

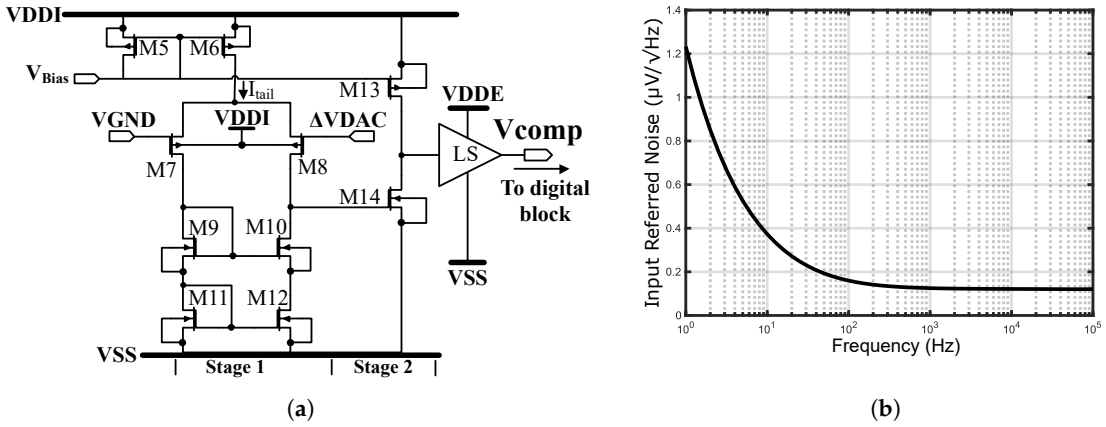


Figure 14. (**a**) Schematic of the open loop comparator used for the ADC where LS indicates level shifter; (**b**) Simulated input referred noise of the ADC comparator for a source resistance of 100 kΩ and input capacitance of 20 pF.

Along with the input offset voltage, the thermal noise and the $\frac{1}{f}$ noise also brings in limitations for the accuracy of the comparator. The total input referred noise figure for the comparator is illustrated in the following noise analysis part.

The gain provided by the first stage of the comparator is A_{v1} and that of second stage is A_{v2}, where the overall gain A_v is given by:

$$A_v = A_{v1} \cdot A_{v2} \tag{13}$$

$$A_{v1} = -G_{m1} R_{o1}$$

where G_{m1} is the gain for the first stage and R_{o1} is the equivalent output resistance for the first stage. Now $G_{m1} = g_{m7} = g_{m8}$ and R_{o1} is given by the equation:

$$R_{o1} = \frac{r_{o8}\left[r_{o10}\left(1 + g_{m10} r_{o12}\right) + r_{o12}\right]}{\left[\left(r_{o10} + r_{o8} + r_{o12}\right) + g_{m10} r_{o10} r_{o12}\right]} \tag{14}$$

$$\Rightarrow A_{v1} = \frac{-g_{m8} r_{o8}\left[r_{o10}\left(1 + g_{m10} r_{o12}\right) + r_{o12}\right]}{\left[\left(r_{o10} + r_{o8} + r_{o12}\right) + g_{m10} r_{o10} r_{o12}\right]} \tag{15}$$

$$A_{v2} = g_{m14}\left(\frac{r_{o13} r_{o14}}{r_{o13} + r_{o14}}\right) \tag{16}$$

$$\Rightarrow A_v = \frac{-g_{m8} g_{m14} r_{o8} r_{o13} r_{o14}\left[r_{o10}\left(1 + g_{m10} r_{o12}\right) + r_{o12}\right]}{\left[\left(r_{o10} + r_{o8} + r_{o12}\right) + g_{m10} r_{o10} r_{o12}\right]\left(r_{o13} + r_{o14}\right)} \tag{17}$$

Equation (13) can be further interpreted as Equation (17) in terms of transconductance g_{mi} and output resistance r_{oi} for the individual devices where suffix i denotes the respective device from Figure 14.

The total input referred noise $\overline{V^2_{n,in,tot}}$ is given as the sum of low frequency noise or $\frac{1}{f}$ noise and thermal noise. For the noise analysis, the noise contribution for each of the stages are considered depending on the region of operation for the individual devices.

Since the noise sources are uncorrelated, the principle of superposition can be used for the addition of the noise power. The $\frac{1}{f}$ noise $\overline{V^2_{n,1/f-1}}$ for the first stage differential pair is given as:

$$\overline{V^2_{n,1/f-1}} = \left[\frac{2K_P}{C_{ox}\,(W.L)_{7,8}}\frac{1}{f}\right] \tag{18}$$

where K_P is a process dependent constant for PMOS devices provided by the foundry, C_{ox} is the oxide thickness, $(W.L)_{7,8}$ is the device dimension for M7-8 and f is the frequency. The process dependent factor K_P is smaller for PMOS devices in compare to the NMOS devices (K_N) as the later uses buried channel to carry holes. The thermal noise depends on the region of operation. Similarly the low frequency noise contribution for the second stage $\overline{V^2_{n,1/f-2}}$ is given by:

$$\overline{V^2_{n,1/f-2}} = \left(\frac{1}{C_{ox}f}\right)\left[\frac{K_N}{(W.L)_{14}} + \frac{K_P}{(W.L)_{13}}\left(\frac{g_{m13}}{g_{m14}}\right)^2\right] \tag{19}$$

As shown in Equation (19), if the process dependent factors are kept constant, the $\frac{1}{f}$ noise is only dependent on the device dimensions. Hence large device dimensions are chosen to ensure smaller noise figures at low frequency.

$(W.L)_{13/14}$ and $g_{m13/14}$ are the device dimension and transconductances for the devices M13 and M14 respectively. So the total $\frac{1}{f}$ noise for both the stages combined $\overline{V^2_{n,1/f-tot}}$ are given by:

$$\overline{V^2_{n,1/f-tot}} = \left(\frac{1}{C_{ox}\cdot f}\right)\left[\frac{2K_P}{(W.L)_{7,8}} + \frac{K_N}{(W.L)_{14}} + \frac{K_P}{(W.L)_{13}}\left(\frac{g_{m13}}{g_{m14}}\right)^2\right] \tag{20}$$

For long channel devices operating in strong inversion region the noise current $\overline{I^2_n}$ is given by:

$$\overline{I^2_n} = 4kT\gamma g_m \tag{21}$$

where γ is called the excess noise factor. For devices in strong inversion $\gamma = \frac{2}{3}$ for long channel devices and $\geq$2 to 3 for short channel devices. For devices in weak inversion region $\gamma = \frac{n}{2}$. The thermal noise voltage $\overline{V^2_{n,T}}$ for individual devices is given as:

$$\overline{V^2_{n,T}} = \overline{I^2_n} r^2_o \tag{22}$$

where r_o is the output resistance for the particular device. For the first stage the differential pair (M7 and M8) and the load devices (M9-12) operate in weak inversion region. The total output thermal noise for the first stage $\overline{V^2_{nout,T-1}}$ is given as:

$$\overline{V^2_{nout,T-1}} = 4kTn\left[G_{m1}R^2_{o1} + g_{m10}r^2_{o10} + g_{m12}r^2_{o12}\right] \tag{23}$$

Total input noise figure $\overline{V^2_{nin,T-1}}$ for the first stage is given as:

$$\overline{V^2_{nin,T-1}} = \frac{\overline{V^2_{nout,T-1}}}{A^2_{v1}} \tag{24}$$

$$\Rightarrow \overline{V^2_{nin,T-1}} = 4kTn\left[\frac{1}{G_{m1}} + \frac{g_{m10}}{G^2_{m1}}\left(\frac{r_{o10}}{R_{o1}}\right)^2 + \frac{g_{m12}}{G^2_{m1}}\left(\frac{r_{o12}}{R_{o1}}\right)^2\right] \tag{25}$$

where R_{o1} is given by Equation (14).

Similarly for the second stage the thermal noise figure can be obtained depending on the operating region for the individual devices. The device M13 operates in strong inversion region and M14 is kept in weak inversion region, so the second stage output thermal noise $\overline{V^2_{nout,T-2}}$ is given as:

$$\overline{V^2_{nout,T-2}} = 2kTn\left(\frac{r_{o13}r_{o14}}{r_{o13}+r_{o14}}\right)\left[g_{m14}+\frac{2}{3}g_{m13}\right] \tag{26}$$

Total input noise figure $\overline{V^2_{nin,T-2}}$ for the second stage is given as:

$$\overline{V^2_{nin,T-2}} = \frac{\overline{V^2_{nout,T-2}}}{A^2_{v2}} \tag{27}$$

$$\Rightarrow \overline{V^2_{nin,T-2}} = 2kTn\left(\frac{1}{g_{m14}}\right)\left(\frac{r_{o13}r_{o14}}{r_{o13}+r_{o14}}\right)\left(1+\frac{2}{3}\left(\frac{g_{m13}}{g_{m14}}\right)\right) \tag{28}$$

So the total input thermal noise $\overline{V^2_{nin,T-tot}}$ contribution for the first stage and the second stage combined is given by the sum of Equations (25) and (28):

$$\overline{V^2_{nin,T-tot}} = 4kTn\left[\left\{\frac{1}{G_{m1}}+\frac{g_{m10}}{G^2_{m1}}\left(\frac{r_{o10}}{R_{o1}}\right)^2+\frac{g_{m12}}{G^2_{m1}}\left(\frac{r_{o12}}{R_{o1}}\right)^2\right\}+ \frac{1}{2}\left\{\left(\frac{1}{g_{m14}}\right)\left(\frac{r_{o13}r_{o14}}{r_{o13}+r_{o14}}\right)\left(1+\frac{2}{3}\left(\frac{g_{m13}}{g_{m14}}\right)\right)\right\}\right] \tag{29}$$

The total input noise figure $\overline{V^2_{n,in-tot}}$ including both the low frequency and the thermal noise is given as:

$$\overline{V^2_{n,in-tot}} = \overline{V^2_{n,1/f-tot}} + \overline{V^2_{nin,T-tot}} \tag{30}$$

Due to cascoding of the load for the differential pair, $\overline{V^2_{n,T}}$ has a smaller value in compare to the differential pair without cascoding load. The usage of cascode load and weak-inversion operation, reduces the overall input noise figure for the comparator. The input noise simulation for the comparator is shown in Figure 14, for an input source resistance of 100 kΩ and an input capacitance of 20 pF. From the figure, one can see $\frac{1}{f}$ noise figure is very low which is 170 nV/$\sqrt{\text{Hz}}$ at 100 Hz frequency.

The SR is also dependent on the region of operation. The slew rate is given by:

$$SR = \frac{4\pi I_{Ds}}{g_m}\cdot GBW \tag{31}$$

where GBW is the gain bandwidth. Now for weak inversion region $\frac{I_{Ds}}{g_m}=\frac{nkT}{q}$, hence Equation (31) can be written as:

$$SR = 4\pi\left(\frac{nkT}{q}\right)\cdot GBW \tag{32}$$

Hence, if the GBW is kept constant, the SR for weak inversion is only dependent on the temperature T.

The differential pair M7 and M8 is divided into four parallel transistors and each of them are arranged in a common centroid layout to avoid the effect of mismatches due to temperature or oxide gradients. The current mirrors and bias circuits are also constructed by using dummy transistors to reduce the effect of mismatches. The usage of the sub-threshold operation helps to reduce the offset voltage value and the overall power consumption. For typical cases at a nominal temperature (T = 27 °C), the comparator has a sensitivity of 8 µV and for human body temperature (37 °C) the offset is at 10 µV. Some of the key figure-of-merits for the comparator is listed in Table 4.

Table 4. Important parameters of the comparator as obtained from the simulation.

Parameters	Value
Input offset voltage	8 µVat nominal condition
Bandwidth	132 kHz
Gain margin	121.9 dB at 132 kHz
Slew rate	3.6 V/µs @ 27 °C
Propagation delay	20 ns
Input noise voltage	120 nV/$\sqrt{\text{Hz}}$ at 100 kHz
CMR	101.1 dB
Power consumption	252 nW
Layout area	0.0064 mm^2

ADC Capacitive array

The capacitor array for the ADC can be implemented in a different manner, for example, the works [64,67] have a split architecture with two separate DACs. The work [65] implements the DAC array with differential capacitor networks, which are composed of 10-bit split schemes along with an additional sampling capacitor. The work presented in [62] uses a segmented binary weighted capacitor DAC. In this case, a charge redistribution type DAC is used with a binary weighted capacitor array [58,59,61,65].

Physically the capacitor arrays are manufactured by using unit metal, i.e., two top metal layers in MIM (metal-dielectric-metal) capacitors which reduce the effect of fringe capacitances to a considerable extent. This because of capacitance, in general, is inversely proportional to the distance in between the parallel plates. Hence, considering the dielectric constants and the overall area are kept constant, the capacitance value will be reduced as the distance between the metal layers and the substrate increases.

In a conventional switching scheme of SAR ADC, a lot of energy gets lost in charging and discharging the capacitors as also mentioned in [57]. Also, the energy required to charge and discharge a capacitor is directly proportional to the value of the unit capacitor used. The value of the unit capacitor largely depends on the thermal noise and the mismatch where the later plays a dominant role. A detailed discussion regarding the nominal value of the unit capacitor and the standard deviation due to mismatch is provided in the works [61,68–70]. The matching of a MIM capacitor can be given as:

$$\sigma\left(\frac{\triangle C}{C}\right) = \frac{K_\sigma}{\sqrt{A_C}} \tag{33}$$

where $\sigma\left(\frac{\triangle C}{C}\right)$ is the standard deviation of the capacitor mismatch, K_σ is the matching coefficient and A_C is the capacitor area. Further it can be simplified for the standard deviation $\sigma(C)$ for a single capacitor:

$$\sigma(C) = K_C \cdot K_\sigma \cdot \sqrt{\frac{A_C}{2}} \tag{34}$$

In the CMOS process used here, the MIM capacitor has a density of 1.23 fF/µm^2 and a matching of 1%. Keeping this in consideration, the value of the unit capacitor chosen is 4 fF with a dimension of 1.86 µm × 1.86 µm. A test structure for the characterization of small metal fringe capacitances is discussed in detail in [71]. An offset capacitor C_{offset} is included so as to set the entire voltage range of conversion which also depends on the accuracy of the comparator. Each of the bits is represented by a capacitor value starting from 2N to 2(N-1) where 'N' denotes the number of bits. For the LSB (least significant bit), the number of the unit capacitor is 1 and for the MSB (most significant bit) it is 4096. Each capacitor has a driver stage S_{2N} which is again controlled by the bit value. This reduces the effect

of variation in line impedance [49] which in this case is same for each capacitor as shown in Figure 13. The total capacitance C_{total} value is 16.36 pF and as the VDDI is 1.2V the range of ΔVDAC:

$$\triangle VDAC = (VDDI) \cdot \left(\frac{C_{total}}{C_{total} + C_{offset}} \right) \tag{35}$$

$$C_{total} = \sum_{N=1}^{12} C_{(N-1)} \tag{36}$$

where the voltage range lies in between 1.06 V (max) and 150 mV (min). The equivalent digital value can be calculated by using the following relationship:

$$ADC_N = \left[\frac{V_{ana} - V_L}{(V_H - V_L)} \right] \cdot \left(2^N - 1 \right) \tag{37}$$

where V_{ana} is the value of the analog input signal, V_H = 1.06 V, V_L = 150 mV and N = 1 to 12.

Only mismatch consideration for the unit capacitors is not enough; a common centroid layout is required for the capacitive array to avoid the consequence of the temperature or the process gradients. A considerable insight, into the DAC layout strategy for mismatches, is provided in [72]. Most of the designs use a full centroid layout, as in [57]. In this case, a partial centroid layout is used as shown in Figure 15 which is similar to the layout presented in [61]. The bit 0 to 6 and bit 7 are constructed without centroid layout, whereas bit 8 to bit 11 are constructed by using centroid layout. All the rows in the layout are constructed symmetrically including the offset capacitors by using the bit 7 as the unit cell. In this way, the total area for the capacitor array can be kept around 8.75% of the complete chip area. Dummy capacitors are provided to maintain the same environment for all the capacitors and the capacitor units are isolated from each other by using guard rings.

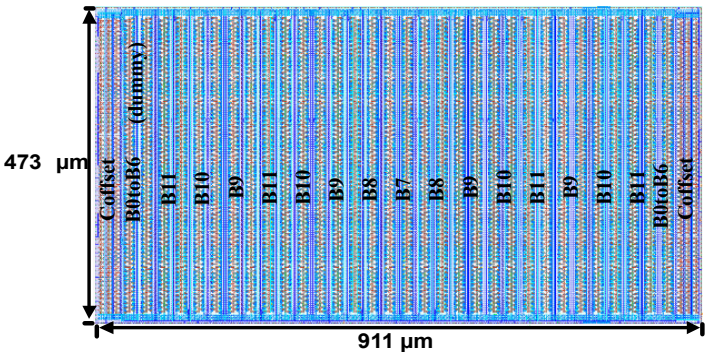


Figure 15. Partial centroid layout of the ADC capacitive array.

Post layout simulation is done after parasitic extraction in order to realize the effect of the parasitics on the design. The complete input range of the ADC is 903 mV, the theoretical value of LSB is 220 µV which is smaller than the one proposed in [57]. The effective resolution of the comparator is 8 µV without any mismatches, which is almost 28 times smaller than the LSB. The differential non linearity (DNL) and integral non linearity (INL) is simulated with a sinusoidal signal of 50 mV peak-to-peak close to the Nyquist frequency (3.3 kHz) and the sampling rate used is 6.6 kHz. The simulated INL is +0.62/−0.56 LSB and simulated DNL is +0.5/−0.68 LSB.

From the knowledge of DNL the signal-to-noise-ratio due to quantization can be estimated by:

$$SNR_{Q+DNL} = 6.02N - 9.03 - 10\log_{10}\left(\frac{1}{12} + \frac{DNL^2}{2\lambda^2} \right) \tag{38}$$

where N is the number of bits for the ADC and λ is the threshold value in the Gaussian probability function. For N = 12, λ = 3.0 and DNL = −0.68LSB, $SNR_{Q+DNL} = 72.83$ dB. From this the effective number of bits (ENOB) can be calculated by using the formula:

$$ENOB = \frac{SNR_{Q+DNL}\,(dB) - 1.76\,(dB)}{6.02\,(dB/bit)} \tag{39}$$

which gives a value of $ENOB = 11.80$. The estimated value for Spurious-free-dynamic-range (SFDR) is 76.4 dB which is obtained from the knowledge of INL by using the relation $SFDR = 20\log_{10}\left(2^N/INL\right)$.

4.3. Power Consumption Distribution of the Analog Part

The RFID/NFC communication and power management unit consumes 48.8 µW. The sensor readout unit consumes 543 µW which make a total power consumption of 592 µW for the analog block. Figure 16 shows the power consumption, distribution for the analog block. In the power management unit, the majority of the power is consumed by LDO1 = 15.3 µW, LDO2 = 7.6 µW and bandgap reference circuit = 5.1 µW. The communication circuit consumes 16.1 µW, the field detector and the clock regenerator consumes 1.8 µW and 2.9 µW respectively. In the sensor readout unit, the most of the power is consumed by the PGA = 363 µW and Virtual ground generator = 172 µW. Other than that, the power consumption for the bias generator is 7.8 µW and that of the ADC module which includes the comparator, DAC and sampling switch is 310 nW.

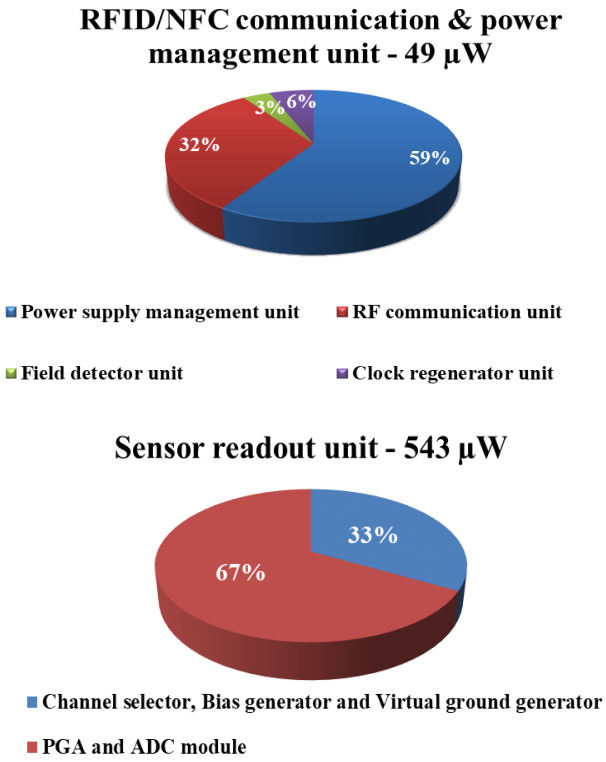


Figure 16. Power consumption distribution of the analog block.

4.4. Digital Design

Figure 17 shows the digital architecture of the proposed SoC which consists of a 32-bit microcontroller core (SIRIUS JANUS 2.0), memory cells (RAM and ROM) and other peripherals. The field on/off signal generated by the field detector circuit is used as the reset for all the digital peripherals including the microcontroller.

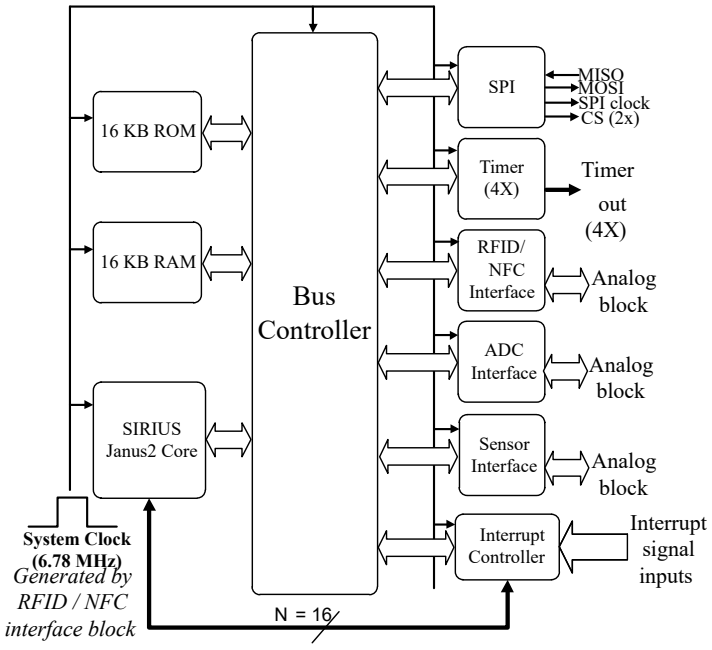


Figure 17. System level block diagram of the digital block for GAPSIC.

The microcontroller used here is developed by the ASIC design center at Hochschule Offenburg, based on the Von Neumann architecture proposed in [73,74]. Since then, further modifications have been carried out over the years, and the present version has been the one presented in [75]. It has a 16-bit data bus and a 32-bit address bus and the arithmetic and logical operations are based on Reduced Instruction Set Computing (RISC). The microcontroller is designed to operate at a frequency of 50 MHz, for this SoC it operates at a much lower frequency of 6.78 MHz. Slower clock frequency has two-fold advantages: firstly no internal PLL (Phase locked loop) is required which otherwise would have occupied 12.5% extra area; secondly, the slower clock frequency ensures that overall power consumption of the digital part remains low - which is already discussed in Section 3.

The SPI (serial peripheral interface) is used to communicate with the external memory device like a flash or a FRAM, where the application firmware is kept stored which is uploaded into the internal RAM of the SoC. The standard SPI signals used are MISO (Master input slave output), MOSI (Master output slave input), SPI clock and two CS (chip select) outputs. The maximum SPI clock frequency is $\frac{1}{5^{th}}$ of the system clock. One of the chip select is by default set for selecting the external memory device while the other chip select is free to be used for another SPI device.

There are four timers available, out of which two are dedicated to the internal operation and two are left free to be used by the application firmware if required. One of the internal timers is used by the bootup routine, and the other one is used by the RFID/NFC interface block.

The RFID/NFC interface consists of the digital logic required to extract the message from the demodulated signal and subsequently preparing the response.

The ADC interface consists of the SAR logic, ADC clock pre-scaler, data registers and control registers. The SAR logic consists of the binary logic required for the measurement in successive approximation. The SAR logic consists of shift registers which enable each bit starting from the MSB synchronized with the ADC clock. The ADC has a maximum conversion rate of 96 kbps and a sampling rate of 6.6 kHz; further, it can either be operated in single or continuous conversion mode. At the end of a conversion cycle, an interrupt signal is generated. The interrupt signal is then synchronized with the system clock, to avoid the asynchronous operation. The result of the ADC conversion is stored in two eight bit data registers, one for MSB and the other one for LSB values.

The ROM contains the initial bootup process, which includes a hardware initialization routine required to make the SoC functional and an SPI routine. The SPI routine initiates the SPI communication in between the SoC and the external memory device, as it loads the application specific firmware from the external memory device into the internal RAM. The ROM also contains a UID (unique identification) for the SoC which can be read by using the RFID or NFC communication protocol. This is also part of the initialization check for the system, which assures the integrity of the hardware and the internal memory of the system.

4.5. Duty Cycle of Operation

Figure 18 shows a brief overview of the complete duty cycle of operation involved in a measurement process in case a single ADC conversion mode is activated. The boot-up sequence requires the maximum duty cycle, which is nearly 75%. The sensor readout unit which consumes the maximum power in the analog part is only active for approximately 5% of the entire duty cycle.

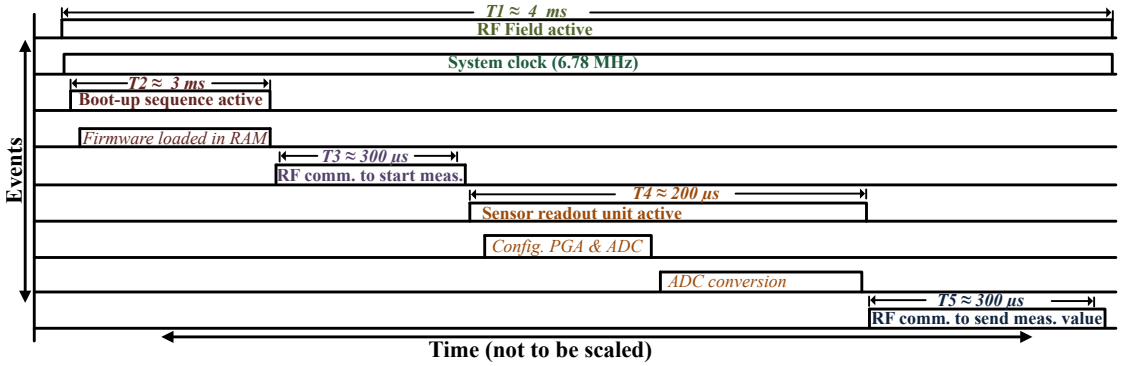


Figure 18. Brief overview of the timing sequence and hence the duty cycle for different events involved in a measurement process, considering only single ADC conversion mode is activated. Note: Config.—Configuration; comm.—communication; meas.—measurement.

5. Complete Layout of the SoC

Figure 19 shows the complete layout of the system. The power circuitries like the rectifiers, over-voltage protection, and the LDOs are kept away from the sensitive circuits like that of the PGA or the SAR ADC comparator. The RFID/NFC energy harvesting and management block are kept isolated from the sensor interface and SAR ADC block by using guard rings. Similar isolation is also provided in between the analog and the digital blocks. For all the input signals of the sensor interface part, shielding is provided for noise immunity. The bond pads are placed right on the pin cells, which saves nearly 30for the analog and the digital part are kept isolated from each other. Some of the critical design detail for the digital layout are included in Table 5.

Table 5. Design detail of the digital layout.

Parameters	Values
Total load capacitance of the clock tree	50 fF
Rise/fall delay	2 ps
Total standard cell area	0.516 mm^2
Total I/O pad cell area	0.126 mm^2
Total number of instances	35,573
Total number of nets	17,194
Total number of standard cells	35,209
Total I/O pad cell number	541

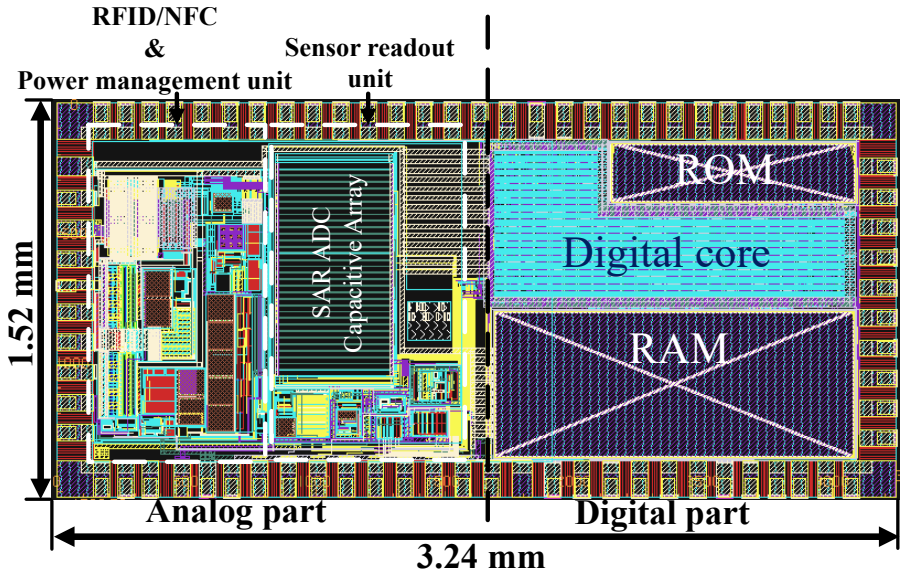


Figure 19. Computer aided design (CAD) view of the complete layout of the SoC.

6. Functional Verification and Testing

The RFID/NFC communication and power management unit is realized as a stand-alone chip and is tested for full functionality. The power rectifier of the power supply and management unit has a measured power conversion efficiency of 45% (max) for a load of 1 kΩ.The communication unit is designed in conformation to the ISO 15693/NFC 5 standard. The overall power consumption of the standalone chip is 107 µW which is least in comparison to some other state-of-the-art ICs [30–32,76,77].

For the sensor readout unit, post layout mixed signal simulation is done to test the full functionalities.

To test the compatibility between the analog and the digital part, an FPGA (Field Programmable Gate Array) evaluation board is used which is marked as 'SIRIUS eval board' in Figure 20. The evaluation board is further interfaced with the analog circuit interface board designed using discrete components. The analog circuit interface board consists of RFID/NFC communication unit, sensor interface unit and ADC. A post-layout simulation is carried out with the extracted netlist for the digital part after the final layout is accomplished. For the post-layout simulation, internal RAM and ROM and the external SPI flash device containing the application firmware is included to test the real-time functionalities. Table 6 gives an overview of the complete design of the SoC.

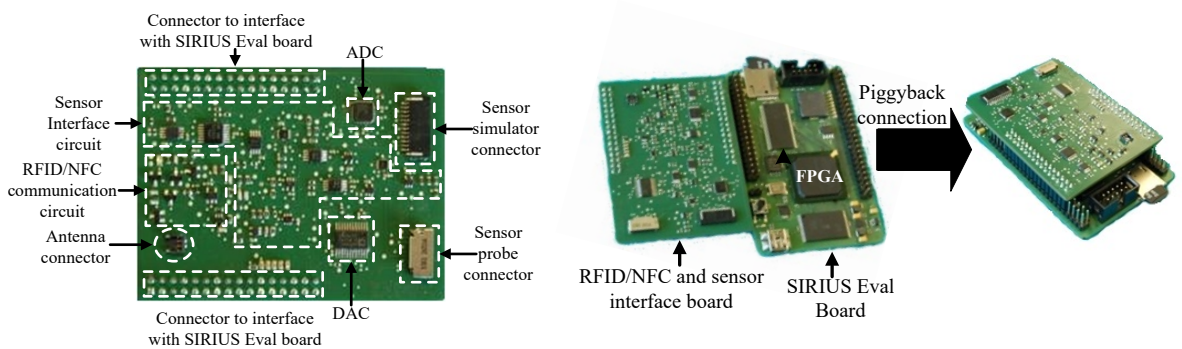


Figure 20. Left hand side: RFID/NFC communication and sensor readout board is shown. Right hand side: The SIRIUS evaluation board together with the interface board.

To the best knowledge of the authors, an exactly similar SoC is unavailable for comparison which possesses all the features discussed in this paper. Table 7 presents a comparative view of

the related works in this field. The work presented in [10] is an NFC enabled SoC which uses the communication protocol of ISO 15693 standard. The application area of the SoC is limited to glucose sensor measurement. A very similar application type SoC is discussed in [12] , but is incompatible with RFID/NFC communication protocol, besides it does not include an integrated microcontroller. Nevertheless, values presented by other works in the table are measured, while in this work only simulation values are presented.

Table 6. SoC—Key design parameters.

Parameters	Values
Energy source	Inductive coupling, Passive
Carrier frequency	13.56 MHz
Communication protocol	ISO 15693, NFC 5
Modulation type and index	ASK 10% NRZ
Data rate (max)	26.48 kbps
Supply (analog)	1.2 V
Supply (digital)	1.4 V to 1.8 V
Analog power (min)	51 µW
Analog power (max)	594 µW
Integrated microcontroller	32-bit, RISC 0.309 CoreMark/MHz
ADC	12-bit SAR ADC
Operating temperature	−30 °C to 85 °C
Technology	CMOS 0.18 µm
Die Area	4.92 mm^2 including pads
Type of external sensors	Temperature, ECG electrodes, Pressure sensor

Table 7. Comparison with related works.

Parameters	This work *	[10]	[12]	[13]
CMOS Tech.	0.18 µm	0.6 µm	0.35 µm	0.13 µm
Energy source	Passive	Passive	Solar/RF powered	TEG/RF power
Communication	13.56 MHz	13.56 MHz	OOK/403 MHz	402/403 MHz
Protocol	ISO 15693, NFC 5	ISO 15693		
Supply (analog)	1.2 V	NA	1.8 V	30 mV
Supply (digital)	1.4 V to 1.8 V	2.85 V	NA	NA
Integ. µC	32-bit RISC	No	No	8-bit RISC
ADC	12-bit SAR ADC	11-bit sigma delta ADC	10-bit SAR ADC	8-bit SAR ADC
Power (min)	49 µW(analog)	NA	226.3 µW	NA
Power (max)	592 µW(analog)	250 µW	942.9 µW	19 µW
Die Area	4.92 mm^2 including pads	9.98 mm^2	11.25 mm^2	25 mm^2 including pads
Application	Temperature, pressure and ECG measurement	Glucose sensor measurement	Temperature, glucose, protein concentration and pH value	ECG/EMG/EEG measurement

Note: NA indicates not Available; µC is microcontroller; * indicates simulation value; TEG—Thermoelectric Generator; RF—Radio Frequency.

The particular advantage of the SoC is that it is programmable. The firmware can be customized; the PGA and the SAR ADC can be reconfigured based on the application specific requirement. The supply voltage is in the range of 1.4 V–1.8 V. This makes it compatible with commercially available external devices like temperature or pressure sensors or external memory devices like Flash or FRAM. A JTAG (joint test action group) boundary scan is included, for on-chip debugging. The sensor readout part is only activated whenever it is required to make a measurement otherwise, it is kept isolated from the power supply, this reduces the static power consumption.

Next step is the comprehensive functional tests of the SoC after fabrication and the implementation of the proposed blood pressure monitoring implant. In this respect, the present research work includes a selection of the antenna design and the pressure sensor which is suitable to operate in the human body environment. The complete mechanical construction and biocompatible encapsulation of the implant are part of the future research.

7. Conclusions

A low power mixed-signal passive programmable SoC is presented in this paper. The design is implemented in a 0.18 µm CMOS technology, on a die area of 1.52 mm × 3.24 mm—which includes the pads. The analog front-end consists of circuitries required for RFID/NFC communication and sensor readout. The digital part consists of a 32-bit RISC microcontroller along with other digital peripherals. The SoC has 16 KB of RAM and ROM as internal memory devices. It is a passive SoC which uses inductive coupling to power the entire sensor tags developed using the SoC. It uses a carrier frequency of 13.56 MHz in compliance with ISO 15693 or NFC5 standard. The complete integration of the microcontroller along with the analog part for communication and sensor readout is useful for small size, low cost, and low power sensor applications. The application area can be a temperature measurement for industrial applications or a bioimplant to measure blood pressure or ECG. The complete measurement of the chip after fabrication and realization of the proposed implant discussed in the paper is part of the future work.

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