# Design Validation of a Single Semiconductor-based Marx-generator Stage for fast step-wise Arbitrary Output Waveforms

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*Abstract*—A new modular pulsed power source with fast rise time and step-wise arbitrary output waveform generation is currently under development to drive the GESA device investigated at IHM. Acknowledging the complex design procedures necessary to set up a modular pulsed power source for voltages of up to 120 kV, this paper focuses on the circuit design for a single stage and its validation prior to generator assembly. Using a semiconductor-based Marx generator topology, the stages are designed to have an output voltage of 1 kV with a pulse current of up to 600 A. When connected to an ohmic load, the measured current rise times are in the order of 46 ns resulting in current rise rates of up to 10 kA/µs using commercial devices. The step-wise arbitrary output waveform is created by generating the switching commands on the stage using a microprocessor and a fast optical synchronization unit. Effective stage shielding is verified by operating the stage in a 100 kV, 2.5 kA EMI test bed. The paper presents the design considerations and corresponding measurements.

*Index Terms*—Marx generators, Insulated Gate Bipolar Transistors, Power semiconductor devices, Pulse circuits, Pulse power systems, Pulse shaping circuits, Optical fiber communication

## I. INTRODUCTION

**T**HE pulsed electron beam device (GESA) has been used for many years to study the application of intense electron beams for altering metal surface properties such as surface hardness and corrosion resistance [1]. As electron source, the device uses a multipoint explosive emission cathode, requiring a voltage rise rate of the driving pulse generator in the order of 100 kV/100 ns [2]. The typical pulse parameters are: 120 kV output voltage (negative with respect to ground) at pulse currents between 200 A and 600 A for pulse lengths of up to 100 µs in single pulse operation [3]. New experiments concerning the plasma stability additionally demand the output voltage to be adjustable during the pulse.

Active pulse shaping by using modular pulsed power sources is state-of-the-art and can be achieved using Linear Transformer Driver (LTD) [4] or Marx generator [5], [6] topologies. Considering the long pulse length (100 µs) and high currents (600 A), Marx generators are preferable to avoid the resulting high core volumes in LTDs. Additionally, Marx generators can be used to drive capacitive as well as inductive loads [7]. While other researchers (see [8], [9]) control the switching signal generation by a control unit on ground potential, the

generator presented in this paper uses a microprocessor unit on each stage to generate its switching signal directly on the stage, thereby simplifying the control circuitry.

As for any modular pulsed power source, the design of the respective stages has to be tailored to the specific application. Due to the substantial financial investment associated with building a new pulsed power generator, it is of great interest to test individual stages and to validate the design requirements before setting up a generator assembly. This paper presents the most important aspects of the circuit design used in the new generator, namely:

1) Selection and driving of fast pulse switches.
2) Development of fast and cost-efficient optical trigger circuitry.
3) Low inductance capacitor layout of the stage.
4) Reliable microprocessor function in a harsh EMI (Electro-magnetic Interference) environment.

The paper concludes with pulse measurements confirming the proper function of one stage at maximum pulse parameters.

## II. STAGE DESIGN

### A. Generator schematic

The modular design of the semiconductor-based Marx generator under development consists of several stages, each equipped with a pulse capacitor C, a switching element T and a freewheeling diode D. Fig. 1 shows the simplified schematic. All capacitors are charged in a parallel configuration (charging path not shown) and upon closing the switching elements, the capacitors are connected in a series configuration, leading to a voltage multiplication at the output. Due to the freewheeling diodes, not all switching elements have to be switched on simultaneously, as the load current can by-pass inactive stages. This enables full temporal control over the output voltage $V_n(t)$ of a n-stage generator applied to load impedance $Z_L$, which can be derived using equation 1 from the current capacitor voltage $V_{C,a}(t)$ of stage a and its corresponding switching function $T_a(t)$ ($T_a$ = 1: switching element $T_a$ closed; $T_a$ = 0: switching element $T_a$ open) [10].

$$V_n(t) = -\sum_{a=1}^{n} V_{C,a}(t) \cdot T_a(t) \qquad (1)$$

The simplified circuit design compared to other topologies [7] uses only one active pulse switch per stage but is, as a result, only able to deliver a unipolar output voltage. In this
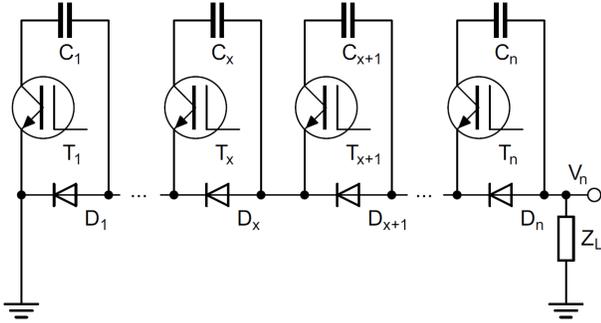
Fig. 1: Simplified schematic of a unipolar semiconductor-based Marx-generator, consisting of n stages, each comprising a switching element T, a pulse capacitor C and a freewheeling diode D. The output voltage $V_n$ is applied to the load impedance $Z_L$.

design, each stage is equipped with a microprocessor handling the communication with a central control unit. The desired switching function $T_a(t)$ is uploaded to the microprocessor and is started synchronized. After synchronized pulse start, no communication is necessary during the pulse. Additionally, each stage is equipped with a Complex Programmable Logic Device (CPLD) for implementing fast safety relevant turn-off functions. Both, microprocessor and CPLD, run at 100 MHz clock speed. On the one hand this greatly simplifies the control circuitry, since no communication is necessary during the pulse, on the other hand the increased circuit complexity may be vulnerable to EMI. The limited clock speed gives rise to a trigger jitter in the order of 10 ns. Synchronization of all stages at the beginning of the pulse is ensured using a fast optical synchronization unit.

*B. Switching elements*

For achieving a fast rise time of the final generator, using fast switching elements is key. Whereas Insulated Gate Bipolar Transistors (IGBT) are slower than Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET), they are considered more cost-efficient with respect to switching power [11]. By using a gate-boosting circuit [12], we enable the use of originally slow rise time IGBTs in fast pulse circuits. The gate drive circuit as presented in [12] allows for an increase in switching speed by a factor of 8 for certain devices, thereby enabling pulse bursts in the MHz range with current rise rates in the order of 4 kA/µs for cost-efficient commercial devices. To cope with the current amplitudes of up to 600 A, the design uses six IGBTs (NGTB40N120) in a parallel configuration per stage, each capable of carrying up to 320 A maximum current [13]. The freewheeling diodes (C4D10120D) as seen in Fig. 1 can be considered passive switches, as they carry the pulse current once the IGBT is turned off. For active pulse shaping, it is necessary for the IGBT to be able to turn on, while the diode is carrying the pulse current. Therefore, it is crucial to use Schottky diodes at this point. The turn-on of the IGBT would otherwise lead to a transient short circuit of the stage during the reverse recovery time of a pn-junction diode. Due to the high current rise time of the IGBT and the low inductance

layout of the stage, the resulting high current would inevitably damage IGBT and diode.

*C. Stage capacitors*

The required pulse length of 100 µs at pulse currents up to 600 A necessitates the use of large stage capacitances to minimize voltage droop during the pulse caused by the continuous discharge of the capacitors. Other researchers successfully employ special pulse shaping stages in the generator [14] for compensating the voltage droop, however, they introduce additional inductance in the circuit. Another way is to subsequently activate spare stages throughout the pulse once the output voltage has dropped by the charging voltage of one stage. In comparison to using very large stage capacitances to limit the voltage droop, the overall capacitance can be drastically reduced with this scheme [15]. Beside fast switching elements, using low Equivalent Series Inductance (ESL) capacitors and low inductance traces for connecting them to the switching elements is essential for fast current rise times. Additionally, any leakage inductance in the capacitors or their leads will cause an inductive voltage overshoot at the switching element during turn-off, necessitating snubber [16] or active clamping [17] circuits. The required stage capacitance for the given parameters is in the order of 200 µF. In that capacitance range, commercially available, cost-efficient capacitors feature parasitic inductances in the order of several 10 nH [18], which will demand snubber circuits to protect the switching elements and will slow down the current rise rate. To overcome this limitation, the presented design features a combination of two high value capacitors with high leakage inductance (944U101K122ACM, 100 µF, 40 nH) in combination with four low value capacitors with very low leakage inductance (WIMA MKP10, 1 µF, approx. 4 nH). Fig. 2 presents the equivalent circuit of the arrangement, where the stage capacitance C is comprised of $C_1$ representing the parallel connection of two 100 µF capacitors (leakage inductance $L_1$) and $C_2$ representing the parallel connection of four 1 µF capacitors (leakage inductance $L_2$). The smaller, low inductance capacitors ensure on the one hand a fast current rise due to their low inductance and on the other hand serve as snubber capacitors as the energy stored in $L_1$ is transferred to $C_2$ during turn-off. For an efficient arrangement, $L_2$ has to be minimized for fast turn-on and minimal inductive voltage stress on the switching element, whereas $L_1$ has to be minimized to avoid charge oscillations between the capacitors.

Fig. 3 illustrates one Marx-generator stage with the pulse capacitors. To keep the parasitic lead inductance at a low level, the capacitors are connected to the switching elements using broadside Printed Circuit Board (PCB) traces (traces for forward and return current on adjacent layers to minimize the inductance) over the whole width of the board. Given the dimensions of the PCB of width w = 10 cm, length l = 13 cm and a board thickness of t = 1.5 mm, the additional wiring inductance can be calculated using Grover's formulas [19] to L = 1.6 nH. The switching elements therefore are arranged along the short side of this trace. The low-inductance capacitors are connected directly through the traces, whereas the
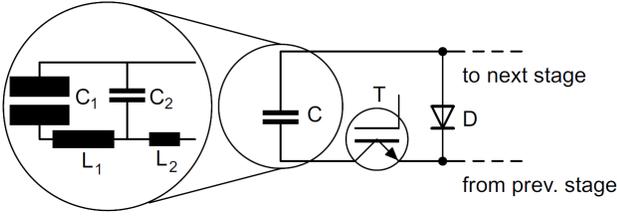
Fig. 2: The capacitor arrangement of one stage. The stage capacitance C consists of $C_1$, a big capacitor with a high leakage inductance $L_1$ and $C_2$, a small capacitor with a low leakage inductance $L_2$. The combination allows for a fast current rise and low inductive voltage overshoot during turn-off.

high-inductance capacitors are placed towards the end of the board due to space limitations. The mechanic decoupling as well as a low-inductive connection is achieved by connecting the capacitors to the board by means of high surface area contact springs.



(a) Side view.



(b) Top view.

Fig. 3: Photo of the presented Marx-generator stage. The switching elements and the capacitors are connected via broadside traces across the whole PCB width.

As an example, Fig. 4 shows the voltage across the switching element (black trace) during one pulse. For the measurement, a stage was operated in a low-inductance test circuit (see Sec. III-A) at 1 kV charging voltage and 600 A pulse current into ohmic load. During the fast turn-off ($t_{f,I}$ = 67 ns, resulting in a current fall rate of dI/dt = −7 kA/μs), only a marginal over-voltage below 1060 V is measurable across the switching element - proving that the low inductance capacitors act as efficient snubbers. However, due to the resonance circuit formed by $C_2$ and $L_1$, charge oscillations occur between the two capacitors. This can be observed as slight voltage oscillations across the switching element after turn-off. Simulating the circuit according to Fig. 2 in SPICE (Fig. 4, red trace) shows a reasonable agreement for parasitic inductance values of 30 nH

for the parallel connection of two 100 μF capacitors ($L_1$) and 1 nH for the parallel connection of four 1 μF capacitors ($L_2$). Damping was introduced in the simulation to account for ohmic loss, dielectric loss, magnetic loss and radiated loss. The resonance frequency of the resulting circuit is around 470 kHz. In order to prevent excitation of the resonance circuit near the resonance frequency, the maximum switching frequency will be limited by software to below 400 kHz in the final version of the generator, whereas a maximum switching frequency of 500 kHz is possible (see Sec. III-C). These charge oscillations may be a concern at high repetition rates, however, their additional stress on the capacitors can be neglected in single pulse operation.
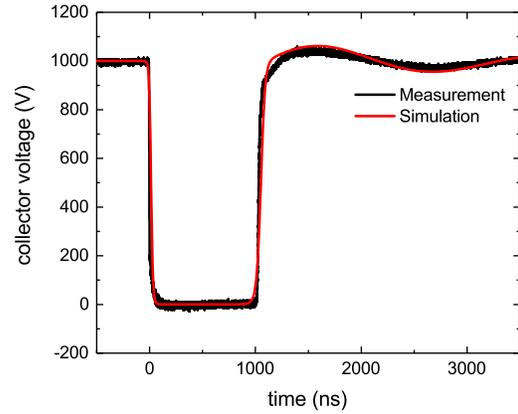


Fig. 4: Comparison between measurement (black trace) and simulation (red trace) of collector-emitter voltage across the switching element during a short pulse. After turn-off, charge oscillations occur between the stage capacitors are visible. There is no significant voltage over-shoot during turn-off.

### D. Optical signal transmission

The fast rise time requirement of the generator demands for a good synchronization of all stages. While it is possible to achieve synchronized switching by means of inductive switching signal distribution [20], the design described in this paper features an optical synchronization. Thereby, stray capacitances to ground can be reduced [7] and isolation issues at high output voltages are omitted. Due to the fast rise time requirement, a synchronization of the stages with a jitter of around 10 ns is necessary. In order to avoid additional jitter caused by the recognition of the optical synchronization signal, a fast optical rise time is important. Commercial solutions for high band-width transmission are available, however, they often require DC-balanced data transmission [21] and, hence, are not suitable for transmitting a single fast rise time synchronization pulse. For a reliable communication, the design presented in this paper uses commercial LED housings (HFBR-2526Z) for secure connection of the optical fiber and easy mechanical assembly. The limiting factor of the turn-on delay in LEDs is the charging process of the junction capacitance [22], which can be limited by biasing the LED close to its knee-voltage.

High LED drive currents generally shorten the optical rise and fall times [22], whereas a negative voltage after the pulse extracts excess minority carriers from the junction to further reduce the turn-off delay. The latter can be achieved by using a peaking network parallel (RC combinations, tuned for the respective device) to the current limiting resistor in series to the LED when driving it with a voltage source. The resulting optical output pulse can be seen in Fig. 5. The optical signal exhibits a slight overshoot due to the peaking network but has an optical rise time of 3.2 ns and an optical fall time of 3.0 ns. As receiver we use a commercial combination of photo diode and pre-amplifier (HFBR-1527Z) with typical electrical rise and fall times of 3.3 ns. The associated jitter has been determined by measurements to be less than 1 ns and, hence, is sufficiently small for the intended application.
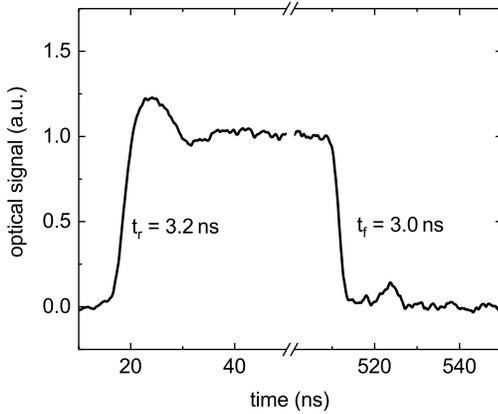
Fig. 5: Optical output signal of the designed LED drive circuitry using a fast current-feedback amplifier to achieve an optical rise time of 3.2 ns and an optical fall time of 3.0 ns.

*E. EMI shielding*

Due to the fast high voltage transients and related pulsed currents in the application, the design of the stages has to be very EMI robust. To test the stages prior to the generator assembly, one stage was equipped with a floating power supply and was connected to the output of a spark-gap based Marx-generator. The generator was able to supply a total output voltage of approximately $-100$ kV with respect to ground at a load current of up to 2.5 kA, thereby simulating the EMI levels of the final generator. Connecting the stage's local ground plane to the output of the generator and passing the load current in close vicinity to the stage, this test setup could verify the stages robustness against the following EMI sources:

1) Capacitive coupling: The steep voltage rise of the stage with respect to ground quickly charges parasitic capacitances.
2) Magnetic coupling: The fast rise time load current may induce currents into the circuitry.
3) Radiated EMI: The employed spark-gaps feature a broadband interference spectrum [23].

As especially the analogue signals on the stage are susceptible to EMI, the stage was programmed to transmit its clock signal as long as the optical receivers do not (falsely) receive a signal. Thereby it was possible to monitor the optical receivers and the clock signal at the same time. The test results are displayed in Fig. 6. The upper graph shows the output of the generator; the lower graph shows the recorded optical signal from the stage. For the unshielded measurement (Fig. 6), the recorded clock signal fails with the start of the Marx generator erection, indicating a false recognition of an optical input signal. When the load current is increasing, the clock signal is slowed down and does speed up again after the peak current. This variation in clock speed hints towards an interference in the (analogue) microprocessor clock generator using an external quartz causing a disturbance in the internal PLL. Whereas this effect has not been investigated in detail, it is obvious that deviations in clock speed are not acceptable - especially since the stage timing is performed using the clock reference.
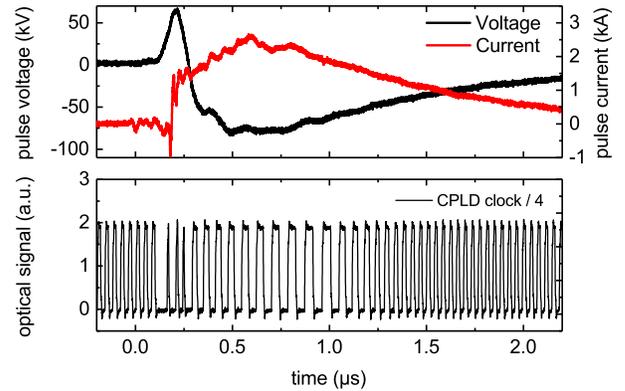
Fig. 6:
Upper graph: Output voltage (black trace) and output current (red trace) of the conventional Marx-generator to which the stage-under-test was connected.
Lower graph: Transmitted divided clock signal.
When the Marx-generator is erecting, a false optical recognition occurs as there is no more signal from the stage. Afterwards the clock signal returns with varying speed, indicating a clock generator failure.

For a robust stage design, hence, shielding is inevitable. The designed copper housing is pictured in Fig. 7. It is a box, closed on 5 sides, in which the PCB can be inserted and is connected to circuit ground. Thereby, capacitive and radiated coupling can be strongly reduced, as the sensitive circuit parts are shielded from the electric field when inside the box. Magnetic shielding is achieved for the x axis (aligned with the long side of the PCB). As the magnetic field can penetrate - up to the skin depth - into the material, the thickness of the copper housing was chosen to be thick enough for the maximum designed pulse length of 100 µs. At a resulting frequency f = 5 kHz the calculated skin depth $\delta$ according to Eq. 2 for copper with a resistivity of $\rho = 1.6 \times 10^{-8}\,\Omega\,m$

and a permeability of $\mu = 1$ is $0.922\,\text{mm}$, hence, the copper thickness was chosen to be $1\,\text{mm}$.

$$\delta = \sqrt{\frac{\rho}{\pi \cdot f \cdot \mu}} \qquad (2)$$

To further reduce capacitive and radiated coupling via the open side as well as to reduce magnetic coupling for the y-axis parallel to the short side of the PCB (compensating current $I_y$, yellow, in Fig. 7) and the z-axis perpendicular to the PCB ($I_z$, blue), a copper block is mounted onto the PCB to electrically seal the housing once the PCB is inserted. The electrical contact from copper block to copper housing is established via $CuBe_2$ contact springs. Thereby, the currents as depicted in Fig. 7 are not limited to faces of the box but can flow around the whole volume. Additionally, signal traces from the inside of the housing to the outside are filtered by PI-filters consisting of two capacitors and a ferrite bead. The switching elements themselves are inside of the housing as the fast gate signals cannot be filtered effectively. The voltage gradients occurring at the device leads of the switching elements are in the order of $1\,\text{kV}/10\,\text{ns}$ have proven not to cause any issues for the circuit. Additionally, the microprocessor and the CPLD are shielded by a SMD shielding cabinet (see photo Fig. 3b). The effectiveness of the proposed shielding can be seen in Fig. 8, as there are no disturbances in the clock signal as well as no false recognition concerning the optical receivers during the firing of the external Marx generator.
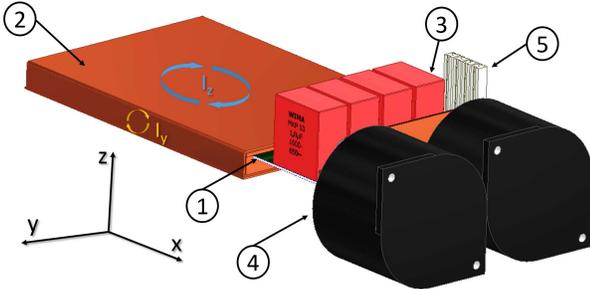


Fig. 7: The shielded stage corresponding to the measurement in Fig. 8. The PCB (1, compare Fig. 3) is inserted in a closed copper housing (2) and the open side is sealed by a copper block mounted onto the PCB. $I_z$ represents the induced current compensating magnetic field in z-direction, whereas $I_y$ compensates magnetic field in y-direction. As discussed in Sec. II-C, the stage pulse capacitance is a combination of low inductance capacitors (3) and high capacitance capacitors (4). For safety reasons, each stage features discharge resistors (5).

## III. Pulse Measurements

### A. Pulse circuit

In order to benchmark the stages switching behavior, the stage was operated in a low-inductive pulse circuit up to the designed output voltage of 1kV with different loads. The pulse circuit schematic can be seen in Fig. 9, with C being the stage capacitance as described in Sec. II-C, T representing the switching elements (six parallel-connected $1.2\,\text{kV}$ IGBTs NGTB40N120 - see Sec. II-B), the freewheeling diodes D
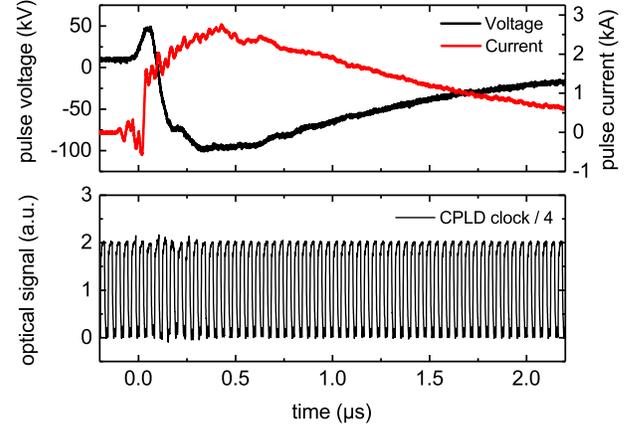


Fig. 8:
Upper graph: Output voltage (black trace) and output current (red trace) of the conventional Marx-generator to which the stage-under-test was connected.
Lower graph: Transmitted divided clock signal of one stage with proper shielding.
As can be seen, the transmitted signal is not influenced by the external Marx-generator, proving the efficiency of the shielding.

(three parallel-connected $1.2\,\text{kV}$ SiC Diodes C4D10120D) and the load resistor $R_L$. For a low inductive arrangement, the load resistor consists of several solid carbon resistors able to handle the pulse energy. The voltage V was measured directly across the switching elements using a fast high voltage probe (Philips PM8932) with a rise time of $1.2\,\text{ns}$, whereas the load current I was measured using a fast shunt resistor with a bandwidth of nearly $1\,\text{GHz}$ [24]. The circuit and
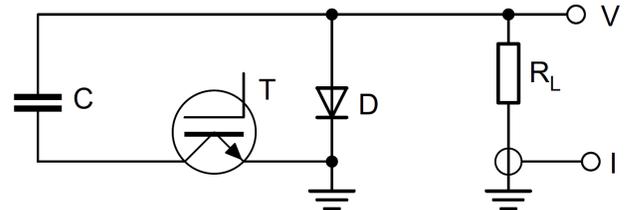


Fig. 9: One stage (Switching element T, Stage capacitor C and free-wheeling diode D) in a low inductive pulse circuit with ohmic load $R_L$. Voltage V is measured directly over the switching element, the load current I is measured by means of a shunt resistor.

the acquired rise times have to be seen as benchmark test for the switching behavior of one stage only. In the final generator assembly, the rise time of the generator will be determined by the rise time of the stages, the total inductance of the circuit and the stray capacitance towards ground. For all following measurements, one stage was operated in the complete control chain, including a preliminary PC interface and the control board on ground potential. The switching sequence was generated by the microprocessor on the stage.

## B. Fast rise time measurements

Fig. 10 shows a 1 µs pulse of the stage at nominal charging voltage of 1 kV and maximum peak current of 600 A. All following rise and fall times were calculated using the 10 % to 90 % definition. As can be seen, the voltage fall time (26 ns, red trace) is still faster than the current rise time (46 ns, black trace), indicating a inductive component in the load. With a load resistance of 1.66 Ω and a current rise time $\tau$ = 46 ns, the residual inductance in the pulse circuit can be calculated to 76 nH according to Eq. 3.

$$\tau = \frac{L}{R} \tag{3}$$

The calculated inductance value hereby includes the complete circuit, including capacitor connections, switching element, load resistor, shunt resistor and associated wiring leakage inductance. The current rise rate as calculated from the measure-
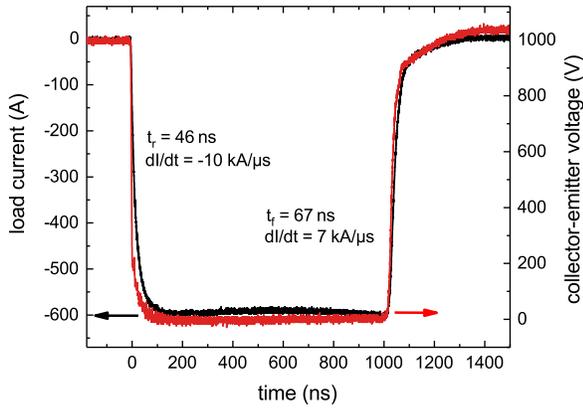


Fig. 10: Load current (black trace) and collector-emitter voltage (red trace) across the switching element at nominal charging voltage of 1 kV and 1.66 Ω load resistance - resulting in a current rise time of 46 ns for 600 A load current.

ment is approx. −10 kA/µs during turn-on and 7 kA/µs during turn-off. For the final generator assembly, these measurements confirm that the stage design is able to deliver a fast-rise time output pulse at nominal amplitudes (1 kV, 600 A). By surpassing the defined 100 ns rise time requirement for the whole generator by a factor of two, the stage design leaves enough room for an increase in rise time due to imperfect synchronization of stages and additional circuit inductance and stray capacitance in the generator assembly.

## C. Arbitrary switching sequence

Beside the fast rise time, the stage is capable of an arbitrary switching sequence. As example, Fig. 11 shows 500 kHz switching with 50 % duty cycle of the stage at nominal charging voltage of 1 kV and a load current of 250 A. The switching sequence is created during the pulse without interaction with the control circuitry by the microprocessor on the stage. The measurement thereby proves the stage's capability of creating very fast switching sequences in order to meet the demand for the generator assembly to deliver arbitrary output waveforms.
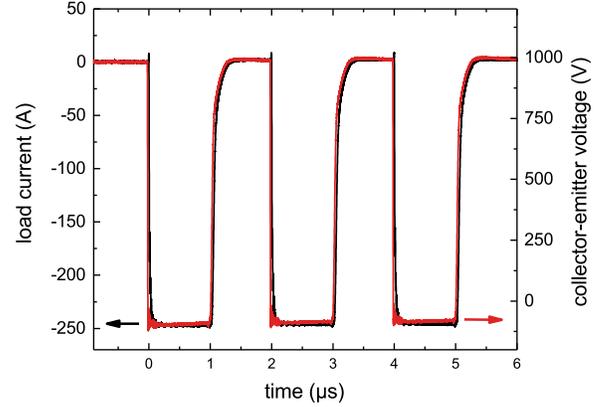


Fig. 11: Load current (black trace) and collector-emitter voltage (red trace) across the switching element at nominal charging voltage of 1 kV and 4 Ω load resistance - to demonstrate the arbitrary switching sequence generation, the graph shows 500 kHz switching with 50 % duty cycle.

## IV. CONCLUSION

The requirements of new experiments on the GESA device investigated at IHM, KIT lead to the development of a new fast rise time semiconductor-based Marx generator with step-wise arbitrary output voltage as driving pulsed power source. The paper describes design aspects of individual stages necessary to comply with these challenging requirements. As switching elements, the stages use IGBTs featuring a gate-boosting circuit. A low inductance capacitor layout is achieved by the combination of two capacitor types, omitting the requirement for a snubber circuit under regular operating conditions. For synchronous triggering, the paper presents an optical trigger unit capable of optical rise and fall times of around 3 ns. The efficiency of a shielding against fast high voltage and current transients has been proven by measurements on a stage connected to a 100 kV, 2.5 kA pulse circuit. The design was verified in experiments showing current rise times of 46 ns for 600 A load current, resulting in current rise rates of up to 10 kA/µs. Arbitrary switching signal generation was demonstrated by burst-mode switching sequences with 500 kHz.
The experiments validated the design of one stage and a small-scale generator is currently being set up.

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