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Test-beam results of a SOI pixel-detector prototype☆

Roma Bugiel [a,*], Szymon Bugiel [a], Dominik Dannheim [b], Adrian Fiergolski [b], Daniel Hynds [b], Marek Idzik [a], Piotr Kapusta [d], Wojciech Kucewicz [c], Ruth Magdalena Munker [b,1], Andreas Nürnberg [b,2]

[a] Faculty of Physics and Applied Computer Science, AGH University of Science and Technology, Al. Mickiewicza 30, Krakow, Poland
[b] European Organization for Nuclear Research (CERN), CH-1211 Geneva 23, Switzerland
[c] Faculty of Computer Science, Electronics and Telecommunications, AGH University of Science and Technology, Al. Mickiewicza 30, Krakow, Poland
[d] The Henryk Niewodniczanski Institute of Nuclear Physics, Polish Academy of Sciences, Krakow, Poland

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ABSTRACT

This paper presents the test-beam results of a monolithic pixel-detector prototype fabricated in 200nm Silicon-On-Insulator (SOI) CMOS technology. The SOI detector was tested at the CERN SPS H6 beam line. The detector is fabricated on a 500 μm thick high-resistivity float-zone n-type (FZ-n) wafer. The pixel size is 30 μm × 30 μm and its readout uses a source-follower configuration. The test-beam data are analysed in order to compute the spatial resolution and detector efficiency. The analysis chain includes pedestal and noise calculation, cluster reconstruction, as well as alignment and η-correction for non-linear charge sharing. The results show a spatial resolution of about 4.3 μm.

1. Introduction

A high-precision position measurement is required for vertex and tracking detectors at future linear colliders with a resolution of about 3 μm for the vertex detector and 7 μm for the tracking detector. To limit multiple scattering, such measurements have to be done using very low detector material thickness corresponding to about 0.1 to 0.2% of a radiation length per single detector layer in the innermost region. Monolithic silicon detectors fit very well to these requirements, because of their potential for fine segmentation (down to a few μm) and possibility to thickness reduction (down to 50 μm). In comparison to most hybrid pixel detector, there is no need for mechanical bump-bonding of sensor and readout electronics, such that smaller pixels and less complex detector systems can be produced.

The Silicon-On-Insulator (SOI) CMOS implements a SiO_2 insulator (BOX - buried oxide) between a thick high-resistivity substrate and a thin low-resistivity silicon layer. Such a structure provides the possibility to fabricate a monolithic pixel-detector with a sensor matrix on the substrate and readout electronics above the BOX in an thin outer silicon layer. The separated sensor layer has the particular advantage that it can be fully depleted. The SOI CMOS process allows also to implement a full set of standard CMOS circuitry. The scheme of an SOI structure working as a particle detector is shown in Fig. 1.

The SOI CMOS, implemented in a very thin silicon layer, is highly resistant to Single Event Effects (SEE) and latch-ups, which is a big advantage in comparison to standard CMOS processes for applications in radiation environments [1].

The recent results of pixel detectors implemented in 200 nm Lapis SOI technology [2] show that this particular process seems to be a very good candidate for detectors on future linear colliders, since the benefits provided by the SOI technology allows to fulfil demanding requirements of space and time resolution. Systems in SOI technology combine monolithic pixel detector advantages among with the high signal from a fully depleted structures as in hybrid detectors. Also the backgate effect, that seemed to be a main problem of SOI process, is solved by implementation of a doping region called Buried P(N)-Well (BP(N)W) under the BOX [3].

Therefore, the strong suit of the proposed project is the used technology and the presented prototype is treated as a first test version for future solutions dedicated for CLIC vertex/tracking detectors.

In this paper, the test-beam results and laser measurements of an SOI pixel-detector prototype fabricated in Lapis 0.2 μm SOI CMOS

☆ This work was carried out in the framework of the CLICdp collaboration.

* Corresponding author.
E-mail address: roma.dasgupta@cern.ch (R. Bugiel).

[1] Also University of Bonn, Bonn, Germany.

[2] Present address: Institut für Experimentelle Teilchenphysik, Karlsruhe Institute of Technology, 76131 Karlsruhe, Germany.

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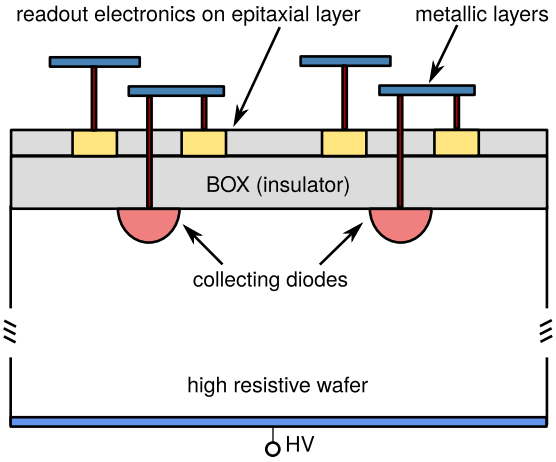


Fig. 1. Scheme of an SOI CMOS structure working as a particle detector.

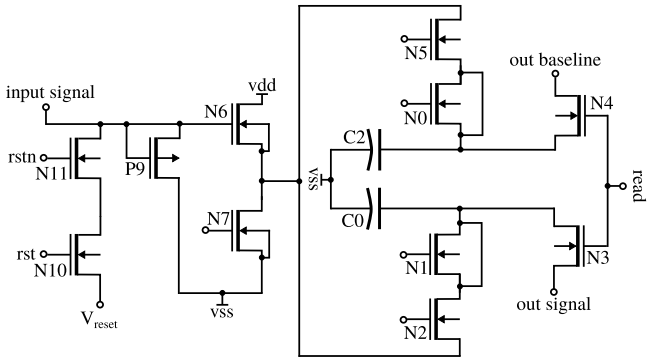


Fig. 2. Simplified scheme of the pixel front-end electronics. The *vdd* and *vss* are power supply voltages and *rst*, *rstn* and *read* are digital signals for controlling the reset phase and reading of the pixel.

technology are presented. Section 2 gives a brief description of the detector design, including matrix layout and pixel architecture. Section 3 presents experimental setup as well as the data acquisition (DAQ) system used during the beam tests. The analysis chain and basic detector performance are described in Section 4. Spatial resolution and the detector efficiency calculations are reported in Section 5. The final section summarizes the results.

2. Sensor design

2.1. Matrix layout

The sensor matrix follows the design of a previously described chip [4]. The whole matrix contains 8 × 36 integrating-type pixels with pixel pitch of 30 μm × 30 μm each. The pixel readout is based on a source-follower configuration. The matrix is further divided into eleven smaller submatrices (4 × 6 or 8 × 6 pixels) with the same pixel architecture but slightly different sensor layouts and transistor sizes. Splitting the matrix into submatrices was performed in order to identify optimal pixel-circuit parameters in terms of noise and floating body effects. In this work the detailed submatrices description is skipped, because the test-beam data analysis is not performed for each submatrix separately. The reason for this is that the collected data sets were not large enough to perform independent analysis for single submatrix. However, the matrix splitting issue is mentioned to explain the patterns occurring on the noise and gain maps presented in Section 4.2.

2.2. Pixel front-end

Each pixel comprises the front-end electronics shown in Fig. 2. The input signal charge integrated on the input capacitance results in a voltage rise on the gate of the Source Follower N6, loaded with a sample-and-hold (SH) circuit built of the capacitors C0 and C2 and the charge compensated NMOS gates N2 and N5. The voltage samples are taken at the beginning and at the end of the integration period and then the difference of this two voltages comprises output signal of the pixel. Such processing may be considered as a Correlated Double Sampling (CDS) filtering with a very long time constant. During the readout phase, C0 and C2 are connected to the differential column amplifier through the gates N3 and N4. Each integration period is followed by a short reset phase, during which the collected charge is removed via the charge compensated N10 gate. The P9 PMOS protects the input gate of N6 against negative voltage levels. The Buried P-Well layer implanted around the central pixel contact protects the electronics against the back-gate effect and results with the pixel capacitance of about 15 fF. Thus, the Minimum Ionizing Particle (MIP) signal has a amplitude of a few hundred mV.

2.3. Readout scheme

The 8 × 36 matrix operates continuously in a rolling-shutter mode sending out serially, row by row, analogue signals stored in the pixel memory, to an external 12-bit sampling analogue-to-digital converter (ADC). The charge integration time is determined by the clock frequency. Reset signal and clock are the only signals controlling the sensor operation.

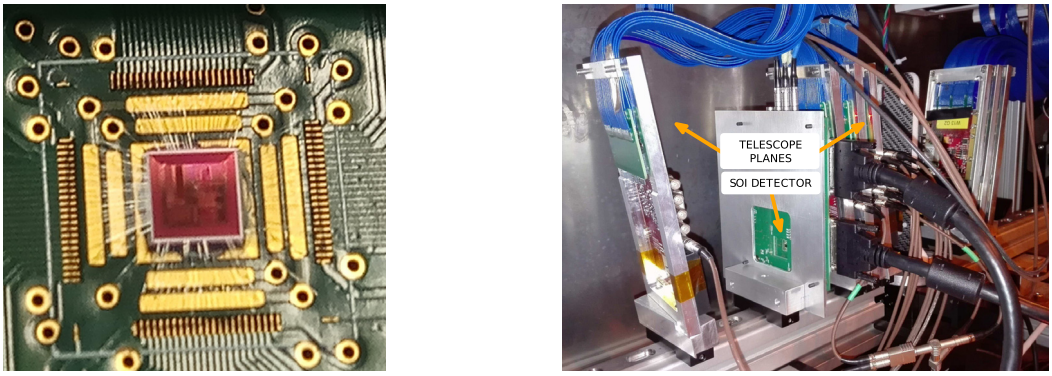
In each row, the start of the integration period $T_{\mathrm{int}} \sim 120$ μs is shifted with respect to the previous row by the time: $T_{\mathrm{int}}/N_{\mathrm{rows}}$. Thus, a pixel cluster resulting from a particle hit can be divided among two consecutive frames. Since the position of the hit is derived from charge sharing between the pixels, the clusters affected by row resetting might introduce in the worst case two hits (instead of one) both with distorted space position. In the analysed data sets there are about 1% of events that recorded a hit in two consecutive frames. Because this sample could contain reset-affected clusters, this class of events was discarded.

Another rolling-shutter feature is related to the periodic pixel resets. The integration cycles in each row (and in the whole matrix) last for 792 cycles of the 5.68 MHz clock. Out of these, six cycles are used for the reset and CDS sampling. The relevant probability that the hit arrived during this period is about 0.76%. The average observed cluster size in y (perpendicular to the resetting direction) is about 2.5 pixel, so the fraction of affected clusters is around 2%. Removal of such events is not possible.

3. Experimental setup and DAQ

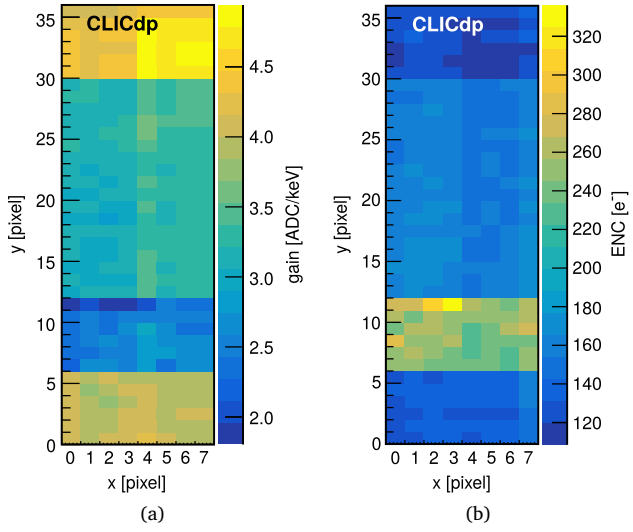
The SOI detector depicted in Fig. 3(a) was tested in summer 2016 in the SPS H6 beam line at CERN. A high-resolution telescope based on Timepix3 pixel sensors [5] provided a reference measurement during the beam tests [6]. The expected tracking resolution of the telescope at the Device Under Test (DUT) position was about 2 μm. A pion beam with an energy of 120 GeV was used. The DUT in the telescope box is shown in Fig. 3(b).

The detector was placed on a mezzanine board that was assembled on a dedicated readout board containing a 12-bit external ADC. This system was connected to a Genesys Virtex-5 FPGA (Field-Programmable Gate Array) Board via two 68-bit wide VHDCI (Very-High-Density Cable Interconnect) cables. The FPGA read and buffered data frames, and sent them via Ethernet to a computer.



(a) (b)

Fig. 3. The photograph of the ASIC (application-specific integrated circuit) with a tested SOI prototype detector (a) and the test-beam setup (b). The structure of the telescope box is shown with seven reference detector planes and the tested detector prototype.



(a) (b)

Fig. 4. The gain (a) and the pixel Equivalent Noise Charge (b). The visible patterns have an origin in slightly different pixel types (the same architecture but various transistor sizes and pixel layouts).

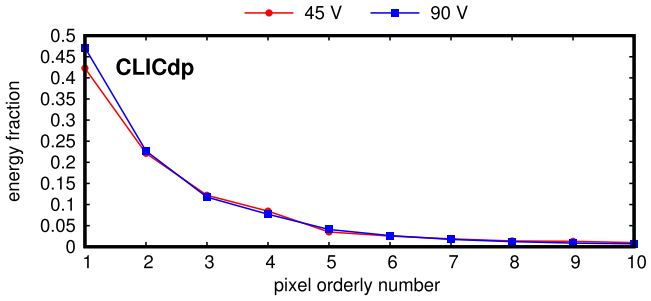


Fig. 5. Fractional signal of pixels within a cluster for two different back bias voltages. The pixels on the x-axis are numbered from the highest to the lowest carried signal. On the y-axis the average fraction of the carried cluster energy is shown.

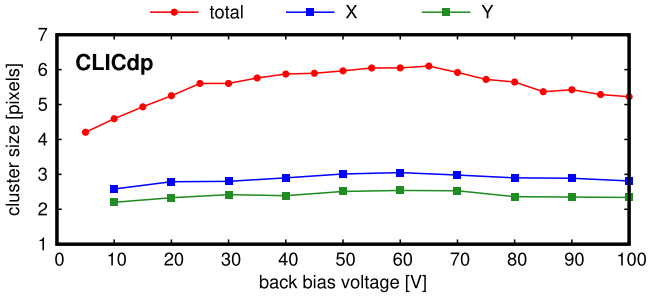


Fig. 6. Total, x and y cluster size versus back bias voltage.

4. Basic detector performance

4.1. Analysis chain

The reference tracks from the telescope have been reconstructed in Marlin (Modular Analysis and Reconstruction for the LINear collider) framework while the actual analysis has been implemented in standalone software developed for the SOI detector prototype. In order to build an event, hits from the SOI detector need to be associated with tracks from the telescope. For this reason the SOI detector and the telescope used the same time stamping clock and the signal resetting time counters.

The analysis flow performed for the hit reconstruction from the SOI detector is as follows. In a first step the pedestal and noise for each pixel are calculated. Then, the cluster is reconstructed if the SOI detector recorded a signal from the particle. After that the basic device performance is studied, analysing beam particle energy spectra, signal-to-noise ratio (SNR) and full depletion depth. The last step in the analysis chain concerns hit position calculation as well as the spatial resolution and efficiency estimation.

4.2. Pixel gain and noise

As it was mentioned before, the source-followers matrix is built of different submatrices. The pixels differ with transistor sizes and layouts. This may cause a distortion of the hit position, when the cluster is at the border between the submatrices. To alleviate this issue, a gain correction for each submatrix is applied. The gain calibration is done by measuring the response of each pixel to the 6 keV K_α peak of a Fe^{55} radioactive source. In Fig. 4(a) the gain factors for the whole matrix are shown. The gain correction is applied to each pixel.

The Equivalent Noise Charge (ENC) distribution of the pixel matrix is presented in Fig. 4(b). At full depletion the ENC varies from 120 e^- to 320 e^- per pixel, depending on the submatrix architecture. Commonly reported ENC levels of SOI detectors are in a range of 30 e^- to 100 e^- [7–9], while the lowest values are obtained at low temperatures.

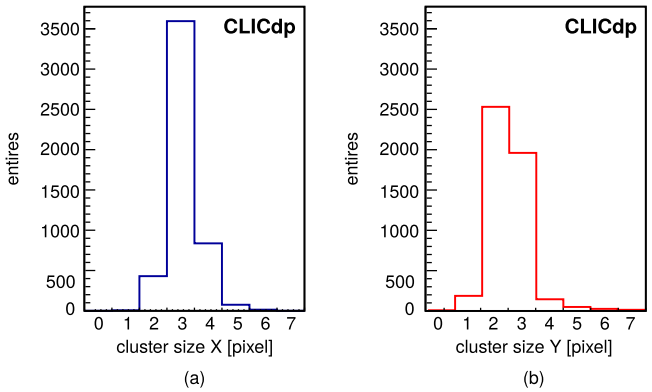


Fig. 7. Histogram of cluster size in x (a) and y (b) at 90 V back bias voltage. The mean cluster size is 2.9 and 2.5 pixels in y.

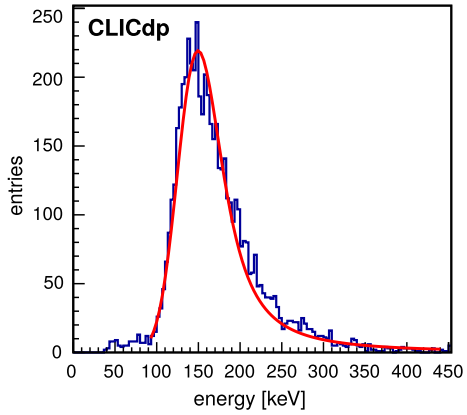


Fig. 8. Spectrum of energies deposited by 120 GeV beam particles; 90 V back bias voltage.

The comparably high noise level measured in the beam tests can be attributed to two principal causes: the small size of the sensor and temperature effects. Since the sensor matrix is small, a large fraction of pixels is situated in the vicinity of the matrix border, where negative effects related to a discontinuity of the sensing diode layer are observed. Also, a common mode filtering could not be applied as efficiently as in large matrices. Concerning the second point of high noise sources, it is well known, that SOI analogue circuits suffer from self-heating effects. The tested chip operated continuously at room temperature and no provisions for cooling existed.

4.3. Cluster reconstruction

To identify hits in the detector, cluster reconstruction is performed at the beginning of the analysis chain. The Two Seed Method (TSM) is used for this purpose. In a first step the seed pixel is determined. The signal s_i of the ith pixel is extracted as $s_i = r_i - p_i$, where r_i is the raw signal from the detector and p_i is its pedestal value. The threshold th_{seed} is defined with respect to the signal measured in units of the pixel noise σ_i. The pixel is taken as a seed when $s_i > th_{\text{seed}}$.

After finding a seed pixel the algorithm searches for neighbour pixels exceeding the second threshold where $th_{\text{seed}} \geq th_{\text{neighbour}}$. If a new neighbour pixel satisfying this condition is found, the algorithm repeats the search around it. The algorithm is completed, when no more pixels can be added. All found pixels build a cluster. If any of the pixels touches the border of the considered 8×36 matrix, the cluster is rejected in order to exclude events in which a fraction of a total cluster charge leaks outside the active area.

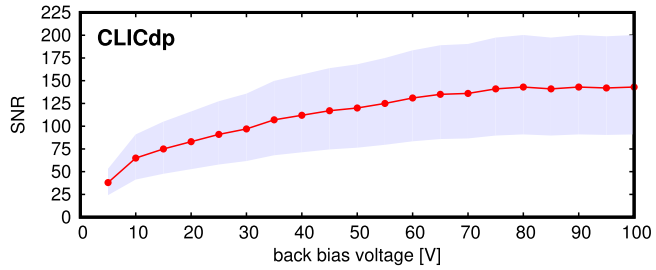


Fig. 9. Signal to noise ratio as function of back bias voltage. The red curve shows the average SNR for the whole matrix while the blue area shows the range of variations for different submatrices. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

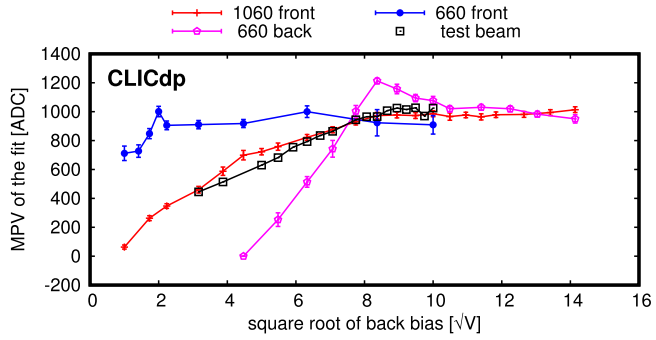


Fig. 10. The measurements of depletion depth using laser data and the test-beam data. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

As can be seen in Fig. 5, almost half of the cluster energy is stored in the pixel with the highest signal. Taking also into account that the SNR is around 100 (described in Section 4.4), $th_{\text{seed}} = 30\,\sigma_i$ is chosen for default condition during clusterization. Changing the th_{seed} in a wide range does not affect the detector spatial resolution. The second threshold is set to $th_{\text{neighbour}} = 4\,\sigma_i$. It is also verified that the results are not sensitive to small $th_{\text{neighbour}}$ changes ($th_{\text{neighbour}}$ equal $2\,\sigma_i$, $3\,\sigma_i$ and $4\,\sigma_i$ were tested).

In Fig. 6 the dependence of the mean cluster size in x, y, and the total cluster size as a function of the sensor back bias voltage is shown. The total cluster corresponds to number of all pixels building the cluster. The maximum cluster size is reached for a voltage of about 65 V, suggesting that full depletion is achieved around this value (discussed further in Section 4.5). Beyond this voltage, the total cluster size drops slightly, because the electric field is increasing and the charge diffusion is reduced.

Fig. 7 shows a histogram of the cluster size in x and in y at 90 V back bias voltage. The mean value is 2.9 pixels for x and 2.5 pixels for y. A higher mean cluster size in x is observed at all back bias voltages, as shown in Fig. 6. This may be connected to boundary effects (small and not square pixel matrix), to the asymmetries in matrix layout in the x and y direction, or due to remaining misalignment of the DUT with respect to the telescope.

4.4. Signal to noise ratio

The signal-to-noise ratio is estimated taking as a signal the most probable value (MPV) of the Landau-Gaussian convolution fit to the energy spectra of beam particles, for a given back bias voltage. The energy spectra are obtained from all pixels in the matrix and the example energy distribution taken for 90 V back bias voltage is shown in Fig. 8. To estimate the SNR, the MPV is divided by the mean RMS of the

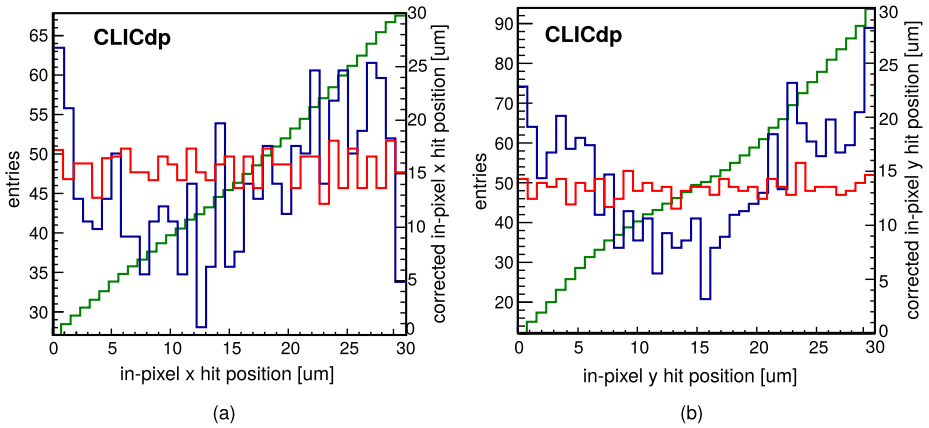


Fig. 11. In-pixel hit position distribution before (blue) and after (red) correction for x (a) and y (b) direction. The green curve shows the normalized cumulative function of the COG in-pixel hit distribution. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

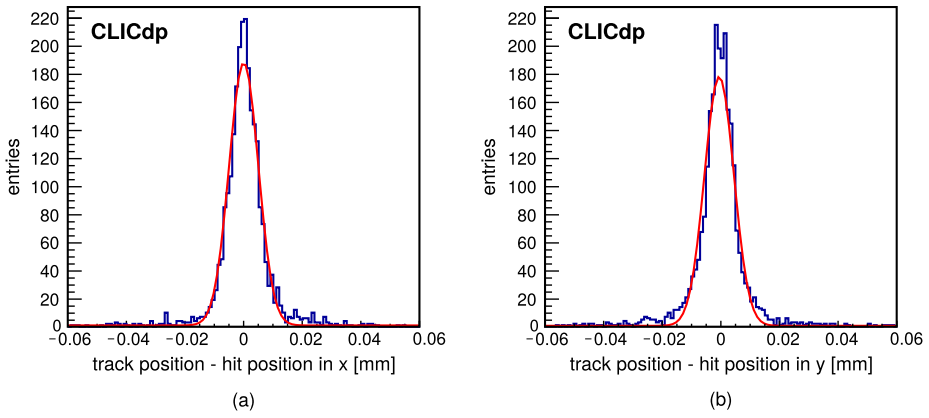


Fig. 12. The difference between track position and reconstructed DUT hit position in x (a) and in y (b) at 90 V back bias voltage. The σ of a Gaussian fit (red curve) for these distributions are (4.83 ± 0.12) μm for x and (4.92 ± 0.13) μm for y. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

pixel noise calculated over the whole matrix. The SNR as function of sensor bias voltage is presented in Fig. 9. Above 30 V the mean SNR exceeds 100. For a given sensor bias, large SNR variations are seen due to different noise performance of some submatrices.

4.5. Depletion depth

Knowing the energy spectrum of minimum ionizing particles for different back bias voltages one can find the depletion voltage of the detector. The substrate thickness for FZ(n) wafer is 500 μm. The MPV of a Landau fit as a function of the square root of the back bias voltage from the test-beam data is presented in Fig. 10 (black curve). For a planar sensor one expects a linear dependence until full depletion and a flat saturation after the full depletion is achieved. From the obtained results it may be concluded that the full depletion in the tested SOI prototype is achieved at around 70 V of back bias voltage ($\sqrt{70\,\mathrm{V}} = 8.3\ \sqrt{\mathrm{V}}$).

In addition to test-beam results, measurements of the SOI detector signal as a function of the square root of back bias voltage, obtained in the laboratory with 1060 nm and 660 nm lasers, are also presented in Fig. 10. The signal dependence on the sensor bias voltage for the 1060 nm laser, penetrating the whole sensor, and for the MIP should be similar, allowing to cross-check the results from the laboratory measurement and with the test-beam data. Both curves (black and red) in Fig. 10 saturate at around 70 V confirming that the full depletion is achieved at this bias voltage. For the 660 nm laser, a shallow deposition (with a penetration depth of 10 μm) is expected. Therefore, for front side illumination the signal saturates already at very low back bias voltage while for back side illumination the signal starts to grow rapidly and saturates only when the sensor is almost fully depleted.

Knowing the full depletion voltage allows to calculate the resistivity of the sensor wafer (ρ_d):

$$\rho_d = \frac{d^2}{2\epsilon\mu V_d}, \tag{1}$$

where d is the sensor thickness, μ - the majority carrier mobility, ϵ - the electric constant for silicon, and V_d - the full depletion voltage. The calculated resistivity of the float-zone n-type wafer used in the prototype SOI detector is around (12 ± 1) kΩ cm. The foundry did not specify the exact resistivity, but it declared that it is above 2 kΩ cm.

5. Measurement results: spatial resolution and efficiency

5.1. Alignment

As a alignment of the DUT with the telescope the x and y offset correction and a single rotation were done. The offset correction transfers the origin of the DUT coordinate system into telescope coordinate system. The rotation is made in the plane perpendicular to the beam direction and is obtained by optimizing (minimizing) the resolution as a function of rotation angle. Such a procedure is repeated for each data sets separately.

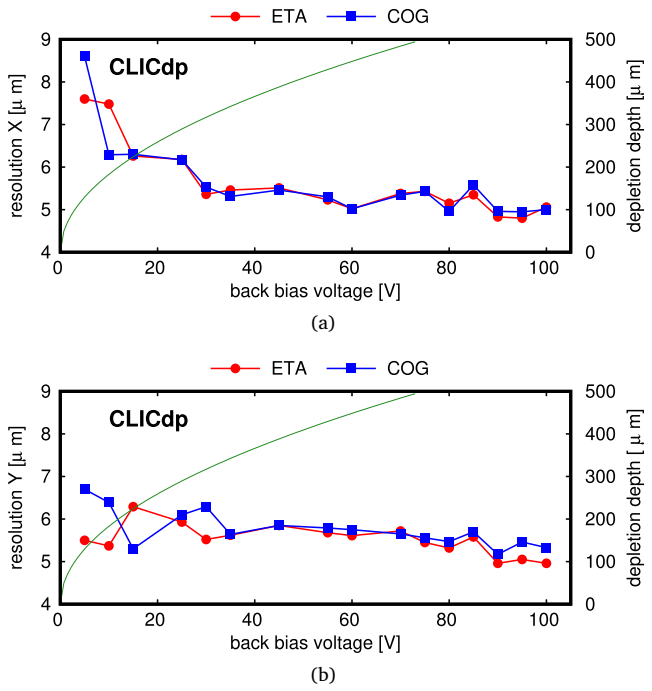


Fig. 13. The resolution in x (a) and y (b) before and after η-correction. In green the theoretical relation for depletion depth in function of back bias voltage is shown. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

5.2. Position reconstruction using COG method

After the cluster reconstruction and the alignment the DUT hit position is calculated using the Centre of Gravity (COG) method. For the x direction it is expressed as:

$$x_{\mathrm{COG}} = \frac{\sum_{i=0}^{N}(A_i \cdot x_i \cdot P) + \frac{P}{2}}{\sum_{i=0}^{N} A_i}, \tag{2}$$

where i is the pixel ordinal number, N - the number of pixels in cluster, A_i - the signal of i_{th} pixel, x_i - the position of i_{th} pixel, P - the pixel pitch. An important assumption in this method is that the charge collected by neighbouring pixels depends linearly on the distance to these pixels (smaller distance resulting in higher charge).

5.3. Eta correction

As the assumption of linear charge sharing between pixels is not realistic, COG-reconstructed hit position is not distributed uniformly along the pixel pitch. The measured in-pixel SOI hit distribution in the x and y coordinates obtained with the COG method is shown in Fig. 11 (in blue curve). To alleviate this issue, a so-called η-correction is commonly applied [10]. In the most basic approach the η-correction is done for two-pixel clusters. For the analysed data, the cluster size distribution is as shown in Fig. 7, so not only two-pixels cluster are reconstructed. Nevertheless, as the beam profile was much larger than the pixel pitch, the hit position distribution within the pixel pitch should be uniform. The η-correction procedure proposed in this analysis leads to uniforming the in-pixel hit position and is done as follows.

In a first step the integration of the COG in-pixel hit distribution is performed. The result of this procedure is the cumulative function $f(x)$ normalized to the pixel pitch which is shown in Fig. 11 (green curve). In the analysis, the cumulative function is used to obtain the position after η-correction ($f(x_0)$) for each measured DUT hit position (x_0).

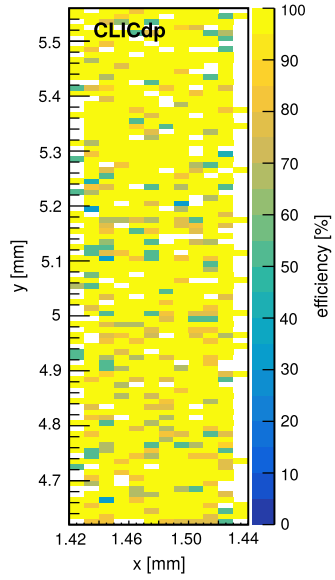


Fig. 14. The efficiency map for full SOI prototype matrix at 90 V. In green the theoretical relation for depletion depth in function of back bias voltage is shown. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

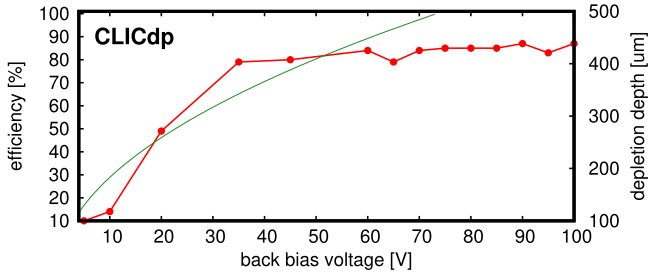


Fig. 15. An average efficiency versus back bias voltage.

After the η-correction a more uniform in-pixel hit distribution is obtained, as also shown in Fig. 11(red). The comparison between spatial resolution obtained with hit positions calculated with COG and after η-correction is presented in the next section.

5.4. Spatial resolution

The position of the hit reconstructed in the SOI sensor is compared with the one obtained from the telescope. The example distribution of the difference between the reconstructed particle position by the DUT and the reference track intersection in x and y direction is shown in Fig. 12. The DUT positions are after η-correction. The spatial resolution is calculated as the sigma of a Gaussian fit to the presented histogram. The fit is applied to the whole distribution.

The comparison of the spatial resolution in x and y direction as a function of the sensor bias voltage obtained before and after η-correction, is shown in Fig. 13. The theoretical depletion depth, calculated using Eq. (1), is also presented. The results obtained with and without the η-correction depend slightly on the sensor bias voltage. Using the η-correction gives either very similar or slightly better results (at high back bias voltages) than the COG position reconstruction method.

Fig. 13 shows that at full depletion the spatial resolution saturates around 5 μm. Taking into account the beam telescope resolution (around 2 μm at DUT point) one can estimate the SOI prototype resolution

to about (4.3 ± 0.1) μm. For a depletion thickness of about 100 μm (corresponding to about 5 V back bias voltage) that is compatible with the CLIC vertex and tracking detector requirements, the spatial resolution is measured to be approximately 6–7 μm, or 5.5–6.5 μm when subtracting the telescope resolution.

5.5. Detector efficiency

In the last analysis the efficiency of the prototype SOI detector is calculated. The detection efficiency is of primary interest by itself but it is also important to make sure that the sample of events used in the previous analyses is not biased.

It should be stressed that considerations presented in this section regard combined efficiency of the detector and the DAQ system. Unfortunately, there were some problems detected in the DAQ. They were mainly connected with an overflow of the memory, because DAQ was too slow to process incoming events. Also, pickup noise originating in the unshielded VHDCI connectors occasionally led to corrupted events. To limit this effects, parts of the data set with frequent acquisition problems were discarded, but this issue still affects efficiency.

The 2D efficiency histogram shown in Fig. 14 is created as a ratio of two particle hit maps. The first hit map contains particle positions from the telescope, for which a time-correlated SOI hit is reconstructed within 30 μm distance. The second hit map contains positions of all particles registered in the telescope. The efficiency map is the ratio between them. To estimate the average efficiency, the average of inner entries from Fig. 14 is taken. The bins at the border are rejected (corresponding to pixel pitch of 30 μm) to eliminate boundary effects. Fig. 15 shows the average efficiency versus back bias voltage. The observed efficiency of the SOI detector prototype is 87% when fully depleted.

6. Conclusions

This work presents the SOI prototype pixel-detector performance characterized with a laser test setup and in the CERN SPS test-beam. The detector was fabricated on a 500 μm thick high-resistivity float-zone n-type wafer which resistivity is estimated on about (12 ± 1) kΩ cm. The pixel size is 30×30 μm and it is based on source-followers architecture.

A spatial resolution of about (4.2 ± 0.1) μm is measured for the fully depleted sensor. Since the detector was not well adapted for the spatial resolution measurement, mainly because of the large influence of border effects, these results should be treated rather as a first conservative estimation for possibilities of future prototypes. The combined efficiency of tested detector and its readout system is found to be around 87%.

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