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# Test beam measurement of ams H35 HV-CMOS capacitively coupled pixel sensor prototypes with high-resistivity substrate



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# Test beam measurement of ams H35 HV-CMOS capacitively coupled pixel sensor prototypes with high-resistivity substrate

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Abstract: In the context of the studies of the ATLAS High Luminosity LHC programme, radiation tolerant pixel detectors in CMOS technologies are investigated. To evaluate the effects of substrate resistivity on CMOS sensor performance, the H35DEMO demonstrator, containing different diode and amplifier designs, was produced in ams H35 HV-CMOS technology using four different substrate resistivities spanning from 80 Ω cm to 1000 Ω cm. A glueing process using a high-precision flip-chip machine was developed in order to capacitively couple the sensors to FE-I4 Readout ASIC using a thin layer of epoxy glue with good uniformity over a large surface. The resulting assemblies were measured in beam test at the Fermilab Test Beam Facilities with 120 GeV protons and CERN SPS H8 beamline using 180 GeV pions. The in-time efficiency and tracking properties measured for the different sensor types are shown to be compatible with the ATLAS ITk requirements for its pixel sensors.

Keywords: Analogue electronic circuits; Electronic detector readout concepts (solid-state); Front-end electronics for detector readout; VLSI circuits

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## 1 Introduction

The new ATLAS inner detector for the High Luminosity LHC programme, called ITk, will require a large production of radiation tolerant pixel detectors in order to cover the large ITk surface area. CMOS technologies, where high-voltage and high-resistivity substrate can be used, represent a promising avenue to produce large number of low cost pixel detectors, taking advantage of the large scale industrial production facilities offered by the CMOS foundries. The high resistivity of the substrate, combined with the possibility to apply bias voltage larger than 120 V allows the creation of a large depletion zone within the sensor substrate with a drift field sufficient to generate fast and large enough signals both before and after the irradiation of the sensors.

Previous small prototypes, produced in multi-project wafer projects in ams h18 technology [1] using standard low-resistivity substrate have shown good tracking performances before and after irradiation using capacitive-coupling of the sensor to its readout electronics [2–6]. However, it was concluded that higher signal from high-resistivity substrate would contribute to a better timing and better radiation hardness.

To demonstrate the possibility of producing CMOS sensors using high-resistivity substrates, a prototype of large area CMOS sensor, the H35DEMO, was designed, for capacitive-coupling to a readout ASIC or standalone readout. This prototype was produced in an engineering run in ams h35 technology which first allowed the use of high-resistivity substrates. This prototype was assembled to readout ASICs using capacitive-coupling and studied in test beam campaigns to evaluate its tracking properties, measure the improvement in signal expected using higher resistivity substrate and demonstrate the feasibility of producing large area sensors of the order of $cm^2$ as required for

ATLAS ITk project. However, poor performances are expected from the ams h35 350*nm* technology after irradiation and the capacitively coupled prototypes were not design to withstand ATLAS ITk specifications in terms of radiation. They have therefore been characterised un-irradiated.

## 2 The H35DEMO demonstrator chip

The H35DEMO demonstrator chip [7] is a large size pixel sensor chip designed and produced in the ams H35 HV-CMOS technology using three types of high-resistivity substrates: 80 Ω cm, 200 Ω cm and 1000 Ω cm. The design, as seen in figure 1, includes four independent sub-matrices: the NMOS and CMOS monolithic matrices integrating sensor and readout electronics into the same die and the two analog matrices 1 and 2 designed for capacitive-coupling to the FE-I4 readout ASIC [8], in order to decouple readout electronics aspects from sensor diode properties. The monolithic matrices were tested before and after irradiation and demonstrated good performance of the readout circuitry required for the monolithic integration of CMOS pixel sensors in ams HV-CMOS technology [9, 10]. The pixels in the analog matrix, measuring 250 µm × 50 µm, contain a large collection diode in which the amplification circuitry is implemented. The amplified signal is then routed to an output pad matching the input of the FE-I4 ASIC in order to be detected and digitised. The large signal excursion of the amplifier allows for an efficient transmission of the signal through a small capacitor formed by a thin layer of glue between the H35DEMO and the FE-I4 pads. To achieve a good uniformity of the coupling between pixels over the whole matrix, a glueing process using high-precision flip-chip machine was developed and used.

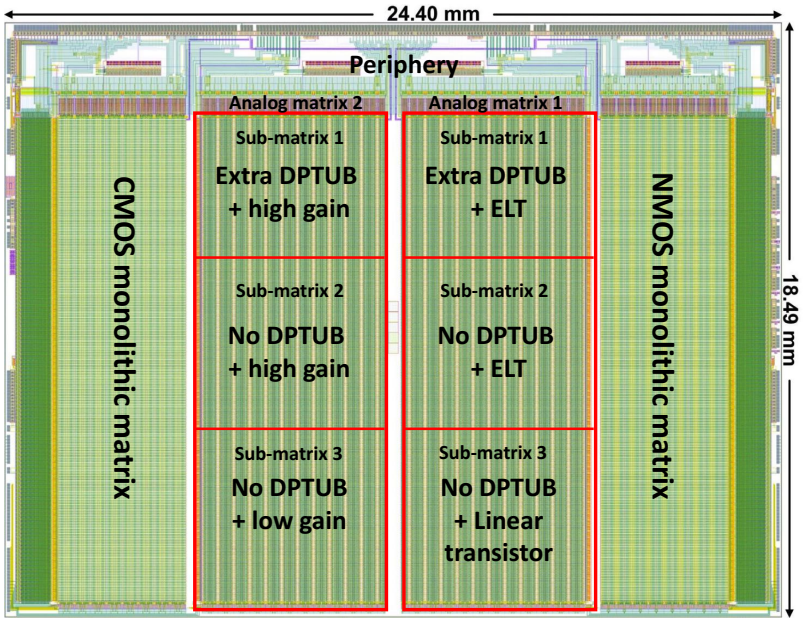


**Figure 1.** Floor plan of the H35DEMO demonstrator sensor. The monolithic matrices including sensor elements and readout electronics are located at the left and right. The two capacitively coupled detector matrices are located in the middle.



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**Table 1.** Sub-matrix flavours in H35DEMO analog sensors.

| | Matrix Analog 1 (ANA1) | Matrix Analog 2 (ANA2) |
|---|---|---|
| sub-matrix 1 | - Extra DPTUB for High Voltage<br>- ELT in the feedback circuitry | - Extra DPTUB for High Voltage<br>- High gain |
| sub-matrix 2 | - Without DPTUB for high voltage<br>- ELT in the feedback circuitry | - Without DPTUB for high voltage<br>- High gain |
| sub-matrix 3 | - Without DPTUB for high voltage<br>- Linear transistors in feedback | - Without DPTUB for high voltage<br>- Low gain |

### 2.1 Analog pixel flavours

The H35DEMO analog matrices were each sub-divided along the columns into three flavours of in-pixel amplification circuit of equal size (23x100 pixels). The first analog matrix consists of circuits containing different flavours of transistors, linear or enclosed layout (ELT) and different P-Wells (with or without the Deep P-Well (DP) illustrated in figure 2) for high voltage biasing. The second analog matrix also contains three types of pixel, with different gain in the second stage of amplification and different P-Wells for high-voltage biasing as in the first matrix. The different flavours are summarised in table 1. The H35DEMO prototype pixel amplifiers have not been optimised to produce a fast signal meeting LHC requirements, as the 3.3V power supply and the large capacitance of the pixels matching the FE-I4 pixel size would yield to a large power consumption complicating the operation of the sensor.

### 2.2 Capacitive coupling to the FE-I4 ASIC

In capacitively coupled hybrid detectors, the signal processed in the sensor is transmitted to the read-out chip (ROC) via a capacitive injection. The pixel pads at the top surface (last metal layer) of the sensor and of the ROC are aligned with each other and coupled together by a thin layer (from 0.2 µm up to 10 µm, depending on the bonding force) of a non-conductive resin by the flip-chip process. Each pixel pad will act as a capacitor terminal with the glue as a dielectric layer in between. The particle signal in the sensor is transmitted as a voltage pulse generated in the pixel pad that then creates a charge pulse signal in the ROC pixel pad, where it is followed by a charge sensitive amplifier and so on, as illustrated in figure 3.

As the method of signal transfer between the sensor and the ROC is via a capacitive injection, potential crosstalk to neighbouring pixels must be considered. For that, a 3D simulation of the coupling between the pixel pads is performed with the COMSOL Multiphysics software, using the Finite Element Analysis method. A detailed 3D 3x3 pixel matrix was modeled based on each chip GDSII design file. The model includes the CMOS stack from the 3rd metal layer up to the last passivation layer. Figure 4 shows the 3D geometry created for the simulation.

COMSOL simulates the electric field between the pixel pads, shown on figure 5, and calculates the capacitance between all pads. Table 2 lists the coupling capacitances between the center pixel of the 3x3 H35DEMO matrix with all the 9 pixels in the 3x3 FE-I4 pixel matrix. As the charge transferred between the sensor and the ROC is linearly proportional to the capacitance, the 3rd column of table 2 shows the coupling capacitance normalized with respect to the middle pixel of



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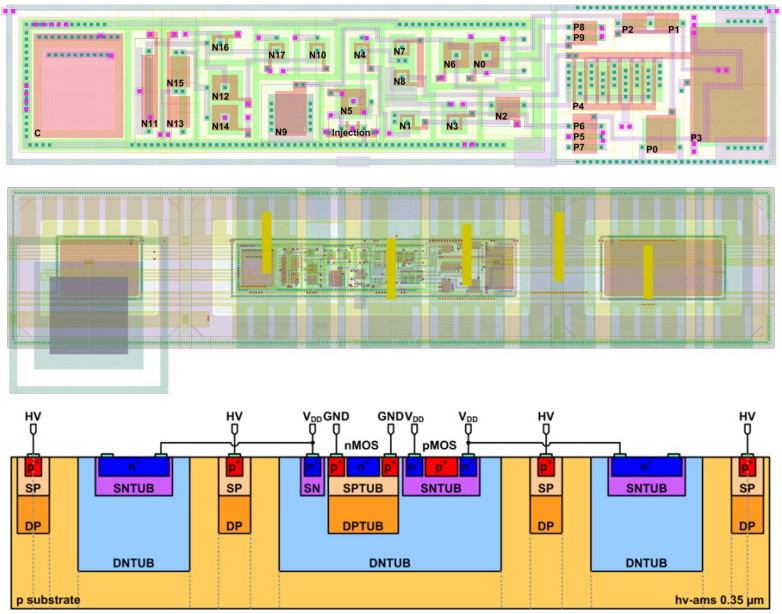


**Figure 2.** Top: transistor layout ($20.25\,\mu m^2 \times 95.05\,\mu m^2$) of one flavour of the H35DEMO pixel in the Analog Matrix. Middle: amplifier and output stage transistors embedded in the central deep N-Well while to additional peripheral deep N-Well are added to each side of the central well to fill the pixel area with the collection electrode. The three deep N-Wells are electrically connected through metal to the input of the amplifier. The output top metal pad (dark blue square) is located on the extremity of the pixel with a small offset in the vertical direction. Bottom: doping structure of the H35DEMO analog pixel, illustrating the different doping structures. N-type implants are represented by the letter "n", while p-type is represented by "p". Shallow doping is indicated by "S" while deep implants are represented by "D". It is also possible to see the HV, GND and $V_{dd}$ input connections.

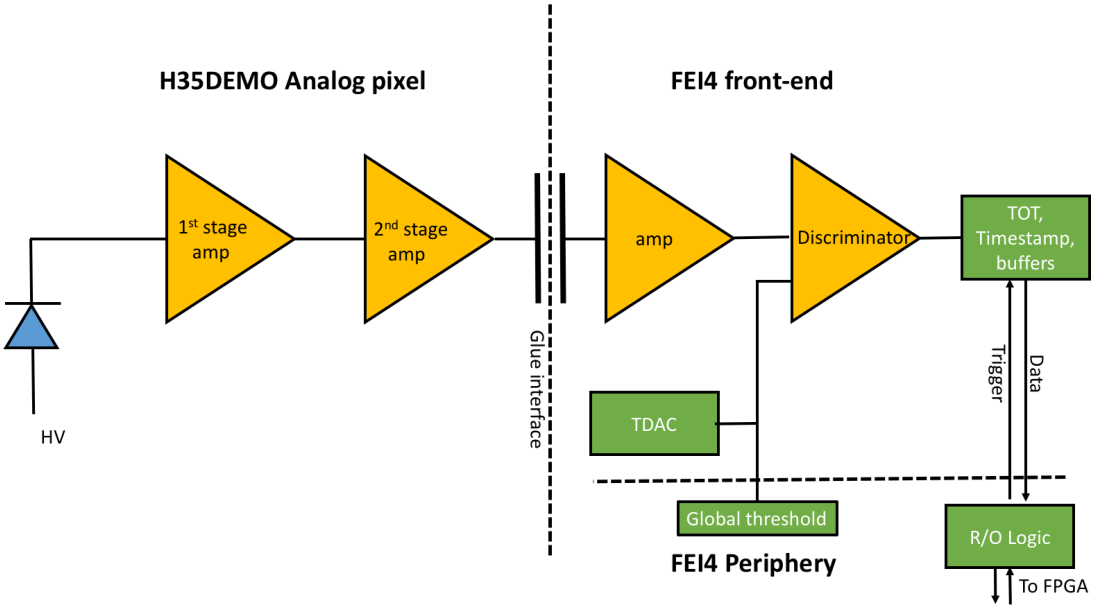


**Figure 3.** Schematic representation of the readout chain of the H35DEMO prototype capacitively coupled to FE-I4.



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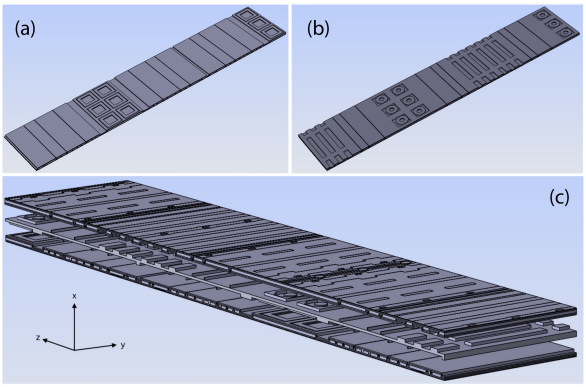


**Figure 4.** (a) H35DEMO 3x3 pixel matrix. (b) FE-I4 3x3 Pixel matrix. (c) 3x3 matrices facing each other, with the conformal dielectric glue layer in between.

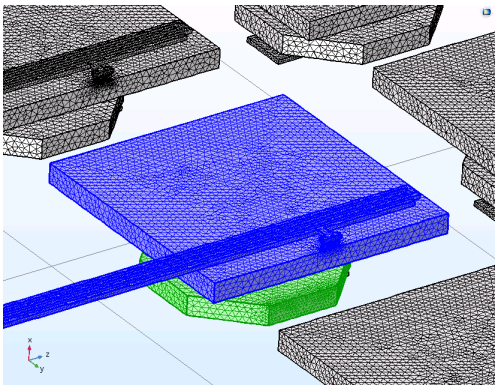

**Figure 5.** H35DEMO pixel pad (blue) and FE-I4 pad (green), plus neighbouring pixels, simulation mesh.

**Table 2.** Coupling capacitances between 9 FE-I4 pixels and a H35DEMO pixel with a 2.5 µm gap in between.

| FE-I4 Pixel | Capacitance [fF] | Cross-talk [%] |
|---|---|---|
| 1 | $10^{-63}$ | $10^{-61}$ |
| 2 | $10^{-62}$ | $10^{-60}$ |
| 3 | $10^{-62}$ | $10^{-61}$ |
| 4 | $5.5 \times 10^{-4}$ | $1.60 \times 10^{-2}$ |
| 5 | 3.46 | 100 |
| 6 | $5.54 \times 10^{-4}$ | $1.60 \times 10^{-2}$ |
| 7 | $6.42 \times 10^{-7}$ | $1.86 \times 10^{-5}$ |
| 8 | $5.61 \times 10^{-4}$ | $1.62 \times 10^{-2}$ |
| 9 | $6.68 \times 10^{-7}$ | $1.93 \times 10^{-5}$ |

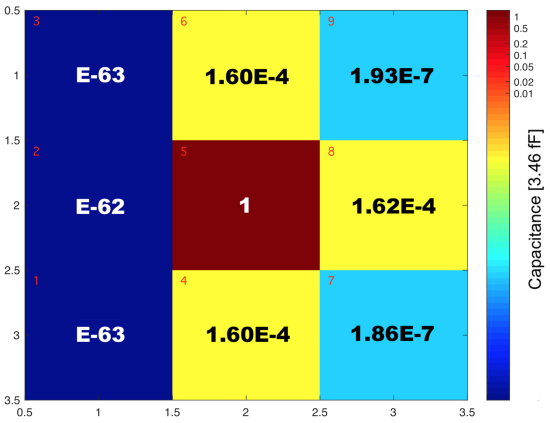


**Figure 6.** Normalized coupling between H35DEMO pixel and 9 FE-I4 pixels.

the FE-I4 matrix, and the same relative coupling is also shown on figure 6, helping to visualize the amount of charge that would be transferred due to the cross-coupling to neighbouring pixels. The asymmetry observed in coupling capacitance is due to the layout of pixels in the FE-I4 in double columns, reproduced in the model, as can be seen in figure 4 a) and b). This geometry allow to extract the coupling capacitance for the pixels inside a double column and between double columns. The results from the simulation shows that the expected coupling capacitance for the main pixel is in the order of 3.5 fF, with a maximum cross-coupling around 0.016%, meaning that the charge induced to the neighbouring pixels, due to cross-talk, will mostly be under the detection threshold.

The glueing process was developed using the Acc$\mu$ra 100 flip-chip bonder. The machine controls the bonding with a precision of ±1.5 µm and a parallelism of ±1 µrad. Araldite 2011 epoxy was used as the adhesive and coupling medium. Forty lines of glue, one for each FE-I4 double-column, were dispensed at a speed of 2 cm s$^{-1}$ using a 3 cc syringe with a 600 µm dispensing tip and 4 bar of pressure in the time-pressure dispenser. Figure 7 shows the dispensing process inside the flip-chip machine and the final assembly mounted on PCB.



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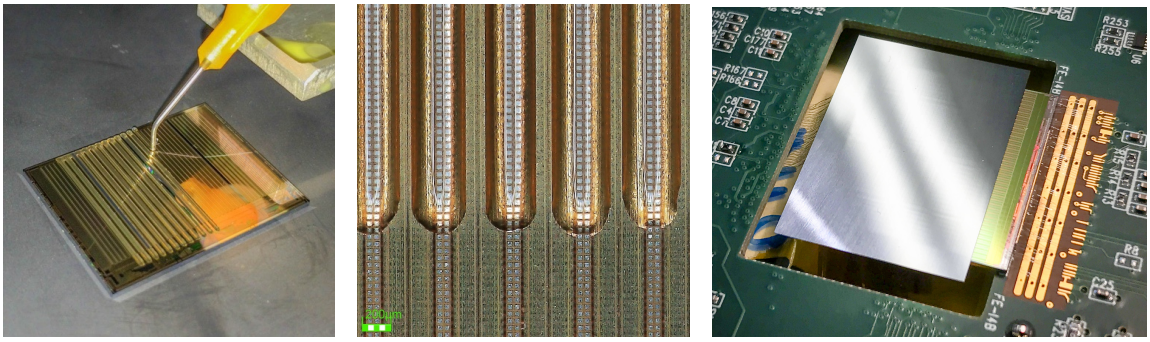

**Figure 7.** Left: deposition of epoxy on the H35DEMO matrix by the automatic glue time-pressure dispenser of the Acc$\mu$ra 100. Middle: glue (partially) deposited on double pixel column. Right: 100 µmthin H35DEMO-FE-I4 assembly on PCB.

During the production, several mechanical samples were assembled and cross-section and metrology studies were performed on the glue interface to verify the parallelism and measure the distance between the H35DEMO and FE-I4 pads. Figure 8 shows the cross-section image for one of these samples on both sides of the assembly, at 2 cm distance. The measurement demonstrated that the process we developed produces assemblies with a good parallelism, i.e. less than 100 nm difference in silicon to silicon distance over the whole assembly, and good control of the distance between the coupling pads with the passivation of each pad in contact with its respective pad on the FE-I4 ASIC.

Later, data taken during testbeam also confirmed the good flip-chip parallelism as shown on the ToT map on figure 9. The amplitude coming from the pixel output has been simulated to be on the range between 100 mV, for an injected charge of 750 e (0.5 MIP), and 300 mV for 4500 e (3 MIP) [7], with a noise corresponding to 120 e. With the simulated H35DEMO pad coupling capacitance of 3.5 fF, the current signal generated in the FE-I4 amplifier (by a MIP particle) will be in the order of 2000 e. The FE-I4 amplifier was tuned to yield a ToT = 10 for an input charge of 16 e. Figure 9 combines the data taken separately from analog matrix 1 and 2 and shows that an uniform ToT distribution is achieved on both analog matrices. The lower ToT on the second analog matrix is due to the higher threshold used during data acquisition with ANA2, where the FE-I4 threshold was set to 3000 e, while the FE-I4 threshold was set at 2000 e for ANA1.

## 3 Test beam experimental setup and reconstruction

The Geneva FE-I4 Telescope [11] was used for the measurements of the H35DEMO prototypes. It comprises six telescope planes built from ATLAS IBL hybrid sensors, i.e. a planar passive silicon sensor bump-bonded to a FE-I4 readout ASIC. It is placed inside a particle beam and the six planes are used to measure the beam particles independent from the device-under-test (DUT). A RCE readout system [12] was used for the data acquisition of the telescope planes and the DUT. The hit bus signal of the first and the last telescope planes are combined to provide a trigger for the data acquisition system. The CaRIBOu system [13] was used for the slow control of the H35DEMO



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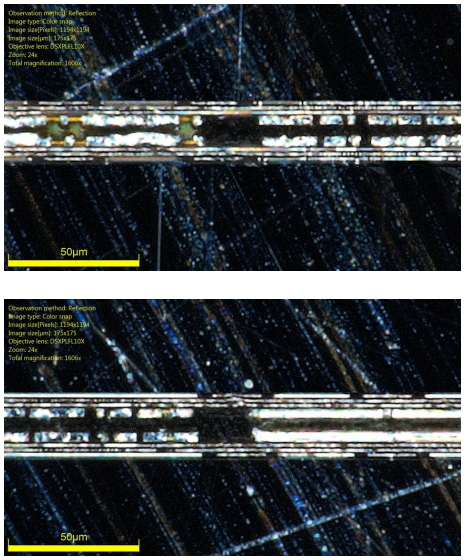


**Figure 8.** Thickness of the glue layer along the chip edge at two locations along the chip at 2 cm distance showing good parallelism, less than 100 nm difference measured with an optical microscope, from left to right.

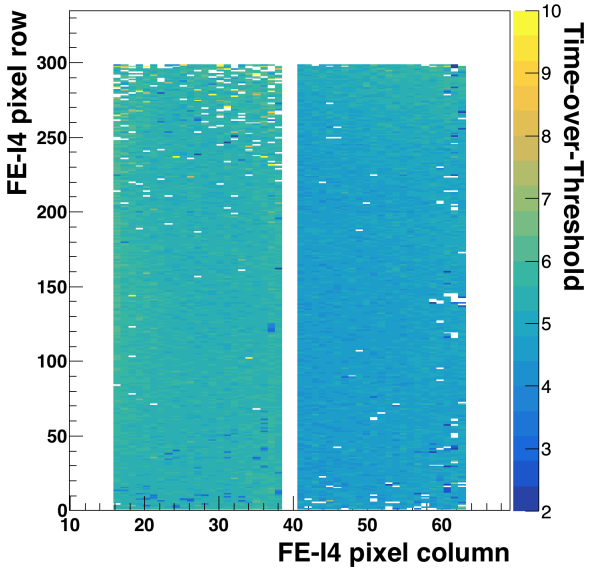


**Figure 9.** Combined ToT map from analog matrix 1 (left) and 2 (right). The lower threshold on the second analog matrix is due to the higher FE-I4 threshold (3000 e), comparing with the 2000 ethreshold for the first analog matrix, during data acquisition.

prototypes. DUT samples were mounted inside a thermally insulated box equipped with cooling provided by a chiller and maintained at 25 °C or less during data taking.

The reconstruction and analysis of the data obtained were performed using the Proteus reconstruction software [14]. Proteus starts with the raw hit data and provides fully reconstructed clusters and tracks. First, it combines neighboring hits on each sensor into clusters using a greedy clustering algorithm. Then, it estimates the cluster position and cluster signal. The specific algorithms can be configured for each sensor type and here both the telescope sensors and the DUT use the time-over-threshold-weighted center-of-gravity as a position estimator.

For track finding, clusters on the telescope planes are transformed into the global coordinate system using a three-dimensional geometry description of all planes that takes into account all degrees of freedom of a planar surface in three-dimensional space. Starting from clusters on the first sensor, track candidates are found by extrapolating the initial position to all further telescope planes along the beam direction and adding matching clusters. Ambiguities are solved by bifurcation of the track candidate. From all candidates, tracks are selected by exclusively associating clusters to tracks starting from the longest track with the lowest fit $\chi^2$ value.

All planes are aligned first using a rough alignment based on correlations and then using a track-based alignment that minimises track residuals. To provide a consistent performance over long data taking periods, the alignment procedure is performed for each run. The first 20 000 events are used to align the geometry and are not used during the analysis.

For the analysis, only tracks with clusters on all six telescopes and a $\chi^2/d.o.f.$ below 5 are considered. All further operations are performed in a local coordinate system anchored on the surface of the DUT. Tracks are reconstructed by performing a weighted least squares fit in the local



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**Table 3.** Summary of measurements performed on the H35DEMO prototypes in test beam. The Analog 2 matrix of the 1000 Ω cm sample was not measured due to an early increase in leakage current below the breakdown voltage as described later in the text. Note that the FE-I4 threshold regards the signal being transferred by the capacitive injection from the H35DEMO, instead of the real charge generated on the sensor.

| Resistivity (Ω cm) | Matrix | Bias Voltages (V) | FE-I4 Threshold (e) |
|---|---|---|---|
| 80 | Analog 1 | 0-160 | 1500, 2000 |
| 200 | Analog 1 | 0-160 | 2500, 3000, 4000 |
| 200 | Analog 2 | 0-140 | 2000, 2500, 3000, 4000 |
| 1000 | Analog 1 | 0-160 | 1500, 2000, 2500, 3000 |

coordinate system using a linear track model. The reconstructed positions on the DUT surface have a resolution of 10 µm along the column direction and 12 µm along the row direction of the H35DEMO prototype. Reconstructed tracks are then matched to H35DEMO clusters using a matching cut on the distance between the two of 250 µm along each axis.

Samples of three different resistivities (80 Ω cm, 200 Ω cm and 1000 Ω cm) were studied with bias voltage scanned from 0 V to 160 V and FE-I4 thresholds from 1000 e to 4000 e as described in table 3. For each point, one to ten million triggers were recorded.

## 4 Results

### 4.1 Current-bias (I-V) characterisation

The H35DEMO samples tested were first characterised using a probe station to verify the quality of the assemblies and measure the leakage current versus device temperature when high voltage was applied to the sensor. Figure 10 shows the I-V curves for the different resistivities under study. The 80 Ω cm and 200 Ω cm show low leakage current well below 1 µA cm$^{-2}$ for all temperatures up to the breakdown voltage, determined to be 178 V and 180 V, respectively. For the 1000 Ω cm sample, an early offset of current is observed at a bias voltage of 30 V. This was initially mistaken for an early breakdown. However, further measurements have shown that a plateau of current is reached in the device before a second upset in current at 180 V is observed, corresponding to the real breakdown. This effect is known as the Rise-And-Flatten (RAF) effect [15]. This additional leakage current corresponds to a surface current generated in other unbiased test structures of the H35 submission located at the periphery when reached by the depletion zone, larger laterally for the higher resistivity substrate. An Arrhenius plot was extracted from the data at different temperatures confirming that the generated leakage current does not correspond to a generation current from the bulk of the sensor. This effect could be limited in the future by removing or placing further the structures outside of the main matrix. As this phenomenon was discovered later during the testbeam campaign, due to time constraints only the first analog matrix of the 1000 Ω cm was studied with a bias voltage larger than to 30 V, the second matrix show same behaviour but was not studied due to limited beam time.



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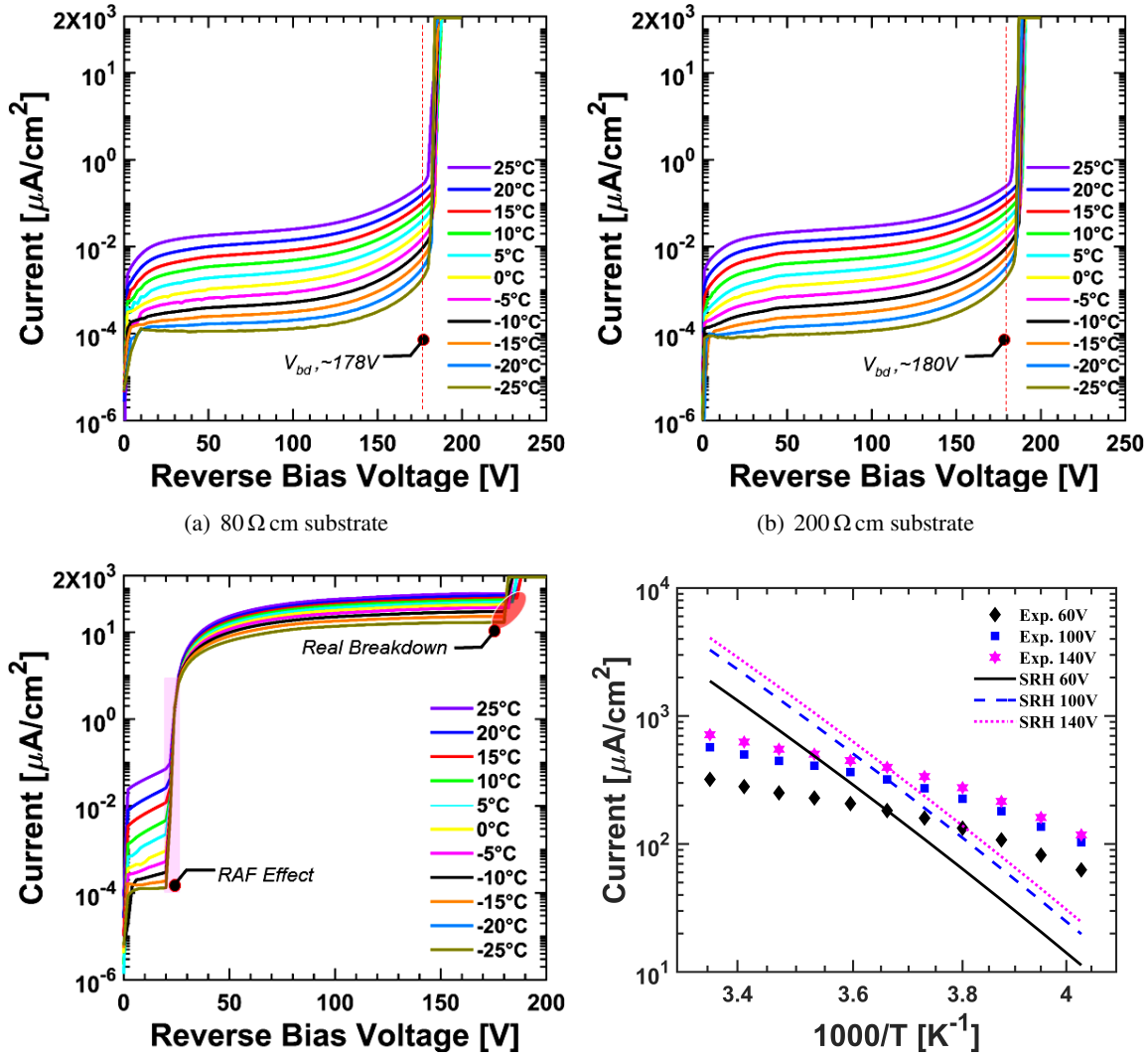


(a) 80 Ω cm substrate

(b) 200 Ω cm substrate

(c) 1000 Ω cm substrate

(d) Arrhenius plot for 1000 Ω cm substrate

**Figure 10.** Characteristic I-V curves and Arrhenius plot for 80 Ω cm, 200 Ω cm and 1000 Ω cm substrate resistivity samples for temperatures ranging from −25 °C to 25 °C. Leakage current dependence on temperature as a function of the inverse of the temperature for a 1000 Ω cm substrate, also known as the Arrhenius plot, is presented in figure d). Leakage current differs from the prediction from the Shockley-Read-Hall (SRH) model of Generation-recombination of thermal carriers in a silicon bulk [19].

### 4.2 Comparison of pixel flavours

The H35DEMO analog matrices contain six flavours of pixels with different gain, feedback and biasing schemes. The purpose of these variations is to determine the best scheme to ensure a low noise and a high-efficiency operation of the pixel. The Deep P-Well, a deep implant located below the high voltage implant (see figure 2) influences the pixel input capacitance and therefore the noise and rise time of the signal. Enclosed layout transistors (ELT) are used to make the circuitry more radiation tolerant to ionising dose but will negatively affect the gain and rise-time of the pulse



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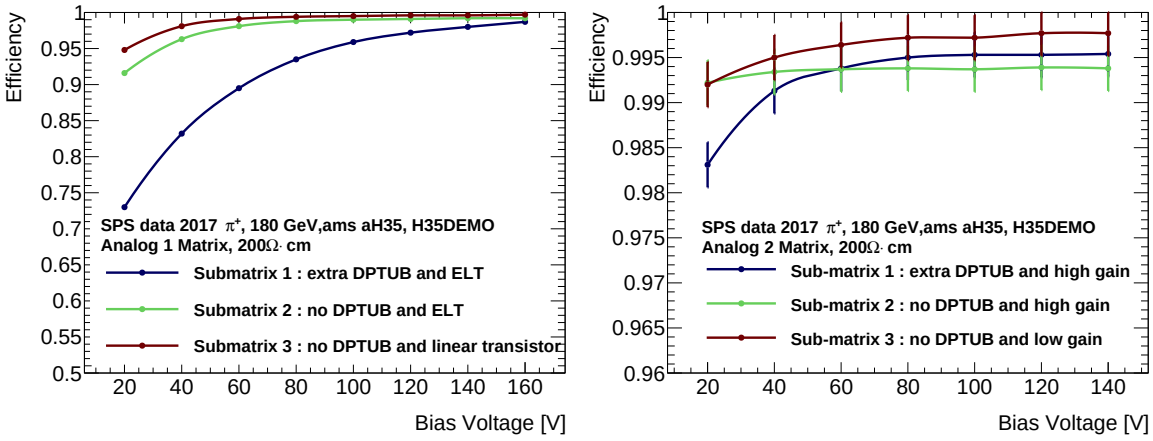


(a) 200 Ω cm Analog Matrix 1 efficiency *vs* HV bias.

(b) 200 Ω cm Analog Matrix 2 efficiency *vs* HV bias.

**Figure 11.** Detection efficiency as a function of bias voltage for the three sub-matrices of analog matrix 1 (left) and analog matrix 2 (right) for a 200 Ω cm sample for a threshold of 2000 e.

generated by the circuitry. The gain, as determined by the feedback capacitor in the pixel amplifier, will affect the noise and the detection efficiency, for a given injection charge. Figure 11 shows the detection efficiency for all sub-matrices of the analog matrices of the 200 Ω cm sample, as a function of the bias voltage applied to the sensor. The detection efficiency is defined as the ratio between number of reconstructed tracks matched to a cluster on the DUT and the total number of reconstructed tracks in the acceptance. Figure 11(a) shows that the use of an ELT in the feedback circuitry of the pixel (sub-matrix 2) doesn't impact significantly the pixel detection efficiency when compared with the pixel flavour using linear transistors (sub-matrix 3). The most significant effect is however linked to the addition of the Deep P-Well implant to the high-voltage implant, degrading the detection efficiency in both analog matrices. The addition of capacitance between the Deep N-Well and the biasing contact due to this implant affects the gain and rise-time of the amplifier and should be avoided for particle detection. In Analog matrix 2, for the three cases, efficiency is well above 99 % in the conditions of figure 11(b).

Another important aspect that must be assessed with regard to the different pixel types is the timing accuracy as measured by the FE-I4 ASIC that relates to the rise time of the pulse and the associated time walk due to the detection threshold.

### 4.3 Cluster size, spatial resolution and time resolution

The effect of different substrate resistivity on the behaviour of the H35DEMO prototypes can also be observed through the changes of cluster properties for the hit clusters produced by the beam. Figure 12 shows the typical cluster size measured for the high-gain matrix, that shows the highest detection efficiency. For all resistivities, the dataset is dominated by clusters containing only one pixel. This is due to the large size of the pixel (250 µm × 50 µm) and the small depletion depth expected (<50 µm). At higher resistivity, the influence of a large depletion depth can be observed and two phenomena are competing. The charge deposited deeper in the bulk will drift for a longer time than the charge deposited close to the electrodes. Meanwhile, the increased electric field in



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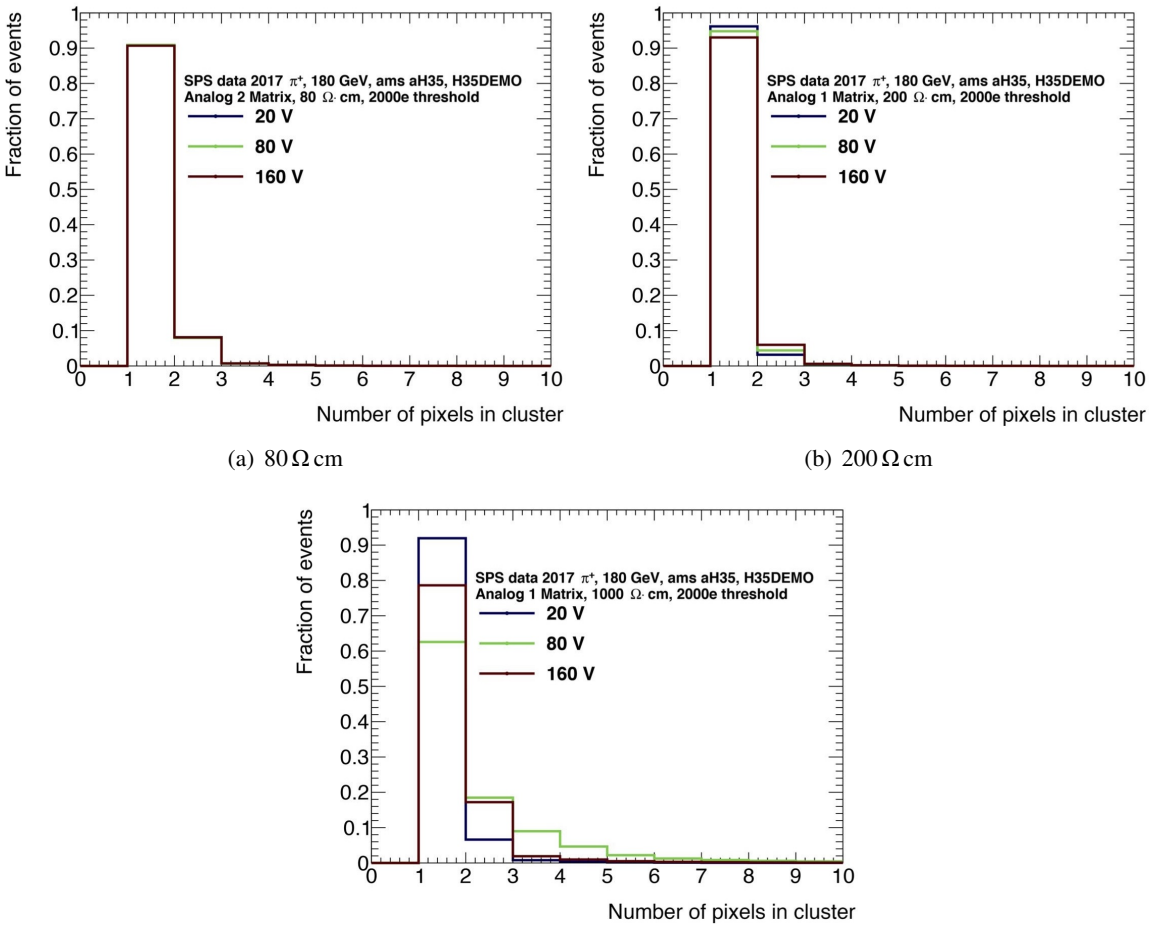
the bulk increases the charge speed, making the charge drift time smaller. This second effect is enhanced in our prototype as the bias voltage is applied on an electrode surrounding the collection diode. As the depletion depth reaches values larger than the electrode to N-Well distance (10 µm), the behaviour of the diode diverges from that of a planar diode. It can be observed in figure 12(c) that the charge sharing producing larger clusters is maximal at an intermediate bias voltage of 80 V.




(a) 80 Ω cm

(b) 200 Ω cm

(c) 1000 Ω cm

**Figure 12.** Cluster size versus bias voltage and different substrate resistivity for 2000 e threshold.

As most clusters contain only one pixel, the spatial resolution of the prototypes is mainly determined by the size of the pixels. Figure 13 shows a typical unbiased residual distribution for a 200 Ω cm sample operated with 160 V bias voltage and 2000 e threshold. Some tails can be observed on the residual curves. These can be explained as clusters containing more than one pixel, with the charge induced due to capacitive coupling between a pixel pad and its neighbours, as previously observed [16]. This charge is then due to the coupling method and not due to the charge sharing inside the bulk of the sensor. The cluster position is reconstructed using the time-over-threshold-weighted center of gravity. The cross-coupling increases the measured time-over-threshold away from the true hit position. Consequently, the reconstructed cluster position is also calculated to be further away and the residuals are enlarged. As the particle beam illuminating the sensor is not



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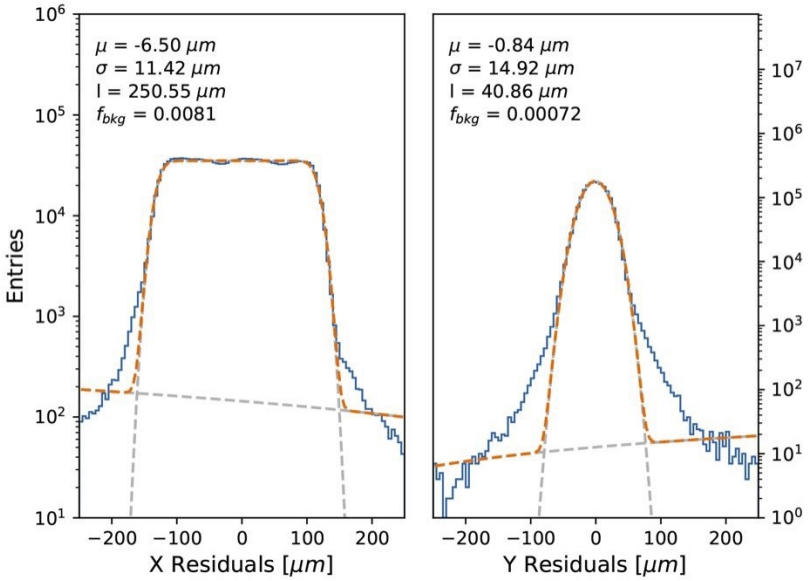


**Figure 13.** Unbiased residual for a 200 Ω cm sample, 160 V bias voltage, 2000 e threshold, analog matrix 1 (blue). Fit of a gaussian convoluted with a box function (orange). $\mu$ is the mean of the distribution, $\sigma$ the width of the gaussian, $l$ the width of the box and $f_{bkg}$ the fraction of background events.

uniform, the fraction of background events is dependent on the sensor, resulting in the tilt observed on the residual plots.

The resistivity of the substrate should also have an effect on the rise time of the signal and the amount of charge generated. Figure 14 shows the dependence of the timing resolution of the H35DEMO for different bias voltage and resistivity for the second high-gain matrix. No significant variation of the distribution was observed in the other matrices. It was not possible to adjust the delay of the clock for the FE-I4 ASIC to optimise the binning of the timing distribution. No clear dependence of the timing resolution on resistivity, gain or presence of the Deep P-Well can be observed. However, in all cases, the timing distribution is constrained to less than 50 ns for bias voltages over 80 V. We can deduct from this that the timing resolution is dominated by the intrinsic jitter of the preamplifier and not by the sensor signal amplitude or rise time.

### 4.4 Detection efficiency

The particle detection efficiency is a key parameter to determine the usability of high-resistivity substrate CMOS sensors. This parameter is influenced by the signal strength and the gain of the preamplifier. Figure 15 shows the threshold scan performed for the individual matrices for different thresholds settings of the FE-I4. A clear dependence of the efficiency on the substrate resistivity for comparable thresholds can be observed. The higher the resistivity, the smaller the bias voltage needed to obtain a good detection efficiency, in agreement with our expectation. Excellent detection efficiency superior to 99 % can be achieved for all resistivities studied with a threshold of 2000 e, corresponding to approximately 1500 e signal in the H35DEMO sensor, assuming 3.5 fF coupling capacitance and a gain of 100 mV/1500e.



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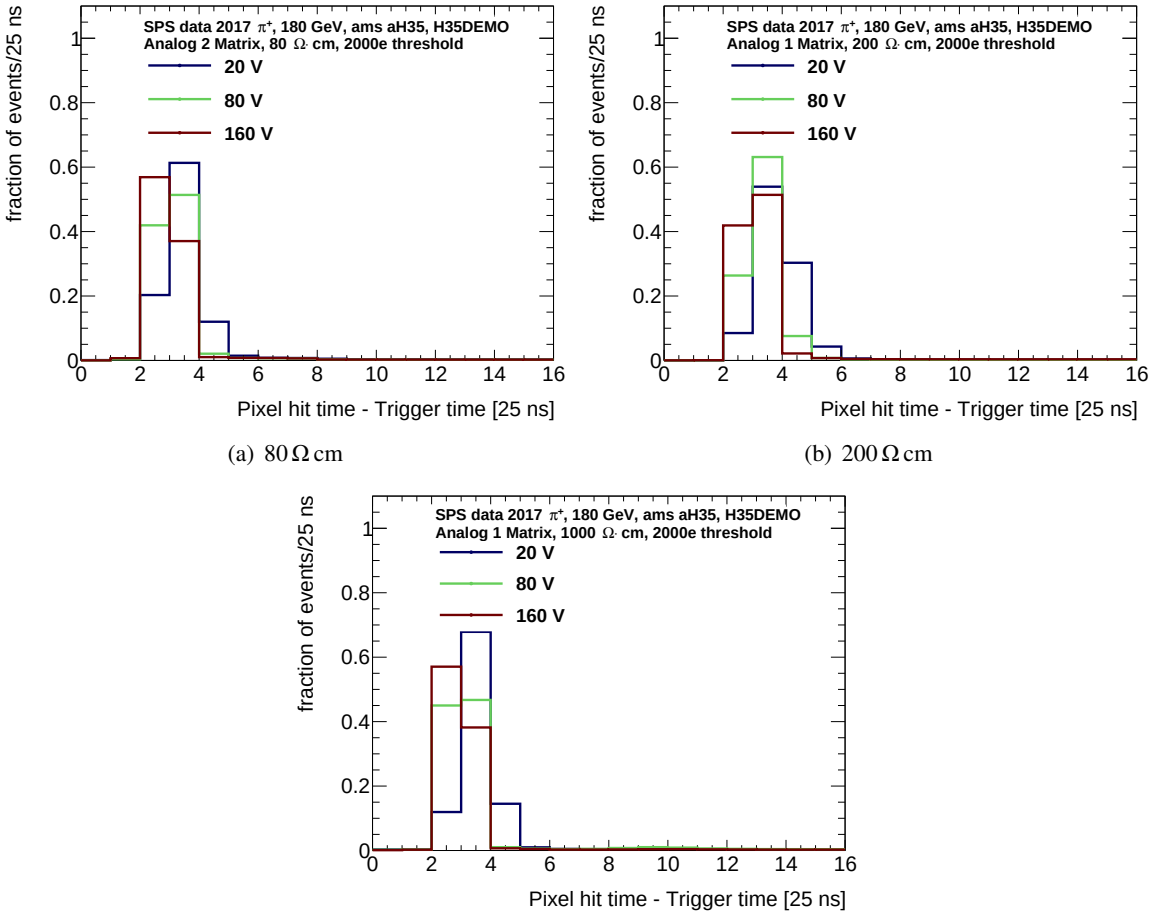


(a) 80 Ω cm

(b) 200 Ω cm

(c) 1000 Ω cm

**Figure 14.** Signal arrival time distributions in 25 ns bins versus bias voltage and different substrate resistivity for 2000 e threshold.

Figure 16 shows the efficiency for each pixel of the second high-gain matrix for each of the three resistivities, taken at 2000 e FE-I4 threshold and 160 V bias voltage. These results show, after careful tuning of the glueing method, a good detection uniformity over the matrix has been achieved. This demonstrates a good uniformity of the pixel's electrical behaviour within the columns and good uniformity of the glue interface and preamplifier properties.

Figure 17 shows the in-pixel efficiency measured for the high-gain matrices for different resistivities and HV bias. Figure 17(a), (c) and (e) shows the efficiency at low bias voltage, where intra-pixel regions with lower efficiency are visible, more evident for the lower resistivity substrate. TCT measurements [18] has confirmed that lower depletion volumes are achieved with lower resistivity substrates, when compared with an higher resistivity substrate at the same HV bias. This effect can be observed as the less efficient region between pixels as shown on figure 17(a). All samples could be operated with high efficiency when sufficient bias was applied, as shown on figure 17(b), (d) and (f).



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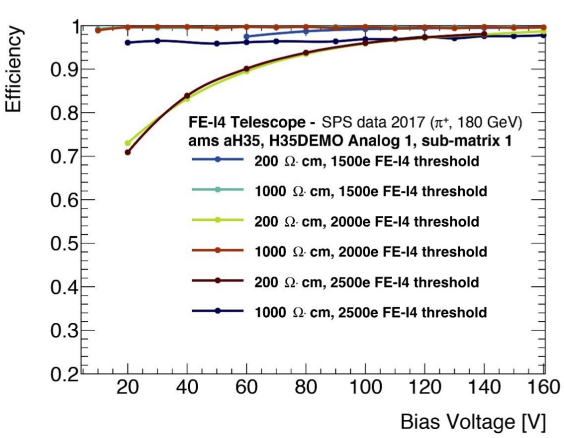
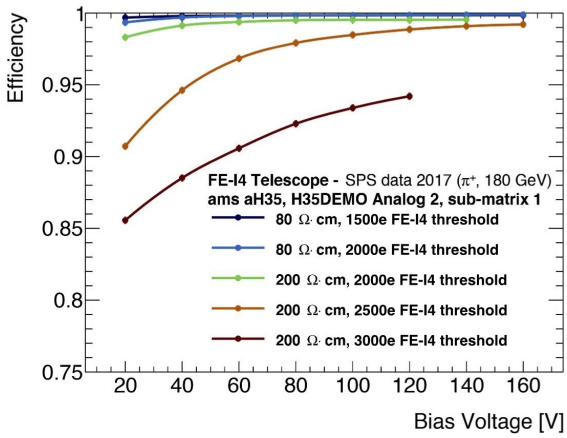
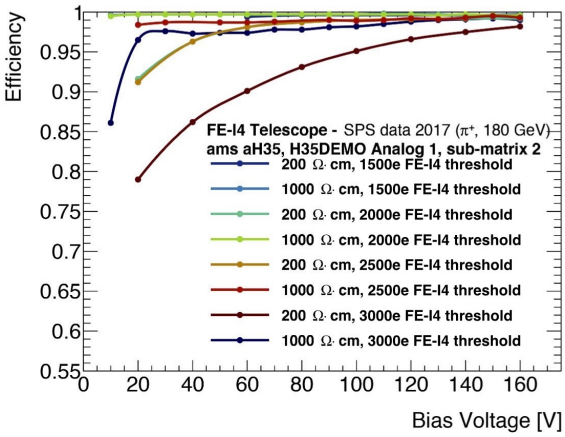


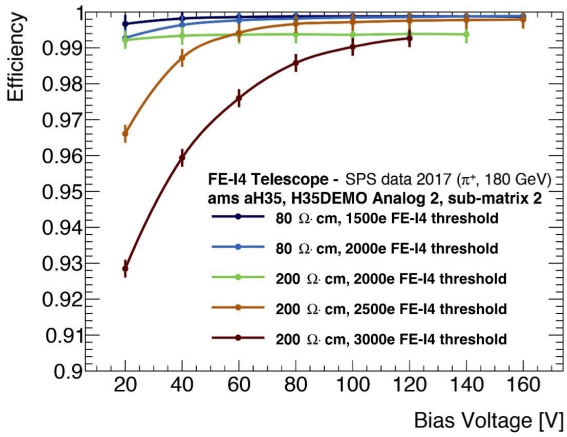

(a) Analog 1, submatrix 1



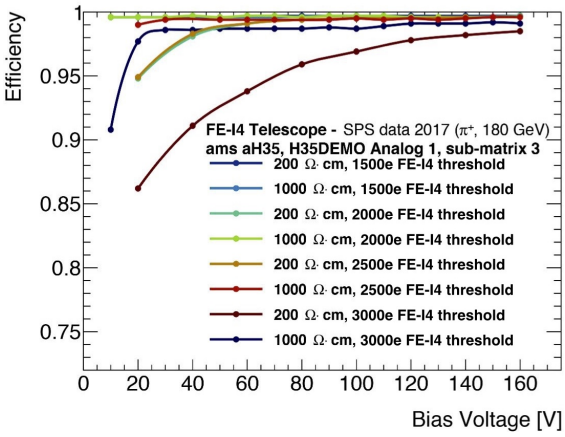

(b) Analog 2, submatrix 1



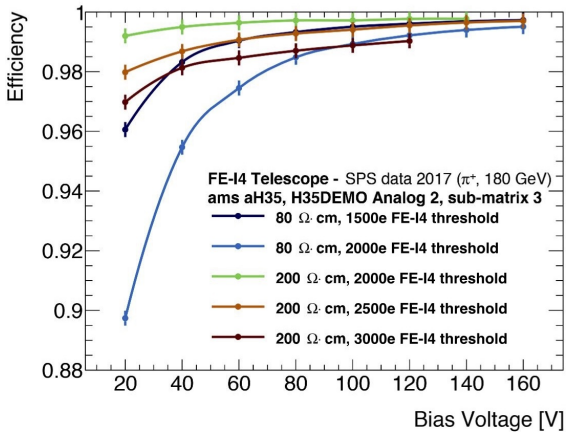

(c) Analog 1, submatrix 2




(d) Analog 2, submatrix 2




(e) Analog 1, submatrix 3




(f) Analog 2, submatrix 3

**Figure 15.** Global efficiency of 80 Ω cm, 200 Ω cm and 1000 Ω cm resistivity substrate samples for the different sub-matrices as a function of bias voltage for different substrate resistivities and FE-I4 detection threshold.

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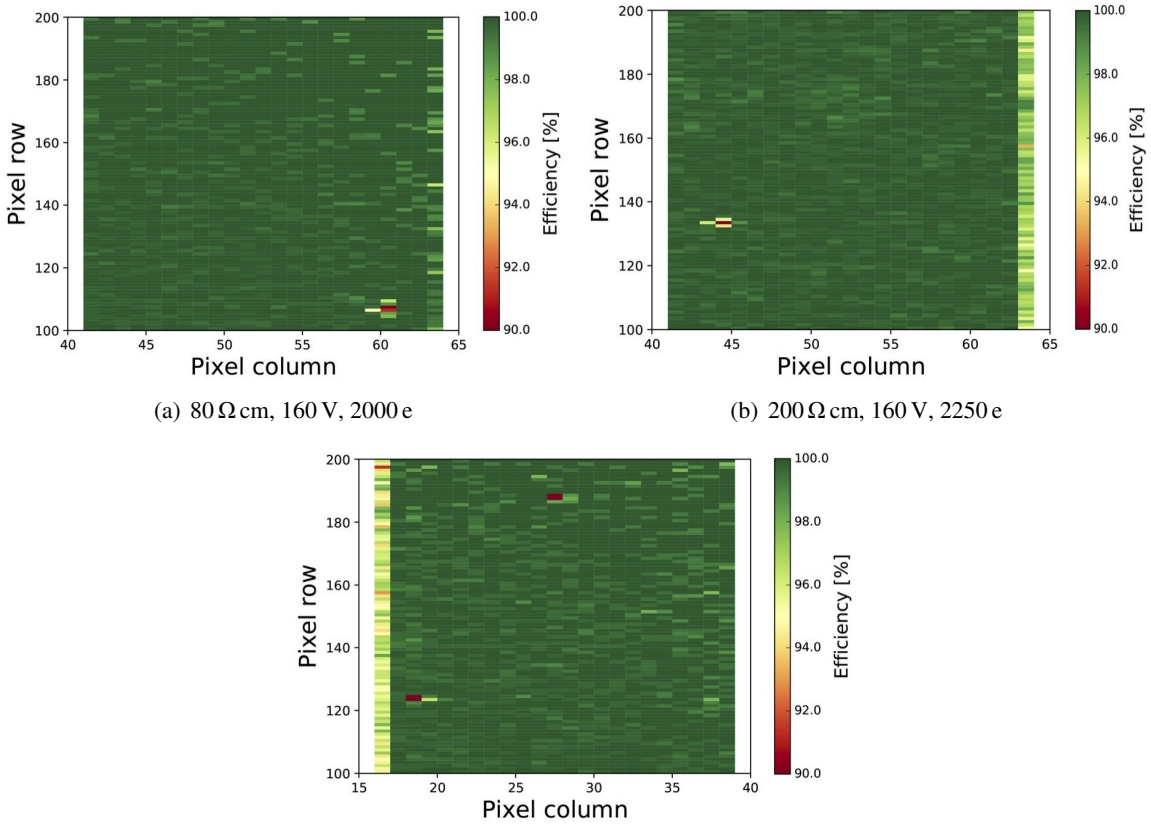


(a) 80 Ω cm, 160 V, 2000 e

(b) 200 Ω cm, 160 V, 2250 e

(c) 1000 Ω cm, 160 V, 2000 e

**Figure 16.** Efficiency for the analog high-gain sub-matrices, covering rows 100 to 200 of the FE-I4 and spanning over 24 columns, at 160 V and different substrate resistivity for 2000 e threshold. The left column for analog matrix 2 and right column for analog matrix 1 show lower efficiency due to the proximity with the pixels of the monolithic NMOS and CMOS matrices, which can compete for the charge signal.

In light of the results obtained during this test beam campaign, the following observations can be made:

- The use of ELT in the feedback circuitry does not affect significantly the performance of the amplifier, as shown on figure 11(a).
- The extra deep P-Well (DPTUB) should not be used, placed under the P-Well providing the contact to the substrate, in order to reduce the input capacitance of the preamplifier. Figure 11 shows that a higher efficiency is achieved without the DPTUB.
- High-Gain is required to achieve good detection efficiency over a large range of bias in these conditions, as results from the second analog matrix has shown.
- Time resolution of the sensor is limited by the amplifier power consumption but is not affected significantly by the gain or feedback transistor used. The H35 technology uses 3.3V power supplies for the front-end and the current distributed to the pixels was limited to allow for efficient cooling during operation. A higher power consumption or a transition to a 1.8V



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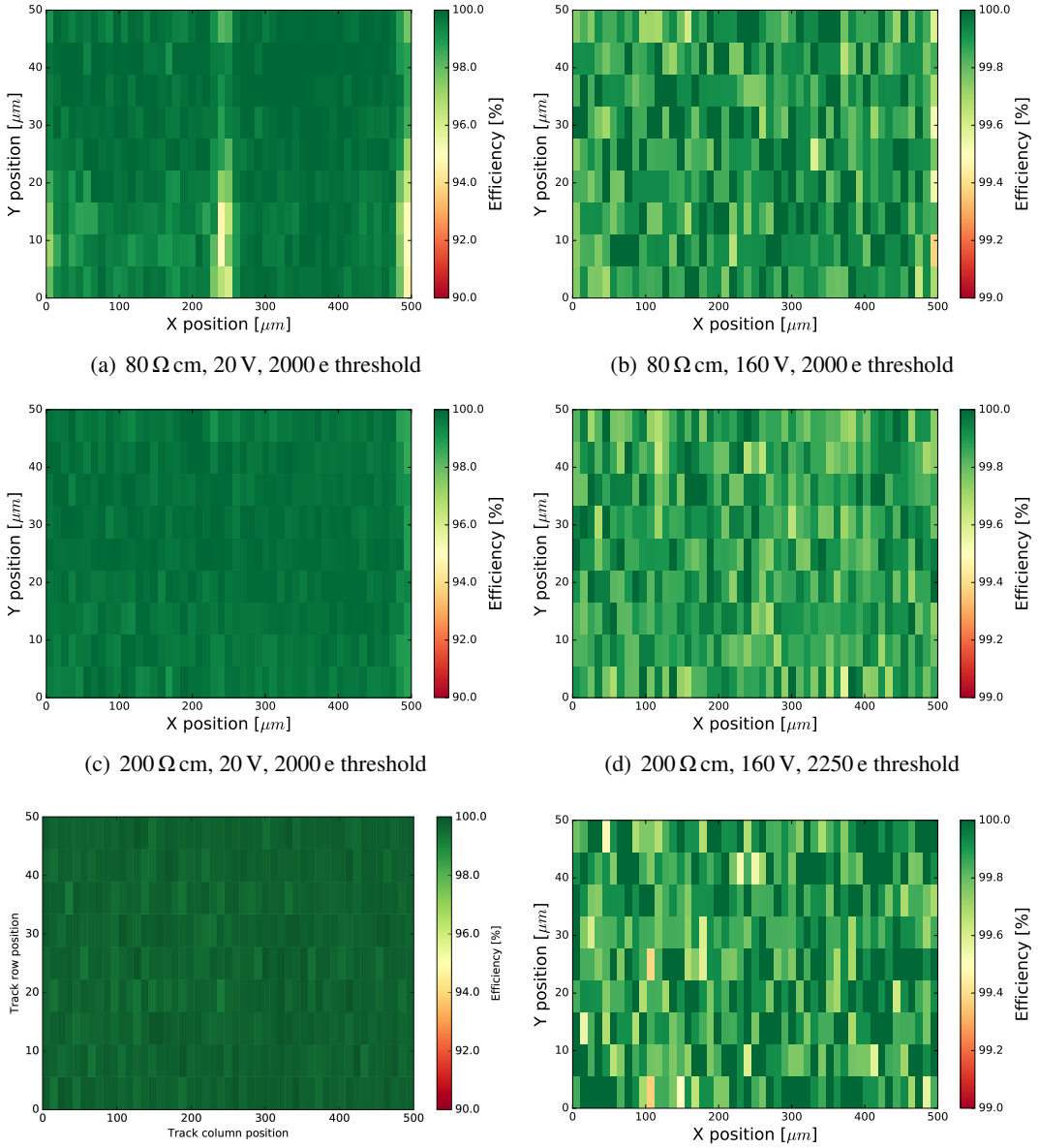


(a) 80 Ω cm, 20 V, 2000 e threshold

(b) 80 Ω cm, 160 V, 2000 e threshold

(c) 200 Ω cm, 20 V, 2000 e threshold

(d) 200 Ω cm, 160 V, 2250 e threshold

(e) 1000 Ω cm, 10 V, 2000 e threshold

(f) 1000 Ω cm, 160 V, 2000 e threshold

**Figure 17.** In-pixel efficiency of 80 Ω cm, 200 Ω cm and 1000 Ω cm resistivity substrate samples for submatrix 2 (Analog 2 for 80 and 200 Ω cm, Analog 1 for 1000 Ω cm). Pixels are arranged in a symmetric double column pattern. Note the difference in the color scale between data at 160 V and 20 V and the different threshold for d).

technology would yield to better timing, as show in our previous results with the IBM h18 technology [4, 5].

- A threshold of 1500 e or less must be achieved to ensure good detection efficiency superior to 99 % for all resistivities when the discriminator is to be implemented in the pixel, for monolithic integration (2000 e equivalent in FE-I4).



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## 5 Conclusion

Extensive test beam measurements of capacitively coupled pixel detectors designed in ams aH35 HV-CMOS technology were performed to evaluate the effects of high-resistivity substrates on the properties of the detector and evaluate the feasibility of building large area CMOS sensors. A method for uniform and reproducible glueing of the H35DEMO prototypes to the FE-I4 ASIC was developed and successfully used to produce a series of prototypes in three resistivities that were measured in beam tests. The results of this investigation shows that detection efficiencies larger than 99% can be achieved for all prototypes. A good uniformity in the coupling and on detection efficiency over a large area was measured. The advantages of using higher resistivity are illustrated by the measurement of the detection efficiency as a function of bias voltage and FE-I4 threshold. Higher resistivity results in larger signals and better efficiency at lower bias voltage. The time resolution of the different prototypes were evaluated and the results show little dependence on the substrate. This indicates that the timing resolution is determined by the preamplifier itself, with little influence from the signal strength and varying rise time.

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