A Fast Modular Semiconductor-Based Marx Generator for Driving Dynamic Loads

Martin Hochberg, *Student Member, IEEE,* Martin Sack, *Member, IEEE,* Dennis Herzog, Alfons Weisenburger, Wladimir An, Renate Fetzer, Georg Mueller, *Member, IEEE*

***Abstract*—The challenging demands of pulsed electron beam devices (such as the GESA device) with respect to their pulsed power supply have lead to the development of a new semiconductor-based Marx generator. At a maximum output voltage of 120 kV and 600 A pulse current for a duration of up to 100 µs, step-wise arbitrary output waveforms are desired. A fast rise time of the generator is achieved by using fast switching circuitry, low inductance capacitors and a low inductance stage arrangement. For low jitter triggering of all stages and efficient signal transmission, the generator uses an optical bus system for communication. Due to the inherent dynamic load characteristics of the GESA device, the generator features a fast over-current protection scheme. This work presents selected design aspects of the generator and their validation in a small-scale assembly able of delivering up to 8 kV at 600 A load current.**

***Index Terms*—Pulse power systems, Pulse generation, Pulse circuits, Pulse power system switches, Power semiconductor devices, Insulated gate bipolar transistors, Marx generator, Fast switching, Fast signal transmission, Optical communication**

I. Introduction

In electron beam accelerators used for surface modification, such as the GESA (Gepulste Elektronenstrahlanlage, german for pulsed electron beam device), LC-chain Marx generators have been used with great success as driving pulsed power sources [1]. With a simple setup, the required pulse amplitudes of 120 kV at 600 A load current can be achieved in a quasi-rectangular pulse. Due to the fixed arrangement of capacitors and inductors, however, any change in pulse length requires physical manipulation of components. Additionally, since the generator uses spark gaps as closing-only switches, the pulse shape follows the discharge of the pulse forming network. For improving the GESA process quality, a more flexible pulsed power source with respect to output voltage shape and amplitude is required.

In recent years, semiconductor-based Marx generators have received significant attention from various researchers due to the possibility of active pulse shaping [2], [3], [4]. The challenging requirements of the GESA device, especially with respect to the fast pulse rise time of 100 ns for 100 kV output voltage [5], lead to a new generator design [6]. Beside using a gate boosting circuit for speeding up the switching elements [7], a low inductance, low stray capacitance layout is key for achieving fast rise rates. Whereas some researchers use high stage voltages of up to 10 kV [4], employing more but lower voltage stages allows for more accurate adjustments of the output pulse. As more individual stages, on the other hand, increase the control complexity, the approach presented in this paper uses an optical bus system for stage communication and synchronized switching. Since the GESA device is still under development, sudden load shorts may occur. To protect the generator, a fast over-current detection has been implemented. This work presents the design of the generator-under-development and first measurements in a 8 kV, 600 A small scale version.

The authors are with Karlsruhe Institute of Technology, Institute for Pulsed Power and Microwave Technology, Eggenstein-Leopoldshafen 76344, Germany (e-mail: Martin.Hochberg@KIT.edu).

II. Generator design

A. Generator schematic

Considering the design constraints of the GESA device, namely the output voltage of up to 120 kV and the output current of up to 600 A for a pulse length of 100 µs, a Marx generator circuit is an efficient solution. This modular concept comprises a pulse capacitor C, a pulse switch T and a free-wheeling diode D. The schematic can be seen in Fig. 1.

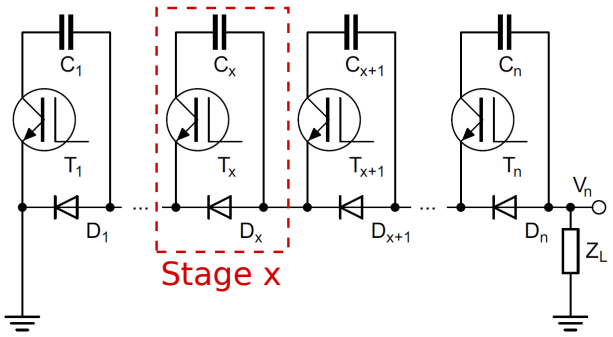


Fig. 1: Simplified circuit diagram of the modular Marx Generator consisting of n identical stages. Each stage comprises a pulse switch T, a pulse capacitor C and a free-wheeling diode D. The generator delivers the output voltage V_n to the load impedance Z_L.

Prior to pulse execution, all capacitors are charged in a parallel configuration to the same voltage V_0 (charging path not shown). During the pulse, the stage's charging path is transiently isolated - by closing the pulse switches the capacitors can be connected in series configuration leading to a reduction of the overall capacitance and a voltage multiplication at the output. By closing or opening individual switches during the pulse, the output voltage V_n applied to the load impedance Z_L can be modulated according to the active number of

switches, as the pulse current can by-pass inactive stages via the free-wheeling diodes. Therefore, the output waveform can be chosen step-wise arbitrarily. As the beam energy in the GESA process is directly dependent on the acceleration voltage, a flat-top pulse is desirable [8]. Choosing a small stage voltage of 1 kV allows for a voltage ripple of less than 1 % of the maximum output voltage. Additionally, a vast number of switching elements and capacitors are available in the 1 kV range, benefiting the costs of those devices. By selecting a 1.2 kV IGBT instead of a device with an higher voltage rating, the switching losses can be reduced [9]. The fast switching circuitry used on each stage, the optical signal transmission and the EMI (Electro-Magnetic Interference) shielding has been described elsewhere [10].

B. Stage arrangement

As for any modular pulsed power source, significant effort was devoted to the arrangement of stages. A photograph of one stage can be seen in Fig. 2. In the picture, the clear separation from logic and gate drive components on the left hand side (no. 1) and the pulse switches (2), namely six 1200 V IGBTs (NGTB40N120IHLW - ON Semiconductor) and the two 100 µF capacitors (3), on the right hand side is visible.

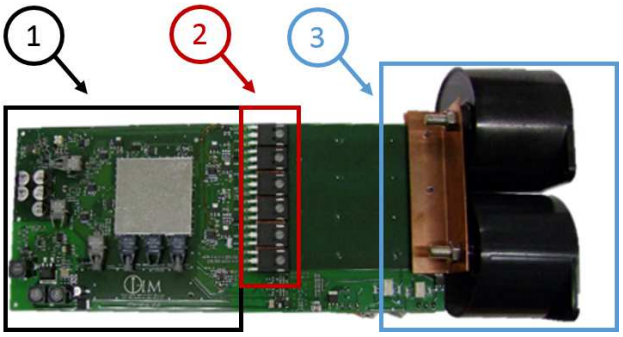
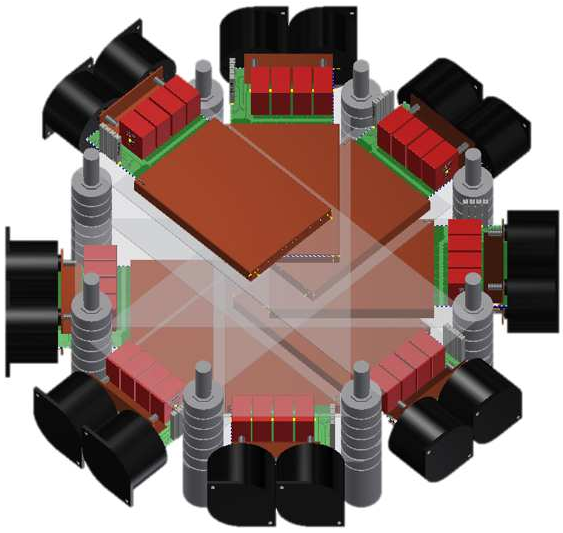


Fig. 2: Photo of one stage, showing the control circuitry (1), the pulse switches (2) and the pulse capacitors (3).

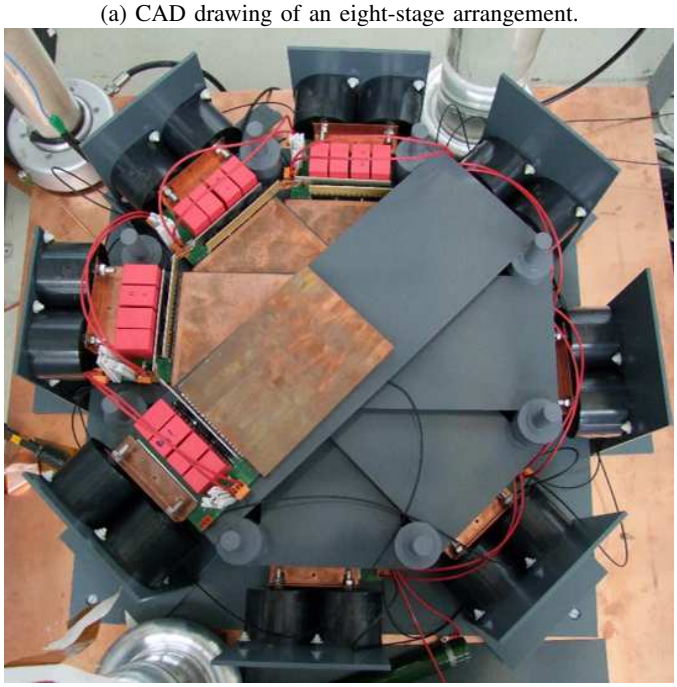
A low inductance connection between the stages as well as a low inductance output and return conductor is a basic requirement for a fast-rising output waveform. Fig. 3a shows a CAD drawing of an arrangement of up to eight stages, where the stages are inserted into a copper housing for adequate EMI shielding. The stages are arranged in a helical pattern. A diameter of 460 mm has been chosen according to the board width being the major spacial constraint. Due to the height of the shielding enclosure and the necessary isolation distance, the pitch of the arrangement results to 160 mm.

The load current passes next to the four red 1 µF capacitors upwards. Since the conductor carrying the load current is wound in a helical structure. A helical structure is commonly known for having a significant inductance, therefore FEM static magnetic field simulations (COMSOL, magnetic field module) were carried out to estimate the resulting inductance per turn (i.e. eight stages).

Fig. 4 (a) shows the model, a helical current path with the



(a) CAD drawing of an eight-stage arrangement.

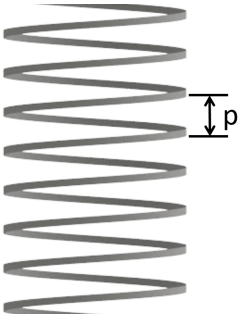


(b) Photo of the corresponding experimental setup.

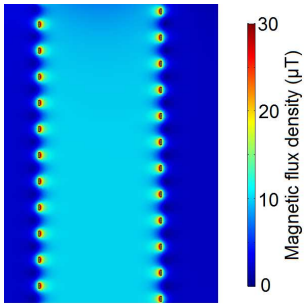
Fig. 3: Photo and CAD drawing of the eight-stage generator arranged in a helical pattern.

dimensions of the pulse current path as used in the generator and pitch p. The return (ground-) conductor passes on the outside of the cylindrical arrangement modeled by six sheets of copper forming a cuboid.

The magnetic field for a DC current of 1 A is depicted in Fig. 4 (b) for a small pitch of 50 mm with a significant field overlap from one turn to the next. The total inductance value has been derived from the total magnetic energy as delivered by the FEM simulation and divided by the number of turns. Therefore, the plotted inductance value per turn is a mean value. The inductance per turn as calculated from these simulations depending on the pitch is displayed in Fig. 5.



(a) Simulation model used in the inductance simulations. The path of the pulse current forms a helical coil with pitch p, connecting the stages.



(b) Result of a stationary magnetic field simulation using COMSOL for 1 A pulse current.

Fig. 4: Model (a) and magnetic field (b) of 3D stationary magnetic field simulations of the generator inductance.

As can be seen in the graph, the coupling between two turns only becomes important for a pitch much smaller than 200 mm by a strong increase in inductance. A larger pitch than 200 mm only slightly reduces the inductance while the physical dimensions of the generator become impractical. Since the simulations were carried out for DC, they neglect effects like induced eddy-currents. Due to the amount of copper close to the load current, induced currents will reduce the circuit inductance. Therefore, the calculated values can be seen as upper limit. The estimated inductance per turn amounts to 1.4 µH (see Fig. 5, red star). Thereby, the results confirm that the chosen arrangement offers a good trade-off between generator size and generator inductance.

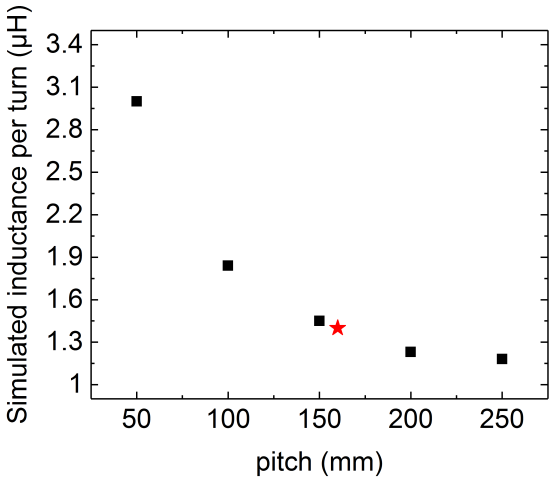


Fig. 5: Simulated inductance per turn (i.e. eight stages of the generator) as function of the pitch of the pulse current connection. The weak dependence of the inductance on the pitch ($p > 200$ mm) indicates a weak coupling of the conductor turns. The red star indicates the value used in the setup.

C. Control schematic

The total design output voltage of 120 kV demands for at least 120 stages with a stage voltage of 1 kV. There are different approaches for coping with voltage droop during the pulse caused by the gradual discharge of the pulse capacitors. Whereas some researches employ PWM compensation stages at the output of the generator [11], the presented design in this work activates spare stages once the output voltage has dropped by 1 kV. Thereby, the switching events – and therefore the switching losses – can be minimized for a given size of pulse capacitors. As discussed in [10], the total number of stages will amount to 150. The desired fast rise time of the output voltage demands a synchronized triggering of every stage. Additionally, the switching commands for creating the step-wise arbitrary output waveform have to be transferred to each stage. Using a powerful control circuitry with a direct fiber-optic link to each individual stage has been proven to work for some researches [12]. The high number of stages the presented design uses would demand for a highly complex control circuitry with 150 optical links. Since in this configuration each stage is merely a switch, such a control circuitry would have to generate the switching signals for every stage in real-time. Failure detection in such a generator arrangement is challenging, since the stages comprising a simple switch only usually are not able to identify malfunction. The design we propose in this paper is to equip each stage with a microprocessor running at 100 MHz clock speed responsible for the switching signal generation and a fast Complex Programmable Logic Device (CPLD) to implement all safety-relevant logic functions. The stages are then grouped in several modules. In each module, the stages are connected via an optical bus system. An illustration of this concept can be seen in Fig. 6.

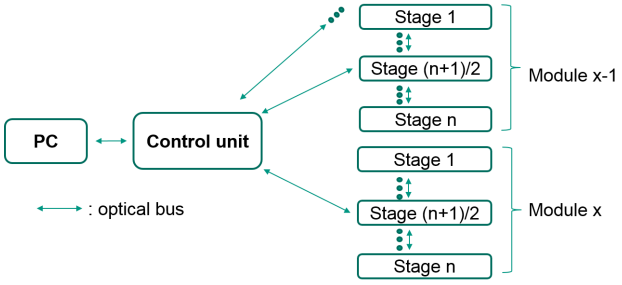


Fig. 6: Generator control schematic, consisting of a PC as user interface, the control unit responsible for addressing x individual modules and the optical bus connecting n stages within one module.

Prior to the pulse, the user enters the desired output voltage shape (e.g. the individual switching commands) via a PC. The PC transmits the data representing the output waveform to the control unit responsible for addressing the individual stages. The control unit only communicates directly with the middle stage in each module, which then forwards the signal to adjacent stages. Thereby, the data for operating each individual switch is stored and processed by the microprocessors locally on each stage. As data is transfered serially before pulse generation, the optical

connections from the generator to the control unit can be drastically reduced. After all stages are parametrized, the pulse is executed synchronized by transmitting a fast-rising trigger pulse. During the pulse, each stage generates its own switching commands off-line.

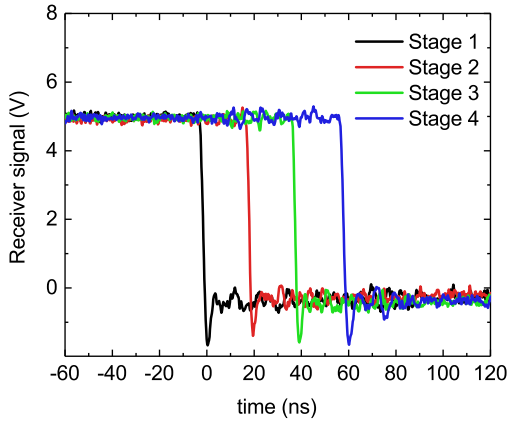


Fig. 7: Optical bus signals of four subsequent stages. Every stage transmits the signal with 20 ns delay, which is compensated for a synchronized pulse start.

Due to the bus connection, the trigger pulse is delayed by approx. 20 ns per stage. Fig. 7 shows the trigger signal for four subsequent stages in the bus. Since the time delay per stage is constant, it can easily be compensated. In Fig. 8, we measured simultaneously the gate signal of the pulse switches on four stages connected via the bus and overlapped 100 pulses. As can be seen, the residual jitter of the gate signal is in the order of 10 ns due to the temporal uncertainty introduced by the microprocessor running at 100 MHz.

The microprocessor enables advanced monitoring of each stage, since temperature and charging voltage can be measured. To prevent over-current conditions in case of external flash-over of the GESA device, each stage is equipped with a fast shunt resistor. During the pulse, each stage can send an emergency-off command to the control unit for switching off the generator in case of a detected failure. Therefore, the number of stages in one module is limited by the traveling time of the emergency-off signal to the main control unit. Using just one optical link for the whole generator is possible, but would lead to very high delay times for the emergency-off signal.

Fig. 9 sketches the connection of three stages in one module. On each stage, there is a control unit handling the communication and fault detection. Solid lines are logical signals on one stage, dotted lines indicate fiber optic links. Prior to pulse execution, (a), the signal sent from the main control unit is transmitted upwards (and downwards) to all stages. Addressing the individual stages is part of the transmission protocol. The response line to the main control unit acts comparable to a logical OR connection. Each stage can write data, overlapping telegrams are prevented by software. During the pulse, (b), the

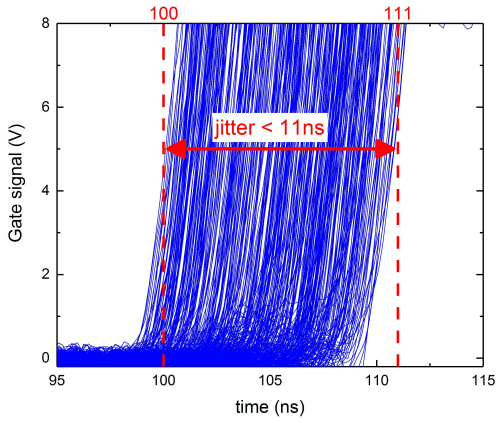


Fig. 8: Overlap of the gate signal at the beginning of one pulse measured at four stages simultaneously for 100 pulses. The resulting jitter is below 11 ns and is mainly determined by the limited clock speed (100 MHz) of the CPLD responsible for trigger signal recognition.

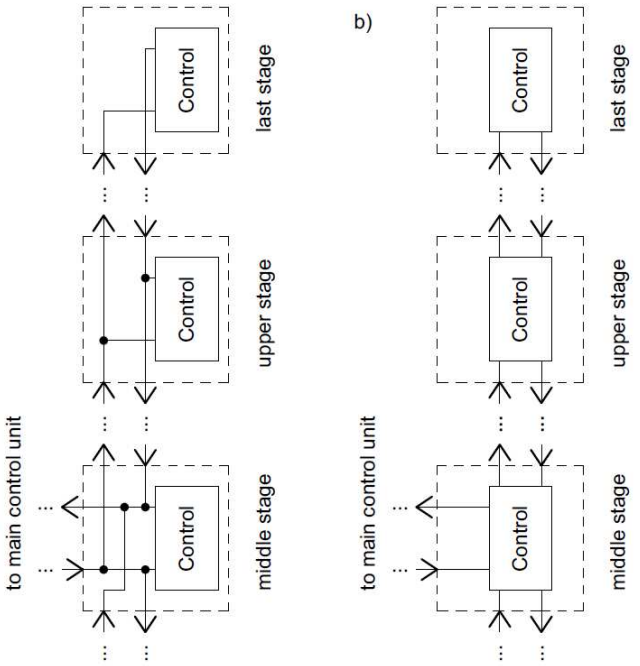


Fig. 9: Optical bus arrangement for an upper branch as displayed in Fig. 6.
(a): Signal path before the pulse. The control signal is forwarded to the last stage.
(b): Signal path during the pulse. Each stage can interrupt the optical chain in case of an error.

control unit continuously activates the fiber-optic transmitter's LED. If a stage is ready and has not detected any faults, it transmits incoming light to the upper stage (if the light is coming from below) and downwards (if the light is coming from above). The last stage in the branch, however, transmits the signal back downwards. A middle stage sends light to the

control unit only if it receives light from the neighboring stages above and below it (logical AND connection). In case a stage detects any faults, all transmitters are shut off. If a following stage detects a transmitter being deactivated, it is registered as emergency-off signal and this stage will also deactivate its transmitters. For the main control unit, fault detection on one branch is therefore reduced to detecting the light transmitted from the middle stage and, consecutively, deactivating all transmitters. The travel time for the emergency-off signal from the last stage to the control unit is therefore 20 ns delayed with each stage in the branch. Additionally, adjacent stages to the stage detecting the fault will start to turn off before the main control unit has to react - thereby already starting to clear the fault. The efficiency of this control scheme is proven in Sec. III-B. Fig. 10 shows a photo of the designed main control unit in its EMI shielding enclosure. The communication with all 150 stages will be possible with just 17 optical links.

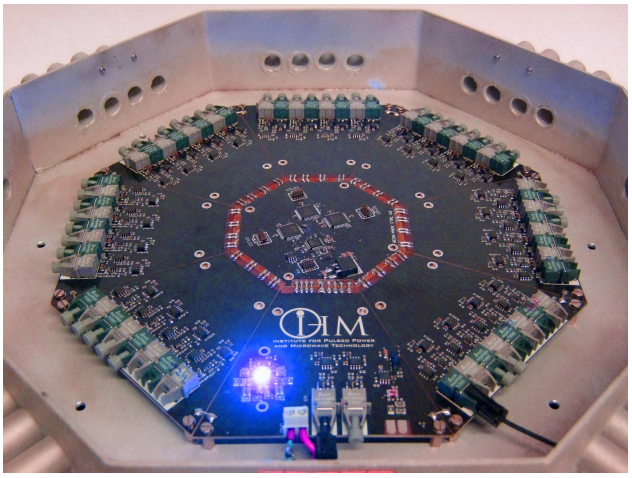


Fig. 10: The generator's main control unit in its EMI shielding enclosure. For the communication with all 150 stages, it uses 17 optical links.

III. Design validation

A. Fast arbitrary output waveforms

For demonstrating the generator's ability to create an arbitrary output waveform, up to eight stages were connected to form a small-scale generator. The generator was operated with a 13 Ω ohmic load. The output voltage was measured using a fast high voltage divider HVT-40-RCR from HILO-TEST, whereas the current was measured using a Pearson current monitor type 110. Rise and fall times and corresponding rise rates were calculated using the 10 % to 90 % definition. A photograph of the experimental setup can be seen in Fig. 3 (b).
Fig. 11 demonstrates that the generator is able to deliver a step-wise arbitrary output waveform with an output voltage of 7.6 kV at pulse currents of up to 600 A resembling our institute logo (IHM).
The rise time of the generator is mainly limited by the stray inductance. For this setup, the total inductance is approximately 1.4 µH, which is in agreement with the simulations presented in Sec. II-B.

Fig. 12a shows a magnification of the leading edge in Fig. 11. As can be seen, the current rise time is in the order of 108 ns.

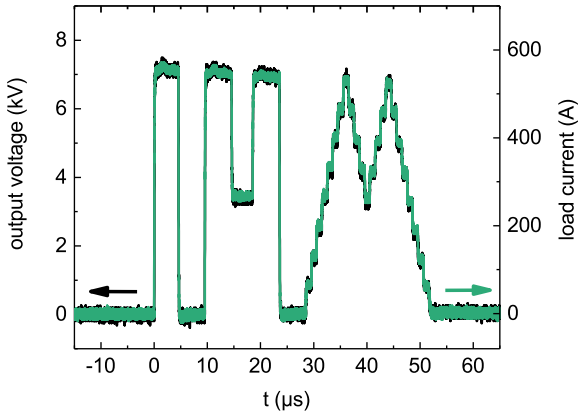


Fig. 11: Arbitrary output waveform as delivered by the generator connected to an ohmic load, resembling the IHM institute logo.

An increase of the load resistance to 50 Ω, see Fig. 12b, results in a decrease of current rise time to 40 ns.
The whole circuit can be seen as an ideal generator with an inherent rise time $t_{r,Gen}$ and a connected LR circuit with rise time $t_{r,LR}$:

$$t_{r,LR} = \frac{L}{R} \tag{1}$$

In a Gaussian system, the combined rise time as measured in the previous graphs can be calculated as the geometric sum of those values [13]:

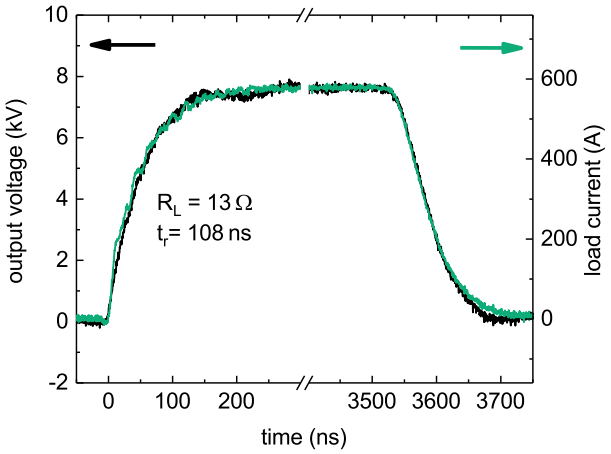
$$t_{r,Total} = \sqrt{t_{r,Gen}^2 + t_{r,LR}^2} \tag{2}$$

The inherent rise time of the generator can, hence, be calculated to $t_{r,Gen}$ = 28 ns. The same result is achieved when operating the generator with a very high value resistor close to open-circuit conditions as seen in Fig. 13. The oscillations are caused by the excitation of parasitic resonances. Due to the connected high voltage divider, the load now has a considerable capacitive component.

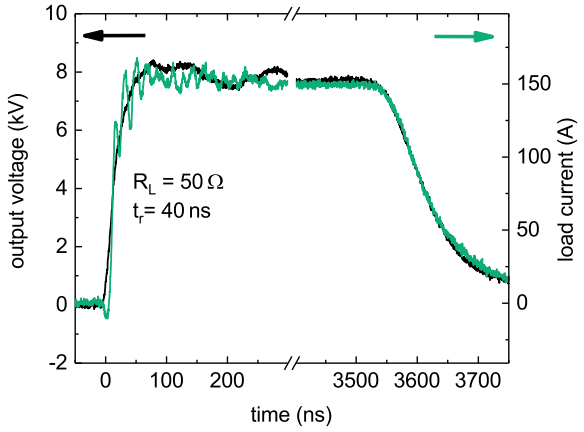
B. Dynamic load tests

Since the inherent plasma dynamics can cause the GESA cathode to suddenly short in certain modes of operation, fault tolerance is an important requirement for the generator [14]. When the resistance of the load decreases strongly, the load current will rise nearly linearly as limited by the driving voltage V_{Out} and the remaining circuit inductance L:

$$\frac{dI}{dt} = \frac{V_{Out}}{L} \tag{3}$$



(a) Output voltage and output current at nominal output current of 600 A.



(b) By reduction of the RL time constant, a high value ohmic load speeds up the generator rise time.

Fig. 12: Illustration of the influence of the load resistor on the generator rise time.

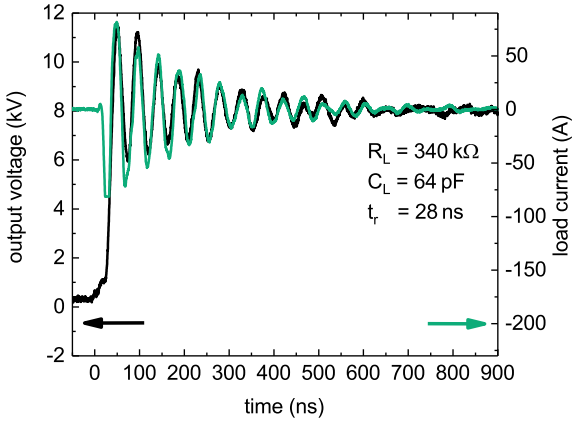


Fig. 13: Generator operated on a high-value ohmic load in near open circuit conditions.

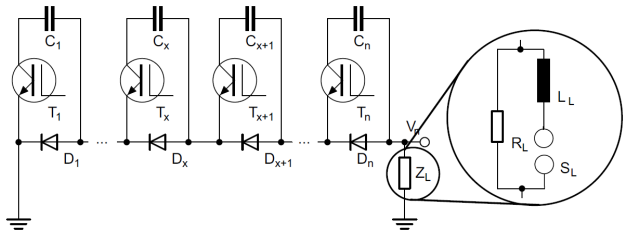


Fig. 14: For testing the behavior on dynamic loads, an additional inductance can be connected in parallel to the load during the pulse by means of a spark gap.

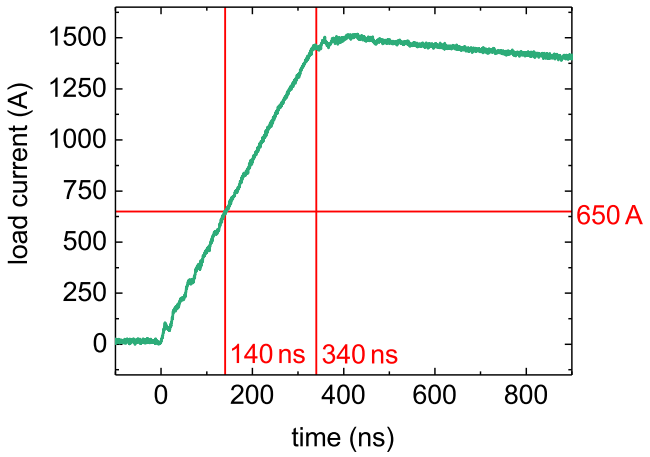
According to further FEM simulations, the total inductance of the GESA experiment after a flash-over, including the generator, will be in the order of 30 µH. The expected current rise time in case of a flash-over for 120 kV total output voltage will therefore be about 4 kA/µs.

For the following measurements, we used a 7-stage arrangement. The load resistor of the generator was replaced by a dynamic load as depicted in Fig. 14. Using a spark gap, an additional inductance can be connected in parallel to the load resistor during the pulse. The inductance is chosen such, that the resulting current rise rate for 7 kV output voltage matches the required 4 kA/µs.

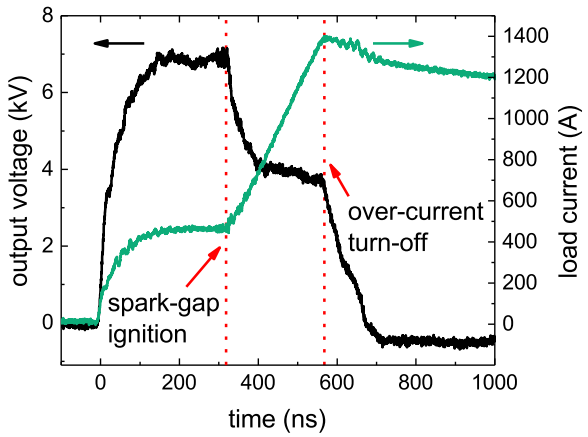
Two different scenarios have been considered: Fig. 15a shows the measured current when all stages are charged to a maximum voltage of 1 kV and the generator is discharged onto a short circuit. Therefore, the spark gap was shorted and the generator turned on onto a low-inductance short.

This turn-on fault may happen in case of an external flash-over or an ignition failure of the cathode plasma. The current rises linearly until the over-current threshold of 650 A is reached. Detecting the over-current condition at t = 140 ns, it takes approx. 100 ns for the control circuitry to turn off the switching devices. Due to the remaining charge carriers in the IGBTs, the time delay from the turn-off signal on the gate until the device starts blocking is around 100 ns. After a total of 200 ns, the generator turns off. Due to the high current rise rate the current crests at around 1.5 kA in this time. The six IGBTs used per stage are rated to a maximum pulsed current of up to 320 A each, resulting in a total maximum current capability of 1.9 kA, leaving enough safety margin for such short pulse lengths.

The second scenario is more likely, a so-called fault-under-load where the over-current fault occurs during the pulse. Fig. 15b shows a nominal pulse with 7 kV output voltage on 14 Ω load. The parallel spark-gap triggered 300 ns after pulse start. The measured voltage drops according to the resulting inductive voltage divider of generator and load. As discussed before, it takes around 200 ns for the generator to detect the fault and turn off. As can be seen, the current peaks around 1.4 kA in this case and again stays well below the specified maximum current rating of the switching devices.



(a) Current measurement of the generator turn-on onto a low inductive short.



(b) Dynamic load testing of the generator: the load is shorted around 300 ns after pulse start.

Fig. 15: Measurements of different fault scenarios.

The generator has therefore proven to protect itself in case of shorts at the load. However, due to the dead time related to the over-current detection and limited device speed, the current rise time has to be limited to the nominal value of below 4 kA/µs. Should measurements reveal the inductance of the final assembly being significantly below 30 µH, an additional current-limiting inductance will be introduced. As a flash-over is only expected at the load, this inductance can be connected in series to the output of the generator. Therefore, it does not hinder the charging process of the stray capacitances within the generator, not changing its fast output waveform.

IV. Conclusion

The GESA device investigated at IHM has high demands regarding its pulsed power supply. The presented approach uses a Marx-type generator with 150 stages at 1 kV stage voltage to achieve a total output voltage of 120 kV at an output current of 600 A for pulse length of up to 100 µs. For design validation, we presented the results of a small-scale version of the generator capable of delivering up to 8 kV at full load current. The generator's control chain using a fast optical bus for reduced control circuit complexity and increased safety against malfunction has proven to be effective. We could verify the generation of step-wise arbitrary output waveforms and the generators robustness against turn-on-fault and fault-under-load short circuit conditions. With these promising results, we currently are manufacturing the full-scale version of the generator to be able to conduct measurements on the GESA device in the near future.

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Martin Hochberg received the B. Sc. degree in Physics from Frankfurt University, Germany in 2011 and the Master 2 Recherche in Physics for Energetics from Grenoble INP, France together with the M.Sc. Degree in Physics from Karlsruhe Institute of Technology, Germany in 2014.
Currently, he is with Karlsruhe Institute of Technology, Institute for Pulsed Power and Microwave Technology, pursuing his PhD. His research interests include fast semiconductor switches, the design of pulsed power generators and the generation of intense electron beams.

Dennis Herzog received the B. Eng. degree in electrical engineering from Baden-Wuerttemberg Cooperative State University in 2016, Germany. Currently, he is with Karlsruhe Institute of Technology, Institute for Pulsed Power and Microwave Technology working on fast modular pulsed power sources, PEF treatment devices and high voltage components.

Martin Sack received the Diploma and Ph.D. degree in electrical engineering from Karlsruhe University, Karlsruhe, Germany, in 1995 and 2002, respectively. Since 2002 he is with Karlsruhe Institute of Technology, Institute for Pulsed Power and Microwave Technology (IHM) and since 2006 he is head of the research group "Pulsed Power Technologies and Systems" at IHM. His current research interests cover pulse generators and circuits for pulsed power applications, including industrial applications, fast switching, pulsed electric field (PEF) treatment of plant cells, measurement technology related to pulsed power and PEF treatment, and electromagnetic compatibility. Martin Sack is lecturer for "Electronic Devices and Electromagnetic Compatibility" at KIT, Department for Electrical Engineering and Information Technology.

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Alfons Weisenburger Biography not available.

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Wladimir An Biography not available.

Renate Fetzer Renate Fetzer received the Diploma degree in physics from the University of Ulm, Germany, in 2003 and the Ph.D. degree in natural sciences from the Saarland University, Saarbrücken, Germany, in 2006. From 2007 to 2009, she was a Research Associate with the University of South Australia, Adelaide, Australia. Since 2010, she has been a Senior Scientist with the Institute for Pulsed Power and Microwave Technology, Karlsruhe Institute of Technology, Germany. Her current research interests include the generation and characteristics of intense electron beams and material surface modification by pulsed electron beams.

Georg Mueller received the Diploma degree in physics and Ph. D. degree from the University of Karlsruhe, Germany, in 1990 and 1999 respectively. Since 1990, he was with the Research Centre Karlsruhe, where he worked in different research fields including thin film deposition by channel spark, plasma and electron beam diagnostics, development of multi point explosive emission cathodes, transport of large area powerful pulsed electron beams and surface modification by pulsed electron beams (GESA-process). He is author and co-author of more than 200 publications in peer reviewed journals, conference proceedings and two book chapters. He is member of the European Pulse Power Society, the International Advisory Committees of the HLMC-, BEAMS- and EAPPC-conferences and member of the contact expert group of the European Commission on transmutation and the OECD/NEA expert group on HLM. Since 2006 he is Deputy Director and Head of the Pulsed Power Department of the Institute for Pulse Power and Microwave Technology at Karlsruhe Institute of Technology (KIT). He is responsible and is involved in research and development of pulsed power applications in the field of electrodynamic fragmentation of solid dielectric materials, material surface modification by pulsed electron beams, electroporation of biological cell membranes by pulsed electric fields and basic research in bioelectrics.