High Voltage

Research Article

IET Journals
The Institution of Engineering and Technology

Transient voltage stresses in MMC–HVDC links – impulse analysis and novel proposals for synthetic laboratory generation

ISSN 2397-7264
Received on 13th September 2017
Revised 18th December 2017
Accepted on 24th January 2018
E-First on 15th March 2018
doi: 10.1049/hve.2017.0141
www.ietdl.org

Claudius Freye[1] ✉, Simon Wenig[2], Max Goertz[2], Thomas Leibfried[2], Frank Jenau[1]

[1]*Institute of High Voltage Engineering, TU Dortmund University, 44227 Dortmund, Germany*
[2]*Institute of Electrical Energy Systems and High-Voltage Technology, Karlsruhe Institute of Technology (KIT), 76131 Karlsruhe, Germany*
✉ *E-mail: claudius.freye@tu-dortmund.de*

Abstract: To evaluate and optimise insulation coordination concepts for state of the art high-voltage direct current (HVDC) transmission systems, appropriate test voltage shapes are required for laboratory imitation of occurring stresses. While especially transient voltages in the monopolar modular multilevel converter (MMC)–HVDC links show an extensive deviation from commonly applied switching impulse shapes, this study focusses on the analysis of over-voltages subsequent to direct current pole to ground faults. Additionally, novel methods for synthetic laboratory test voltage generation are proposed. Based on simulated transients occurring during fault scenarios in different symmetrical monopolar ±320 kV MMC–HVDC schemes, curve fitting, and related analysis techniques are used in order to compare simulated over-voltages with standard test voltage shapes. Moreover, these techniques further allow the identification of novel relevant impulse characteristics. Subsequently, design considerations for the generation of non-standard impulses based on single-stage circuits are derived and discussed. Those synthetically generated voltages may, later on, provide the basis for future investigations on related dielectric effects caused by those non-normative over-voltages.

1 Introduction

High-voltage direct current (HVDC) transmission is currently a vital part of the area of electric energy transmission technology. While modular multilevel converters (MMCs) have been steadily established due to their superior characteristics [1], insulation coordination aspects – especially if rated voltages increase even further – require additional investigations. Until now, applicable switching impulse (SI) test voltage ratings for MMC–HVDC monopolar configurations are not yet fully standardised compared with high-voltage alternating current [2, 3] and line commutated converter-HVDC schemes [4]. Nevertheless, recent research activities and provided case studies in the field of transient system simulations show a rising interest in corresponding overvoltage shapes [5–9]. While the latter research activities are mostly related to cable stresses, associated impacts on air clearance calculation [10] at the converter direct current (DC) busbar are still rare.

Even though calculation methods (e.g. [11]) based on normative standard impulses, such as lightning impulses and SIs, provide first steps towards insulation strategies, no general standard exists for voltage source converters [12]. Under consideration of [10], major differences between standard SI and occurring over-voltages are evident. To evaluate associated consequences for insulation coordination concepts, transient voltage stresses at the converter DC busbar in MMC–HVDC schemes need to be evaluated, analysed and compared with normative impulses in greater detail. Furthermore, besides theoretical influence analysis based on accessible test data results, novel proposals to generate non-standard laboratory test voltage waveforms need to be derived.

2 Transient simulation of MMC–HVDC transmission schemes

To cover the variety of available transmission technologies and different corridor lengths in recent MMC–HVDC projects, different monopolar schemes are investigated in this contribution as visualised in Fig. 1. The following paragraphs provide a brief overview of the selected technical system parameters, on the different scenarios and load flow set points as well as on implemented system protection loops. An appropriate simulation time step is selected as slow-front transient events shall be evaluated [4].

2.1 System modelling

Converter and system modelling are of significant importance to derive feasible results in transient time domain investigations. According to [13], a consensus on implementation possibilities has

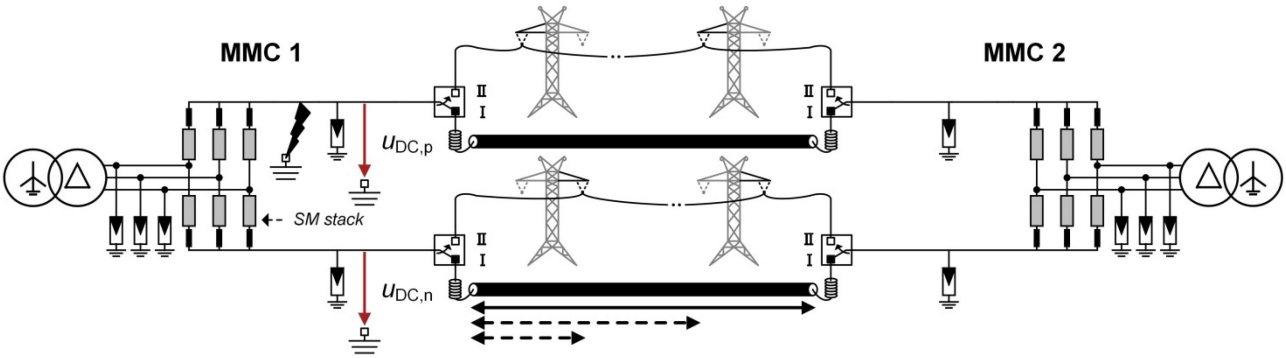

Fig. 1 *Scheme of investigated MMC–HVDC links with different transmission technologies and variable transmission length*

Table 1 Utilised surge arrestor *V–I* curve

Voltage level, pu	1.366	1.403	1.441	1.494	1.600	1.706	1.790	1.940	2.014
Arrestor current, kA	0.0001	0.001	0.01	0.1	1	4	10	50	100

Table 2 Main technical MMC station parameters

Parameter	Description	Value
P_r, Q_r	rated power	1 GW, 300 MVA
C_{SM}	sub-module capacitor	8500 μF
N_{SM}	number of modules per arm	320
L_{arm}	arm inductance	50 mH
$u_{DC,r}$	rated DC transmission voltage at voltage controlled station	$\pm$320 kV
u_{AC}/u_{conv}	converter transformer ratio	400/330 kV
$\Delta t_{control}$	converter control system delay	50 μs

Table 3 Investigated scenarios for characteristic overvoltage shape determination

Scenario ID	Transmission system	Active Power set point @ PCC of MMC1
O-150a	150 km OHL	1 GW AC in-feed
O-150b	150 km OHL	1 GW AC export
C-150a	150 km XLPE cable	1 GW AC in-feed
C-150b	150 km XLPE cable	1 GW AC export
C-100a	100 km XLPE cable	1 GW AC in-feed
C-100b	100 km XLPE cable	1 GW AC export
C-50a	50 km XLPE cable	1 GW AC in-feed
C-50b	50 km XLPE cable	1 GW AC export

been defined, where the selected classification (*Types* 1–7) is related to the underlying study purpose. Within the context of this simulation framework, either *Type* 3 for single sub-module related faults or *Type* 4 (computationally improved) Thévenin equivalent representations [14, 15] for other system faults are utilised. Further in depth analysis related to insulated-gate bipolar transistor (IGBT) and diode modelling is elaborated in [16], where appropriate conformity of non-linear and simplified (on-/off-resistance) power electronic device representations is identified. As a remark it should be noted that switching actions of power electronic devices (e.g. changing diode conduction states) require appropriate software-specific electromagnetic transients (EMT) solving techniques in addition to suitable modelling approaches. Besides, frequency dependent XLPE cable and overhead line (OHL) models are considered as short circuit faults and the following sub-module blocking events are investigated. Especially an appropriate representation of a travelling wave phenomenon is inevitable to determine transient voltage overshoots with an acceptable accuracy at the DC clamps. In addition, surge arrestor columns have a severe impact on the system overvoltage level as well as on shape and need to be modelled carefully. Due to the fact that slow-front transients are in the scope of this contribution, a non-linear *V–I*-curve with regard to this type of stimulus has been selected and is implemented accordingly. This leads to the related SI protective level of 512 kV (1.6 pu) @ 1 kA discharge current. The detailed *V–I* characteristics related to a 30/60 μs current shape are attached within Table 1, while other relevant system parameters are summarised in Table 2.

2.2 Transmission scenarios

Besides basic design, the selected transmission technology as well as different power transfer set points influence shape and severity of over-voltages due to inherently different system conditions. To address these differences appropriately, in total eight scenarios are further evaluated. Hereby, varying fault resistances (between 1 mΩ – 30 Ω) during a DC pole to ground fault at the positive pole of MMC 1, as depicted in Fig. 1, are investigated. The directly affected station MMC 1 is a DC current controlled converter, MMC 2 at the opposite end acts as the DC voltage regulating station. Additionally, both converters obtain a reactive power reference of +300 MVA (cap.). An overview of all scenarios is provided in Table 3.

2.3 System protection

To derive feasible over-voltages, appropriate system behaviour after fault inception is required. Therefore, the implementation of protection loops at both converter stations of the MMC–HVDC link is an essential aspect to be considered. In contrast to ideal (non-delayed) converter blocking subsequent to arbitrary DC faults, results considering current and voltage thresholds, protection delays and measurement-quantity-triggered module blocking provide more realistic results in terms of accuracy. Especially the latter issue leads to time-shifted travelling wave phenomena affecting the transmission system. This has a significant influence on transient voltage peaks, their instant and maximum level.

This contribution considers both a simple converter arm overcurrent and a DC pole to ground voltage imbalance detection concept. The scheme has been initially proposed and described in [10]. While the overcurrent threshold is related to technical boundaries of state of the art IGBTs (maximum allowed peak current 2.7 kA), the voltage imbalance criterion is related to a deviation from normal operation conditions (imbalance > 50 kV). A brief overview of this scheme and relevant parameters is shown in Fig. 2.

3 Transient simulation results

Based on the underlying simulation framework introduced in Section 2, results obtained using PSCAD™–EMTDC™ with a simulation time step 5 µs for the OHL and 25 µs for the different cable schemes are presented in the following paragraphs. Besides a discussion of main characteristics like general shape, rate of rise and remaining steady state levels, results for the different transmission scenarios are additionally compared amongst each other.

3.1 Scenario OHL 150 km

For an OHL transmission setting with a total length of 150 km, transient over-voltages at the healthy pole of MMC 1 are shown in

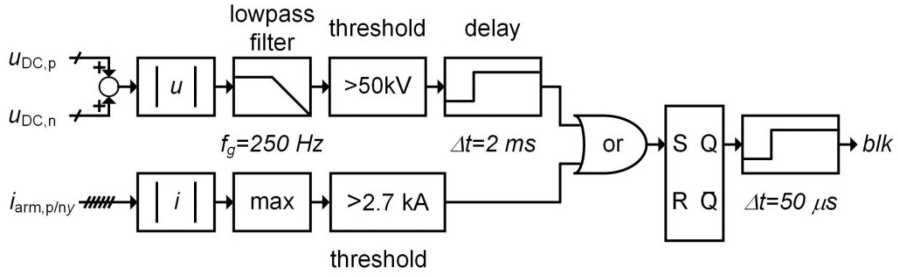

Fig. 2 *Implemented MMC protection loops*

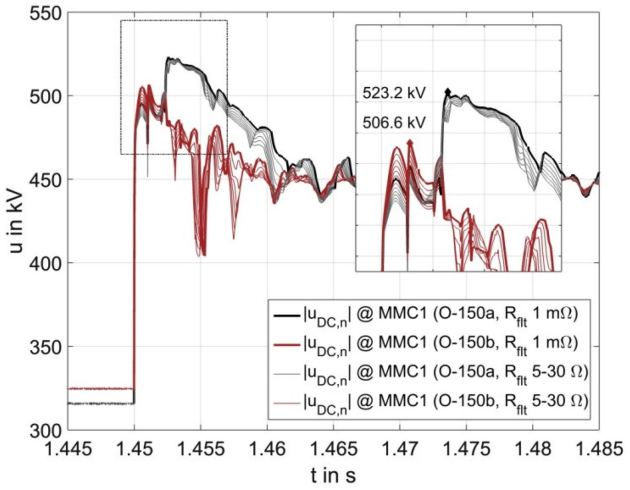

Fig. 3 *Transient overvoltage at the negative DC pole of MMC1 (absolute voltage values, fault instant t_{flt} = 1.45 s) for 150 km OHL (O-150)*

Fig. 3. Due to the relatively small line capacitance, a rapid voltage overshoot takes place, which shows a rising edge to ∼ 1.63 pu significantly faster (< 50 μs) than a standard SI test voltage envelope. Besides, a significant influence of pre-fault power transfer on the occurring maximum peak and a minor impact on fault resistance on the maximum peak value can be observed. A post-fault steady state is not reached within the simulated duration, as it is assumed that the alternating current (AC) circuit breakers and DC grounding switches do not operate. Therefore, we see remaining (i) slowly damped oscillations due to resonant excitation caused by module blocking directly connected to the healthy DC pole and (ii) coupling effects on the transmission line caused by the diode rectifier behaviour of half-bridge MMCs subsequent to DC pole to ground faults at the faulted pole.

3.2 Scenario cable 150/100/50 km

In Figs. 4*a*–*c*, transient over-voltages of the MMC-HVDC link with different cable transmission lengths (150, 100, 50 km) are shown. Voltages are recorded at the healthy pole of MMC 1. Again, a significant influence on pre-fault power transfer on the occurring maximum peak as well as a moderate influence of the present fault resistance can be observed. Generally – caused by the cable segments in contrast to an OHL scheme – the highest overvoltage peak is reached within a timeframe of one to several milliseconds instead of microseconds. A post-fault steady state is reached at ∼ 1.42 pu when surge arrestors re-enter their normal operation high impedance region. In case no further action is triggered, this level remains nearly constant as arrestors only discharge the system with negligible leakage currents and intrinsic cable discharge occurs within a much longer timeframe up to several minutes.

While especially recent offshore MMC-HVDC links for wind farm connection are relatively short regarding the transmission distance, which is reflected in the last scenario cable 50 km shown in Fig. 4*c*, the visible initial voltage post-fault step nearly disappears. Generally, due to reduced wave travelling times, occurring converter-individual effects become blurred and are more challenging to be differentiated based on the obtained transients. System behaviour tends towards the initial OHL response in terms of general shape, as overall system capacitance continues to decrease for a shorter cable length.

4 Evaluation methods

Insulation coordination which either follows well-established standards known from AC [2, 3] or is based on guidance for line commutated HVDC converters [4] aims for the determination of withstanding voltages (U_w). These withstand voltages are related to their corresponding representative voltages and over-voltages (U_{rp}) determined by system analysis. During the converter design stage focusing on transient phenomena, the determination of representative voltages and over-voltages is inevitably linked with fault scenario analysis, as shown in Section 3. To evaluate and compare those results, derived and applied methods which allow a simulation data reduction (SDR) followed by different overvoltage approximations concepts and related evaluations are presented in the following.

4.1 Simulation data reduction

In a first step, maximum occurring over-voltages based on an extensive set of simulations for each scenario need to be determined. Therefore, data is condensed into one worst-case voltage-time curve $u_{SDR}(t)$ for $t_{flt} \le t \le t_{sim,max}$. This voltage time curve consists of the maximum absolute voltage per time step and scenario. As a major difference compared with [10], different power flow configurations (sub-scenarios a and b) are not considered separately, aiming in the derivation of a more generic voltage time curve in dependence on transmission technology (IDs: O-150, C-150, C-100, C-50).

4.2 Derived methods for over-voltage approximation

Influences of SI voltages superimposed on a DC pre-stress are investigated in [17, 18]. Here it is concluded that for practical external air insulation influences of DC pre-stress may be disregarded, if instead impulses having the combined amplitude $U_{SI} + U_{DC}$ are considered. As concluded in [10], voltage shapes differ significantly from any normative SI, therefore a deeper analysis of impulse shapes is required.

4.2.1 Estimation of SI amplitudes (SI estimation): Voltage time behaviour of normative SI is described using the solution for the differential equation of single-stage equivalent circuits for impulse voltage generation [19]

$$u(t) = U_A \cdot \left[e^{-\alpha_1 t} - e^{-\alpha_2 t}\right] \quad (1)$$

where U_A instead of $(U_0/K) \cdot (1/(\alpha_2 - \alpha_1))$ is used. For normative SI $1/\alpha_1$ yields to $1/\alpha_1 = 3155.0\ \mu s$ and $1/\alpha_2 = 62.48\ \mu s$, respectively.

Instead of using simplified peak amplitudes only, (1) allows the determination of U_A using least-squares solution techniques for non-linear curve-fitting problems. Generally, Levenberg–Marquardt algorithm may be chosen, whereas solution techniques using the trust-region-reflection (TRR) method also achieve similar results. For this purpose, the TRR method is chosen.

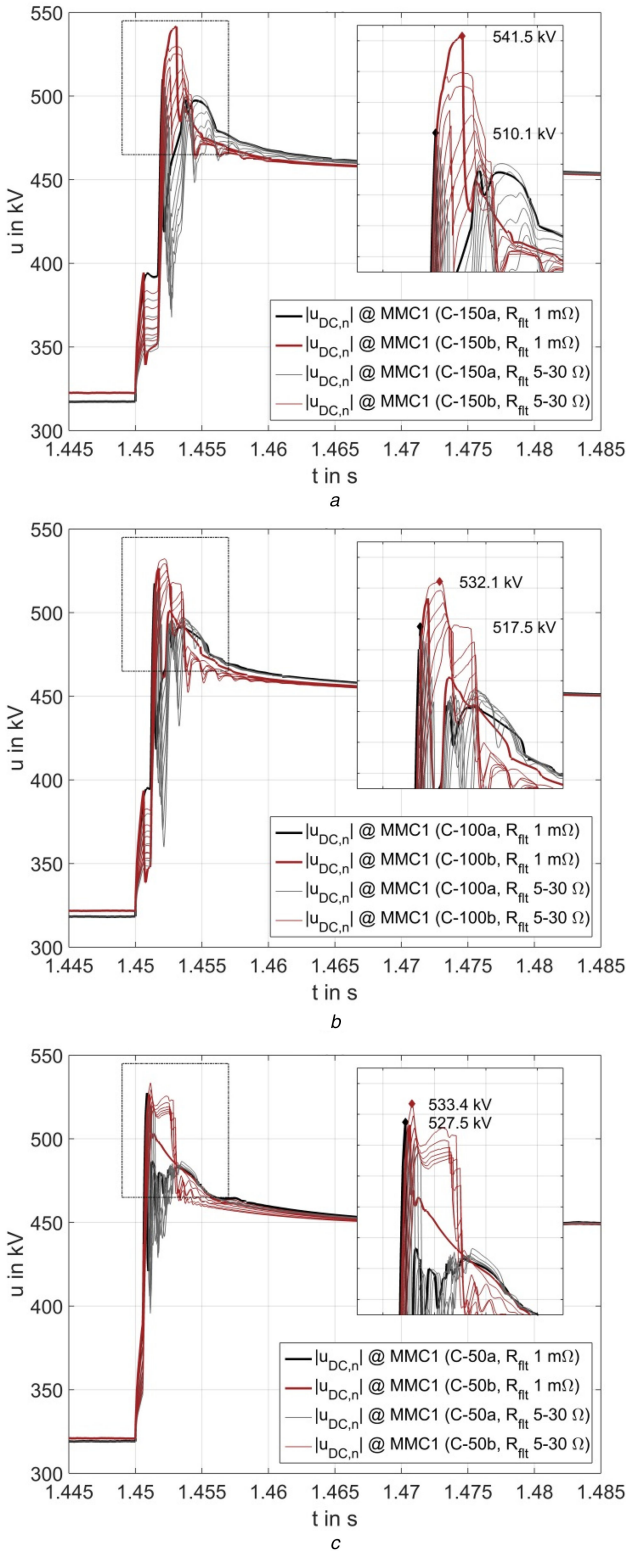

Fig. 4 *Transient overvoltage at the negative DC pole of MMC1 (absolute voltage values, fault instant $t_{flt} = 1.45$ s) for*
(a) 150 km XLPE Cable (C-150), ***(b)*** 100 km XLPE Cable (C-100), ***(c)*** 50 km XLPE Cable (C-50)

4.2.2 Double exponential impulse (DEI) estimation: With the objective of improving the approximation by a DEI on simulated data, the degree of freedom in (1) is increased allowing the approximation of U_A, α_1 and α_2. Resulting exponential impulses (u_{DEI}) contain fault related transients and steady state DC voltage prior to the fault.

4.2.3 Superimposed DEI estimation: Known from HVDC cable tests [20] and motivated by previous considerations presented in [10], superimposed testing is considered as a promising approach for laboratory imitation of obtained over-voltages and for identification of relevant overvoltage impulse parameters. Therefore, DC steady-state operational voltage prior to the fault is subtracted and DEI estimation is carried out in order to obtain u_{SDEI}. This approximation is especially meaningful as it allows the determination and discussion of relevant circuit parameters for a laboratory imitation of simulated over-voltages utilising superimposed double exponential impulses (SDEIs).

4.3 Derived methods for evaluation of overvoltage approximation

To evaluate the goodness of derived overvoltage approximations and to highlight major differences between considered scenarios, different criteria are used. For an assessment of the voltage curve approximation over an evaluation time window $t_{flt} \leq t \leq t_{eval}$ the method uses the basic idea of voltage–time areas. The overall peak voltage approximation is rated using parameter $q_{fit,max}$, whereas parameter $q_{fit,A}$ is used to quantify overall voltage approximation

$$q_{\mathrm{fit,A}} = \left(\int_{t_{\mathrm{flt}}}^{t_{\mathrm{eval}}} u_i(t)\mathrm{d}t\right)\left(\int_{t_{\mathrm{flt}}}^{t_{\mathrm{eval}}} u_{\mathrm{SDR}}(t)\mathrm{d}t\right)^{-1}. \tag{2}$$

In the case of SI estimation $u_i = u_{SI}(t)$, in the case of DEI estimation $u_i = u_{DEI}(t)$ and in the case of SDEI estimation $u_i = u_{SDEI}(t) + U_{DC}(t_{flt})$ are considered. Besides this, amplitude comparison uses $q_{fit,max}$ introduced as

$$q_{\mathrm{fit,max}} = \hat{u}_i \cdot \hat{u}_{\mathrm{SDR}}^{-1} \tag{3}$$

focusing on obtained maximum voltages with the same underlying restrictions as for (2).

4.4 Derived methods for quantification of transmission technology influences

The quantification of influences related to chosen transmission technologies is carried out based on the evaluation of suitable voltage time approximations. For this aim, parameters such as time to peak (t_p) and time to half (t_{50}) ratios are used. Parameter q_p allows time to peak, q_{50} time to half and factors $q_{A,\infty}$ and $q_{A,eval}$ voltage time curve area comparison. Quantities follow

$$q_{\mathrm{p}} = t_{\mathrm{p,e}} \cdot t_{\mathrm{p,d}}^{-1}, \tag{4}$$

$$q_{50} = t_{50,\mathrm{e}} \cdot t_{50,\mathrm{d}}^{-1}, \tag{5}$$

$$q_{\mathrm{A},\infty} = \left(\int_{t_{\mathrm{flt}}}^{t\to\infty} u_{i,\mathrm{e}}(t)\,\mathrm{d}t\right)\left(\int_{t_{\mathrm{flt}}}^{t\to\infty} u_{i,\mathrm{d}}(t)\mathrm{d}t\right)^{-1}, \tag{6}$$

$$q_{\mathrm{A,eval}} = \left(\int_{t_{\mathrm{flt}}}^{t_{\mathrm{eval}}} u_{i,\mathrm{e}}(t)\mathrm{d}t\right)\left(\int_{t_{\mathrm{flt}}}^{t_{\mathrm{eval}}} u_{i,\mathrm{d}}(t)\mathrm{d}t\right)^{-1} \tag{7}$$

each using suitable overvoltage approximations for $u_{i,e}(t)$, $t_{p,e}$, $t_{50,e}$ as the enumerator and for $u_{i,d}(t)$, $t_{p,d}$, $t_{50,d}$ as the denominator. Time parameters for time to half values are obtained using the numerical solution of (1).

5 Over-voltage analysis

This section is separated into four parts. First, obtained results for overvoltage approximation using different fitting horizons are shown and associated impacts are discussed. This results in the selection of a suitable evaluation time window for further analysis. Second, the evaluation of the voltage curve approximation is presented. Third, differences in chosen transmission technologies are investigated. Last, key results for overvoltage approximation and analysis are summarised.

Table 4 Obtained curve parameters based on applied methods following Sections 4.2.1–4.2.3 in dependence on chosen curve fitting horizons (*I*)

	$t_{flt} \le t \le t_{sim,max}$			
	DEI			SI
	t_p in µs	t_{50} in ms	$\hat{U}$ in kV	$\hat{U}$ in kV
O-150	35	704.2	477.5	946.2
C-150	675	6424.1	456.0	852.1
C-100	675	5756.4	455.1	873.4
C-50	675	5622	453.7	898.7

	$t_{flt} \le t \le t_{sim,red,100}$			
	DEI			SI
	t_p in µs	t_{50} in ms	$\hat{U}$ in kV	$\hat{U}$ in kV
O-150	35	804.9	473.9	946.2
C-150	775	1404.9	466.1	852.1
C-100	775	1475.1	464.3	873.4
C-50	750	1649.3	462.3	898.7

	$t_{flt} \le t \le t_{sim,max}$			
	SDEI			
	t_p in µs	t_{50} in ms	$\hat{U}_{DC+I}$ in kV	$\hat{U}_I$ in kV
O-150	140	136.8	492.7	168.2
C-150	5775	1657.8	456.9	134.4
C-100	4125	1517	455.8	134.1
C-50	2550	1503.5	454.2	133.4

	$t_{flt} \le t \le t_{sim,red,100}$			
	SDEI			
	t_p in µs	t_{50} in ms	$\hat{U}_{DC+I}$ in kV	$\hat{U}_I$ in kV
O-150	95	221	475.4	150.9
C-150	5200	322.4	469.2	146.7
C-100	3775	362.9	466.3	144.6
C-50	2350	438.3	463.3	142.5

Table 5 Obtained curve parameters based on applied methods following Sections 4.2.1–4.2.3 in dependence on chosen curve fitting horizons (II)

	$t_{flt} \le t \le t_{sim,red,60}$			
	DEI			SI
	t_p in µs	t_{50} in ms	$\hat{U}$ in kV	$\hat{U}$ in kV
O-150	35	385.5	484.6	946.2
C-150	850	711.4	471.7	852.1
C-100	850	651.1	471.1	873.4
C-50	825	667.7	469.3	898.7

	$t_{flt} \le t \le t_{sim,red}$			
	DEI			SI
	t_p in µs	t_{50} in ms	$\hat{U}$ in kV	$\hat{U}$ in kV
O-150	40	203.1	497.1	946.2
C-150	900	486.8	475.1	852.1
C-100	950	377.1	476.9	873.4
C-50	900	328.9	477.1	898.7

	$t_{flt} \le t \le t_{sim,red,60}$			
	SDEI			
	t_p in µs	t_{50} in ms	$\hat{U}_{DC+I}$ in kV	$\hat{U}_I$ in kV
O-150	115	107.2	487.1	162.6
C-150	4950	151.7	476.8	154.3
C-100	3575	157.2	474.3	152.7
C-50	2200	178.3	470.9	150

	$t_{flt} \le t \le t_{sim,red}$			
	SDEI			
	t_p in µs	t_{50} in ms	$\hat{U}_{DC+I}$ in kV	$\hat{U}_I$ in kV
O-150	**155**	**58.4**	**500.3**	**175.8**
C-150	**4775**	**90.1**	**482.8**	**160.3**
C-100	**3425**	**88.5**	**481.4**	**159.7**
C-50	**2100**	**89.3**	**479.2**	**158.3**

5.1 Over voltage approximation

Considered curve fitting horizons are closely linked to potential post fault measures within the system. Initially, as previously shown in [10], subsequent to $t_{flt} = 1.45$ s no further overvoltage reduction measures till $t_{sim,max} = 1.84$ s are assumed. In contrast, assuming feasible AC circuit breaker opening delays prior to related DC de-energisation measures yield reduced overvoltage durations and therefore to a shorter curve fitting horizon. The reduced horizon is, in this case, limited to $t_{sim,red} = t_{flt} + 40$ ms, corresponding to two AC grid cycles after the fault. For the purpose of identifying influences related to additional delays, e.g. due to fault detection or AC breaker restrikes, additional cases are considered using $t_{sim,red,60} = t_{flt} + 60$ ms and $t_{sim,red,100} = t_{flt} + 100$ ms. Related impulse parameters are shown in Tables 4 and 5.

Results of overvoltage approximation for 150 km OHL and 150 km cable transmission based on SDR voltage time curves using the reduced curve fitting horizon $t_{flt} \le t \le t_{sim,red} = t_{flt} + 40$ ms are presented in Fig. 5. From the first impression, results appear similar to those presented in [10] using the increased curve fitting horizon ($t_{flt} \le t \le t_{sim,max} = t_{flt} + 390$ ms) but show greater deviations if impulse parameters shown in Tables 4 and 5 are taken into account.

In the case of cable transmission, time to half values decrease and impulse amplitudes increase when the chosen fitting horizon is shortened. Furthermore, a slight reduction of time to peak values in case of SDEI is observed, whereas a reduction in horizon length leads to a slight increase of time to peak values for DEI impulses. Considering OHL transmission (O-150) sporadic discrepancies on those observations arise which are related to the chosen curve fitting methods in the least square sense.

Nevertheless, it is obvious, if no countermeasures are considered, time to half values are tremendously long. Especially in the case of cable transmission technology, this is leading to values being up to 18 times larger for DEI and SDEI estimation. Whereas, if a reduced fitting horizon of $t_{flt} \le t \le t_{sim,red}$ is used, time to half values are reduced from several seconds to milliseconds. Therefore, it is considered more reasonable to focus on obtained curve parameters taking into account the reduced curve fitting horizons related to overvoltage reduction measures.

Time to peak values is less affected by post fault behaviour. Furthermore, it is evident for SDEI impulses that time to peak decreases with a reduction of cable length, whereas the shortest time to peak is found for OHL. Besides this, SDEI impulses clearly show that time to half values is minor affected by cable length, but

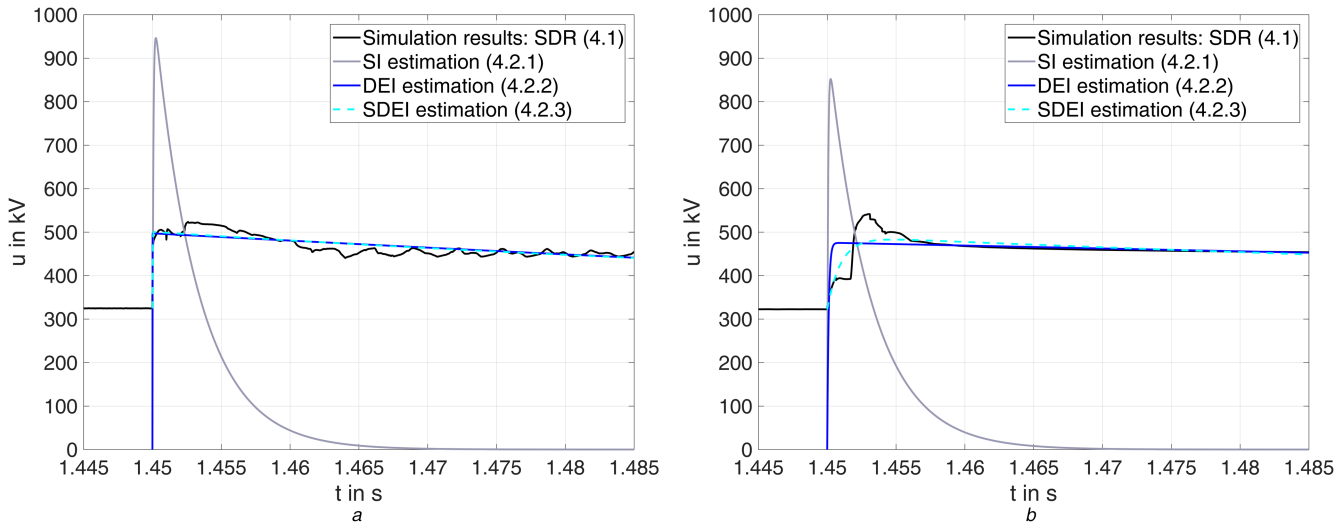

Fig. 5 *Overvoltage approximation for*
(a) 150 km OHL (O-150) considering further overvoltage reduction measures (curve fitting horizon $t_{\mathrm{flt}} \leq t \leq t_{\mathrm{sim,red}} = t_{\mathrm{flt}} + 40\,\mathrm{ms}$), ***(b)*** 150 km cable (C-150) considering further overvoltage reduction measures (curve fitting horizon $t_{\mathrm{flt}} \leq t \leq t_{\mathrm{sim,red}} = t_{\mathrm{flt}} + 40\,\mathrm{ms}$)

Table 6 Fitting evaluation in dependence on chosen curve fitting horizons

Curve fitting horizon $t_{\mathrm{flt}} \leq t \leq t_{\mathrm{sim,max}}$ and $t_{\mathrm{eval}} = t_{\mathrm{flt}} + 40\,\mathrm{ms} = t_{\mathrm{sim,red}}$

	SI			DEI			SDEI	
	$q_{\mathrm{Fit,A}}$ in %	$q_{\mathrm{Fit,max}}$ in %		$q_{\mathrm{Fit,A}}$ in %	$q_{\mathrm{Fit,max}}$ in %		$q_{\mathrm{Fit,A}}$ in %	$q_{\mathrm{Fit,max}}$ in %
O-150	17.4	180.8	O-150	100.8	91.3	O-150	102.6	94.2
C-150	15.8	157.4	C-150	98.5	84.2	C-150	98.3	84.4
C-100	16.2	164.1	C-100	98.6	85.5	C-100	98.6	85.6
C-50	16.8	168.5	C-50	98.8	85.1	C-50	98.8	85.2

Curve fitting horizon $t_{\mathrm{flt}} \leq t \leq t_{\mathrm{sim,red}}$, and $t_{\mathrm{eval}} = t_{\mathrm{flt}} + 40\,\mathrm{ms} = t_{\mathrm{sim,red}}$

	SI			DEI			SDEI	
	$q_{\mathrm{Fit,A}}$ in %	$q_{\mathrm{Fit,max}}$ in %		$q_{\mathrm{Fit,A}}$ in %	$q_{\mathrm{Fit,max}}$ in %		$q_{\mathrm{Fit,A}}$ in %	$q_{\mathrm{Fit,max}}$ in %
O-150	17.4	180.8	O-150	100	95.0	O-150	**100**	**95.6**
C-150	15.8	157.4	C-150	99.9	87.7	C-150	**100**	**89.2**
C-100	16.2	164.1	C-100	99.9	89.6	C-100	**100**	**90.5**
C-50	16.8	168.5	C-50	99.9	89.5	C-50	**100**	**89.8**

by transmission technology leading to the shortest values being found for OHL.

A quantification of the voltage curve approximation is carried out in the next section.

5.2 Evaluation of over-voltage approximation

To evaluate the goodness of the overvoltage approximation, methods introduced in Section 4.3 are applied leading to results shown in Table 6. The evaluation window boundary is equalised to $t_{\mathrm{eval}} = t_{\mathrm{flt}} + 40$ ms in order to guarantee a consistent investigation of all voltage curve approximations independent of the chosen curve fitting horizon.

It is found that voltage time areas $q_{\mathrm{Fit,A}}$ are for SI within the range of about $\overline{q_{\mathrm{fit,A}}} = 16.55\%$. Therefore, voltage time areas are significantly smaller in the case of SI approximation compared with simulated over-voltages. Furthermore, occurring SI peak voltages $\overline{q_{\mathrm{fit,max}}} = 167.7\%$ are leading to peak stresses being roughly 1.7 times higher compared with obtained simulation results. Approximations of $q_{\mathrm{fit,A}}$ and $q_{\mathrm{fit,max}}$ are found unaffected for SI approximation if either extended or reduced curve fitting horizon is chosen. This is related to the aspect that only parameter U_{A} is determined and the overall duration of normative SI compared with chosen curve fitting horizon and evaluation window is rather short, causing minor effects on related results. Changes are observed for DEI and SDEI approximation methods as the degree of freedom for the underlying optimisations is significantly increased.

Voltage curve approximation is utilising curve fitting methods which are carried out in the least square sense. Therefore, from a mathematical perspective, it is a causal consequence that those overvoltage approximations using equal curve fitting horizon and evaluation window will obtain superior results in terms of voltage time areas $q_{\mathrm{fit,A}}$, whereas, this is not necessarily valid for evaluation of peak voltage approximation $q_{\mathrm{fit,max}}$.

These findings are noticeable if $q_{\mathrm{fit,A}}$ and $q_{\mathrm{fit,max}}$ for DEI and SDEI impulses are considered. As the value chosen for t_{eval} is identical with $t_{\mathrm{sim,red}}$, approximations using the reduced curve fitting horizon are leading to a perfect reconstruction of the voltage time area. Contrary, if the extended curve fitting horizon is considered all evaluation parameters are smaller, as discussed above. Evaluation value $q_{\mathrm{fit,max}}$ indicates that representation of simulated over-voltages is less accurate if DEI approximation is chosen. Good results are obtained using SDEI approximation utilising the reduced curve fitting horizon ($t_{\mathrm{flt}} \leq t \leq t_{\mathrm{sim,red}}$). Therefore, it can be concluded that an increased curve fitting horizon will lead to longer time to half values but in a less accurate representation of peak voltages.

Besides this, for the determination of relevant impulse characteristics of over-voltages in MMC–HVDC links, suitable

Table 7 Transmission technology comparison matrix using enumerator in column and denominator in row for reduced curve fitting horizon $t_{\mathrm{flt}} \leq t \leq t_{\mathrm{sim,red}}$

	q_{p}			
	O-150	C-150	C-100	C-50
O-150	1	30.81	22.10	13.55
C-150	0.03	1	0.72	0.44
C-100	0.05	1.39	1	0.61
C-50	0.07	2.27	1.63	1

	q_{50}			
	O-150	C-150	C-100	C-50
O-150	1	1.54	1.52	1.53
C-150	0.65	1	0.98	0.99
C-100	0.66	1.02	1	1.01
C-50	0.65	1.01	0.99	1

	$q_{\mathrm{A,eval}}$			
	O-150	C-150	C-100	C-50
O-150	1	0.99	0.99	0.99
C-150	1.01	1	1	0.99
C-100	1.01	1	1	1
C-50	1.02	1.01	1	1

	$q_{\mathrm{A},\infty}$			
	O-150	C-150	C-100	C-50
O-150	1	1.37	1.35	1.36
C-150	0.73	1	0.99	0.99
C-100	0.74	1.01	1	1.01
C-50	0.73	1.01	0.99	1

evaluation windows, and curve fitting horizons are required. As already mentioned in Section 5.1, it is considered more reasonable assuming suitable post fault measures leading to reduced overvoltage durations and related curve fitting horizons.

With the intention of analysing and imitating over-voltages during DC pole to ground faults, SDEI impulses are capable of representing the voltage time area. However, for an accurate representation of peak insulation stresses the peak voltage approximation (parameter $q_{\mathrm{Fit,max}}$ in Table 6) demands for additional safety margins. This especially gains importance if SDEI impulses are considered as a test voltage waveform, or are used in future investigations related to associated dielectric effects.

5.3 Quantification of transmission technology influences

Based on derived voltage time approximations it is now possible to address aspects caused by different transmission technologies. Therefore, parameters introduced in Section 4.4 are used in conjunction with overvoltage approximations based on SDEI. In this case, t_{p}, t_{50}, $u_{i,\mathrm{e}}$ and $u_{i,\mathrm{d}}$ used in (4)–(6) refer to the superimposed impulse voltages, which are applied to constant DC voltage $U_{\mathrm{DC}}(t_{\mathrm{flt}})$. For determination of $q_{\mathrm{A,eval}}$ based on (7), impulse data $u_{i,\mathrm{e}}$ and $u_{i,\mathrm{d}}$ are set as $u_i = u_{\mathrm{SDEI}}(t) + U_{\mathrm{DC}}(t_{\mathrm{flt}})$. The overall transmission technology comparison matrix, focussing on the reduced curve fitting horizon and SDEI approximation, is shown in Table 7. Additionally, Fig. 6 summarises SDEI voltages for all four scenarios.

It is found that voltage time areas for $t_{\mathrm{flt}} \leq t \leq t_{\mathrm{eval}}$ are nearly unaffected by chosen transmission technology as parameter $q_{\mathrm{A,eval}} \simeq 1$. If overall voltage time area is taken into account,

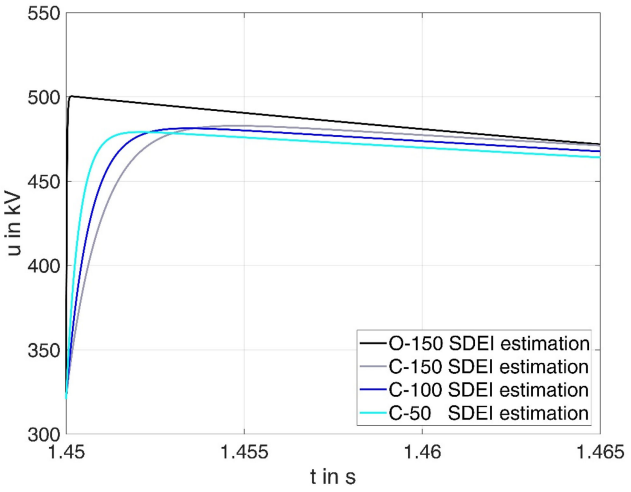

Fig. 6 *Enlarged overview of all SDEI approximations with respect to chosen transmission technology using a reduced curve fitting horizon* $t_{flt} \leq t \leq t_{sim,red}$

voltage time areas are less affected by cable length but by transmission technology. Parameter $q_{\mathrm{A},\infty}$ indicates that voltage stresses associated with voltage time areas are reduced in the case of OHL to ∼73–74% compared with cable transmission. Similar observations are enabled focusing on time to half. The parameter q_{50} is nearly independent of cable length but tremendously affected by transmission technology. Time to half is in the case of a 150 km cable 1.54 times larger than for a 150 km long OHL. Peak voltages $\left(\hat{U}_{\mathrm{DC+I}}\right)$, see Table 5 (values in bold), are found within the same range with the highest values occurring for OHL systems. This value is 4.4% larger than for the shortest cable transmission (50 km). Considering only peak voltages $\left(\hat{U}_{\mathrm{I}}\right)$ of the superimposed impulses, this effect is slightly more severe as values occurring for OHL systems are 11.1% larger. In the case of time to peak, indicator q_{p} allows the identification of cable length and transmission technology influences. OHL has the shortest t_{p} which is compared with a C-150 ∼31 times larger. Besides this, a reduced cable length is always accompanied by a reduced time to peak.

Indicative values for extended curve fitting horizon and SDEI can be found in [10] and for the sake of closed-form representation in Table 8. Deviations are mainly due to the chosen SDR method, which combines both power flow configurations.

5.4 Summary of results

Based on yet presented results, several key aspects are found.

- Double exponential voltages are found suitable to imitate occurring over-voltages in MMC——HVDC schemes.
  - ○ Even if curve fitting techniques are used in order to obtain the peak value of SIs, the overall voltage approximation remains poor with respect to voltage time area and peak voltage reproduction.
  - ○ Impulse voltage approximation capability increases significantly for DEI voltages if besides voltage U_{A} the parameters α_1 and α_2 are as well determined using curve fitting techniques.
  - ○ Superior results based on voltage time area reproduction are obtained if a double exponential voltage superimposed on a constant DC offset is considered.
- Overall voltage approximation is affected by the selected curve fitting horizon, which is closely linked to potential post fault measures within the system. It is considered more reasonable to focus on obtained curve parameters utilising a reduced curve fitting horizon, which is related to overvoltage reduction measures. In the presented cases, feasible AC circuit breaker opening delays prior to related DC de-energisation measures

Table 8 Transmission technology comparison matrix using enumerator in column and denominator in row for reduced curve fitting horizon $t_{\mathrm{flt}} \leq t \leq t_{\mathrm{sim,max}}$

	q_{p}			
	O-150	C-150	C-100	C-50
O-150	1	41.25	29.46	18.21
C-150	0.02	1	0.71	0.44
C-100	0.03	1.4	1	0.62
C-50	0.05	2.26	1.62	1

	q_{50}			
	O-150	C-150	C-100	C-50
O-150	1	12.12	11.09	10.99
C-150	0.08	1	0.92	0.91
C-100	0.09	1.09	1	0.99
C-50	0.09	1.10	1.01	1

	$q_{\mathrm{A,eval}}$			
	O-150	C-150	C-100	C-50
O-150	1	0.95	0.95	0.95
C-150	1.05	1	1	1
C-100	1.05	1	1	1
C-50	1.05	1	1	1

	$q_{\mathrm{A},\infty}$			
	O-150	C-150	C-100	C-50
O-150	1	9.68	8.84	8.71
C-150	0.1	1	0.91	0.90
C-100	0.11	1.09	1	0.99
C-50	0.11	1.11	1.01	1

yield to the reduced curve fitting horizon of $t_{\mathrm{sim,red}} = t_{\mathrm{flt}} + 40$ ms, corresponding to two AC grid cycles.

- Presented methods for curve fitting approximation and their evaluation (see Sections 4.2 and 4.3) are generally applicable.
- Influences related to additional delays, e.g. due to fault detection or breaker restrikes, are shown in Section 5.1.

- Using SDEI approximation allows the identification of effects caused by different transmission technologies:
  - Time to peak is the fastest for OHL transmission and in the case of cable transmission 13.55–30.81 times larger. Time to peak significantly increases with increasing cable length.
  - Time to half is the shortest for OHL transmission technology and in the case of cable transmission larger, whereas time to half is less affected by cable length but by chosen curve fitting horizon.
  - Voltage time areas are roughly similar if evaluation time is limited to $t_{\mathrm{eval}} = t_{\mathrm{flt}} + 40$ ms. Overall voltage time areas are the smallest for OHL transmission and roughly 1.3 times larger for cable systems if the reduced curve fitting horizon is considered.

6 Laboratory test voltage generation

Under consideration of presented results in Section 5, it is considered most promising to use superimposed impulses for a synthetical approximation of simulated over-voltages within a high voltage laboratory. This entitles an evaluation of the influences on discharge and material behaviour and their related causes on the dielectric strength in the case of non-standard impulses. To discuss related influences and challenges for the design of test circuits indicative considerations based on single-stage equivalent circuits are derived. A description of considered design rules will be given in Section 6.1. In the subsequent section, aspects related to the realisation of superimposed test setups are presented and associated consequences are discussed. A comparison between voltage approximations derived in Section 5 and those voltage time curves obtained using circuit simulation is presented in Section 6.3.

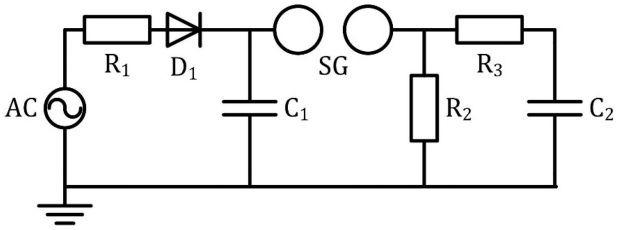

Fig. 7 *Single-stage equivalent circuit for impulse test voltage generation*

6.1 Consideration and design rules for single-stage equivalent circuits

Focusing on impulse voltage generation, circuit parameters as shown in Fig. 7, may be obtained following [19, 21] leading to simplified (8)–(11). If Marx generators are used, their related single-stage equivalent circuit needs to be determined in the first place

$$R_2 = \frac{1}{2(C_1 + C_2)}\left[\left(\frac{1}{\alpha_1} + \frac{1}{\alpha_2}\right) + \sqrt{\left(\frac{1}{\alpha_1} + \frac{1}{\alpha_2}\right)^2 - \frac{4(C_1 + C_2)}{\alpha_1 \alpha_2 C_1}}\right], \tag{8}$$

$$R_3 = \frac{1}{2C_2}\left[\left(\frac{1}{\alpha_1} + \frac{1}{\alpha_2}\right) - \sqrt{\left(\frac{1}{\alpha_1} + \frac{1}{\alpha_2}\right)^2 - \frac{4(C_1 + C_2)}{\alpha_1 \alpha_2 C_1}}\right], \tag{9}$$

$$\eta = \frac{U_{\mathrm{out}}}{U_{\mathrm{DC}}} \simeq \frac{C_1}{C_1 + C_2}. \tag{10}$$

It is found that parameters α_1 and α_2 identified during voltage approximation are vital for solving the equations above and are therefore presented in Section 6.2.1. Besides this, values for C_1 and C_2 are required. More accurate efficiency calculation is achieved, if instead of (10)

$$\eta^* = \frac{U_{\mathrm{out}}}{U_{\mathrm{DC}}} = \frac{C_1}{C_1 + C_2} \cdot \mathrm{e}^{-\alpha_1 \cdot t_p} \tag{11}$$

is used.

Test circuit design is usually carried out under various limitations, such as available laboratory equipment, space considerations and relevant electrical parameters of the device under test (DUT). Due to this, circuit design will be discussed within this contribution in a more general manner. For a realistic circuit parameter estimation, a capacitance of 750 nF with a maximum voltage of 100 kV per stage of Marx-generator is assumed. Besides this, the degree of simplified efficiency following (10) is set to a minimum of $\eta = 85\%$.

6.2 Superposition of an impulse voltage on a DC voltage

This section describes the necessities for impulse voltage generation. It is followed by additional considerations which need to be taken into account for superimposed tests.

6.2.1 Impulse voltage generation: The highest amplitude of superimposed voltage approximation is in combination with the claimed degree of simplified efficiency demanding for at least three stages of a Marx generator. This is resulting in a maximum capacitance of $C_1 = 250$ nF and leads to $C_2 = 44.2$ nF. Table 9 lists the overall curve parameters and their related circuit parameters. To guarantee the validity of the equations above, the assumption $R_1 \gg R_2 \gg R_3$ is used. Large values for R_1 are required

Table 9 Voltage waveform data (see Table 5), related exponents and calculated circuit parameters following (8) and (9)

	SDEI								
	Curve fitting horizon $t_{flt} \leq t \leq t_{sim,red}$								
	t_p in µs	t_{50} in ms	α_1 in 1/s	α_2 in 1/s	$\hat{U}_{DC+I}$ in kV	$U_{DC}(t_{flt})$ in kV	$\hat{U}_I$ in kV	R_2 in kΩ	R_3 in kΩ
O-150	155	58.4	11.9	53891.5	500.3	324.5	175.8	285.6232	0.4941
C-150	4775	90.1	8.2	1014.3	482.8	322.5	160.3	413.9199	26.2870
C-100	3425	88.5	8.2	1531.2	481.4	321.7	159.7	414.1231	17.4045
C-50	2100	89.3	8	2791.6	479.2	320.8	158.3	424.6650	9.5422

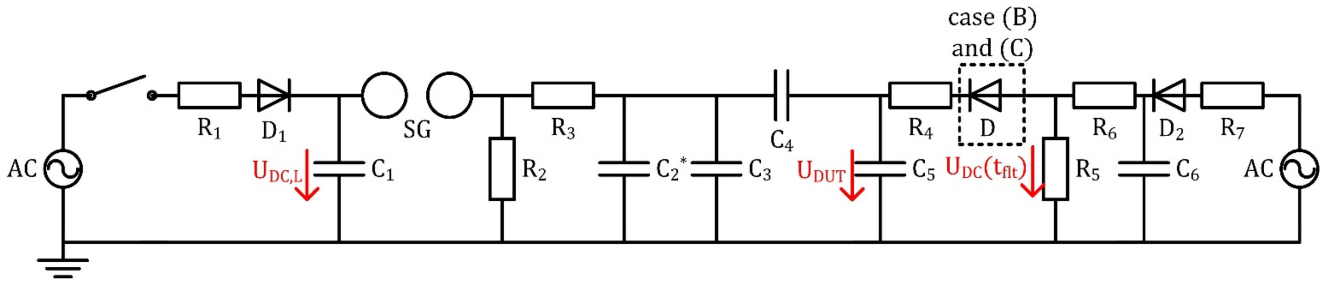

Fig. 8 *Overview of overall circuit for synthetic overvoltage imitation*

Table 10 Efficiencies and voltage set points for generation of superimposed impulses

		O-150	C-150	C-100	C-50
SDEI	η^* in % (according to (11))	84.8	81.7	82.6	83.6
	$U_{DC,L} = \frac{\hat{U}_I}{\eta^* \cdot \eta_{VD}}$ in kV	243.8	230.8	227.3	222.8

in order to minimise any further charge process of C_1 and C_2 during the tail of the impulse. Instead of using large values for R_1, it may also be technically considered switching off the AC supply which feeds the diode rectifier prior impulse triggering as depicted in Fig. 8.

6.2.2 Superposition of impulse voltage on DC voltage: To separate DC voltage generation from impulse voltage generation and vice versa, additional components such as blocking capacitors and protection resistors are required. Those components and additional measuring devices need to be considered in circuit design as well. An overview of the overall circuit for synthetic overvoltage imitation is provided in Fig. 8.

Following [22], values are set for the blocking capacitor $C_4 = 1000$ pF and for impulse measuring using a capacitive voltage divider $C_3 = 500$ pF. These additional components affect the circuit behaviour. Especially the blocking capacitor in combination with the DUT will act as a capacitive voltage divider limiting the maximum peak voltage. Assuming that this voltage divider reduces the single-stage circuit efficiency by another $\eta_{VD} = 85\%$, this is limiting maximum capacitance of the DUT to $C_5 = 176$ pF. To keep the efficiency of the Marx generator and its calculated parameters, as shown in Table 9, the value for C_2 needs to be corrected to C_2^* following:

$$C_2^* = C_2 - C_3 - \frac{C_4 \cdot C_5}{(C_4 + C_5)} = 43.6\,\text{nF}. \tag{12}$$

Overall efficiency for the peak amplitude at the DUT may, in this case, be approximated using $\eta_{ges} = \eta \cdot \eta_{VD} = 72.3\%$. To obtain more accurate values for efficiency and consequently for the relevant impulse capacitor loading voltage $U_{DC,L}$ calculation follows (11) and takes the efficiency of the additional capacitive voltage divider into account as shown in Table 10.

To obtain circuit parameters for a simulation of the DC voltage generation, similar assumptions as chosen for the Marx circuit are used, leading to $C_6 = 187.5$ nF.

Based on [22], for measuring and protection devices values of $R_4 = 2.5$ MΩ, $R_5 = 1100$ MΩ and $R_6 = 500$ kΩ may be chosen. If these parameters are considered for the depicted circuit design retroactive effects on DC generation cannot be excluded. In this case, the resulting impulse voltage at the DUT will be heavily affected due to the resistive voltage divider is given by R_4 and R_5. Bearing information from Table 9 in mind, the ratio $(U_{DC}(t_{flt})/\hat{U}_I) \simeq 1.85, \ldots, 2.02$ is found. Therefore, the same ratio has to be chosen for R_5/R_4, resulting in a realisation using values of $R_5 = 1100$ MΩ and $R_4 = 550$ MΩ. If instead $R_4 = 2.5$ MΩ and $R_5 = 5$ MΩ are chosen, an impact on time to half values will be observed, as an additional and non-negligible discharge path for C_5 has to be considered. Instead of taking the ratio of the resistive voltage divider into account, whilst avoiding a further de-energisation of C_5, a diode stack behind R_4 provides a remedy. In this case, for a technical realisation, the impulse strength and parasitic capacitances of the used diodes need to be considered. Besides this, retroactive effects have always been considered in order to avoid any damage to the used DC generator.

6.3 Results of circuit simulation and discussion

Within this subsection results based on circuit simulation for a laboratory impulse generation of SDEI voltages are presented. This is followed by a discussion of the results and capabilities of the presented circuit.

6.3.1 Results: For all simulations, the following parameters are used: $C_1 = 250$ nF, $C_2^* = 43.6$ nF, $C_3 = 500$ pF, $C_4 = 1000$ pF, $C_5 = 176$ pF, $C_6 = 187.5$ nF, $R_1 = 1$ MΩ, $R_6 = 500$ kΩ, $R_7 = 1$ MΩ. Besides this, all circuit components are considered as ideal including spark gaps (SGs). Overall three different realisations are discussed for scenarios O-150 and C-150. The first realisation (A) considers the use of a resistive voltage divider $R_4 = 550$ MΩ and $R_5 = 1100$ MΩ. For the second realisation (B), the same values are chosen for R_4 and R_5 but an additional diode after R_4 is used. The third implementation (C) follows [22] with $R_4 = 2.5$ MΩ and $R_5 = 1100$ MΩ, but is also extended with an additional Diode after R_4. For O-150 simulations, impulse forming resistance values are set to $R_2 = 285.6232$ kΩ and $R_3 = 0.4941$ kΩ, whereas impulse capacitor loading voltage is set to $U_{DC,L} = 243.90$ kV and a

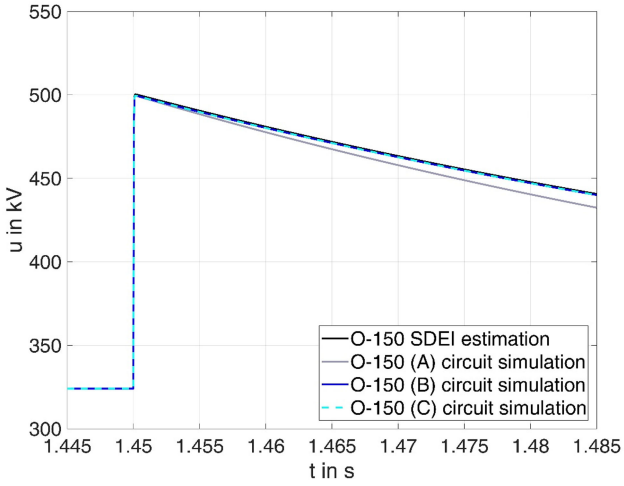

Fig. 9 *Results of circuit simulation for SDEI estimation of O-150 using three different circuit realisations as mentioned in Section 6.3.1*

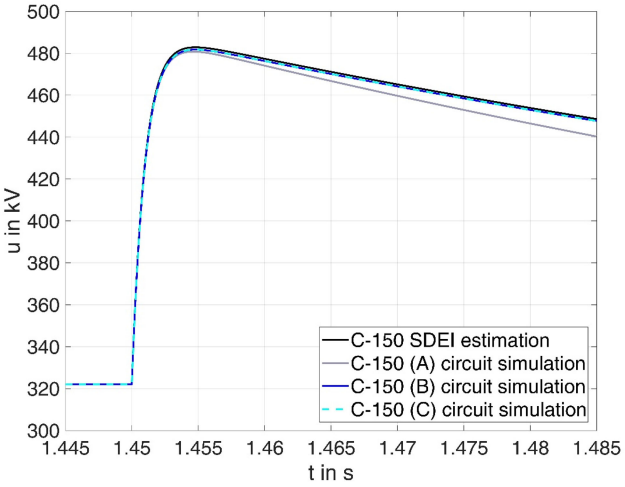

Fig. 10 *Results of circuit simulation for SDEI estimation of C-150 using three different circuit realisations as mentioned in Section 6.3.1*

Table 11 Determined results of impulse characteristics using circuit simulation and realisation concept (B)

	$t_{p-(B)}$, μs	$\Delta_{t_{p-(B)}}$, %	$t_{50-(B)}$, ms	$\Delta_{t_{50-(B)}}$, %	$\hat{U}_{(B)}$, kV	$\Delta_{\hat{U}-(B)}$, %
O-150	155.5	0.3	58.4	0	175.5	−0.2
C-150	4782.6	0.2	90.2	0.1	159.7	−0.4

constant DC voltage of $U_{DC}(t_{flt}) = 324.5\,\text{kV}$ is used. Results are shown in Fig. 9.

For C-150 simulations, the same scenarios as mentioned for O-150 are considered but slightly different values are used $R_2 = 413.9199\,\text{k}\Omega$, $R_3 = 26.2870\,\text{kV}$, $U_{DC,L} = 230.83\,\text{kV}$ and $U_{DC}(t_{flt}) = 322.5\,\text{kV}$. Obtained results are depicted in Fig. 10.

6.3.2 Discussion and further opportunities for the presented circuit: It is noteworthy that overall design considerations and aspects presented in Sections 6.2.1 and 6.2.2 lead to a good realisation of voltage waveforms accompanied by the derived novel impulse parameters. Associated nominal times to peak are ranging from $155\,\mu\text{s} \leq t_p \leq 4775\,\mu\text{s}$ and time to half values from $58.4\,\text{ms} \leq t_{50} \leq 90.1\,\text{ms}$. Superior results are obtained, if R_4 is followed by a diode stack as considered for realisation (B). Table 11 presents the results and related errors for each parameter.

Similar results are found for implementation (C), resulting for O-150 in $\Delta_{t_{p-(C)}} \simeq 0.6\%$, $\Delta_{t_{50-(C)}} \simeq 0\%$, $\Delta_{\hat{U}-(C)} \simeq -0.1\%$ and for C-150 in $\Delta_{t_{p-(C)}} \simeq 0.4\%$, $\Delta_{t_{50-(C)}} \simeq 0.2\%$, $\Delta_{\hat{U}-(C)} \simeq -0.4\%$. If realisation (A) is considered associated errors are higher, especially considering the time to half values, leading for O-150 approximation to $\Delta_{t_{p-(A)}} \simeq -1.1\%$, $\Delta_{t_{50-(A)}} \simeq -15.1\%$, $\Delta_{\hat{U}-(A)} \simeq -0.2\%$ and for C-150 approximation to $\Delta_{t_{p-(A)}} \simeq -3.2\%$, $\Delta_{t_{50-(A)}} \simeq -19.7\%$, $\Delta_{\hat{U}-(A)} \simeq -1\%$.

As a consequence of the associated errors related to realisation (C), it is found that the use of the diode stack is beneficial in order to keep the shape of impulses as close as possible to the desired voltage waveform. If the use of this additional diode is not applicable, a different supportive measure may be provided by the impulse generator. In Section 6.2.1, a further charge process of C_1 and C_2 was stated avoidable in order to stop an enlargement of the wave tail. This identified causality provides valuable benefits. A further charge process may act as a supportive measure to enlarge the wave tail, especially if the de-energisation caused by R_4, R_5 (Section 6.2.2) or additional parallel resistances of used capacitors or currents due to surface contaminations are taken into account.

Furthermore, the use of switching concepts besides commonly used air filled SGs may be broached in order to ensure the desired trigger operation. If commonly used air filled SGs cannot guarantee reliable operation without a self-extinguishing arc, compact pressure controlled gas insulated SGs may provide a remedy. Besides this, circuits based on semiconductors, as recently presented in [23], seem promising in the future. Those may provide additional benefits if electrode erosion or trigger problems are taken into account.

7 Conclusion & outlook

After a brief conclusion, an outlook motivating further research aspects is presented in the following.

7.1 Conclusion

Transient overvoltage stresses in MMC–HVDC links have been simulated and investigated for DC pole to ground faults. As slow front transients do occur, a feasible non-linear surge arrestor *V–I*-curve needs to be selected. Furthermore, varying fault resistances (between 1 mΩ and 30 Ω), different load flow scenarios and appropriate post-fault system behaviour influences – caused by the system protection setting – are considered. To determine as well changes occurring in over-voltages associated with different transmission technologies, simulations are carried out for OHL and cable schemes.

The analysis of obtained simulation results shows that normative test voltage waveforms such as SIs only allow a poor approximation of the occurring over-voltages. As occurring voltage shapes differ significantly from any normative SI, further analysis of the impulse shapes is carried out. It is concluded that double exponential voltages provide benefits for analysis and imitation of occurring over-voltages in MMC–HVDC schemes. Superior results are obtained if a double exponential voltage superimposed on a constant DC offset is considered. The use of curve fitting techniques allows the identification of several valuable overvoltage parameters. Time to peak significantly increases with increasing cable length and is the fastest for OHL transmission, whereas time to half is the shortest for OHL transmission technology and in the case of cable transmission larger. Peak voltages are found around the same range independent of the chosen transmission technology.

To propose a laboratory imitation of those impulses, circuit design based on single stage impulse equivalent circuits is presented and related aspects for superimposed testing are derived and described. Those synthetically generated voltages may, later on, provide the basis for follow-up investigations on related dielectric effects caused by those non-normative over-voltages.

7.2 Outlook

The field of transient voltage stresses in MMC–HVDC systems is a vital area for high-voltage research. While solely monopolar configurations have been investigated within this initial study, on-going considerations related to bipolar topologies and their different characteristics seem essential. Additionally, refinements regarding modelling accuracy related to superposed high frequent occurrences meanwhile or subsequent to converter blocking are desirable.

Concentrating on test voltage application, the use of Marx generators or their related single stage equivalent circuits is one option, especially if in the first instance consequences for air insulation as mentioned in Section 4.2 and [10, 11, 24] are addressed. The presented concept may result in application challenges if the derived novel waveforms are applied on DUT with an increased capacitance. In this case, charging the DUT to peak voltage and utilising a defined ohmic path for a slow discharge process is considered beneficial for the generation of the relevant time to half values. The regard of a negative impulse superimposed on this positive decaying voltage may provide the relevant dynamics. Besides this, achieving time to half values whilst using a controllable DC supply or more general an appropriate voltage converter with sufficient output current is seen promising. For this purpose, utilising high-voltage transformers, as presented for SI generation in [25] may provide benefits for a future generation of presented novel impulse shapes.

Moreover, the consideration of parasitic influences, as presented in [26] during circuit simulation prior to laboratory implementation is seen valuable. Future experiments are considered precious in order to evaluate the effects caused by those non-standard impulses on HVDC insulation. As accessible research data of air discharge mechanisms for impulses under consideration of DC pre-stress are only available for SI, those investigations are of high importance besides investigations on cables and their accessories. Furthermore, if analogies to already existing normative test voltages can be concluded, a more transparent way for distance estimation during the design stage of a converter, as mentioned in [10, 11, 24] will be enabled.

References

[1] Lesnicar, A., Marquardt, R.: 'An innovative modular multilevel converter topology suitable for a wide power range'. Proc. IEEE Power Tech Conf., Bologna, Italy, June 2003, pp. 1–6

[2] IEC 60071-1 (2011–03): Insulation co-ordination – part 1: definitions, principles and rules

[3] IEC 60071-2 (1996–12): Insulation co-ordination – part 2: application guide

[4] IEC 60071-5 (2014–10): Insulation co-ordination – part 5: procedures for high-voltage direct current (HVDC) converter stations

[5] Badrkhani Ajaei, F., Iravani, R.: 'Cable surge arrester operation due to transient overvoltages under DC-side faults in the MMC–HVDC link', *IEEE Trans. Power Del.*, 2016, **31**, (3), pp. 1213–1222

[6] Dennetiere, S., Saad, H., Naud, A., *et al.*: 'Transients on DC cables connected to VSC converters'. 9th Int. Conf. on Insulated Power Cables (JICABLE), Versailles, France, June 2015

[7] Salimi, M., Woodford, D.: 'Overvoltage assessment for insultation coodrination of HVDC overhead lines with MMC-VSC technology'. CIGRE Winnipeg Colloquium 2017, Winnipeg, Canada, September 2017

[8] Greve, M., Koochack Zadeh, M., Rendel, T., *et al.*: 'Behaviour of the HVDC links with MMC technology during DC cable faults'. CIGRE Winnipeg Colloquium 2017, Winnipeg, Canada, September 2017

[9] Saltzer, M., Nguyen-Tuan, M., Crippa, A., *et al.*: 'Surge and extended overvoltage testing of HVDC cable systems'. 10th. Int. Symp. on HVDC Cable Systems JICABLE-HVDC'17, Dunkirk, France, November 2017

[10] Wenig, S., Freye, C., Goertz, M., *et al.*: 'Transient voltage stresses in MMC-HVDC links and associated impacts on air clearance calculation'. 20th Int. Symp. on High Voltage Engineering, Buenos Aires, Argentina, August 2017

[11] Freye, C., Lühring, U., Jenau, F.: 'Air clearance calculation under consideration of atmospheric, statistic and geometric influences for HVDC converter stations based on normative procedures'. 19th Int. Symp. on High Voltage Engineering, Pilsen, Czech Republic, August 2015

[12] CIGRE Study Committee B4: 'Proposal for the creation of a new working group: application guide for the insulation coordination of voltage source converter HVDC (VSC HVDC) stations', February 2015

[13] Wachal, R., Jindal, A., Dennetière, S., *et al.*: 'Guide for the development of models for HVDC converters in a HVDC grid'. Tech. Rep., Cigré TB604 (WG B4.57), Paris, December 2014

[14] Gnanarathna, U.N., Gole, A.M., Jayasinghe, R.P.: 'Efficient modeling of modular multilevel HVDC converters (MMC) on electromagnetic transient simulation programs', *IEEE Trans. Power Deliv.*, 2011, **26**, (1), pp. 316–324

[15] Beddard, A., Barnes, M., Preece, R.: 'Comparison of detailed modelling techniques for MMC employed on VSC-HVDC schemes', *IEEE Trans. Power Deliv.*, 2015, **30**, (2), pp. 579–589

[16] Saad, H., Dennetière, S., Mahseredjian, J., *et al.*: 'Modular multilevel converter models for electromagnetic transients', *IEEE Trans. Power Deliv.*, 2014, **29**, (3), pp. 1481–1489

[17] CIGRE Technical Brochure 72: 'Guidelines for the evaluation of the dielectric strength of external insulation', 1992

[18] Cortina, R., Marrone, G., Pigini, A., *et al.*: 'Study of the dielectric strength of external insulation of HVDC systems and application to design and testing'. Cigre 1984, Int. Conf. on Large High Voltage Electric Systems, Paris, France, 29th August - 6th September

[19] Beyer, M., Boeck, W., Möller, K., *et al.*: '*Hochspannungstechnik*' (Springer Verlag, Berlin, Heidelberg, 1992)

[20] CIGRE TB 496: 'Recommendations for testing DC extruded cable systems for power transmission at a rated voltage up to 500 kV', April 2012, Working Group B 1.32

[21] Kuffel, E., Zaengl, W.S., Kuffel, J.: '*High voltage engineering – fundamentals*' (Newnes, Oxford/Auckland/Boston/Johannesburg/ Melbourne/New Delhi, 2000, 2nd edn)

[22] Knudsen, N., Iliceto, F.: 'Flashover tests on large air gaps with DC voltage and with swichting surges superiposed on DC voltage', *IEEE Trans. Power Apparatus Syst.*, 1970, **PAS-89**, (5/6), pp. 781–788

[23] Sack, M., Herzog, D., Ruf, J., *et al.*: 'Semiconductor-based marx circuit for soft-switching operation'. 20th Int. Symp. on High Voltage Engineering, Buenos Aires, Argentina, August 2017

[24] Freye, C., Niedik, C.F., Jenau, F.: 'Numerical air clearance calculation method for HVDC converter stations: atmospheric, statistic and geometric input parameter variation study'. IEEE Int. Energy Conf. Energycon 2016, Leuven, Belgium, April 2016

[25] Wehinger, H.: '*Ausgleichsvorgänge in prüftransformatoren bei der erzeugung von schaltstossspannungen*'. PhD thesis, Technische Universität Carolo-Wilhelmia zu Braunschweig, 1976

[26] Karmokar, T., Jeroense, M., Abbasi, A.: 'Assessing the impacts of VSC converter configurations on performance and testing of up to 640 kV extruded cable systems'. JICABLE-HVDC'17, Dunkirk, France, November 2017