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Graphene Field-Effect Transistors Employing Different Thin Oxide Films: A Comparative Study

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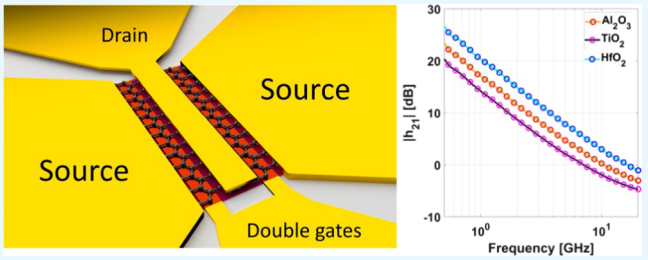
ABSTRACT: In this work, we report on a comparison among graphene field-effect transistors (GFETs) employing different dielectrics as gate layers to evaluate their microwave response. In particular, aluminum oxide (Al_2O_3), titanium oxide (TiO_2), and hafnium oxide (HfO_2) have been tested. GFETs have been fabricated on a single chip and a statistical analysis has been performed on a set of 24 devices for each type of oxide. Direct current and microwave measurements have been carried out on such GFETs and short circuit current gain and maximum available gain have been chosen as quality factors to evaluate their microwave performance. Our results show that all of the devices belonging to a specific group (i.e., with the same oxide) have a well-defined performance curve and that the choice of hafnium oxide represents the best trade-off in terms of dielectric properties. Graphene transistors employing HfO_2 as the dielectric layer, in fact, exhibit the best performance in terms of both the cutoff frequency and the maximum frequency of oscillation.



INTRODUCTION

The choice of the gate dielectric, as is well known, is crucial to develop highly competitive transistors,[1] especially for microwave applications. This aspect is particularly critical for graphene field-effect transistors (GFETs)[2,3] due to the intrinsic material incompatibility between pristine graphene and dielectric oxide layers.[2] Graphene surfaces are, in fact, chemically inert[3] to atomic layer deposition precursors and this peculiarity makes the integration of high-dielectric constant materials still an open issue.[2] Of course, intentional graphene lattice damage that could improve oxide layers adhesion is strongly undesirable.[4] In metal oxide semiconductor field effect transistor (MOSFET) technology, a thinner oxide, i.e., a higher oxide capacitance (C_{OX}), is desired to maximize the high-frequency performance of the device, since it leads to a higher value of transconductance and, consequently, cutoff frequency.[5] Unfortunately, a thin gate oxide has two main drawbacks: high leakage current due to tunneling phenomena and poor long-time reliability.[6] As shown by Benz et al.,[7] hexagonal boron nitride (h-BN) could operate as a superior gate dielectric. However, synthesis of large-area h-BN is in its infancy and deposition of high-quality material is not yet well established.[8] Another alternative dielectric could be mica, but it suffers from electrical hysteresis and hydrophilicity: this makes mica not a good candidate for FET gating.[9] As a possible solution, oxides with a high dielectric constant κ (i.e., high-κ oxide insulators) have been widely employed.[10] In this case, a good compromise between the κ-factor and the semiconductor/oxide band offset needs to be found, since high-κ oxides exhibit low band-offset values.[11] Traditionally, HfO_2 has been the most exploited oxide, thanks to its high dielectric constant ($\kappa \approx 25$). TiO_2 presents an even higher κ value ($\kappa \approx 80$), but it is thermally unstable when deposited over silicon.[12] On the other hand, Al_2O_3 exhibits a too low dielectric constant ($\kappa \approx 9$) but a very high breakdown voltage.[10,13] All of the above-mentioned oxides can potentially be used in the GFETs fabrication as gate oxide layers.

In this work, we report on the fabrication and electrical characterization (in both DC and microwave regimes) of back-gated GFETs employing Al_2O_3, TiO_2, and HfO_2 as insulating layers. Our work is aimed at evaluating the dependence of the high-frequency performance of such devices on the oxide material. Although in the literature different studies have been

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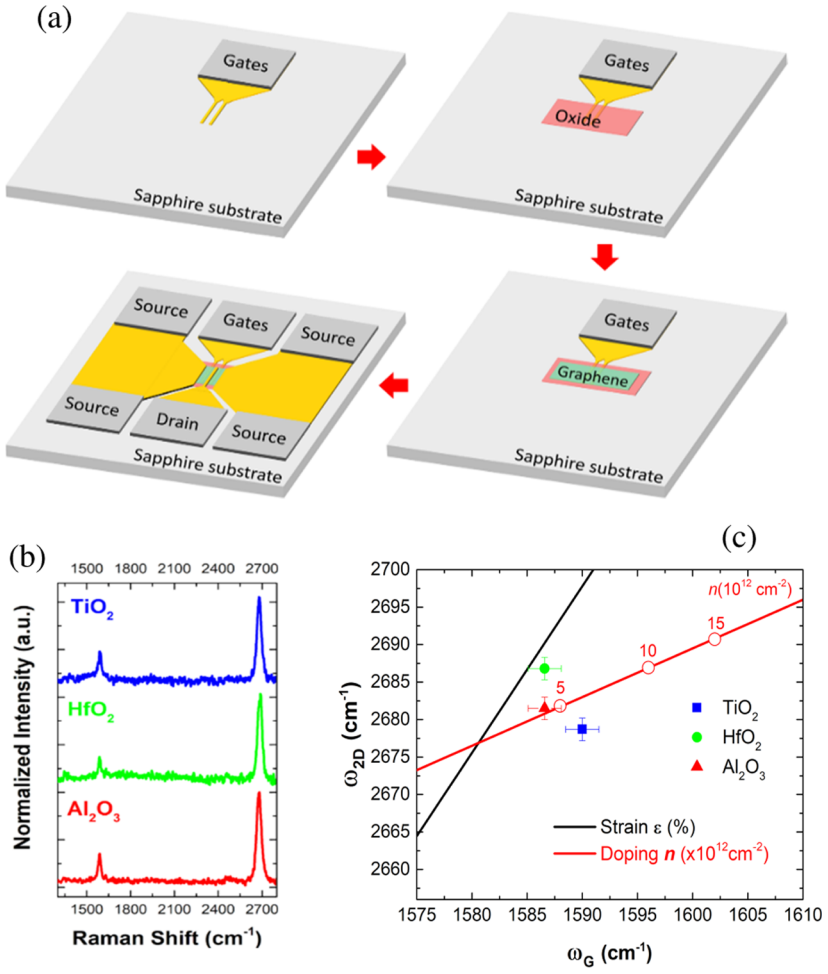

Figure 1. (a) Schematic representation of GFETs fabrication steps, (b) comparison among Raman spectra of transferred graphene on Al_2O_3, TiO_2, and HfO_2. (c) Strain-doping map of Raman G- and 2D-peak positions (ω_G, ω_{2D}, respectively) obtained from the samples with the three different oxides.

carried out on GFETs devices employing separately Al_2O_3, TiO_2, and HfO_2 (for example, we refer the reader to refs 14−16), none of them have performed a comparison of microwave performance of devices fabricated on the same chip. For this reason, our study can give a contribution in the field especially for manufacturers, confirming that the choice of hafnium oxide as the gate dielectric represents a promising solution to obtain the best compromise in terms of both contact resistance and field-effect mobility.

FABRICATION AND METHODS

The back-gated design allows our GFETs to be used for optical mixing, illuminating them via free-space radiation,[17] even if the underlying gate structure does not provide a flat surface for graphene deposition. Furthermore, top-gated graphene FETs typically require a seeding layer for high-quality dielectric deposition, which can lead to the deterioration of graphene quality.[4] Although not perfect for RF performance, back-gated geometry is still suitable for statistical investigation of oxide properties. Herein, we will refer to a "devices group" as a set of about 24 nominally identical devices fabricated on the same chip and employing the same gate oxide (i.e., Al_2O_3, TiO_2, or HfO_2). Three different groups of devices have been fabricated on sapphire substrate[18,19] and then their microwave performance has been studied in detail and compared. Figure 1a shows the GFETs fabrication steps.

First, the dual-finger back-gate has been patterned on a sapphire substrate by e-beam lithography followed by the evaporation of a thin Ti/Au bilayer (∼5/40 nm) and lift-off in acetone. Then, atomic layer deposition (ALD) has been used to deposit three different oxides. Particularly, a thickness of ∼11, 13, and 11 nm has been obtained for Al_2O_3, TiO_2, and HfO_2, respectively. Both Al_2O_3 and TiO_2 have been deposited at 100 °C, whereas 120 °C cycles have been employed for HfO_2 deposition. Then, a CVD-grown graphene film, previously grown on copper foil and laminated on oxidized silicon substrate, was transferred onto different oxides using wet transfer technique. One mol NaOH solution was used to etch a thin film of silicon dioxide, helping the delamination of graphene from the substrate and a poly(dimethylsiloxane) (PDMS) stamp was adopted to pick it up from the substrate and transfer onto the devices. After oxide deposition, graphene was patterned in a meandered structure by reactive ion etching to minimize contact resistance.[20] Subsequently, source/drain electrodes have been patterned onto a graphene sheet using E-beam lithography followed by a Ti/Au (∼5/100 nm) deposition and lift-off in acetone. All of the fabricated devices exhibit the same geometry. In particular, the gate−drain/source distance is 0.25 μm, the gate length is 0.5 μm, and gate width is 20 μm. Such values have been chosen after a parametrical study based on GFETs geometry.[21] We employed Raman spectroscopy to assess the high quality of the transferred monolayer graphene

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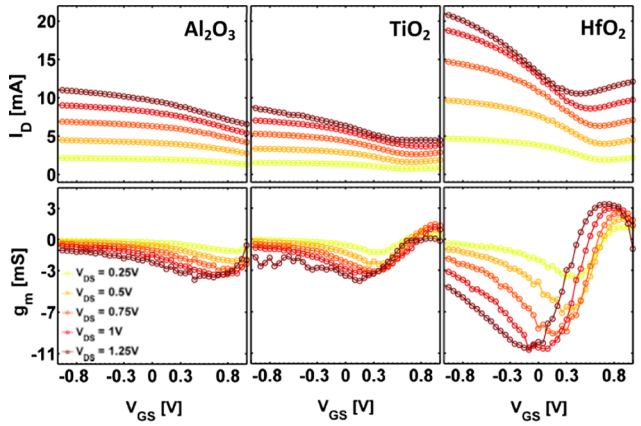

Figure 2. I_D and g_m vs V_{GS} curves as a function of V_{DS} for GFETs employing Al_2O_3, TiO_2, and HfO_2 as gate oxide.

Table 1. On/Off Ratio and Maximum Static Transconductance of the Best Devices for Each Oxide Group

device oxide	ON/OFF ratio	g_m [mS]
Al_2O_3	1.67	−3.86
TiO_2	1.93	−4.03
HfO_2	1.97	−10.66

onto all of the three oxides, as shown by the distinctive G (1580 cm^{-1}) and 2D (2680 cm^{-1}) peaks[22] reported in Figure 1b. The quality of the transferred graphene is benchmarked by evaluating the width of the 2D peak and the strain-doping figure of merit. The 2D width are 37, 38, and 40 cm^{-1} for the TiO_2, HfO_2, and Al_2O_3 substrates, respectively. Figure 1c shows the strain-doping figure of merit of graphene obtained by plotting the positions of G and 2D peaks for each oxide layer.[23] Graphene on Al_2O_3 is the least strained and has a carrier concentration of about 5×10^{12} cm^{-2}, whereas HfO_2 and TiO_2 show higher degree of strain, but HfO_2 is the least doped and TiO_2 has the highest carrier concentration (above 5×10^{12} cm^{-2}). From the Raman analysis, we expect that GFETs with HfO_2 as a dielectric layer show the highest mobility performance due to the lowest doping of graphene (about 2×10^{12} cm^{-2}), even if graphene suffers from tensile strain. However, devices fabricated using Al_2O_3 show a slightly higher level of doping concentration (about 5×10^{12} cm^{-2}) and negligible strain of graphene. The TiO_2-based devices suffer from concurrent effect of higher doping concentration (about 6×10^{12} cm^{-2}) and compressive strain of graphene.

RESULTS AND DISCUSSION

After fabrication, all of the samples were electrically characterized in ambient conditions. In particular, microwave and DC measurements were simultaneously performed for each GFET operating point, employing an automated bench, controlled via dedicated software to avoid the shift of the static curves due to the well-known hysteresis in graphene-based devices.[24−26]

DC measurements, performed in the ranges $V_{GS} = -1$ to 1 V and $V_{DS} = -1$ to 1 V, allowed us to obtain the static transconductance curves (I_D vs V_{GS}) and, hence, to evaluate the incremental low-frequency transconductance ($g_m = \partial I_D/\partial V_{GS}$ $|V_{DS}$=const), whose value deeply influences the performance of all of the devices. Figure 2 depicts the results of the measurements carried out on three samples, each one showing the best performance in terms of the ON/OFF ratio and maximum g_m, within each device group (we will refer to them as "best devices" in the following). All of the curves are parameterized in V_{DS}. Our transistors exhibit a p-type behavior as inferred from the position of the Dirac point.[27] As a consequence of the different gate oxides employed, each DC curves group shows a different broadening. This aspect is of great interest, since it leads to different ON/OFF ratios and static g_m values, as reported in Table 1.

Our measurements show that the use of HfO_2 as the oxide layer leads to an improvement in terms of static transconductance and a moderate increase of the ON/OFF ratio.

S-parameters have been measured using a N5232A Vector Network Analyzer and a Cascade Summit 9000 wafer-probe station in the frequency range [300 kHz to 20.003 GHz], biasing each GFET in its operating point where it exhibits the highest g_m value. All of the measurements have been performed in standard environment conditions. Starting from the S-parameters, short-circuit current gain ($|h_{21}|$) and maximum available gain (MAG) (and, consequently, f_T and f_{max}) have been calculated for each device and chosen as figures of merit for high-frequency analysis.[28] To extrapolate the intrinsic device gain values, we performed a de-embedding procedure through experimental measurements on auxiliary test structures implemented on the same chip.[29] The de-embedded $|h_{21}|$ and |MAG| curves are depicted in Figure 3.

The data refer to a statistical average of 24 identical GFETs for each device group. As depicted in Figure 3a, the $|h_{21}|$ curves

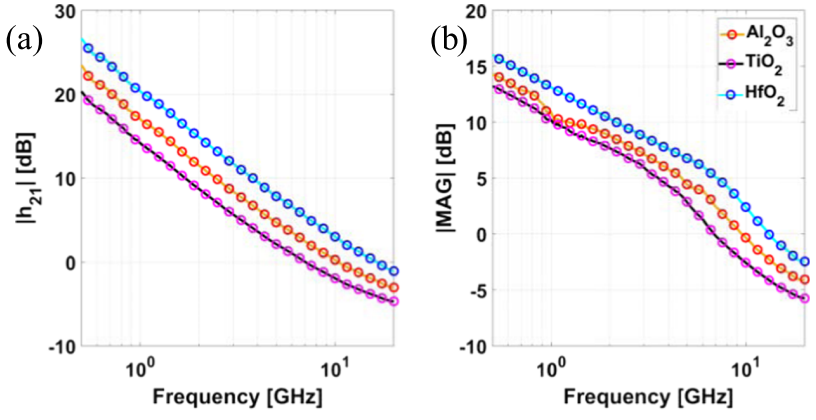

Figure 3. (a) $|h_{21}|$ and (b) |MAG| plots for GFETs employing Al_2O_3, TiO_2, and HfO_2 as gate oxide.

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trends are well defined and show a 20 dB/dec slope. As expected from the DC analysis, the devices with HfO_2 show the best performance in terms of maximum gains, with f_T = 16.46 GHz and f_{max} = 13.19 GHz. Instead, Al_2O_3 and TiO_2 devices exhibit lower f_T and f_{max} values, as reported in Table 2. Gain error bars at f_T and f_{max} ($\Delta|h_{21}|$ and $\Delta|MAG|$, respectively) are also listed.

Table 2. Cutoff Frequency, Maximum Frequency of Oscillation and Error Bars for Each Oxide Group

device oxide	f_T [GHz]	f_{max} [GHz]	$\Delta\|h_{21}\|$ [dB]	$\Delta\|MAG\|$ [dB]
Al_2O_3	10.56	9.72	±2.92	±1.00
TiO_2	7.15	6.96	±0.43	±1.20
HfO_2	16.46	13.19	±1.71	±1.07

Starting from the DC data reported in Figure 2, we used the model proposed by Kim et al.[30] to extract the average contact resistance and the field-effect mobility for the devices belonging to the three oxides groups. The results are depicted in Figure 4a,b, respectively.

Although showing the highest field-effect mobility ($\mu \sim 1700$ cm^2/(V s)), Al_2O_3-based devices exhibit the highest contact resistance ($R_c \sim 1240\ \Omega\ \mu$m). On the other hand, the lowest value of contact resistance has been measured in HfO_2-based transistors ($R_c \sim 480\ \Omega\ \mu$m) together with an intermediate value of mobility ($\mu \sim 1150$ cm^2/(V s)) among the three oxides. Conversely, TiO_2-based transistors show the lowest value of mobility ($\mu \sim 300$ cm^2/(V s)) together with an intermediate value of contact resistance ($R_c \sim 700\ \Omega\ \mu$m). As expected from Raman analysis, the TiO_2-based devices show the lowest mobility; meanwhile, Al_2O_3- and HfO_2-based GFETs have comparable mobilities. Clearly, since both low contact resistance and high field-effect mobility are in principle required, these data suggest that a trade-off needs to be found in the selection of the dielectric material.

To this purpose, a specific figure of merit ($\rho_{\mu R}$), defined as the ratio between the field-effect mobility and the contact resistance, can be introduced (Figure 4c). Then, by plotting the above-defined $\rho_{\mu R}$ as a function of the gate oxide, we can easily come to the conclusion that HfO_2, although having a lower κ-factor than TiO_2, allows the designer to get the best compromise in terms of contact resistance and field-effect mobility and, consequently, to obtain the best high-frequency performance.

These results can be explained considering the role of both the dielectric constants and the semiconductor/oxide band offset (Figure 5). A higher dielectric constant implies a lower semiconductor/oxide band offset, as in the case of TiO_2, if compared to Al_2O_3 and HfO_2. This brings a higher charge carriers transport through the potential barrier (Figure 5b), but worsens graphene channel modulation capability (Figure 2). For these reasons, we can conclude that, even in graphene-based transistors, the κ-factor is not the only parameter that designers can take into account to improve microwave performance. In fact, a compromise between the band offset and the κ-factor should be found and, among the three different investigated dielectrics, hafnium oxide represents the best choice in this sense.

CONCLUSIONS

In conclusion, in this work, we reported on a comparison among aluminum oxide, titanium oxide, and hafnium oxide

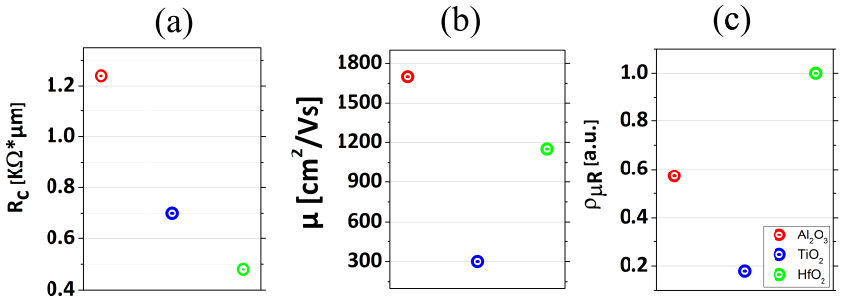

Figure 4. (a) Average contact resistance, (b) average field-effect mobility, and (c) ratio between the field-effect mobility and the contact resistance for Al_2O_3-, TiO_2-, and HfO_2-based devices.

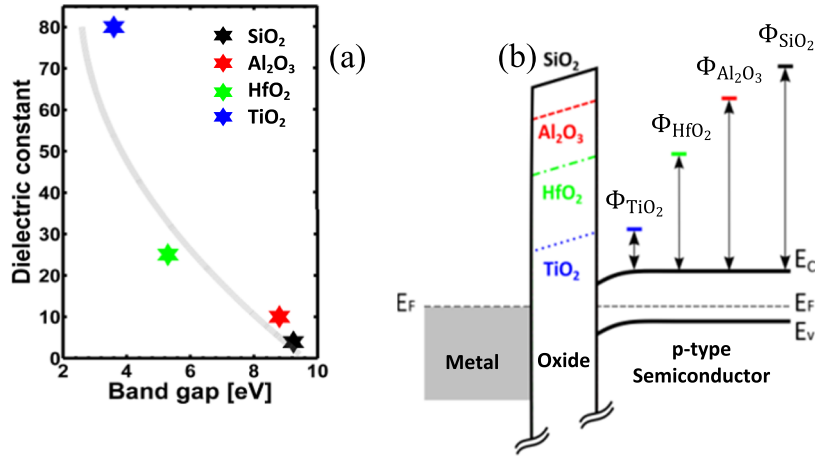

Figure 5. (a) Static dielectric constant vs band gap for Al_2O_3, TiO_2, and HfO_2, adapted from Robertson.[11] (b) Energy band diagram for a metal/oxide/p-type graphene structure.

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employed as gate dielectrics in graphene field-effect transistors. We fabricated 24 identical devices for each oxide insulator and evaluated their microwave response. We found that graphene transistors employing hafnium oxide show the best performance in terms of both cutoff frequency and maximum frequency of oscillation. This confirms that for graphene-based transistors, likewise for silicon MOSFETs,[21] the choice of hafnium oxide as the gate dielectric represents a promising solution, allowing to obtain the best compromise in terms of both contact resistance and field-effect mobility.

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Notes

The authors declare no competing financial interest.

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