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Grid-connected medium-voltage converters with parallel voltage-source active filters

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Abstract: Grid-connected medium-voltage converters are typically operated at switching frequencies of several hundred hertz per switch position, requiring bulky and expensive LCL filters in order to meet the harmonic limits given by the grid code. Commonly, semiconductor current derating and increased switching frequencies are used to reduce the LCL-filter costs, leading to a reduced utilisation and efficiency of the converter system. To overcome these disadvantages of conventional converter systems, the presented hybrid converter uses a parallel voltage-source active output filter and thus allows a significant reduction of the passive component demand. The harmonic performance is improved for the operation with small passive filter components, revealing the potential for increasing the utilisation and efficiency of high power medium-voltage converters. As a result, significant reductions of the filter losses and passive components as well as an increased output power are achieved compared to a reference LCL-filter-based converter system.

1 Introduction

Emerging applications such as solid-state transformers (SST) for grid couplings, medium-voltage-DC-transmission-systems (MVDC), flexible-AC-transmission-systems (FACTS) and medium-voltage electric drives use grid-connected medium-voltage converters. In [1], voltage source converters (VSC) for industrial medium-voltage applications are classified and compared. As a result of competitive costs, high robustness and low complexity, half of the commercially available converter solutions (e.g. by Abb, Siemens, Tmeic) in the lower medium-voltage range from 2.3 to 4.16 kV use the 3L-neutral point clamped (NPC) or the 3L-active neutral point clamped (ANPC) converter [2], respectively. In consequence of significant semiconductor losses resulting from high blocking voltages and load currents, the switching frequency of the 3L-NPC is typically limited to below 600 Hz per switch. Therefore, meeting the harmonic limits (e.g. given by the IEEE Standard 519 [3]) requires passive LCL filters composed of bulky inductors and capacitors. In order to limit the resulting LCL filter costs that often surpass the costs of the converter, the LCL-filter inductances and capacitances need to be reduced. Beyond improved modulation schemes such as optimised pulse patterns, e.g. investigated in [4] for medium-voltage drives, this can only be achieved by derating the semiconductor current and increasing the switching frequency, causing a reduced utilisation and efficiency of the converter system. Further important disadvantages of LCL-filter-based converter systems are substantial additional losses, reduced dynamic performance, frequency dependency and susceptibility to oscillation, requiring significant and lossy damping.

The objective of the combined use of multiple voltage source converters in a single converter system is to achieve a decoupling of the high- and low-power components. Conventional two- and three-level converters offer a superior relation between attainable output power and costs. However, the few voltage levels and the limited switching frequency as a result of significant switching losses lead to a low output power quality and require expensive and bulky passive output filters. In contrast, using an additional low power converter as a filter allows a significantly improved output power quality at competitive additional effort and costs. This basic principle of hybrid converters has been investigated and existing topologies can be found, e.g. in [5, 6]. In series hybrid converter topologies, the low power components carry the full load current at a reduced voltage load compared to the overall system. Series

hybrid converters are composed of a series connection of the high- and low-power converter and have been investigated in [7–12]. In comparison, parallel hybrid converter topologies use a parallel coupling of the high- and low-power converter. Therefore, the voltage load of the low power component corresponds to the full voltage rating, while the current load is reduced compared to the overall system. A single-phase parallel hybrid converter using a two-level high power converter and a low power linear amplifier is proposed in [13] in order to increase the output power. For applications with power ranges beyond the capability of linear amplifiers, the tandem inverter composed of a high power current source inverter (CSI) and a parallel connected low power two-level converter was introduced in [14, 15] and further investigated [16]. Compared to the use of a voltage source converter, the inherently higher and load-dependent harmonic distortion of the CSI output current leads to an increased power rating of the low power converter. Active power filters constitute a further implementation of parallel power converters [17]; however, they operate independently and therefore are not considered hybrid converters. A large number of active power filter topologies in combination with passive components have been investigated in previous works and are commonly called hybrid active power filters [18–21].

In [22], we introduced the combination of a high power main converter (MC) and a low power parallel voltage-source active filter (AF) for low voltage applications. Therein, the implementation of a coupled control scheme on a single control unit according to Fig. 1 allows the mitigation of the MC switching frequency current ripple and thereby the replacement of the passive LCL filter.

This contribution approaches the aforementioned disadvantages of conventional LCL-filter-based medium-voltage converter systems by using the previously introduced hybrid converter concept to design a hybrid medium-voltage multilevel converter. Considering the potential of silicon (Si) and silicon carbide (SiC) power semiconductors, the achievable impact of the hybrid topology on important characteristics such as passive component demand, efficiency, power density and utilisation of high power medium-voltage converters is investigated.

Fig. 2 shows the proposed hybrid medium-voltage multilevel converter. To achieve competitive costs, high robustness and high power density, a conventional 3L-NPC based on silicon insulated-gate bipolar transistors (Si-IGBTs) is used as MC. The topology used as AF is composed of cascaded full-bridge cells in star configuration and is referred to as a cascaded H-bridge active filter

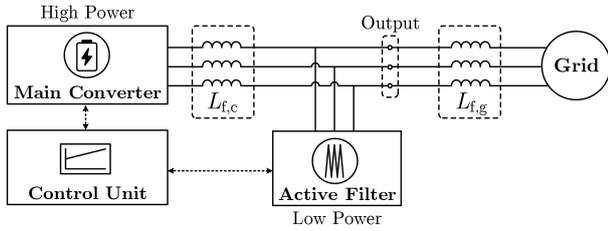


Fig. 1 Proposed hybrid converter topology combining a high power MC and a low power active output filter

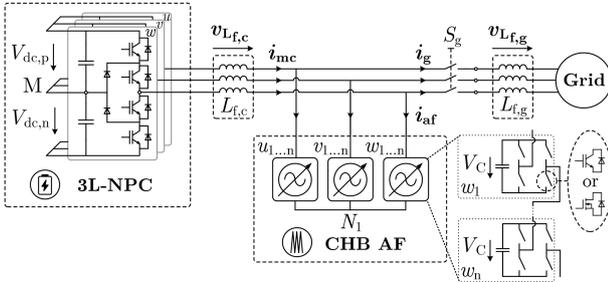


Fig. 2 Proposed hybrid medium-voltage multilevel converter composed of a 3L-NPC MC with CHB AF

Table 1 Parameters of the grid-connected medium-voltage converter systems

| | Parameter | Symbol | Value |
|-------------------------|-------------------------|------------------|------------|
| system p.u. base values | power | S_r | 5 MVA |
| | voltage | V_r | 3.3 kV |
| | current | I_r | 875 A |
| main converter | IGBT voltage rating | V_{CES} | 4.5 kV |
| | IGBT current rating | $I_{C,nom}$ | 1200 A |
| | DC-link voltage | V_{dc} | 5.3 kV |
| | switching frequency | $f_{sw,mc}$ | 750 Hz |
| active filter | IGBT voltage rating | V_{CES} | 1.2 kV |
| | DC-link voltage | V_C | 700 V |
| | number of cells per leg | n_{af} | 4 |
| | cell capacitance | C_{af} | 0.7 mF |
| transformer | short-circuit voltage | v_k | 6 % |
| grid at PCC | voltage | V_{PCC} | 3.3 kV |
| | voltage range | Δv_{PCC} | ± 10 % |
| | frequency | f_g | 50 Hz |
| | power factor | $\cos(\varphi)$ | ≥ 0.9 |

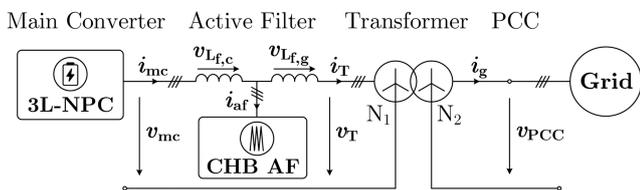


Fig. 3 Proposed hybrid medium-voltage multilevel converter

(CHB AF). The design and control of CHB converters for STATCOM applications has been investigated in previous works [23–25]. They are commercially available as SVC PLUS by Siemens [26] or SVC Light by Abb [27].

The MC supplies the active power of the hybrid converter system. In contrast, the AF compensates the MC current ripple and is ideally not exchanging active or fundamental reactive power, allowing a low CHB AF power rating. Compared to full power multilevel converters with comparable characteristics, the decoupling of high- and low-power components within the hybrid converter system offers important advantages such as high power density and efficiency. At the same time, the use of a conventional

IGBT-based high power converter leads to a high robustness and competitive costs.

In order to evaluate the competitiveness compared to conventional LCL-filter-based converter systems, a converter design and analysis in compliance with the medium-voltage grid code requirements is presented in Section 2.1. A reference LCL-filter design is described in Section 2.2 and used for the converter comparison in Section 2.3. In Section 3, the simulation results illustrate the harmonic performance of the hybrid converter under reasonable medium-voltage grid conditions.

2 Potential for grid applications

In this section, the competitiveness of the hybrid converter system compared to the conventional LCL-filter-based converter systems is evaluated. The converter designs are carried out considering the application of a grid-connected power converter and the associated harmonic requirements as defined by the medium-voltage grid code. A 3L-NPC is used as MC for the hybrid- and the LCL-filter-based converter system, respectively. The INFINEON IGBT power module (PM) FZ1200R45HL3 with a collector-emitter voltage of $V_{CES} = 4.5$ kV and a continuous DC collector current of $I_{C,nom} = 1200$ A is used for the MC, leading to the system parameters in Table 1. It is assumed that a medium-voltage transformer with a short-circuit voltage of 0.06 per-unit (pu) is used for the converter connection to the point of common coupling (PCC). According to common grid codes, the permitted grid voltage deviation is limited to $\pm 10\%$ of the rated grid voltage. The power factor range $\cos(\varphi) \geq 0.9$ is considered for capacitive and inductive loads. In order to ensure comparability, the converter systems are designed for equal grid code requirements according to the IEEE Standard 519.

Simulation models of the converter systems including datasheet-based semiconductor and heat sink models were implemented to ensure a realistic converter design. They use pulsewidth-modulation schemes for the calculation of time-variant current and voltage waveforms in order to compute reasonable conduction and switching losses. A maximum junction temperature of $\vartheta_j = 125^\circ\text{C}$ is assumed for all PMs.

2.1 Design of the hybrid converter system

Fig. 3 shows the grid-connected hybrid converter system composed of the 3L-NPC MC, the CHB AF, an MC- and grid-side filter inductance as well as the three-phase medium-voltage transformer. In comparison to a passive LCL output filter, the AF replaces the passive filter capacitances and thereby eliminates the oscillation susceptibility of the filter system. This allows an independent design of all filter components of the hybrid converter system.

To ensure high availability and low costs, the AF design of the hybrid converter system is based on power semiconductor devices with collector-emitter voltages of $V_{CES} = 1.2$ kV. Hence, the reference DC-link voltage of the CHB AF is $V_C = 700$ V. To limit the DC-link voltage deviation to $\Delta V_C/V_C \leq 10\%$ and considering operation at maximum grid voltage as well as transient currents, e.g. during grid-side faults, the cell capacitance is determined as $C_{af} = 0.7$ mF. The number of full-bridge cells per leg $n_{af} = 4$ is chosen to attain a maximum AF output voltage that corresponds in good approximation to the maximum MC output voltage.

2.1.1 Grid-side filter inductance: The grid-side filter inductance is dependent on the switching frequency of the CHB AF and the harmonic limits given by the IEEE Standard 519. Due to the direct parallel connection to the output, the AF provides the output voltage of the hybrid converter system and thereby determines the output grid current. Assuming the grid voltage as an undistorted fundamental voltage, the injected current harmonics are dependent on the grid-side filter inductance as well as the number of voltage levels $2n_{af} + 1$, the modulation index $m_{i,af}$ and the switching frequency $f_{sw,af}$ of the AF. For a maximum demand current equal to the rated current of 875 A, Fig. 4 shows the simulation results for the required grid-side inductance $L_{f,g}$ according to IEEE 519 as

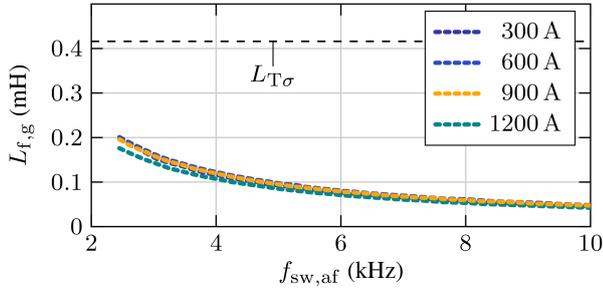


Fig. 4 Required grid-side inductance $L_{f,g}$ to meet IEEE 519 for a demand current of 875 A as a function of the AF switching frequency $f_{sw,af}$ and the injected grid current i_g

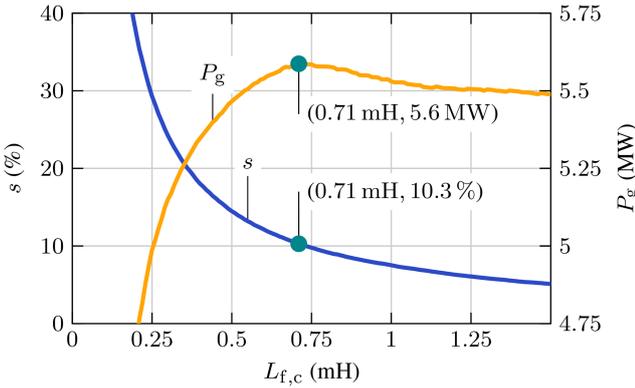


Fig. 5 Hybrid converter power ratio s and maximum active output power P_g at $\vartheta_j \leq 125^\circ\text{C}$ and $\cos(\varphi) = 1$

Table 2 Investigated PMs for application in the active filter

| Index | Company | Identifier | Type | $I_{C,nom}$, A |
|-------|----------|--------------|------------|-----------------|
| PM1 | INFINEON | FF150R12RT4 | Si-IGBT | 150 |
| PM2 | INFINEON | FF200R12KE4P | Si-IGBT | 200 |
| PM3 | INFINEON | FF8MR12W2M1 | SiC-MOSFET | 150 |
| PM4 | ROHM | BSM180D12P3 | SiC-MOSFET | 180 |

a function of the AF switching frequency $f_{sw,af}$. In order to take the modulation index into account, the results are carried out for output currents from 300 to 1200 A.

It can be seen that the required grid-side inductance decreases exponentially with the switching frequency, allowing values below $L_{f,g} \leq 0.2$ mH even for switching frequencies in the low kilohertz range. However, the short-circuit voltage of the grid-side transformer corresponds to a leakage inductance of

$$L_{Ts} = \frac{1}{2\pi f_g} v_k \frac{V_r^2}{S_r} = 0.42 \text{ mH} (\hat{=} 0.06 \text{ pu}), \quad (1)$$

clearly demonstrating that no additional grid-side filter inductance is needed for the hybrid converter system. Furthermore, Fig. 4 shows that a low grid-side inductance results in small changes of the modulation index over a wide range of output currents. Taking into account the beneficial impact of an increased switching frequency on the energy control, the AF switching frequency is set to

$$f_{sw,af} = 8.05 \text{ kHz} \quad (2)$$

in order to allow an accurate energy balancing for the operation with small passive filter components.

2.1.2 Converter-side filter inductance: As mentioned in previous sections, the AF output voltage determines the hybrid converter output current. Therefore, the output characteristics of the hybrid converter system are ideally not affected by the MC and

its filter inductance. However, the converter-side filter inductance limits the MC current ripple that needs to be compensated by the AF. Moreover, a reduction of the current ripple leads to a reduced current load of the MC and allows a higher fundamental current using the same power semiconductors. For a given switching frequency of the 3L-NPC, the MC current ripple can only be reduced with an increased converter-side filter inductance. Therefore the increased voltage drop across the filter inductance reduces the achievable voltage at the transformer primary side and thereby requires a higher transformer turns ratio. This clearly demonstrates the trade-off between a high and low converter-side filter inductance: a high converter-side inductance reduces the MC current ripple and allows an increased fundamental output current as well as a lower AF power rating. At the same time, it causes an increased voltage drop across the filter inductance and thereby reduces the achievable voltage at the transformer primary side. Since the output power depends on the fundamental output current and the achievable transformer primary voltage, a maximum power at the transformer primary side is expected for an inductance $L_{f,c,opt}$.

Fig. 5 shows the hybrid converter power ratio $s = S_{af}S_{mc}$ (where S_{af} and S_{mc} is the overall apparent power exchanged by the AF and the MC, respectively) and the fundamental output power P_g at $\cos(\varphi) = 1$ as a function of the converter-side filter inductance $L_{f,c}$. It is seen that the achievable output power decreases for low inductances, since the large MC current ripple requires a significant reduction of the fundamental current in order to keep the semiconductor junction temperatures below $\vartheta_j \leq 125^\circ\text{C}$. At the same time, the voltage drop $v_{L_{f,c}}$ increases with the filter inductance $L_{f,c}$ and leads to a reduction of the output power for high inductances. At $L_{f,c,opt} = 0.71$ mH, the combined impact of current ripple and voltage drop leads to a maximum achievable output power of $P_{g,opt} = 5.6$ MW at an electrical hybrid converter power ratio of $s = 10.3\%$.

According to Fig. 5, the converter-side filter inductance has a significant impact on the required power rating of the AF. This is caused by the MC current ripple arising due to the ripple voltage drop across $L_{f,c}$

$$\sum_{\nu=2}^{\infty} v_{i_{mc}} = \frac{1}{L_{f,c}} \int \left(\sum_{\nu=2}^{\infty} \nu v_{L_{f,c}} \right) dt, \quad (3)$$

where $i_{mc} = [i_{mc,u}, i_{mc,v}, i_{mc,w}]^T$ is the MC current, $v_{L_{f,c}} = [v_{L_{f,c,u}}, v_{L_{f,c,v}}, v_{L_{f,c,w}}]^T$ the voltage drop across the converter-side inductance $L_{f,c}$ and $\nu = \{h \in \mathbb{N} | h \geq 2\}$ the order of the voltage and current harmonics. Although further analysis of (3) is not within the scope of this paper, it shows the inversely proportional characteristic of the current ripple and the filter inductance seen in Fig. 5.

In the following, the resulting impact of the converter-side filter inductance on the AF design is investigated using the commercial 1.2 kV PMs given in Table 2.

The achievable AF switching frequencies are depicted in Fig. 6 as a function of the converter-side filter inductance. Therein, the operating points within and outside the safe operating area (SOA) of the PMs are represented by the solid and the dashed lines, respectively. For the optimal converter-side inductance $L_{f,c,opt} = 0.71$ mH, only the IGBT PMs PM1 and PM2 allow an operation at the determined AF switching frequency of $f_{sw,af} = 8.05$ kHz.

In order to achieve an accurate trade-off between additional semiconductor effort and maximum output power, the installed semiconductor power per output power ratio

$$\text{SPR} = \frac{S_{SC}}{P_g} \quad (4)$$

with the installed semiconductor power S_{SC} and the output power P_g is introduced. According to [28], the installed semiconductor

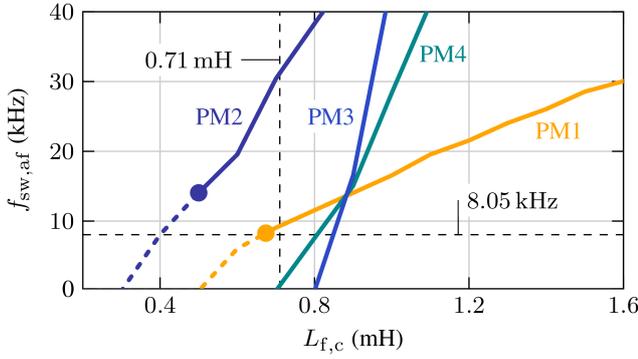


Fig. 6 Achievable AF switching frequency as a function of the converter-side filter inductance at $\theta_j \leq 125^\circ\text{C}$ with respect to the PM safe operating area limits (\bullet)

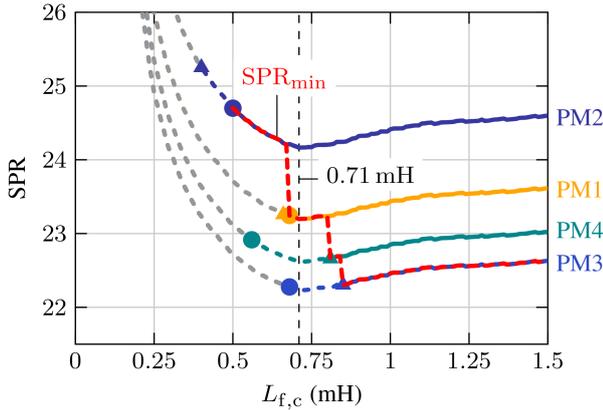


Fig. 7 Installed semiconductor power per output power ratio as a function of the converter-side filter inductance with respect to the PM limits given by a maximum junction temperature of $\theta_j \leq 125^\circ\text{C}$ (\blacktriangle) and safe operating area (\bullet)

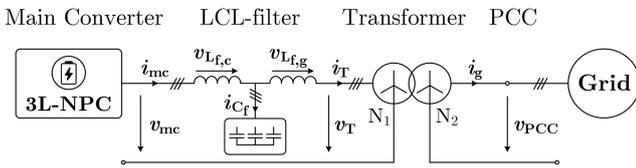


Fig. 8 Conventional LCL-filter-based medium-voltage 3L-NPC

Table 3 Reference LCL-filter parameters

| Parameter | Symbol | Value | pu |
|---------------------------|----------------|---------------|------|
| converter-side inductance | $L_{f,c(LCL)}$ | 1.25 mH | 0.18 |
| grid-side inductance | $L_{f,g(LCL)}$ | 1.8 mH | 0.26 |
| filter capacitance | C_f | 0.55 mF | 0.38 |
| damping resistance | R_d | 0.76 Ω | 0.35 |
| resonant pole frequency | ω_p | 1571 rad/s | 5 |
| damping factor | ζ_p | 0.33 | 0.33 |

power for IGBTs is given by $S_{SC(IGBT)} = 1.5V_{CES}I_{C,nom}$ per switch, considering a diode chip size of half the IGBT chip size. The installed semiconductor power for silicon carbide metal-oxide-semiconductor field-effect transistors (SiC-MOSFETs) is calculated by $S_{SC(SiC-MOSFET)} = V_{CES}I_{D,nom}$ per switch, since no diode chips are required due to the body diodes. In Fig. 7, the operating points meeting and exceeding the PM limits given by maximum junction temperature and safe operating area are represented by the solid and the dashed lines, respectively. The lowest achievable SPR at the optimal converter-side inductance is found by 23.2 for PM PM1, corresponding to an installed semiconductor power of 23.2 MVA per megawatt of output power. Since the output power is only slightly reduced for a small increase

of the converter-side inductance (see Fig. 5) and in order to ensure an operation within the safe operating area limit at $L_{f,c} = 0.67$ mH, a converter-side inductance of

$$L_{f,c} = 0.75 \text{ mH} (\hat{=} 0.11 \text{ p.u.}) \quad (5)$$

is used for the IGBT module PM1. A further reduction of the installed semiconductor power would be feasible using the SiC-MOSFETs PM3 or PM4 and further increased converter-side inductances of 0.85 or 0.81 mH, respectively. However, since the low AF switching frequency allows the use of IGBT modules at reduced converter-side inductances, the use of expensive silicon carbide PMs is avoided.

2.1.3 Transformer turns ratio: The MC DC-link voltage of $V_{dc} = 5.3$ kV leads to a maximum line-to-neutral output voltage of $V_{mc(max)} = 2.16$ kV. In consideration of the chosen filter inductances, operation at rated current and the worst case power factor of $\cos(\varphi) = 0.9_{ind}$, the achievable transformer primary voltage is limited to $V_{T(max)} = 2$ kV. At the upper limit of the permitted grid voltage range, the transformer secondary voltage is $V_{PCC(max)} = 2.1$ kV. Taking into account a control reserve of 3% of the MC DC-link voltage, the transformer turns ratio is determined to be

$$u_{T,af} = 0.91. \quad (6)$$

2.1.4 Active filter loss compensation: Neglecting the converter losses, the CHB AF supplies only harmonic reactive power and is thus not injecting a fundamental current. However, in order to compensate the semiconductor losses, a low fundamental current leading to an active power exchange is required. The worst case conduction losses of $P_{S,cond} = 4.9$ kW, turn-on losses of $P_{S,on} = 2.5$ kW and turn-off losses of $P_{S,off} = 3.4$ kW are determined for the IGBT module PM1, resulting in total AF semiconductor losses of $P_S = 10.8$ kW. With respect to the transformer turns ratio determined in (6) and operation at the lower limit of the permitted grid voltage range, a maximum fundamental current of

$$i_{af} = \frac{P_S}{\sqrt{3}u_{T,af} \cdot 0.9V_{PCC}} = 2.3 \text{ A} \quad (7)$$

is required for loss compensation. Hence, the AF fundamental current corresponds to <0.3% of the overall rated current and <2% of the rated AF current.

2.2 Reference LCL-filter-based converter system

The conventional and commonly used grid-connected LCL-filter-based converter system is shown in Fig. 8. Compared to the hybrid converter in Fig. 3, it uses passive filter capacitors instead of an additional power converter as an AF.

Due to the high-volume application, the design of LCL filters for power converters is addressed in a large number of research contributions. It has been investigated, e.g. in [29, 30] for low voltage applications and in [31–35] for medium-voltage applications. Contributions on LCL-filter design with comparable voltage and power rating can be found in [31–33]. The reference LCL-filter parameters used in this work are based on [31] and given in Table 3.

The output current harmonic spectrum of the converter system with LCL filter in Fig. 9 is based on the virtual voltage harmonic spectrum as introduced in [31]. It corresponds to the worst case current harmonics assembled over the entire operating range for modulation indices from 0.8 to 1.15. It is seen that all the worst case grid current harmonics are below the harmonic limits of IEEE 519, demonstrating the grid code compliance of the presented LCL-filter design. However, Fig. 9 illustrates the superior harmonic performance of the proposed hybrid converter system: despite the significantly reduced passive filter components, all grid

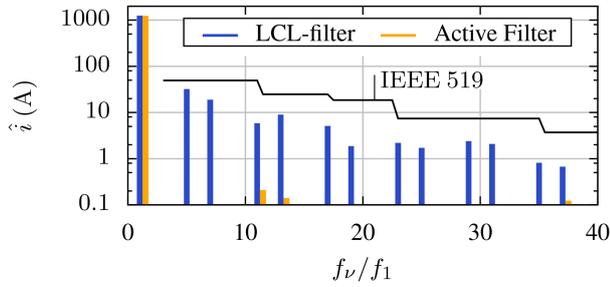


Fig. 9 Harmonic limits according to IEEE 519 and the worst case grid current harmonics of the investigated converter systems

Table 4 Comparison of the hybrid converter and the LCL-filter-based converter

| Parameter | Symbol | Δx in % |
|----------------------------------|---------------|-----------------|
| installed semiconductor power | S_{SC} | + 11 |
| converter-side filter inductance | $L_{f,c}$ | -40 |
| grid-side filter inductance | $L_{f,g}$ | -77 |
| total filter inductance | L_f | -62 |
| stored energy in $L_{f,c}$ | $W_{L_{f,c}}$ | -31 |
| stored energy in $L_{f,g}$ | $W_{L_{f,g}}$ | -83 |
| stored energy in L_f | W_{L_f} | -64 |
| maximum output power | P_g | + 17 |

current harmonics in the lower frequency range are limited below 1 A and thereby distinctly reduced compared to the conventional LCL filter. It has been shown in [31] that the highest current ripple occurs at the maximum modulation index, which is required at the upper limit of the grid voltage range (see Section 2.1). At this operating point, the hybrid converter and the LCL filter-based converter systems attain a grid current with a total demand distortion of 3%.

Similar to the hybrid converter system, the filter capacitors provide the output voltage of the LCL-filter-based converter system and thereby determine the output grid current. To meet the harmonic limits of the grid code, a sinusoidal output voltage with a small harmonic distortion is needed to reduce the harmonic distortion of the output current. This requires a high fundamental current through the filter capacitors and causes an additional current load of the converter-side filter inductance for a given output current. As a result, the increased voltage drop across the high-filter inductance leads to a significantly lower achievable transformer primary voltage compared to the hybrid converter system. Considering a control reserve comparable to the designed hybrid converter in Section 2.1, the transformer turns ratio results in

$$u_{T,LCL} = 0.8. \quad (8)$$

The maximum stored energies in the inductive filter components given by

$$\hat{W}_L = \frac{1}{2} L_L^2 \quad (9)$$

and

$$\hat{W}_C = \frac{1}{2} C v_C^2 \quad (10)$$

occur at the upper limit of the permitted grid voltage, the worst case power factor of $\cos(\varphi) = 0.9_{ind}$ and operation with maximum output current. They result in $\hat{W}_{L_{f,c}} = 4.7$ kWs for the converter-side filter inductance, $\hat{W}_{L_{f,g}} = 7.97$ kWs for the grid-side inductance and $\hat{W}_{C_f} = 5.2$ kWs for the filter capacitance. For the computation of the resulting damping losses, a resonant damping

circuit in series with the filter capacitors, as described in [31], is considered. Based on the required damping factor, an additional damping inductance and capacitance of $L_d = 0.68$ mH and $C_d = 0.6$ mF, respectively, are inserted in parallel with the damping resistor. As a result of the amount of capacitive reactive power required, significant losses of $P_d = 17$ kW per phase are caused by the damping circuit.

2.3 Comparison of the hybrid converter topology and LCL-filter-based converter systems

This section compares the designed hybrid converter system (Section 2.1) and the reference LCL-filter-based converter system (Section 2.2). The results in Table 4 show the relative variation of the converter parameters according to

$$\Delta x = \frac{x_{af} - x_{LCL}}{x_{LCL}}, \quad (11)$$

where x_{af} is a parameter of the hybrid converter and x_{LCL} the corresponding parameter of the LCL-filter-based converter system. Due to the replacement of the passive filter capacitors by a low power AF, the hybrid converter requires an 11% increase in installed semiconductor power compared to the conventional converter system. First of all, this eliminates the disadvantageous oscillation susceptibility of passive LCL filters. The absence of a resonant-pole frequency allows significantly reduced filter inductances, whereas the converter-side inductance is reduced by 40% and the grid-side inductance by 77%. Thereby, the required energy to be stored in the converter- and grid-side inductances decreases by 31 and 83%, respectively. Due to the use of DC capacitors in the hybrid converter and AC capacitors in the LCL-filter-based converter system, a comparison of the maximum energy stored in the filter capacitors is not reasonable. However, it should be emphasised that the AF current corresponds in good approximation to the MC current ripple, while the fundamental current share needed to compensate the semiconductor losses is negligible. In comparison, the LCL-filter capacitors carry a fundamental reactive current of several hundred amperes and therefore require an increased current rating compared to the DC-link capacitors of the AF. It is noteworthy that the semiconductor losses of the AF are significantly lower compared to the power losses of the LCL-filter damping circuit, even for resonant RLC damping. Furthermore, the reduced filter components of the hybrid converter allow an increased transformer primary voltage and therefore lead to a 17% higher maximum output power at the lower limit of the grid voltage and the in terms of output power worst case power factor of $\cos(\varphi) = 0.9_{cap}$.

The lowest efficiencies of the converter systems at operation with maximum output current occur at the lower limit of the grid voltage range and the power factor $\cos(\varphi) = 0.9_{ind}$. Considering MC losses, damping losses and filter inductance losses due to an assumed equivalent series resistance of 0.005 pu, the LCL filter with resonant damping circuit leads to a converter efficiency of $\eta_{LCL} = 96.9\%$. For the hybrid converter system the MC losses, the AF losses and the filter inductance losses result in an efficiency of $\eta_{af} = 97.6\%$.

3 Simulation results

Simulation results are carried out for the hybrid converter system designed in Section 2.1 at rated operation. The 3L-NPC MC is operated with space vector modulation according to [36]. Fig. 10 shows the voltages and currents of the hybrid converter and the transformer, respectively. The low switching frequency of the MC three-level output voltage leads to an output current with a total harmonic distortion of 9.8%. As a result of the multilevel output voltage and high effective switching frequency, the CHB AF in good approximation provides a sinusoidally shaped hybrid converter output voltage. Even for the low output filter inductance, this leads to a nearly sinusoidal output current with a harmonic distortion of only 0.9% that is injected into the medium-voltage

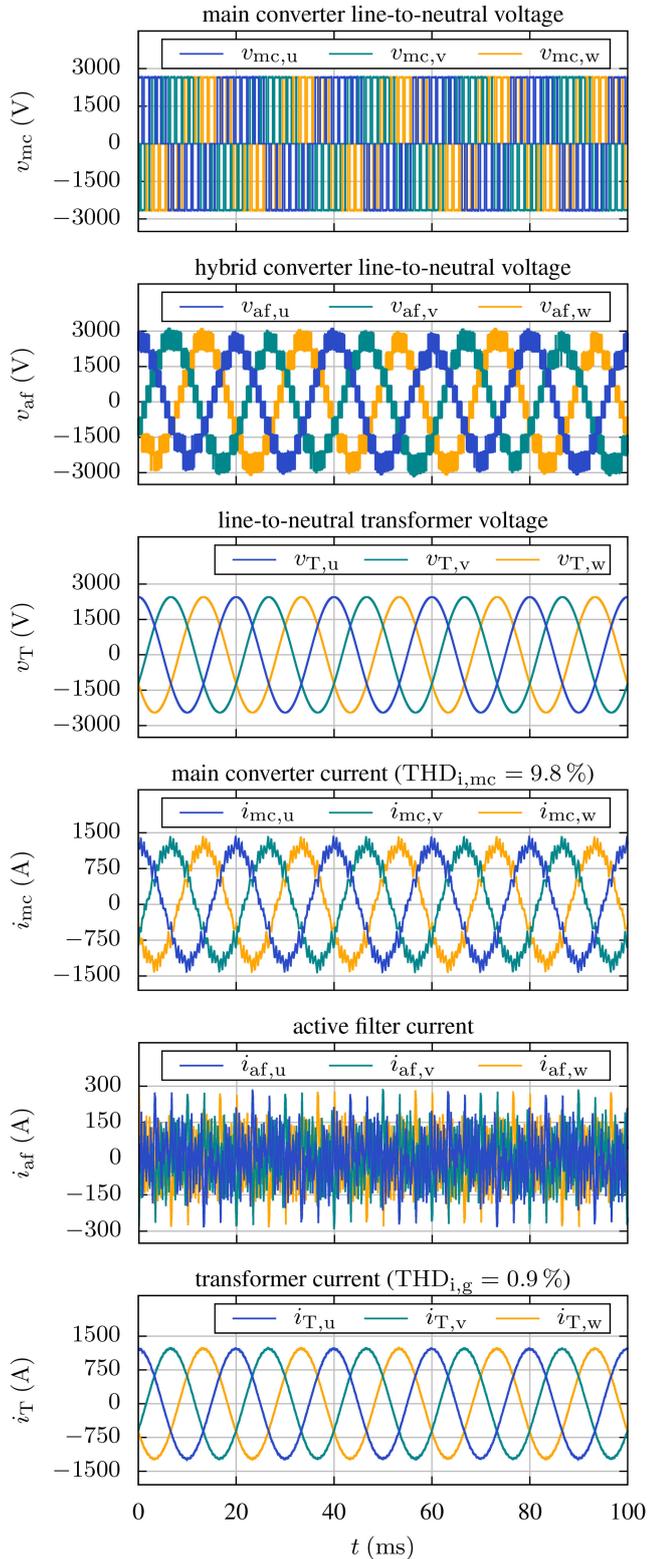


Fig. 10 Simulation results of the medium-voltage hybrid converter

grid. Due to the very low fundamental current i_{af} required for the CHB AF energy control (see Section 2.1.4), the AF current shown in Fig. 10 corresponds in good approximation to the total MC current ripple $\sum_{\nu=2}^{\infty} v_{i_{mc}}$ and has a root mean square value of $I_{af} = 92$ A. It is seen that the converter-side filter inductance effectively limits the MC current ripple to below 300 A, ensuring an operation within the SOA limits of the AF IGBT modules. The MC and the AF have an output power of $S_{mc} = 4.46$ MVA and $S_{af} = 0.35$ MVA, respectively. This leads to an AF to MC electrical power ratio of only $s = S_{af}/S_{mc} = 7.7\%$ and illustrates the advantage of the hybrid converter topology: A conventional MC

with IGBT PMs allows a high power rating of the converter system at low costs, while the parallel multilevel AF allows a high quality voltage-source output characteristic at only a small share of the total power. Therefore, the multilevel AF can be designed with low power components at low costs as related to the overall converter system. As a result, the hybrid converter offers superior characteristics such as high power density and low costs compared to conventional multilevel converters.

4 Conclusion

In this work, a novel hybrid converter topology for medium-voltage applications is proposed. It is composed of a high power conventional 3L-NPC and a low power CHB converter as an AF. A grid-application-based analysis reveals significant potential of the hybrid converter for increasing the efficiency and utilisation as well as reducing the costs and filter size of grid-connected medium-voltage converters. The proposed increase of the installed semiconductor power by 11% eliminates important disadvantages of passive LCL filters and reduces the total filter inductance by over 60%. As a result, the energy stored in the inductive filter components is reduced by over 60%, significantly impacting the filter costs. Since the resonant circuit is eliminated by the active output filter and no damping circuit is required, the hybrid converter surpasses the efficiency of the reference LCL-filter-based converter system. Further advantages are an increased converter utilisation, allowing a 17% higher output power at the worst case operating point, as well as a superior dynamic performance for a given control reserve. The developed control scheme ensures an accurate energy balancing of the AF DC-link capacitors and leads to an excellent harmonic performance of the load current under reasonable grid conditions, as shown by the simulation results. For applications such as grid-connected VSCs, electric drives and power-hardware-in-the-loop systems, this illustrates the significant potential and competitive characteristics of the proposed hybrid converter compared to conventional medium-voltage converter solutions.

5 References

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