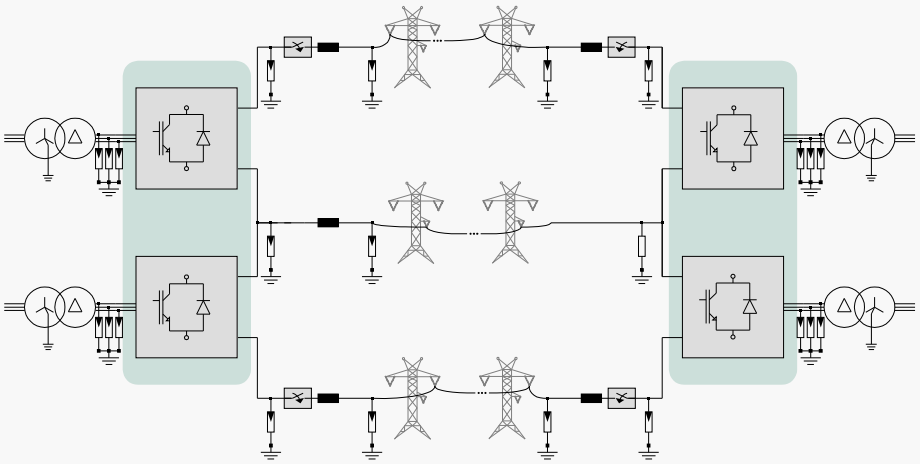
Doctoral Thesis

Simon Wenig

Potential of Bipolar Full-Bridge MMC-HVdc Transmission for Link and Overlay Grid Applications



Karlsruhe Institute of Technology

IEH

Potential of Bipolar Full-Bridge MMC-HVdc Transmission
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Potential of Bipolar Full-Bridge MMC-HVdc Transmission for Link and Overlay Grid Applications

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Karlsruhe, in May of 2019

Simon Wenig

Abstract

The increasing share of renewable energy sources imposes a strong pressure to adapt existing alternating current (ac) grids. Hence, especially caused by remote power in-feed leading to longer transmission distances and changing power flow patterns, a significant demand for highly flexible and powerful grid expansion measures exists. In this context, high-voltage direct current (HVdc) transmission based on the modular multilevel converter (MMC) topology meets the diverse technical needs – requested in recent grid codes – and provides a suitable option to face existing operational challenges.

As of today, mainly symmetric monopolar MMC-HVdc links have been built for offshore wind integration and market coupling purposes. Consequently, the majority of research activities is focussed on this system configuration. However, in light of large-scale onshore grid bottlenecks caused by a completely changed generation mix, even higher transmission capacities are requested and concerns regarding ac grid stability intensify. This amplifies the need for powerful and cost-effective transmission solutions providing inherent redundancy. Therefore, the bipolar MMC-HVdc solution with dedicated metallic return (DMR) gained further interest. Since contributions in the field are rather scarce, this doctoral thesis tackles several existing scientific gaps.

First, bipolar scheme control relations and energy balancing possibilities are unveiled in the course of a thorough circuit and energetic quantity analysis. This paves the way to integrate advanced fault handling, which comprises reactive current injection during ac faults and control-wise dc fault current interruption utilizing full-bridge (FB) submodules (SM). Based on this preparatory evaluation, a generic control concept is developed and presented. This aims to facilitate an in-depth analysis possibility, which is indispensable for various stakeholders to develop a more profound understanding.

Since the severity of interactions in bipolar schemes is significant, sophisticated and carefully designed protection concepts are required. This thesis proposes a multi-zonal approach including a backup-functionality to achieve highly selective and robust performance. Furthermore, to ensure a smooth liason with converter

controls, energy balancing during faults is further elaborated and signal routing is implemented in a coordinated manner.

Grid development and project-related design considerations are almost entirely based on simulative evaluations. Therefore, especially related to new classes of assets, a reliable simulation environment and fundamental design guidelines are of high importance. With respect to the previous requirements, an EMT simulation framework for bipolar MMC-HVdc schemes is compiled. On the one hand, this enables a thorough concept validation. On the other hand, the foundation for further studies and functional extensions is laid.

Finally, to also address ongoing conceptual considerations mainly driven by authorities and non-governmental organizations, prospects of the bipolar MMC-HVdc configuration related to dc overlay grids are outlined. As highlighted, especially a combination of converters equipped with FB SMs and efficiently utilized dc circuit breaker units presents an interesting use case.

Kurzfassung

Der zunehmend steigende Anteil erneuerbarer Energiequellen übt einen starken Anpassungsdruck auf heutige Wechselstromverbundnetze aus. Deshalb besteht ein erheblicher Bedarf an hochflexiblen und leistungsstarken Netzerweiterungsmaßnahmen. Dies ist insbesondere durch räumlich entfernte Einspeisung begründet, die zu längeren Transportwegen und geänderten Leistungsflussmustern führt. In diesem Zusammenhang erfüllt die Hochspannungsgleichstromübertragung unter Verwendung von Modular Multilevel Convertern die vielfältigen technischen Anforderungen und bietet eine adäquate Möglichkeit operativen Herausforderungen zu begegnen.

Da bis heute vornehmlich Gleichstromverbindungen zur Anbindung von Offshore-Windparks und zur Kopplung von Energiemärkten in der Konfiguration symmetrischer Monopol errichtet wurden, konzentriert sich hierauf die Mehrheit der Forschungsaktivitäten. Jedoch werden, angesichts großflächiger landseitiger Engpässe bedingt durch die gänzlich geänderte Einspeisesituation, noch höhere Übertragungsleistungen nachgefragt und Bedenken hinsichtlich der Systemstabilität verschärfen sich. Hierdurch verstärkt sich die Nachfrage nach leistungsstarken und kosteneffizienten Lösungen mit inhärenter Redundanz, weshalb auch die bipolare Hochspannungsgleichstromübertragung mit metallischem Rückleiter zusätzliches Interesse erlangte. Da Beiträge in diesem Feld jedoch eher selten zu finden sind schließt diese Arbeit einige der wissenschaftlichen Lücken.

Zu Beginn werden regelungstechnische Zusammenhänge und Möglichkeiten der Energiebilanzierung in bipolaren Anordnungen im Rahmen einer vollständigen Schaltungsanalyse und Untersuchung energetischer Größen aufgedeckt. Dies ebnet den Weg zur Integration fortschrittlicher Fehlerbehandlung, was Blindstromeinspeisung im ac Fehlerfall sowie die regelungstechnische Unterbrechung von dc Fehlerströmen mittels Vollbrückensubmodulen umfasst. Basierend auf der vorbereitenden Auswertung wird im Anschluss ein generisches Regelungskonzept entwickelt und präsentiert. Dieses zielt auf eine tiefgehende Analysemöglichkeit ab, welche für verschiedene Beteiligte eine unabdingbare Funktionalität zur Erlangung eines fundierten Verständnisses darstellt.

Da das Ausmaß von Interaktionen in bipolaren Anordnungen signifikant ist sind differenzierte und sorgfältig ausgestaltete Schutzkonzepte erforderlich. Diese Arbeit schlägt ein mehrzoniges Konzept mit Backup-Funktionalität zur Gewährleistung eines hochselektiven und robusten Verhaltens vor. Darüber hinaus, um eine leichtgängige Verbindung mit der Umrichterregelung zu gewährleisten, ist die Energiebilanzierung während Fehlerfällen weiter ausgearbeitet sowie eine koordinierte Signalführung implementiert.

Netzentwicklung und projektbezogene Designüberlegungen basieren nahezu gänzlich auf simulativen Untersuchungen. Daher sind eine zuverlässige Simulationsumgebung sowie grundlegende Design-Richtilinien von immenser Wichtigkeit, was insbesondere bei neuen Klassen von Betriebsmitteln zutrifft. Unter Berücksichtigung der vorherigen Anforderungen wurde eine Simulationsumgebung für bipolare Gleichstromübertragungssysteme erstellt. Einerseits ermöglicht dies eine gründliche Validierung, andererseits ist die Basis für zusätzliche Studien und funktionale Erweiterungen gelegt.

Schlussendlich werden Perspektiven zu bipolaren – dem heutigen ac Verbundnetz überlagerten Gleichstromnetzen – dargelegt, um sich ebenso mit laufenden konzeptionelle Überlegungen getrieben durch Behörden und Nichtregierungsorganisationen zu befassen. Wie hervorgehoben bietet hier eine Kombination aus Umrichtern mit Vollbrückensubmodulen und effizient eingesetzten dc Leistungsschaltern einen interessanten Anwendungsfall.

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Chapter 1

Introduction

One fundamental challenge of modern society is to ensure sustainable electric power supply with maximum reliability and affordable price. This is motivated primarily by environmental aspects. Nevertheless, even though limitation of climate change is based on a broad consensus, also increasingly complex political conditions encourage authorities to strive for enhanced resource-independence to preserve future economic competitiveness and social prosperity. When transferred to a purely technical layer, the associated and still ongoing task, commonly referred to as energy transition, requires substantial efforts and progress in various fields. These are namely renewable power generation and energy storage, transmission and distribution as well as operational flexibility and grid stability preservation.

In Europe, but also worldwide, high-voltage direct current transmission based on advanced modular multilevel converter (MMC-HVdc) technology turned out to provide an economically and technically viable solution to solve a wide range of renewable energy integration and network enhancement issues. As of today, commonly applied monopolar MMC-HVdc configurations have not yet reached transmission capacities to present a severe threat to alternating current (ac) grid stability. But, this drastically changes in the case of more powerful MMC-HVdc installations to re-route large-scale inter-regional power flows, which is typically caused by aggregated in-feed of renewable energy in remote areas and thereto related high ac line utilization. Therefore, providing an inherent redundancy, bipolar MMC-HVdc configurations appear beneficial for bulk power transmission projects. This is especially valid if advanced full-bridge (FB) submodules (SMs) with general current interruption capability are utilized. Regarding available literature, such realizations have been hardly studied, even though overall complexity significantly exceeds the one of their monopolar counterparts. Within the described context, this thesis investigates single point grounded bipolar FB MMC-

HVdc with dedicated metallic return (DMR) and assesses link as well as overlay grid applications.

1.1 Energy Transition Progress and HVdc Evolution

Retrospectively, as the energy transition forged ahead in several waves, the importance of state-of-the-art HVdc technology continuously gained momentum. Initially, during post-millennial industrialized solar and wind generation rollout, neither line commutated converters (LCC) nor low-level (two- or three-level) voltage source converters (VSC) were of crucial relevance from an operational perspective with few exceptions related to single European LCC interconnectors[1]. In the following, starting with invention of MMC-HVdc topologies [50], general conditions changed as a disruptive power electronic option for massive offshore wind deployment, ac grid bottleneck removal and market area coupling became available. As a result, MMC-HVdc schemes were widely deployed and achieved a profound degree of technical maturity within the last decade. This was caused by both increasing scientific activity due to the tremendous application potential and also industrial experience through various projects, where stakeholders were able to gather knowledge during several specification, engineering and commissioning stages.

Nevertheless, reviewing progress in the light of the energy transition or even society's global carbon footprint, total share of renewable generation and related grid expansion projects as well as their dimensions still need to expand. To halt or even reverse the trend of rising CO_2 emissions, renewable capacity increase must exceed and not only compensate surging global electricity demand[2]. Even though there has been substantial progress, see stalling emissions in times of significant economic growth within the last five years and an upward trend of renewable share on global primary energy demand in Fig. 1.1 (a)-(b), large scale embedded transmission solutions to integrate massive remotely installed renewable energy sources with main load centres are urgently needed. While sole ac grid enforcement is mostly limited in terms of operational boundaries and sometimes even restricted due to non-technical aspects, authorities in some countries are targeting bulk-power MMC-HVdc corridors to solve several problems

[1] The utilization of LCC technology regarding the connection of far distant generation at ultra high voltage levels and power ratings up to more than several gigawatts, e.g. hydro power plant grid integration in Asia and South America, shall not be unmentioned. But, those project are classified in a different manner, as dominantly fundamental power supply motives and grid development purposes triggered their installation. This is in contrast to the intention to realize the so called energy transition, where conventional generation capacities within already existing grid structures shall be substituted by more volatile renewable energy sources.

[2] As massive electrification within the transportation sector and nearly all other branches is assumed the role of renewable power supply is considered crucial and increasingly important to achieve global emission reduction targets.

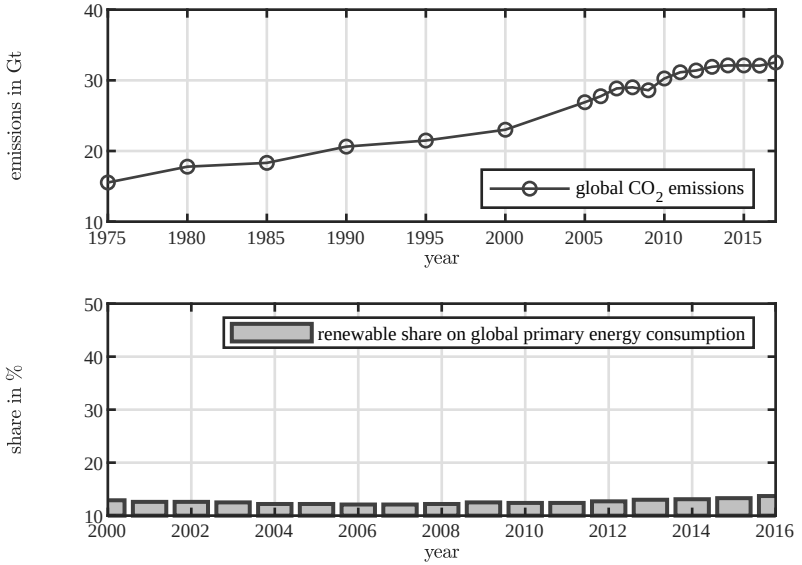

Figure 1.1: Progress of the ongoing global energy transition: (a) global CO_2 emissions, (b) global renewable share on primary energy consumption; data provided by International Energy Agency (IEA).

simultaneously [129]. These are: *i)* the relief of overloaded ac lines or even bypassing whole grid corridors, *ii)* the prevention of excessive renewable energy curtailment due to a lack of transmission capacity, *iii)* the potential to utilize long underground cable segments to minimize visible impacts, *iv)* the capability to connect remote resources to urban or industrial electricity consumption hubs and *v)* the unprecedented operational flexibilities and control features compared to previous generations of HVdc technology to account for changing grid conditions. Analyzing these diverse requirements and the desired single corridor transmission capacities of several gigawatts, bipolar MMC-HVdc configurations appear superior compared to multiple monopolar solutions in parallel. Also from an operational perspective, as already indicated in [121], benefits are mainly found in terms of inherent redundancy at reduced investment expenses compared to multiple parallel links. This includes remaining partial availability in the case of a wide range of contingencies.

1.2 Main Objective and Regulatory Scope

Electricity generation has been historically dominated by thermal power plants. Accordingly, power systems were built for this use-case and optimized over decades. As utilized technology has only been subject to moderate changes, profound understanding of related phenomena, well developed normative frameworks and substantial project as well as component related experiences were developed and gathered. In contrast, facing progress leading to latest generation power electronic assets based on either MMC-HVdc or different power electronic technology, a tremendous change in complexity and related ac grid dynamic characteristics takes place. While this influences fault and performance validation studies in a µs time domain, as visualized in Fig. 1.2, adapted and extended simulation frameworks are required to minimize or at least quantify novel technology-dependent risks at early project preparation stages or during design phase. Within this doctoral thesis, requirements to derive a generic bipolar MMC-HVdc control and protection concept for fault, dynamic performance and interaction studies are compiled and further elaborated. This includes system modeling, an overview of SM realizations and aspects of modulation. Though, the main focus lays on grid synchronization and sequence detection, control design for conventional operation and fault handling purposes, balancing during and subsequent to fault events, protection design as well as selected aspects of scheme wide system-performance coordination for link and overlay grid applications.

With regards to the regulatory frame presented in [125] and [114], research is guided by the following key premises. There shall be:

- capability to withstand quantity fluctuations and variations at the specified connection point (frequency, ac and dc voltages)
- conformity with operational and dynamic requirements related to active and reactive power control (control modes, technical constraints, prioritization)
- fault ride-through (FRT) capability and post fault recovery
- enhancement potential for advanced control features (mitigation or even suppression of interactions, power oscillation damping, black start)
- and selective fault handling and protection design including a compliant priority order

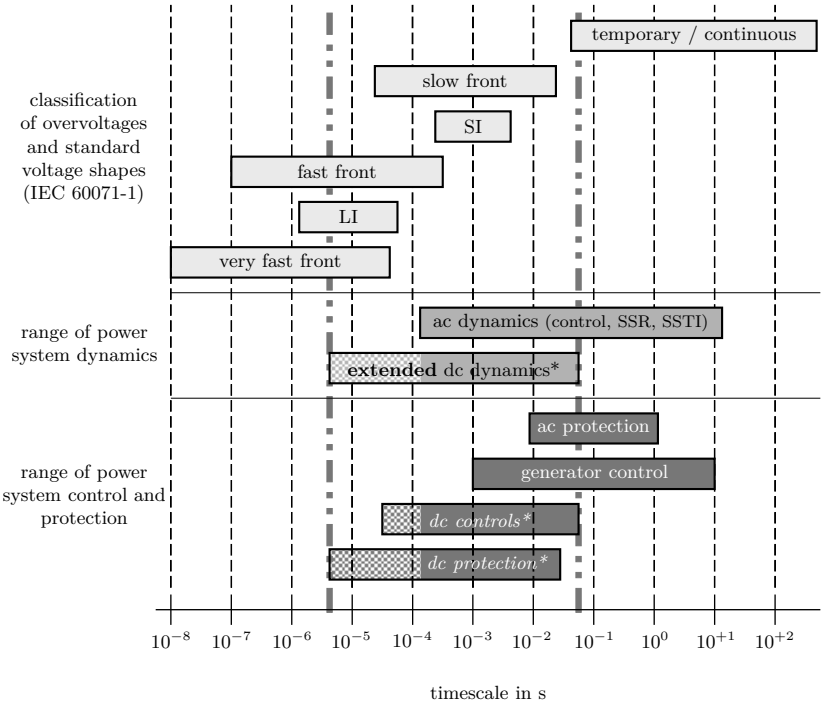

Figure 1.2: Classification of overvoltages and power system phenomena indicating changes related to recent MMC-HVdc technological developments (bars marked with *); modified representation related to [116] and [135]; abbreviations given in the Appendix.

1.3 Potential Impact and Intended Contribution

Even though a broad range of power engineering disciplines is striven, contribution particularly targets control, protection and system performance aspects. In order to unveil the full potential of bipolar FB MMC-HVdc structures:

- a set of relevant basics in accordance with the desired simulation framework objective is compiled. This includes MMC basics, system configuration overview and state-of-the-art grid-code requirements
- a consistent converter-individual control and arm sum voltage balancing concept is proposed
- the latter is extended with comprehensive ac FRT as well as control-wise dc fault current interruption (FCI) capability utilizing FB SMs
- and a multi-layered protection and fault handling concept to detect and differentiate typical faults within bipolar schemes is introduced

By means of electro-magnetic transient (EMT) simulations the proposed framework facilitates a deeper understanding of occurring characteristic fault behavior, shows the extent of acdc as well as intra-scheme interactions, validates dynamic performance and permits quantification of converter-internal effects under various operation conditions. Supplementary, potentials related to future overlay grid application broaden the acquired insights.

1.4 Thesis Outline

This doctoral thesis is partitioned into eight chapters:

- Initially, Chapter 2 introduces fundamentals of MMC-HVdc systems. This comprises MMC basics, SM topologies and their switching states, an overview of modulation methods as well as modeling approaches suitable for EMT studies. Additionally, a brief introduction of typical system configurations and recent grid-code requirements is provided.
- Chapter 3 compiles control fundamentals and energetic relations followed by a thorough literature review. Subsequently, the utilized control and balancing concept, consisting of four layers and several subordinate functional blocks, is presented.
- In Chapter 4 a multi-stage fault handling and protection concept is introduced. This ensures a clear differentiation of various fault types and enables an appropriate response to contingencies. Furthermore, energy-balancing restrictions during faults and backup protection are discussed.

- Related to a bipolar scheme utilizing overheadline (OHL) transmission, Chapter 5 elaborates a generic design including brief insights into control, fault handling and protection parameter determination.
- Closely linked to the previous part, Chapter 6 evaluates bipolar link response to various contingencies. Results of EMT simulations are analyzed to validate the proposed performance and selected sensitivities are highlighted to promote a deeper understanding of parametric dependencies.
- Beyond, to also address the arising technical potential for future applications, Chapter 7 complements this thesis. The intrinsic potential of bipolar FB MMC-HVdc related to multi-terminal and overlay grid transmission solutions is highlighted.
- Finally, Chapter 8 concludes the thesis and names additional research possibilities.

A reading of this thesis following the sequence of content is recommended as the individual chapters are built upon each other. Mathematical derivations, transformations or additional technical details related to the investigated schemes are summarized within the Appendix.

Chapter 2

Fundamentals of MMC-HVdc Systems

This chapter presents MMC-HVdc fundamentals and links related literature. Beyond a brief introduction of the MMC topology itself, types of SMs are listed and switching states during operation as well as related insulated gate bipolar transistor (IGBT) blocking behavior is composed. Further, modulation and converter modeling accuracy are briefly addressed, since these aspects are considered vital for a suitable EMT simulation framework. Finally, system configurations in different variants are described and the bipolar solution is briefly compared to monopolar schemes in terms of macroscopic characteristics. An overview of the regulatory frame complements the analysis and collects a set of operational requirements to be considered in the subsequent control and protection design.

2.1 Modular Multilevel Converter Basics

Introduction of the MMC enhanced the capability to connect remotely located renewables and broadened the transmission grid extension and enforcement portfolio [130, 50]. Compared to LCC and previously available VSC topologies, several technical and economic drawbacks have been resolved and disruptively boosted the VSC-HVdc power transmission market. Alongside that development, a fully new class of modular power converters for various applications has been introduced [62, 79]. Underlying superior technical and economic characteristics, especially related to MMC-HVdc, are mainly affected by the following reasons:

- MMCs offer a high degree of modularity and are easily scalable for a wide power range. Therewith associated benefits comprise utilization of medium-voltage products and efficient manufacturing possibilities.

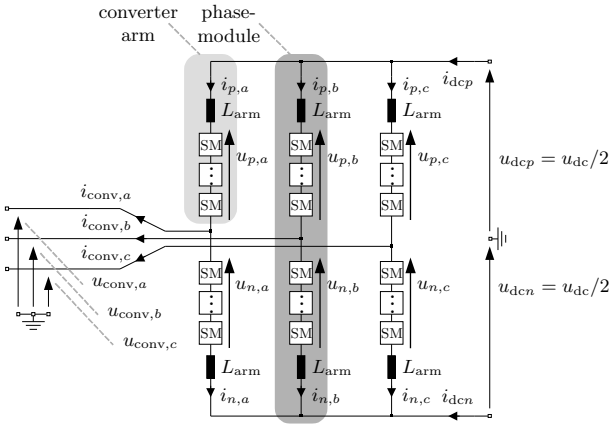

Figure 2.1: MMC three-phase equivalent circuit.

- There are significantly reduced or even no ac filter needs due to quasi-sinusoidal output quantities, which directly impacts converter station space requirements.

- Active and reactive power at the ac point of common coupling (PCC) can be independently controlled.

- Advanced operational features of MMCs can be unveiled by utilizing the distributed nature of SM energy storage to buffer fluctuations and to suppress acdc interactions.

- The implementation of redundant SMs reduces unscheduled downtime due to improved predictability and maintenance strategies.

- Lower losses occur due to the reduced switching frequency of power electronic devices to insert or bypass individual SMs compared to pulse-width modulation-based (PWM) switching of multiple series-connected devices in low-level VSC applications in a kilohertz range.

Further amplified with commissioning of the first MMC-HVdc project *Trans Bay Cable* in the early year 2010 by SIEMENS [98], extensive research in power transmission, high voltage engineering, power electronics as well as control development was initiated. Besides analytical fundamentals and design optimization, see [49, 126, 39, 77], especially controls – covered separately in section 3.3 later on – attracted significant scientific interest.

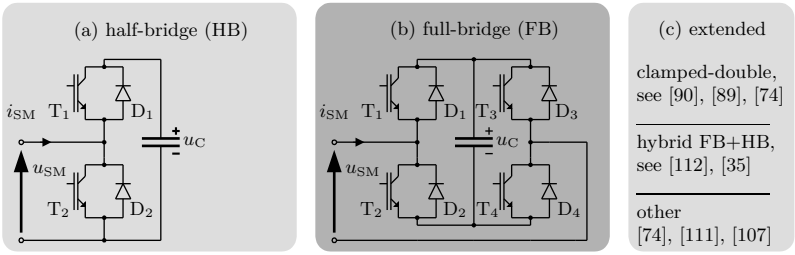

Figure 2.2: Overview of SM topologies: (a) half-bridge (HB), (b) full-bridge (FB), (c) extended SMs.

Typically, a three-phase MMC, excluding peripheral equipment as depicted in Fig. 2.1, is composed of three phase-modules ($y \in \{a,b,c\}$) consisting of an upper (subscript p, positive) and lower (subscript n, negative) converter arm. Here, each arm is equivalent to a series connection of m SMs and an arm inductor L_{arm}. Different from conventional VSC topologies, the distributed nature of energy storage enables arm-independent output voltage emulation by either inserting or bypassing corresponding SM capacitors to obtain nearly undistorted sinusoidal output voltages and currents.

2.1.1 Submodule Topologies

The selection of a SM topology presents a key design factor influencing a variety of MMC-HVdc scheme characteristics. Besides economic aspects like losses and hardware costs, mainly linked to the number of utilized power electronic devices [65], operational performance related to FCI capability and transient[1] scheme behavior are affected. As of today, half-bridge (HB) SMs, see Fig. 2.2 (a), present the state-of-the-art for offshore wind integration and interconnector projects with full or a very high share of cable segments. Due to a generally reduced fault likeliness caused by external origin (e.g. lightning, pollution), relatively slow fault clearance by ac circuit breaker operation within several grid-cycles remains acceptable. But, higher power ratings and utilization of OHL segments onshore require improved performance to meet tightened fault clearance and auto-reclosure requirements defined by transmission system operators (TSOs). Representing one feasible alternative, an MMC-HVdc solution with FB SMs as shown in Fig. 2.2 (b) has been selected for a first bipolar transmission project called ULTRANET in Germany [96, 8] and is further investigated within this thesis. Obviously, besides boosted operational flexibility like control-wise or IGBT blocking-based FCI addressed

[1] Scheme response is in a µs timescale. There is a negligible impact of the converter control system on initial scheme response.

within section 2.1.3, utilization of FB SMs significantly increases operational losses due to the doubled number of participating power electronic switches. Therefore, the overall degree of FB-utilization for MMC-HVdc applications is still relatively scarce and mostly linked to mandatory operational demands. Those are for example fast control-wise dc-side auto-reclosure with permanent reactive power supply on the ac-side or improved multi-terminal or overlay grid extendability.

For the sake of completeness, see also Fig. 2.2 (c), research activities trying to resolve this drawback shall be listed even though these topologies are not further addressed. Their aim is to develop solutions beyond conventional FB solutions offering similar operational benefits but with optimized system loss conditions. In [89] a clamp-double SM (CDSM) has been proposed, which represents a series connection of two HB SMs including a conduction-loss-optimized intermediate switch. This switch is turned off during contingencies to form a structure similar to a FB SM, where a countervoltage with respect to the present current direction is applied to interrupt SM current flows. The achievable loss reduction compared to a pure FB solution equals approximately 20 % according to [65]. Another widely discussed measure is hybrid MMCs consisting of mixed SM stacks comprising conventional [112, 35] or enhanced series-parallel HB and FB cells [107]. Hereby, loss reduction can be achieved by reducing the ratio between FB and HB modules. But, to maintain fault blocking capability, this measure is restricted as a critical minimum countervoltage level shall not be violated[2].

2.1.2 Switching States in Normal Operation

Typically HB cells equipped with two IGBTs (T_1, T_2) and two anti-parallel diodes (D_1, D_2) are deployed in existing MMC-HVdc projects, see Fig. 2.2 (a). To set individual output voltages u_{SM} the SM capacitor is either bypassed or inserted by switching on the corresponding power electronic device T_2 or T_1, respectively. While inserted, this charges or discharges the SM capacitor (voltage marked as u_C) related to the prevalent arm current direction as given in the upper part of Table 2.1. Assuming a stack with unequal charging states, a suitable intra-arm balancing logic selects SMs to achieve a homogenizing behavior, where activation order either starts from lowest or highest capacitor voltage, respectively. Generally, this principle is similar for FB applications consisting of four IGBTs (T_1-T_4) and anti-parallel diodes (D_1-D_4) as shown in Fig. 2.2 (b). Nevertheless, due to the additional degree of freedom related to the achievable negative output voltage, increased complexity (dimension of switching logic signals) and coordinated activation of pairs of IGBTs need to be resolved. Considering also the fact that two bypass states exist, mainly from an operational and reliability perspective, those should be altered to distribute stresses equally among the

[2]It should be noted that hybrid MMC solutions may additionally require adapted modulation concepts and have an impact on converter-internal energetic behavior.

individual semiconductor devices.

2.1.3 Blocking Behavior

Beyond conventional operation, contingencies which can not be handled by control actions and arbitrary malfunctions must strictly lead to immediate IGBT blocking. This is to avoid irreversible hardware damage primarily due to thermal issues. Typically, as these events represent the most severe hardware stresses, design of MMC-HVdc schemes and mainly selection of semiconductors are determined by their severity.

Partially, conventional HB-realizations behave differently in blocked state compared to FB systems as indicated in Fig. 2.3 and Table 2.2. Immediately at the blocking instant, currents commutate into the anti-parallel diodes. Here, either cell capacitors are directly bypassed (diode rectifier behavior, HB-specific) or the full stack is inserted and a countervoltage is applied while modules are further charged. This effect lasts either until the voltage across the SM stack drops below the arm sum voltage, whereby remaining magnetic energy within the network is fully dissipated, or an ac circuit breaker has cleared the fault. While the latter behavior equals the one of a FB solution for a positive SM current, the uncontrolled diode rectifier behavior can only be interrupted by opening corresponding ac circuit breakers. This typically requires several grid cycles and must be considered for the design of current and thermal withstand capability of the anti-parallel diodes or an additionally triggered bypass thyristor.

Shifting the view towards the right part of Fig. 2.3, blocking of FB modules has

Table 2.1: HB and FB SM states during conventional operation.

topology	u_{SM}	T_1	T_2	T_3	T_4	i_{SM}	$\mathrm{d}u_{\mathrm{C}}/\mathrm{d}t$	state
HB	$+u_{\mathrm{C}}$	1	0	-	-	>0	>0	inserted
HB	$+u_{\mathrm{C}}$	1	0	-	-	<0	<0	inserted
HB	≈ 0 V	0	1	-	-	>0	-	bypassed
HB	≈ 0 V	0	1	-	-	<0	-	bypassed
FB	$+u_{\mathrm{C}}$	1	0	0	1	>0	>0	inserted
FB	$+u_{\mathrm{C}}$	1	0	0	1	<0	<0	inserted
FB	$-u_{\mathrm{C}}$	0	1	1	0	>0	<0	inserted
FB	$-u_{\mathrm{C}}$	0	1	1	0	<0	>0	inserted
FB	≈ 0 V	1	0	1	0	>0	-	bypassed
FB	≈ 0 V	1	0	1	0	<0	-	bypassed
FB	≈ 0 V	0	1	0	1	>0	-	bypassed
FB	≈ 0 V	0	1	0	1	<0	-	bypassed

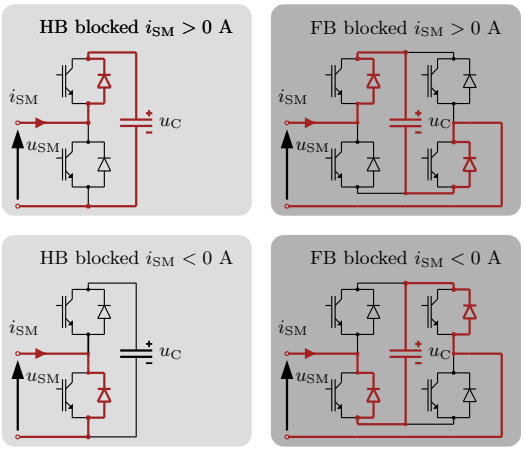

Figure 2.3: HB and FB SM blocking behavior.

an identical effect regardless of the SM current direction. The cell capacitors are always inserted in such a way that the FB voltage counteracts the present current flow, which is therefore quickly terminated[3]. Nevertheless, also in this realization, unwanted charging occurs in case the voltage across the SM stack exceeds the present arm sum voltage or remaining magnetic energy must be dissipated, even though the immediate need to open the ac circuit breakers becomes obsolete for faults on the dc-side.

[3]Faults between converter transformer and SM stacks are continuously fed from the ac-side.

Table 2.2: HB and FB SM states subsequent to IGBT blocking.

topology	u_{SM}	T_1	T_2	T_3	T_4	i_{SM}	du_C/dt	state
HB	$+u_C$	0	0	-	-	> 0	> 0	blocked
HB	≈ 0 V	0	0	-	-	< 0	-	blocked
HB	$= 0$ V	0	0	-	-	$= 0$	-	blocked
FB	$+u_C$	0	0	0	0	> 0	> 0	blocked
FB	$-u_C$	0	0	0	0	< 0	> 0	blocked
FB	$= 0$ V	0	0	0	0	$= 0$	-	blocked

2.1.4 Modulation Methods

The main task of the modulator, acting as the interface between control system and hardware, is to translate corresponding reference values into individual SM switching commands. In addition, retention of SM capacitor voltage deviations within a tolerable range must be assured by appropriate insertion strategies [133]. The resulting multi-dimensional optimization task [77], which underpins the importance of appropriate logic-/algorithm-design and corresponding parameter selection, is to determine a trade-off between average semiconductor switching frequency (switching losses), maximum allowed SM voltage deviation from steady-state during operation (defined by a tolerance band) and required size of the SM capacitor or the selected number of spare SMs. Focussing further on control aspects, additional delays and the discontinuous output voltage due to the binary switching states of single SMs impact converter controls and subsequently MMC dynamics. Therefore, simulative representation of modulation phenomena is essential to obtain feasible results in the context of EMT studies.

Generally, a wide spectrum of literature covers modulation aspects for different MMC applications in an industrial or power transmission context [79]. But, while the overall cell number and the relative height of individual cell voltages related to the maximum arm output voltage strongly differ, suitability for MMC-HVdc applications with several hundred modules operated at low single digit kilovolts is of particular interest. The following paragraph briefly evaluates:

- precalculated switching pattern methods
- space vector methods
- multi-carrier methods
- algorithm-based methods

and identifies major characteristics.

One possibility to implement cell modulation is the utilization of precalculated switching patterns updated every grid-cycle depending on the intended operation setpoint provided by the control system. Those can be designed to eliminate either specific harmonics or to reduce the average switching frequency of power electronic devices to minimize corresponding losses [49, 37]. Furthermore, adaptions to deal with circulating currents by adjusting the width of square pulses are presented in [36] and capacitor voltage ripples are minimized in [38] by means of predictive cell sorting. Nevertheless – with respect to the intended application, advanced fault handling and operation under varying grid frequency or unbalanced ac grid conditions – performance including active cell voltage balancing measures appear limited due to the limited response speed within approximately one grid-cycle.

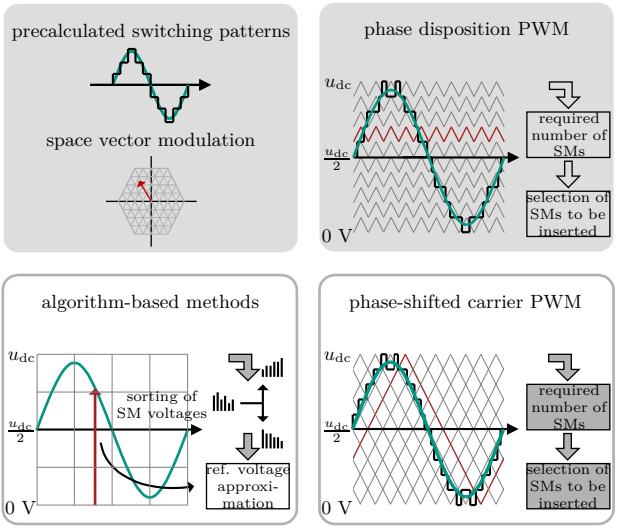

Figure 2.4: Overview of MMC modulation schemes.

Regarding extended Space Vector Modulation (SVM) schemes, as further elaborated in [49], the required reference voltage vector is compared with predetermined switching states as indicated in Fig. 2.4. Here, the closest neighbouring options (by assigning appropriate duty-cycles) enable emulation of the desired output behavior. Drawbacks of this method are quickly increasing complexity for high numbers of SMs, neglection of fluctuating SM voltages and sole consideration of phase-related output quantities. This contradicts individual arm reference assignment requirements by advanced control and balancing schemes, as no differentiation between upper and lower arm is made.

Also, PWM schemes have been investigated for MMC applications by utilizing a multitude of – triangular- or sawtooth-type – signals. Depending on the arrangement of the carriers, this leads to either in-phase stacked Phase Disposition-PWM (PD-PWM) or Phase-Shifted Carrier-PWM (PSC-PWM) techniques. By comparing the requested reference waveform with the carrier signals, the number of cells to be inserted is determined by a simple comparison. Again, methods differ related to application to a full phase in [86] or directly to an individual arm [102]. Subsequently, the final switching decisions for each arm are derived in a second stage[4] with respect to present current direction and individual SM charging

[4]Ordinary modulation schemes do not provide this downstream cell selection logic (reflecting instantaneous SM capacitor charging status and arm current direction) and each SM is assigned

status to achieve a harmonizing behavior of cell voltages. The corresponding basic principle is depicted for individual arm modulation in Fig. 2.4. As carriers are not continuously adapted with respect to varying cell voltages potential discrepancies related to requested and effective output voltage with unfavourable impacts on converter controls may occur. This is leading to tightened requirements related to average switching frequency as well as SM capacitor size to minimize intra-arm voltage deviations.

Consequently, algorithm-based methods arose. Typically, those are based on Nearest Level Control (NLC) modulation [100, 27, 30] schemes, which differ compared to previous approaches due to their immediate consideration of SM voltages. Hereby, a given arm reference value is approximated by accumulating the measured individual SM voltages within the correspondingly sorted vector and inserting the cells until the requested setpoint is exceeded, see Fig. 2.4. While activation logic dealing with the last cell is generally uncritical for applications with a relatively high number of levels, more sophisticated methods like hybrid modulation or rather tolerance band modulation are beneficial for low-level MMCs or within relatively flat peak regions of reference voltages as discussed in [42] and [32].

Even though these methods increase complexity related to signal acquisition and computational resources, the improved accuracy – especially in the case of significantly deviating SM voltages – unveils a set of previously non-accessible degrees of freedom and benefits. Those are: *i)* an increasing permitted voltage operation range of SMs including less stringent sorting repetition rate requirements, *ii)* more flexible cell design and *iii)* preservation of highly accurate emulation of requested arm reference voltages during contingencies.

2.1.5 Submodule Stack Representation

Increasing utilization of power electronics in high voltage transmission networks imposes challenges related to operational risk management. Beyond conventional power system simulation (load flow, phasor domain) and small-signal stability analysis, frameworks to address control interactions, harmonics and arbitrary ac, dc, converter- or even SM-internal contingencies call for detailed EMT studies. Especially in the case of drastically more complex MMC-HVdc technology (in terms of number of power electronic switching devices) the choice of a meaningful modeling depth needs to reflect the underlying study purpose to reach a reasonable compromise between required accuracy and therewith related computational burden.

In [122], different modeling approaches have been clustered related to their suitability for circuit simulation, EMT, phasor domain or load flow studies. In total,

to one carrier. This potentially leads to significant cell voltage fluctuations and also highly unequal duty-cycles and is therefore directly skipped within this compilation.

five out of seven modeling approaches are considered appropriate for different EMT-type studies, as indicated and briefly commented in Table 2.3. Nevertheless, since the intended research purpose requires insights into converter-internal quantities like energetic states of converter arms and arm currents, aggregated models (*Type 5-6*) have to be discarded. Apart from that, very detailed representations of individual SMs (*Type 2-3*) exceed a reasonable computational effort as they massively increase the number of electrical nodes within the system.

Hence, a computationally more efficient but mathematically equivalent solution to represent a full SM stack (SM quantities labeled by subscript SM) by a two-node Thévenin – or rather solver-requested Norton equivalent – has been proposed in [23]. It is based on a SM representation treating IGBT switches and anti-parallel diodes as two state resistors (high and low impedance value R_{off} and R_{on}) like in a *Type 3* model, as depicted in Fig. 2.5, where only one device is conducting at a given instance. Using the trapezoidal integration method, the SM capacitor dynamics (quantities labeled by subscript C) during one simulation step can be

Table 2.3: Classification of converter arm modeling approaches according to [122].

classification	application	study purpose and remarks
Type 1	circuit simulation	detailed circuit simulations for design validation, focussing on individual or few stacked SMs, very high complexity
Type 2	EMT tools	suitable for SM-internal faults, based on simplified nonlinear IGBT and diode representations, access to individual SMs, high complexity
Type 3	EMT tools	suitable for SM-internal faults, based on two-value IGBT and diode representations, access to individual SMs, high complexity
Type 4	**EMT tools**	suitable for arbitrary faults except SM-internal contingencies, reduced equivalent circuit based on two-value IGBT and diode representations, remaining access to individual SM voltages, reduced complexity
Type 5	EMT tools	suitable for ac and dc transient studies, includes harmonic content, no access to individual SMs and converter-internal quantities, low complexity
Type 6	phasor domain / EMT tools	suitable for remote ac and dc transient studies, excludes harmonic content, no access to individual SMs and converter-internal quantities, very low complexity
Type 7	load flow calculation	suitable for steady-state studies only

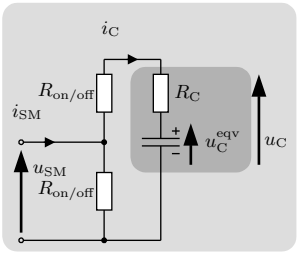

Figure 2.5: HB SM representation following [23].

expressed as

$$u_C(t) = \frac{1}{C_{SM}} \int i_C(t)\mathrm{d}t \approx u_C(t - \Delta T) + \frac{1}{C_{SM}} \left(\frac{i_C(t - \Delta T) + i_C(t)}{2} \right) \Delta T, \tag{2.1}$$

where ΔT corresponds to the simulation step width and C_{SM} is the SM capacitor size. By slightly reorganizing the term in eq. (2.1), this relation can be interpreted as an equivalent voltage source and a series-connected resistor according to

$$u_C(t) = R_C \cdot i_C(t) + u_C^{eqv}(t - \Delta T), \tag{2.2}$$

where

$$R_C = \frac{\Delta T}{2C_{SM}}$$

$$u_C^{eqv}(t - \Delta T) = \frac{\Delta T}{2C_{SM}} i_C(t - \Delta T) + u_C(t - \Delta T).$$

Note that R_C is solely related to the capacitance and the simulation step width, while u_C^{eqv} additionally depends on values of the last time step. Considering further the resistances R_{on} and R_{off}, where information of the recent state is required[5], individual and subsequently the full multi-valve representation is obtained following [23]. Thus, information related to individual SM capacitor voltages remains available.

Alternatively, accelerated SM stack models suitable for control design and dynamic investigations represented by a controllable voltage source have been proposed. While remaining access to aggregated SM quantities is provided [108], see also a related comparison provided in [9], this solution is typically utilized for converter control and energy-balancing studies, see [81, 82].

[5] While a SM is blocked a diode network remains, which imposes simulative challenges to determine the accurate status resulting in valid effective resistances within the electrical network. Depending on the utilized simulation tool, different strategies utilizing either interpolation or iterative techniques are further addressed in [106] and [84].

2.2 System Configurations

HVdc schemes can be realized in monopolar or bipolar configurations [121], while the selection is depending on various technical and non-technical aspects. Besides economic considerations (e.g. investment costs and system losses), regulatory requirements, planned future scheme or grid expansion capability, equipment ratings as well as environmental constraints like ground return (GR) currents may influence preferences. As visualized in Fig. 2.6, three main categories, namely asymmetric or symmetric monopolar and bipolar configuration, exist. Related to [121] and [52], the following overview is guided by associated feasibility investigations and a thorough forward-looking analysis and comparison of grounding conditions for potential dc networks, respectively.

Focussing on asymmetric monopolar schemes, a single high voltage pole conductor operating at full voltage rating is required. For the return path, either ground currents via electrodes or a single point grounded DMR are utilized, see Fig. 2.6 (a). As GR solutions are unlikely due to environmental constraints high DMR operation voltage requirements and associated withstand ratings are supposed to be avoided to account for economic reasons. Therefore, a solid grounding is commonly applied. Nevertheless, pole to ground faults lead to high steady-state fault currents, which have to be handled by appropriate hardware and protection design.

Turning the view towards symmetric monopolar schemes with high impedance grounding divergent characteristics are revealed. As typically indirect grounding is realized by a high impedance star point reactor like shown in Fig. 2.6 (b) or by high value resistive or capacitive grounding, steady-state fault currents are avoided. This relieves pressure on protection speed requirements and FCI capability to operate the system within feasible technical (current rating) boundaries. Also, the converter transformer has not to be designed to withstand permanent superimposed ac and dc voltage stresses. Assuming a need for a return conductor, initial investment difference between DMR for an asymmetric scheme and fully isolated cable for a symmetric scheme appears rather small (similar copper cross section and cable laying costs) and favour this type of configuration. Also, to achieve equal transmission capacity, an asymmetric monopole must be designed to withstand twice the rated voltage (to ground) compared to its symmetric monopolar counterpart.

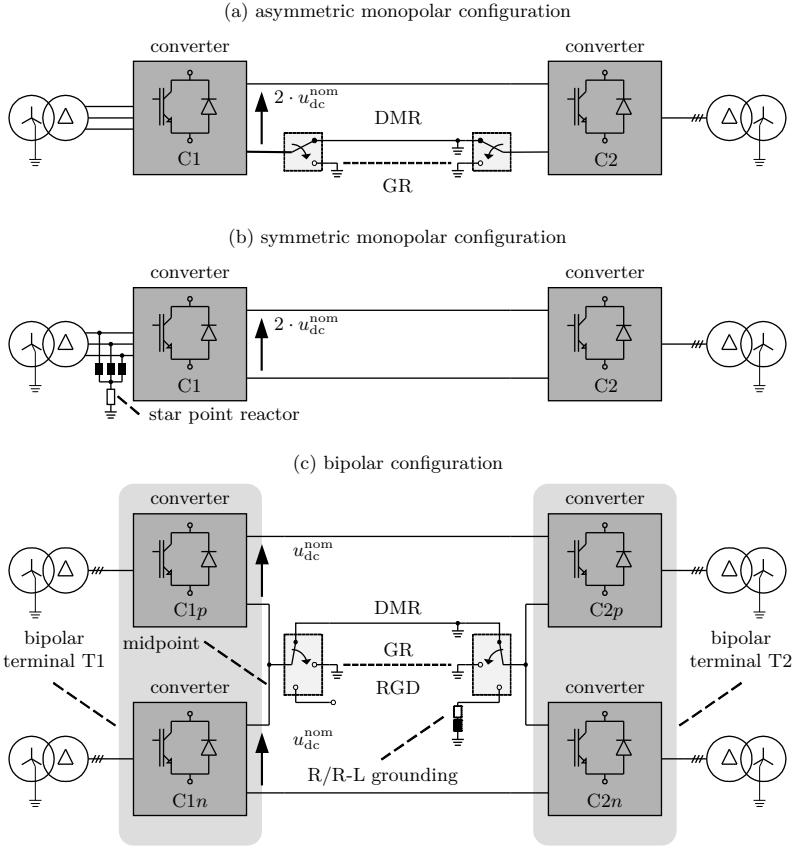

Figure 2.6: Overview of system configurations including terminal and converter labels as well as nominal pole to pole voltages: (a) asymmetric monopolar configuration, (b) symmetric monopolar configuration, (c) variants of the bipolar configuration.

This initially appears to contradict the need for bipolar HVdc solutions since asymmetric monopolar schemes represent the underlying core building block. However, to satisfy the need for bulk-power interconnectors, as for example proposed and approved in recent grid development plans [129] and [128] in Germany, HVdc schemes with increased power ratings and inherent redundancy or at least measures to mitigate permanent full power-loss during contingencies are required. Related to these changing prerequisites the following issues motivate utilization of partially redundant rigid (RGD) or even fully redundant bipolar schemes with GR or DMR, as shown in Fig. 2.6 (c):

- Due to the solid grounding in bipolar schemes, extensive equipment voltage ratings can be avoided as overvoltages are less severe compared to symmetric monopolar configurations.

- The RGD configuration presents a trade-off in terms of redundancy since a faulted converter can be bypassed assuming an appropriately designed dc switchyard. Nevertheless, permanent transmission line faults still lead to full system shut-down as a spare return conductor is absent. Therefore, this solution appears solely beneficial for schemes with full or a high share of cable transmission segments.

- To avoid full power loss during arbitrary contingencies two parallel links are required in case a symmetric monopolar configuration is selected. While this accounts for four fully isolated conductors bipolar links in DMR or GR configuration, consisting of two quasi-independent subsystems, reduce this number to three (two fully isolated conductors, one dedicated metallic return) or to two (two fully isolated conductors, one ground return), respectively. These types of implementations seem beneficial for schemes comprising a significant share of OHL to account for increasing fault likeliness.

Within Table 2.4, a summary of macroscopic characteristics related to the introduced bipolar configurations is compiled. As highlighted above, the corresponding choice impacts redundancy or rather the extent of power loss due to contingencies as well as environmental and economic aspects. Besides the typical grounding configurations listed, variations utilizing combinations of solid, low to mid-size impedance grounding or only surge protection of the terminal midpoint shown in Fig. 2.6 (c) by arrestors[6] can be applied with respect to the given technical requirements. As this significantly affects fault response and scheme-wide insulation coordination, a thorough analysis of the grounding concept is required.

[6]Floating terminal midpoint during normal operation, overvoltages clamped by surge arresters during contingencies.

Table 2.4: Overview of characteristics of different bipolar configurations.

bipolar configuration	RGD	GR	DMR
return conductor	×	(✓)	✓
dc current degrees of freedom	1	2	2
inherent redundancy	(✓)	✓	✓
redundancy related to dc line faults	×	✓	✓
redundancy related to converter faults	(✓)	✓	✓
grounding configuration (floating, low to mid-size impedance)	floating/low to mid-size	low/low	floating/low
midpoint voltage shift	✓	×	✓

2.3 Grid Code Requirements

MMC-HVdc schemes in general, but especially embedded bulk-power interconnectors, show a significant impact on regional load flows, system dynamics and ac grid stability. Therefore, in response to [125], a thorough set of connection rules and dynamic characteristics has to be specified by relevant (significantly affected) TSOs.

To assess the developed control, balancing, fault handling and protection framework within this thesis, the following key premises related to recently published *Technical requirements for grid connection of high-voltage direct current systems and direct current-connected power park modules* [114] are considered. The following list qualitatively summarizes most relevant aspects:

- The converter shall remain connected to the power grid during frequency deviations[7] within a range of 47 Hz to 52 Hz, where the maximum rate of change of frequency (ROCOF) stays below 2.5 Hz/s.
- Active power adjustments shall be achieved with respect to specified ramp rates. Adaption must be initiated within less than 100 ms or 10 ms after setpoint modification during normal or faulted conditions, respectively.
- The converter shall provide ride-through capabilities in the case of high or low ac voltages. Depending on fault type the converter may only disconnect if the highest or lowest ac phase-to-phase voltage violates specified voltage envelopes.

[7] The range has been split into several intervals with different minimum connection period requirements. As those exceed the duration of performed investigations they are not further considered.

- The converter shall provide a dynamic voltage response by injecting appropriate positive and negative sequence reactive currents. Their reference value is determined by the relative voltage drop multiplied by an injection gain between two and six. Currents shall be modified to limit deviations of positive and negative sequence compared to steady-state operation conditions (boost or suppress positive sequence voltage, suppress negative sequence voltage).

- Reactive current injection during faults shall be prioritized related to active current provision. Furthermore, the corresponding rise time shall stay below 30 ms until 90 % of the requested current level is reached, overshoots shall remain below 15 % and overall settling time shall be less than 60 ms.

- The converter output voltage shall follow quality requirements within a frequency range up to 5 kHz. If needed, additional active damping or conventional filter capabilities shall be provided.

- The converter shall be capable to provide additional control features like power oscillation damping, emergency power control, sub-synchronous oscillation damping as well as black start capability.

- The order of protection and control priorities shall follow: protection of power grid and HVdc system, sub-synchronous oscillation damping, dynamic voltage response, emergency power control, synthetic inertia provision, fulfillment of automatic response requirements, power oscillation damping, limited frequency sensitive mode at under-frequency, steady-state voltage control, limited frequency sensitive mode at over-frequency and limitation of power ramp-rates.

Chapter 3

Bipolar MMC-HVdc Controls and Balancing

3.1 Bipolar Terminal and Control Fundamentals

To pave the way towards the main part of this chapter, this section presents fundamentals related to bipolar HVdc and MMC controls.

According to the HVdc network expansion each bipolar terminal (identifier Tx), where x is an index numbered consecutively, consists of two series-connected MMCs. These are assigned to the upper/positive or lower/negative subsystem (Cxs), with $s \in \{p, n\}$ as shown in Fig. 3.1. Due to the presence of a DMR, dc quantity controls of upper (Cxp) and lower (Cxn) converter are fully independent and enable asymmetric bipolar operation. Since (single point) grounding at a distant terminal is implied to obtain the most generalized case, the intermediate busbar – called midpoint – must be designed to handle rated current and withstand associated maximum voltage offsets related to the grounding position and occurring transients. As usual for HVdc applications, a wye-delta transformer decouples zero-sequence current propagation towards the HVac grid.

3.1.1 Three-Phase Equivalent Circuit

To perform circuit analysis and derive basic single- and three-phase relations, a detailed equivalent circuit is provided within Fig. 3.2. Quantities related to the upper subsystem C1p of investigated Terminal T1 and quantities related to the dc-side are named explicitly.

Starting from the ac-side, each subsystem is connected to the three-phase network ($y \in \{a, b, c\}$) at the PCC, where quantities are tagged accordingly (subscript

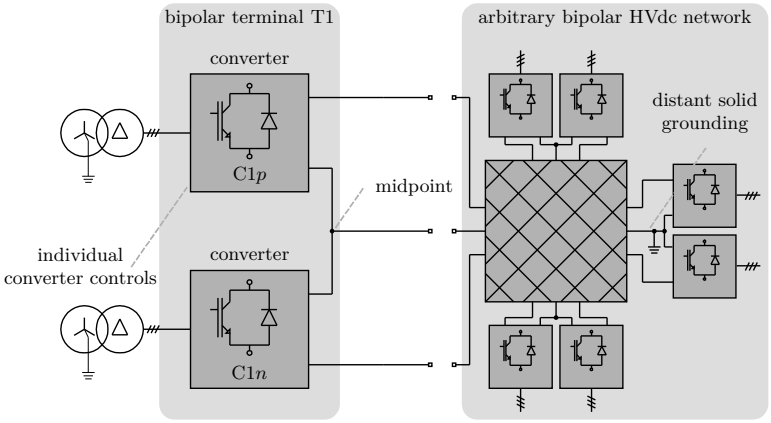

Figure 3.1: Schematic of an arbitrary bipolar HVdc network.

PCC). As grid voltages typically differ from required levels at the converter-side, the adjacent transformer exhibits a non-unity transmission ratio and a phase shift related to its vector group. This implies that it is required to measure and monitor a second set of quantities (subscript conv), where related currents can be directly linked to converter-internal stresses. Furthermore, due to the bipolar configuration, voltages on the converter-side consist of an alternating part but also imply an offset approximately half of the dc pole to ground voltage under steady-state conditions. Turning the view towards the converter, SM stacks and series connected inductors represent the six converter arms and are split into an upper/positive and lower/negative group to enable an unequivocal marking (subscript s,y). This is further supplemented by inflowing busbar currents (subscript dc$s$) and the converter-side dc voltage (subscript dc) mainly relevant for control purposes. Proceeding to the dc-side, a differentiation between converter-near voltages (subscript conv,dc$s$/DMR) and voltages beyond the dc smoothing inductor and HVdc switch (subscript line,dc$s$/DMR) is made to differentiate between stresses affecting insulation coordination of converters or the transmission scheme. Further, to clearly assign incoming fault current traveling waves to one bipolar subsystem for fault classification purposes, terminal currents on the transmission side of the dc inductor (superscript Tx, subscript dc$s$/DMR) are monitored. For the sake of completeness, aspects related to protection zone definitions and surge arrestor placement, which will be addressed in-depth in the following chapters, are indicated.

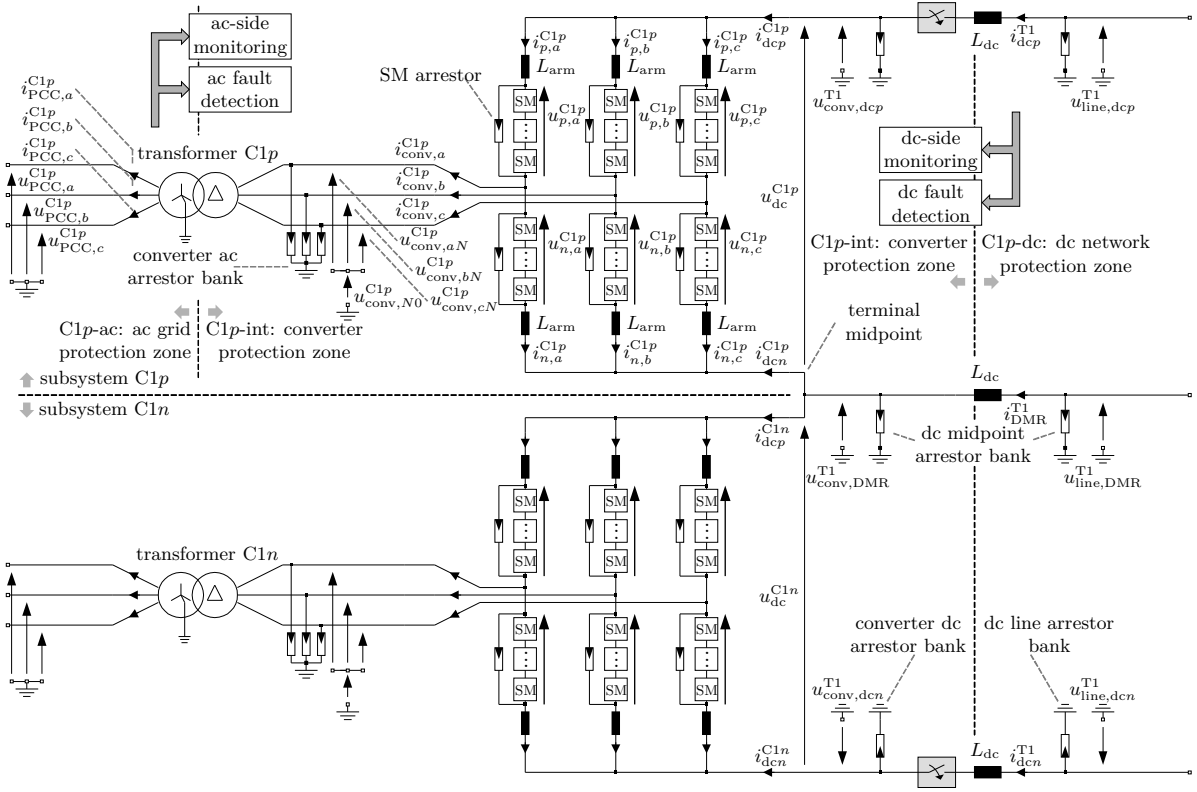

Figure 3.2: MMC three-phase equivalent circuit in bipolar configuration connected to an arbitrary dc network.

3.1.2 Single-Phase Relations

To derive basic relations for a converter within a bipolar MMC-HVdc terminal according to the equivalent circuit shown in Fig. 3.2, single-phase relations for converter C1p are analyzed. Neglecting ac- and dc-side grid connection, this leads to

$$u_{\mathrm{conv},N0}^{\mathrm{C1}p} + u_{\mathrm{conv},yN}^{\mathrm{C1}p} + u_{p,y}^{\mathrm{C1}p} + i_{p,y}^{\mathrm{C1}p} \cdot R_{\mathrm{arm}} + \dot{i}_{p,y}^{\mathrm{C1}p} \cdot L_{\mathrm{arm}} - u_{\mathrm{dc}}^{\mathrm{C1}p} - u_{\mathrm{conv,DMR}}^{\mathrm{T1}} = 0 \tag{3.1}$$

and

$$u_{\mathrm{conv},N0}^{\mathrm{C1}p} + u_{\mathrm{conv},yN}^{\mathrm{C1}p} - u_{n,y}^{\mathrm{C1}p} - i_{n,y}^{\mathrm{C1}p} \cdot R_{\mathrm{arm}} - \dot{i}_{n,y}^{\mathrm{C1}p} \cdot L_{\mathrm{arm}} - u_{\mathrm{conv,DMR}}^{\mathrm{T1}} = 0. \tag{3.2}$$

Here, L_{arm} represents the arm inductor and R_{arm} aggregates parasitic ohmic components related to the arm inductor, SM stacks (semiconductors and capacitors) as well as connecting lines and busbars. This element is not explicitly shown within the equivalent circuit. Assuming equal distribution of $i_{\mathrm{conv},y}^{\mathrm{C1}p}$ among the upper and lower arms and considering the relation

$$i_{\mathrm{conv},y}^{\mathrm{C1}p} = i_{p,y}^{\mathrm{C1}p} - i_{n,y}^{\mathrm{C1}p}, \tag{3.3}$$

a phase-module current (subscript phm)

$$i_{\mathrm{phm},y}^{\mathrm{C1}p} = \frac{i_{p,y}^{\mathrm{C1}p} + i_{n,y}^{\mathrm{C1}p}}{2} \tag{3.4}$$

can be introduced. Calculating difference and sum according to eq. $[(3.1)\mp(3.2)]/2$, the basic control principle for decoupled ac- and dc-side current control related to decoupled voltages $u_{\Sigma,y}^{\mathrm{C1}p}$ and $u_{\Delta,y}^{\mathrm{C1}p}$ with eliminated current system interdependencies

$$u_{\Sigma,y}^{\mathrm{C1}p} = \frac{u_{p,y}^{\mathrm{C1}p} + u_{n,y}^{\mathrm{C1}p}}{2} = -i_{\mathrm{phm},y}^{\mathrm{C1}p} \cdot R_{\mathrm{arm}} - \dot{i}_{\mathrm{phm},y}^{\mathrm{C1}p} \cdot L_{\mathrm{arm}} + \frac{u_{\mathrm{dc}}^{\mathrm{C1}p}}{2} \tag{3.5}$$

and

$$u_{\Delta,y}^{\mathrm{C1}p} = \frac{u_{n,y}^{\mathrm{C1}p} - u_{p,y}^{\mathrm{C1}p}}{2} = +i_{\mathrm{conv},y}^{\mathrm{C1}p} \cdot \frac{R_{\mathrm{arm}}}{2} + \dot{i}_{\mathrm{conv},y}^{\mathrm{C1}p} \cdot \frac{L_{\mathrm{arm}}}{2} + u_{\mathrm{conv},yN}^{\mathrm{C1}p} + Offset \tag{3.6}$$

becomes apparent, see also [42, 30]. The highlighted remaining offset incorporates $u_{\mathrm{conv},N0}^{\mathrm{C1}p}$, $u_{\mathrm{dc}}^{\mathrm{C1}p}/2$ and $u_{\mathrm{conv,DMR}}^{\mathrm{T1}}$, but has no direct control impact as it is equal for all three phases and the transformer setting (wye-delta) suppresses direct current propagation towards the ac-side.

3.1.3 Three-Phase Relations in $\alpha\beta 0$-frame

The previous section unveiled the basic concept of decoupled current systems in MMCs by introducing $u_{\Sigma,y}$ and $u_{\Delta,y}$. In light of the underlying power system application context, this relation is extended towards a generalized three-phase representation resulting in

$$\begin{bmatrix} u_{\Sigma,a} \\ u_{\Sigma,b} \\ u_{\Sigma,c} \end{bmatrix} = \begin{bmatrix} -i_{\mathrm{phm},a} \cdot R_{\mathrm{arm}} - \dot{i}_{\mathrm{phm},a} \cdot L_{\mathrm{arm}} + \frac{u_{\mathrm{dc}}}{2} \\ -i_{\mathrm{phm},b} \cdot R_{\mathrm{arm}} - \dot{i}_{\mathrm{phm},b} \cdot L_{\mathrm{arm}} + \frac{u_{\mathrm{dc}}}{2} \\ -i_{\mathrm{phm},c} \cdot R_{\mathrm{arm}} - \dot{i}_{\mathrm{phm},c} \cdot L_{\mathrm{arm}} + \frac{u_{\mathrm{dc}}}{2} \end{bmatrix} \tag{3.7}$$

and

$$\begin{bmatrix} u_{\Delta,a} \\ u_{\Delta,b} \\ u_{\Delta,c} \end{bmatrix} = \begin{bmatrix} +i_{\mathrm{conv},a} \cdot \frac{R_{\mathrm{arm}}}{2} + \dot{i}_{\mathrm{conv},a} \cdot \frac{L_{\mathrm{arm}}}{2} + u_{\mathrm{conv},aN} \\ +i_{\mathrm{conv},b} \cdot \frac{R_{\mathrm{arm}}}{2} + \dot{i}_{\mathrm{conv},b} \cdot \frac{L_{\mathrm{arm}}}{2} + u_{\mathrm{conv},bN} \\ +i_{\mathrm{conv},c} \cdot \frac{R_{\mathrm{arm}}}{2} + \dot{i}_{\mathrm{conv},c} \cdot \frac{L_{\mathrm{arm}}}{2} + u_{\mathrm{conv},cN} \end{bmatrix}. \tag{3.8}$$

Typically, to obtain linear independent quantities for control development, voltages and currents are transformed into orthogonal stationary $\alpha\beta 0$-frame utilizing

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = \boldsymbol{T}^{abc \to \alpha\beta 0} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{3.9}$$

as specified according to *IEC 62428:2008* within Appendix A. This leads to

$$\begin{bmatrix} u_{\Sigma,\alpha} \\ u_{\Sigma,\beta} \\ u_{\Sigma,0} \end{bmatrix} = \begin{bmatrix} -i_{\mathrm{phm},\alpha} \cdot R_{\mathrm{arm}} - \dot{i}_{\mathrm{phm},\alpha} \cdot L_{\mathrm{arm}} \\ -i_{\mathrm{phm},\beta} \cdot R_{\mathrm{arm}} - \dot{i}_{\mathrm{phm},\beta} \cdot L_{\mathrm{arm}} \\ -i_{\mathrm{phm},0} \cdot R_{\mathrm{arm}} - \dot{i}_{\mathrm{phm},0} \cdot L_{\mathrm{arm}} + \frac{u_{\mathrm{dc}}}{2} \end{bmatrix} \tag{3.10}$$

and

$$\begin{bmatrix} u_{\Delta,\alpha} \\ u_{\Delta,\beta} \end{bmatrix} = \begin{bmatrix} +i_{\mathrm{conv},\alpha} \cdot \frac{R_{\mathrm{arm}}}{2} + \dot{i}_{\mathrm{conv},\alpha} \cdot \frac{L_{\mathrm{arm}}}{2} + u_{\mathrm{conv},\alpha} \\ +i_{\mathrm{conv},\beta} \cdot \frac{R_{\mathrm{arm}}}{2} + \dot{i}_{\mathrm{conv},\beta} \cdot \frac{L_{\mathrm{arm}}}{2} + u_{\mathrm{conv},\beta} \end{bmatrix}. \tag{3.11}$$

Again, due to the selected transformer configuration, no zero-sequence component $i_{\mathrm{conv},0}$ can propagate towards the ac-side. This reduces the number of degrees of freedom from six to five independently adjustable currents.

3.1.4 Equivalent Circuit in $\alpha\beta 0$-frame

Within Fig. 3.3 the performed decomposition according to eq. (3.10) and (3.11) is visualized. Even though the previous analysis neglected ac and dc peripheral equipment and interconnecting lines, distant sources connected by an arbitrary impedance are indicated since these are later on respected during control development. Inspecting the result, it is obvious that five linear independent and

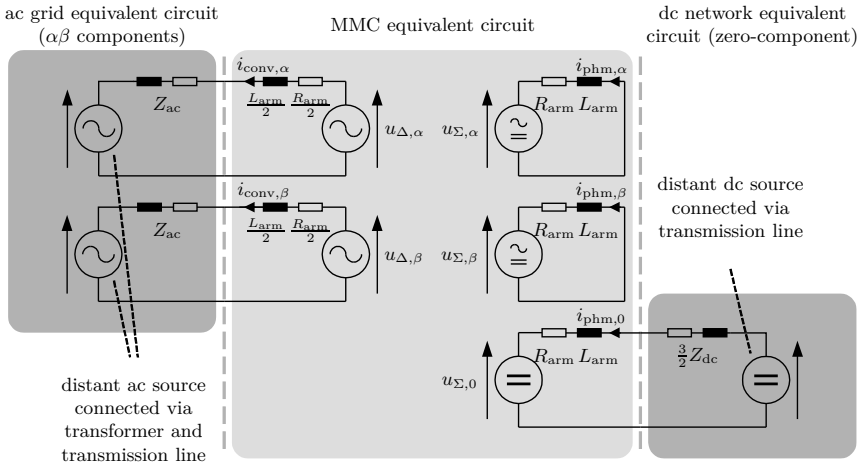

Figure 3.3: MMC equivalent circuit in $\alpha\beta 0$-frame connected to arbitrary ac and dc networks represented by Z_{ac} and Z_{dc} [16].

therefore fully decoupled subsystems exist. This comprises two currents $i_{\mathrm{conv},\alpha/\beta}$ to manipulate the ac output, two inner currents $i_{\mathrm{phm},\alpha/\beta}$ without any impact on external quantities and a zero-sequence current $i_{\mathrm{phm},0}$ to adjust the current at the dc-side of the converter. Assuming balanced operation conditions, the relation between $i_{\mathrm{phm},0}$ and mapped dc-side currents of C1p corresponds to

$$i_{\mathrm{phm},0} = \frac{1}{3} i_{\mathrm{dc}p} = -\frac{1}{3} i_{\mathrm{dc}n}. \tag{3.12}$$

3.1.5 Arm Reference Voltages

Quantities are segmented further within this section to obtain insights related to individual arm output voltages. Reminiscing the fact that

$$\boldsymbol{T}^{abc\to\alpha\beta 0} \begin{bmatrix} a_a + b_a \\ a_b + b_b \\ a_c + b_c \end{bmatrix} = \boldsymbol{T}^{abc\to\alpha\beta 0} \begin{bmatrix} a_a \\ a_b \\ a_c \end{bmatrix} + \boldsymbol{T}^{abc\to\alpha\beta 0} \begin{bmatrix} b_a \\ b_b \\ b_c \end{bmatrix}, \tag{3.13}$$

introduced voltage components in $\alpha\beta 0$-frame can be rewritten as follows:

$$u_{\Sigma,\alpha/\beta/0} = \frac{u_{p,\alpha/\beta/0} + u_{n,\alpha/\beta/0}}{2}, u_{\Delta,\alpha/\beta} = \frac{u_{n,\alpha/\beta} - u_{p,\alpha/\beta}}{2}. \tag{3.14}$$

Utilizing this manipulation and calculating difference and sum with respect to eq. (3.10) and eq. (3.11), this leads to

$$\begin{bmatrix} u_{p,\alpha} \\ u_{p,\beta} \\ u_{p,0} \end{bmatrix} = \begin{bmatrix} u_{\Sigma,\alpha} - u_{\Delta,\alpha} \\ u_{\Sigma,\beta} - u_{\Delta,\beta} \\ u_{\Sigma,0} \end{bmatrix}, \begin{bmatrix} u_{n,\alpha} \\ u_{n,\beta} \\ u_{n,0} \end{bmatrix} = \begin{bmatrix} u_{\Sigma,\alpha} + u_{\Delta,\alpha} \\ u_{\Sigma,\beta} + u_{\Delta,\beta} \\ u_{\Sigma,0} \end{bmatrix}. \tag{3.15}$$

Transforming expressions back into *abc*-frame by means of

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \boldsymbol{T}^{\alpha\beta 0 \rightarrow abc} \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} \tag{3.16}$$

given in Appendix A.1, individual arm voltage reference values transferred to the final modulation layer are obtained:

$$\begin{bmatrix} u_{p,a} \\ u_{p,b} \\ u_{p,c} \end{bmatrix} = \begin{bmatrix} u_{\Sigma,a} - u_{\Delta,a} \\ u_{\Sigma,b} - u_{\Delta,b} \\ u_{\Sigma,c} - u_{\Delta,c} \end{bmatrix}, \begin{bmatrix} u_{n,a} \\ u_{n,b} \\ u_{n,c} \end{bmatrix} = \begin{bmatrix} u_{\Sigma,a} + u_{\Delta,a} \\ u_{\Sigma,b} + u_{\Delta,b} \\ u_{\Sigma,c} + u_{\Delta,c} \end{bmatrix}. \tag{3.17}$$

3.2 Energetic Relations and Instantaneous Arm Power

While the previous section deduced fundamental relations with respect to current control possibilities and highlighted decoupling of linear independent subsystems, this section evaluates energy-related fundamentals and instantaneous arm powers. In a comparable manner, evaluation of an arm or rather a phase-module is extended towards a comprehensive representation including suitable decomposition into transformed components. Subsequently, possibilities related to targeted energy-balancing under balanced and unbalanced grid conditions are identified.

3.2.1 Energetic Relations in $\alpha\beta 0$-frame

The total energy content stored within a single converter arm is defined by the sum of SM energy contents and can be written as

$$E_{s,y} = \frac{1}{2} \cdot C_{\mathrm{SM}} \cdot \sum_{i=1}^{m} \left(u_{s,y}^{i}\right)^2, \tag{3.18}$$

where m is the number of SMs per arm, C_{SM} the cell capacitor and $u_{s,y}^{i}$ the corresponding voltage of the i-th cell. Presupposing appropriate intra-arm voltage balancing[1], where $u_{s,y}^{\mathrm{avg}}$ represents an averaged SM charging status, the sum voltage

[1] It is not intended to control arm-internal imbalance between single SMs by means of energy-balancing controls. Instead, intra-arm balancing is realized by appropriate sorting strategies/logics, which are supposed to level out deviations.

can be approximated by

$$u_{s,y}^{\Sigma} = \sum_{i=1}^{m} \left(u_{s,y}^{i}\right) \approx m \cdot u_{s,y}^{\text{avg}}. \tag{3.19}$$

Utilizing this relation, eq. (3.18) can be reformulated according to [31] as

$$E_{s,y} = \frac{1}{2} \cdot \frac{C_{\text{SM}}}{m} \cdot (u_{s,y}^{\Sigma})^2. \tag{3.20}$$

Introducing again sigma and delta components

$$E_{\Sigma,y} = \frac{1}{2}\left(E_{p,y} + E_{n,y}\right), \qquad E_{\Delta,y} = E_{p,y} - E_{n,y} \tag{3.21}$$

to obtain linear independent quantities, this leads to a set of relations in $\alpha\beta 0$-frame as follows:

$$\begin{bmatrix} E_{\Sigma,\alpha} \\ E_{\Sigma,\beta} \\ E_{\Sigma,0} \end{bmatrix} = \frac{1}{2} \cdot \boldsymbol{T}^{abc\rightarrow\alpha\beta 0} \begin{bmatrix} E_{p,a} + E_{n,a} \\ E_{p,b} + E_{n,b} \\ E_{p,c} + E_{n,c} \end{bmatrix} \tag{3.22}$$

and

$$\begin{bmatrix} E_{\Delta,\alpha} \\ E_{\Delta,\beta} \\ E_{\Delta,0} \end{bmatrix} = \boldsymbol{T}^{abc\rightarrow\alpha\beta 0} \begin{bmatrix} E_{p,a} - E_{n,a} \\ E_{p,b} - E_{n,b} \\ E_{p,c} - E_{n,c} \end{bmatrix}. \tag{3.23}$$

The converter is within a balanced state if all components (filtered by appropriate measures to suppress fluctuating superimposed shares), except $E_{\Sigma,0}$, equal zero. In the case of $E_{\Sigma,0}$, the appropriate reference value needs to be derived based on the desired average SM stack charging voltage $u_{\Sigma,0}^{\Sigma,\text{ref}}$ equal for all arms according to

$$E_{\Sigma,0}^{\text{ref}} = \frac{1}{2} \cdot \frac{C_{\text{SM}}}{m} \cdot (u_{\Sigma,0}^{\Sigma,\text{ref}})^2. \tag{3.24}$$

3.2.2 Instantaneous Arm Power in Steady-State

The instantaneous power of an arbitrary converter arm $p_{s,y}$ corresponds to the derivative of the energy content $\dot{E}_{s,y}$ and is expressed as

$$p_{s,y} = \dot{E}_{s,y} = u_{s,y} \cdot i_{s,y}, \tag{3.25}$$

where $u_{s,y}$ can be replaced by the appropriate relation given in eq. (3.17). Additionally, $i_{s,y}$ comprises $i_{\text{phm},y}$ consisting of a dc component as well as initially neglected inner current components for balancing purposes and – assuming non-saturated arm inductors [42] – the ac currents of the converter $i_{\text{conv},y}$ are equally distributed among upper and lower arms.

Analyzing a single phase-module y of converter C1p, this results in

$$p_{p,y} = \dot{E}_{p,y} = (u_{\Sigma,y} - u_{\Delta,y}) \cdot \left(i_{\mathrm{phm},y} + \frac{1}{2} i_{\mathrm{conv},y} \right) \tag{3.26}$$

and

$$p_{n,y} = \dot{E}_{n,y} = (u_{\Sigma,y} + u_{\Delta,y}) \cdot \left(i_{\mathrm{phm},y} - \frac{1}{2} i_{\mathrm{conv},y} \right). \tag{3.27}$$

Reviewing eq. (3.7) and eq. (3.8), under the assumption that resistive and inductive voltage drops are relatively small in relation to the remaining voltage components, the relations $u_{\Sigma,y} \approx \frac{1}{2} u_{dc}$ and $u_{\Delta,y} \approx u_{\mathrm{conv},yN}$ become apparent. Furthermore, $i_{\mathrm{phm},y}$ is constant while $i_{\mathrm{conv},y}$ solely contains fundamental grid frequency components in steady-state operation. Performing above stated multiplications, this leads to

$$\begin{aligned} p_{p,y} = \dot{E}_{p,y} = u_{\Sigma,y} \cdot i_{\mathrm{phm},y} - \frac{1}{2} u_{\Delta,y} \cdot i_{\mathrm{conv},y} \\ + \frac{1}{2} u_{\Sigma,y} \cdot i_{\mathrm{conv},y} - u_{\Delta,y} \cdot i_{\mathrm{phm},y} \end{aligned} \tag{3.28}$$

and

$$\begin{aligned} p_{n,y} = \dot{E}_{n,y} = u_{\Sigma,y} \cdot i_{\mathrm{phm},y} - \frac{1}{2} u_{\Delta,y} \cdot i_{\mathrm{conv},y} \\ - \frac{1}{2} u_{\Sigma,y} \cdot i_{\mathrm{conv},y} + u_{\Delta,y} \cdot i_{\mathrm{phm},y}. \end{aligned} \tag{3.29}$$

Following the presented order, individual terms can be characterized in detail as highlighted within Table 3.1, if no additional internal currents are required for balancing purposes. Here, ω represents the grid angular frequency.

Table 3.1: Composition of instantaneous arm powers in steady-state.

term	main impact	composition during steady-state operation
$u_{\Sigma,y} \cdot i_{\mathrm{phm},y}$	dc-side power exchange	$p = const$
$\frac{1}{2} u_{\Delta,y} \cdot i_{\mathrm{conv},y}$	ac-side power exchange	$p = const + f(2\omega)$
$\frac{1}{2} u_{\Sigma,y} \cdot i_{\mathrm{conv},y}$	oscillating power component	$p = f(\omega)$
$u_{\Delta,y} \cdot i_{\mathrm{phm},y}$	oscillating power component	$p = f(\omega)$

By defining

$$p_{\Sigma,y} = \frac{1}{2} \cdot (p_{p,y} + p_{n,y}), \qquad p_{\Delta,y} = p_{p,y} - p_{n,y}, \tag{3.30}$$

a direct link between instantaneous arm powers and energetic deviations following the calculation of eq. [(3.28)±(3.29)]/2 can be established. This leads to

$$p_{\Sigma,y} = \dot{E}_{\Sigma,y} = u_{\Sigma,y} \cdot i_{\mathrm{phm},y} - \frac{1}{2} u_{\Delta,y} \cdot i_{\mathrm{conv},y} \tag{3.31}$$

and

$$p_{\Delta,y} = \dot{E}_{\Delta,y} = u_{\Sigma,y} \cdot i_{\mathrm{conv},y} - 2 \cdot u_{\Delta,y} \cdot i_{\mathrm{phm},y}, \tag{3.32}$$

which results in

$$\begin{bmatrix} p_{\Sigma,\alpha} \\ p_{\Sigma,\beta} \\ p_{\Sigma,0} \end{bmatrix} = \begin{bmatrix} \dot{E}_{\Sigma,\alpha} \\ \dot{E}_{\Sigma,\beta} \\ \dot{E}_{\Sigma,0} \end{bmatrix} = \frac{1}{2} \boldsymbol{T}^{abc \to \alpha\beta 0} \begin{bmatrix} p_{p,a} + p_{n,a} \\ p_{p,b} + p_{n,b} \\ p_{p,c} + p_{n,c} \end{bmatrix} \tag{3.33}$$

and

$$\begin{bmatrix} p_{\Delta,\alpha} \\ p_{\Delta,\beta} \\ p_{\Delta,0} \end{bmatrix} = \begin{bmatrix} \dot{E}_{\Delta,\alpha} \\ \dot{E}_{\Delta,\beta} \\ \dot{E}_{\Delta,0} \end{bmatrix} = \boldsymbol{T}^{abc \to \alpha\beta 0} \begin{bmatrix} p_{p,a} - p_{n,a} \\ p_{p,b} - p_{n,b} \\ p_{p,c} - p_{n,c} \end{bmatrix} \tag{3.34}$$

in $\alpha\beta 0$-frame.

3.2.3 Unbalanced Conditions

Under unbalanced grid conditions, converter voltages and currents comprise positive and negative sequence components. As the transformer blocks the zero-sequence component it is discarded in this section. Following the definition in [119] and assuming equal quantity amplitudes in each phase, voltages are expressed by

$$\begin{aligned} u_{\mathrm{conv},aN} &= \hat{u}^{+1}_{\mathrm{conv}} \cdot \sin(\omega t + \vartheta^{+1}) + \hat{u}^{-1}_{\mathrm{conv}} \cdot \sin(\omega t + \vartheta^{-1}) \\ u_{\mathrm{conv},bN} &= \hat{u}^{+1}_{\mathrm{conv}} \cdot \sin(\omega t - \frac{2}{3}\pi + \vartheta^{+1}) + \hat{u}^{-1}_{\mathrm{conv}} \cdot \sin(\omega t + \frac{2}{3}\pi + \vartheta^{-1}) \\ u_{\mathrm{conv},cN} &= \hat{u}^{+1}_{\mathrm{conv}} \cdot \sin(\omega t + \frac{2}{3}\pi + \vartheta^{+1}) + \hat{u}^{-1}_{\mathrm{conv}} \cdot \sin(\omega t - \frac{2}{3}\pi + \vartheta^{-1}), \end{aligned} \tag{3.35}$$

whereas the currents correspond to

$$\begin{aligned} i_{\mathrm{conv},a} &= \hat{i}^{+1}_{\mathrm{conv}} \cdot \sin(\omega t + \varphi^{+1}) + \hat{i}^{-1}_{\mathrm{conv}} \cdot \sin(\omega t + \varphi^{-1}) \\ i_{\mathrm{conv},b} &= \hat{i}^{+1}_{\mathrm{conv}} \cdot \sin(\omega t - \frac{2}{3}\pi + \varphi^{+1}) + \hat{i}^{-1}_{\mathrm{conv}} \cdot \sin(\omega t + \frac{2}{3}\pi + \varphi^{-1}) \\ i_{\mathrm{conv},c} &= \hat{i}^{+1}_{\mathrm{conv}} \cdot \sin(\omega t + \frac{2}{3}\pi + \varphi^{+1}) + \hat{i}^{-1}_{\mathrm{conv}} \cdot \sin(\omega t - \frac{2}{3}\pi + \varphi^{-1}). \end{aligned} \tag{3.36}$$

Here, $\hat{u}_{\text{conv}}^{\pm 1}$ and $\hat{i}_{\text{conv}}^{\pm 1}$ are the positive/negative sequence ac voltage and ac current amplitudes, respectively. Further, ω represents the grid angular frequency and $\vartheta^{\pm 1}$ as well as $\varphi^{\pm 1}$ describe phase shifts.

Converting eq. (3.35) and eq. (3.36) into stationary $\alpha\beta$-frame, the following arm voltage (neglecting additional voltage drops)

$$\begin{aligned} u_{\text{conv},\alpha} &= +u_{\text{conv},\alpha}^{+1} + u_{\text{conv},\alpha}^{-1} \\ &= +\hat{u}_{\text{conv}}^{+1} \cdot \sin\left(+\omega t + \vartheta^{+1}\right) + \hat{u}_{\text{conv}}^{-1} \cdot \sin\left(+\omega t + \vartheta^{-1}\right) \end{aligned} \tag{3.37}$$

$$\begin{aligned} u_{\text{conv},\beta} &= +u_{\text{conv},\beta}^{+1} + u_{\text{conv},\beta}^{-1} \\ &= -\hat{u}_{\text{conv}}^{+1} \cdot \cos\left(+\omega t + \vartheta^{+1}\right) + \hat{u}_{\text{conv}}^{-1} \cdot \cos\left(+\omega t + \vartheta^{-1}\right), \end{aligned} \tag{3.38}$$

and current components

$$\begin{aligned} i_{\text{conv},\alpha} &= +i_{\text{conv},\alpha}^{+1} + i_{\text{conv},\alpha}^{-1} \\ &= +\hat{i}_{\text{conv}}^{+1} \cdot \sin\left(+\omega t + \varphi^{+1}\right) + \hat{i}_{\text{conv}}^{-1} \cdot \sin\left(+\omega t + \varphi^{-1}\right) \end{aligned} \tag{3.39}$$

$$\begin{aligned} i_{\text{conv},\beta} &= +i_{\text{conv},\beta}^{+1} + i_{\text{conv},\beta}^{-1} \\ &= -\hat{i}_{\text{conv}}^{+1} \cdot \cos\left(+\omega t + \varphi^{+1}\right) + \hat{i}_{\text{conv}}^{-1} \cdot \cos\left(+\omega t + \varphi^{-1}\right) \end{aligned} \tag{3.40}$$

result.

3.2.4 Instantaneous Arm Powers Under Unbalanced Conditions

Remembering that $p_{s,y} = \dot{E}_{s,y}$, the direct impact of instantaneous power component deviations on energetic changes arises based on the integral relation

$$E_{s,y}(t) = \int_0^t p_{s,y}(\tau)\mathrm{d}\tau + E_{s,y}(0). \tag{3.41}$$

Following further the definition given in [119], where instantaneous arm powers are separated into an average and oscillating component

$$p_{s,y} = \bar{p}_{s,y} + \tilde{p}_{s,y} = \dot{\bar{E}}_{s,y} + \dot{\tilde{E}}_{s,y}, \tag{3.42}$$

obtained non-fluctuating power components $\bar{p}_{s,y} = \dot{\bar{E}}_{s,y}$ or rather the transformed relations indicate theoretically available balancing possibilities[2]. Inserting the expressions stated in eq. (3.37) to (3.40) into eq. (3.33) and (3.34), see [47] as well as Appendix B for further details and supplementary maths, the resulting relations unveil possibilities to modify energetic quantities by adjusting corresponding power components. This requires internal converter currents – which

[2] The following mathematical derivation implies ideal suppression of intrinsically present instantaneous power or rather energy fluctuations within an MMC. Implementation details related to filter types and design are provided later in the course of this thesis.

are independently controllable and do neither affect power exchange on the ac- nor dc-side of the MMC – are appropriately selected to generate non-fluctuating power terms. With respect to the present dc as well as positive and negative sequence ac voltages introduced in section 3.2.3 converter-internal currents shall be composed of dc ($i^{\mathrm{dc}}_{\mathrm{phm},\alpha/\beta}$), see Appendix C, and individual sequence current components ($i^{\pm 1}_{\mathrm{phm},\alpha/\beta}$)

$$\begin{bmatrix} i_{\mathrm{phm},\alpha} \\ i_{\mathrm{phm},\beta} \end{bmatrix} = \begin{bmatrix} i^{\mathrm{dc}}_{\mathrm{phm},\alpha} + i^{+1}_{\mathrm{phm},\alpha} + i^{-1}_{\mathrm{phm},\alpha} \\ i^{\mathrm{dc}}_{\mathrm{phm},\beta} + i^{+1}_{\mathrm{phm},\beta} + i^{-1}_{\mathrm{phm},\beta} \end{bmatrix}. \tag{3.43}$$

To exclude inappropriate methods, the following evaluation names and briefly characterizes the range of suitable measures for HVdc applications.

Total Energy-Balancing

The average energy drift $\bar{p}_{\Sigma,0} = \dot{\bar{E}}_{\Sigma,0}$ of a converter, which is affecting all arms and their corresponding SM charging status in an equal manner, changes in the case of an imbalance between ac- and dc-side power exchange. Therefore, three possibilities exist under unbalanced conditions to return the system into a steady-state. Within Table 3.2, the obtained expression

$$\begin{aligned} \bar{p}_{\Sigma,0} = \underbrace{u_{\Sigma,0} i_{\mathrm{phm},0}}_{TOT\text{-}A} \underbrace{-\frac{1}{4}\left(u^{+1}_{\Delta,\alpha} i^{+1}_{\mathrm{conv},\alpha} + u^{+1}_{\Delta,\beta} i^{+1}_{\mathrm{conv},\beta}\right)}_{TOT\text{-}B} \\ \underbrace{-\frac{1}{4}\left(u^{-1}_{\Delta,\alpha} i^{-1}_{\mathrm{conv},\alpha} + u^{-1}_{\Delta,\beta} i^{-1}_{\mathrm{conv},\beta}\right)}_{TOT\text{-}C} \end{aligned} \tag{3.44}$$

is term-wise interpreted according to general suitability of individual parts.

Horizontal Energy-Balancing

A horizontal imbalance between the three phase-modules mainly occurs in the case of contingencies. Inspecting

$$\begin{aligned} \bar{p}_{\Sigma,\alpha} = \underbrace{u_{\Sigma,0} i^{\mathrm{dc}}_{\mathrm{phm},\alpha}}_{HOR\text{-}A} \underbrace{-\frac{1}{4} u^{+1}_{\Delta,\alpha} i^{-1}_{\mathrm{conv},\alpha} + \frac{1}{4} u^{+1}_{\Delta,\beta} i^{-1}_{\mathrm{conv},\beta}}_{HOR\text{-}B} \\ \underbrace{-\frac{1}{4} u^{-1}_{\Delta,\alpha} i^{+1}_{\mathrm{conv},\alpha} + \frac{1}{4} u^{-1}_{\Delta,\beta} i^{+1}_{\mathrm{conv},\beta}}_{HOR\text{-}C} \end{aligned} \tag{3.45}$$

and

$$\bar{p}_{\Sigma,\beta} = \underbrace{u_{\Sigma,0} i^{\mathrm{dc}}_{\mathrm{phm},\beta}}_{HOR\text{-}A} + \underbrace{\frac{1}{4} u^{+1}_{\Delta,\alpha} i^{-1}_{\mathrm{conv},\beta} + \frac{1}{4} u^{+1}_{\Delta,\beta} i^{-1}_{\mathrm{conv},\alpha}}_{HOR\text{-}B} + \underbrace{\frac{1}{4} u^{-1}_{\Delta,\alpha} i^{+1}_{\mathrm{conv},\beta} + \frac{1}{4} u^{-1}_{\Delta,\beta} i^{+1}_{\mathrm{conv},\alpha}}_{HOR\text{-}C}, \tag{3.46}$$

three theoretically available modes are unveiled. Again, the corresponding Table 3.3 evaluates feasibility of each potential mode.

Vertical Energy-Balancing

Unlike the previously discussed total and horizontal instantaneous power components, deviations in vertical dimension require provision of a suitable composition of converter-internal positive and negative sequence currents. Unfortunately, no alternative utilizing ac or dc currents exists. Nevertheless – where *VER-a* depicts unbalanced ($u^{-1}_{\Delta,\alpha/\beta} \neq 0$) and *VER-b* balanced ($u^{-1}_{\Delta,\alpha/\beta} = 0$) conditions – when considering the relevant equations

$$\bar{p}_{\Delta,\alpha} = -u^{+1}_{\Delta,\alpha} i^{-1}_{\mathrm{phm},\alpha} + u^{+1}_{\Delta,\beta} i^{-1}_{\mathrm{phm},\beta} - u^{-1}_{\Delta,\alpha} i^{+1}_{\mathrm{phm},\alpha} + u^{-1}_{\Delta,\beta} i^{+1}_{\mathrm{phm},\beta} \tag{3.47a}$$

$$\underbrace{=}_{u^{-1}_{\Delta,\alpha/\beta}=0} -u^{+1}_{\Delta,\alpha} i^{-1}_{\mathrm{phm},\alpha} + u^{+1}_{\Delta,\beta} i^{-1}_{\mathrm{phm},\beta} \tag{3.47b}$$

$$\bar{p}_{\Delta,\beta} = +u^{+1}_{\Delta,\alpha} i^{-1}_{\mathrm{phm},\beta} + u^{+1}_{\Delta,\beta} i^{-1}_{\mathrm{phm},\alpha} + u^{-1}_{\Delta,\alpha} i^{+1}_{\mathrm{phm},\beta} + u^{-1}_{\Delta,\beta} i^{+1}_{\mathrm{phm},\alpha} \tag{3.48a}$$

$$\underbrace{=}_{u^{-1}_{\Delta,\alpha/\beta}=0} +u^{+1}_{\Delta,\alpha} i^{-1}_{\mathrm{phm},\beta} + u^{+1}_{\Delta,\beta} i^{-1}_{\mathrm{phm},\alpha} \tag{3.48b}$$

$$\bar{p}_{\Delta,0} = -u^{+1}_{\Delta,\alpha} i^{+1}_{\mathrm{phm},\alpha} - u^{+1}_{\Delta,\beta} i^{+1}_{\mathrm{phm},\beta} - u^{-1}_{\Delta,\alpha} i^{-1}_{\mathrm{phm},\alpha} - u^{-1}_{\Delta,\beta} i^{-1}_{\mathrm{phm},\beta} \tag{3.49a}$$

$$\underbrace{=}_{u^{-1}_{\Delta,\alpha/\beta}=0} -u^{+1}_{\Delta,\alpha} i^{+1}_{\mathrm{phm},\alpha} - u^{+1}_{\Delta,\beta} i^{+1}_{\mathrm{phm},\beta}. \tag{3.49b}$$

it is obvious that permanent drifts only occur during transients and are not linked to the currents relevant for power exchange. This is guiding the way towards measures to entirely turn off vertical balancing during unbalanced conditions, mainly to lower current stresses of power electronic devices as highlighted within Table 3.4.

Table 3.2: Possibilities to realize total energy-balancing.

mode	measure	quantity	remark
TOT-A	adjust dc current	i_{dc}	utilized to guarantee the specified ac power exchange at the PCC, applied during ac faults
TOT-B	adjust ac positive sequence current	$i^{+1}_{\mathrm{conv},\alpha/\beta}$	utilized in the case of specified dc current or dc voltage control, applied during dc faults
TOT-C	adjust ac negative sequence current	$i^{-1}_{\mathrm{conv},\alpha/\beta}$	negative sequence voltage only present during ac faults, high current stresses due to typically low voltage amplitudes, grid-code restrictions apply

Table 3.3: Possibilities to realize horizontal energy-balancing.

mode	measure	quantity	remark
HOR-A	adjust inner current	$i^{\mathrm{dc}}_{\mathrm{phm},\alpha/\beta}$	related inner converter currents have no impact on ac or dc output quantities, requires presence of a dc voltage
HOR-B	adjust ac negative sequence current	$i^{-1}_{\mathrm{conv},\alpha/\beta}$	utilization of negative sequence currents solely required during unbalanced ac faults, use discarded for balancing purposes
HOR-C	adjust ac positive sequence current	$i^{+1}_{\mathrm{conv},\alpha/\beta}$	utilization of positive sequence currents is discarded to avoid impact on ac power exchange, high additional current stresses due to typically low negative sequence voltage amplitudes

Table 3.4: Possibilities to realize vertical energy-balancing.

mode	measure	quantity	remark
VER-a (unbalanced)	adjust inner currents	$i^{\pm 1}_{\mathrm{phm},\alpha/\beta}$	vertical energetic drifts solely caused by transient events, no impact of ac- or dc-side currents during normal operation, instantaneous disturbance rejection requires highly accurate and fast sequence voltage decomposition
VER-b (balanced)	adjust inner currents	$i^{\pm 1}_{\mathrm{phm},\alpha/\beta}$	vertical balancing disabled during unbalanced conditions, avoidance of additional inner currents especially during transient events, rebalancing only subsequent to contingencies

3.3 Introduction to the Control and Balancing Realization

As presented, the distributed allocation of capacitors in MMC arms increase available degrees of freedom but also complexity related to converter operation. This is in contrast to centralized energy storage solutions on the dc-side related to two- or three-level VSCs and requires novel control and balancing concepts. The following literature review briefly summarizes history, identifies present practice and arranges the initial starting point for the proposed control and balancing concept.

3.3.1 Literature Review

As previously indicated in section 2.1, related topics represent a vital field of power engineering and are extensively covered in academia. This section describes evolution and state-of-the-art MMC control approaches for HVdc applications during balanced and unbalanced grid conditions including effects on converter-internal energy distribution and aspects related to grid synchronization.

Evolution of MMC Controls and Balancing

Initial works on converter controls, as intrinsic MMC dynamics differ compared to previous VSC topologies, mainly addressed measures to mitigate unprecedented effects related to inner converter currents (often also referred to as circulating or differential currents excluding the zero-sequence component). If unconsidered, related currents cause additional stresses of IGBTs as well as losses and increasing requirements related to SM quantity and capacitor size due to higher SM stack sum voltage fluctuations. As a solution, [5] proposed an adapted modulation concept and [102] introduced a circulating current suppressing controller (CCSC) leading to improved performance during steady-state operation. Due to the straightforward applicability, by eliminating negative-sequence double line-frequency circulating current components utilizing a corresponding rotating reference frame, the CCSC is still widely utilized in HVdc scheme and grid studies [122]. While these measures solely addressed internal currents, fundamental circuit analysis has been further extended by energetic considerations [31] and several contributions proposed supplementary energy-balancing loops to improve performance during and subsequent to dynamic operation point changes, see [12, 11, 85]. Nevertheless, proposed controls still provided limited performance during unbalanced ac grid conditions. To achieve a more generalized degree of applicability, additional modifications to suppress dc voltage ripples by a zero-sequence differential voltage controller including a band-pass filter [101] or rather a proportional-integral-resonant (PIR) individual arm current controller have been introduced [67, 68].

Decoupled MMC Controls and Balancing

Even though previously introduced control and balancing methodologies provide a suitable response to a wide range of operational conditions, performance limitations arise due to deficient decoupling of current and voltage quantities as well as energy states related to the SM stack charging status. As proposed in several contributions following a similar methodology, indicated in [89] as well as in commercial patents [126] and elaborated in greater detail in [72, 16, 42], straightforward analysis and separation of linear independent quantities enable decoupled current controls and targeted energy-balancing for arbitrary applications. In total, this comprises six current (five+one depending on the ac-side transformer configuration) and six energy states for a three-phase converter. Appropriate utilization of these degrees of freedom enables independent control of ac-side, inner and dc-side currents and offers energy-balancing possibilities in several dimensions as stated in Table 3.2-3.4. Besides total energy control via ac- or dc-side, this incorporates the chance to rebalance the system in a horizontal (between the three converter phase-modules) or vertical (between upper and lower arm of a single converter phase-module) dimension without manipulating converter-external quantities.

MMC Controls and Balancing in the Case of External Contingencies

Based on previously introduced basics and considering grid code related requirements specified within section 2.3, appropriate performance of HVdc converters has to be assured in the case of external contingencies. This includes, besides dc faults leading to an immediate output current reduction, handling of unbalanced ac conditions and coordinated FRT during distant ac faults within the connected network. Technically, this affects sequence detection and grid synchronization, sequence current controls as well as converter energy-balancing strategies.

In grid-connected converter applications, as addressed in [134, 25], synchronous reference frame phase-locked loops (SRF-PLL) do not provide suitable characteristics in terms of phase angle and grid frequency estimation during unbalanced grid faults or in the case of distorted grid conditions. Therefore, implementation of advanced PLL structures utilizing selective filtering techniques – which also enable appropriate estimation of sequence or harmonic components – is inevitable to overcome related drawbacks. Even though a wide range of solutions is available, only a limited number of approaches is offering fast dynamic response, disturbance rejection and furthermore harmonic extraction capability. Besides widely applied decoupled double synchronous reference frame PLL (DDSRF-PLL) utilizing a cross-feedback decoupling network or notch-structures, these are – given in the most generalized form – multiple second-order generalized integrator-based frequency or phase-locked loop (MSOGI-FLL/-PLL) and multiple complex coefficient filter-based PLL (MCCF-PLL), see [24] for a comparison.

Self-commutated power electronic circuits based on IGBT switches, like in type 4 wind turbines (WT) with fully rated converters or any VSC, enable independent adaption of positive and negative sequence currents during unbalanced ac grid conditions, see [110]. Besides negative sequence current suppression, either utilizing a simple negative sequence feed-forward or an active control-wise current suppression strategy, also more sophisticated methods to balance individual phase output voltages or to boost/reduce corresponding sequence voltage amplitudes injecting appropriate reactive current components exist. While this field mainly evolved based on considerations related to wind power plant controls, as addressed in [105, 76], also a growing interest related to MMC-HVdc applications arose. While [3] provides a general overview related to different control strategies and effects on ac output quantities as well as dc link voltage ripples, [19] investigates effects related to an embedded MMC-HVdc scheme with respect to predefined reactive current injection strategies and [92, 93] discuss extended current limitation aspects. Nonetheless, insights related to converter energy-balancing still remain rather indistinct.

This shortcoming has been picked up by several contributions focussing on MMC analysis under arbitrary unbalanced conditions. In [81, 82], current reference determination under singular unbalanced voltage conditions and a universally applicable control design methodology are proposed. Furthermore, [47] provides a straightforward analysis of non-fluctuating power components to identify available balancing possibilities and presents a control concept based on proportional (integral) resonant (P(I)R) current controllers.

3.3.2 Related Publications

The control and balancing concept presented in this chapter has been developed and extended throughout the entire duration of this thesis. Major milestones, besides additional contributions listed in Appendix G.3, have been published in *IEEE Transactions on Power Delivery* [Jrnl2016a, Jrnl2018d] and have been presented at the *IEEE International Energy Conference (Energycon)* [Conf2016a] in May 2016.

3.4 Control and Balancing Concept

This section presents the implemented control and balancing concept for an individually controlled MMC in the bipolar configuration with DMR. It is partitioned into four layers taking into account both signal flows and cascaded control structures. Individual layers are subdivided into core building blocks related to their functionality. An overview, including references to subsections, is provided within Fig. 3.4. In the first layer quantity determination as well as outer control loops are covered, which requires transformation of various measurements for control purposes and processing of external references provided by a dispatch center. Note that ac quantities now refer to the selected PCC located on the ac-side of the converter transformer. This differs compared to the circuit analysis provided within section 3.1, where quantities are related to the converter-side of the transformer. The second layer addresses energy-balancing aspects to remain the system within its operational boundaries, while the third layer discusses implementation and design of converter-internal current controls. To determine SM-individual IGBT switching commands, the fourth layer highlights arm output reference value determination and cell modulation.

As already indicated in the previous literature review in section 3.3.1, design and especially tuning of MMC-related controls calls for a well-structured and straightforward approach. Furthermore, to add functional enhancements or modify individual parts in the course of generic studies, simple extendability or replacement of individual building blocks is required. Therefore, a cascaded control structure based on proportional integral (PI)-controllers with optional anti-windup extension has been selected[3]. The detailed structure of the selected parallel PI-controller is indicated in Fig. 3.5 and corresponds to

$$K(s) = \left(k_\mathrm{p} + \frac{1}{sT_\mathrm{i}}\right) \tag{3.50}$$

in Laplace domain. To specify the controller settings, assuming the most generalized representation, proportional gain k_p, integral time constant T_i as well as upper lim_up and lower $\mathrm{lim}_\mathrm{low}$ output limit need to be defined.

[3]It should be noted that fully integrated state-space approaches leading to periodic bilinear time-varying models exist, see evolution in [63, 64, 71, 72].

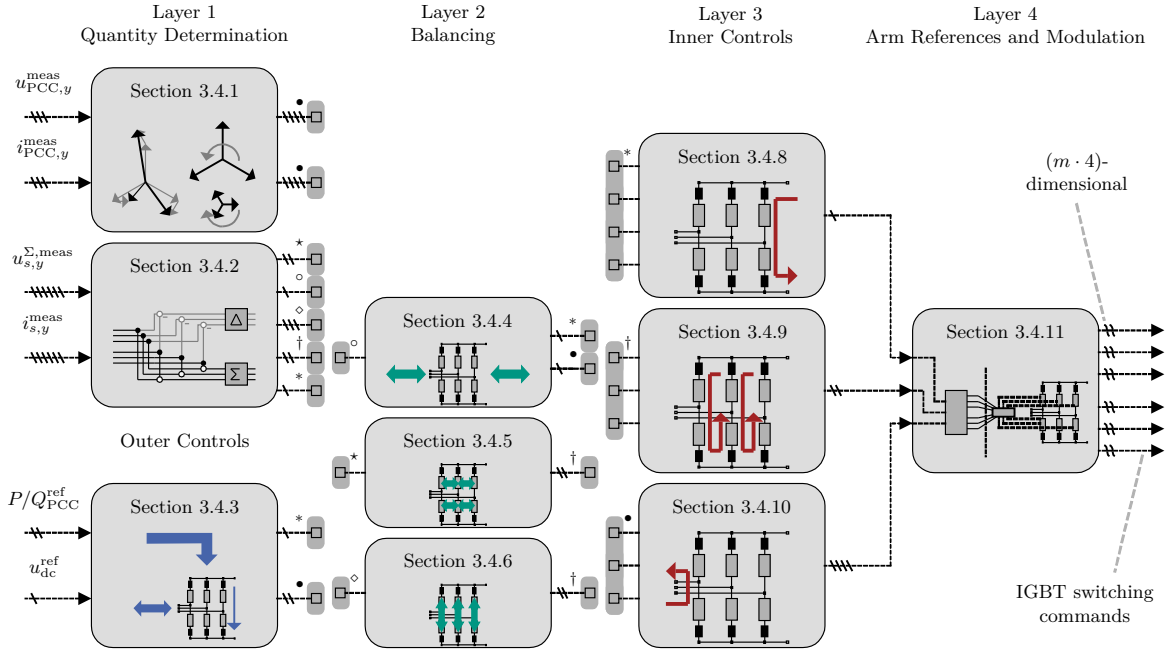

Figure 3.4: Overview of proposed converter control and balancing concept partitioned into four layers and several underlying core building blocks. Signal flows and dimensions indicated accordingly.

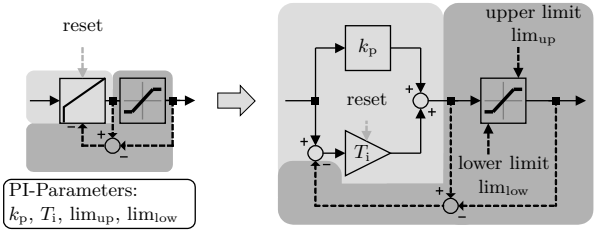

Figure 3.5: Utilized parallel PI-structure with optional anti-windup functionality.

If not stated differently, control parameters are approximated by applying either the *symmetrical optimum method* or the *modulus optimum method* depending on the loop characteristics (outer or inner loop) and dynamic requirements (high disturbance rejection capability or fast dynamic response), see [127] and [132] for further in-depth theoretical background. Feasible performance has been validated for a wide range of converter-related (conventional VSC as well as MMC) applications [6, 42, 30] and enables the requested straightforward adaptation possibility in the case of changing normative constraints/guidelines or transmission system as well as converter design modifications.

3.4.1 Sequence Component Decomposition and PLL

Unlike for offshore wind applications or weak electrical grid conditions, no grid-forming properties like in [93] are needed in the case of embedded HVdc[4]. However, it is required to appropriately synchronize to the grid-imposed and variable frequency and decompose positive and negative sequence components (voltages and currents) to comply with grid-codes under balanced and unbalanced operation conditions. Typically, this is realized by decoupled double synchronous rotating reference frames (sequence indicator and order $\pm n = \pm 1$) and low-pass or notch filtering of dq-components [91]. Within this work, a different approach utilizing complex transfer functions with polarity-selective filtering capability is selected. Their application is enabled as three-phase quantities transformed into $\alpha\beta$-frame form an orthogonal system, see [99] for further insights. The corresponding two-module complex coefficient filter (TM-CCF) is beneficial for two main reasons. First, with respect to realizations in [134, 91], additional reverse transformations ($\pm n = \pm 2$) into a uniform frame for cross-feedback decoupling become obso-

[4]This excludes black-start capability and potentially requires reconsideration in the case of continuously increasing shares of power electronic in-feed in the future.

lete. Second, the developed framework strives to facilitate easy expandability to implement functions beyond the immediate scope like harmonic extraction and compensation. This can be achieved by utilizing MCCF structures like in [46].

In order to realize sequence component or even harmonic decomposition by polarity-selective filters in Laplace domain, a simple real first-order low-pass structure

$$H(s) = \frac{\omega_\mathrm{c}}{s + \omega_\mathrm{c}} \tag{3.51}$$

with cutoff angular frequency ω_c is modified by substituting

$$s \rightarrow s - j(\pm n)\omega^\mathrm{est}, \tag{3.52}$$

where ω^est represents the estimated grid angular frequency to retune the filters during operation in the case of grid-frequency variations. This leads to the complex[5] first order band-pass filter (CBF) realization

$$\underline{H}^{\pm 1}_\mathrm{CBF}(s) = \frac{\omega_\mathrm{c}}{s \mp j\omega^\mathrm{est} + \omega_\mathrm{c}}. \tag{3.53}$$

Assuming an arbitrary complex $(\alpha + j\beta)$ input quantity in Laplace domain $\underline{X}_{\alpha\beta}(s)$ composed of fundamental as well as harmonic components with highest occurring order k and neglecting further disturbances or noise, the relation

$$\underline{X}_{\alpha\beta}(s) = \sum_{i=-k}^{k} \left[\underline{X}^i_{\alpha\beta}(s)\right] \tag{3.54}$$

can be introduced. Following the calculation of overall control deviation and superimposing the relevant CBF output representing the remaining filter stimulation in steady-state, the generalized MCCF transfer function according to

$$\underline{Y}^{\pm n}_{\alpha\beta}(s) = \underline{H}^{\pm n}_{\mathrm{CBF},\alpha\beta}(s) \underbrace{\left[\underline{X}_{\alpha\beta}(s) - \sum_{i=-k}^{k} \left[\underline{Y}^i_{\alpha\beta}(s)\right] + \underline{Y}^{\pm n}_{\alpha\beta}(s)\right]}_{\underline{E}^{\pm n}_{\mathrm{CBF},\alpha\beta}(s)} \tag{3.55}$$

is obtained. To account for well-established signal processing and control realizations in $\alpha\beta$-frame, it appears convenient to realize the required complex transfer function as a real two-input-two-output system. Herewith, a cross coupling between α and β components is introduced, see [61] for further insights, resulting in the translated time domain CBF representation according to [28, 25] as visualized in Fig. 3.6.

[5] It is important to highlight that corresponding real and imaginary parts do solely describe a relative contribution to the impulse response, see [99].

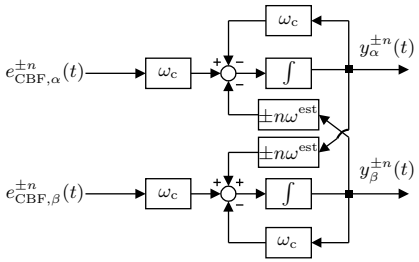

Figure 3.6: Complex bandpass filter implementation.

PCC Voltage Quantity Decomposition and PLL

According to requirements stated in section 2.3, converters need to adapt reactive current references according to the change in sequence voltage amplitudes at the PCC. This presupposes, besides suitable decomposition techniques achieved by the TM-CCF, fast voltage synchronization (individual sequence phase angle determination) to obtain the correct alignments. Under normal operation conditions, as highlighted within Fig. 3.7, this is conventionally achieved by a straightforward PLL implementation where the positive sequence phase angle $\theta^{+1} = +\omega t$ immediately results in the steady-state (subscript stdy) inverse phase angle $\theta^{-1}_{\mathrm{stdy}} = -\theta^{+1} = -\omega t$ used to suppress negative sequence output currents. Here, $\omega = 2\pi f$, where f is the grid frequency. In contrast, unbalanced conditions call for additional modifications, if a particular negative sequence reactive output current is required. Assuming a feasible negative sequence voltage magnitude threshold is exceeded – potentially reflected by reasonable grid-code provided deadband ranges or at least caused by signal acquisition accuracy or present background noise – a simple threshold or hysteresis characteristic is applied to switch between steady-state $\theta^{-1}_{\mathrm{stdy}}$ and dynamic (subscript dyn) $\theta^{-1}_{\mathrm{dyn}}$ phase angle. While [91] resolves this task by determining the required negative sequence angular relation in $\alpha\beta$-frame, this work introduces a second PLL, which is solely enabled during unbalanced conditions. Even though this introduces an additional controller, associated benefits include tuning for comparatively low voltage magnitudes and the possibility to modify dynamic response related to the individual demands.

Design of the TM-CCF including PLL controllers respects recommendations derived in [25]. Besides evaluation of robustness and disturbance rejection capability, especially the accordance of response speed is of interest related to HVdc applications, see [114]. This requires selection of a crossover frequency ω_{co} (typical range $2\pi 20$ up to $2\pi 25$ rad/s, see [25]) as well as a constant parameter g (typical range 1.732 up to 3.732, see [25]) linked to the resulting phase margin.

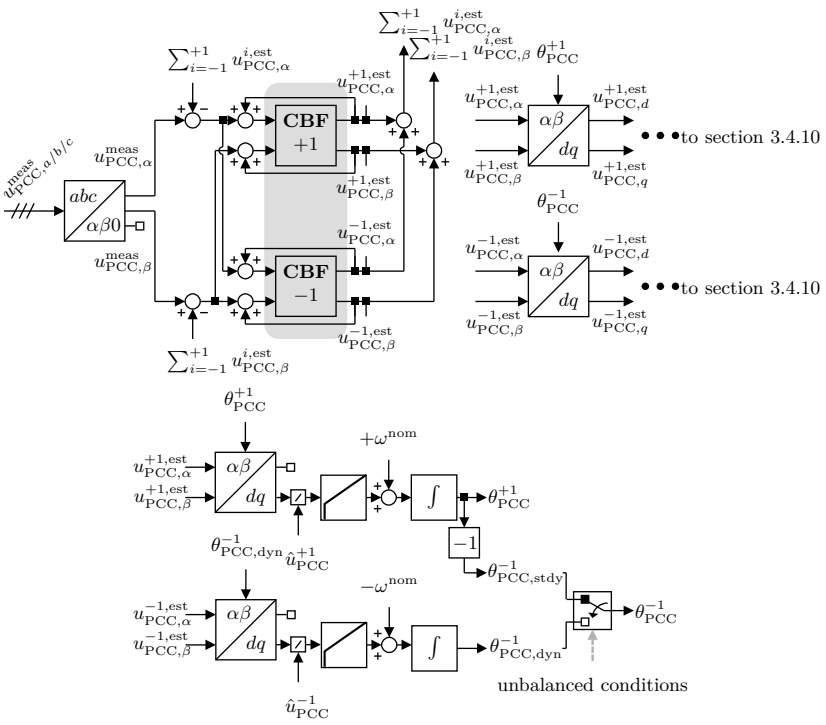

Figure 3.7: TM-CCF implementation to decompose PCC voltages including PLLs.

Subsequently, the parameters can be derived based on

$$k_{\mathrm{p}}^{\mathrm{PLL}} = \omega_{\mathrm{co}}, \qquad T_{\mathrm{i}}^{\mathrm{PLL}} = g/\omega_{\mathrm{co}}^2, \qquad \omega_{\mathrm{c}} = g \cdot \omega_{\mathrm{co}} \tag{3.56}$$

where $k_{\mathrm{p}}^{\mathrm{PLL}}$, $T_{\mathrm{i}}^{\mathrm{PLL}}$ are related to the PLL PI-controllers[6] and ω_{c} is the CBF cutoff angular frequency.

PCC Current Quantity Decomposition

Similar to sequence voltage decomposition, a TM-CCF is established to estimate positive and negative sequence current components, see Fig 3.8. While generally

[6] The PLL controller inputs, as visualized in Fig. 3.7, are per-unitized by dividing through either reference voltage amplitude or deadband width.

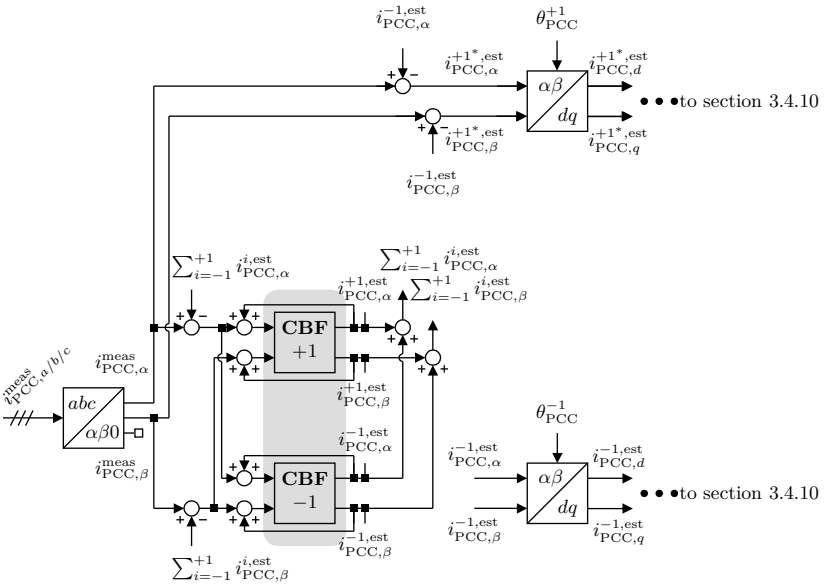

Figure 3.8: TM-CCF implementation to decompose PCC currents including modified fundamental positive sequence estimation.

signal routing and filter-design is equal compared to the previous section, a major difference exists related to the estimated fundamental positive sequence current transferred to the underlying inner control loops. To appropriately decouple the different current regulators under arbitrarily unbalanced or distorted conditions, effects related to unconsidered harmonics, measurement-related noise or power electronic switching distortion are solely incorporated into the modified positive fundamental component (superscript *) $i^{+1^*,\mathrm{est}}_{\mathrm{PCC},\alpha/\beta}$. This is achieved by substracting all separately extracted components as proposed in [45, 44]. Exemplarily for the fundamental sequence case, this corresponds to

$$i^{+1^*,\mathrm{est}}_{\mathrm{PCC},\alpha/\beta} = i^{\mathrm{meas}}_{\mathrm{PCC},\alpha/\beta} - i^{-1,\mathrm{est}}_{\mathrm{PCC},\alpha/\beta} \tag{3.57}$$

and targets the direction of unwanted effects to one control loop to improve dynamic performance.

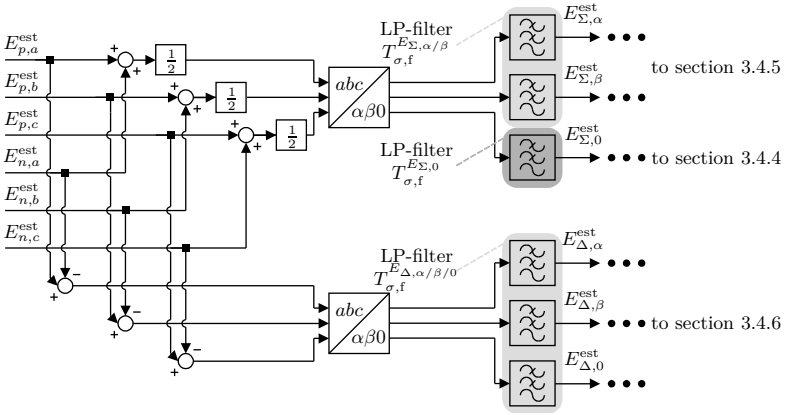

Figure 3.9: Determination of energetic quantities.

3.4.2 Quantity Transformation

Besides PCC voltages and currents, which have been already processed leading to sequence quantity and phase angle estimations, energy states and phase-module currents need to be derived based on SM voltage and arm current measurements.

Energetic Quantity Determination

Prior to the decomposition and application of Clarke transformation, the energy content of each arm has to be estimated. As indicated in section 3.2.1, equal distribution of sum voltage among the SM capacitors is implied as internal arm imbalances are treated separately by appropriate modulation algorithms, see also [82, 47]. This reduces computational efforts related to determination of arm energies by calculating, similar to eq. (3.20), only a single multiplication according to

$$E^{\text{est}}_{s,y} \approx \frac{1}{2} \cdot \frac{C_{\text{SM}}}{m} \cdot \left(u^{\Sigma,\text{meas}}_{s,y}\right)^2 = \frac{1}{2} \cdot \frac{C_{\text{SM}}}{m} \cdot \left(\sum_{i=1}^{m} \left(u^{i,\text{meas}}_{s,y}\right) \right)^2 , \tag{3.58}$$

where $E^{\text{est}}_{s,y}$ is the resulting arm energy estimation to be further processed.

Turning the view towards Fig. 3.9 and following the decomposition, a filter-stage is included to suppress fluctuating components. This separation is required to realize energy controls solely considering average terms as mathematically realized within eq. (3.42) by neglecting oscillating parts. In literature, a wide range of filter types has been considered. Besides finite impulse response (FIR) or notch realizations,

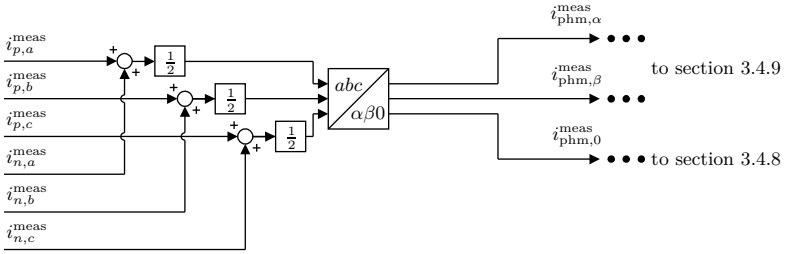

Figure 3.10: Determination of phase-module currents.

see [42, 82], lowpass filters are selected in the course of this thesis to account for mainly two reasons. First, unwanted effects caused by various phenomena (power electronic switching patterns, nonlinearities, etc.) require appropriate suppression to minimize acdc interactions or converter-internal disturbances. Second, the wide frequency range specified within the grid connection conditions compromises the performance of filter structures tuned for a nominal condition. Related filter time constants ($T_{\sigma,\text{f}}^{E_{\Sigma,\alpha/\beta}}/T_{\sigma,\text{f}}^{E_{\Sigma,0}}/T_{\sigma,\text{f}}^{E_{\Delta,\alpha/\beta/0}}$) are clustered according to the energy loop affiliation following the order horizontal, total and vertical balancing.

Phase-Module Current Determination

Phase-module currents are determined in a straightforward manner according to section 3.1.3. As an input, see schematic overview provided within Fig. 3.10, measured arm currents ($i_{s,y}^{\text{meas}}$) are transformed in $\alpha\beta0$-frame and resulting quantities are directed to corresponding current control loops.

3.4.3 Outer Controls

This work investigates embedded MMC-HVdc applications. Therefore, individual converters adjust active and reactive power exchange according to the assigned control mode. At system level, the corresponding TSO or link operator coordinates behavior of affected assets at their specified PCC. Besides numerous derivatives, the two most basic realizations related to a link application are P_{PCC}-Q_{PCC}- or u_{dc}-Q_{PCC}-control mode each implemented at one terminal[7]. Unlike for low-level VSCs, see for example [110], the decoupled control possibility of ac and dc quantities as well as the absence of a centralized dc capacitor in MMC-HVdc applications cause a need for adapted control design and implementation, see [95].

[7]Further possibilities are remaining combinations of $P_{\text{PCC}}/P_{\text{PCC}}(f)/u_{\text{dc}}$ with $Q_{\text{PCC}}/Q_{\text{PCC}}(u_{\text{PCC}})/\cos(\varphi)$, but are beyond the scope of this work.

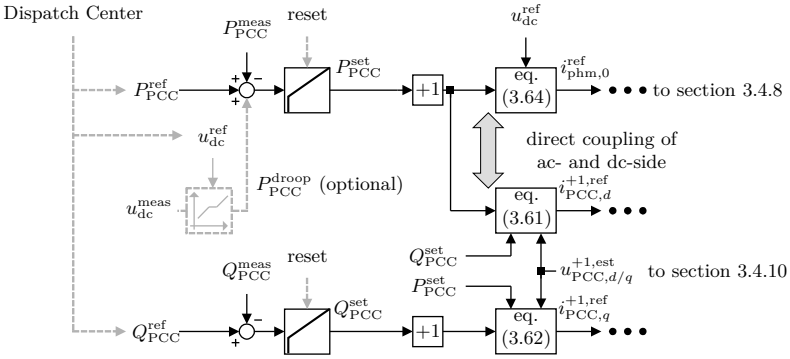

Figure 3.11: Outer control implementation in P_{PCC}-Q_{PCC} control mode.

P_{PCC}-Q_{PCC}-Controlled Station

In order to realize ac-side controls, discussed further in section 3.4.10, direct-quadrature-transformation (dq) is utilized according to Appendix A. Therefore, appropriate reference values must be determined based on the selected active and reactive power setpoints and transferred to the inner control loops as shown in Fig. 3.11. Similar to [92, 30], the generalized relationships at the PCC follow

$$P_{\mathrm{PCC}} = \frac{3}{2}\left(u_{\mathrm{PCC},d}^{+1} i_{\mathrm{PCC},d}^{+1} + u_{\mathrm{PCC},q}^{+1} i_{\mathrm{PCC},q}^{+1}\right) \tag{3.59}$$

and

$$Q_{\mathrm{PCC}} = \frac{3}{2}\left(u_{\mathrm{PCC},q}^{+1} i_{\mathrm{PCC},d}^{+1} - u_{\mathrm{PCC},d}^{+1} i_{\mathrm{PCC},q}^{+1}\right), \tag{3.60}$$

where corresponding current reference values are obtained utilizing estimated (superscript est) input and uncertainty-compensated reference values to be set (superscript set) according to

$$i_{\mathrm{PCC},d}^{+1,\mathrm{ref}} = \frac{2}{3}\frac{\left(u_{\mathrm{PCC},d}^{+1,\mathrm{est}} P_{\mathrm{PCC}}^{\mathrm{set}} + u_{\mathrm{PCC},q}^{+1,\mathrm{est}} Q_{\mathrm{PCC}}^{\mathrm{set}}\right)}{\left(u_{\mathrm{PCC},d}^{+1,\mathrm{est}}\right)^2 + \left(u_{\mathrm{PCC},q}^{+1,\mathrm{est}}\right)^2} \tag{3.61}$$

and

$$i_{\mathrm{PCC},q}^{+1,\mathrm{ref}} = \frac{2}{3}\frac{\left(u_{\mathrm{PCC},q}^{+1,\mathrm{est}} P_{\mathrm{PCC}}^{\mathrm{set}} - u_{\mathrm{PCC},d}^{+1,\mathrm{est}} Q_{\mathrm{PCC}}^{\mathrm{set}}\right)}{\left(u_{\mathrm{PCC},d}^{+1,\mathrm{est}}\right)^2 + \left(u_{\mathrm{PCC},q}^{+1,\mathrm{est}}\right)^2}. \tag{3.62}$$

To maintain the system within a balanced state, the dc-side power exchange

$$P_{\mathrm{dc}} = 3u_{\mathrm{dc}}i_{\mathrm{phm},0} = u_{\mathrm{dc}}i_{\mathrm{dc}p} = -u_{\mathrm{dc}}i_{\mathrm{dc}n} \tag{3.63}$$

is supposed to follow modifications on the ac-side within a reasonable timespan to avoid exceedance of energy-related SM constraints. Therefore, rewriting the relation above leads to

$$i_{\mathrm{phm},0}^{\mathrm{ref}} = \frac{1}{3}i_{\mathrm{dc}s}^{\mathrm{ref}} \underbrace{=}_{P_{\mathrm{dc}}=P_{\mathrm{PCC}}} \frac{P_{\mathrm{PCC}}^{\mathrm{set}}}{3 \cdot u_{\mathrm{dc}}^{\mathrm{ref}}}, \tag{3.64}$$

where power value to be applied and dc voltage reference values are utilized. In the case of a sustaining mismatch or dc voltage drift, the intrinsic buffering capability of an MMC is used and additional energy-balancing loops equalize setpoints. Related to the latter loops, which only compensate permanent energetic drifts (deviation from averaged values), this significantly improves dynamic system response in the case of rapid operation point changes.

As further described in [30], outer PCC active and reactive power controllers are theoretically obsolete. Nevertheless, to account for the impact of peripheral equipment and uncertainties (impedance of power transformer, converter control and adjustable cooling power supply located at the tertiary transformer winding, etc.), controllers with unity gain and a time constant significantly higher than the one of current control loops are set up according to

$$k_{\mathrm{p}}^{\mathrm{P/Q}} = 1, \tag{3.65}$$

and

$$T_{\mathrm{i}}^{\mathrm{P/Q}} > 10 \cdot \left(T_{\mathrm{i}}^{i_{\mathrm{PCC},d/q}^{+1}} \right). \tag{3.66}$$

$u_{\mathbf{dc}}$-$Q_{\mathbf{PCC}}$-Controlled Station

The dc voltage controller is embedded within a cascaded control structure, see Fig. 3.12. Due to the selected current direction, an inverted controller output is required, see Fig. 3.2. Unlike direct (open-loop) dc voltage control (immediate adaption of $u_{\Sigma,0}$), the underlying $i_{\mathrm{phm},0}$ control loop provides a straightforward current limitation capability. This is beneficial – especially related to operation of bipolar schemes – to avoid severe overcurrents during contingencies and dynamic events. To reduce acdc interactions the feed-forward power reference value transferred towards the ac-side is low-pass filtered and again the intrinsic buffering capability of an MMC is exploited. This is, for example, beneficial in case the opposite converter within a link quickly adjusts transmitted dc current leading to an energy balancing task, which requires the voltage-controlled station to

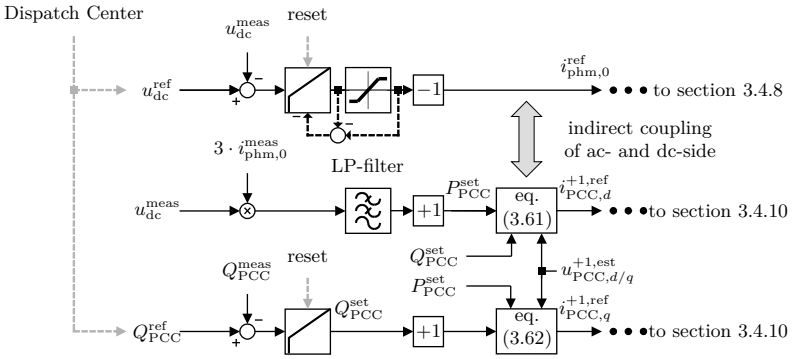

Figure 3.12: Outer control implementation in u_{dc}-Q_{PCC} control mode.

adapt its output power. As requirements related to reactive power control remain unchanged, implementation does not differ compared to a P_{PCC}-Q_{PCC}-controlled station.

In order to derive dc voltage controller parameters the dynamics of the dc link voltage is modeled like in [85]. Therefore, the overall line capacitance is aggregated ($C_{\mathrm{dc}}^{\mathrm{eqv}}$, mainly related to capacitance per km of line C' and dc filters) and connected in parallel to a virtual dc current source/sink ($i_{\mathrm{dc}}^{\mathrm{eqv}}$, not measurable) representing the opposite station as shown in Fig. 3.13. Considering relations given in eq. (3.64), this results in

$$\dot{u}_{\mathrm{dc}} = \frac{i_{\mathrm{dc}}^{\mathrm{eqv}} - 3 \cdot i_{\mathrm{phm},0}}{C_{\mathrm{dc}}^{\mathrm{eqv}}} \tag{3.67}$$

and the coupling between dc voltage and phase-module current is expressed by

$$\underbrace{\left(\frac{1}{3} i_{\mathrm{dc}}^{\mathrm{eqv}} - i_{\mathrm{phm},0}\right)}_{\frac{1}{3} i_{\mathrm{C}}^{\mathrm{eqv}}} = \frac{C_{\mathrm{dc}}^{\mathrm{eqv}} \dot{u}_{\mathrm{dc}}}{3}. \tag{3.68}$$

Control parameters are approximated utilizing the *symmetrical optimum method* similar to [30]. Related to the schematic in Laplace domain presented within Fig. D.1, this leads to

$$k_{\mathrm{p}}^{u_{\mathrm{dc}}} = \frac{T_{\mathrm{loop}}^{u_{\mathrm{dc}}}}{a \cdot k_{\mathrm{loop}}^{u_{\mathrm{dc}}} \cdot T_{\sigma}^{u_{\mathrm{dc}}}} = \frac{C_{\mathrm{dc}}^{\mathrm{eqv}}}{a \cdot 3 \cdot T_{\sigma}^{u_{\mathrm{dc}}}}, \tag{3.69}$$

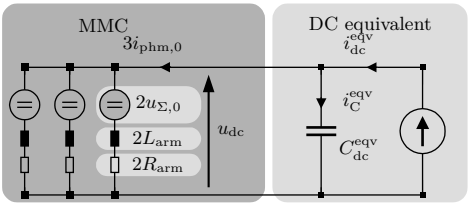

Figure 3.13: Simplified approximation of dc-side voltage dynamics.

and

$$T_{\mathrm{i}}^{u_{\mathrm{dc}}} = a^2 \cdot T_{\sigma}^{u_{\mathrm{dc}}} / k_{\mathrm{p}}^{u_{\mathrm{dc}}}, \tag{3.70}$$

where $T_{\mathrm{loop}}^{u_{\mathrm{dc}}}$ and $k_{\mathrm{loop}}^{u_{\mathrm{dc}}}$ represent loop integral time constant as well as overall gain linked to eq. (3.68). Furthermore, following the design rules as derived in [132], parameter a is set to 2 and

$$T_{\sigma}^{u_{\mathrm{dc}}} = T_{\sigma,\mathrm{f}}^{u_{\mathrm{dc}}} + T_{\sigma,\mathrm{a}}^{u_{\mathrm{dc}}} + T_{\sigma,\mathrm{c}}^{u_{\mathrm{dc}}} + 2(T_{\sigma,\mathrm{c}}^{i_{\mathrm{phm},0}} + T_{\sigma,\mathrm{m}})$$

represents the non-compensable time constant considering measurement filter, data acquisition and control delay (subscript f, a, c) and twice the subordinate control[8] as well as modulation (subscript m) delays.

3.4.4 Total Energy-Balancing

Within section 3.2.4, the average instantaneous arm power component $\bar{p}_{\Sigma,0}$ has been derived. With respect to the intended control of quantities on the dc-side and at the PCC, we can rewrite eq. (3.44) neglecting converter-internal losses as

$$\begin{aligned}\bar{p}_{\Sigma,0} = \frac{1}{2} u_{\mathrm{dc}} i_{\mathrm{phm},0} &- \frac{1}{4}\left(u_{\mathrm{PCC},d}^{+1} i_{\mathrm{PCC},d}^{+1} + u_{\mathrm{PCC},q}^{+1} i_{\mathrm{PCC},q}^{+1}\right) \\ &- \frac{1}{4}\left(u_{\mathrm{PCC},d}^{-1} i_{\mathrm{PCC},d}^{-1} + u_{\mathrm{PCC},q}^{-1} i_{\mathrm{PCC},q}^{-1}\right),\end{aligned} \tag{3.71}$$

where ac quantities have been transformed into dq-frame. Depending on the overall converter operation mode, see Table 3.2 for feasibility considerations, either balancing mode *TOT-A* or *TOT-B* are applied to restore steady-state conditions by adding ancillary power components. Here, $E_{\Sigma,0}^{\mathrm{ref}}$ corresponds to the definition given in eq. (3.24). In the first setting, the phase-module current or rather dc current is modified to avoid unwanted modifications at the PCC (suitable for a P_{PCC}-Q_{PCC}-controlled station). Otherwise, the positive sequence current is adapted (suitable for a u_{dc}-Q_{PCC}-controlled station), see Fig. 3.14.

[8] The inner current control loops are later on designed utilizing modulus optimum strategy. Therefore, these loops can be approximated by a first-order transfer function with twice the intrinsic non-compensable time-constant.

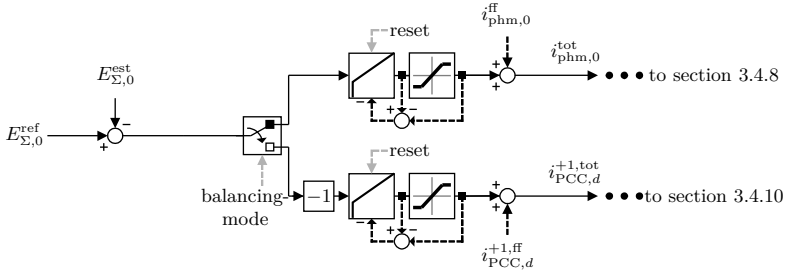

Figure 3.14: Total energy-balancing implementation.

Implementation of *TOT-A*

To improve controller performance, especially during dynamic setpoint adaptions and faults, optional feed-forward (superscript ff) power imbalance compensation can be applied. Setting eq. (3.71) to zero and rearranging the expression to define an additional phase-module current component then leads to

$$i^{\mathrm{ff}}_{\mathrm{phm},0} = \frac{\cancel{+u^{+1,\mathrm{ref}}_{\mathrm{PCC},d} i^{+1,\mathrm{ref}}_{\mathrm{PCC},d}} + u^{+1,\mathrm{ref}}_{\mathrm{PCC},q} i^{+1,\mathrm{ref}}_{\mathrm{PCC},q} + u^{-1,\mathrm{ref}}_{\mathrm{PCC},d} i^{-1,\mathrm{ref}}_{\mathrm{PCC},d} + u^{-1,\mathrm{ref}}_{\mathrm{PCC},q} i^{-1,\mathrm{ref}}_{\mathrm{PCC},q}}{4 \cdot \frac{1}{2} u^{\mathrm{ref}}_{\mathrm{dc}}}, \tag{3.72}$$

where reference values are strictly considered to minimize acquisition impacts encouraged by the fact that the relatively slow superimposed controller accounts for remaining deviations[9]. The first term in the nominator of eq. (3.72) is discarded. Underlying outer controls signal routing including implemented coupling of ac- and dc-side in section 3.4.3 already fed forward this power component. A second consideration has to be avoided to prevent incorrect operating points leading to potentially severe converter energy drifts. Furthermore, as PLL(s) align the sequence voltages to maintain $u^{+1}_{\mathrm{PCC},q} = u^{-1}_{\mathrm{PCC},q} \approx 0$ and typically no active power in-feed is applied in the negative sequence $u^{-1}_{\mathrm{PCC},d} \approx 0$, the remaining parts are of minor significance and are just respected for the sake of completeness.

Control of energy states is mainly required in the case of externally triggered distortions. Therefore, *symmetrical optimum method* is applied to tune the controller. With respect to Fig. D.2, this results in

$$k_{\mathrm{p}}^{E_{\Sigma,0}} = \frac{T_{\mathrm{loop}}^{E_{\Sigma,0}}}{a \cdot k_{\mathrm{loop}}^{E_{\Sigma,0}} \cdot T_{\sigma}^{E_{\Sigma,0}}} = \frac{1}{\frac{a}{2} \cdot u^{\mathrm{nom}}_{\mathrm{dc}} \cdot T_{\sigma}^{E_{\Sigma,0}}}, \tag{3.73}$$

[9] A feed-forward compensation utilizing reference values has proven superior performance subsequent to contingencies during extensive simulative evaluations.

and

$$T_{\mathrm{i}}^{E_{\Sigma,0}} = a^2 \cdot T_{\sigma}^{E_{\Sigma,0}} / k_{\mathrm{p}}^{E_{\Sigma,0}}, \tag{3.74}$$

where

$$T_{\sigma}^{E_{\Sigma,0}} = T_{\sigma,\mathrm{f}}^{E_{\Sigma,0}} + T_{\sigma,\mathrm{a}}^{E_{\Sigma,0}} + T_{\sigma,\mathrm{c}}^{E_{\Sigma,0}} + 2 \cdot \left(T_{\sigma,\mathrm{c}}^{i_{\mathrm{phm},0}} + T_{\sigma,\mathrm{m}} \right)$$

includes the sum of all non-compensable time constants and a is set to 2.

Implementation of Mode *TOT-B*

Following the same procedure for the determined alternative *TOT-B*, the expression is set to zero and rearranged to define an additional positive sequence active current component. This yields to

$$i_{\mathrm{PCC},d}^{+1,\mathrm{ff}} = \frac{\cancel{4 \cdot \frac{1}{2} u_{\mathrm{dc}}^{\mathrm{ref},\mathrm{ref}} i_{\mathrm{phm},0}} - u_{\mathrm{PCC},q}^{+1,\mathrm{ref}} i_{\mathrm{PCC},q}^{+1,\mathrm{ref}} - u_{\mathrm{PCC},d}^{-1,\mathrm{ref}} i_{\mathrm{PCC},d}^{-1,\mathrm{ref}} - u_{\mathrm{PCC},q}^{-1,\mathrm{ref}} i_{\mathrm{PCC},q}^{-1,\mathrm{ref}}}{u_{\mathrm{PCC},d}^{+1,\mathrm{ref}}} \tag{3.75}$$

where strictly reference values are considered. Again, the first term in nominator of eq. (3.75) is discarded, while remaining components are approximately zero as coupling of ac- and dc-side has already been realized utilizing measured dc quantities in the outer control building block[10],

According to Fig. D.3 and similar to the previous part, *symmetrical optimum method* yields to

$$k_{\mathrm{p}}^{E_{\Sigma,0}} = \frac{T_{\mathrm{loop}}^{E_{\Sigma,0}}}{a \cdot k_{\mathrm{loop}}^{E_{\Sigma,0}} \cdot T_{\sigma}^{E_{\Sigma,0}}} = \frac{4}{a \cdot u_{\mathrm{PCC},d}^{+1,\mathrm{nom}} \cdot T_{\mathrm{i}}^{E_{\Sigma,0}}}, \tag{3.76}$$

and

$$T_{\mathrm{i}}^{E_{\Sigma,0}} = a^2 \cdot T_{\sigma}^{E_{\Sigma,0}} / k_{\mathrm{p}}^{E_{\Sigma,0}}, \tag{3.77}$$

where

$$T_{\sigma}^{E_{\Sigma,0}} = T_{\sigma,\mathrm{f}}^{E_{\Sigma,0}} + T_{\sigma,\mathrm{a}}^{E_{\Sigma,0}} + T_{\sigma,\mathrm{c}}^{E_{\Sigma,0}} + 2 \cdot \left(T_{\sigma,\mathrm{c}}^{i_{\mathrm{PCC},d}^{+1}} + T_{\sigma,\mathrm{m}} \right)$$

represents the sum of associated non-compensable time constants and a is set to 2.

[10] Unlike for a P_{PCC}-Q_{PCC}-controlled converter station, straightforward power output prediction can not be provided for a converter controlling the dc voltage. The applied setpoint is mainly related to the independently controlled opposite converter of a link, assuming no physical limits leading to output restrictions are violated. To obtain a reliable and quasi-instantaneous (feed-forward) ac positive sequence current reference, the lowpass filtered value of the instantaneous dc power output is utilized, see section 3.4.3.

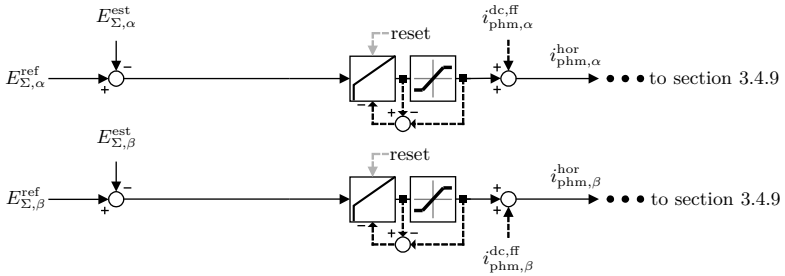

Figure 3.15: Horizontal energy-balancing implementation.

3.4.5 Horizontal Energy-Balancing

Handling of energetic imbalance in horizontal direction (between converter phase-modules) is an essential feature to guarantee appropriate performance of MMC-HVdc schemes. This is especially the case during unbalanced ac grid conditions. Even though several degrees of freedom exist, as shown in Table 3.3 and evaluated in [47], utilization of direct current components in the phase-module currents $i^{\mathrm{dc}}_{\mathrm{phm},\alpha/\beta}$ (mode *HOR-A*) offers a benefit and has therefore been selected. Here, neither ac current nor dc current exchange are modified. While the utilization of lowpass filters to suppress inherent energetic fluctuations retards dynamic performance, a feed-forward compensation is advantageous, see Fig. 3.15. To limit deviations during dynamic setpoint adaptions requested by grid code specifications summarized in section 2.3, requested reference values are directly passed through following a similar strategy as in [13]. The associated mathematical expression is obtained by setting eq. (3.45) and eq. (3.46) to zero, respectively. Considering reference values related to the PCC quantities, this leads to

$$i^{\mathrm{dc,ff}}_{\mathrm{phm},\alpha} = \frac{+u^{+1,\mathrm{ref}}_{\mathrm{PCC},\alpha} i^{-1,\mathrm{ref}}_{\mathrm{PCC},\alpha} + u^{-1,\mathrm{ref}}_{\mathrm{PCC},\alpha} i^{+1,\mathrm{ref}}_{\mathrm{PCC},\alpha} - u^{+1,\mathrm{ref}}_{\mathrm{PCC},\beta} i^{-1,\mathrm{ref}}_{\mathrm{PCC},\beta} - u^{-1,\mathrm{ref}}_{\mathrm{PCC},\beta} i^{+1,\mathrm{ref}}_{\mathrm{PCC},\beta}}{4 \cdot \frac{1}{2} u^{\mathrm{ref}}_{\mathrm{dc}}}, \tag{3.78}$$

and

$$i^{\mathrm{dc,ff}}_{\mathrm{phm},\beta} = \frac{-u^{+1,\mathrm{ref}}_{\mathrm{PCC},\alpha} i^{-1,\mathrm{ref}}_{\mathrm{PCC},\beta} - u^{-1,\mathrm{ref}}_{\mathrm{PCC},\alpha} i^{+1,\mathrm{ref}}_{\mathrm{PCC},\beta} - u^{+1,\mathrm{ref}}_{\mathrm{PCC},\beta} i^{-1,\mathrm{ref}}_{\mathrm{PCC},\alpha} - u^{-1,\mathrm{ref}}_{\mathrm{PCC},\beta} i^{+1,\mathrm{ref}}_{\mathrm{PCC},\alpha}}{4 \cdot \frac{1}{2} u^{\mathrm{ref}}_{\mathrm{dc}}}. \tag{3.79}$$

Application of *symmetrical optimum method* further enables achievement of suit-

able distortion rejection capability. With respect to Fig. D.4, this results in

$$k_{\mathrm{p}}^{E_{\Sigma,\alpha/\beta}} = \frac{T_{\mathrm{loop}}^{E_{\Sigma,\alpha/\beta}}}{a \cdot k_{\mathrm{loop}}^{E_{\Sigma,\alpha/\beta}} \cdot T_{\sigma}^{E_{\Sigma,\alpha/\beta}}} = \frac{1}{a \cdot \frac{u_{\mathrm{dc}}^{\mathrm{nom}}}{2} \cdot T_{\sigma}^{E_{\Sigma,\alpha/\beta}}}, \tag{3.80}$$

and

$$T_{\mathrm{i}}^{E_{\Sigma,\alpha/\beta}} = a^2 \cdot T_{\sigma}^{E_{\Sigma,\alpha/\beta}} / k_{\mathrm{p}}^{E_{\Sigma,\alpha/\beta}}, \tag{3.81}$$

where

$$T_{\sigma}^{E_{\Sigma,\alpha/\beta}} = T_{\sigma,\mathrm{f}}^{E_{\Sigma,\alpha/\beta}} + T_{\sigma,\mathrm{a}}^{E_{\Sigma,\alpha/\beta}} + T_{\sigma,\mathrm{c}}^{E_{\Sigma,\alpha/\beta}} + 2 \cdot \left(T_{\sigma,\mathrm{c}}^{i_{\mathrm{phm},\alpha/\beta}} + T_{\sigma,\mathrm{m}} \right)$$

features all non-compensable time constants and a is set to 2.

3.4.6 Vertical Energy-Balancing

As highlighted within section 3.2.4, vertical energetic deviations between upper and lower arms of phase-modules are solely adjustable by utilizing specific converter-internal currents referred to as $i_{\mathrm{phm},\alpha/\beta}^{\mathrm{ver}}$ in Fig. 3.16. Even though it initially appears straightforward to neglect this adaptability, observing the fact that only internal currents are capable to cause permanent vertical drifts, unforeseen imbalances may occur due to other reasons. These could be uncertainties related to quantity estimation during dynamic events, effects caused by occurring contingencies or inaccuracies depending on the inherent system complexity. Unfortunately, with respect to the generalized relations in eq. (3.47a)-(3.49a), continuous regulation under arbitrary voltage conditions imposes difficulties. As described in [81], singular unbalanced situations – where positive and negative sequence voltage magnitudes equal each other – lead to a current reference calculation problem resulting in infinite values. Therefore, as proposed in [82] as one possible workaround, vertical balancing is turned off during unbalanced contingencies and re-initiated after voltage recovery[11].

This simplifies the relevant power component terms and leads to the statements provided in eqs. (3.47b)-(3.49b). Subsequently, similar to [71, 42, 30], associated voltage and current quantities in stationary $\alpha\beta$-frame are re-expressed by a superposition of positive and negative sequence quantities in forward and backward rotating dq-frame, respectively.

In the case of steady-state (balanced) voltage conditions ($u_{\Delta,q}^{+1} \approx 0, u_{\Delta,d/q}^{-1} \approx 0$) and neglecting fluctuating components, this results in

[11] A thorough overview and evaluation of alternative measures to mitigate current reference value determination difficulties and their impacts on energetic behavior is provided in [81].

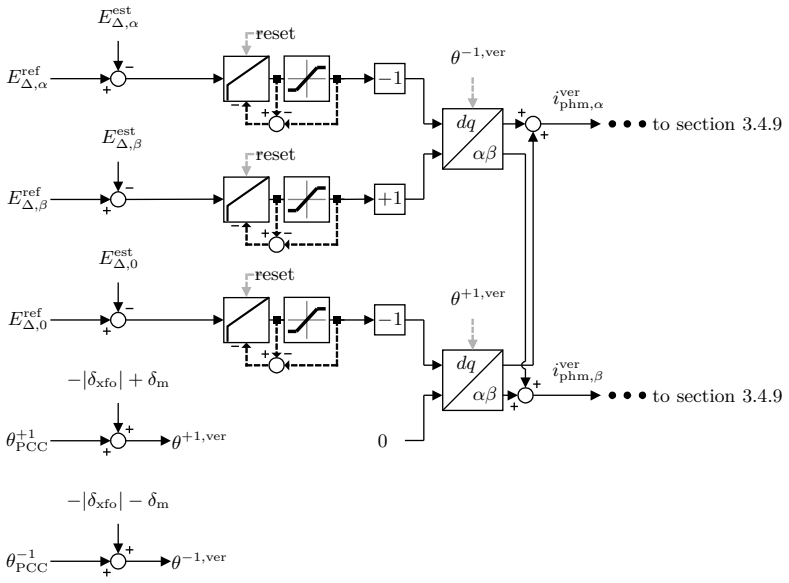

Figure 3.16: Vertical energy-balancing implementation.

$$\bar{p}_{\Delta,\alpha} = -u^{+1}_{\Delta,d} i^{-1}_{\text{phm},d} \underbrace{+u^{+1}_{\Delta,q} i^{-1}_{\text{phm},q}}_{\approx 0} \Rightarrow i^{-1}_{\text{phm},d} = -\frac{\bar{p}_{\Delta,\alpha}}{u^{+1}_{\Delta,d}} \tag{3.82}$$

$$\bar{p}_{\Delta,\beta} = +u^{+1}_{\Delta,d} i^{-1}_{\text{phm},q} \underbrace{+u^{+1}_{\Delta,q} i^{-1}_{\text{phm},d}}_{\approx 0} \Rightarrow i^{-1}_{\text{phm},q} = +\frac{\bar{p}_{\Delta,\beta}}{u^{+1}_{\Delta,d}} \tag{3.83}$$

$$\bar{p}_{\Delta,0} = -u^{+1}_{\Delta,d} i^{+1}_{\text{phm},d} \underbrace{-u^{+1}_{\Delta,q} i^{+1}_{\text{phm},q}}_{\approx 0} \Rightarrow i^{+1}_{\text{phm},d} = -\frac{\bar{p}_{\Delta,0}}{u^{+1}_{\Delta,d}}, \tag{3.84}$$

where maximum active power components are obtained by phase-module currents in phase with the ac voltage at the converter. Since the phase angle is acquired at the PCC a compensation of transformer (subscript xfo) phase shift δ_{xfo} and the modulation delay δ_{m} to obtain $\theta^{+1,\text{ver}}$ and $\theta^{-1,\text{ver}} = -\theta^{+1,\text{ver}}$ is required. Consequently, vertical balancing reference currents in $\alpha\beta$-frame are derived according

to

$$\begin{bmatrix} i^{\mathrm{ver}}_{\mathrm{phm},\alpha} \\ i^{\mathrm{ver}}_{\mathrm{phm},\beta} \end{bmatrix} = \begin{bmatrix} i^{+1}_{\mathrm{phm},\alpha} + i^{-1}_{\mathrm{phm},\alpha} \\ i^{+1}_{\mathrm{phm},\beta} + i^{-1}_{\mathrm{phm},\beta} \end{bmatrix} = \underbrace{\boldsymbol{T}^{dq\rightarrow\alpha\beta}}_{\theta=\theta^{+1,\mathrm{ver}}} \begin{bmatrix} i^{+1}_{\mathrm{phm},d} \\ i^{+1}_{\mathrm{phm},q} \end{bmatrix} + \underbrace{\boldsymbol{T}^{dq\rightarrow\alpha\beta}}_{\theta=\theta^{-1,\mathrm{ver}}} \begin{bmatrix} i^{-1}_{\mathrm{phm},d} \\ i^{-1}_{\mathrm{phm},q} \end{bmatrix}. \quad (3.85)$$

Finally, utilization of *symmetrical optimum method* with respect to Fig. D.5 leads to the following set of control parameters

$$k_{\mathrm{p}}^{E_{\Delta,\alpha/\beta/0}} = \frac{T_{\mathrm{loop}}^{E_{\Delta,\alpha/\beta/0}}}{a \cdot k_{\mathrm{loop}}^{E_{\Delta,\alpha/\beta/0}} \cdot T_{\sigma}^{E_{\Delta,\alpha/\beta/0}}} = \frac{1}{a \cdot u_{\Delta,d}^{+1,\mathrm{nom}} \cdot T_{\sigma}^{E_{\Delta,\alpha/\beta/0}}}, \quad (3.86)$$

and

$$T_{\mathrm{i}}^{E_{\Delta,\alpha/\beta/0}} = a^2 \cdot T_{\sigma}^{E_{\Delta,\alpha/\beta/0}} / k_{\mathrm{p}}^{E_{\Delta,\alpha/\beta/0}}, \quad (3.87)$$

where

$$T_{\sigma}^{E_{\Delta,\alpha/\beta/0}} = T_{\sigma,\mathrm{f}}^{E_{\Delta,\alpha/\beta/0}} + T_{\sigma,\mathrm{a}}^{E_{\Delta,\alpha/\beta/0}} + T_{\sigma,\mathrm{c}}^{E_{\Delta,\alpha/\beta/0}} + 2 \cdot \left(T_{\sigma,\mathrm{c}}^{i_{\mathrm{phm},\alpha/\beta}} + T_{\sigma,\mathrm{m}} \right)$$

features the related sum of non-compensable time constants and a is set to 2.

3.4.7 Balancing Current Limitation

Especially in the case of MMC applications, it is necessary to monitor and limit currents consisting of a multitude of individual components[12]. Related to balancing current contribution and respecting introduced feed-forward compensation, general relations are obtained for total (both modes), horizontal and vertical balancing limiters. Those are:

$$\lim_{\mathrm{up/low}}^{i_{\mathrm{phm},0}^{\mathrm{tot,max}}} = \pm(i_{\mathrm{phm},0}^{\mathrm{tot,max}} - |i_{\mathrm{phm},0}^{\mathrm{ff}}|). \quad (3.88)$$

$$\lim_{\mathrm{up/low}}^{i_{\mathrm{PCC},d}^{+1,\mathrm{tot,max}}} = \pm(i_{\mathrm{PCC},d}^{+1,\mathrm{tot,max}} - |i_{\mathrm{PCC},d}^{+1,\mathrm{ff}}|), \quad (3.89)$$

$$\lim_{\mathrm{up/low}}^{i_{\mathrm{phm},\alpha/\beta}^{\mathrm{hor,max}}} = \pm(i_{\mathrm{phm},\alpha/\beta}^{\mathrm{hor,max}} - |i_{\mathrm{phm},\alpha/\beta}^{\mathrm{hor,ff}}|), \quad (3.90)$$

$$\lim_{\mathrm{up/low}}^{i_{\mathrm{phm},d/q}^{\pm1,\mathrm{ver,max}}} = \pm i_{\mathrm{phm},d/q}^{\pm1,\mathrm{ver,max}}, \quad (3.91)$$

where currents with superscript max represent the maximum reference current contribution of a single balancing loop to be defined with respect to maximum IGBT current limits. Unlike for total and horizontal balancing, limitation measures concerning vertical balancing must not consider additional feed-forward terms.

[12]Note that arm currents cannot be limited, which is mainly due to the decoupled current control approach. Furthermore, to avoid significant oversizing of inherent current capabilities, selected thresholds shall reflect occuring simultaneity of balancing needs.

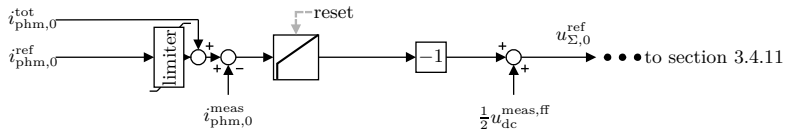

Figure 3.17: DC current control and limitation implementation.

3.4.8 DC Current Controls

Control implementation to adjust the zero-sequence phase-module current $i_{\text{phm},0}$, which is directly linked to the dc current, is depicted within Fig. 3.17 and follows eq. (3.10). To address given hardware constraints related to the limited SM current capability, the maximum setpoint $i^{\text{ref}}_{\text{phm},0}$ must be restricted[13].

With respect to the connected dc-side transmission scheme and related dynamics, see indication given within the simplified control loop representation in Laplace domain in Fig. D.6, controller tuning according to the derived equivalent circuit utilizing *modulus optimum method* in Fig. 3.3 has been discarded. Instead, control parameters are determined following an approach according to [21, 56], where structured feedback gains are utilized. Here, to reflect necessities to utilize only locally available quantities, a PI-control structure is emulated.

To highlight the underlying methodology a generalized extended control problem according to Fig. 3.18 is considered. This corresponds to

$$\underbrace{\begin{bmatrix}\dot{\mathbf{x}}\\ \dot{\mathbf{e}}\end{bmatrix}}_{\dot{\tilde{\mathbf{x}}}} = \underbrace{\begin{bmatrix}\mathbf{A} & \mathbf{0}\\ -\mathbf{C} & \mathbf{0}\end{bmatrix}}_{\tilde{\mathbf{A}}} \cdot \underbrace{\begin{bmatrix}\mathbf{x}\\ \mathbf{e}\end{bmatrix}}_{\tilde{\mathbf{x}}} + \underbrace{\begin{bmatrix}\mathbf{B}\\ \mathbf{0}\end{bmatrix}}_{\tilde{\mathbf{B}}} \cdot \mathbf{u}, \tag{3.92}$$

where

$$\mathbf{y} = \mathbf{C} \cdot \tilde{\mathbf{x}} \tag{3.93}$$

and with $\mathbf{C} = \mathbf{I}$ (identity matrix)

$$\mathbf{u} = -\underbrace{\left[+\mathbf{F}^{\text{sc}}_{\text{p}}, \quad +\mathbf{F}^{\text{sc}}_{\text{i}}\right]}_{\mathbf{F}} \cdot [\tilde{\mathbf{x}}]\,. \tag{3.94}$$

Here, $\mathbf{F}$ is the feedback gain matrix subject to structural constraints (superscript sc) dictating its zero entries.

[13] Note that the limitation must be chosen in coordination with the ac current controller. The bypassed balancing current is independently limited within the total energy controller.

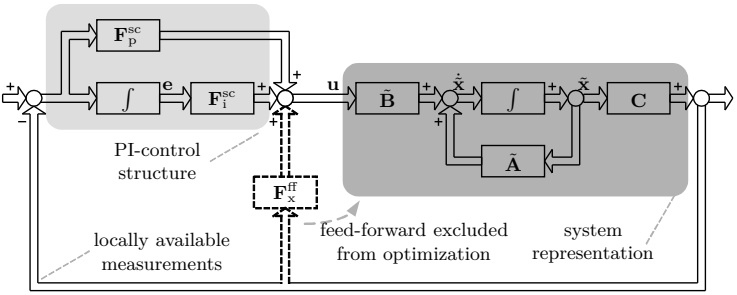

Figure 3.18: Block diagram of structurally constrained control problem.

This leads to the task to

$$\underset{\tilde{\mathbf{x}}}{\text{minimize}} \qquad J = \frac{1}{2}\int_0^\infty \left(\tilde{\mathbf{x}}^T\mathbf{Q}\tilde{\mathbf{x}} + \mathbf{u}^T\mathbf{R}\mathbf{u}\right)\mathrm{d}t, \tag{3.95}$$

$$\text{where} \qquad \dot{\tilde{\mathbf{x}}} = \left(\tilde{\mathbf{A}} - \tilde{\mathbf{B}}\mathbf{F}\right)\tilde{\mathbf{x}} \qquad \text{and} \qquad \mathbf{F} \in \mathbb{S}. \tag{3.96}$$

Here, $\mathbb{S}$ determines the subspace which includes the provided set of structural constraints.

To apply this methodology to the underlying $i_{\mathrm{phm},0}$-control loop, the following steps must be performed:

- determination of a suitable transmission line model utilizing parallel π-sections based on the given line geometry according to [29]
- identification of effective $i_{\mathrm{phm},0}$ converter control loop impedance and delays
- formulation of corresponding state space representation,
- selection of structural constraints to emulate a PI-control structure based on locally available quantities
- selection of suitable weighting matrices to promote the intended behavior
- and solving of optimization problem utilizing the algorithm presented in [21]. This results in a directly applicable set of PI-parameters k_p and T_i

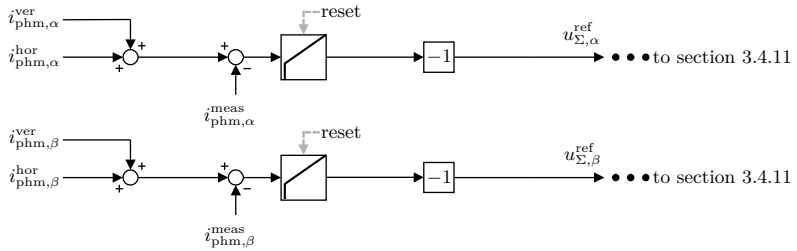

Figure 3.19: Internal current control implementation.

3.4.9 Internal Current Controls

Dynamics related to inner converter currents $i_{\mathrm{phm},\alpha/\beta}$, as derived in section 3.1.4 and visually depicted in Fig. 3.3, correspond to a first order system mainly affected by the selected converter arm inductor L_{arm} and aggregated resistance R_{arm}[14]. Therefore, to obtain the fastest possible dynamics and settling time, *modulus optimum method* is utilized to design the implemented PI-controller. With respect to the reference current composition consisting of constant and alternating components, use of an integral gain may be discarded for two reasons. First, an integral gain causes a phase shift between input and output signal, which has an adverse effect in light of the desired current alignment related to the vertical balancing task. Second, presence of an integral gain in upstream energy-balancing controllers already ensures appropriate performance.

With respect to Fig. D.7, this yields to the following proportional and (optional) integral gain

$$k_{\mathrm{p}}^{i_{\mathrm{phm},\alpha/\beta}} = \frac{T_{\mathrm{loop}}^{i_{\mathrm{phm},\alpha/\beta}}}{2 \cdot k_{\mathrm{loop}}^{i_{\mathrm{phm},\alpha/\beta}} \cdot T_{\sigma}^{i_{\mathrm{phm},\alpha/\beta}}} = \frac{L_{\mathrm{arm}}}{2 \cdot T_{\sigma}^{i_{\mathrm{phm},\alpha/\beta}}}, \tag{3.97}$$

and (not recommended as mentioned above)

$$T_{\mathrm{i}}^{i_{\mathrm{phm},\alpha/\beta}} = T_{\mathrm{loop}}^{i_{\mathrm{phm},\alpha/\beta}} / k_{\mathrm{p}}^{i_{\mathrm{phm},\alpha/\beta}} = \frac{2 \cdot T_{\sigma}^{i_{\mathrm{phm},\alpha/\beta}}}{R_{\mathrm{arm}}}, \tag{3.98}$$

where

$$T_{\sigma}^{i_{\mathrm{phm},\alpha/\beta}} = T_{\sigma,\mathrm{f}}^{i_{\mathrm{phm},\alpha/\beta}} + T_{\sigma,\mathrm{a}}^{i_{\mathrm{phm},\alpha/\beta}} + T_{\sigma,\mathrm{c}}^{i_{\mathrm{phm},\alpha/\beta}} + T_{\sigma,\mathrm{m}}$$

represents the total non-compensable time constant.

[14] This includes parasitic resistive elements related to the inductor, busbars and internal connecting lines as well as power electronic switches.

3.4.10 AC Current Controls

For MMC-HVdc applications, ac-side controls refer to a particular PCC specified by the relevant TSO. This connection point is typically located on the grid-side of the converter transformer. To derive underlying dynamics for control design, initially in $\alpha\beta$-frame, the basic relations given in eq. (3.11) need to be adapted with respect to the shifted reference point and a non-unity transformer ratio r_{xfo}[15]. Consequently, transforming arm-related impedances (R'_{arm},L'_{arm}) to the PCC-side according to

$$\frac{\hat{u}_{\mathrm{PCC}}}{\hat{u}_{\mathrm{conv}}} = r_{\mathrm{xfo}}, \qquad \frac{1}{2}L'_{\mathrm{arm}} = r_{\mathrm{xfo}}^2 \cdot \frac{1}{2}L_{\mathrm{arm}}, \qquad \frac{1}{2}R'_{\mathrm{arm}} = r_{\mathrm{xfo}}^2 \cdot \frac{1}{2}R_{\mathrm{arm}}, \quad (3.99)$$

and representing the transformer by its characteristic series impedance (R_{xfo}, L_{xfo}), this leads to

$$\begin{bmatrix} u'_{\Delta,\alpha} \\ u'_{\Delta,\beta} \end{bmatrix} = \begin{bmatrix} u_{\mathrm{PCC},\alpha} \\ u_{\mathrm{PCC},\beta} \end{bmatrix} + R_{\mathrm{ac}} \begin{bmatrix} i_{\mathrm{PCC},\alpha} \\ i_{\mathrm{PCC},\beta} \end{bmatrix} + L_{\mathrm{ac}} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{PCC},\alpha} \\ i_{\mathrm{PCC},\beta} \end{bmatrix}, \quad (3.100)$$

where

$$\begin{bmatrix} u_{\Delta,\alpha} \\ u_{\Delta,\beta} \end{bmatrix} = \frac{1}{r_{\mathrm{xfo}}} \begin{bmatrix} u'_{\Delta,\alpha} \\ u'_{\Delta,\beta} \end{bmatrix} \quad (3.101)$$

and

$$L_{\mathrm{ac}} = L_{\mathrm{xfo}} + \frac{1}{2}L'_{\mathrm{arm}}, \qquad R_{\mathrm{ac}} = R_{\mathrm{xfo}} + \frac{1}{2}R'_{\mathrm{arm}}. \quad (3.102)$$

The corresponding equivalent circuit is visualized in Fig. 3.20.

Associating this modification with previously introduced sequence currents as well as voltages and replacing $\alpha\beta$-frame quantities by their corresponding relations in oppositely rotating dq-frames according to

$$\begin{bmatrix} x_\alpha^{+1} \\ x_\beta^{+1} \end{bmatrix} = \underbrace{\mathbf{T}^{dq\to\alpha\beta}}_{\theta=\theta_{\mathrm{PCC}}^{+1}} \begin{bmatrix} x_d^{+1} \\ x_q^{+1} \end{bmatrix} \quad , \quad \begin{bmatrix} x_\alpha^{-1} \\ x_\beta^{-1} \end{bmatrix} = \underbrace{\mathbf{T}^{dq\to\alpha\beta}}_{\theta=\theta_{\mathrm{PCC}}^{-1}} \begin{bmatrix} x_d^{-1} \\ x_q^{-1} \end{bmatrix}, \quad (3.103)$$

the fundamental reference frame current control relations are obtained like in [134, 44, 30][16]. Those correspond to

$$\begin{bmatrix} u_{\Delta,d}^{+1'} \\ u_{\Delta,q}^{+1'} \end{bmatrix} = \begin{bmatrix} u_{\mathrm{PCC},d}^{+1} \\ u_{\mathrm{PCC},q}^{+1} \end{bmatrix} + \begin{bmatrix} +R_{\mathrm{ac}} & -\omega L_{\mathrm{ac}} \\ +\omega L_{\mathrm{ac}} & +R_{\mathrm{ac}} \end{bmatrix} \begin{bmatrix} i_{\mathrm{PCC},d}^{+1} \\ i_{\mathrm{PCC},q}^{+1} \end{bmatrix} + L_{\mathrm{ac}} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{PCC},d}^{+1} \\ i_{\mathrm{PCC},q}^{+1} \end{bmatrix} \quad (3.104)$$

[15] Note this does not include the transformer vector group. This aspect will be addressed and considered later on in section 3.4.11.

[16] Note that a positive current represents in-feed/injection into the ac grid.

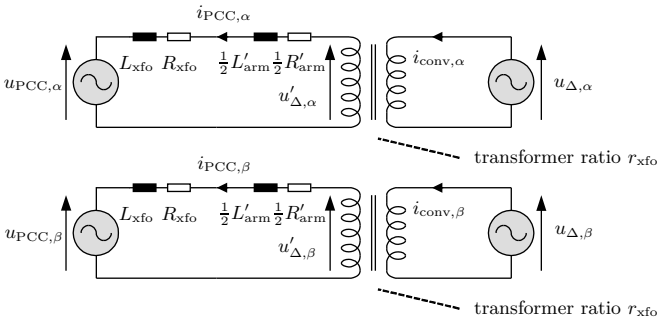

Figure 3.20: Extended ac-side equivalent circuit in $\alpha\beta$-frame respecting a non-unity transformer ratio.

and

$$\begin{bmatrix} u^{-1\prime}_{\Delta,d} \\ u^{-1\prime}_{\Delta,q} \end{bmatrix} = \begin{bmatrix} u^{-1}_{\mathrm{PCC},d} \\ u^{-1}_{\mathrm{PCC},q} \end{bmatrix} + \begin{bmatrix} +R_{\mathrm{ac}} & +\omega L_{\mathrm{ac}} \\ -\omega L_{\mathrm{ac}} & +R_{\mathrm{ac}} \end{bmatrix} \begin{bmatrix} i^{-1}_{\mathrm{PCC},d} \\ i^{-1}_{\mathrm{PCC},q} \end{bmatrix} + L_{\mathrm{ac}} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i^{-1}_{\mathrm{PCC},d} \\ i^{-1}_{\mathrm{PCC},q} \end{bmatrix}. \tag{3.105}$$

Utilizing the relations above as well as the decoupled estimated sequence quantities based on section 3.4.1, controls according to Fig. 3.21 can be set up resulting in four arm output reference voltages $u^{\pm 1}_{\Delta,d/q}$. Furthermore, inspecting the control loop approximation in Fig. D.8, control parameters can be calculated applying *modulus optimum method* to achieve fast settling time[17].

$$k_{\mathrm{p}}^{i^{\pm 1}_{\mathrm{PCC},d/q}} = \frac{T_{\mathrm{loop}}^{i^{\pm 1}_{\mathrm{PCC},d/q}}}{2 \cdot k_{\mathrm{loop}}^{i^{\pm 1}_{\mathrm{PCC},d/q}} \cdot T_{\sigma}^{i^{\pm 1}_{\mathrm{PCC},d/q}}} = \frac{L_{\mathrm{ac}}}{2 \cdot T_{\sigma}^{i^{\pm 1}_{\mathrm{PCC},d/q}}}, \tag{3.106}$$

and

$$T_{\mathrm{i}}^{i^{\pm 1}_{\mathrm{PCC},d/q}} = T_{\mathrm{loop}}^{i^{\pm 1}_{\mathrm{PCC},d/q}} / k_{\mathrm{p}}^{i^{\pm 1}_{\mathrm{PCC},d/q}} = \frac{2 \cdot T_{\sigma}^{i^{\pm 1}_{\mathrm{PCC},d/q}}}{R_{\mathrm{ac}}}, \tag{3.107}$$

where

$$T_{\sigma}^{i^{\pm 1}_{\mathrm{PCC},d/q}} = T_{\sigma,\mathrm{f}}^{i^{\pm 1}_{\mathrm{PCC},d/q}} + T_{\sigma,\mathrm{a}}^{i^{\pm 1}_{\mathrm{PCC},d/q}} + T_{\sigma,\mathrm{c}}^{i^{\pm 1}_{\mathrm{PCC},d/q}} + T_{\sigma,\mathrm{m}}$$

[17] As indicated in [85, 82], the considered time constant $T_{\sigma}^{i^{\pm 1}_{\mathrm{PCC},d/q}}$ is typically chosen within a range of several milliseconds.

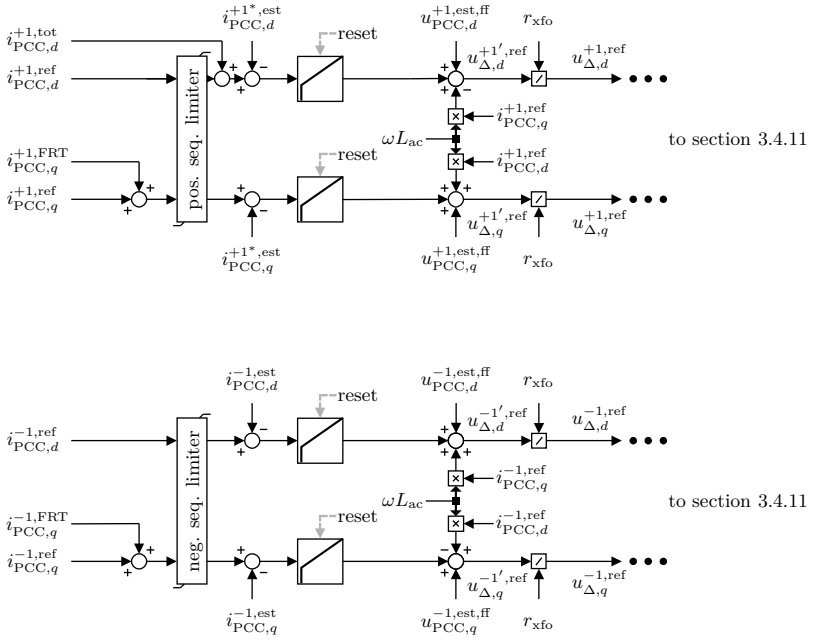

Figure 3.21: AC current control and limitation implementation.

represents the overall non-compensable time constant.

The determination of applicable current reference values – except the balancing current components which are individually limited within the corresponding energy control loops – offers no inherent restriction functionality. Therefore, a sequence-individual saturation with reactive current prioritization is added prior to the ac sequence current control blocks. This implies a maximum continuous ac current limit under balanced conditions (superscript max, subscript stdy) and an extended current limit during dynamic events to account for additional negative sequence current capacity (superscript max, subscript dyn) exists[18].

$$|i^{\mathrm{max}}_{\mathrm{PCC,stdy}}| \geq |\underline{i}^{+1,\mathrm{max}}_{\mathrm{PCC},dq}|, \qquad |i^{\mathrm{max}}_{\mathrm{PCC,dyn}}| \geq |\underline{i}^{+1,\mathrm{max}}_{\mathrm{PCC},dq}| + |\underline{i}^{-1,\mathrm{max}}_{\mathrm{PCC},dq}|, \tag{3.108}$$

where worst case superposition is expected, the following instantaneous conditions

[18] The applied increased current rating concept during dynamic events has been indicated within [19].

have to be continuously met

$$|\underline{i}_{\mathrm{PCC},dq}^{+1,\max}| = \sqrt{(i_{\mathrm{PCC},d}^{+1})^2 + (i_{\mathrm{PCC},q}^{+1})^2}, \tag{3.109}$$

$$|\underline{i}_{\mathrm{PCC},dq}^{-1,\max}| = \sqrt{\cancel{(i_{\mathrm{PCC},d}^{-1})^2} + (i_{\mathrm{PCC},q}^{-1})^2}. \tag{3.110}$$

to remain within the specified operational range. Due to the negative sequence alignment, ensured by the additional PLL during unbalanced conditions, no d-axis current is required.

3.4.11 Arm Reference Voltage Determination and Cell Modulation

Subsequent to the cascaded decomposition and multiple control layers, the final layer addresses arm voltage reference determination and subsequent conversion into SM-individual power electronic switching commands.

Arm Reference Voltage Determination

To determine individual arm voltage reference values in *abc*-frame, inverse Clarke or Park transformation is applied to the set of voltage quantities provided by the seven current control loops ($i_{\mathrm{phm},\alpha/\beta/0}$, $i_{\mathrm{conv},d/q}^{+1}$, $i_{\mathrm{conv},d/q}^{-1}$). Here, as indicated within section 3.4.10, particular attention must be paid to compensate the phase displacement introduced by the transformer for the ac control loops. For a lagging/leading converter-side voltage or rather lagging/leading delta-winding, see also [70], the positive sequence angle is corrected by

$$\theta_{\mathrm{conv}}^{+1} = \theta_{\mathrm{PCC}}^{+1} \mp |\delta_{\mathrm{xfo}}| + \delta_{\mathrm{c}}, \tag{3.111}$$

where $\mp$ indicates lagging or leading configuration, δ_{xfo} is a multiple of $\frac{\pi}{6}$ depending on the transformer vector group and δ_{c} compensates control-related delays to improve dynamic performance. Thereafter, allocation of quantities according to eq. (3.17) leads to the final *abc*-frame arm reference values transferred to the arm-individual modulators as depicted in Fig. 3.22.

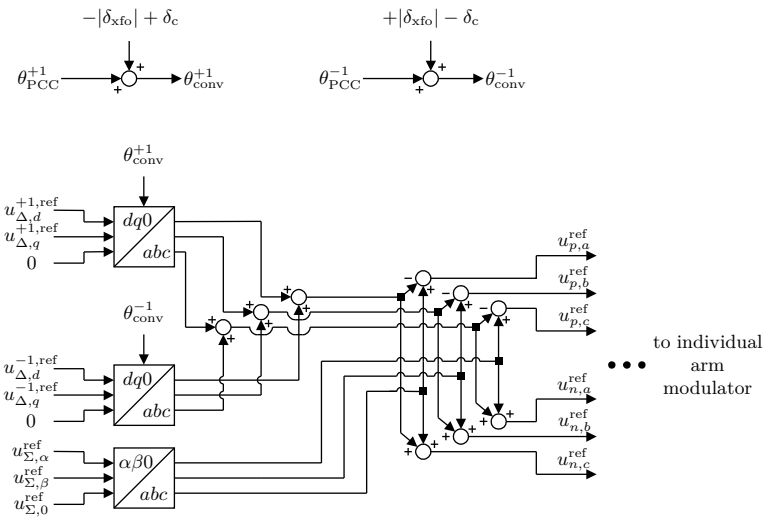

Figure 3.22: Determination of arm voltage references.

Cell Modulation

The intended use of the developed simulation framework prerequisites appropriate arm models as addressed within section 2.1.5 and accurate simulative replication of the modulation interface. As this may impact or even deteriorate system performance, effects like SM switching harmonics, intra-arm voltage distribution and overall number of switching actions need to be traceable.

As visualized in Fig. 3.23, translation of the requested arm reference voltage into SM-individual switching commands requires a multitude of steps divided into several functional blocks. First, input quantities are discretized by a sample and hold function (S&H) and delayed to artificially reflect the response speed of the control system. While reference voltage and measured arm current are immediately transferred to the NLC modulator and the switching logic block, additional intermediate steps are required related to the vector consisting of instantaneous measured SM voltages. To perform intra-arm voltage balancing it is necessary to sort corresponding values, which is integrated into the block labeled as indexer.

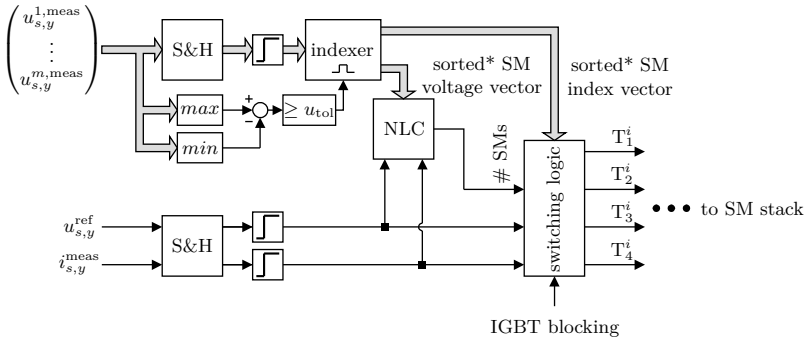

Figure 3.23: Cell modulation interface implementation utilizing a SM voltage tolerance band and NLC.

The following list briefly describes individual functionalities:

- **indexer**: Continuously transfers available SM information to following functions and periodically applies a triggered resorting of elements (order low to high SM voltages). Provided output includes a vector containing the sorted*[19] voltage information as well as a vector containing the corresponding SM index to ensure appropriate triggering of the desired SMs later on. As continuous resorting would lead to an excessive number of switching actions, the deviation between minimum and maximum SM voltage must exceed a selected threshold, which is defined by a tolerance band u_{tol}.

- **Nearest Level Control (NLC)**: This algorithm determines the number of SMs to be inserted based on the actual voltage information transferred by the indexer until the sum of SM voltages exceeds the requested reference value. The respected order or starting point (top or bottom element of voltage vector) depends on the direction of measured arm current and polarity of output voltage. The provided output is the number of SMs to be inserted.

- **switching logic**: This functional block translates available information into final switching commands for all IGBTs within the arm. Depending on the actual arm current direction, the insertion process either starts from the top or bottom of the sorted* SM index vector until the requested number of cells is inserted. With respect to the operational range of FB SMs, the polarity of the reference voltage is respected by either inserting the capacitor in positive or negative polarity.

[19] The transferred vector is only sorted accurately at the time instant a trigger signal has been received.

Chapter 4

Bipolar MMC-HVdc Fault Handling and Protection

4.1 Introduction to Fault Handling and Protection Realization

To fully utilize operational advantages related to FB SMs and unveil the intrinsic redundancy of a bipolar scheme with DMR, consisting of upper and lower subsystem, a sophisticated and well-coordinated fault handling and protection concept is required. To achieve correct discrimination and afterwards an adequate response to arbitrary faults, contingencies must be quickly detected, clearly localized and – in the case of control-wise measures – managed without violating safe operating area (SOA) boundaries.

This chapter introduces the developed multi-stage fault handling and protection concept able to differentiate between dc (pole-dependent, actively handled), internal (converter-dependent, leads to IGBT blocking) and ac (terminal-dependent, actively handled) faults. To additionally account for unforeseen malfunctions, a conventional SOA monitoring functionality with overriding priority is included as a backup. Furthermore, integration aspects of control-wise dc FCI and ac FRT measures are elaborated.

4.1.1 Literature Review

In congruence with higher complexity of system configurations, converter designs, fault handling as well as protection schemes proposed in literature have evolved. Furthermore, their sophistication has been modified related to underlying technical capabilities and operational requirements.

Conventional Protection and Fault Handling

For conventional symmetric monopolar HB MMC-HVdc applications, IGBTs are strictly blocked in the case of converter-internal or dc faults to protect power electronic devices triggered by criteria related to converter SOA constraints. Typically, those are arm overcurrents [22], SM voltage deviations from steady-state, dc over-/under-voltages as well as relatively slow dc pole voltage imbalance [133]. Subsequently, as the passivated converter acts as a diode rectifier, fault clearance requires ac circuit breaker operation within several grid-cycles. This limits, also with respect to thyristor-bypassed anti-parallel diodes for thermal reasons, achievable response speed prior to potential scheme restart. Nevertheless, the performance has been suitable for offshore wind power plant connectors or market coupling applications with in-feed levels well below the most severe contingency design-case of ac grids and mainly cable transmission[1]. Related to the ac grid, converters are generally capable of riding through faults. In this context, mostly double synchronous rotating reference frame control approaches following different current injection strategies related to positive and negative sequence voltage deviations are utilized, see for example [110, 3].

Utilization of Fault-Blocking SM Types

Triggered by demands for more powerful HVdc schemes, mainly related to embedded bulk-power interconnector projects [8], considerations to build bipolar links with partial or full OHL transmission segments evolved. To account for increasing fault likeliness along the transmission line, significantly faster dc FCI methods gained further interest. Initially, utilization of advanced SM types to interrupt fault currents subsequent to IGBT blocking, which is triggered by SOA violations as mentioned above, have been addressed. While [109] elaborates fault performance of a bipolar scheme based on CDSMs, detailed analysis of IGBT blocking behavior under various fault conditions for purely FB and a hybrid HB+FB solution are performed in [75] and [73]. But, even though these measures typically avoid ac circuit breaker operation and enable fast scheme restart, the intrinsic capability of advanced SM topologies to control-wise force fault currents to zero by opposing the output voltage polarity, including permanent (non-interrupted) STATCOM functionality, remains unexploited.

Selective Protection and Control-Wise DC Fault Handling

Consequently, following up the previous development stage, advanced FB dc fault handling strategies have been proposed to further boost operational flexibility

[1] It is furthermore assumed that occurrence of converter-internal and especially dc cable faults require additional inspections and diagnostic measures. This reduces the importance of a fast restart capability.

[17]. By actively reducing the dc fault current to zero, continuous reactive power provision and a controlled active power reduction can be achieved at the PCC (ac-side). Nevertheless, to be able to differentiate between dc and converter-internal contingencies, this requires an additional highly responsive and well-coordinated protection layer, e. g. based on derivative criteria (analysis of incoming traveling waves on the dc-side) as shown for example in [54]. Moreover, [103] analyzes dc fault detection including DMR involvement, [97] addresses detection of arc extinction time to minimize delays prior to reclosure and transmission power ramp-up in the case of non-permanent faults and [80] investigates specific characteristics of hybrid acdc lines including inter-system faults and related control aspects.

Reactive Current Injection during AC Grid Faults

The transition of power systems towards renewable generation and mainly power-electronic in-feed increases the necessity to promote supportive ac fault handling strategies. While conventional converter control schemes solely call for additional positive sequence reactive currents during faults, additional negative sequence components are required by recent grid codes as previously evaluated in section 2.3. Those specify a defined injection at the corresponding PCC, which is typically located on the grid-side of the converter transformer or even beyond as indicated in [48, 44]. Additionally, dynamic requirements related to overshoot and settling time are given but vary between different countries, while Germany imposes the most strict standards [41]. Even though available literature is rather detailed within the context of voltage support by wind turbines [105, 76] and voltage support in offshore wind power plants utilizing converter and turbines [92, 93], aspects related to the performance of bulk-power MMC-HVdc schemes embedded within a large transmission network remain disregarded.

4.1.2 Related Publications

The proposed protection and fault handling scheme within this thesis has been influenced by several publications. While the overall concept is closely related to an article published in *IEEE Transactions on Power Delivery* [Jrnl2018d], further insights are related to contributions presented within *Elsevier Electric Power System Research* [Jrnl2018b] and *IET Journal of Engineering* [Jrnl2018c].

4.2 Overview

An overview of implemented protection loops to locate or rather classify faults and trigger an appropriate handling strategy is shown in Fig. 4.1. As this comprises four main functional blocks the following sections are arranged accordingly.

Besides criteria directly linked to the protection zones defined within Fig. 3.2, where the outermost terminal of dc inductor and ac transformer represent the related boundary, continuous SOA monitoring serves as a backup. While faults within the dc network and ac grid are actively handled by converter controls, converter-internal faults and remaining cases, e.g. malfunctions during control-wise actions, lead to IGBT blocking and subsequent ac circuit breaker operation.

To achieve high selectivity, distinct criteria and a feasible set of thresholds must be determined. Due to fast dc current increase rates, leading to high overcurrents, mainly fast protection based on derivative criteria is utilized to trigger a rapid output current reduction by control-wise measures. In the case of converter-internal faults, a differential protection monitoring applied to various zones is proposed. This significantly minimizes detection time and reduces the undesired impact on the unaffected bipolar subsystem, typically referred to as the healthy part. During ac faults, detected by monitoring positive and negative sequence amplitudes, the converter injects reactive currents to influence grid voltages in the desired manner. Moreover, a backup-functionality realized by various SOA-related criteria guarantees protection of assets from irreversible damage.

4.3 Detection and Handling of DC Faults

Utilization of embedded bulk-power MMC-HVdc interconnectors increases requirements related to advanced dc fault handling. To remain operational flexibility, and especially to enable continuous reactive power support, control-wise dc FCI represents a desirable feature.

4.3.1 DC Fault Detection

To detect dc faults, current and voltage quantities on the dc network-side of the inductor are utilized, see Fig. 4.2. This incorporates: *i)* derivative methods as a critical rate of rise can be observed in the case of low-impedance faults and *ii)* common absolute value limits.

Furthermore, converter-internal faults within the opposite converter of a subsystem are also treated like dc faults. Here, the trigger is activated by a delayed signal indicating IGBT blocking of the opposite converter transmitted within a conservatively estimated timespan.

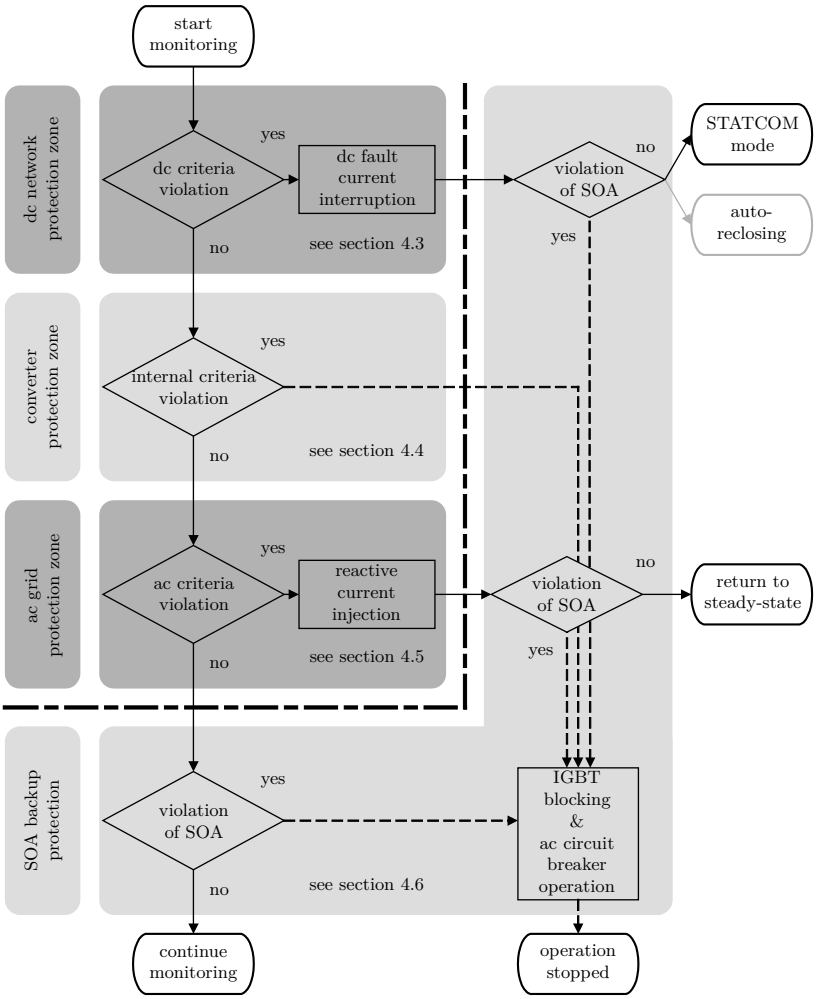

Figure 4.1: Fault classification and handling flowchart.

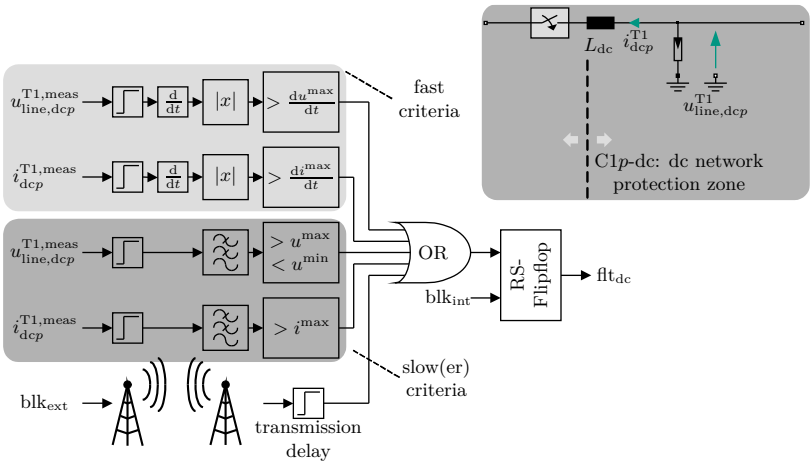

Figure 4.2: Protection loops related to the dc network protection zone, example given for upper converter C1p of Terminal T1.

du/dt-Loop and Threshold

Input to the voltage derivative loop is the measured pole to ground voltage located on the network-side of the dc inductor. For detailed protection studies, accuracy may include additional peripheral transfer functions, e.g. the voltage transformer (VT). This is followed by a delay to represent computational routines. Further, signal processing consists of a derivative function, absolute value determination and a comparator to identify threshold violations.

di/dt-Loop and Threshold

The derivative current loop utilizes the measured current on the network-side of the dc inductor as an input. Again, for detailed protection studies accuracy may include additional peripheral transfer functions, e.g. the current transformer (CT). Similar to the procedure described above, the signal is delayed, differentiated and its absolute value is compared to a previously defined threshold.

u-Loop and Threshold

This loop is designed to detect prolonged (typically non-transient) voltage drifts by comparing dc voltage with an extended operational range. This criterion might be triggered by high-impedance faults, which are not detected by derivative criteria or

by operational limitations of a distant station affecting the power balance within the dc network.

i-Loop and Threshold

Similar to the previous loop an additional dc overcurrent protection is included to account for insufficient derivative loop sensitivity. To select an appropriate threshold, coordination with the arm overcurrent loop, leading to immediate IGBT blocking, is essential.

Opposite Station Trip Indicator

Depending on severity, fault instant and pre-fault operation conditions converter-internal faults within the opposite converter do potentially not result in a noticeable impact (threshold violation) on local dc-side quantities and an immediate protection trigger[2]. To avoid long-term operation at an open line and more important to speed up restoration activities[3], a signal to indicate IGBT blocking within the opposite converter transmitted within a conservatively estimated timespan results in controlled dc current reduction, HVdc switch operation and subsequent line discharge by a grounding resistor. This enables, if retention in STATCOM mode is not desired, a coordinated reconnection, voltage ramp-up and power flow restoration of the affected subsystem.

4.3.2 DC Fault Current Interruption

Successful dc fault handling by control-wise measures relies on an immediate dc-side current limitation and a subsequent reduction. But, as also challenges related to ac current setpoint adaption as well as energy-balancing limitations emerge, additional aspects need to be considered and are discussed within this section.

Setpoint Adaption

Detection of a relevant contingency leads to immediate dc FCI. Here, regardless of pre-fault dc-side control mode, the dc current loop setpoint is immediately set to zero ($i_{\mathrm{phm},0} \propto \frac{i_{\mathrm{dc}}}{3} = 0$ A) as indicated in Fig. 4.3. By actively reducing or rather opposing the converter dc output voltage, utilizing the full operational flexibility

[2] To avoid any communication need significant threshold reductions are required to detect such events. As this significantly impacts selectivity related to the fact that faults within or close to a converter also lead to interactions affecting the healthy subsystem and unwanted trips, this option has been discarded.

[3] Assuming a non-permanent fault within the opposite converter occurred and power flow restoration is enabled.

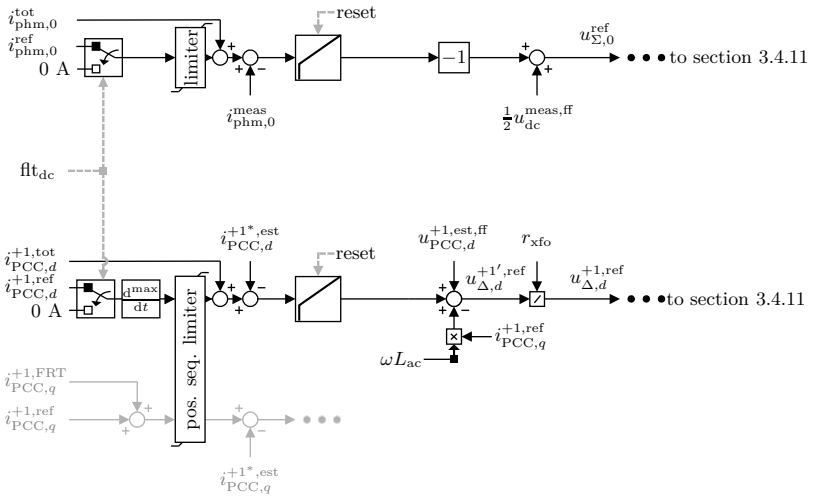

Figure 4.3: Setpoint adaptions related to dc FCI, see also Fig. 3.17 and Fig. 3.21.

of FB SMs, a rapid current reduction is achieved[4]. Due to the decoupled control capability of ac and dc currents, a smooth power output reduction can be realized on the ac-side by restricting the rate of change of power setpoint. Even though this degree of freedom is limited due to the selected SM capacitor sizing, dynamic impact on the ac system can be reduced as the ac current controller must not follow fluctuating power output on the dc-side.

If the related transmission corridor utilizes cable segments[5] priorly unrestricted FCI dynamics may have to be adapted. This is done by setting the lower controller limit – excluding the feed-forward voltage – to zero (avoid additional negative controller output voltages). Otherwise, this may affect overall reliability of cable assets and potentially shrinks the remaining lifetime.

[4]Resetting the $i_{\mathrm{phm},0}$ control loop integrator for several milliseconds after fault detection is recommended. Otherwise, as significant fault-related current surges may cause an integrator offset/drift, this delays full current interruption and HVdc switch operation.

[5]It is assumed that schemes utilizing only partial XLPE cable sections are also equipped with FB converters to gain a higher degree of controllability and enable auto-reclosure in the case of faults along the OHL.

Impact on Energy-Balancing

During dc FCI the energy-balancing capability of a converter is partially constrained. As operational setpoints are massively adjusted, a short term power imbalance is inevitable. Furthermore and compared to balanced operation as shown in Chapter 3, limitations related to total and horizontal balancing arise. Due to the resulting reduced degrees of freedom several corrective measures to improve dynamic performance during FCI, especially related to energy (re)distribution, become necessary.

In the case an affected converter has been balanced by adjusting $i^{\mathrm{tot}}_{\mathrm{phm},0}$ during conventional operation – this is likely for the P_{PCC}-Q_{PCC}-control mode where the requested power is provided at the PCC – detection of a dc contingency calls for a total balancing re-orientation towards the ac-side[6]. Furthermore, as the dc voltage drops to an insufficient level during most dc contingencies, the required power components for horizontal balancing cannot be provided and the corresponding loop is (temporarily) turned off until either a significant dc voltage returns or the converter enters dc-side isolated STATCOM mode and sets a predefined dc-side voltage. By reinspecting eq. (3.45) as well as eq. (3.46), those dependencies are directly traceable in the first terms

$$\bar{p}_{\Sigma,\alpha} = \underbrace{\overbrace{u_{\Sigma,0}}^{\approx 0} \cdot i^{\mathrm{dc}}_{\mathrm{phm},\alpha} \ldots}_{HOR\text{-}A}, \qquad \bar{p}_{\Sigma,\beta} = \underbrace{\overbrace{u_{\Sigma,0}}^{\approx 0} \cdot i^{\mathrm{dc}}_{\mathrm{phm},\beta} \ldots}_{HOR\text{-}A}. \tag{4.1}$$

[6] An u_{dc}-Q_{PCC}-controlled converter is already balanced by adapting the ac-side current $i^{+1,\mathrm{tot}}_{\mathrm{PCC},d}$. Therefore, no adaption is required.

Table 4.1: Impact of dc network faults on operation and energy-balancing.

dc fault type	total bal.	hor. bal.	vert. bal.	immediate operational impact
pole to ground	ac-side	off	on	power ramped down, enters STATCOM mode
pole to DMR	ac-side	off	on	power ramped down, enters STATCOM mode
DMR to ground	ac-side	on	on	enters rigid bipole mode
pole to DMR to ground	ac-side	off	on	power ramped down, enters STATCOM mode
pole to pole	ac-side	off	on	power ramped down, enters STATCOM mode
pole to pole to ground	ac-side	off	on	power ramped down, enters STATCOM mode

Within Table 4.1 impact of various dc fault types on balancing reconfiguration and related operational consequences are summarized. The procedure is rather straightforward as either one subsystem or the full bipolar scheme is affected, except for DMR to ground faults. As the latter fault type has no noticeable impact during typical bipolar operation, a smooth transition into the rigid bipolar mode[7] is possible without setpoint adaptions.

4.4 Detection and Handling of Converter-Internal Faults

The necessity to detect and clear converter-internal faults is primarily motivated by the desire to prevent severe hardware damage. But, with respect to increasing transmission capacities of bipolar schemes, high responsiveness with a minimized delay time gains importance. Reason for this is to limit interactions between upper and lower subsystem before multiple threshold violations in both converters occur, which reduces the risk of a full transmission capacity outage.

4.4.1 Internal Fault Detection

Detection of internal faults is based on a differential concept similar to an implementation indicated in [14]. Related to the highlighted current measurement positions[8] in total six converter-internal protection zones are defined, see Fig. 4.4. A fault is detected within one zone, if a deviation of overall current in- and outflow exceeds a given threshold. The latter choice is based on the accuracy of affected measurements and can be roughly estimated by

$$i_{\mathrm{pz}}^{\max} \geq \sum_{k=1}^{3\ldots4} |\Delta i_k| \tag{4.2}$$

where $|\Delta i_k|$ is the worst case measurement uncertainty (absolute value) at the k^{th} involved current measurement position under actual operation conditions. A detailed list of implemented protection zones, their unique IDs and the corresponding trigger criteria are provided within Table 4.2.

4.4.2 Internal Fault Handling

As internal faults impose a major risk to power-electronic assets immediate IGBT blocking is indispensable to commutate currents into anti-parallel diodes. This

[7] Controls of a rigid bipolar scheme differ substantially as the number of degrees of freedom is reduced by one per terminal. Due to the absence of a spare return conductor, the dc-side quantities within each terminal have to be consolidated.

[8] Marked current measurement positions in Fig. 4.4 are required to detect critical overcurrents.

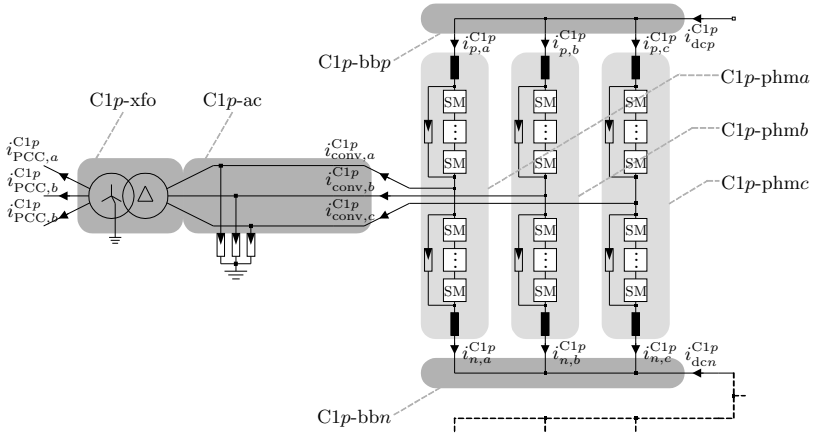

Figure 4.4: Converter-internal differential protection zones.

is executed independent of pre-fault operation and strictly outrules any control targets in the modulation layer. Due to the characteristics of FB SMs current flow through the converter arms is terminated, if the remaining magnetic energy within the fault current path is reduced. Except for high-voltage dc or midpoint busbar faults, which have an inevitable effect on other converters, this additionally interrupts current flow towards the dc-side or the other subsystem enabling continuous operation. Furthermore, return to mind that immediate provision of a large countervoltage leads to a charging process of SM capacitors as highlighted in section 2.1.3.

Table 4.2: Converter-internal differential protection trigger criteria.

protection Zone ID	condition
C1p-phm$a$	$\lvert + i_{p,a}^{\mathrm{C1}p} - i_{n,a}^{\mathrm{C1}p} - i_{\mathrm{conv},a}^{\mathrm{C1}p} \rvert > i_{\mathrm{pz}}^{\max}$
C1p-phm$b$	$\lvert + i_{p,b}^{\mathrm{C1}p} - i_{n,b}^{\mathrm{C1}p} - i_{\mathrm{conv},b}^{\mathrm{C1}p} \rvert > i_{\mathrm{pz}}^{\max}$
C1p-phm$c$	$\lvert + i_{p,c}^{\mathrm{C1}p} - i_{n,c}^{\mathrm{C1}p} - i_{\mathrm{conv},c}^{\mathrm{C1}p} \rvert > i_{\mathrm{pz}}^{\max}$
C1p-ac	$\lvert + i_{\mathrm{conv},a}^{\mathrm{C1}p} + i_{\mathrm{conv},b}^{\mathrm{C1}p} + i_{\mathrm{conv},c}^{\mathrm{C1}p} \rvert > i_{\mathrm{pz}}^{\max}$
C1p-bbp	$\lvert - i_{p,a}^{\mathrm{C1}p} - i_{p,b}^{\mathrm{C1}p} - i_{p,c}^{\mathrm{C1}p} + i_{\mathrm{dc}p}^{\mathrm{C1}p} \rvert > i_{\mathrm{pz}}^{\max}$
C1p-bbn	$\lvert - i_{n,a}^{\mathrm{C1}p} - i_{n,b}^{\mathrm{C1}p} - i_{n,c}^{\mathrm{C1}p} + i_{\mathrm{dc}n}^{\mathrm{C1}p} \rvert > i_{\mathrm{pz}}^{\max}$

From an ac grid perspective, the ac circuit breaker has to be additionally opened, which defines the response time to internal faults equal to several grid cycles[9]. This ensures interruption of fault currents fed from the ac-side in the case of contingencies between converter arms and secondary winding of the converter transformer.

4.5 Detection and Handling of AC Faults

Dynamic response of MMC-HVdc schemes related to faults within the ac grid is individually configurable as long as technical restrictions related to output current limits as well as energetic boundaries (an appropriate SM capacitor voltage range) are respected. But, facing significantly higher penetration levels of power electronics, these assets are required to support the ac grid during unbalanced voltage conditions as described in recent connection codes.

4.5.1 AC Fault Detection

Contingencies are identified by sequence voltage deviations compared to steady-state conditions and refer to quantities acquired at the PCC. As indicated in Fig. 4.5, outputs of the TM-CCF in $\alpha\beta$-frame are transformed into dq-frame, where instantaneous sequence magnitudes are calculated. Depending on the design of underlying positive and negative sequence voltage deadbands[10] additional reactive current injection is enabled. To avoid multiple activation/deactivation repetitions, especially during events leading to unbalanced conditions in close vicinity to the selected thresholds, it is recommended to implement a sufficient minimum hold or hysteresis characteristic prior to a state switch.

4.5.2 AC Fault Ride-Through

In line with an increasing share of power electronic assets requirements related to grid-supportive control actions during ac contingencies gain importance. Besides withstand capability related to distortions, a coordinated dynamic response must be ensured while energetic fluctuations stay within a feasible range.

Setpoint Adaptions

In the case of sequence voltage magnitude deviations from steady-state conditions ($|\underline{u}^{+1}_{\mathrm{PCC},dq}| \neq |\underline{u}^{+1,\mathrm{nom}}_{\mathrm{PCC},dq}|$,$|\underline{u}^{+1}_{\mathrm{PCC},dq}| \neq 0$ kV), the detection loops presented

[9] Appropriate scheme design considers an ac circuit breaker failure leading to additional time delays and equipment stress.

[10] A deadband is beneficial to overcome negative sequence voltage acquisition uncertainty, see also [91]. This is not necessarily required for the positive sequence component.

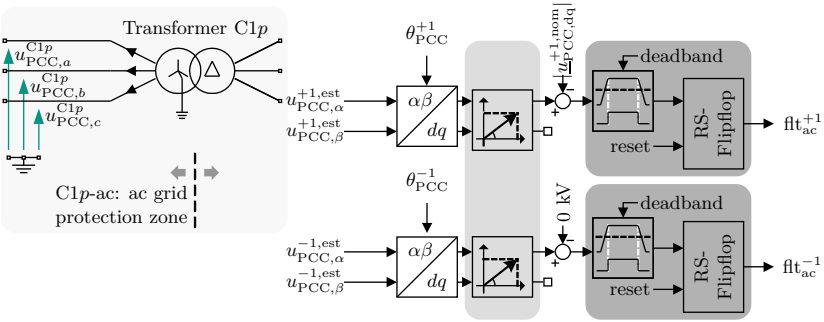

Figure 4.5: Protection loops related to the ac grid protection zone, example given for upper subsystem of Terminal T1.

within section 4.5.1 detect an ac contingency and immediately activate voltage stabilizing measures. This implies the behavior to boost/increase the remaining positive sequence and lower/suppress the negative sequence voltage by modifying the corresponding reactive current setpoints. In the process, loop sensitivity parameters are individually selectable, see [114] for a feasible range. This leads to the expressions

$$\Delta i^{+1,\mathrm{FRT}}_{\mathrm{PCC},q} = k_{i_q^{+1}} \cdot \frac{\left(|\underline{u}^{+1,\mathrm{est}}_{\mathrm{PCC},dq}| - |\underline{u}^{+1,\mathrm{nom}}_{\mathrm{PCC},dq}|\right)}{|\underline{u}^{+1,\mathrm{nom}}_{\mathrm{PCC},dq}|} \cdot |\underline{i}^{+1,\mathrm{max}}_{\mathrm{PCC},dq}| \tag{4.3}$$

and

$$\Delta i^{-1,\mathrm{FRT}}_{\mathrm{PCC},q} = -k_{i_q^{-1}} \cdot \frac{\left(|\underline{u}^{-1,\mathrm{est}}_{\mathrm{PCC},dq}| - 0\ \mathrm{kV}\right)}{|\underline{u}^{+1,\mathrm{nom}}_{\mathrm{PCC},dq}|} \cdot |\underline{i}^{-1,\mathrm{max}}_{\mathrm{PCC},dq}|, \tag{4.4}$$

where $|\underline{i}^{\pm 1,\mathrm{max}}_{\mathrm{PCC},dq}|$ represent maximum individual current magnitudes, $|\underline{u}^{+1,\mathrm{nom}}_{\mathrm{PCC},dq}|$ corresponds to the steady-state positive sequence voltage magnitude, $|\underline{u}^{\pm 1,\mathrm{est}}_{\mathrm{PCC},dq}|$ are the estimated sequence voltage magnitudes and $k_{i_q^{\pm 1}}$ define the sensitivity. To trace the current component determination in eq. (4.4), which aims to suppress the appearing negative sequence voltage during unbalanced conditions, two issues need to be highlighted. First, reactive currents solely consists of an $i_q^{\pm 1}$ current component. This is due to the realized (sequence-individual) alignment ensured by the additional PLL in the case of unbalanced conditions. Second, as negative sequence controls are realized by a backward rotating $dq0$-frame, the negative sign is introduced to obtain a suppressive behavior, see [83] and Appendix A.2[11].

[11] Note that a backward rotating $dq0$-frame is equivalent to the complex conjugate negative sequence in symmetrical components as derived in [124], indicated in [76] and trackable in the

On an operational layer, reactive currents are typically prioritized by the converter ac current controller and quickly reach significant levels. This potentially affects the remaining power transfer capability along the link. In the case of low-impedance ac faults, leading to a severe voltage drop at the PCC, the remaining transmission capacity is either limited or even set to zero. To provide an overview, operational changes during different fault conditions are listed in Table 4.3. This provides insights into reference value adaption, details related to negative sequence rotating reference frame alignment and potential impact on remaining power transmission capability.

Furthermore, an impact beyond directly adjacent converters exists. It must be ensured that a link or even an arbitrary dc network is capable to follow related operational changes either by appropriate intrinsic behavior or adapted outer control loops. For a conventional link scenario, assuming each bipolar subsystem consists of one dc voltage-controlled and one power controlled terminal, this implies that:

- An ac fault in close vicinity to the power controlled terminal leads to a dc output current reduction caused by prioritized injection of reactive currents and subsequent transmission capacity reduction. The resulting immediate power input to output mismatch is automatically equalized as the dc voltage control loop of the opposite terminal provides an intrinsic balancing functionality as long as each converter stays within its operational boundaries.

appendix of [117].

Table 4.3: Impact of ac grid faults on operation.

ac fault type	$\Delta i_{\mathrm{PCC},q}^{+1,\mathrm{FRT}}$	$\Delta i_{\mathrm{PCC},q}^{-1,\mathrm{FRT}}$	$\theta_{\mathrm{PCC}}^{-1}$	immediate impact on power transmission (if applicable)
three-phase to ground	yes	no	$\theta_{\mathrm{stdy}}^{-1}$	temporary reduction
two-phase to ground	yes	yes	$\theta_{\mathrm{dyn}}^{-1}$	temporary reduction
two-phase	yes	yes	$\theta_{\mathrm{dyn}}^{-1}$	temporary reduction
single-phase to ground	yes	yes	$\theta_{\mathrm{dyn}}^{-1}$	temporary reduction

- An ac fault in close vicinity to the dc voltage-controlled terminal leads to an immediate dc output current restriction. Due to the potential mismatch between dc input and output current setpoints at both terminals a dc voltage drift occurs. A new stable operating point can be determined by a voltage droop functionality, which introduces $\Delta P_{\mathrm{PCC}}^{\mathrm{ref}}$ at the power controlled terminal to pass into a new global power equilibrium.

Impact on Energy-Balancing

Depending on ac fault type and severity, the extent of energetic deviations is affected by both acquisition phenomena (settling time of PLL or rather TM-CCF based sequence estimation) as well as dynamic setpoint adaptions due to different control loop dynamics. While the horizontal energy-balancing capability remains intact, aspects of vertical and restrictions related to total balancing require further discussion.

For total balancing a separate analysis depending on the pre-fault converter control mode is required. Again, a conventional link scenario is considered. This leads to the fact that:

- An ac fault in close vicinity to the power controlled terminal does not lead to an immediate adaption need. Both converters are already balanced in mode *TOT-B*, where a component $i_{\mathrm{phm},0}^{\mathrm{tot}}$ is superimposed on the dc current reference $i_{\mathrm{phm},0}^{\mathrm{ref}}$. Subsequently, occurring power deviations are automatically leveled out by the dc voltage-controlled terminal.

- An ac fault in close vicinity to the dc voltage-controlled terminal requires a switchover to *TOT-B* total balancing mode. Moreover, the outer dc voltage control loop is halted and maintains the pre-fault steady-state current reference. If applicable, reactive current prioritization even further reduces this limit. As both stations are de-facto current controlled, the likely power mismatch results in a voltage drift. A new stable operation point is determined by means of an appropriate droop implementation at the opposite terminal or within a more complex dc network.

The implemented vertical balancing strategy implies balanced voltage conditions and is otherwise turned off, as emphasized in section 3.4.6. Reminiscing eqs. (3.47a)-(3.49a), where terms depending on positive and negative sequence voltages are separated, four main aspects shall be highlighted to underpin this decision. These are: *i)* The occurence of a negative sequence voltage deteriorates balancing performance of the realized concept, as coupling between power components is introduced. E.g. the positive sequence current also has an impact on $\bar{p}_{\Delta,\alpha}$ and $\bar{p}_{\Delta,\beta}$. *ii)* Further, uncertainties exist related to positive and negative sequence magnitude as well as phase angle estimation. *iii)* The remaining reduced sequence

Table 4.4: Impact of ac grid faults on energy-balancing.

ac fault type	total bal.	hor. bal.	vert. bal.	remark
three-phase to ground	dc-side	yes	yes	balanced ac-grid voltage conditions; remaining vertical balancing capability; potentially restricted by current limits in the case of very low residual sequence voltage amplitudes
two-phase to ground	dc-side	yes	no	unbalanced voltage conditions, vertical balancing turned off
two-phase	dc-side	yes	no	unbalanced voltage conditions, vertical balancing turned off
single-phase to ground	dc-side	yes	no	unbalanced voltage conditions, vertical balancing turned off

voltages cause increasing current amplitudes. *iv*) No permanent vertical energy drifts are caused by converter currents responsible to ensure power exchange[12]. With respect to the above highlighted aspects, Table 4.4 summarizes elaborated findings for typical ac contingencies. This includes an overview of remaining balancing loops as well as a short explanatory remark.

4.6 Backup Protection by Safe Operating Area Monitoring

Beyond the previously introduced protection loops, which have been designed to detect faults located in specific zones, an additional backup-functionality is indispensable. Activation is triggered by SOA violations and leads to IGBT blocking under all circumstances. Criteria are either motivated by grid code imposed or technical constraints.

The following list names all decisive aspects, which are permanently monitored, leading to IGBT blocking:

- Operation is interrupted if the lowest/highest ac phase-to-phase voltage violates the specified low-voltage/high-voltage FRT profile stated in the applicable grid code.

- Operation is interrupted if the system frequency exceeds limits stated in the applicable grid code.

[12] In [94], but beyond the scope of this thesis, an extended vertical balancing scheme has been presented to account for unbalanced voltage conditions. Here, utilization of a second harmonic ac zero sequence voltage is proposed to gain an additional degree of freedom in order to influence $\bar{p}_{\Delta,\alpha/\beta/0}$- components.

- Operation is interrupted if converter arm currents increase up to levels beyond the specified peak current threshold given by the manufacturer.
- Operation is interrupted if voltages of operational SMs are beyond the selected upper/lower boundaries. This ensures both permanent controllability of converter currents due to a sufficient minimum voltage reserve stored within all SMs and avoidance of SM failures due to critically high charging states leading to capacitor or IGBT failures.

Chapter 5

Bipolar MMC-HVdc Design Aspects

5.1 Introduction to Scheme Design Realization

Design of MMC-HVdc schemes strongly depends on detailed technical requirements and includes manufacturer-specific solutions. Therefore, generic models are a beneficial tool to support accompanying quality assurance for mainly two reasons. First, if neither specifications are finalized nor the supplier of a project is decided, generic models provide an attractive possibility to perform preliminary system studies. Second, generic models overcome restrictions introduced by intellectual property issues leading to inaccessible (black-boxed) features. But, to ensure general feasibility of results, careful selection of a large set of technical parameters is required. This chapter discusses and summarizes general design aspects related to a bipolar FB MMC-HVdc link with DMR.

5.2 Overview

In Fig. 5.1 a schematic overview of the investigated generic bipolar FB MMC-HVdc link with DMR is provided. Corresponding terminals, where terminal T1 is located on the left and operates in power control mode while T2 is located on the right and operates in dc voltage control mode, are interconnected by a 700 km long OHL. Furthermore, placement of inductors, grounding electrode, HVdc switches, ac circuit breakers and surge arrestors are indicated.

Prior to simulations provided in Chapter 6, investigated fault locations, their corresponding IDs and relevant dc quantities are highlighted.

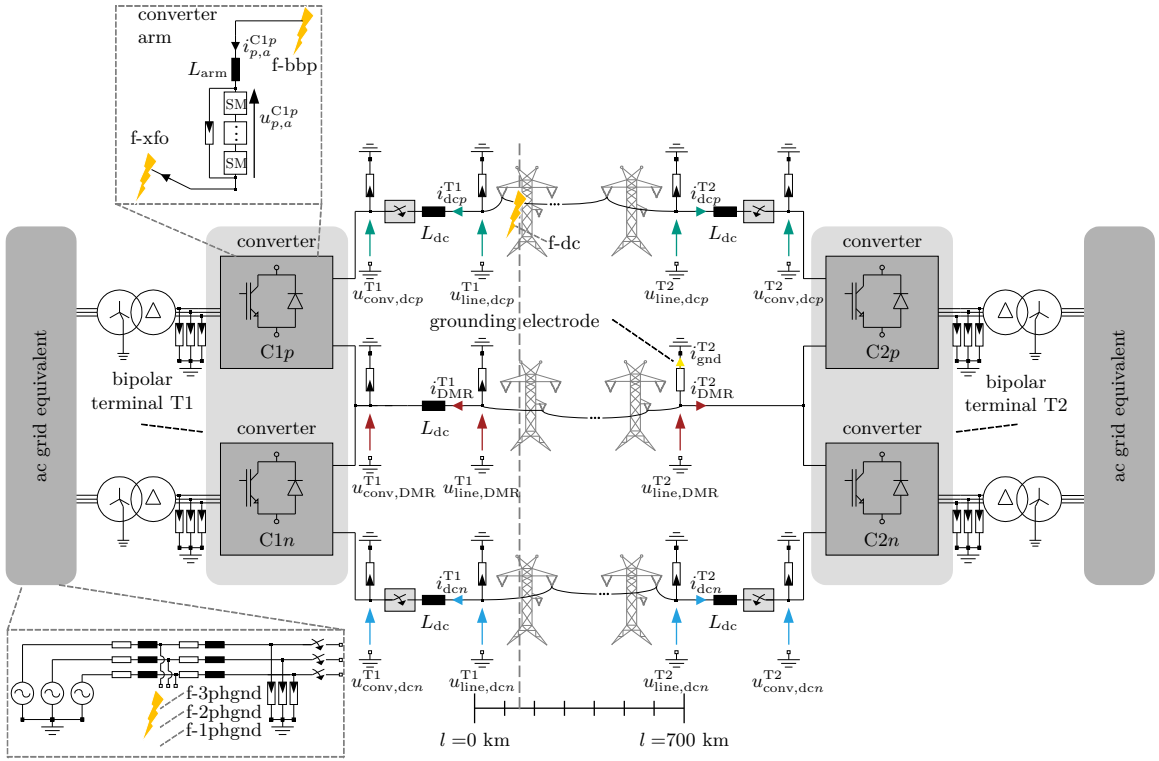

Figure 5.1: Schematic of investigated bipolar MMC-HVdc link including investigated fault locations.

5.3 Scheme Design Determination

This section provides the main parameters related to the overall scheme design and discusses the purpose of individual components.

5.3.1 Transmission Capacity

The recent intention to boost individual scheme ratings beyond one gigawatt has been triggered by various reasons. Those are, besides an increasing demand for more powerful interconnectors to improve trading-potentials, needs for large-scale embedded power transmission schemes to relief heavily overloaded ac grid corridors and avoid renewable curtailment. Recently, existing technical limitations have been overcome and recent advances in power electronics, converter station design and HVdc equipment (e.g. cross-linked polyethylene (XLPE) cables and accessories, gas-insulated switchgear) enable overall transmission capacities of around two gigawatts per link. In particular, this is due to increasing dc voltage ratings up to 525 kV and extended IGBT current capabilities[1].

5.3.2 Terminal and Converter Specification

The specifications of bipolar terminals and corresponding converters need to reflect steady-state as well as dynamic operational requirements. Furthermore, if required device withstand capabilities are appropriately defined, stresses related to characteristic contingencies are considered. This ensures short repair downtimes due to an avoidance of extensive damage involving multiple parts.

DC Network Interface

The inductors at the high-voltage poles mark the electrical termination towards the dc network and mainly fulfill two purposes. First, in coordination with arm inductors, rate of current rise is limited. This ensures stresses on converter equipment remain at non-critical levels and full controllability is maintained, which is even more important for the proposed advanced FB operation. Second, selectivity related to current derivative protection criteria is improved, as a more clear differentiation between traveling waves originating from the dc-side and interactions transferred through the bipolar terminal is supported. In series to the inductors, the HVdc switch[2] is located. This device is capable to isolate the adjacent converter from the HVdc network after successful dc FCI.

[1] Recent trends in the IGBT market (e.g. *ABB SNA 300k452300* and [104]) already indicate further potential.

[2] As non-ideal current interruption leads to remaining currents of several amperes, a limited interruption capability is required for this device.

Therewith aligned, horizontal balancing capability is regained as the converter sets a predefined dc-side output voltage and enters STATCOM mode.

While this solely presents one possibility to design post-fault sequences, the following aspects are highlighted for the sake of completeness. In the case of an OHL scheme, there is a high probability of non-permanent single pole to ground faults. Switch to STATCOM mode might be stalled until several restart attempts have failed, as addressed in [97], indicating the existence of a permanent fault. Furthermore, an extended dc yard arrangement enabling a reconfiguration to asymmetric monopolar configuration or rigid bipolar configuration provides additional flexibility related to redundancy aspects. This requires the possibility to bypass individual converters and connect lines in parallel for asymmetric operation or to isolate a faulty line and switch to rigid bipolar operation. If one high-voltage conductor is faulty, the former option requires a DMR with full voltage rating.

Converter Arms and Submodules

Design of converter equipment must reflect system losses. Typically, the dc voltage-controlled terminal provides line and converter losses (superscript loss) as well as auxiliary supply and transformer losses at the opposite terminal (subscripts are accordingly named line, conv, aux, xfo). Furthermore, reactive power consumption of the converter transformer is excluded in specified maximum PCC in-feed, which is valid for both sides. To obtain resulting specification values, this leads to the corrected nominal converter active and reactive power capability estimations

$$P_{\mathrm{conv}}^{\mathrm{nom}} = P_{\mathrm{PCC}}^{\mathrm{nom}} + P_{\mathrm{line}}^{\mathrm{loss}} + 2 \cdot P_{\mathrm{conv}}^{\mathrm{loss}} + 1 \cdot P_{\mathrm{aux}}^{\mathrm{loss}} + 1 \cdot P_{\mathrm{xfo}}^{\mathrm{loss}} \tag{5.1}$$

and

$$Q_{\mathrm{conv}}^{\mathrm{nom}} = Q_{\mathrm{PCC}}^{\mathrm{nom}} + Q_{\mathrm{xfo}}^{\mathrm{loss}}. \tag{5.2}$$

Other important aspects related to the performance of HVdc schemes are sizing and placement of arm inductors. Besides needs related to dynamic performance, a significant impact on voltage and current stresses at different locations exists. By installing the inductor between high-voltage busbar or midpoint and SM stack, decoupling of dc contingencies can be improved [57]. Consequently, propagation of fast blocking impulses towards the dc-side as well as effects of incoming traveling waves on power electronic equipment are further attenuated[3].

Subsequently, to determine the number of required SMs various aspects must be considered:

[3]Note that these effects gain even more importance if cable transmission segments are utilized.

- Unrestricted controllability of MMCs is only maintained as long as instantaneous arm sum voltages $u_{s,y}^{\Sigma}$ are greater or equal than the requested reference voltages by the controller $u_{s,y}^{\mathrm{ref}}$. The boundary can be approximated in a simplified manner by $\max(u_{s,y}^{\mathrm{ref}}) \approx u_{\mathrm{dc}}^{\mathrm{nom}}/2 + \hat{u}_{\mathrm{conv}}^{+1,\mathrm{nom}}$, see Fig. 3.2.

- Assuming a given capacitor size due to standardized configuration of SMs, fluctuations of arm sum voltages during conventional operation must be additionally reflected.

- Further uncertainties exist related to average switching frequency minimization by introducing a SM voltage tolerance band, diminishing SM redundancy between scheduled maintenance events, varying ac- and dc-side voltages as well as deviations during and subsequent to contingencies.

To provide a basic idea of arm sum voltage behavior over time, assuming ideal intra-arm balancing (infinite sorting and switching speed), several link load flow cases named Case1-Case3 have been investigated and are shown for a converter of the voltage-controlled terminal T2 in Fig. 5.2 (a). The simulation utilizes the final scheme design consisting of 270 SMs per arm with a capacitor size of 8.5 mF operated at an average voltage of 2.5 kV and considers load flow cases given in Table 5.1. Assuming a maximum rated SM voltage of 4.5 kV, this is considered feasible according to [4]. To validate model performance, Case1 is compared against calculated arm sum voltage fluctuations according to [39][4], where arm inductor and resistive voltage drops are added to improve accuracy. To broaden this perspective, Fig. 5.2 (b) and (c) visualize maximum and minimum SM voltage deviations for an arbitrary operation setpoint in the case of nominal ac- and dc-side voltages. This information provides a valuable indication to determine the adequacy of selected SM capacitors and built-in redundancy.

Table 5.1: Scheme load flow scenarios and corresponding individual converter setpoints.

case ID	in-feed P_{PCC} (on T1-side)	in-feed Q_{PCC} (both sides)	resulting P_{conv} (on T2-side)	resulting Q_{conv} (on T2-side)
Case1	+1050 MW	+400 MVAr	-1140 MW	+620 MVAr
Case2	-1050 MW	0 MVAr	+987.5 MW	+137 MVAr
Case3	+300 MW	-200 MVAr	-317 MW	-172.5 MVAr

[4] Note that ac and dc voltages are subject to fluctuations and do not necessarily equal nominal values, e.g. converter ac voltage amplitudes change related to the selected reactive power setpoint.

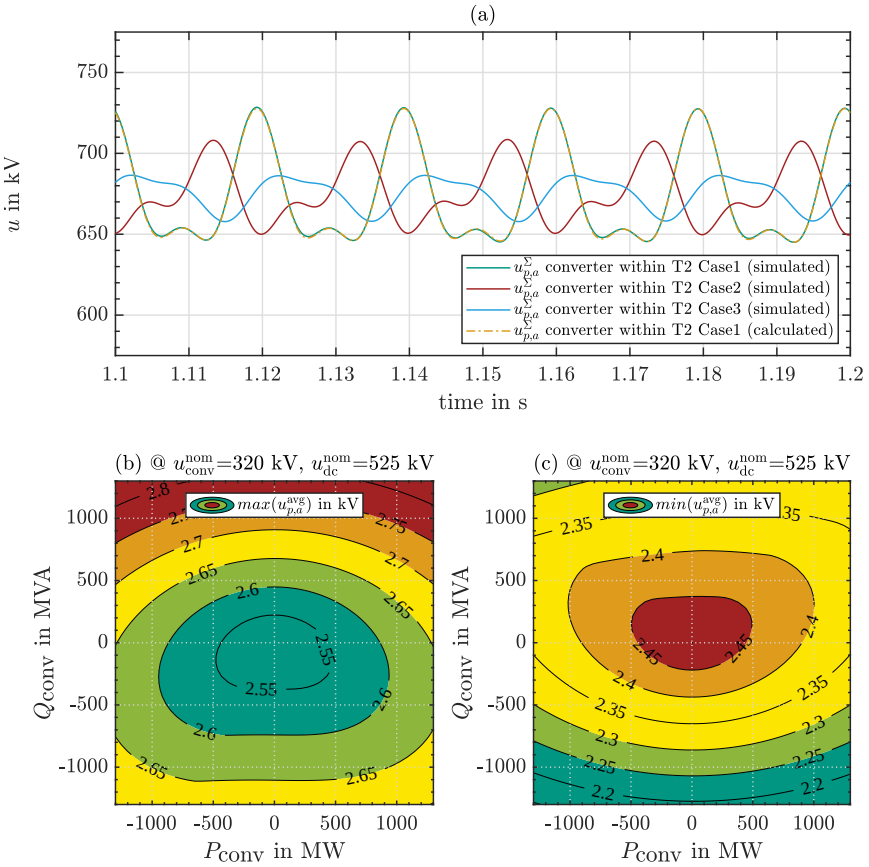

Figure 5.2: Impact of load flow setpoints on arm sum voltage fluctuations and average SM voltage extremes under nominal voltage conditions:
(a) converter arm sum voltage over time at T2,
(b) maximum average SM voltage depending on converter load flow setpoint,
(c) minimum average SM voltage depending on converter load flow setpoint.

AC Grid Interface

Similar to considerations provided for the dc network interface, ac FRT capability of a converter requires a sufficiently high impedance (sum of effective arm and ac-side inductances) for decoupling reasons. In the case of bipolar HVdc schemes, as reflected in eq. (3.6), an additional need for galvanic separation leads to utilization of a typical wye-delta HVdc transformer configuration[5]. While overall apparent power needs exceed available three-phase transformer ratings, single-phase units are utilized and connected accordingly. To avoid transformer core saturation and overload, an overrating of transformer basic insulation level and apparent power is recommended to account for control delays, especially subsequent to voltage recovery after ac contingencies. Furthermore, to supply peripheral equipment as well as cooling facilities, an additional medium-voltage winding is present. To fully isolate the converter during maintenance and subsequent to converter-internal or transformer faults, circuit breakers are located on the grid-side of the transformer.

Parameter Overview

Within the following Tables 5.2-5.4, specifications of dc network interface, converter as well as ac network interface are provided. Furthermore, Table 5.5 presents selected current limits related to power exchange, reactive current injection and various balancing task requirements.

Table 5.2: Specification of dc network interface.

description	parameter	value
nominal dc voltage (pole to ground)	$u_{\mathrm{dc}}^{\mathrm{nom}}$	$\pm$ 525 kV
nominal dc current	$i_{\mathrm{dc}}^{\mathrm{nom}}$	2.10 kA
dc inductor	L_{dc}	25 mH
grounding electrode resistance	R_{gnd}	0.7 Ω

[5] Due to the mixed ac and dc stresses on the converter-side, transformer design differs related to conventional ac insulation and bushings realizations as described in [20].

Table 5.3: Specification of converters.

description	parameter	value
rated apparent power per converter	$S_{\text{conv}}^{\text{nom}}$	1300 MVA
nominal converter-side ac voltage	$u_{\text{conv}}^{\text{nom}}$	320 kV
arm inductor	L_{arm}	50 mH
SMs per arm	m	270
SM capacitor	C_{SM}	8.5 mF
SM IGBT/diode on-state resistance	R_{on}	3 mΩ
SM maximum rated voltage	$u_{\text{SM}}^{\text{max}}$	4.5 kV
SM operational voltage (nominal)	$u_{\text{SM}}^{\text{nom}}$	2.5 kV
ratio of stored energy and apparent power	-	33.1 $\frac{\text{kJ}}{\text{MVA}}$

Table 5.4: Specification of ac grid interface.

description	parameter	value
rated converter apparent power at PCC (in P_{PCC}-Q_{PCC}-control mode)	$S_{\text{PCC}}^{\text{nom}}$	1200 MVA
nominal grid-side ac voltage	$u_{\text{PCC}}^{\text{nom}}$	400 kV
rated converter transformer apparent power (sum of single-phase units)	$S_{\text{xfo}}^{\text{nom}}$	1400 MVA
transformer vector group	-	YNyn0d11
leakage reactance (base $S_{\text{xfo}}^{\text{nom}}$)	$X_{\text{xfo,1-3}}$	0.2 p.u.
leakage reactance (base $S_{\text{xfo}}^{\text{nom}}$)	$X_{\text{xfo,1-2}}$	3.0 p.u.
leakage reactance (base $S_{\text{xfo}}^{\text{nom}}$)	$X_{\text{xfo,2-3}}$	2.4 p.u.
ac grid short circuit power	S''	45 GVA
ac grid X/R ratio	-	10

Table 5.5: Specification of individual current component limits.

description	limit	value	remark
ac-side (pos. seq.)	$\pm\lvert i_{\mathrm{PCC},dq}^{+1,\max}\rvert$	2.5 kA	defined by converter operation range
ac-side (neg. seq.)	$\pm\lvert i_{\mathrm{PCC},dq}^{-1,\max}\rvert$	0.8 kA	additional dynamic current margin
dc-side (u_{dc}-control mode)	$\pm i_{\mathrm{phm},0}^{\max}$	1.0 kA	maximum in u_{dc}-control mode
dc-side (P_{PCC}-control mode)	$\pm i_{\mathrm{phm},0}^{\max}$	n/a	linked to remaining PCC active power capability
total balancing mode TOT-A	$\pm i_{\mathrm{phm},0}^{\mathrm{tot,max}}$	0.5 kA	-
total balancing mode TOT-B	$\pm i_{\mathrm{PCC},d}^{+1,\mathrm{tot,max}}$	1.5 kA	-
horizontal balancing	$\pm i_{\mathrm{phm},\alpha/\beta}^{\mathrm{hor,max}}$	0.8 kA	-
vertical balancing	$\pm i_{\mathrm{phm},d/q}^{\pm 1,\mathrm{ver,max}}$	0.8 kA	-

5.3.3 Overheadline Tower and Conductor Arrangement

The utilized OHL configuration and transmission tower arrangement are presented within Fig. 5.3. Besides two ground wires at a height of 47 m, both pole conductors – realized by a bundle of four subconductors – are located at a height of 33.5 m, while pole to pole distance equals 16 m. The DMR, which is carried out with full current and voltage rating, is located at a height of 25.5 m. Single conductor type is Chukar with a diameter of 32.83 mm. This results in $R_{\mathrm{dc}}^{'} = 51.14$ mΩ/km of a single conductor.

5.3.4 Overvoltage Protection

The arrangement of surge arrestors within HVdc schemes is an essential design aspect. To avoid excessive insulation coordination requirements for utilized equipment, which also affects overall investment costs, it is required to limit occurring overvoltages by means of surge arrestors. As previously indicated in Fig. 3.2 and Fig. 5.1, this includes devices close to the converter transformer, across the converter arms to limit SM overcharging, at the dc poles as well as at the terminal midpoint. The latter two positions include separate arrestor banks on both sides of the dc inductors.

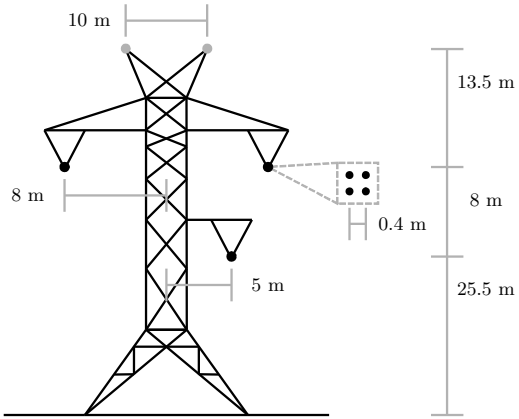

Figure 5.3: Schematic of overheadline tower and conductor arrangement.

Consequently, stresses must be limited to values lower than the designed withstand voltages, see [118]. In Tab. 5.6, residual arrestor voltages are given related to the nominal operating voltages at different positions. The selected design considers appropriate leakage current dimensions during normal operation to avoid thermal runaway. The underlying non-linear voltage-current characteristics of a single metal-oxide arrestor column based on a 30/60 µs current impulse is given in Appendix E. A parasitic inductance of 15 µH is connected in series to each arrestor bank to account for lead wire impacts.

Table 5.6: Specification of surge arrester arrangement. Residual voltage in p.u. (per unit) based on the nominal operating voltage.

location	nominal voltage	residual voltage at discharge current	remark
dc pole	525 kV	1.64 p.u. @ 1 kA	-
dc midpoint	90 kV	1.64 p.u. @ 1 kA	-
SM stack	1215 kV	0.81 p.u. @ 1 kA	equals $m \cdot u_{\mathrm{SM}}^{\mathrm{max}}$
ac conv.-side	560 kV	1.64 p.u. @ 1 kA	offset $u_{\mathrm{dc}}/2$
ac grid-side	327 kV	1.64 p.u. @ 1 kA	-

5.4 Control Parameter Determination

This section provides insights into the determination of control parameters in close relation to Chapter 3. Hence, filters (if applicable), signal acquisition, control and modulation delays are addressed.

5.4.1 Current Control Loops

Derived current control parameters respect a control and modulation processing delay of $T_{\sigma,\mathrm{c}} + T_{\sigma,\mathrm{m}} = 40$ µs. Furthermore, to account for limited data processing speed, an additional acquisition delay of $T_{\sigma,\mathrm{a}} = 20$ µs is considered for all measured or estimated quantities. Utilizing the corresponding inductors within the individual control loops (values are given in section 5.3.2) parameters according to Table 5.7 are obtained.

5.4.2 Phase-Locked Loop

Parametrization of the PLL shows a significant impact on general dynamic performance and robustness of HVdc operation in response to ac contingencies. As recommended in [25], to achieve fast settling time and high disturbance rejection capability, crossover frequency ω_{co} and ξ ($g = 2\xi + 1$) are selected as $2\pi 20$ rad/s and 0.7, respectively. This leads to PLL parameters and MCCF cutoff frequency ω_c presented in Table 5.8. Note that the input to both PLLs is a normalized voltage. While the positive sequence PLL is normalized to the nominal voltage at the PCC, the negative sequence PLL is normalized to the selected activation threshold for reactive current injection, see Fig. 3.7.

5.4.3 Balancing Control Loops

As derived in section 3.2 and highlighted in [47], MMC energetic quantities contain fluctuating terms. Hence, while these do not deviate mean energy values, their impact on balancing controllers must be suppressed by appropriate signal filters. Instead of solutions utilizing notch structures, which appear vulnerable to severe frequency deviations, low-pass filters present an adequate alternative[6].

Besides twice the underlying current control and modulation delay (80 µs), energy loop control as well as acquisition delay (40 µs) and estimated filter time constants are required. Based on 4^{th} order butterworth realizations, where heuristically tuned cut-off frequencies correspond to 60 Hz ($E_{\Sigma,0}$), 50 Hz ($E_{\Sigma,\alpha/\beta}$) and 20 Hz ($E_{\Delta,\alpha/\beta/0}$), corresponding time constants equal 12.18 ms, 14.38 ms and 35.28 ms, respectively. Considering further nominal values stated in the previous sections

[6] While active power setpoints are coupled between ac- and dc-side, and a feed-forward of horizontal deviations exists, overall dynamic requirements for energy controllers are less strict.

and the assumption that $a = 2$ related to the *symmetrical optimum method*, balancing control parameters according to Table 5.9 are obtained.

5.4.4 Outer Control Loops

Remaining parameters are related to outer control loops. For scheduled active and reactive power changes dynamic requirements are generally uncritical and enable a conservative controller tuning, see the upper part of Table 5.10. In contrast, the dc voltage controller must be carefully designed to minimize the impact of disturbances on scheme transmission performance as highlighted in section 3.4.3. Assuming an underlying current control and modulation delay of 80 µs and a dc voltage control, acquisition and filter delays of approximately 75 µs, parameters presented in the lower part of Table 5.10 are obtained. Here, the associated OHL and dc filter capacitance (20 nF) is respected to calculate $C_{\mathrm{dc}}^{\mathrm{eqv}}$. Furthermore, to filter the instantaneous dc power transferred towards the ac-side for reference current calculation reasons, a second order low-pass filter with a cut-off frequency of 1 kHz is applied.

Table 5.7: Determined current control loop parameters.

controller	parameter	reference	value	remark
$i_{\mathrm{phm},0}$	k_{p}	-	$1.11{\cdot}10^{+1}$	see section 3.4.8
$i_{\mathrm{phm},0}$	T_{i}	-	$6.76{\cdot}10^{-2}$	see section 3.4.8
$i_{\mathrm{phm},\alpha/\beta}$	k_{p}	eq. (3.97)	$4.16{\cdot}10^{+2}$	-
$i_{\mathrm{phm},\alpha/\beta}$	T_{i}	-	∞	tracking by balancing loops
$i_{\mathrm{PCC},d/q}^{+1}$	k_{p}	eq. (3.106)	$9.31{\cdot}10^{+2}$	-
$i_{\mathrm{PCC},d/q}^{+1}$	T_{i}	-	$3.00{\cdot}10^{-3}$	typical range, see [85, 82]
$i_{\mathrm{PCC},d/q}^{-1}$	k_{p}	eq. (3.106)	$7.39{\cdot}10^{+2}$	-
$i_{\mathrm{PCC},d/q}^{-1}$	T_{i}	-	$3.00{\cdot}10^{-2}$	sequence decoupling

Table 5.8: Determined PLL control loop parameters.

controller	parameter	reference	value	remark
PLL	k_p	eq. (3.56)	$1.25{\cdot}10^{+2}$	-
PLL	T_i	eq. (3.56)	$1.52{\cdot}10^{-4}$	-
MCCF	ω_c	eq. (3.56)	$3.02{\cdot}10^{+2}$	MCCF cutoff frequency

Table 5.9: Determined balancing control loop parameters.

controller	parameter	reference	value	remark
$E_{\Sigma,0}$	k_p	eq. (3.73)	0.155	mode TOT-A
$E_{\Sigma,0}$	T_i	eq. (3.74)	0.318	mode TOT-A
$E_{\Sigma,0}$	k_p	eq. (3.76)	0.493	mode TOT-B
$E_{\Sigma,0}$	T_i	eq. (3.77)	0.100	mode TOT-B
$E_{\Sigma,\alpha/\beta}$	k_p	eq. (3.80)	0.131	-
$E_{\Sigma,\alpha/\beta}$	T_i	eq. (3.81)	0.442	-
$E_{\Delta,\alpha/\beta/0}$	k_p	eq. (3.86)	0.054	-
$E_{\Delta,\alpha/\beta/0}$	T_i	eq. (3.87)	2.582	-

Table 5.10: Determined outer control loop parameters.

controller	parameter	reference	value	remark
P_PCC	k_p	eq. (3.65)	1	-
P_PCC	T_i	-	$1.60{\cdot}10^{-1}$	heuristically tuned
Q_PCC	k_p	eq. (3.65)	1	-
Q_PCC	T_i	-	$4.00{\cdot}10^{-2}$	heuristically tuned
u_dc	k_p	eq. (3.69)	$8.20 \cdot 10^{-3}$	C'$_\mathrm{OHL}$ equals 10.8 nF/km
u_dc	T_i	eq. (3.70)	$0.11 \cdot 10^{-1}$	C'$_\mathrm{OHL}$ equals 10.8 nF/km

5.5 Detection Trigger and Protection Threshold Determination

This section provides insights into detection trigger and protection threshold determination. To ensure selective behavior a coordinated approach is essential. This is especially important to differentiate between contingencies directly affecting a converter and interactions originating from the opposite subsystem.

5.5.1 DC Detection Thresholds

Derivative Criteria

To determine a feasible set of thresholds ensuring high selectivity a multitude of faults, originating from different fault locations along the OHL scheme, must be analyzed. In Fig. 5.4 absolute peak derivative values of incoming traveling waves related to positive dc pole to ground faults are presented for different load flow setpoints. During the analysis converter protection is turned off. While the left part shows results of T1 (P_{PCC}-Q_{PCC}-controlled station), the right part is related to T2 (u_{dc}-Q_{PCC}-controlled station). Furthermore, marker size is proportional to the fault resistance varied in a range between 0.1-100 Ω and different colors highlight dc pole measurement position at the positive or negative pole (dc network inductor interface). To account for limited data acquisition accuracy, obtained values are filtered by a 10 kHz low pass filter. Besides a marginal impact of load flow setpoints and terminal control modes on occurring peak derivative values, unified thresholds for both terminals can be selected. Marked by the grey dashed lines in Fig. 5.4, $|\mathrm{d}i_{\mathrm{dcs}}^{\mathrm{max}}/\mathrm{d}t|$ is set to 3.5 kA/ms and $|\mathrm{d}u_{\mathrm{line,dcs}}^{\mathrm{max}}/\mathrm{d}t|$ equals 5 kV/µs.

Absolute Value Criteria

To account for high-impedance faults along the OHL or derivative protection malfunctions, absolute value criteria for dc overcurrent and over-/undervoltage[7] are introduced. For the phase-module zero-sequence current loop, the selected threshold equals around 1.5 p.u. compared to rated dc current. While this ensures activation in the case of inappropriate dynamic response, an additional safety margin to avoid IGBT blocking related to arm overcurrents remains. In addition, due to the high volatility of voltages in OHL schemes, a relatively broad voltage range setup is required. Trigger levels are estimated subsequent to extensive simulations and are heavily dependent on selected control parameters. In the given scenario, absolute voltages must remain above 225 kV or below 725 kV. Furthermore, an IGBT block indication originating from the opposite converter

[7] This should be handled with care to avoid inappropriate trips, as dc voltages in OHL schemes are highly volatile.

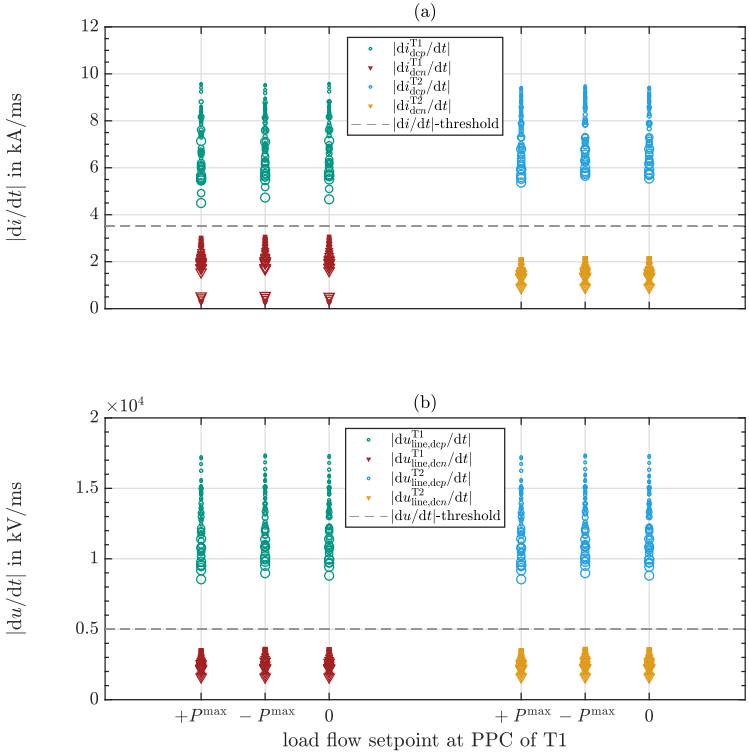

Figure 5.4: Absolute peak derivative values of incoming traveling waves detected at positive and negative pole of both terminals subsequent to positive dc pole to ground faults. Sweep of fault location and fault resistance to determine feasible thresholds: (a) peaks of di/dt values, (b) peaks of du/dt values.

is received with a time delay of 40 ms to ensure activation of control-wise dc FCI. In the meantime, the reactive power capability is preserved.

5.5.2 Internal Detection Thresholds

Related to section 4.4.1, determination of a suitable protection zone threshold requires details about the underlying current transformer accuracy. Following a conservative approach with respect of maximum arm, ac and dc currents, assuming a worst-case accuracy class of 1 %, the selected value of 0.15 kA presents a conservative choice. But, this still significantly speeds up internal fault detection compared to backup protection criteria motivated by SOA limitations.

5.5.3 AC Detection Thresholds

In the case of ac contingencies, a drop or increase in positive and negative sequence voltage occurs. To avoid interactions between conventional reactive power control and positive sequence reactive current injection, as well as to avoid issues related to negative sequence acquisition uncertainty, a deadband of 0.1 p.u. related to steady-state positive sequence voltage at the PCC is introduced [114]. Both corresponding gains $k_{i_q^{\pm 1}}$ are set to three.

5.5.4 Backup Protection Thresholds

To account for arbitrary scheme malfunctions, a backup protection functionality monitors grid-code imposed and technical constraints motivated by physical device limitations. Violations strictly lead to IGBT blocking. Besides given ac voltage and frequency boundaries according to [114], especially arm current and SM voltage limits are of high importance.

To ensure the appropriate dynamic performance of HVdc schemes, especially related to FB systems with advanced fault handling, arm currents must strictly remain below the peak IGBT current limit. Even though reference currents are capped by individual control loops, short term overshoots – due to signal acquisition uncertainties and control delays – may occur. For the given bipolar configuration, a maximum arm current threshold of 4.5 kA is selected, which equals approximately twice the steady-state arm current during operation under full-load[8].

Similarly, determination of individual SM operational limits must respect transient as well as dynamic deviations caused by arbitrary contingencies, as shown in Fig. 5.5 (a) and related to section 5.3.2. With respect to the maximum SM voltage, upper and lower boundaries are set to 3.7 kV and 1.3 kV to enable appropriate fault response. Furthermore, the SM sorting tolerance band u_{tol} equals 0.25 kV during conventional operation and is reduced (tolerating higher short term switching

[8] Estimation of short term overcurrent capabilities of IGBTs presents a challenging task and requires detailed manufacturer-related information on IGBT capabilities and thermal system design.

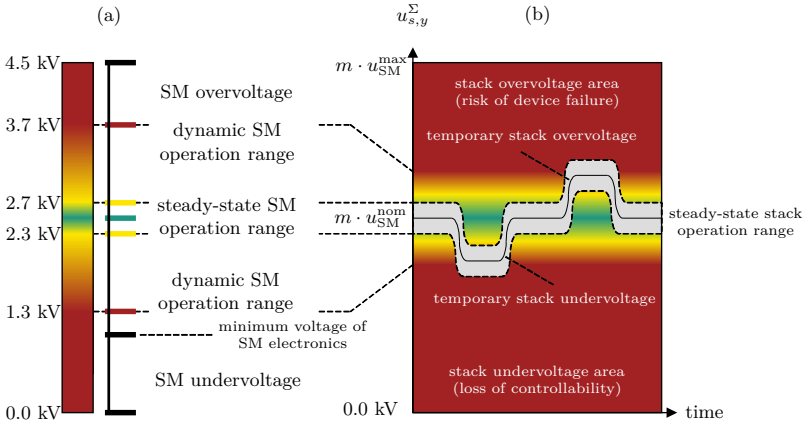

Figure 5.5: SM and stack voltage design approach similar to [4]:
(a) single SM operation range,
(b) stack operation range.

losses) to 0.05 kV in the case of a dc or ac contingency. While ranges for individual SMs are selected relatively wide and equal ±48 %, full stack voltage boundaries are tightened to around ±25-30 % to avoid total loss of converter controllability and arm overcharging, as shown in Fig. 5.5 (b).

Chapter 6

Bipolar MMC-HVdc Link Response to Contingencies

6.1 Introduction

To validate general suitability of the proposed control, balancing, fault handling and protection scheme, this chapter presents and evaluates response of the introduced bipolar link to various dc (f-dc), internal (f-bbp, f-xfo) and ac (f-3phgnd, f-2phgnd, f-1phgnd) contingencies. Related time domain simulations have been performed using PSCAD$^{\text{TM}}$/EMTDC$^{\text{TM}}$. Considering the required frequency range to investigated related phenomena, a step-width of 5 μs is selected.

6.2 Overview

In total six characteristic faults at different locations, which have been previously indicated in Fig. 5.1, and several parametric sensitivities are analyzed in the following. Unless further notice, scheme design and settings correspond to the set of parameters given within Chapter 5. Terminal T1 operates in P_{PCC}-Q_{PCC}-control mode (setpoint $P_{\text{PCC}} = +1.05$ GW / $Q_{\text{PCC}} = +400$ MVAr per converter) terminal T2 runs in u_{dc}-Q_{PCC}-control mode (setpoint $u_{\text{dc}} = +525$ kV / $Q_{\text{PCC}} = +400$ MVAr per converter). The utilized modeling environment comprises a computationally enhanced (accelerated) *Type 4* two-value resistor FB SM stack representation related to [23], frequency dependent line models following [69] and a transformer model including core saturation. Furthermore, surge arrestors are modeled by a non-linear resistor in series with a variable voltage source and the ac grid is represented by a Thévenin equivalent.

6.3 Scheme Response to DC Network Faults

6.3.1 DC Pole to Ground Fault

Within Fig. 6.1 and Fig. 6.2 response to a positive dc pole to ground fault (f-dc) located at $l = 150$ km is shown. The fault instant is at $t = 1.2$ s and R_{flt} corresponds to 1 mΩ.

Initially, the fault-induced traveling waves propagate along the OHL. Both terminals identify abnormal voltage derivative values at their faulty (positive) dc pole and trigger dc FCI in the upper bipolar subsystem, see Fig 6.1 and Fig. 6.2 top row. During this period, voltage and current derivative values at the healthy (negative) dc poles remain below the selected thresholds and normal operation is pursued. At the same time, the midpoint at the non-grounded terminal is shifted, see Fig. 6.1 dc voltage in top row, until the deviation is clamped by the corresponding surge arrestors. Energy absorption of both midpoint arrestor banks corresponds to 1.68 MJ. Furthermore, to interrupt the dc current at T2, converter C2p follows the occurring voltage oscillation by applying a negative dc output voltage. While the horizontal balancing capability is turned off due to a dc-side contingency, the HVdc switches at both terminals open after successful fault current reduction including a mechanical trigger delay of 2 ms. Subsequently, converters enter STATCOM mode (dc-side isolated) to regain full balancing capability[1].

Focussing on individual converters, C1p rapidly reduces its scheduled active power transmission, maintains its reactive power setpoint and switches total balancing orientation towards the ac-side, see Fig. 6.1 C1p (a)+(b). Thus, arm sum voltage deviations remain within a feasible range. The minimum arm sum voltage value corresponds to 621 kV or 0.920 p.u. related to $m \cdot u_{\text{SM}}^{\text{nom}}$ as shown in Fig. 6.1 C1p (c). In contrast, C1n continuously provides the requested active and reactive power at the PCC, see Fig. 6.1 C1n (a)+(b). Therefore, dc-side interactions caused by the faulty subsystem are buffered by the converter SMs (their capacitors) resulting in slightly larger arm sum voltage deviations as shown in Fig. 6.1 C1n (c). At the opposite terminal, C2n is affected in a similar manner, see Fig. 6.2 C2n (a)-(c). In contrast, an increasing impact on upper converter C2p compared to C2n is evident, see Fig. 6.2 C2p (a)-(c), where maximum arm sum voltage reaches approximately 842 kV or 1.247 p.u..

[1] Alternatively, subsequent to an appropriate de-ionization time, attempts for scheme restart could be triggered to restore power flow and resume normal operation.

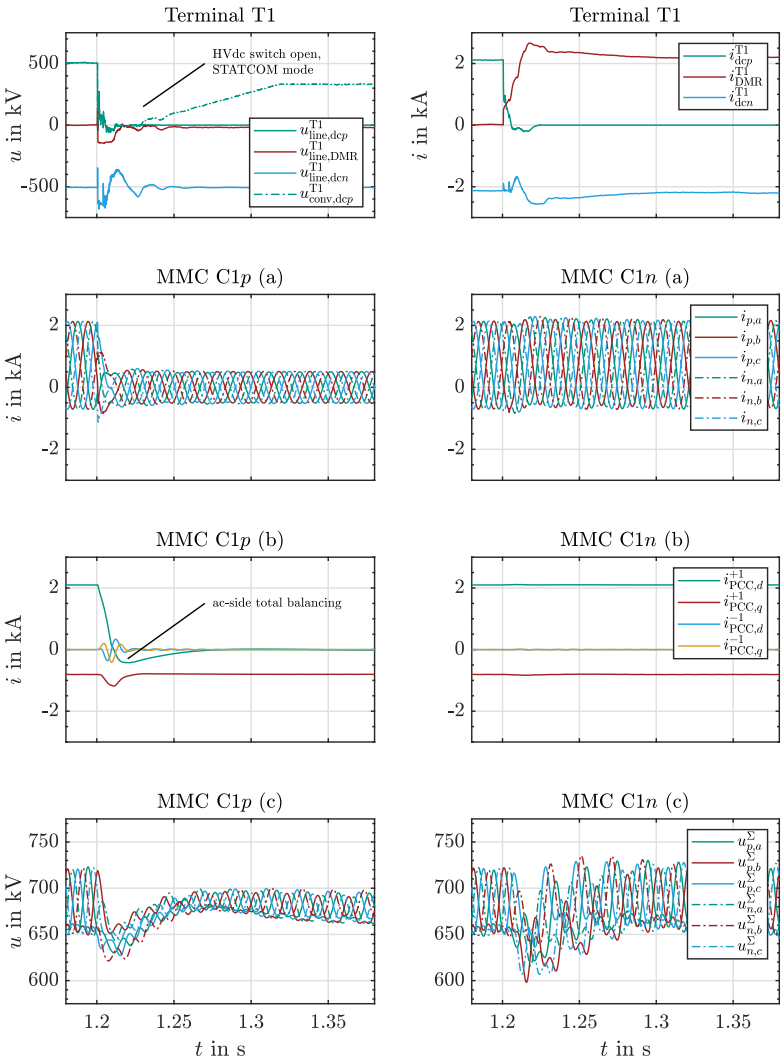

Figure 6.1: Response of T1 to a positive dc pole to ground fault (f-dc) located at $l = 150$ km, fault instant at $t = 1.2$ s. Row-wise plot sequence: terminal dc voltages and currents, converter arm currents, converter PCC currents in dq-frame, converter arm sum voltages.

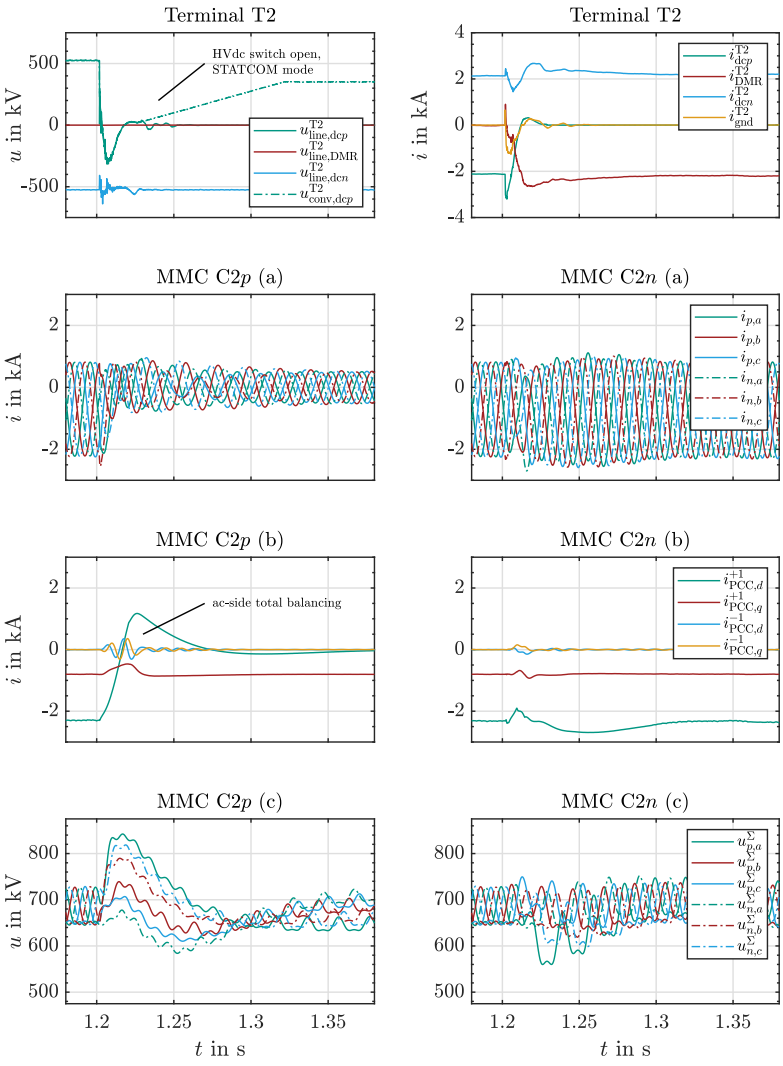

Figure 6.2: Response of T2 to a positive dc pole to ground fault (f-dc) located at $l = 150$ km, fault instant at $t = 1.2$ s. Row-wise plot sequence: terminal dc voltages and currents, converter arm currents, converter PCC currents in dq-frame, converter arm sum voltages.

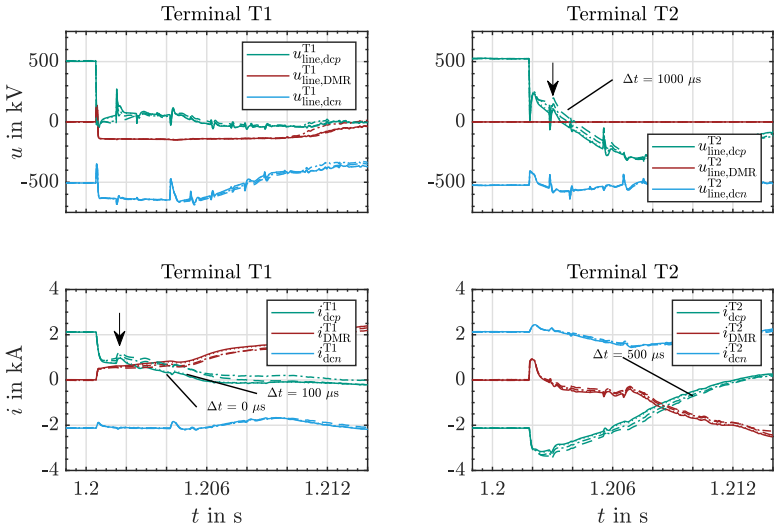

Figure 6.3: Impact of dc fault detection delay on the response to fault (f-dc). Range of additional delay 0 µs up to 1000 µs. Row-wise plot sequence: terminal dc voltages, terminal dc currents.

Sensitivity of DC Fault Detection Delay

Related to the positive dc pole to ground fault (f-dc), see Fig. 6.3, the impact of fault detection speed on dc-side currents and voltages is investigated. In this context, starting from the original scenario, an additional fault detection delay of up to 1000 µs is introduced, where each delay value is highlighted by a different linestyle and marked within the plot.

According to results shown in Fig. 6.3, where the visible time-frame has been shortened to 15 ms, several aspects shall be highlighted: *i)* The initial transient response (first incoming traveling wave) is independent of scheme control and protection setup. *ii)* Visible deviations start to occur after several hundreds of microseconds. This clearly shows that state-of-the-art HVdc technology causes a new kind of fast (control-related) power systems phenomena and validates the importance of advanced simulation frameworks. *iii)* The highly delayed cases show prolonged attempts to return to the previous dc current and dc voltage setpoints (depending on their control mode, see arrows in Fig. 6.3) leading to highest deviations compared to the original scenario.

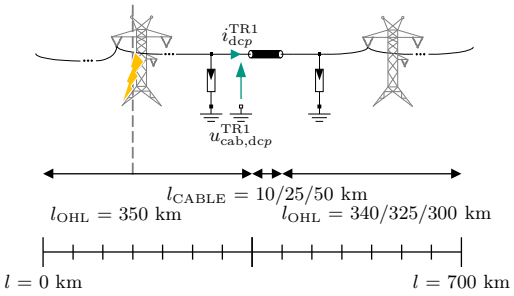

Figure 6.4: Schematic of investigated OHL scheme with partial cable section. Transition station TR1 located at $l = 350$ km, cable length corresponds to 10/25/50 km while OHL length is reduced accordingly.

Sensitivity of Partial Cable Sections

Due to the fact that OHL schemes have a significant visible impact, general attempts promoting HVdc cable transmission for onshore links, or at least partial cable sections like shown in Fig. 6.4, intensify. To sketch related technical challenges and motivate further research, the response of three partially cabled schemes and the original scenario to a positive dc pole to ground fault (f-dc) at $l = 150$ km are compared. Besides dc voltages and currents at T2, quantities at the fault-facing dc cable transition TR1 are highlighted. To facilitate straightforward identification of impacts, which are directly related to the introduced cable segments, control and protection setting are kept unchanged.

Inspecting Fig. 6.5, several distinctive changes occur: *i)* There is a less severe impact of fault-related traveling waves on T2, see enhanced voltage spike damping at T2 compared to the original case. Unfortunately, this diminishes the performance of derivative detection criteria. In all cable scenarios, the fault is detected at T2 by a slow absolute value criteria violation prior to dc FCI. *ii)* Increasing cable length leads to more severe and prolonged voltage polarity changes at the cable transition. Even though opposite polarity amplitudes remain at around 0.478 p.u., which is low with respect to recommended HV tests according to [120], significantly longer durations compared to applied tests may require further consideration (here around 11 ms). *iii)* Generally, in the case of increasing cable length and related dc-side energy content, a more oscillating system behavior results. *iv)* During all cases no SOA-related threshold has been violated. This is valid for both the upper subsystem and the lower (healthy) subsystem.

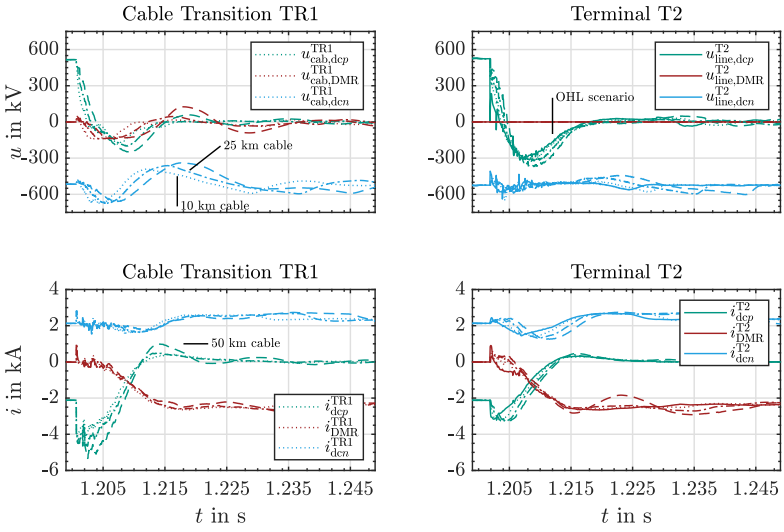

Figure 6.5: Impact of partial cable segments on the response to fault (f-dc). Cable length corresponds to 10/25/50 km. Row-wise plot sequence: transition station and terminal dc voltages, transition station and terminal dc currents.

Consequently, introduction of partial cable segments requires a thorough review of several issues related to MMC-HVdc schemes. It must be ensured that:

- fast derivative protection concepts are revised to ensure high selectivity in mixed transmission corridors
- basic design (converter design) and controls due to changing system dynamics are appropriately adapted
- occurring cable voltage stresses, also within the cable, are appropriately identified and are respected in insulation coordination studies

6.4 Scheme Response to Converter-Internal Faults

6.4.1 DC Busbar Fault

Within Fig. 6.6 and Fig. 6.7 response to a positive dc busbar to ground fault (f-bbp) within the converter-internal protection zone of C1p is shown. The fault instant is at $t = 1.2$ s and R_{flt} corresponds to 1 mΩ.

Different to the previous contingency (f-dc), the fault is located within the converter-internal protection zone C1p-bb$p$. To protect power electronic assets this leads to IGBT blocking, see Fig. 6.6 C1p (a)-(c). This is triggered by the proposed differential protection criterion within one data acquisition cycle of 20 µs subsequent to $i_{\mathrm{pz}}^{\mathrm{max}}$ threshold violation. Compared to common criteria related to physical device limits (e.g. arm overcurrents) detection is substantially accelerated. This reduces the extent of acdc interactions and further impacts on the healthy subsystem. Again, a voltage drift at the terminal midpoint occurs, see Fig. 6.6 top row, and energy absorption of both midpoint arrestor banks corresponds to 2.54 MJ. Arm sum voltage deviations do not differ significantly within C1n compared to a fault along the OHL and ac PCC quantities remain nearly unaffected, see Fig. 6.6 C1n (a)-(c). Nevertheless, dc voltage fluctuations and volatility increases in the healthy subsystem as shown in Fig. 6.6 top row. The maximum absolute deviation compared to steady-state occurs at t = 1.2143 s and corresponds to 246 kV. This illustrates the difficulty to set up suitable dc voltage limits in a bipolar scheme utilizing OHL transmission since a voltage limit violation within the lower subsystem leading to dc FCI shall be avoided in the case of these type of faults.

Heading the scope towards the opposite terminal T2, the incoming traveling wave triggers the current derivative loop around 2.46 ms after fault instant. Activated dc FCI reduces the remaining current to zero within an additional period of 31.34 ms. At this terminal, the extent of the voltage reversal is further boosted in the upper subsystem, see Fig. 6.7 top row. This is mainly influenced by the increasing share of OHL and the additional dc inductor between fault location and C2p. However, this does not show a significant impact on converter quantities. As highlighted in Fig. 6.7 C2p (a)-(c), arm and PCC currents follow a similar pattern compared to (f-dc), where the highest arm sum voltage level corresponds to 843 kV or 1.248 p.u.. Furthermore, as depicted in 6.7 C2n (a)-(c), the lower subsystem is capable to ride through this contingency.

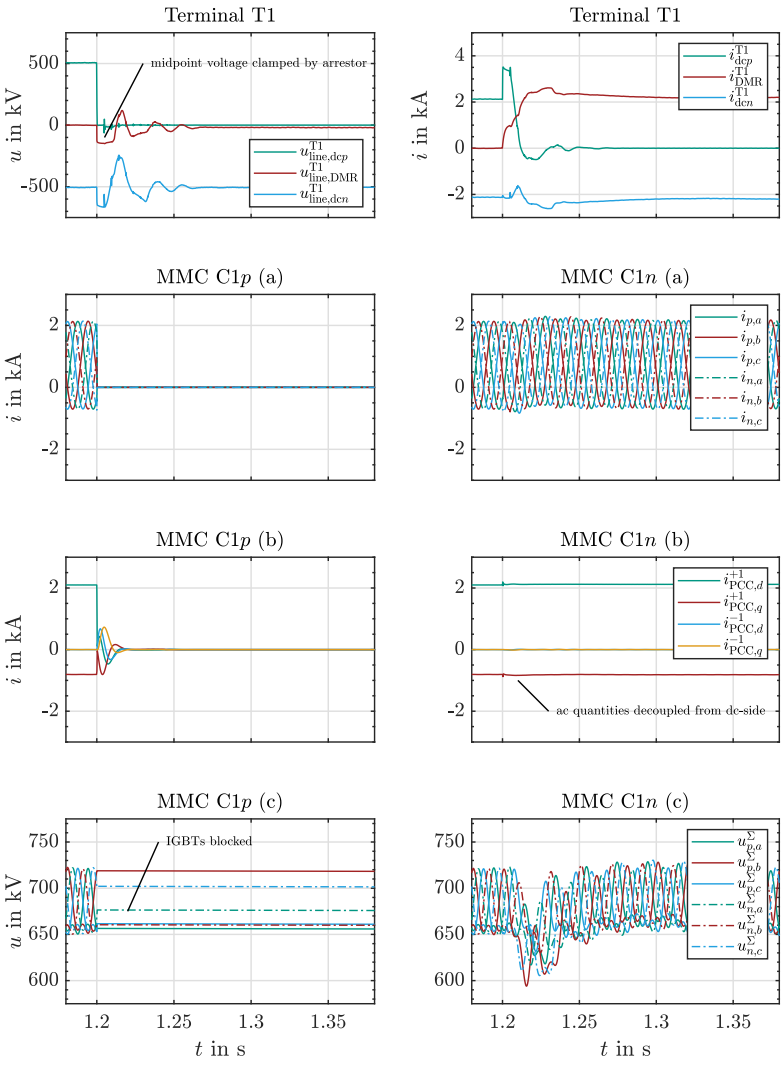

Figure 6.6: Response of T1 to a positive dc busbar to ground fault (f-bbp) at T1, fault instant at $t = 1.2$ s. Row-wise plot sequence: terminal dc voltages and currents, converter arm currents, converter PCC currents in dq-frame, converter arm sum voltages.

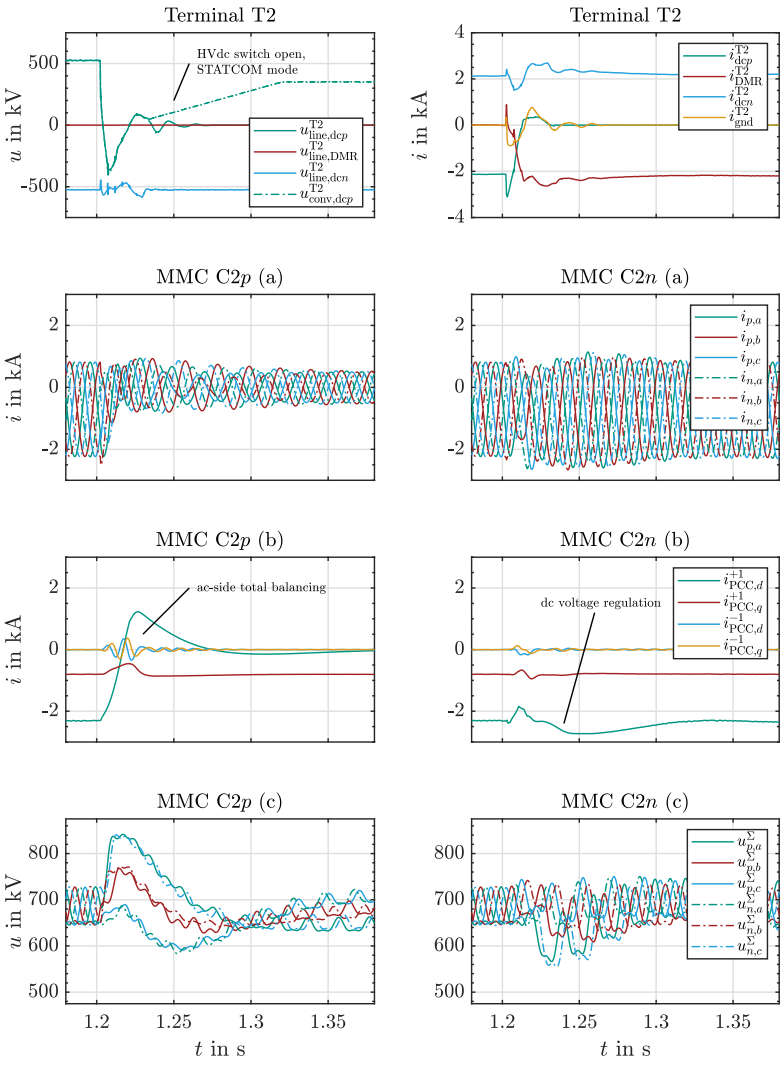

Figure 6.7: Response of T2 to a positive dc busbar to ground fault (f-bbp) at T1, fault instant at $t = 1.2$ s. Row-wise plot sequence: terminal dc voltages and currents, converter arm currents, converter PCC currents in dq-frame, converter arm sum voltages.

6.4.2 Converter-Internal AC Phase to Ground Fault

Within Fig. 6.8 and Fig. 6.9 response to a converter-internal phase to ground fault (f-xfo) located at the phase a transformer bushing of C1p is shown, see Fig. 5.1. The fault instant is at $t = 1.2$ s and R_{flt} corresponds to 1 mΩ.

Due to the low fault impedance, the ac voltage on the converter-side of the transformer is reduced to zero within phase a of C1p. This increases the peak phase to ground voltages of remaining phase b and c by a factor of $\sqrt{3}$ and reduces their phase difference to sixty degrees [55]. Furthermore, the characteristic dc-offset, which is typical for bipolar MMC-HVdc schemes at the converter-side of the transformer, disappears. Triggered by the converter-internal differential protection, all IGBTs in C1p are blocked. The opposite terminal does neither face an immediate derivative criteria violation nor a conventional absolute value threshold violation to detect a dc-side contingency. Therefore, both converters of T2 remain in dc voltage control mode, while C2p continues to operate connected to an open-end OHL transmission line configuration in the first instance, see top row of Fig. 6.8 and Fig. 6.9. The latter fact causes an output current reduction, while the dc voltage is kept at the reference setpoint.

Shifting the view towards T1 and especially C1p, a major dimensioning criteria for bipolar MMC-HVdc applications is unveiled. Even if FB SMs are in blocked state related stacks are further charged, if

$$u_{p,a}^{\Sigma} < u_{\mathrm{conv,dc}p}^{\mathrm{T1}} + 0 \text{ kV}, \tag{6.1}$$

and

$$u_{p,b/c}^{\Sigma} < u_{\mathrm{conv,dc}p}^{\mathrm{T1}} + \sqrt{3}\hat{u}_{\mathrm{conv}}. \tag{6.2}$$

Within the selected scenario, voltages across the SM stack can temporarily reach levels up to one megavolt. This is due to the combination of rising phase to ground voltage amplitudes, which are related to the transformer setting and oscillating positive dc pole to ground voltages. Typically, peaks are correlated to the negative half-wave of the effective converter ac-side voltage. Resulting SM stack charging currents, where a share is also flowing into the parallel SM stack arrestor (peak current 0.82 kA and dissipated energy of 1.65 MJ in arm p,b), and arm sum voltages are depicted in Fig. 6.8 C1p (a)-(c). Proceeding with C1n in the lower subsystem, which is especially remarkable related to the severity of events in C1p, only a marginal extent of interaction occurs, see Fig. 6.8 C1n (a)-(c). Converter controls and energy-balancing show appropriate performance and the converter returns to steady-state operation conditions within approximately 100 ms.

At the opposite side, normal operation (u_{dc}-control mode) of C2p continues until the block signal ($\mathrm{blk}_{\mathrm{ext}}$) trip signal is received. This happens after an additional delay of 40 ms related to the IGBT blocking instant of C1p and triggers dc FCI, see Fig. 6.9 top row. Subsequent to successful control-wise current interruption

the HVdc switch is operated to physically separate converter and OHL segments. Subsequently, the converter enters STATCOM mode and a discharge resistor of 1 kΩ is inserted on the line-side to reduce the remaining permanent pole to ground voltage[2]. Simultaneously, C2p is rebalancing its total energy via an additional ac current, see Fig. 6.9 C2p (a)-(c) and continuously provides reactive power at the PCC. In the case of C2n, no apparent impact of the internal phase to ground fault within the opposite terminal T1 exists. The converter remains in operation and rebalances minor deviations within a few grid-cycles, see Fig. 6.9 C2n (a)-(c).

[2]Alternatively, a slow control-wise dc voltage reduction could be performed without converter disconnection from the dc-side

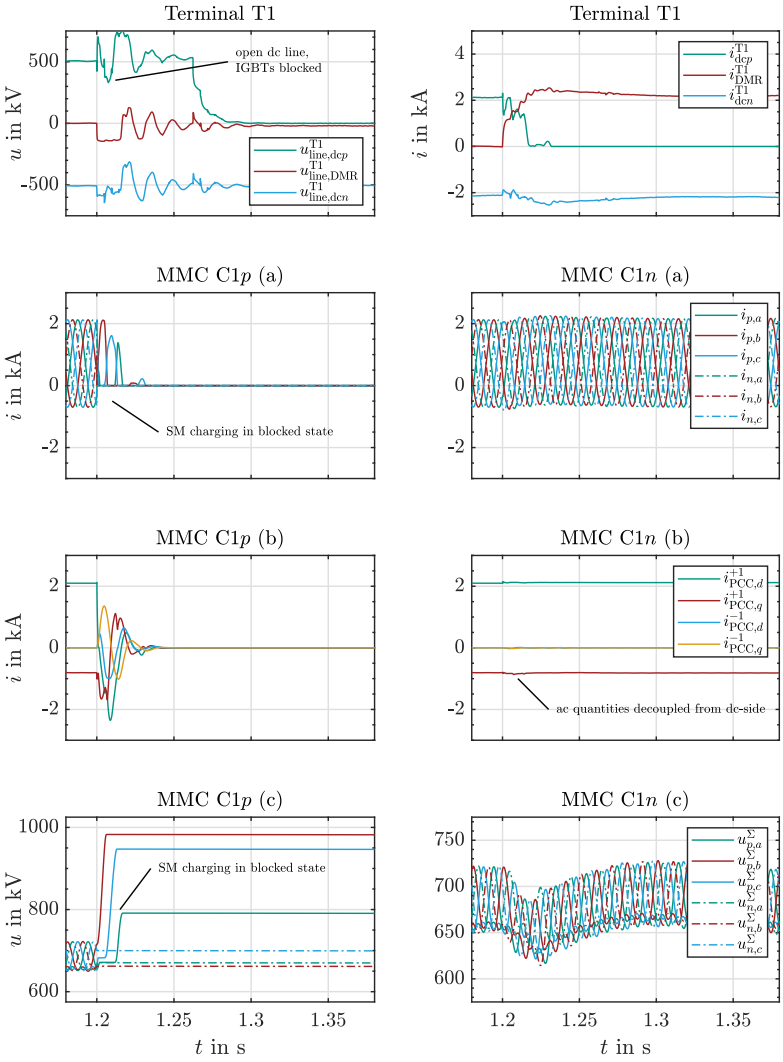

Figure 6.8: Response of T1 to a converter-internal phase to ground fault (f-xfo) located at the phase a transformer bushing of C1p, fault instant at $t = 1.2$ s. Row-wise plot sequence: terminal dc voltages and currents, converter arm currents, converter PCC currents in dq-frame, converter arm sum voltages.

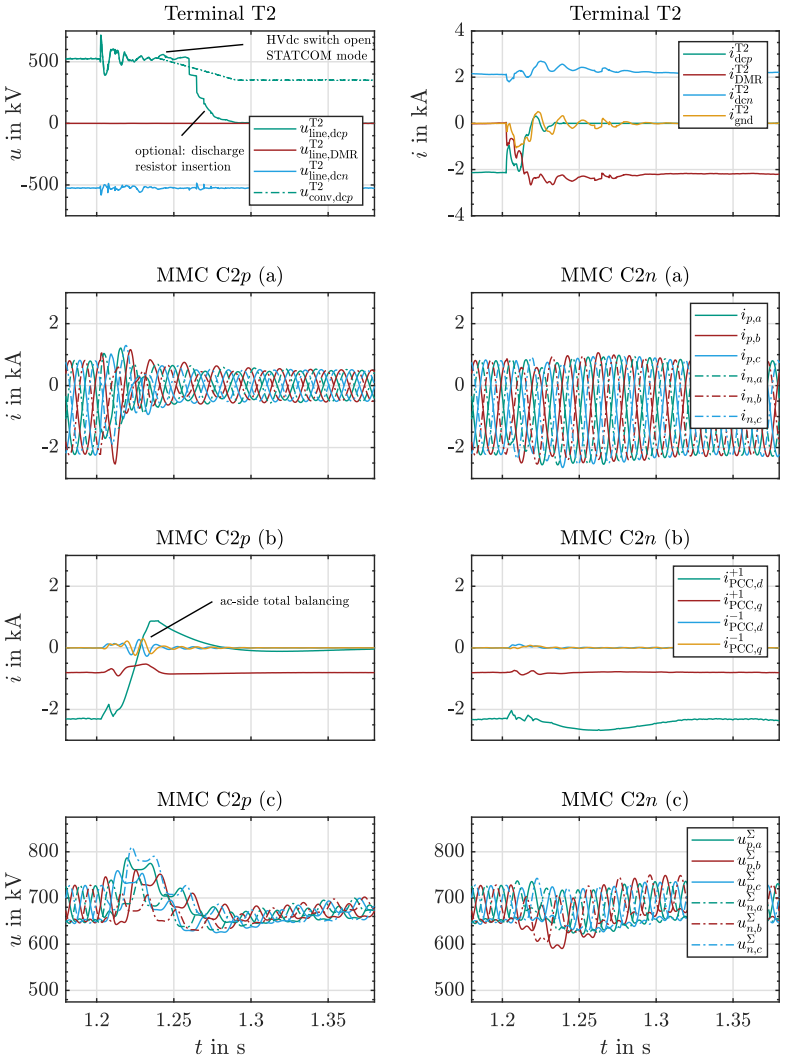

Figure 6.9: Response of T2 to a converter-internal phase to ground fault (f-xfo) located at the phase a transformer bushing of C1p, fault instant at $t = 1.2$ s. Row-wise plot sequence: terminal dc voltages and currents, converter arm currents, converter PCC currents in dq-frame, converter arm sum voltages.

6.5 Scheme Response to AC Grid Faults

While ac faults have an equal impact on upper and lower bipolar subsystem, related converter quantities are solely shown for the upper converters (denoted by subscript p) in the following.

6.5.1 Three-Phase to Ground Fault

Within Fig. 6.10 and Fig. 6.11 response to an ac three-phase to ground fault (f-3phgnd) near T1 is shown. The fault instant is at $t = 1.2$ s and the fault duration corresponds to 0.25 s. To emulate a distant fault with high residual voltage an RL-impedance between converter and fault location is assumed[3], see Fig. 5.1. The fault resistance itself equals $R_{\mathrm{flt}} = 5\ \Omega$.

The fault leads to a positive sequence voltage drop compared to pre-fault conditions. Since the deviation is greater than the selected deadband width of 0.1 p.u., this triggers ac FRT after 11.3 ms and initiates additional positive sequence reactive current injection. Due to the extent of the requested reactive current an active current limitation is required. This shows an immediate impact on scheme transmission capacity, which is reduced to around 0.3 p.u. as shown in Fig. 6.10 top row and C1p (c)+(d). Furthermore, the rapid adaption of power transmission as well as reactive current and signal acquisition uncertainty causes energetic deviations within C1p. Here, related arm sum voltages stay in a range between 559 kV (0.828 p.u.) and 827 kV (1.225 p.u.). Detailed time domain results and corresponding energetic quantities in $\alpha\beta 0$-frame are provided in Fig. 6.10 C1p (e)+(f). During this fault, all converter balancing loops remain in operation[4] and slowly adjust the affected energy components. In addition, arm current and voltage quantities remain in a feasible range and do not trigger SOA-related protection criteria, see Fig. 6.10 C1p (a)+(b).

Facing towards the opposite terminal T2 and especially C2p, a smooth operation setpoint adaption subsequent to active power limitation of T1 is performed. As shown in Fig. 6.11 top row and C2p (a)+(b), neither a significant deviation nor an overshoot of arm voltage, dc voltage or current quantities occur. Furthermore, the ac-side remains nearly unaffected, see Fig. 6.11 (c)+(d), except for a minor total balancing adaption (slight overshoot of $i^{+1}_{\mathrm{PCC},d}$). During the whole considered timeframe, arm sum voltages and energies remain de-facto balanced as shown in Fig. 6.11 (e)+(f).

[3] The grid impedance has been split in a ratio of 1:2 and a short OHL section has been attached.

[4] Note that the balancing control parameters are derived related to nominal voltage conditions. Therefore, dynamic performance, especially related to vertical balancing, is slightly compromised.

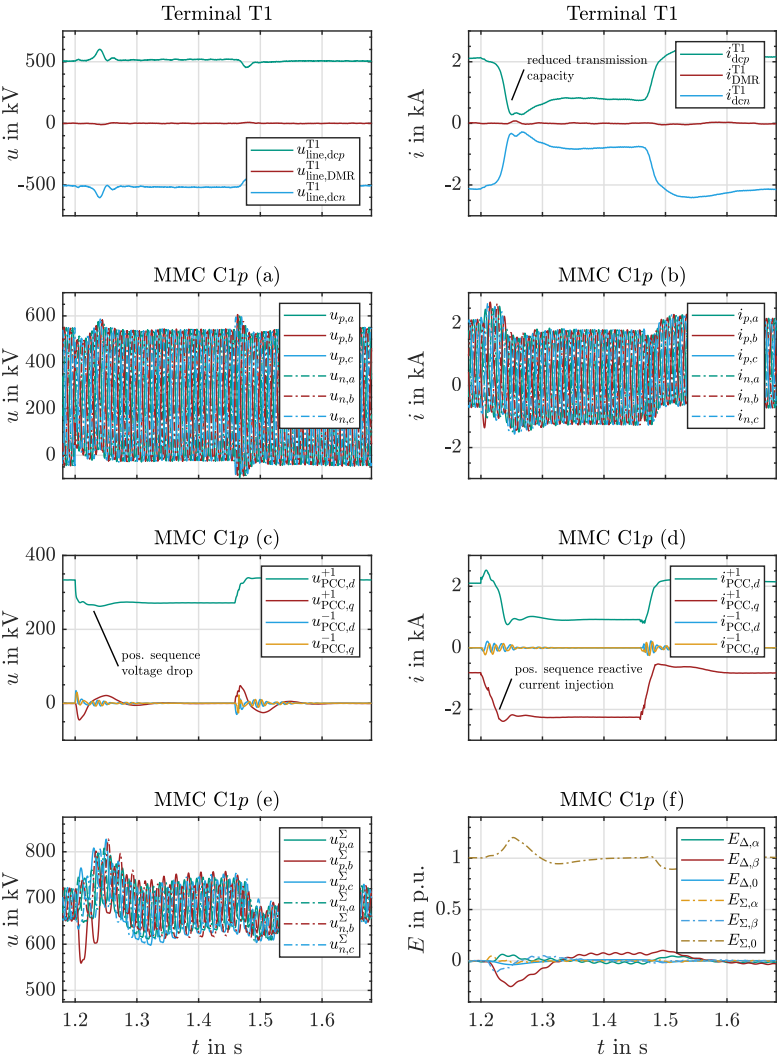

Figure 6.10: Response of T1 to an ac three-phase to ground fault (f-3phgnd) near T1, fault instant at $t = 1.2$ s. Row-wise plot sequence: terminal dc voltages and currents, converter arm quantities, converter PCC quantities in dq-frame, converter arm sum voltages as well as energetic quantities in $\alpha\beta 0$-frame.

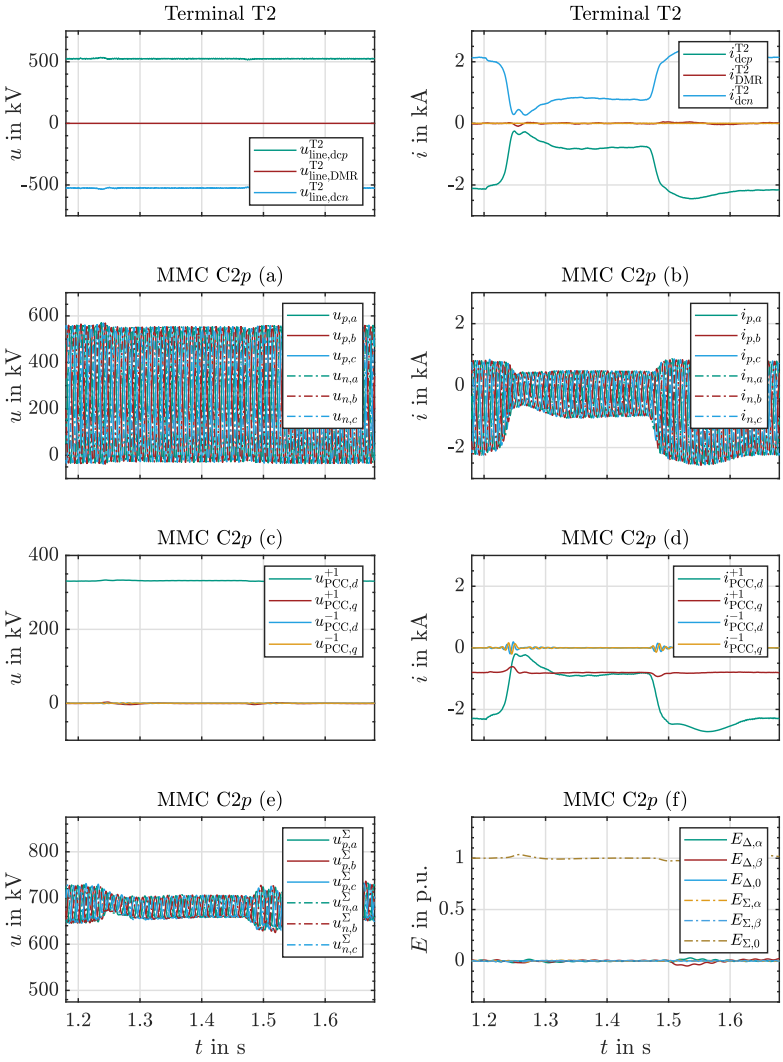

Figure 6.11: Response of T2 to an ac three-phase to ground fault (f-3phgnd) near T1, fault instant at $t = 1.2$ s. Row-wise plot sequence: terminal dc voltages and currents, converter arm quantities, converter PCC quantities in dq-frame, converter arm sum voltages as well as energetic quantities in $\alpha\beta 0$-frame.

6.5.2 Two-Phase to Ground Fault

Within Fig. 6.12 and Fig. 6.13 response to an ac two-phase to ground fault between phase a and phase c (f-2phgnd) near T1 is shown. The fault instant is at $t = 1.2$ s and the fault duration corresponds to 0.25 s. To emulate a distant fault with high residual voltage an RL-impedance between converter and fault location is assumed. This is performed similar to the previous case, see also Fig. 5.1. The fault resistance itself equals $R_{\text{flt}} = 2\ \Omega$.

As a consequence of the chosen fault scenario, a significant positive sequence voltage drop occurs. Furthermore, due to the unbalanced voltage sag characteristics a negative sequence voltage is present, see Fig. 6.12 C1p (a)+(c). With respect to given sequence current limits, regular power flow along the bipolar dc link is smoothly interrupted and subsequently restored. Remaining activities on the dc-side are related to total balancing activities. The latter are initiated by converters within terminal T1, which are balanced in mode TOT-A as shown in Fig. 6.12 top row. After ac fault detection, reactive current injection is initiated as shown in Fig. 6.12 (b)+(d). This is in line with dynamic requirements specified within section 2.3 regarding maximum overshoot and settling time. As indicated in Fig. 6.12 (e)+(f), vertical balancing has been turned off during the unbalanced fault. Corresponding minor deviations remain present until the ac fault is cleared, while total and horizontal deviations are adjusted. Minimum and maximum arm sum voltage peaks correspond to 518 kV (0.767 p.u.) and 861 kV (1.275 p.u.), respectively.

At the opposite terminal T2 a smooth performance related to power flow adaption is achieved, as depicted in Fig. 6.13 top row and C2p (c)+(d). Furthermore, no significant arm sum voltage or energetic deviations occur and arm voltage and current quantities follow the changing control setpoints without noticeable overshoots, see Fig. 6.13 (a)-(b) and (e)-(f).

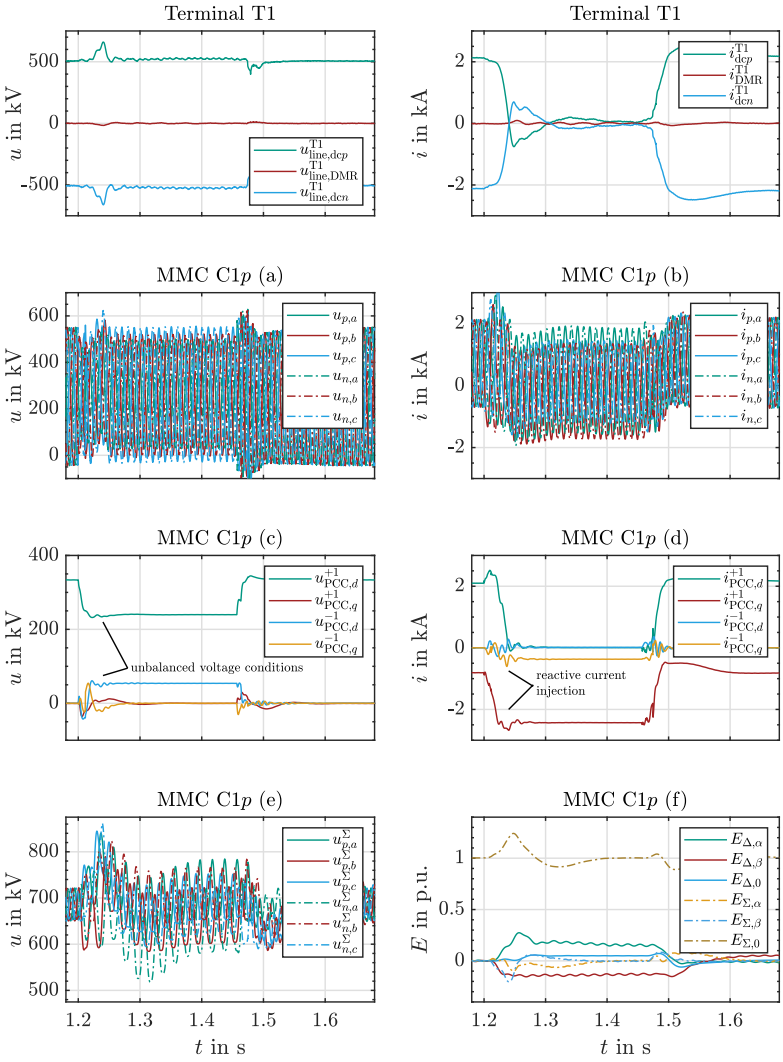

Figure 6.12: Response of T1 to an ac two-phase to ground fault (f-2phgnd) near T1, fault instant at $t = 1.2$ s. Row-wise plot sequence: terminal dc voltages and currents, converter arm quantities, converter PCC quantities in dq-frame, converter arm sum voltages as well as energetic quantities in $\alpha\beta 0$-frame.

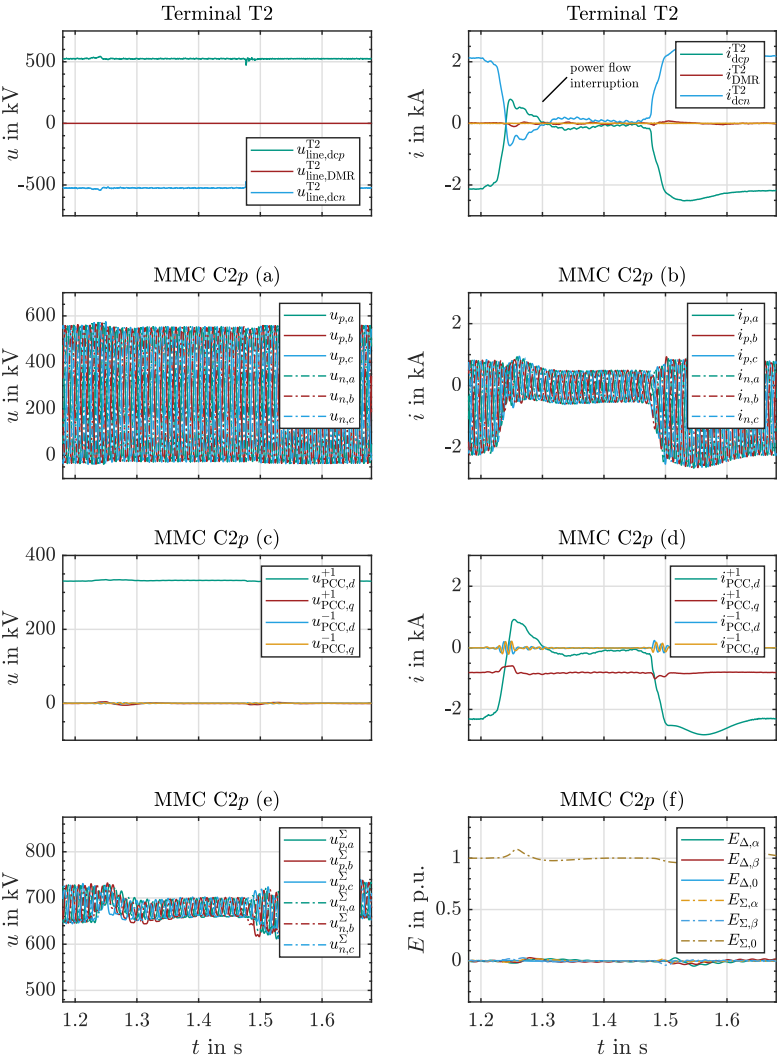

Figure 6.13: Response of T2 to an ac two-phase to ground fault (f-2phgnd) near T1, fault instant at $t = 1.2$ s. Row-wise plot sequence: terminal dc voltages and currents, converter arm quantities, converter PCC quantities in dq-frame, converter arm sum voltages as well as energetic quantities in $\alpha\beta 0$-frame.

6.5.3 Single-Phase to Ground Fault

Within Fig. 6.14 and Fig. 6.15 response to an ac single-phase to ground fault in phase a (f-1phgnd) near T1 is shown. The fault instant is at $t = 1.2$ s and the fault duration corresponds to 0.25 s. To emulate a distant fault with high residual voltage an RL-impedance between converter and fault location is assumed. This is performed similar to the previous cases, see also Fig. 5.1. The fault resistance itself equals $R_{\mathrm{flt}} = 2.5\ \Omega$.

During the fault, a positive sequence voltage drop occurs, which is marginally lower than the positive sequence deadband width of 0.1 p.u.. Furthermore, due to the unbalanced voltage sag characteristics, a negative sequence voltage is present as shown in Fig. 6.14 C1p (a)+(c). Compared to the previous case (f-2phgnd), link power transmission is reduced to around 0.73 p.u., while additional positive and negative sequence reactive currents are injected, see Fig. 6.14 top row and C1p (b)+(d). Vertical balancing is turned off during the fault and minimum and maximum arm sum voltage peaks correspond to 550 kV (0.815 p.u.) and 808 kV (1.197 p.u.), respectively. Nevertheless, arm sum voltages remain within a feasible range and continuous controllability is ensured like in all previous scenarios, see Fig. 6.14 (e)+(f).

Again, the impact on opposite terminal T2 is limited. Power flow adaptions are performed in a smooth manner as depicted in Fig. 6.15 top row and C2p (c)+(d). Furthermore, no significant arm sum voltage or energetic deviations occur and arm voltage and current quantities follow the changing control setpoints. This happens without considerable overshoots causing unintended power electronic device stresses, see Fig. 6.15 (a)+(b) and (e)+(f).

Finally, to quantify overall impact and benefit of implemented reactive current injection strategies, even if a relatively strong ac grid is present, Table 6.1 shows the adverse impact of inverted $k_{i_q^{\pm 1}}$ gains on remaining sequence voltage amplitudes with respect to the given fault scenario.

Table 6.1: Impact of inverted $k_{i_q^{\pm 1}}$ gains on sequence voltage amplitudes.

reactive current injection gains	$u^{+1}_{\mathrm{PCC},d}$	$u^{-1}_{\mathrm{PCC},d}$
$k_{i_q^{+1}}$=$k_{i_q^{-1}}$ = +3	292.2 kV	53.7 kV
$k_{i_q^{+1}}$=$k_{i_q^{-1}}$ = -3	281.0 kV	57.5 kV

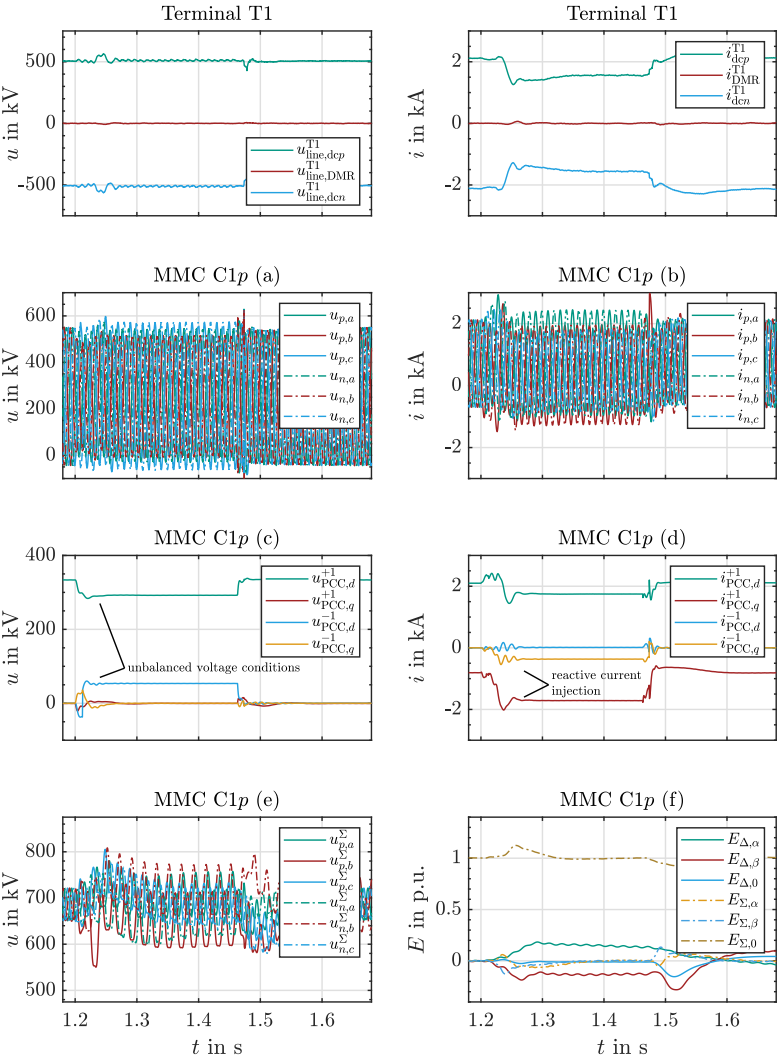

Figure 6.14: Response of T1 to an ac single-phase to ground fault (f-1phgnd) near T1, fault instant at $t = 1.2$ s. Row-wise plot sequence: terminal dc voltages and currents, converter arm quantities, converter PCC quantities in dq-frame, converter arm sum voltages as well as energetic quantities in $\alpha\beta 0$-frame.

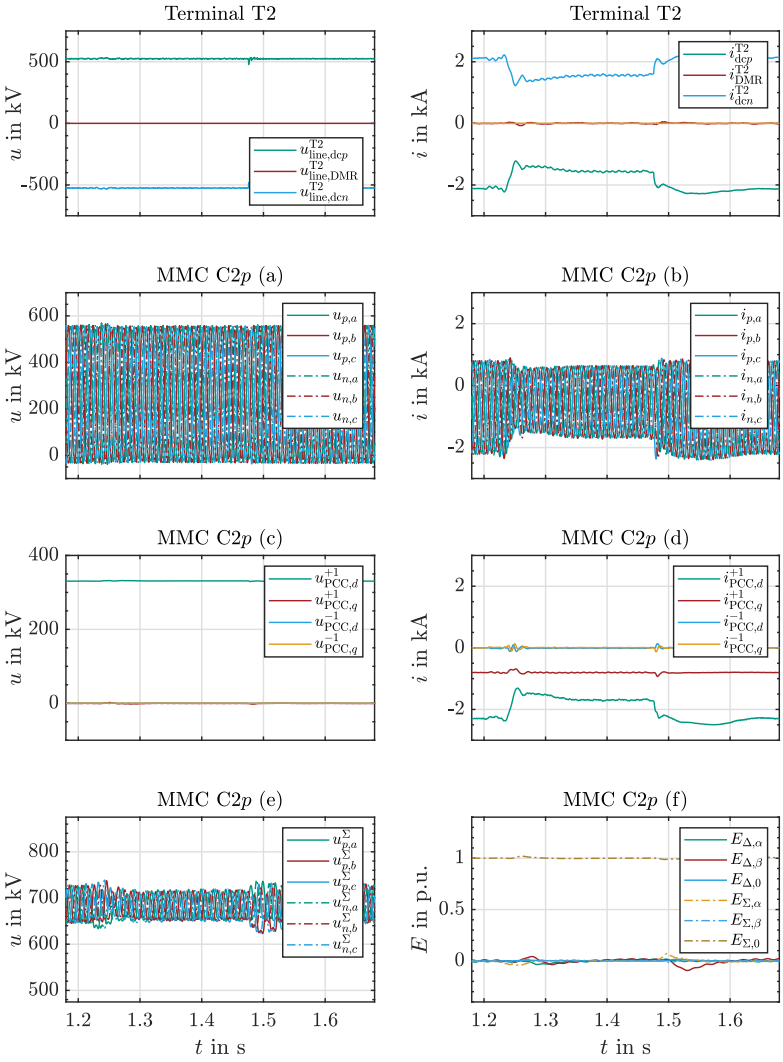

Figure 6.15: Response of T2 to an ac single-phase to ground fault (f-1phgnd) near T1, fault instant at $t = 1.2$ s. Row-wise plot sequence: terminal dc voltages and currents, converter arm quantities, converter PCC quantities in dq-frame, converter arm sum voltages as well as energetic quantities in $\alpha\beta 0$-frame.

Chapter 7

Potential of Bipolar Overlay Grid Applications

7.1 Introduction

In light of a general consensus on long-term targets to reduce greenhouse gas emissions, activities to push the global energy transition forward must be further strengthened. Recently, this has been re-emphasized by the Intergovernmental Panel on Climate Change (IPCC) to limit the impact of global warming [131].

By means of single embedded MMC-HVdc links, regardless of their configuration, regional availability of renewable energy is still a dominant factor. To reach a high level of sustainability over a long period of time a broader area must be integrated. Hence, bipolar HVdc overlay grids may present an attractive solution to collect widespread renewable in-feed and reduce regional dependencies. This chapter briefly discusses the fundamental aspects related to bipolar MMC-HVdc grids based on FB SMs and their application potential. Besides a brief introduction of literature discussing multi-terminal and overlay grid applications as well as protection methodologies, different grid design concepts are introduced and their macroscopic characteristics are compared.

7.1.1 Literature Review

In line with first commercial utilization of HVdc links based on state-of-the-art MMC technology, various stakeholders got attracted by the general suitability to form grid structures. This section sketches identified prospects and challenges related to HVdc grids. In addition, recent contributions in the field of HVdc grid fault handling are introduced and protection methodologies are briefly addressed.

Prospects and Challenges of HVdc Grids

Increasing global solar and wind capacity installation, mainly due to declining prices since the millennium, made policy-makers and non-governmental organizations rethink power system design and power supply aspects. Several concepts related to trans-national or even trans-continental HVdc grid initiatives have been proposed to improve the use of geographically distributed renewable energy sources and to tackle climate change. While such grids are expected to consist of VSCs – most likely MMCs – a lack of standardization, of available control and protection concepts as well as of sufficient transmission capacity has been identified [33]. Consequently: *i)* Standardization activities have been triggered and conducted within the last years, see [88] and [115]. *ii)* Control schemes have been proposed with respect to offshore wind farm control (fixed ac voltage and frequency, rectifier operation mode) and onshore converter control (droop control related to locally measured dc voltage, inverter operation mode) [26]. *iii)* A hybrid dc breaker has been presented in [34] and systemic considerations regarding SM characteristics and protection challenges have been deepened in [1] and [2]. *iv)* A general recommendation related to economic and technical feasibility of HVdc grids as well as remaining issues related to modeling and control have been summarized in [121] and [10], respectively.

Fault Handling and Protection Concepts for HVdc Grids

Beyond previous considerations addressing primarily fundamental aspects, industrial and academic stakeholders refined evaluation depth. In [18] and [15] hybrid HVdc breakers are elaborated on a system and component level involving main breaker, load commutation switch (LCS) as well as fast disconnector realization. Furthermore, fault clearance of a HB MMC-HVdc scheme in coordination with a hybrid HVdc breaker has been shown. This solution is currently also applied in a four-terminal bipolar MMC-HVdc grid project in China, see [78]. In contrast, [60] proposes the sole utilization of converters with fault-handling capability (e.g. FB or CDSMs) to interrupt occurring fault currents within the HVdc grid. To add benefits of advanced converters and operational improvements related to distributed circuit breakers disconnecting faulty grid areas or lines, several concepts combined both methods. Besides [57], which presents a converter-based fault-limiting concept to apply less costly mechanical HVdc breakers, [90] and [7] integrate hybrid HVdc breakers at major busbars and tie-lines to limit the extent of fault-related power transmission outages subsequent to contingencies.

To trigger the intended control-wise fault handling or device switching behavior, protection issues related to meshed HVdc grid structures must be resolved. Besides general challenges related to the currently available standards [40], robust and

selective (typically non-unit[1]) protection with respect to multiple protection zones within an HVdc grid is required. This is tackled by several approaches including: *i)* combined fault discrimination criteria evaluating voltage derivative, current derivative and absolute voltage level [51], *ii)* methods utilizing dc inductor voltages at each pole and their relation [53], *iii)* an approach monitoring the voltage integral of dc inductors [113], and *iv)* advanced signal processing techniques applying wavelet transformation on voltage and current [58, 43], respectively.

7.1.2 Related Publications

Conceptual considerations presented within this chapter are related to several scientific contributions. While considerations about monopolar schemes have been published in *IEEE Transactions on Power Delivery* [Jrnl2016a] and have been presented at the *Cigré Lund Symposium, Across Borders – HVDC systems and markets integration* [Conf2015a] in May 2015, studies based on bipolar schemes have been presented at the *IEEE Electrical Power and Energy Conference (EPEC)* [Conf2016c] in October 2016 and at the *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM-Europe)* [Conf2018b] in May 2018.

7.2 Comparison of Bipolar FB MMC-HVdc Grid Designs

This section highlights different grid designs based on an exemplary bipolar MMC-HVdc grid. The grid includes five bipolar terminals, where utilized converters are equipped with FB SMs, and two additional dc busbars (identifier BBx, x consecutively numbered) connected to multiple dc lines. Furthermore, a single low-impedance grounding is located at the neutral busbar of BB1. This ensures both feasible requirements for midpoint insulation coordination at each terminal and prevention of permanent ground currents [52]. In the following, main characteristics, fault handling sequences and operational impacts are highlighted. The selected nomenclature follows [123].

7.2.1 Non-Selective Grid Design

Interconnection of existing bipolar FB MMC-HVdc links by introducing dc busbars represents the least complex workaround to realize widespread grids[2]. Nevertheless, even though this does not include additional investment costs except

[1] Non-unit protection has no fixed zonal boundaries, as protection zones overlap for backup purposes.

[2] This implies equal dc voltage ratings of involved terminals. Otherwise, dcdc converters are required, which are not covered within this thesis.

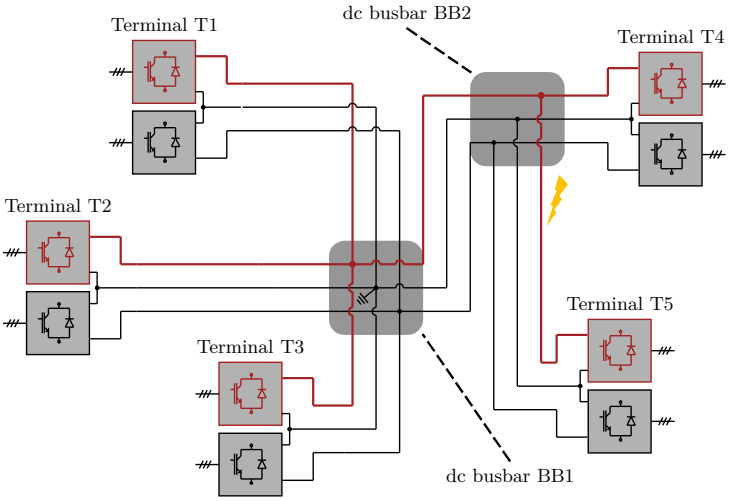

Figure 7.1: Non-selective bipolar MMC-HVdc grid design. Converters are equipped with FB SMs. Solid grounding located at dc busbar BB1. Green and red colored converters and lines indicate continuous availability or loss of transmission capacity subsequent to the highlighted fault, respectively.

for interconnecting lines, busbar modifications and disconnectors to perform (offline) topological changes, significant operational drawbacks exist. Those include contingency-related transmission capacity loss of a full bipolar subsystem. Furthermore, therewith connected reduced overall scheme availability/reliability as well as ac grid stability risks due to massive power flow changes result.

As shown in Fig. 7.1, an arbitrary dc pole to ground fault within the positive bipolar subsystem leads to a full outage in the case of permanent faults. The characteristic fault detection and clearance sequence comprises the following steps:

- Fault instant and traveling wave propagation.
- Detection of the fault within the positive bipolar dc subsystem[3].
- Control-wise FCI performed by affected converters located within the positive bipolar subsystem.
- HVdc switch operation of affected converters to enter STATCOM mode.

[3] As very sensitive thresholds to detect far-distant contingencies are required, high selectivity appears challenging.

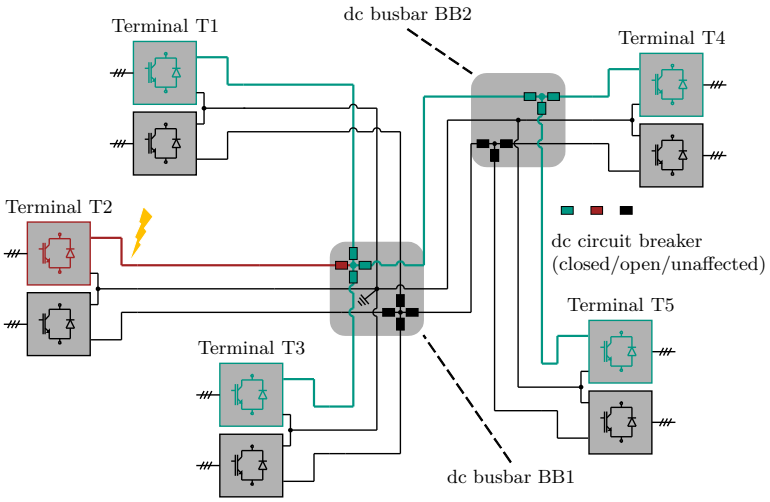

Figure 7.2: Fully-selective bipolar MMC-HVdc grid design. Converters are equipped with FB SMs. Solid grounding located at dc busbar BB1. Red colored converters and lines indicate loss of transmission capacity subsequent to the highlighted fault.

7.2.2 Fully-Selective Grid Design

In contrast to the previous case, a fully-selective bipolar MMC-HVdc grid design utilizing hybrid HVdc breakers at each line connected to a dc busbar is presented, see Fig. 7.2. Additionally, a schematic overview highlighting the basic principle of the hybrid breaker type related to [34] is provided in Fig. 7.3. Here, operation of an IGBT-based LCS commutates the current from the low loss primary current path into the bidirectional main breaker based on IGBTs. This device is capable to interrupt the fault current. But, prior to that action, the fast disconnector must have been opened to ensure a sufficient dielectric strength across disconnector and LCS.

Consequently, in combination with fault-blocking converters, each branch can be individually excluded on- or offline without interrupting power flow within the remaining network. This minimizes related impacts within the grid and ensures the highest possible operational flexibility.

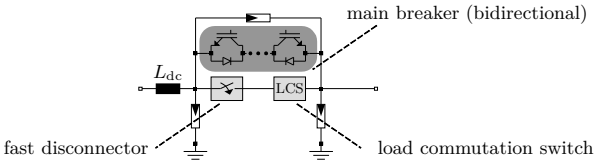

Figure 7.3: Schematic of a hybrid HVdc breaker.

The characteristic fault detection and clearance sequence related to an arbitrary dc pole to ground fault within the positive bipolar subsystem follows:

- Fault instant and traveling wave propagation.
- Fast detection within the affected branch[4].
- Control-wise FCI of directly affected converters (if applicable) and targeted hybrid HVdc circuit breaker operation. The remaining positive bipolar subsystem (remaining part of the dc grid) rides through the fault.
- Hybrid HVdc circuit breaker fault current interruption and HVdc switch operation of affected converters to enter STATCOM mode.

7.2.3 Partially-Selective Grid Design

Even though the fully-selective grid design provides several benefits significant hardware-related requirements exist. Current research activities aim to identify a trade-off between overall investment costs and remaining operational flexibility. While [59] proposes an adapted dc switchyard design based on conventional hybrid breakers, [66] proposes a multi-port hybrid breaker to reduce hardware-related intensity at the cost of a reduced redundancy. Here, as shown in Fig. 7.4 and highlighted in detail in Fig. 7.5, a similar concept according to [87] is chosen. In case a single busbar breaker port is affected by a fault, the corresponding LCS commutates the fault current into the unidirectional main breaker decoupled by a diode network.

With this approach, sub-grids can be formed in a cost-effective manner, as only one unidirectional switching device and a diode decoupling network are required in contrast to several bidirectional hybrid breakers.

[4] A coordinated selection of thresholds is enabled due to clearly separable protection zones, where high selectivity appears feasible.

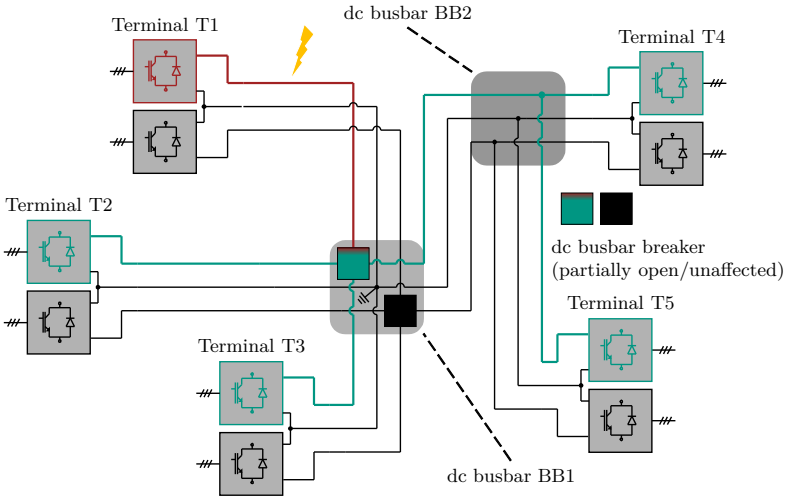

Figure 7.4: Partially-selective bipolar MMC-HVdc grid design. Converters are equipped with FB SMs. Solid grounding located at dc busbar BB1. Green and red colored converters and lines indicate continuous availability or loss of transmission capacity subsequent to the highlighted fault, respectively.

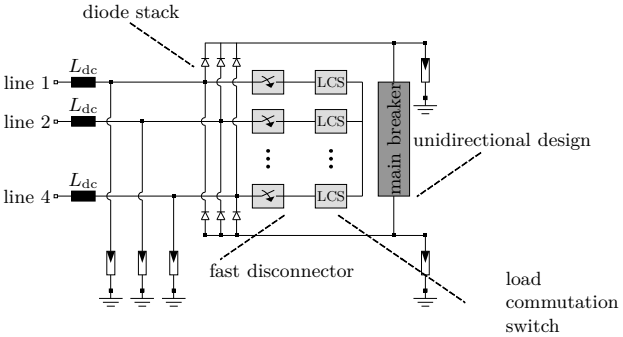

Figure 7.5: Schematic of a busbar HVdc breaker.

In a slightly adapted manner, the characteristic fault detection and clearance sequence follows:

- Fault instant and traveling wave propagation.
- Fast detection within the affected sub-grid[5].
- Control-wise FCI of directly affected converters (if applicable) and targeted busbar HVdc circuit breaker operation. The remaining positive bipolar subsystem (remaining part of the dc grid) rides through the fault.
- Busbar HVdc circuit breaker fault current interruption and HVdc switch operation of affected converters to enter STATCOM mode.

7.2.4 Grid Design Comparison

To conclude this section the presented grid designs are qualitatively compared against each other, as shown in Table 7.1. Considered criteria include projected investment costs, extent of transmission capacity loss (within one bipolar subsystem, in the case of a dc pole to ground fault) and operational flexibility.

Table 7.1: Overview of bipolar grid design characteristics.

grid design	hardware requirements	transmission capacity loss (within bipolar subsystem)	operational flexibility
non-selective	low	high (full)	low
fully-selective	very high	low (single component)	high
partially-selective	moderate	moderate (partial)	moderate

[5] A coordinated selection of thresholds is enabled due to sub-grids separating different protection zones. High selectivity appears feasible.

Chapter 8

Conclusion and Further Research Possibilities

8.1 Conclusion

MMC-HVdc systems in bipolar configuration present an attractive measure to solve challenges related to today's power systems. But, while this happens at the cost of significantly increasing system complexity, an urgent need for generic control, balancing and protection concepts integrated into an easily adjustable simulation framework emerges. This doctoral thesis has addressed identified shortcomings and has delivered the requested concept embedded within an EMT simulation environment. In this context, the potential scope of application ranges from preliminary investigations to performance validation purposes in line with ongoing projects. Besides that, a compilation of fundamentals, an introduction to scheme design aspects and considerations on bipolar overlay grid structures have broadened the scope.

The following list recapitulates the main scientific contribution of individual parts and briefly points out their impact related to the previously described general context:

- The compilation of HVdc fundamentals in Chapter 2 shed light on the MMC topology including SM stack modeling aspects and IGBT blocking behavior. In combination with a brief introduction of system configurations and grid code requirements, a common understanding and prerequisites to set up a suitable simulation framework were provided.
- The circuit analysis and derivation of instantaneous power terms in the first part of Chapter 3 unveiled control relations and energy balancing possibilities. Here, unbalanced grid conditions were assumed to trace the impact of arbi-

trary ac faults on energetic converter quantities. Related findings enabled the selection of a feasible balancing strategy and were inevitable to achieve robust FRT performance.

- Following a thorough literature review, the remaining part of Chapter 3 featured the underlying control and balancing implementation. While this incorporated sequence detection, grid synchronization, quantity determination, multi-dimensional balancing and controls, compliance with the full spectrum of technical requirements was assured. The concept was designed in a modular and easily adjustable manner to facilitate future adaptability.

- Fault handling and protection aspects were refined in Chapter 4. To achieve the desired level of robustness and selectivity, a comprehensive extension into a multi-zonal concept with backup-functionality was suggested. For example, a differential protection loop was proposed to minimize undesired interactions between bipolar subsystems in the case of converter-internal faults. Furthermore, signal routing, reference value determination – including positive and negative sequence reactive current injection – and remaining energy balancing possibilities during ac FRT and dc FCI were presented in detail.

- Reflecting upcoming project ratings, a generic MMC-HVdc scheme in bipolar configuration with DMR was set up in Chapter 5. Consequently, subsequent to the overall model composition as well as control and protection parametrization, a wide range of characteristic contingencies were investigated in Chapter 6. In detailed EMT studies, it was clearly demonstrated that: *i)* A universal applicability of the proposed concept was achieved. *ii)* Dynamic performance requirements were satisfied. *iii)* Excessive deviations from steady-state – or even violations of technical design values – were avoided. In addition, the general importance of in-depth simulative studies to quantify parametric sensitivities was indicated based on two illustrative examples.

- Given the high flexibility of bipolar MMC-HVdc schemes, potential designs of future HVdc grids were sketched in Chapter 7. In particular, advanced variants promoting a symbiosis between fault-blocking (fault current interrupting) converter topologies and resource-optimized HVdc breaker utilizations were discussed and compared.

8.2 Further Research Possibilities

To solve challenges related to the energy transition an increasing penetration of power electronics is undeniably predictable. However, while conventional assets like synchronous generators are replaced, major characteristics of power grids are subject to radical changes. As a consequence, the existing practice in a wide range of technical fields must be re-thought.

The following list provides a brief overview of recommended scientific activities related to stability aspects, scheme design and technical shaping of HVdc overlay grids.

- Reactive current injection during ac faults presents an intermediate stage along the way towards fully power electronic dominated systems. To avoid the need for grid voltage synchronization, grid forming controls appear superior. Nevertheless, this control methodology still lacks of specification-related uncertainties and presents vulnerabilities related to current limitation during faults.

- An increasing number of stability issues related to interactions of converter systems among themselves and also in combination with ac grids are reported. Therefore, the so called multi-frequency stability (up to several kilohertz), including methodological considerations and mitigation methods, is of high interest.

- Even though the fault-blocking capability of FB SMs provides operational advantages, relatively high losses do occur. Hence, to improve overall attractiveness, the development of loss-optimized and cost effective MMC-HVdc schemes with fault-blocking capability appears beneficial.

- The design of HVdc (overlay) grids must reflect the surrounding ac grid or even multiple asynchronous areas. Beyond the primarily fundamental challenges related to grid protection including dc circuit breaker utilization and control design, wide-area acdc interactions and fault propagation are crucial aspects to be solved. To study these effects, dynamic ac grid models must be coupled with detailed EMT models of HVdc assets by means of co-simulation.

Appendix A

Transformations

A.1 Utilized Transformations

Transformations utilized within this thesis correspond to definitions given within [117]. Assuming an arbitrary *abc*-frame vector, Clarke transformation transforms the input into orthogonal $\alpha\beta 0$-frame according to

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = \mathbf{T}^{abc\to\alpha\beta 0} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{A.1}$$

and the inverse expression corresponds to

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \mathbf{T}^{\alpha\beta 0\to abc} \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix}. \tag{A.2}$$

Similarly, for an arbitrary *abc*-frame vector, Park transformation transforms the input into a rotating $dq0$-frame according to

$$\begin{aligned} \begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} &= \mathbf{T}^{abc\to dq0} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \\ &= \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2}{3}\pi) & \cos(\theta + \frac{2}{3}\pi) \\ -\sin(\theta) & -\sin(\theta - \frac{2}{3}\pi) & -\sin(\theta + \frac{2}{3}\pi) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \end{aligned} \tag{A.3}$$

where the inverse expression equals

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \mathbf{T}^{dq0\rightarrow abc} \begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} \tag{A.4}$$
$$= \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 1 \\ \cos(\theta - \frac{2}{3}\pi) & -\sin(\theta - \frac{2}{3}\pi) & 1 \\ \cos(\theta + \frac{2}{3}\pi & -\sin(\theta + \frac{2}{3}\pi) & 1 \end{bmatrix} \begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix}.$$

Furthermore, the transformation from $\alpha\beta$-frame into dq-frame is given as

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \mathbf{T}^{\alpha\beta\rightarrow dq} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} +\cos(\theta) & +\sin(\theta) \\ -\sin(\theta) & +\cos(\theta) \end{bmatrix} \tag{A.5}$$

and the inverse function follows

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \mathbf{T}^{dq\rightarrow\alpha\beta} \begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} +\cos(\theta) & -\sin(\theta) \\ +\sin(\theta) & +\cos(\theta) \end{bmatrix}. \tag{A.6}$$

A.2 Relation between Symmetrical Components and Rotating Frames

Assuming sinusoidal voltages and currents in a three-phase system the complex power equals

$$\underline{S} = \underline{u}_a \underline{i}_a^* + \underline{u}_b \underline{i}_b^* + \underline{u}_c \underline{i}_c^*. \tag{A.7}$$

In symmetrical components, where $a = e^{j\frac{2\pi}{3}}$, utilizing the definition

$$\begin{bmatrix} \underline{x}_{(1)} \\ \underline{x}_{(2)} \\ \underline{x}_{(0)} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & \underline{a} & \underline{a}^2 \\ 1 & \underline{a}^2 & \underline{a} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} \underline{x}_a \\ \underline{x}_b \\ \underline{x}_c \end{bmatrix}, \tag{A.8}$$

we can rewrite eq. (A.7) as

$$\underline{S} = 3\underline{u}_{(1)} \underline{i}_{(1)}^* + 3\underline{u}_{(2)} \underline{i}_{(2)}^* + 3\underline{u}_{(0)} \underline{i}_{(0)}^*. \tag{A.9}$$

Neglecting zero sequence components in the following and assuming knowledge of angles[1] between positive (φ^+) as well as negative (φ^-) sequence voltages and currents, corresponding active and reactive power components follow

$$P_{(1)} = 3u_{(1)} i_{(1)} \cos(\varphi^+), \qquad Q_{(1)} = 3u_{(1)} i_{(1)} \sin(\varphi^+), \tag{A.10}$$
$$P_{(2)} = 3u_{(2)} i_{(2)} \cos(\varphi^-), \qquad Q_{(2)} = 3u_{(2)} i_{(2)} \sin(\varphi^-). \tag{A.11}$$

[1] Where voltage angles $\vartheta^{\pm}$=0 for the sake of simplicity.

To derive the relation between $\alpha\beta$ quantities and symmetrical components the latter are projected onto the corresponding real and imaginary axis. As shown in [124], where the steady-state phasors (capital letters) and rotational terms are separated as well as $\underline{u}_{\alpha\beta} = \alpha + j\beta$, this results in the relation

$$\frac{1}{2}\underline{u}_{\alpha\beta}(t) = \underline{U}_{(1)}e^{+j\omega t} + \underline{U}^{*}_{(2)}e^{-j\omega t}. \tag{A.12}$$

By applying forward and backward rotating Park transformation, it is derived that

$$\frac{1}{2}\underline{u}^{+1}_{dq} = \underline{U}_{(1)} + \cancel{\underline{U}^{*}_{(2)}e^{-j2\omega t}} \tag{A.13}$$

and

$$\frac{1}{2}\underline{u}^{-1}_{dq} = \underline{U}^{*}_{(2)} + \cancel{\underline{U}_{(1)}e^{+j2\omega t}}, \tag{A.14}$$

where proper sequence decoupling is implied to suppress fluctuating terms. This unveils that: *i)* The average value of *dq* voltages in forward rotating frame is related to the positive sequence voltage in symmetrical components. *ii)* The average value of *dq* voltages in backward rotating frame is related to the complex conjugate negative sequence voltage in symmetrical components[2].

Consequently, this also applies to currents regulated in *dq*-frame. If both rotating frames are appropriately aligned, while reminiscing reactive current injection according to eq. (4.3) and eq. (4.4), this verifies that equal reactive currents $i_q^{\pm 1}$ in forward and backward rotating frame lead to opposite voltage-supportive or rather voltage-suppressive behavior.

[2]Note that the factor of 1/2 in above equations disappears when comparing to the space vector transformation given in [117].

Appendix B

Determination of Non-Alternating Power Components

In this part, determination of power terms $p_{\Sigma,a}$ as well as $p_{\Delta,a}$ related to phase a are described. This is followed by a separation into fluctuating and non-fluctuating components. Beyond, the procedure to determine power components in $\alpha\beta 0$-frame is addressed, where further insights discussing re-expression of $p_{\Sigma,0}$ as well as $p_{\Delta,0}$ by $\alpha\beta 0$-frame voltage and current quantities are provided.

With respect to eq. (3.26) and eq. (3.27), instantaneous arm powers of upper and lower arm in phase a can be written as

$$p_{p,a} = \dot{E}_{p,a} = (u_{\Sigma,a} - u_{\Delta,a}) \cdot \left(i_{\mathrm{phm},a} + \frac{1}{2} i_{\mathrm{conv},a} \right) \tag{B.1}$$

and

$$p_{n,a} = \dot{E}_{n,a} = (u_{\Sigma,a} + u_{\Delta,a}) \cdot \left(i_{\mathrm{phm},a} - \frac{1}{2} i_{\mathrm{conv},a} \right). \tag{B.2}$$

Here, voltage components consist of

$$\begin{aligned} u_{\Sigma,a} &\approx +u_{\Sigma,0} \approx +\frac{1}{2} u_{\mathrm{dc}} \\ u_{\Delta,a} &\approx +\hat{u}_{\Delta}^{+1} \sin(\omega t + \vartheta^{+1}) + \hat{u}_{\Delta}^{-1} \sin(\omega t + \vartheta^{-1}) \\ &\approx +\hat{u}_{\mathrm{conv}}^{+1} \sin(\omega t + \vartheta^{+1}) + \hat{u}_{\mathrm{conv}}^{-1} \sin(\omega t + \vartheta^{-1}). \end{aligned}$$

Furthermore, if positive and negative sequence converter-internal current components for balancing purposes and ac-side currents with corresponding angles $\phi^{\pm 1}$ or $\varphi^{\pm 1}$ are present, currents are composed of

$$\begin{aligned} i_{\mathrm{phm},a} &\approx +\bar{i}_{\mathrm{phm}} + \hat{i}_{\mathrm{phm}}^{+1} \sin(\omega t + \phi^{+1}) + \hat{i}_{\mathrm{phm}}^{-1} \sin(\omega t + \phi^{-1}) \\ i_{\mathrm{conv},a} &\approx +\hat{i}_{\mathrm{conv}}^{+1} \sin(\omega t + \varphi^{+1}) + \hat{i}_{\mathrm{conv}}^{-1} \sin(\omega t + \varphi^{-1}), \end{aligned}$$

where $\bar{i}_{\mathrm{phm}}$ represents the non-alternating phase-module current component consisting of the dc current $\frac{1}{3}i_{\mathrm{dc}} \approx i_{\mathrm{phm},0}$ and $i^{\mathrm{dc}}_{\mathrm{phm},\alpha/\beta}$. Following eq. (3.30), this leads to

$$
\begin{aligned}
p_{\Sigma,a} &= +\bar{p}_{\Sigma,a} + \tilde{p}_{\Sigma,a} \\
&= +u_{\Sigma,0}\bar{i}_{\mathrm{phm}} \dots \\
&+ u_{\Sigma,0}\hat{i}^{+1}_{\mathrm{phm}}\sin(\omega t + \phi^{+1}) + u_{\Sigma,0}\hat{i}^{-1}_{\mathrm{phm}}\sin(\omega t + \phi^{-1}) \dots \\
&-\frac{1}{4}\hat{u}^{+1}_{\Delta}\hat{i}^{-1}_{\mathrm{conv}}\cos(\vartheta^{+1} - \varphi^{-1}) + \frac{1}{4}\hat{u}^{+1}_{\Delta}\hat{i}^{-1}_{\mathrm{conv}}\cos(2\omega t + \vartheta^{+1} + \varphi^{-1}) \dots \\
&-\frac{1}{4}\hat{u}^{-1}_{\Delta}\hat{i}^{-1}_{\mathrm{conv}}\cos(\vartheta^{-1} - \varphi^{-1}) + \frac{1}{4}\hat{u}^{-1}_{\Delta}\hat{i}^{-1}_{\mathrm{conv}}\cos(2\omega t + \vartheta^{-1} + \varphi^{-1}) \dots \\
&-\frac{1}{4}\hat{u}^{+1}_{\Delta}\hat{i}^{+1}_{\mathrm{conv}}\cos(\vartheta^{+1} - \varphi^{+1}) + \frac{1}{4}\hat{u}^{+1}_{\Delta}\hat{i}^{+1}_{\mathrm{conv}}\cos(2\omega t + \vartheta^{+1} + \varphi^{+1}) \dots \\
&-\frac{1}{4}\hat{u}^{-1}_{\Delta}\hat{i}^{+1}_{\mathrm{conv}}\cos(\vartheta^{-1} - \varphi^{+1}) + \frac{1}{4}\hat{u}^{-1}_{\Delta}\hat{i}^{+1}_{\mathrm{conv}}\cos(2\omega t + \vartheta^{-1} + \varphi^{+1})
\end{aligned}
\tag{B.3}
$$

and

$$
\begin{aligned}
p_{\Delta,a} &= +\bar{p}_{\Delta,a} + \tilde{p}_{\Delta,a} \\
&= +u_{\Sigma,0}\hat{i}^{+1}_{\mathrm{conv}}\sin(\omega t + \varphi^{+1}) + u_{\Sigma,0}\hat{i}^{-1}_{\mathrm{conv}}\sin(\omega t + \varphi^{-1}) \dots \\
&- 2\hat{u}^{+1}_{\Delta}\bar{i}_{\mathrm{phm}}\sin(\omega t + \vartheta^{+1}) - 2\hat{u}^{-1}_{\Delta}\bar{i}_{\mathrm{phm}}\sin(\omega t + \vartheta^{-1}) \dots \\
&-\hat{u}^{+1}_{\Delta}\hat{i}^{+1}_{\mathrm{phm}}\cos(\vartheta^{+1} - \phi^{+1}) + \hat{u}^{+1}_{\Delta}\hat{i}^{+1}_{\mathrm{phm}}\cos(2\omega t + \vartheta^{+1} + \phi^{+1}) \dots \\
&-\hat{u}^{+1}_{\Delta}\hat{i}^{-1}_{\mathrm{phm}}\cos(\vartheta^{+1} - \phi^{-1}) + \hat{u}^{+1}_{\Delta}\hat{i}^{-1}_{\mathrm{phm}}\cos(2\omega t + \vartheta^{+1} + \phi^{-1}) \dots \\
&-\hat{u}^{-1}_{\Delta}\hat{i}^{+1}_{\mathrm{phm}}\cos(\vartheta^{-1} - \phi^{+1}) + \hat{u}^{-1}_{\Delta}\hat{i}^{+1}_{\mathrm{phm}}\cos(2\omega t + \vartheta^{-1} + \phi^{+1}) \dots \\
&-\hat{u}^{-1}_{\Delta}\hat{i}^{-1}_{\mathrm{phm}}\cos(\vartheta^{-1} - \phi^{-1}) + \hat{u}^{-1}_{\Delta}\hat{i}^{-1}_{\mathrm{phm}}\cos(2\omega t + \vartheta^{-1} + \phi^{-1}),
\end{aligned}
\tag{B.4}
$$

where non-alternating parts are highlighted in red colour.

Consequently, Clarke transformation is applied to the extended three-phase set of equations. This solely comprises the non-fluctuating terms and results in

$$
\begin{bmatrix} \bar{p}_{\Sigma,\alpha} \\ \bar{p}_{\Sigma,\beta} \\ \bar{p}_{\Sigma,0} \end{bmatrix} = \mathbf{T}^{abc\to\alpha\beta0} \begin{bmatrix} \bar{p}_{\Sigma,a} \\ \bar{p}_{\Sigma,b} \\ \bar{p}_{\Sigma,c} \end{bmatrix} \tag{B.5}
$$

and

$$
\begin{bmatrix} \bar{p}_{\Delta,\alpha} \\ \bar{p}_{\Delta,\beta} \\ \bar{p}_{\Delta,0} \end{bmatrix} = \mathbf{T}^{abc\to\alpha\beta0} \begin{bmatrix} \bar{p}_{\Delta,a} \\ \bar{p}_{\Delta,b} \\ \bar{p}_{\Delta,c} \end{bmatrix}. \tag{B.6}
$$

To derive results given in section 3.2.4 individual power components are re-expressed by voltage and current quantities in $\alpha\beta 0$-frame. For converter voltages and currents the latter are given in section 3.2.3 and can be determined analogously for the phase-module currents. Indicated for $\bar{p}_{\Sigma,0}$ as well as $\bar{p}_{\Delta,0}$, which equal

$$\begin{aligned}\bar{p}_{\Sigma,0} =& +u_{\Sigma,0} i_{\mathrm{phm},0} \ldots \\ & -\frac{1}{4}\hat{u}_{\Delta}^{+1}\hat{i}_{\mathrm{conv}}^{+1}\cos(\vartheta^{+1}-\varphi^{+1}) - \frac{1}{4}\hat{u}_{\Delta}^{-1}\hat{i}_{\mathrm{conv}}^{-1}\cos(\vartheta^{-1}-\varphi^{-1})\end{aligned} \tag{B.7}$$

$$\bar{p}_{\Delta,0} = -\hat{u}_{\Delta}^{+1}\hat{i}_{\mathrm{phm}}^{+1}\cos(\vartheta^{+1}-\phi^{+1}) - \hat{u}_{\Delta}^{-1}\hat{i}_{\mathrm{phm}}^{-1}\cos(\vartheta^{-1}-\phi^{-1}), \tag{B.8}$$

results given in the main body of this thesis are obtained utilizing the following mathematical manipulations and trigonometric identities:

$$\begin{aligned}\cos(x-y) &= \cos(x+z-y-z) \\ \cos(x-y) &= \cos(x)\cos(y)+\sin(x)\sin(y) \\ \cos(x)\cos(y) &= \frac{1}{2}\cos(x+y)+\frac{1}{2}\cos(x-y) \\ \sin(x)\sin(y) &= \frac{1}{2}\cos(x-y)-\frac{1}{2}\cos(x+y).\end{aligned}$$

Appendix C

Basic Concept of Horizontal Energy-Balancing

This section presents the basic concept of horizontal energy-balancing in mode *HOR-A*. In the case of an energetic imbalance between the converter phases, requested balancing currents $i^{\mathrm{dc}}_{\mathrm{phm},\alpha/\beta}$ lead to additional output voltage components $u^{\mathrm{dc}}_{\Sigma,\alpha/\beta}$. Furthermore, assuming an arbitrary power flow is applied, a corresponding setpoint $u_{\Sigma,0}$ ensures the desired dc current flow[1].

To unveil the basic concept, the composition of individual arm reference voltages (neglecting u_Δ components) can be rewritten in *abc*-frame according to

$$\begin{bmatrix} u_{s,a} \\ u_{s,b} \\ u_{s,c} \end{bmatrix} = \begin{bmatrix} u_{\Sigma,0} + u^{\mathrm{dc}}_{\Sigma,\alpha} \\ u_{\Sigma,0} - \frac{1}{2} u^{\mathrm{dc}}_{\Sigma,\alpha} + \frac{\sqrt{3}}{2} u^{\mathrm{dc}}_{\Sigma,\beta} \\ u_{\Sigma,0} - \frac{1}{2} u^{\mathrm{dc}}_{\Sigma,\alpha} - \frac{\sqrt{3}}{2} u^{\mathrm{dc}}_{\Sigma,\beta} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} u^{\mathrm{dc}}_{\Sigma,\alpha} \\ u^{\mathrm{dc}}_{\Sigma,\beta} \\ u_{\Sigma,0} \end{bmatrix}. \tag{C.1}$$

While this is equal for upper and lower arm of each phase $s \in \{p, n\}$, the underlying approach is visualized based on a solely converter phase-related equivalent circuit in Fig. C.1. The resulting converter-internal current flows, which do not affect power transmission, are highlighted in grey.

[1] Note that $u_{\Sigma,0} >> u^{\mathrm{dc}}_{\Sigma,\alpha/\beta}$.

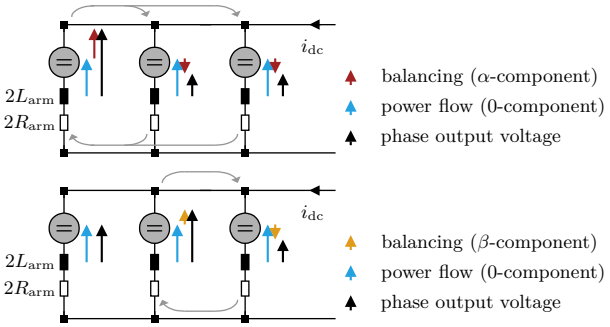

Figure C.1: Output voltage composition during horizontal energy-balancing in mode *HOR-A*. Relation between resulting phase voltages (black), involved voltage components separated according to their purpose (red, orange, blue) and internal current flow (grey).

Appendix D

Control Loops in Laplace Domain

In the following, detailed block diagrams of dc voltage control loop, energy balancing control loops and current control loops are provided.

D.1 Outer DC Voltage Control Loop

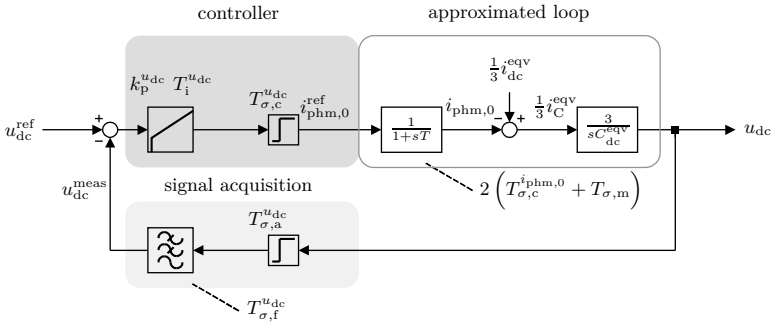

Figure D.1: Block diagram of dc voltage control loop in Laplace domain.

D.2 Energy-Balancing Control Loops

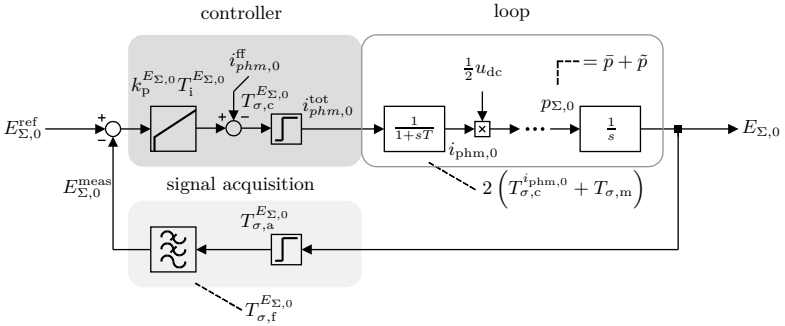

Figure D.2: Block diagram of total energy-balancing loop (mode TOT-A) in Laplace domain.

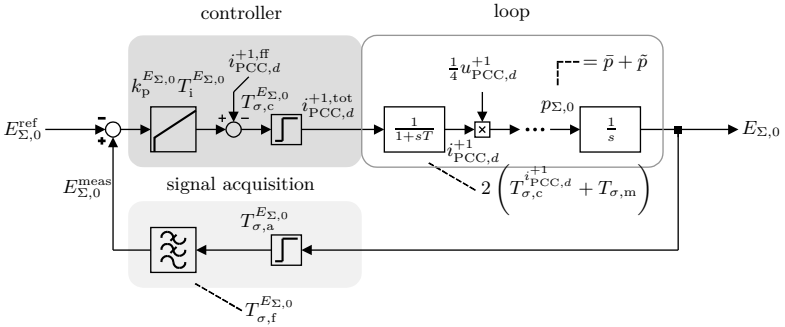

Figure D.3: Block diagram of total energy-balancing loop (mode TOT-B) in Laplace domain.

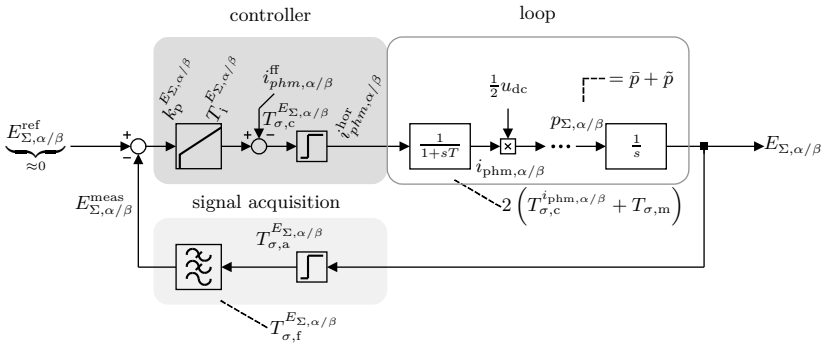

Figure D.4: Block diagram of horizontal energy-balancing loop in Laplace domain.

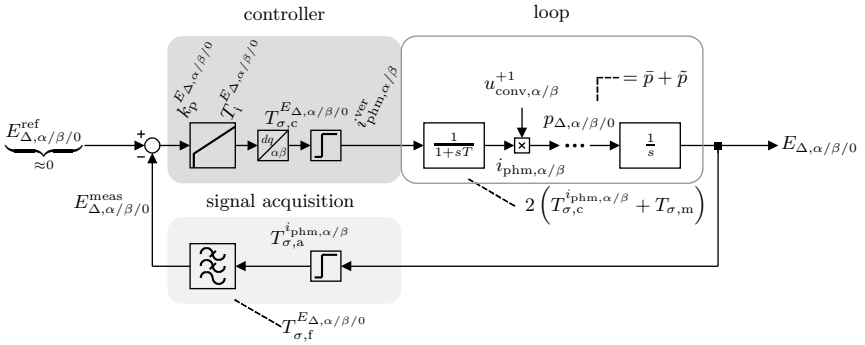

Figure D.5: Block diagram of vertical energy-balancing loop in Laplace domain.

D.3 Current Control Loops

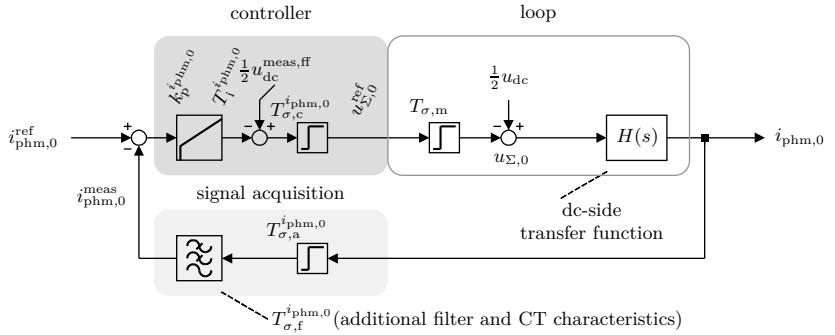

Figure D.6: Block diagram of dc current control loop in Laplace domain.

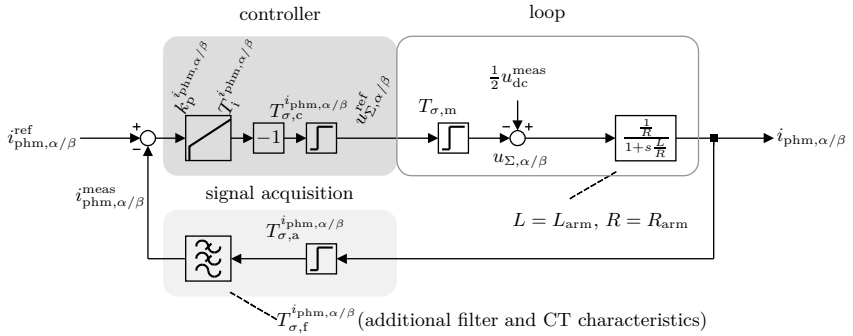

Figure D.7: Block diagram of inner current control loop in Laplace domain.

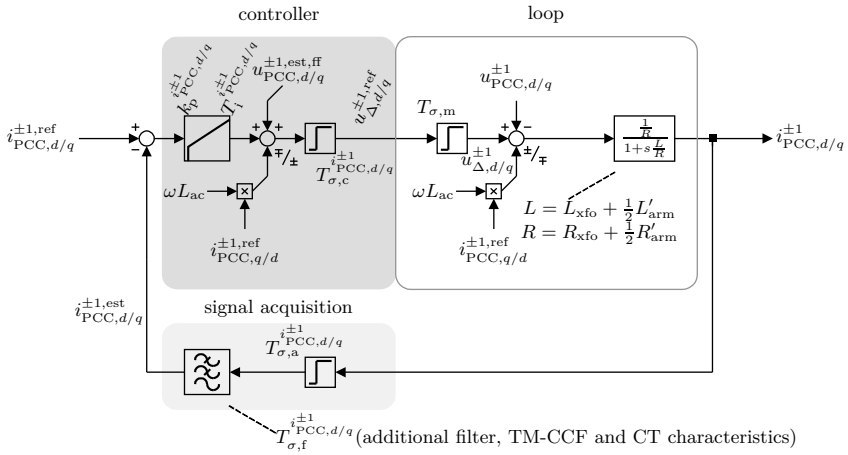

Figure D.8: Block diagram of ac current control loop in Laplace domain.

Appendix E

Surge Arrestor Characteristics

In Fig. E.1, the utilized surge arrestor non-linear voltage-current characteristic curve is presented. Related to a given nominal voltage, corresponding to the maximum continuous voltage level, the response of a single column to a 30/60 μs current shape is shown.

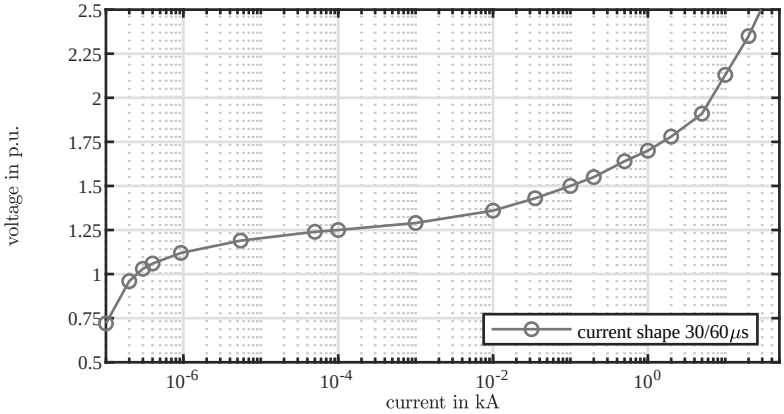

Figure E.1: Single-column non-linear surge arrestor characteristic curve related to a 30/60 μs current shape.

Appendix F

Cable Trench and Geometry

In Fig. F.1 and Table F.1, the underlying cable trench and geometry details of a 525 kV XLPE cable are presented, where a fully rated DMR is utilized.

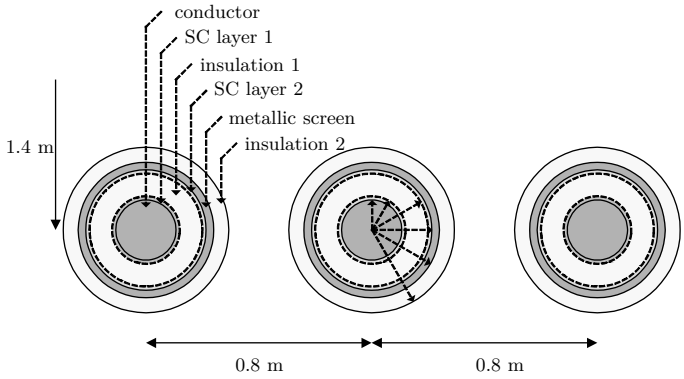

Figure F.1: Schematic of 525 kV XLPE cable trench and geometry.

Table F.1: 525 kV XLPE cable geometry data.

layer	radius†/thickness‡	further remarks
conductor	†31.75 mm	copper, 3000 mm^2
SC layer 1	‡2.00 mm	-
insulation 1	‡27.00 mm	$\epsilon_r = 2.3$
SC layer 2	‡2.30 mm	-
metallic screen	‡1.20 mm	aluminium
insulation 2	‡5.00 mm	$\epsilon_r = 2.5$

Appendix G

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G.2 List of Books, Patents and Technical Documents

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G.3 List of Related Publications

G.3.1 Peer-Reviewed Journals

[Jrnl2018e] M. Goertz, S. Wenig, C. Hirsching, M. Kahl, M. Suriyah, and T. Leibfried. Analysis of extruded HVdc cable systems exposed to lightning strokes. *IEEE Transactions on Power Delivery*, 33(6):3009-3018, Dec. 2018. doi:10.1109/TPWRD.2018.2858569.

[Jrnl2018d] S. Wenig, M. Goertz, C. Hirsching, M. Suriyah, and T. Leibfried. On full-bridge bipolar MMC-HVdc control and protection for transient fault and interaction studies. *IEEE Transactions on Power Delivery*, 33(6):2864-2873, Dec. 2018. doi:10.1109/TPWRD.2018.2823770.

[Jrnl2018c] S. Wenig, M. Goertz, M. Heinisch, M. Suriyah, and T. Leibfried. Fault discrimination and protection coordination for a bipolar full-bridge MMC-HVdc scheme. In *The IET Journal of Engineering*, 2018(15):1261-1266, Oct. 2018. doi:10.1049/joe.2018.0227.

[Jrnl2018b] S. Wenig, M. Goertz, M. Heinisch, S. Beckler, M. Kahl, M. Suriyah, T. Leibfried, and J. Christian. Internal converter- and dc-fault handling for a single point grounded bipolar MMC-HVdc system. *Elsevier Electric Power Systems Research*, 161:177-187, Aug. 2018. doi:10.1016/j.epsr.2018.04.012.
—In "Virtual Special Section" on papers from the *12th International Conference on Power Systems Transients (IPST)*.

[Jrnl2018a] C. Freye, S. Wenig, M. Goertz, T. Leibfried, and F. Jenau. Transient voltage stresses in MMC-HVdc links - impulse analysis and novel proposals for synthetic laboratory generation. *IET High Voltage*, 3(2):115-125, Jun. 2018. doi:10.1049/hve.2017.0141.

[Jrnl2016a] S. Wenig, F. Rojas, K. Schoenleber, M. Suriyah, and T. Leibfried. Simulation framework for dc grid control and acdc interaction studies based on modular multilevel converters. *IEEE Transactions on Power Delivery*, 31(2):780-788, Apr. 2016. doi:10.1109/TPWRD.2015.2417681.
—In "Guest Editorial Special Section" on HVdc transmission systems for large offshore wind power plants.

G.3.2 Conference Papers

[Conf2019b] M. Goertz, C. Hirsching, S. Wenig, K. M. Schaefer, S. Beckler, J. Reisbeck, M. Kahl, M. Suriyah, and T. Leibfried. Analysis of overvoltage levels in the rigid bipolar MMC-HVdc configuration. In *Proceedings of the IET International Conference on AC and DC Power Transmission (ACDC)*, pages 1-6, Feb. 2019. doi:10.1049/cp.2019.0025.

[Conf2019a] C. Hirsching, M. Goertz, S. Wenig, S. Beckler, M. Suriyah, and T. Leibfried. On control and balancing of MMC-HVdc links in rigid bipolar configuration. In *Proceedings of the IET International Conference on AC and DC Power Transmission (ACDC)*, pages 1-6, Feb. 2019. doi:10.1049/cp.2019.0026.

[Conf2018d] C. Hirsching, S. Wenig, M. Goertz, M. Suriyah, and T. Leibfried. Active damping method for harmonic current mitigation in grid-connected MMC-HVdc applications. In *Proceedings of the International Universities Power Engineering Conference (UPEC)*, pages 1-6, Sep. 2018. doi:10.1109/UPEC.2018.8542036.

[Conf2018c] Y. Rink, L. Held, S. Wenig, M. Suriyah, and T. Leibfried. Utilization of MMC-HVdc for primary and secondary control in hybrid acdc power systems. In *Proceedings of the International Universities Power Engineering Conference (UPEC)*, pages 1-6, Sep. 2018. doi:10.1109/UPEC.2018.8542083.

[Conf2018b] R. Sander, S. Wenig, M. Goertz, W. Schulze, M. Suriyah, and T. Leibfried. Fault discrimination in bipolar HVdc MTS equipped with bus bar breakers. In *Proceedings of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM)*, pages 505-512, May. 2018.

[Conf2018a] M. Goertz, S. Wenig, M. Suriyah, and T. Leibfried. Determination of transient overvoltages in a bipolar MMC-HVdc link with metallic return. In *Proceedings of the Power Systems Computing Conference (PSCC)*, pages 1-7, Jun. 2018. doi:10.23919/PSCC.2018.8442507.

[Conf2017d] M. Saltzer, M. Nguyen-Tuan, A. Crippa, S. Wenig, M. Goertz, H. Saad, and others. Surge and extended overvoltage testing of HVdc cable systems. In *Proceedings of the JICABLE-HVDC International Symposium on HVdc Cable Systems*, pages 1-6, Nov. 2017. Additionally published in Cigré Journal of Science and Engineering (CSE 011)

Additionally published in Revue de l'Electricité et de l'Electronique (REE 2018-1)

[Conf2017c] Y. Rink, L. Held, S. Wenig, M. Suriyah, and T. Leibfried. On implementation of primary frequency control in MMC-HVdc transmission systems. In *Proceedings of the IEEE Innovative Smart Grid Technologies - Europe (ISGT-Europe)*, pages 1-6, Sep. 2017. doi:10.1109/ISGTEurope.2017.8260239

[Conf2017b] M. Goertz, S. Wenig, S. Gorges, M. Kahl, S. Beckler, J. Christian, M. Suriyah, and T. Leibfied. Lightning overvoltages in a HVdc transmission system comprising mixed overhead-cable lines. In *Proceedings of the International Conference on Power System Transients (IPST)*, pages 1-6, Jun. 2017.
—Honoured with a "Best Paper Award".

[Conf2017a] S. Wenig, M. Goertz, W. Schulze, S. Beckler, M. Kahl, J. Christian, M. Suriyah, and T. Leibfried. Internal converter- and dc-fault handling for a single point grounded bipolar MMC-HVdc system. In *Proceedings of the International Conference on Power System Transients (IPST)*, pages 1-6, Jun. 2017.
—Honoured with a "Best Paper Award".

[Conf2016e] S. Wenig, M. Goertz, J. Prieto, M. Suriyah, and T. Leibfried. Effects of dc fault clearance methods on transients in full-bridge monopolar MMC-HVdc links. In *Proceedings of the IEEE Innovative Smart Grid Technologies - Asia (ISGT-Asia)*, pages 850-855, Nov. 2016. doi:10.1109/ISGT-Asia.2016.7796496.

[Conf2016d] M. Goertz, S. Wenig, M. Kahl, R. Sander, M. Suriyah, T. Leibfried, S. Beckler, and J. Christian. Auswirkung von Teilverkabelung auf das transiente Systemverhalten und die Isolationskoordination von HVdc-Trassen. In *Proceedings of the VDE-Hochspannugnstechnik ETG-Fachtagung*, pages 1-6, Nov. 2016.

[Conf2016c] S. Weck, J. Hanson, S. Wenig, T. Leibfried, T. Bongers and A. Moser. Planning and design of a European HVdc grid divided into feasible protection zones. In *Proceedings of the IEEE Electrical Power and Energy Conference (EPEC)*, pages 1-6, Oct. 2016. doi:10.1109/EPEC.2016.7771777.

[Conf2016b] R. Sander, S. Wenig, D. Barth, M. Suriyah, and T. Leibfried. HVdc grid protection with integrated fault categorization for selective tripping. In *Proceedings of the European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, pages 1-9, Sep. 2016. doi:10.1109/EPE.2016.7695313.

[Conf2016a] S. Wenig, M. Goertz, M. Suriyah, and T. Leibfried. Active dc fault management of a bipolar full-bridge MMC-HVdc scheme with metallic return. In *Proceedings of the IEEE International Energy Conference (ENERGYCON)*, pages 1-6, Apr. 2016. doi:10.1109/ENERGYCON.2016.7514052.

[Conf2015a] S. Wenig, R. Sander, A. Frank, M. Suriyah, and T. Leibfried. Fault clearing strategies in a multi-terminal HVdc grid with integrated dc circuit breaker. In *Proceedings of the Cigré Lund Symposium, Across Borders - HVdc Systems and Markets Integration*, pages 1-6, May. 2015.

[Conf2014a] S. Wenig, Y. Rink, and T. Leibfried. Multi-terminal HVdc control strategies applied to the Cigré B4 DC Grid Test System. In *Proceedings of the International Universities Power Engineering Conference (UPEC)*, pages 1-6, Sep. 2014. doi:10.1109/UPEC.2014.6934649.

G.3.3 Other Contributions

[Con2017a] M. Goertz, S. Wenig, M. Kahl, R. Sander, M. Suriyah, T. Leibfried, S. Beckler, and J. Christian. Auswirkung von Teilverkabelung auf das transiente Systemverhalten und die Isolationskoordination von HVdc-Trassen. In *ETG Migliederinformation 01/2017 - HOCH SPANNEND Innovative Technik für die Energiewende*, pages 9-12. Invited article. VDE e.V., Frankfurt, Germany, Feb. 2017.

[Con2016a] S. Wenig, F. Rojas, K. Schoenleber, M. Suriyah, and T. Leibfried. Simulation framework for dc grid control and acdc interaction studies based on modular multilevel converters. In *IEEE Power and Energy Society General Meeting (PESGM)*. Invited presentation, Boston, USA, Jul. 2016.

[Con2015a] S. Wenig, R. Sander, M. Suriyah, and T. Leibfried. Components and technical feasibility considerations for multi terminal HVdc transmission grid structures. In *EST 2015 - Energy, Science and Technology*. Invited presentation. Karlsruhe, Germany, May. 2015.

[Con2014a] S. Wenig. Design and Control of future dc Overlay Grids - Key principles of MMC control. In *Manchester Energy and Electrical Power Systems (MEEPS) - Future Trends and Applications in HVdc*. Invited poster, Manchester, UK, Nov. 2014.

G.3.4 Supervised Research

Master's Thesis or Equivalent Research Project

[Hei2017] M. Heinisch. Evaluation and comparison of bipolar MMC-HVdc systems. *Master's Thesis*. Nov. 2017.

[Rie2017] S. Rieker. Technical design requirements for discharge resistors and chopper units in HVdc applications. *Master's Thesis*. Jun. 2017.

[Pre2017] P. Prestel. Determination of transient overvoltages in MMC-HVdc Systems. *Master's Thesis*, May. 2017.

[Sch2016] W. Schulze. Effects of active fault handling strategies on transients in bipolar MMC-HVdc grids. *Master's Thesis*. Nov. 2016.

[Now2016] T. Nowak. Optimal design of structured control for MMC based HVdc grids. *Master's Thesis*. Aug. 2016.

[Pri2016] J. F. Prieto. Validation of control strategies suitable for full-bridge MMC-HVdc systems using the PSCAD software. *Master's Thesis*. Jun. 2016.

[Bar2015] D. Barth. Fault classification for selective isolation of HVdc subgrids. *Master's Thesis*. Nov. 2015.

[Goe2015] M. Goertz. Control and design of bipolar MMC based HVdc converter systems. *Master's Thesis*. Oct. 2015.

[Sko2015] K. Skokna. Modeling and structured control system design of HVdc networks equipped with Modular Multilevel Converters. *Research Project*. Sep. 2015.

[Fra2015] A. Frank. Active fault clearing strategies in multi-terminal HVdc grids with inclusion of dc circuit breaker devices and full-bridge based MMCs. *Master's Thesis*. Apr. 2015.

[Ren2015] B. Rennings. Study of transient phenomena during single line to ground faults in HVdc PLUS Systems. *Master's Thesis*. Mar. 2015.

[Lin2014] B. Linster. Impact of grid contingencies on hybrid acdc power systems. *Master's Thesis*. Nov. 2014.

[Pet2014] D. Petrusic. Systemtheorectical modeling of a Modular Multilevel Converter. *Master's Thesis*. Nov. 2014.

[Roj2014] F. Rojas. Modular Multilevel Converter Modeling, Control and Design for HVdc Applications. *Research Project*. Sep. 2014.

[Rin2014] Y. Rink. Regelungsstrategien zur Systemführung von Hochspannungs-Gleichstrom-Übertragungsnetzen. *Diploma Thesis*. Jul. 2014.

[Fre2014] E. Freer. Betriebsführungsstrategien einer HGÜ-Strecke innerhalb eines synchronen ac-Netzes. *Diploma Thesis*. Jul. 2014.

[Gru2013] L. Grundmann. Modeling and grid integration of Modular Multilevel Converter systems. *Master's Thesis*. Dec. 2013.

Bachelor's Thesis

[Hel2016] K. Hellmuth. Investigation of discharging processes in partially cabled HVdc systems. *Bachelor's Thesis*. Oct. 2016.

[Win2015] A. Winghart. MCCF based harmonic compensation approach for HVdc converter systems. *Bachelor's Thesis*. Oct. 2015.

[Arm2015] M. Armbruster. Overvoltage analysis in partially cable equipped HVdc links. *Bachelor's Thesis*. Oct. 2015.

[Hir2015] C. Hirsching. Roadmap towards a northern European HVdc-grid Under Consideration of Technical Constraints. *Bachelor's Thesis*. Aug. 2015.

[Hel2014] S. Hellmuth. HVdc grid scenario development in the North- and Baltic Sea area to achieve optimal offshore wind power under consideration of technical constraints. *Bachelor's Thesis*. Nov. 2014.

[Ach2014] J. Achstetter. Evaluation and implementation of Modular Multilevel Converter modulation strategies suitable for HVdc applications. *Bachelor's Thesis*. Oct. 2014.

[Foi2014] S. Foitzik. dc-dc converter topology evaluation and advanced operation strategies for future HVdc overlay grids. *Bachelor's Thesis*. Aug. 2014.

Nomenclature

List of Abbreviations

ac	alternating current
CBF	complex bandpass filter
CCF	complex coefficient filter
CCSC	circulating current suppressing controller
CDSM	clamp-double submodule
CO_2	carbon dioxide
CT	current transformer
D	diode
dc	direct current
DDSRF	decoupled double synchronous reference frame
DMR	dedicated metallic return
EMT	electro magnetic transient
FB	full-bridge
FCI	fault current interruption
FIR	finite impulse response
FLL	frequency locked loop
FRT	fault ride-through
GR	ground return
HB	half-bridge
HVdc	high voltage direct current
IEA	International Energy Agency
IGBT	insulated gate bipolar transistor
IPCC	intergovernmental panel on climate change
LCC	line commutated converter
LCS	load commutation switch
LI	lightning impulse
MCCF	multiple complex coefficient filter
MMC	modular multilevel converter
MSOGI	multiple second order generalized integrator
NLC	nearest level control

OHL ..... overheadline
p.u. ..... per unit
PCC ..... point of common coupling
PD ..... phase disposition
PI(R) ..... proportional-integral(-resonant)
PLL ..... phase-locked loop
PSC ..... phase-shifted carrier
PWM ..... pulse-width modulation
RGD ..... rigid
ROCOF .... rate of chance of frequency
S&H ..... sample and hold
SI ..... switching impulse
SM ..... submodule
SOA ..... safe operating area
SRF ..... synchronous reference frame
SSR ..... sub-synchronous resonance
SSTI ..... sub-synchronous torsional interaction
SVM ..... space vector modulation
T ..... transistor
TM ..... two module
TSO ..... transmission system operator
VSC ..... voltage source converter
VT ..... voltage transformer
WT ..... wind turbine
XLPE ..... cross-linked polyethylene

List of Main Variables and Parameters

δ ..... angle
ω ..... angular frequency
ϕ ..... phase-module current phase shift
θ ..... phase angle
φ ..... converter ac current phase shift
ϑ ..... converter ac voltage phase shift
C, C' ..... capacitor, capacitance per km of line
E ..... energy
f ..... frequency
i ..... current
L, L' ..... inductor, inductance per km of line
P ..... active power
p ..... instantaneous power
Q ..... reactive power
R, R' ..... resistor, resistance per km of line
S ..... apparent power
t ..... time

u ..... voltage
X ..... reactance
Z ..... impedance

List of Main Subscripts

$\cdot_{(1)/(2)/(0)}$ ... quantity in (1)/(2)/(0)
$\cdot_{\alpha/\beta/0}$ ..... quantity in $\alpha/\beta/0$-frame
$\cdot_{\Delta}$ ..... delta (difference) component related quantity
$\cdot_{\Sigma}$ ..... sigma (sum) component related quantity
$\cdot_{\mathrm{ac}}$ ..... ac-side related quantity
$\cdot_{\mathrm{arm}}$ ..... arm related quantity
$\cdot_{\mathrm{aux}}$ ..... auxiliary component related quantity
$\cdot_{\mathrm{CBF}}$ ..... CBF related quantity
$\cdot_{\mathrm{conv}}$ ..... converter related quantity
$\cdot_{\mathrm{C}}$ ..... capacitor related quantity
$\cdot_{\mathrm{c}}$ ..... control system related quantity
$\cdot_{\mathrm{dc}s}$ ..... dc pole related quantity ($s \in \{p, n\}$)
$\cdot_{\mathrm{dc}}$ ..... dc-side related quantity
$\cdot_{\mathrm{DMR}}$ ..... DMR related quantity
$\cdot_{\mathrm{dyn}}$ ..... dynamic event related quantity
$\cdot_{\mathrm{flt}}$ ..... fault related quantity
$\cdot_{\mathrm{gnd}}$ ..... ground related quantity
$\cdot_{\mathrm{line}}$ ..... line related quantity
$\cdot_{\mathrm{m}}$ ..... cell modulation related quantity
$\cdot_{\mathrm{off}}$ ..... off state related quantity
$\cdot_{\mathrm{on}}$ ..... on state related quantity
$\cdot_{\mathrm{PCC}}$ ..... PCC related quantity
$\cdot_{\mathrm{phm}}$ ..... phase-module related quantity
$\cdot_{\mathrm{pz}}$ ..... protection zone related quantity
$\cdot_{\mathrm{SM}}$ ..... SM related related quantity
$\cdot_{\mathrm{stdy}}$ ..... steady-state related quantity
$\cdot_{\mathrm{tol}}$ ..... tolerance band related quantity
$\cdot_{\mathrm{xfo}}$ ..... transformer related quantity
$\cdot_{d/q/0}$ ..... quantity in $d/q/0$-frame
$\cdot_{N0}$ ..... neutral to ground related quantity
$\cdot_{s}$ ..... upper or lower arm/subsystem related quantity ($s \in \{p, n\}$)
$\cdot_{yN}$ ..... phase to neutral related quantity ($y \in \{a, b, c\}$)
$\cdot_{y}$ ..... quantity in abc-frame or phase related quantity($y \in \{a, b, c\}$)

List of Main Superscripts

$\cdot^{+1^*}$ ..... modified quantity in positive sequence
$\cdot^{\pm 1}$ ..... quantity in positive or negative sequence
$\cdot^{\pm n}$ ..... harmonic (order n) quantity in positive or negative sequence
$\cdot^{\Sigma}$ ..... arm sum quantity label
$\cdot^{\mathrm{avg}}$ ..... averaged quantity label

$.^{\mathrm{C}xs}$ ..... converter identifier (x consecutively numbered, $s \in \{p, n\}$)
$.^{\mathrm{dc}}$ ..... dc (non-fluctuating) component label
$.^{\mathrm{droop}}$ ..... droop quantity label
$.^{\mathrm{eqv}}$ ..... equivalent (aggregated) quantity label
$.^{\mathrm{est}}$ ..... estimated quantity label
$.^{\mathrm{ff}}$ ..... feed-forward quantity label
$.^{\mathrm{FRT}}$ ..... FRT quantity label
$.^{\mathrm{hor}}$ ..... horizontal balancing quantity label
$.^{\mathrm{loss}}$ ..... loss quantity label
$.^{\mathrm{max}}$ ..... maximum of quantity label
$.^{\mathrm{meas}}$ ..... measured quantity label
$.^{\mathrm{min}}$ ..... minimum of quantity label
$.^{\mathrm{nom}}$ ..... nominal quantity label
$.^{\mathrm{ref}}$ ..... reference quantity label
$.^{\mathrm{set}}$ ..... pre-set output quantity label
$.^{\mathrm{tot}}$ ..... total balancing quantity label
$.^{\mathrm{TR}x}$ ..... cable-OHL transition station identifier (x consecutively numbered)
$.^{\mathrm{T}x}$ ..... terminal identifier (x consecutively numbered)
$.^{\mathrm{ver}}$ ..... vertical balancing quantity label

List of Accents and Indices

$\bar{x}$ ..... non-fluctuating quantity
$\dot{x}$ ..... derivative of quantity
$\hat{x}$ ..... amplitude of quantity
$\mathbf{X}$ ..... matrix quantity
$\mathbf{x}$ ..... vector quantity
$\tilde{x}$ ..... fluctuating quantity
$\underline{x}$ ..... complex quantity
$\underline{x}^*$ ..... conjugate complex quantity

Further Variables and Parameters

ΔT ..... simulation step width
ϵ_{r} ..... relative permittivity
$\mathbf{F}_{\mathrm{i}}^{\mathrm{sc}}$ ..... structurally constrained integral gain matrix
$\mathbf{F}_{\mathrm{p}}^{\mathrm{sc}}$ ..... structurally constrained proportional gain matrix
$\mathbf{F}_{\mathrm{x}}^{\mathrm{ff}}$ ..... state/output feed-forward matrix
ω_{co} ..... crossover angular frequency
ω_{c} ..... cut-off angular frequency
$\mathrm{blk}_{\mathrm{ext}}$ ..... converter-externally triggered IGBT blocking signal
$\mathrm{blk}_{\mathrm{int}}$ ..... converter-internally triggered IGBT blocking signal
$\mathrm{flt}_{\mathrm{ac}}^{+1}$ ..... ac positive sequence fault signal
$\mathrm{flt}_{\mathrm{ac}}^{-1}$ ..... ac negative sequence fault signal
$\mathrm{flt}_{\mathrm{dc}}$ ..... dc fault signal
$\mathrm{lim}_{\mathrm{low}}$ ..... lower controller limit
$\mathrm{lim}_{\mathrm{up}}$ ..... upper controller limit

ξ ..... parameter related to PLL controller tuning
a ..... parameter related to controller tuning
g ..... parameter related to PLL controller tuning
j ..... imaginary unit
k_{loop} ..... loop gain
k_{p} ..... proportional gain
$k_{i_q^{\pm 1}}$ ..... sequence-individual reactive current injection gain
l ..... length/position along the transmission line
m ..... number of SMs
r_{xfo} ..... transformer turns ratio
s ..... Laplace variable
$T_{\sigma,\mathrm{a}}$ ..... acquisition time delay
$T_{\sigma,\mathrm{c}}$ ..... control time delay
$T_{\sigma,\mathrm{f}}$ ..... filter time delay
$T_{\sigma,\mathrm{m}}$ ..... modulation time delay
T_{σ} ..... time delay
T_{i} ..... integral time constant
T_{loop} ..... loop time constant
X_{xfo} ..... transformer leakage reactance

MMC-HVdc systems in bipolar configuration present an attractive solution to tackle multiple challenges related to today‘s power systems. But, while this happens at the cost of significantly increasing system complexity, an in-depth understanding of transient behavior and dynamic characteristics is of upmost importance.

This doctoral thesis delivers a thorough analysis of fundamentals related to MMC-HVdc schemes in bipolar configuration and proposes a generic control, balancing and protection concept. Overall performance is validated by means of EMT simulations.