Modeling the Interdependencies between Voltage Fluctuation and BTI Aging

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***Abstract*—With technology scaling the susceptibility of circuits to different reliability degradations is steadily increasing. Aging in transistors due to Bias Temperature Instability (BTI) and voltage fluctuation in the power delivery network of circuits due to IR-drops are the most prominent. *In this work, we are reporting for the first time, that there are interdependencies between voltage fluctuation and BTI aging, that are non-negligible.* Modeling and investigating the *joint* impact of voltage fluctuation and BTI aging on the delay of circuits, while remaining compatible with the existing standard design flow, is indispensable in order to answer the vital question, "What is an efficient (i.e. small, yet sufficient) timing guardband to sustain the reliability of circuit for the projected lifetime?" This is, concisely, the key goal of this paper. Achieving that would not be possible without employing a physics-based BTI model that precisely describes the underlying generation and recovery mechanisms of defects under arbitrary stress waveforms. For this purpose, our model is validated against varied semiconductor measurements covering a wide range of voltage, temperature, frequency and duty cycle conditions.**

To bring reliability awareness to existing EDA tool flows, we create standard cell libraries that contain the delay information of cells under the joint impact of aging and IR-drop. Our libraries can be directly deployed within the standard design flow because they are compatible with existing commercial tools (e.g., Synopsys and Cadence). Hence, designers can leverage the mature algorithms of these tools to accurately estimate the required timing guardbands for any circuit despite its complexity. Our investigation demonstrates that considering aging and IR-drop effects *independently*, as done in state of the art, leads to employing insufficient and thus unreliable guardbands because of the non-negligible (on average 15% and up to 25%) underestimations. Importantly, considering interdependencies between aging and IR-drop does not only allow correct guardband estimations but it also results in employing more efficient guardbands.

I. Introduction

After the discontinuation of Dennard's scaling, the operating voltage started to disproportionally scale with respect to the geometry of transistors in every new generation. This has led to two key reliability problems at the device and circuit levels:
1) Strong aging effects in transistors: elevated electric fields in transistors accelerate the underlying physical mechanisms of aging. Generated defects manifest themselves as a shift in the key electrical characteristics of MOSFETs such as threshold voltage (V_{th}) [1]. In addition to ΔV_{th}, BTI can also alter other transistor parameters like carried mobility (μ), sub-threshold slope (SS) and gate-drain capacitance (C_{gd}) [2]. However, ΔV_{th} is the dominant degradation caused by BTI[1]. In turn, an increase in V_{th}, reduces the drain current of transistor in the ON state increasing the propagation delay of cells, as Eqs. 1, 2 demonstrate. Hence, timing violations in circuits occur due to unsustainable clock frequencies if insufficient timing guardband ($t_{guardband}$) was included on top of the critical path delay (see Eqs. 2, 3). Other sources of V_{th} shifts are from time-zero variability (compared to aging, which is time-dependent variability). Time-zero variability is static and occurs in addition to the time-dependent variability with negligible interdependency [3].
2) High IR-drops in circuits: elevated on-chip power densities increase the demands on the Power Delivery Network (PDN) of circuit due to high current densities. In other words, due to technology scaling, the power lanes in circuits need to deliver higher currents to function more cells within the same area. The non-ideality in PDN manifests itself as IR-drops that lead to voltage fluctuations in which every cell within the circuit receives a different reduced V_{dd} from the ideal/nominal voltage. When V_{dd} drops below the nominal level, the propagation delay of cells increases due to the direct relation between V_{dd} and cell's delay (see Eq. 2) and, additionally, due to the reduction in I_{on} (see Eq. 1). Therefore, circuits under IR-drop become subject to sudden timing violations if an insufficient guardband (to protect against unexpected delay increases induced by IR-drops) was introduced on top of the critical path delay (see Eqs.2 and 3).

$$I_{on} \approx \frac{W}{2 \cdot L} \cdot C_{ox} \cdot \mu \cdot (V_{dd} - V_{th} - \Delta V_{th}) \tag{1}$$

$$t_{delay}(CP) = \sum_{m_i \in CP} \tau_{m_i};\ \tau_{m_i} \approx \frac{CV_{dd}}{4}\left(\frac{1}{I_{onN}} + \frac{1}{I_{onP}}\right) \tag{2}$$

$$t_{clock} < t_{CP} + t_{guardband} \Rightarrow \textit{timing violations}\ \mathbf{!} \tag{3}$$

Here, m_i refers to transistors that form the critical path (CP) of circuit. τ_{m_i} is the simplified propagation delay of an Inverter [4], which is used here as an example. C represents the capacitances connected to the cell. μ and C_{ox} are the carrier mobility and the oxide capacitance of transistor, respectively.

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[1]For simplicity, our focus is ΔV_{th}. However, our approach is not limited to ΔV_{th} alone. Other parameters can be analogously included during the cell library characterization (further details in Section VI-(3) and [2]).

A. Interdependencies between Aging and IR-drop

Both aging and IR-drop degradations have been studied in detail in the last decade *but independently*. This is because aging has been typically considered as a "long-term" reliability degradation that its effects can be only observed in hours and days, while IR-drop has been considered as a "short-term" reliability degradation that its effects can be observed within microsecond regime [5]. However, advances in measurement equipment recently revealed that aging effects in current technologies can be also observed in a significantly shorter time regime [6], [7]. This is because technology scaling pushed transistors to an atomic level in which some kinds of defects can be generated and healed very fast due to e.g., quantum effects [8], [9]. In addition, technology scaling is approaching limits where displacing just a few atoms/carriers due to aging can considerably alter the key electrical characteristics of transistor and thus endanger its entire functionality.

The existing assumption of considering aging as a sole long-term degradation has led to that state of the art, when estimating aging along with voltage fluctuation, considers the average voltage over time rather than considering the dynamics in V_{dd} induced by IR-drops at runtime. *Hence, interdependencies between aging and IR-drop were hidden*. More importantly, employed empirical aging models in state of the art (e.g., [10]) are inherently limited to considering a constant V_{dd} value. Therefore, such models can only model the impact of average/maximum V_{dd} on aging but not the impact that dynamics in V_{dd} have over time on aging. This is in contrast to physics-based aging models, for example the model presented in [8], where the underlying differential equations precisely describe how defects due to BTI (i.e. breaking/recovering Si-H bonds, capturing/emitting carriers within the oxide vacancies in the dielectric, etc.) can be generated and healed over time under arbitrary voltage waveforms. *This, in turn, opens the door to investigate aging and IR-drop jointly instead of independently.*

In this work, we demonstrate that the existing interdependencies between aging and IR-drop do matter. It cannot be excluded that aging and IR-drop effects influence – at least to some degree – each other, i.e. amplify or mitigate each other, as it will be summarized in the following.

(a) Aging $\rightarrow$ IR-drop: On the one hand, aging-induced degradation (ΔV_{th}) *amplifies* the impact that IR-drop has on the delay of a circuit. This can be observed in Eqs. 1 and 2. Note that the impact of a V_{dd} reduction on I_{on} of transistor and later on the cell's delay becomes even larger when aging-induced degradation takes place (i.e. $\Delta V_{th} > 0$).

(b) Aging $\leftarrow$ IR-drop: IR-drop, on the other hand, partially *mitigates* aging-induced ΔV_{th}. A reduction in voltage actually allows some of the generated defects to heal. Therefore, IR-drop has the potential to reduce the induced ΔV_{th} and hence mitigate the deleterious impact of aging on circuit's delay.

(c) Aging $\leftrightarrow$ IR-drop: To answer the question of "what is an efficient (i.e. small, yet sufficient) timing guardband under the joint impact of aging and IR-drop?", investigating the *interdependencies* between aging and IR-drop becomes indispensable. Neglecting the *amplification* impact leads to underestimating the required guardbands and thus including insufficient guardbands (i.e. reliability will not be sustained during the projected lifetime). Neglecting the *mitigation* impact leads to overestimating the required guardbands and thus including inefficient (i.e. larger than what is actually needed) guardbands, leading to unnecessary performance losses.

Our novel contributions within this paper are as follows:
(1) We explore, for the first time, the joint impact that aging in conjunction with IR-drop has on the delay of circuits. Using a physics-based aging model, which is able to precisely consider fluctuations in V_{dd} and is validated against semiconductor measurements under a wide range of stress scenarios, we demonstrate the existing interdependencies between them and how their effects can amplify and mitigate each other.
(2) By providing existing commercial EDA tool flows (e.g., Synopsys, Cadence) with the delay information of standard cells under the joint impact of aging and IR-drops, we leverage their mature algorithms to accurately estimate the required timing guardbands of circuits to sustain reliability (i.e. keeping timing violations caused by aging and IR-drops at bay for the projected lifetime of circuit). To achieve that, we create a set of Aging-IR-Aware Cell Libraries that covers a wide range of scenarios. Libraries are *publicly available at* [11]. They are compatible with existing tool flows. Hence, designers can directly deploy them to seamlessly estimate the timing of circuits (regardless its complexity) under the joint and/or separated impact of aging and IR-drop.

II. Related Work

In the context of this paper, previous work can be divided into the following categories:

Analyzing aging and IR-drop effects: While investigating how aging or IR-drop *alone* (e.g., [12], [13]) can increase the delay of circuits has been largely explored in the past years, research w.r.t estimating the required timing guardbands due to both of them *jointly* is still in its infancy. In [5], authors assumed that the rate of ΔV_{th} change due to BTI is significantly larger than the rate of V_{dd} change caused by IR-drops and as a result it was concluded that aging and IR-drop effects can be *independently* considered. Based on that, authors calculated the overall timing guardband due to aging and IR-drop as a summation of the guardband that is required for each of them *individually*, i.e. $t_{clock} = t_{delay}(CP) + t_{guardband}(Aging) + t_{guardband}(IR_drop)$. However, we demonstrate later in our evaluation that such a methodology incorrectly estimates the required guardbands and the underestimation reaches 15%, on average, and up to 25% due to the existing interdependencies between aging and IR-drop effects, which had been neglected. Even though none of existing state of the art analyzed how dynamics in V_{dd} (when IR-drop occurs) influence the underlying mechanisms of aging, some previous work aimed at estimating how aging-induced degradation (ΔVth) might have a different impact on the circuit's delay when V_{dd} becomes lower. [14] experimentally reported the delay of a ring oscillator under the effect of aging at various voltages showing that the impact of aging-induced ΔV_{th} becomes higher at the moment of switching from a high to a low V_{dd}. Several works (e.g., [15]) focused on estimating the circuit's delay at the slow-slow (SS)

design corner – where the supply voltage (V_{dd}) is minimum – in conjunction with the worst-case ΔV_{th} that can be potentially induced by aging at the maximum V_{dd}. However, in our analysis (details in Section III-A), we show that an IR-drop may cause a reduction in V_{dd} below the minimum V_{dd} that exists is the SS corner. [15] studied the impact of ΔV_{th} due to BTI in SRAM cells under a constant V_{dd} reduction of 10% at different technology nodes. Recently, [16] showed how voltage scaling in power management schemes narrows aging-induced ΔV_{th} due to the partial recovery that happens at the low V_{dd}.

Estimating the impact of degradations on circuits' delay: To translate how a degradation (e.g., an increase in V_{th} or a reduction in V_{dd}) results in a delay increase in circuits, [17] employed a machine learning scheme after converting the CP into timing graph to estimate delay increases. Looking at a specific path is insufficient to capture how degradation affects the delay because different paths may switch their role w.r.t criticality when degradations come into play [12] – this hold even more when analyzing complex circuits like full processors. [12] proposed to characterize the standard cell library under a constant ΔV_{th} and then use the obtained "degraded' library with the Static Timing Analysis (STA) tool to estimate the resulting delay increase caused by that ΔV_{th}. While this work can accurately estimate the impact of aging on circuits, the method is inherently limited to aging standalone as it assumes an ideal voltage source in which no fluctuation in V_{dd} will occur at runtime due to IR-drops.

Limitations in existing EDA tool flows: Existing EDA tool flows for power signoff like (e.g, Cadence Voltus) are able to extract the voltage waveforms due to IR-drop across the circuit. If multiple cell libraries at varied V_{dd} levels are then provided to the timing signoff tool, the overall delay increases caused by IR-drop can be estimated through inter/extrapolations. Unlike IR-drops, to which the existing timing signoff tools are well prepared for, estimating aging-induced delay increase in circuits is not an option there yet.

Distinction from existing state of the art:
(1) We consider the interdependencies between aging and IR drop (i.e. aging $\leftrightarrow$ IR-drop) through investigating a) how aging *amplifies* the impact that IR-drop has on the circuit's delay (i.e. aging $\rightarrow$ IR-drop) and b) how dynamics in V_{dd} due to IR-drop *mitigate* aging-induced ΔV_{th} (i.e. aging $\leftarrow$ IR-drop).
(2) Our implementation is based on available commercial EDA tool flows in order to a) leverage their mature algorithms and b) remain compatible with the standard flow design of circuits.
(3) We employ our physics-based BTI model, which is carefully calibrated to predict arbitrary voltage waveforms, in order to accurately model the interdependencies between voltage fluctuations and aging.

III. Impact of IR-drop and BTI Aging on Circuits Reliability

In the following we explain the origins behind degradations caused by IR-drops and aging and how reliability is affected.

A. Voltage Fluctuation due to IR-drops

IR-drop is a fundamental property of any electrical circuit mainly due to the intrinsic parasitics (e.g., resistances and

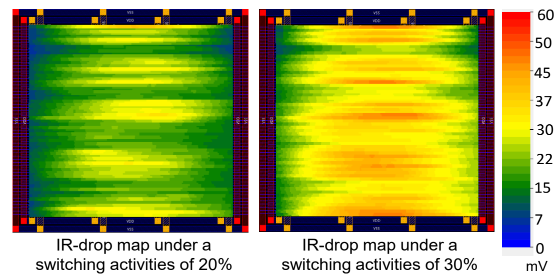

Fig. 1. IR-drop maps under different switching activity rates for a 32-bit microprocessor implemented at the 45nm technology node.

capacitances of power lanes) inside the non-ideal PDN [18], which causes fluctuations in V_{dd}. Two types of IR-drop are typically investigated when designing circuits [19], [20]:

Static IR-drop analysis: It aims at quickly obtaining a rough estimation of the potential IR-drop in the circuit in the absence of any activities. Such an analysis relies on DC analysis of the PDN considering the average power of the circuit to estimate a constant driving current in every cell within the circuit. Static IR-drop analysis guides designers early to further optimize the PDN (e.g., using wider power lanes, increase the number of lanes for better balancing, etc.) towards minimizing static IR-drop as much as possible.

Dynamic IR-drop analysis: It aims at obtaining more accurate estimations of the potential IR-drop across the chip under the impact that switching activities have. The pattern of switching activities are "driven" by the running workloads on top of the circuit. The higher the activities, the larger the drop in V_{dd} due to the rapid increase in the consumed dynamic/switching power. With each rising edge of clock, the simultaneous switching of standard cells results in peaks in driving current and thus high IR-drop as well [20], [21]. To examine the role of activities in dynamic IR-drop analysis, we demonstrate in Fig 1 the IR-drop map of a 32-bit microprocessor under two different rates (20% and 30%) of switching activities. The microprocessor has been implemented at the 45nm technology node (details in Section VII). As shown, the IR-drop noticeably increases at higher activities and it can reach more than 60mV. A voltage reduction due to IR-drop manifests itself as an increase in the circuit's delay [22], [23]. As explained in Section I, this is due to the direct impact of V_{dd} on the propagation delay of cells (see Eq. 2) and the indirect impact through lowering the I_{on} current of MOSFETs (see Eq. 1). Therefore, to suppress the deleterious impact of IR-drops, designers, in addition to optimizing the PDN, include a timing guardband on top of critical path delay of circuit (see Eq. 3) in which timing constraints are always met at runtime. Alternatively, designers may insert decoupling capacitors/cells near high switching cells in order to prevent sudden changes in V_{dd}. However, decoupling capacitors consume area and increase leakage power [24]. In this work, we focus only on timing guardbands as a means to overcome the impact of IR-drop on the circuit's delay.

Voltage Window (V_{win}): When IR-drop occurs, not only the V_{dd} drops below the nominal level but additionally V_{ss} increases above the nominal ground level (0V) as well [23]. This

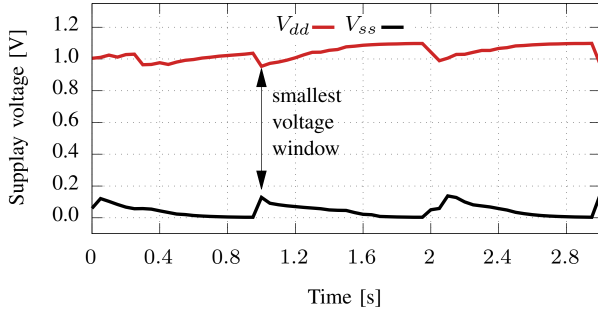

Fig. 2. V_{dd} and V_{ss} waveforms due to IR-drop extracted from 32-bit microprocessor implemented at the 45nm. As shown, the fluctuation in V_{ss} cannot be neglected and it should, similar to V_{dd} fluctuations, be considered as well. Therefore, a voltage window ($V_{dd} - V_{ss}$) needs to be considered when analyzing the impact of IR-drop on circuits' delay.

is because both V_{dd} and V_{ss} share similar power topologies over non-ideal power lanes in the PDN. Voltage by definition is an electric potential difference between two points, in this case between the points V_{dd} and ground. Therefore, considering V_{dd} fluctuations only while still assuming an ideal/nominal V_{ss} will lead to underestimating (approximately halve) the overall impact of IR-drop on circuits. In order to consider the impact of IR-drop on both V_{dd} and V_{ss}, a voltage window (see Eq. 4) [23] is typically calculated while analyzing the impact of IR-drop on the circuit's delay instead of looking solely at V_{dd}. The worst case (i.e. maximum IR-drop) occurs when the voltage window is minimum because this leads to the largest impact on the circuit's delay (see Eq. 5). In Fig. 2 we show an example of the extracted V_{dd} and V_{ss} waveforms for a 32-bit microprocessor implemented at the 45nm (details on experimental setup in Section VII). As can be seen, V_{dd} and V_{ss}, fluctuate from the nominal levels of 1.1V and 0V, respectively. The worst-case IR-drop occurs at the point where the voltage window is minimum[2].

$$V_{win}(t) = V_{dd}(t) - V_{ss}(t) \tag{4}$$

$$\text{IR-drop(Max)} = V_{dd}(nominal) - Min(V_{win}(t)) \tag{5}$$

B. Aging-Induced Degradation

BTI is one of the key aging phenomena in the current technology nodes [25] and it is predicted to also remain a key degradation in the upcoming nodes including nanowires [26]. Generated defects, due to BTI either at the Si-SiO$_2$ interface or deep within the dielectric, are undesired charges that interact (due to Coulomb scattering) with the applied electric field on a transistor [1] and, as a result, the transistor becomes "weaker" akin to an increase in the threshold voltage. As explained in Section I, ΔV_{th}, in turn, leads to a reduction in the I_{on} current (see Eq. 1) and thus an increase in the propagation delay of standard cells (see Eq. 2).

Impact of lowering V_{dd} on BTI: The underlying mechanisms of BTI are "driven" by the operating voltage (V_{dd}). Higher V_{dd} results in stronger electric fields and therefore more defects due BTI can be generated leading to a larger ΔV_{th}. However, when the V_{dd} is reduced or ceased, some of the generated defects can be healed leading to a reduction in ΔV_{th}. Thus, lowering V_{dd} leads to *mitigating* the BTI-induced ΔV_{th} due to the occurring partial recovery. Importantly, according to recent results in [8], [9] BTI is able to follow even ultra-fast voltage changes in the current technology (details in Section IV-B).

Importantly, presented measurements in [27] as well as simulation-based analysis in [16] showed that the same BTI-induced ΔV_{th} results in a larger delay increase at lower V_{dd}. This, as explained in Section I, is expected because the I_{on} current in a transistor is proportional to $(V_{dd} - V_{th} - \Delta V_{th})$ (see Eq. 1). Hence, the impact of ΔV_{th} on increasing the prorogation delay of a standard cell is *amplified* in the presence of a V_{dd} reduction.

[2]This is not necessarily at the peak ΔV_{dd} or ΔV_{ss}.

C. Bringing Voltage Fluctuation and BTI Together Into Play

When IR-drops occur, voltage fluctuations happen. As explained earlier, reductions in V_{dd} do influence BTI in two ways: a) they *amplify* the impact of induced ΔV_{th} on delay and b) they partially *mitigate* aging by reducing the induced ΔV_{th}. In fact, because the underlying BTI mechanisms can follow ultra-fast V_{dd} changes in the current technology, as demonstrated in [8], [9], it cannot be excluded that the IR-drop and BTI-induced degradation do influence each other – at least to some degree. This opens the door for the question whether interdependencies between each other do exist or not, and, if yes, what would be the consequence of such interdependencies on reliability analysis and timing guardband estimations.

IV. Interdependecies between Voltage Fluctuations and BTI Aging

In this section we first explain the underlying mechanisms of BTI and how they react to V_{dd} changes along with our employed model. Then, we discuss rates of defects generation/recovery due to BTI and whether they can react to V_{dd} changes caused by IR-drops. Afterwards, we describe how drops in V_{dd} can *mitigate* some of BTI-induced ΔV_{th} due to the partial recovery and how the BTI-induced degradation *amplifies* the impact that a V_{dd} has on the delay of circuit.

A. Impact of Voltage on the Underlying Mechanisms of BTI

BTI is the generation of defects at the Si-SiO$_2$ interface and the capture/emission of carriers in defects (e.g., oxide vacancies) inside the gate dielectric of a transistor. Both physical mechanisms are driven by the applied V_{dd} to transistor. When the gate-source voltage (V_{gs}) of a MOSFET transistor increases, the electric field over the gate dielectric rises, which provides sufficient activation energy to break the atomic bonds (e.g., *Si-H* bonds) [1]. Pre-existing defects due to imperfect manufacturing have to capture a carrier, tunneled from the channel, in order to be transferred from electrically passive (neutral) to electrically active (charged). To reach a defect embedded deep within the insulator, the channel carriers need to tunnel through (a section of) the gate dielectric through quantum tunneling. The likelihood of tunneling depends on

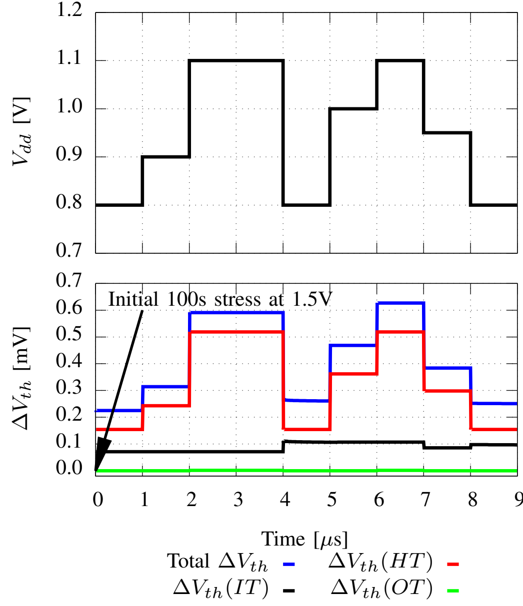

Fig. 3. Voltage dynamics governing the BTI-induced degradation (ΔV_{th}). When V_{dd} increases, ΔV_{th} increases due to BTI defects are being generated. When V_{dd} decreases, BTI recovers and hence ΔV_{th} decreases. To show non-zero contribution of interface traps ($\Delta V_{th}(IT)$) and to demonstrate interface trap and hole trap interaction, the trace was prefaced by a 100s stress phase at 1.5V mimicking a month of operation at the nominal voltage. HT reacts almost instantaneous to changes in voltage, while OT cannot contribute on this time-scale to the overall/total ΔV_{th} (further details are in Fig. 8a).

the strength of the electric field over the insulator. Therefore, applied V_{dd} plays a major role in "driving" the underlying mechanisms of defect generation in BTI because it determines the probability of tunneling and capturing carriers as well as the probability of breaking atomic bonds (e.g., Si-H bonds).

In order to properly capture the complex dependency of BTI on V_{dd}, physics-based BTI models must be employed because empirical BTI models (e.g., [10], [28]) can only macroscopically observe degradation rates of circuits and thus they cannot model/describe the underlying physical mechanisms of BTI themselves. In addition, empirical BTI models can deal solely with a constant voltage and hence they cannot be employed to investigate the interdependencies between voltage fluctuation and BTI because the latter inevitably necessitates taking voltage dynamics caused by IR-drops into account.

In this work, we employ our state-of-the-art physics-based BTI model recently presented in [8]. Our BTI Analysis Tool (BAT) consists of various models (details later in Fig. 7) to accurately model the different underlying mechanisms of BTI. BAT has been validated against measurements (details in Section V) and it is capable to predict ΔV_{th} induced by any arbitrary voltage waveforms, thanks to modeling the three defect types caused by BTI (see Fig. 7): Interface Traps (IT), Oxide Traps (OT) and Hole Traps (HT). Interface Traps (IT) are broken Si-H bonds at the channel interface or H-passivated defects at the high-k/low-k interface in the gate dielectric. Oxide Traps (OT) are the newly generated defects in the interface layer (low-k gate dielectric) in which capturing of carriers can occur. Hole Traps (HT) is capturing carriers in pre-existing defects due to imperfect manufacturing. Details on the defect generation mechanisms are available in [29].

Importantly, by modeling each of the aforementioned defect types, our BTI model is able to model the voltage dependency of BTI correctly because each defect type has a different voltage acceleration factor [8]. *Only the combination of the three defect types allows considering how fluctuations in V_{dd} impact the resulting BTI-induced ΔV_{th}.* To demonstrate that we show in Fig. 3 how the resulting BTI-induced ΔV_{th} follows changes and dynamics in V_{dd}. As can be noticed, when the V_{dd} drops, a partial recovery of the induced ΔV_{th} occurs and when V_{dd} becomes high, the BTI degradation gets accelerated and an increase in ΔV_{th} is observed.

Our BTI model consists of a set of physics-based equations for each defect type (IT, HT, OT) [8]. To provide a quantitative insight of our BTI model and demonstrate the voltage dependency, we present in the following a simplified version of the underlying equations. The equations describe IT stress (Eq. 6), IT recovery (Eq. 9), HT stress (Eq. 7), HT recovery (Eq. 10), OT stress (Eq. 8) and OT recovery (Eq. 11).

Stress:

$$\Delta V_{th}(IT) = A \cdot t^n \cdot e^{\Gamma E_{OX}} \cdot e^{\frac{-E_{AIT}}{kT}}$$
$$\Gamma = \Gamma_\cap + \frac{\alpha_{IT}}{kT} \tag{6}$$

$$\Delta V_{th}(HT) = B \cdot e^{\Gamma_{HT} E_{OX}} \cdot e^{\frac{-E_{AHT}}{kT} \cdot [1 - e^{-(\frac{t}{\tau_{HT}})^{\beta_{HT}}}]} \tag{7}$$

$$\Delta V_{th}(OT) = \frac{q}{C_{OX}} k_{FOT} \left[1 - e^{-(\frac{t}{m})^{\beta_S}}\right],$$
$$m = \eta \cdot (V_{OV})^{-\frac{\Gamma_{OT}}{\beta_S} \frac{E_{AOT}}{e^{kT\beta_S}}},$$
$$\Gamma_{OT} = \Gamma_{OT0} + \frac{\alpha_{OT}}{kT} \tag{8}$$

Recovery:

$$\Delta V_{th}(IT) = \Delta V_{IT}(EOS) \cdot e^{-(\frac{t}{\tau})^{\beta}} \tag{9}$$

$$\Delta V_{th}(HT) = \Delta V_{HT}(EOS) \cdot e^{-(\frac{t}{\tau_{DT}})^{\beta_{DT}}} \tag{10}$$

$$\Delta V_{th}(OT) = \Delta V_{OT}(EOS) \cdot e^{-(\frac{t}{\tau_R})^{\beta_R}} \tag{11}$$

A, B, K_{FOT}: pre-factors for bulk trap generation, n: time exponent, η: dispersion parameter, Γ: field acceleration factor, $\Gamma 0$: temperature independent field acceleration factor, Γ_{OT0}: voltage acceleration parameter, α_{IT}: bond polarization factor, α_{OT}: bond polarization factor, E_{AIT}: IT temperature activation, E_{AHT}: HT temperature activation, E_{AOT}: OT temperature activation, E_{OX}: oxide electric field, τ: Recovery time constant (depends on recovery bias), τ_{HT}: trapping time constant, T_{DT}: detrapping time constant, τ_{DT}: time constant for recovery, β: time constant dispersion parameter, β_{HT}: time constant dispersion parameter for trapping, β_{DT}: time constant dispersion parameter for detrapping, β_S: stretching parameter for stress, β_R: stretching parameter for recovery, $\Delta V_{IT}(EOS)$, $\Delta V_{HT}(EOS)$, $\Delta V_{OT}(EOS)$: induced degradation at the end of stress in the previous cycle.

B. Short- and long-Term BTI Degradations

BTI consists of two parts; long-term and short-term degradations. Long-term BTI degradation is due to the accumulation of

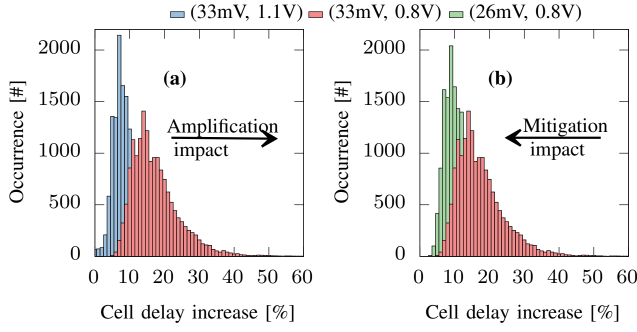

Fig. 4. (a) shows the amplification impact in which the same ΔV_{th} results in a larger delay increase in all standard cells within 45nm cell library. (b) shows how a reduction in ΔV_{th} due to BTI recovery results in mitigating the delay increases. Each pair refers to a (ΔV_{th},V_{dd}) scenario.

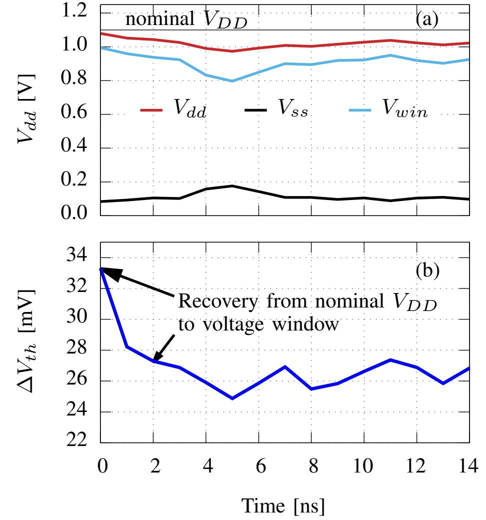

Fig. 5. (a) shows V_{dd} and V_{ss} traces during voltage fluctuation caused by IR-drop as well as the corresponding voltage window (V_{win}) trace (details on V_{win} in Section III-A and Fig 2). (b) demonstrates the resulting ΔV_{th} waveform. A drop in V_{dd} results in BTI recovery. As shown, the resulting ΔV_{th} waveform follows the fluctuations present within the V_{win} trace.

generated defects over time (e.g., hours, days). In practice, the BTI degradation is higher, the longer the V_{dd} is applied to the transistor. It is uniformly accepted, that long-term BTI follows a power law with $A \cdot t^n$ with n close to $\frac{1}{6} \approx 0.16$ [1], [8]. Short-term BTI degradation (which in this work is of interest because IR-drops are within the microsecond scale) occurs at a significantly smaller time scale. Research in the last years has changed the traditional view of BTI. Traditionally, BTI was always assumed as a pure long-term phenomenon. However, scaling transistors to an atomic level beside the advent of ultra-fast sub-microsecond transistor measurements [30], revealed that BTI is actually a very fast phenomenon in which its degradation can be observed after just a couple of μs of stress [9], [30], [31]. The measurements are in good agreement with the predictions of recent physics-based BTI model like our model that we employ in this work. As the model describes the underlying physical mechanisms of BTI, it is able to go beyond the experimental time window, which is a couple of μs, which suits well our targeted analysis in the context of voltage fluctuation caused by IR-drops.

Unlike long-term BTI degradation, which is due to interface and oxide traps (IT and OT), short-term BTI degradation is due to interface and hole traps (IT and HT). Interface traps span both short- and long-term as they break up in electron capture (see the TTOM model in Fig. 7) and traditional reaction-diffusion interface trap modeling. However, hole trap generation is significantly faster than the generation of interface and oxide traps because quantum tunneling, which the underlying mechanisms behind HT, is almost instantaneous and thus it is significantly faster than hydrogen diffusion, which is the underlying mechanism of IT and OT generation [8], [9], [31], [32]. Note that hole trapping rapidly saturates in about $\frac{1}{10}$s [8] and hence it can only contribute to the short-term part of BTI, unlike the long-term part of BTI, which is governed by the slower physical mechanisms forming IT and OT. For a detailed look at the actual individual impact across time of the three defect types, see Fig. 8(a and c) for BTI stress and recovery.

C. Joint Impact of IR-drop and BTI

As explained in Section I, aging and IR-drop can mutually influence each other creating interdependencies them (aging $\leftrightarrow$ IR-drop). On the one hand, BTI-induced ΔV_{th} *amplifies* (aging $\rightarrow$ IR-drop) the impact that IR-drop has on the circuit's delay. On the other hand, IR-drop *mitigates* – at least to some degree – (aging $\leftarrow$ IR-drop) the BTI-induced ΔV_{th} due to the partial recovery when V_{dd} is being dropped. In the following, we demonstrate how each of the two dependencies occur.

(a) The Amplification Impact (Aging $\rightarrow$ IR-drop): When the V_{dd} is lowered, the resiliency of the circuit against increases in V_{th} decreases. [16] reported that the impact that the same ΔV_{th} of 10mV has on the delay of a ring oscillator will increase from 5% to around 10% when V_{dd} is reduced from 1.2V to 0.8V. To further investigate the *amplification*, we analyzed the delay increase caused by ΔV_{th} of 33mV (which is the estimated BTI degradation after a lifetime of 1 year using our physics-based aging model) across all sequential and combination cells within a 45nm standard library at two different voltages; 1.1V and 0.8V. As can be noticed in Fig. 4(a) the distribution of the cell delay increase (caused by ΔV_{th} of 33mV) moves further towards the right side when V_{dd} drops from 1.1V (which is the nominal V_{dd} in the targeted library) to 0.8V. This demonstrates how the impact of the same ΔV_{th} is amplified when V_{dd} drops.

(b) The Mitigation Impact (Aging $\leftarrow$ IR-drop): Despite the amplification impact, IR-drop can partially *mitigate* the BTI-induced ΔV_{th}. When the voltage applied to a transistor is reduced, BTI-induced ΔV_{th} reduces. This effect is called BTI recovery. Physically, the hole traps (HT) emit their carriers back to the channel or the metallic gate. Defects within the gate dielectric and interface, i.e., oxide traps (OT) and interface traps (IT), recover by recapturing their diffusing atoms and reforming the atomic bonds. Relevant to the short-term BTI degradation, which is within the focus of this work as voltage fluctuations occur in the μs scale, recovery is governed by electron capture in interface traps as well as the hole traps because they can emit their carriers to the channel or metallic

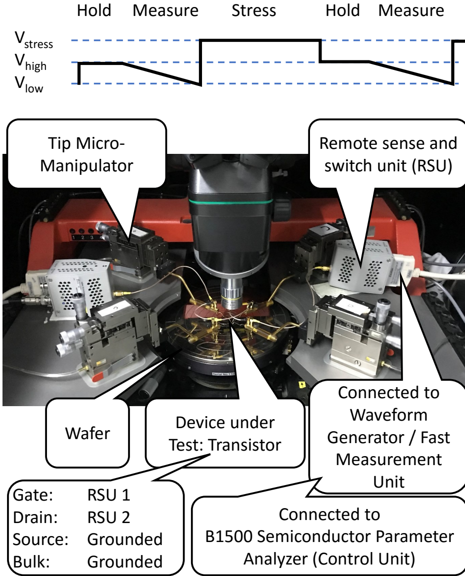

Fig. 6. Experimental setup for BTI measurements. On top, the measure-stress-measure pattern is shown, which clarifies when V_{gs} is kept at V_{stress}, V_{high} and V_{low}. The bottom shows the experimental setup itself, shown without wafer in place.

gate extremely fast (within a pico-second time scale) [8], [9]. Note that our employed BTI model is capable of modeling both mechanisms of electron capture in IT (TTOM model) as well as capture and emission in hole traps. Therefore, when analyzing voltage waveform extracted from IR-drops, the model estimates the corresponding caused ΔV_{th} waveform. To demonstrate the impact of mitigating ΔV_{th} on reducing the delay increase of standard cells, we show in Fig. 4(b) how the delay increase distribution of cells moves towards the left side (i.e. the delay increase in cells becomes less) when the ΔV_{th} gets reduced by 7mV (i.e. ΔV_{th} is reduced from 33mV to 26mV). In Fig. 5, we present an example of the resulting ΔV_{th} due to an IR-drop (experimental details in Section VII. As shown, the reduction in V_{dd} below the nominal voltage of 1.1V has led to reduction of the induced BTI-induced ΔV_{th}.
In Summary: Knowing that aging *amplifies* the impact of an IR-drop on the delay of standard cells (see Fig. 4(a)) and knowing that an IR-drop partially *mitigates* the impact of aging degradation on the delay of standard cells (see Fig. 4(b)), the key question is then; "*Can BTI recovery sufficiently reduce ΔV_{th} during IR-drop such that the amplification is compensated? Neither way, what would the small, yet sufficient timing guardband be to sustain reliability and hence overcome the joint impact of aging and IR-drop effects?*"

V. BTI Model Validation and Calibration

This section presents measurements and the corresponding BTI model predictions. These measurements validate that our BTI model was carefully calibrated to estimate the impact of voltage fluctuations on BTI. Our BTI model is able to follow the measured ΔV_{th} points for a wide variety of conditions (temperature, voltages, frequencies and duty cycles), both in short- and long-term time domains.

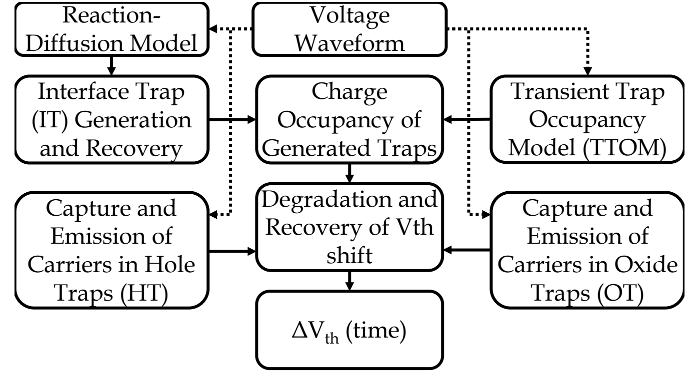

Fig. 7. Process flow of the BTI model. IT are modeled in detail, as these traps contribute to both short-term and long-term BTI and are responsible for the majority of observed BTI-induced degradation. HT and OT can be modeled simpler, while still accurately matching the measurements presented in Section V. For details refer to [8] and [32].

All measurements are obtained from our experimental setup shown in Fig. 6. The figure shows on top the measure-stress-measure pattern, which is used to obtain each point (indicated by a symbol) in the figures Fig.8, Fig.9 and 10. During the stress phase (inducing degradation at elevated voltages), the drain voltage $V_{ds} = 0V$ to prevent non-BTI degradation (e.g., hot carriers). During the measure phase, V_{ds} is set to the same value as the pre-stress IV-characterization. Then any degradation in the drain current I_D can directly be translated (with the help of the pre-stress IV-characteristics) to ΔV_{th}.

A. Short- and Long-term BTI Measurements

BTI behaves differently across the short- (e.g., micro-seconds) and long-term (e.g., hours) time domains. Fig. 8 shows how BTI breaks down to its individual physical origins, i.e. its individual defect types. Each defect type is linked to its own physical processes during generation, electrical activation and passivation of the defect. These processes in turn need different amount of time. For example, hydrogen from IT needs to diffuse through the material, which takes time, while HT might capture a channel carrier with almost instantaneous quantum tunneling. Fig. 8a) and Fig. 8c) show the individual time evolution of BTI broken down by induced ΔV_{th} by defect type. HT are extremely fast, but saturate quickly. IT start in the order of milli-seconds, but do not saturate. Instead they continue with the universal time exponent of approximately 0.16 [32]. OT are slow defect types, as they are harder to create. Therefore, in order to model the short- and long-term behavior of BTI correctly, it is paramount to model all three different defect types. HT and IT describe the short-term behavior of BTI, while IT and OT describe the long-term behavior of BTI.

As the physical processes behind the three defect types might be affected differently by temperature/voltage changes, we present Fig. 8(b) and Fig. 8(d) in which our model accurately predicts BTI during stress (Fig. 8(b) and recovery (Fig. 8(d) for three different voltage and temperature pairs. This validates that our model considers the temperature and voltage dependency of HT, IT and OT correctly, as otherwise

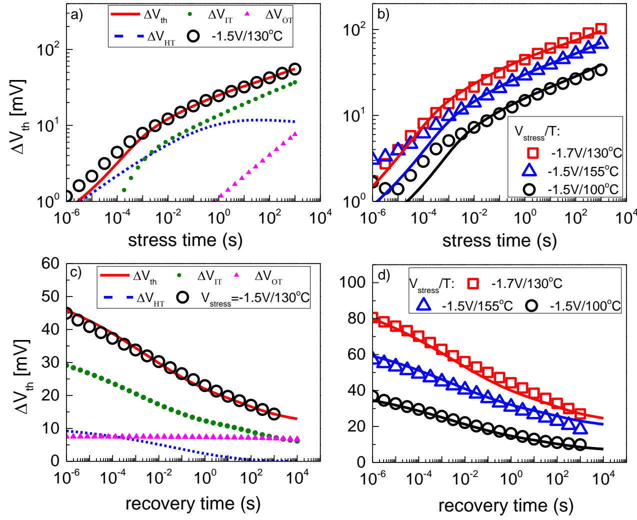

Fig. 8. Measured BTI-induced ΔV_{th} for a wide time span from microseconds ($10^{-6}s$) to hours ($10^{3}s$) under various conditions. Our model can predict BTI under different voltages and temperatures from short-term (micro-seconds) to long-term (hours). a) BTI stress is broken down to its individual physical origins, i.e. the ΔV_{th} contributions of IT, OT and HT. The initial mismatch is due to $10\mu s$ measurement delay (required time for I-V characterization) in the used experimental setup (Keithley B1500). b) BTI-induced ΔV_{th} under stress for multiple V_{dd}, T pairs to highlight how our model can accurately predict the voltage and temperature dependency of BTI. c) BTI recovery is broken down to individual ΔV_{th} contributions of IT, OT and HT. d) BTI-induced ΔV_{th} during recovery for multiple V_{dd}, T pairs.

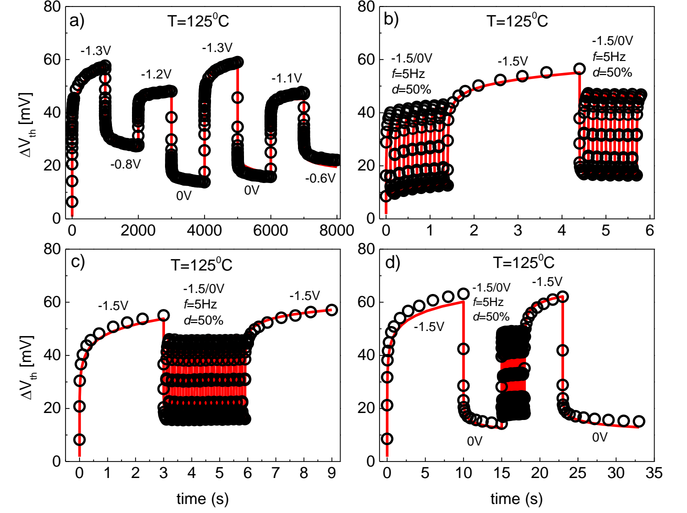

Fig. 9. BTI-induced ΔV_{th} measured (circles) compared to our BTI model (lines). a) ΔV_{th} for different V_{gs} ranging from $0V$ to $1.3V$ in an arbitrary order. b) ΔV_{th} for high-frequency, low-frequency and again high-frequency voltage fluctuations. c) ΔV_{th} for low-frequency, high-frequency and again low-frequency voltage fluctuations. d ΔV_{th} for high-frequency voltage fluctuations in the middle of a rising stress edge of a low-frequency signal.

drifts at short- or long-term time spans would be visible. The initial mismatch in our stress curve is due to the $10\mu s$ measurement delay and thus not a physically motivated mismatch, but a limitation of the experimental setup.

B. Alternating Voltage BTI Measurements

To correctly predict the impact of voltage fluctuations on BTI-induced degradation, the BTI model must be able to predict ΔV_{th} under arbitrary voltage waveforms. A voltage waveform in this context is defined by the following:

- Transistor on-/off-ratio – duty cycle d
- Switching frequency f
- Voltage of upper part of waveform V_{high}
- Voltage of lower part of waveform V_{low}

As voltage fluctuations due to IR-drops are not controlled by the circuit designer or the end-user, but instead are an uncontrollable artifact, the voltage waveforms can take any arbitrary shape. Therefore, the employed BTI model should be able to predict BTI under any arbitrary voltage waveforms. To accurately model arbitrary voltage waveforms, our BTI model has been calibrated against a wide range of on-/off-ratios d, frequencies f, high- V_{high} and low voltages V_{low} scenarios. Importantly, the BTI model should also be able to model partial recovery caused by non-zero V_{gs} (see Fig. 3).

BTI-induced ΔV_{th} recovery for non-zero V_{gs} in both measurement (symbol) and model (lines) is shown in Fig. 9(a). In fact, various switches to non-zero and zero Volt are made to re-create a complex response to an arbitrary waveform, similar to the one shown before in Fig. 3. The model closely follows the measurement, highlighting that stress and recovery can be modeled starting and ending at arbitrary voltages.

Figs. 9(b-d) show BTI under different frequencies. While Fig. 9(b) and Fig. 9(c) show alternating high- and low-f regions[3], Fig. 9(d) shows a high-f region in the rising edge of a low-f region. These measurements prove that our model is capable of modeling even complex frequency changes, not just from steady states, but also during rising or falling edges.

Lastly, to successfully validate our BTI model for arbitrary voltage waveforms, the BTI model should be able to predict BTI under different duty cycles d, frequencies f and conjunctions of frequencies and voltages. Fig. 10a) shows BTI-induced ΔV_{th} measured under different frequencies (10, 20 and $40Hz$) for a fixed $V_{gs} = 1.5V$ voltage. Fig. 10b) shows for the same frequency $f = 5Hz$ for different voltages $V_{gs} = 1.2, 1.3, 1.5V$. The combination of different voltages V_{gs} and frequencies f is shown in Fig. 10(c). Duty cycles can also be accurately predicted, as presented in Fig. 10(d).

In summary, our BTI model is able to accurately predict BTI under a wide variety of conditions. Frequencies, duty cycles and voltages can be arbitrarily chosen during both stress and recovery. In all of these cases, the BTI model can accurately track the measurements for both short-term and long-term domains and under a variety of temperatures. Therefore, our BTI model is well-suited for the prediction of the impact of arbitrary voltage fluctuations on BTI aging.

C. Different Semiconductor Technologies with our BTI Model

Our BTI model has been validated against a wide range of semiconductor technologies and has been successfully used to explain the NBTI in gate first HKMG planar devices

[3] High frequencies are 40Hz and less in this context, as even higher frequencies cannot be visualized. Our model is calibrated even at higher frequencies [32].

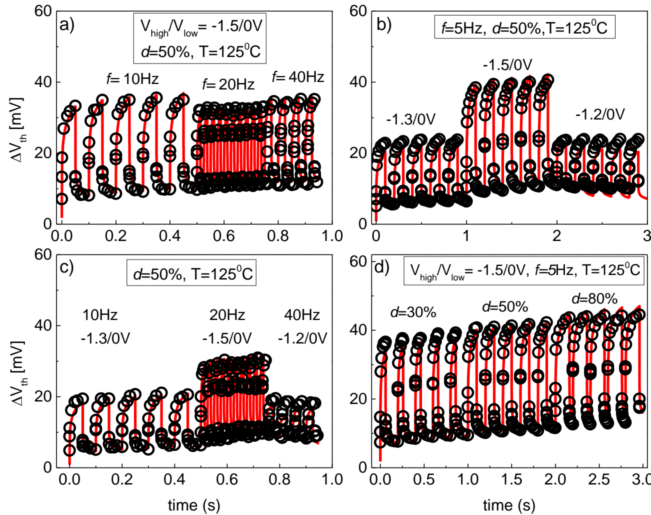

Fig. 10. a) BTI-induced ΔV_{th} measured (circles) compared to our BTI model (lines) for various switching frequencies f under identical voltages V_{gs}. b) BTI-induced ΔV_{th} under the same frequency (f), but different voltages V_{gs}. c) BTI-induced ΔV_{th} under different frequencies f as well as different voltages V_{gs}. d) BTI-induced ΔV_{th} under same frequency and voltage but at different duty cycles (d).

[8], FDSOI devices [33], HKMG Si-capped SiGe devices [34], and RMG SOI [35] and bulk FinFETs [36]. For each technology the model has to be calibrated and parameterized, but the underlying models of physical processes remained the same. Therefore, our aforementioned measurements and the further observations and trends within this work hold for other technologies.

VI. Our Implementation Linking the Physical and Circuit Levels Under Aging and IR-drop Effects

To achieve our goal of estimating an efficient (i.e. small, yet sufficient) timing guardband that protects circuits against the joint impact of aging and IR-drop, we implemented the following flow. The implementation is integrated within the commercial EDA tool flows for circuit design. This allows designers to seamlessly estimate the required guardbands for circuits. Fig. 11 demonstrates an overview of the general process flow of our approach. Our implementation is divided into the following steps (experimental details are provided later in Section VII-B):

(1) Physical design: Following the standard design flow of circuits from RTL to GDSII, the layout of the targeted circuit is created and the PDN is designed. Based on several criteria like number of power lanes, width of lanes, location, circuit's floorplan, etc. the PDN can be optimized while trading-off cost (area and power overheads) and reliability (intensity of IR-drop) [37]. Because starting from an optimized PDN is essential to properly investigate the interdependencies between aging and IR-drop, we iteratively optimize the PDN until the static IR drop becomes close to 0% and the dynamic IR-drop each of V_{dd} and V_{ss} becomes below 10%. This is similar to state of the art in PDN optimization [38], [39].

(2) IR-Drop Analysis: Using a standard power signoff tool, which is typically required before fabrication to perform necessary electrical and physical verifications for the final design, we extract the IR-drop in every cell within the circuit. To do that, the signoff tool estimates the power consumption over time of the circuit based on its switching activity. Then, it estimates the fluctuations in both V_{dd} and V_{ss} over time for every standard cell based on the electrical characteristics of the PDN (i.e. existing parasitics due to resistances, capacitances). Since at the design time, the actual activities that could be later generated by the running workloads are not yet known, designers typically perform IR-drop analysis under different switching activities. In our work, we consider switching activities ranging from 10% all the way to 80% covering a wide range of scenarios. The voltage window waveform, based on the extracted V_{dd} and V_{ss} waveforms, allows us to estimate the maximum IR-drop (where the voltage window is minimum) in every cell (see Eq. 4 and Eq. 5). In addition, we also analyze IR-drops under the actual activities caused by varied running benchmarks executed on top of the circuit for workload-dependent analysis.

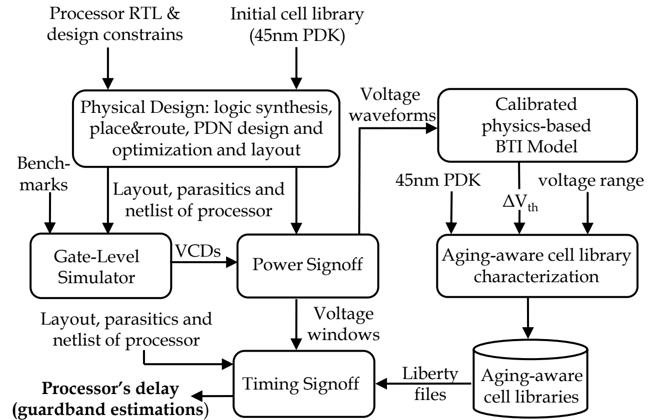

Fig. 11. A general overview of our approach demonstrating the required steps for our implementation.

(3) Aging-IR-Aware Cell Libraries: Employing our physics-based aging model, which is able to consider the dependency of BTI on V_{dd}, enables us to translate the extracted voltage window waveform to the corresponding ΔV_{th} waveform. When the voltage window waveform is applied to the gate-source voltage of transistor, the BTI model calculates the generated defects over time and then estimates the maximum ΔV_{th}. Note that BTI model will consider any potential BTI recovery when voltage starts to fluctuate below the nominal level akin to IR-drops. Afterwards, an aging-aware cell library, is created in which all standard cells are characterized in the scope of the estimated maximum ΔV_{th}. This is done using a commercial cell library characterization tool, which employs SPICE simulations to estimate the delay of every cell under the effect that ΔV_{th} has at the targeted voltage level. To cover varied voltage levels, which might be reached when an IR-drop occurs, we create cell libraries for the entire range from nominal voltage (i.e. 1.1V in the targeted 45nm cell library) to a minimum voltage of 0.6V with a step of 50mV. Our created aging-IR-aware cell libraries are available at [11].

(4) Timing Guardband Estimation: Finally, the timing sig-

noff tool employs our created cell libraries along with the extracted IR-drop profile (which contains the minimum voltage window for every standard cell within the circuit) in order to calculate how the overall delay of circuit's paths will increase. Hence, the required timing guardband under the joint impact of aging and IR-drop can be accurately estimated. Note that the fine granularity akin to having 50mV as V_{dd} voltage steps when creating our cell libraries, increases the accuracy of timing analysis because the timing signoff tool will not exhibit large errors when it needs to interpolate between the provided voltage levels.

VII. Evaluation and Comparison

In the following we first explain the implementation details for our experimental setup and then we present our evaluation demonstrating the individual and joint impacts of IR-drop and aging w.r.t timing guardbands. In addition, we compare with different state-of-the-art approaches demonstrating the necessity of considering the interdependencies between voltage fluctuation and aging to not only estimate correct guardbands but to also estimate more efficient ones.

A. Experimental Environment

The used platform in our simulations is Intel Core i7-3770K CPU with 32GB of RAM. The employed EDA tools are Synopsys Design Compiler (v2016.12-SP4) [41] for logic synthesis. The Cadence Innovus tool (v17.11) [42] is used for layout as well as PDN design. The Cadence Voltus tool (version 17.11) [43] is employed for power signoff and IR-drop waveforms extraction. Lastly, the Cadence Tempus tool (v17.11) [44] is employed for signoff timing analysis.

B. Experimental Setup

Since our implementation crosses different layers, we summarize in the following the required details at each of them.
(1) EDA Tool Flows: We used Synopsys Design Compiler for logic synthesis and Cadence Innovus for layout and PDN design/optimization. For accurate power signoff (IR-drop analysis) and accurate timing signoff (guardband estimation), Cadence Voltus and Cadence Tempus tools are employed.
(2) RTL Design: To consider a relatively complex circuit, we targeted state-of-the-art PULPino processor [45], which is a 32-bit CPU based on the RISC-V ISA. The processor has been synthesized under high-effort performance optimizing.
(3) Cell Libraries Creation: We employed the open-source 45nm Nangate library [46] to create our IR-Aging-Aware Cell Libraries (details in Section VI). To later enable a wide range of reliability analysis, libraries were created under the *individual* and *joint* impacts of IR-drop and aging effects. For library characterization, the Synopsys SiliconSmart tool has been used along with HSPICE.
(4) Circuit and Transistor Levels: We used the industrial MOSFET compact model (BSIM4.8) [47]. The model is suitable for 45nm high-k MOSFET as we target. The 45nm high-performance PTM is employed as a transistor modelcard [48]. Delay and power of standard cells are measured when creating cell libraries using HSPICE. For correct estimations, post-layout SPICE netlists for standard cell libraries are considered. Every standard cell is characterized under (7×7) input signal slews and output load capacitances.
(5) Physical Level: As explained in Section III-B, our physics-based BTI model is employed. The model has been validated against semiconductor measurements and it is able to precisely capture both short- and long- BTI degradations under arbitrary voltage waveforms within μs time scale.

C. Experimental Results and Comparisons

In this section we demonstrate our experimental results along with comparisons with state of the art. In order to cover various scenarios and for fair comparisons, we implemented and analyzed the following case studies.
(a) IR-drop alone: Timing guardbands are estimated under the impact of IR-drop alone, i.e. aging effects are not considered (i.e., $\Delta V_{th} = 0$).
(b) IR-Aging-1 (amplification impact): Timing guardbands are estimated (using our implementation) under the impact that IR-drop has together with the impact of BTI degradation. In this case, BTI aging recovery caused by IR drop is not considered (i.e., BTI stress without recovery due to constant $V_G = 1.1V$). Hence, *only the amplification impact* is investigated.
(c) IR-Aging-2: Timing guardbands are estimated as summation of both individual guardbands of aging and IR-drop *separately*, as in [5]. The average voltage (V_{avg}) across the circuit due to IR-drop is considered, similar to [5], [40] (i.e., BTI stress without recovery due to constant $V_G = V_{avg}$).
(d) IR-Aging-3: Timing guardband are estimated as assumption of both individual guardbands of aging and IR-drop *separately*, similar to [5], [40]. Unlike the previous case, the full IR-drop waveforms are here considered (instead of average voltage, i.e., BTI stress with recovery considering the entire V_G waveform.) This gives fairer comparisons against our technique, that also considers the full IR-drop waveform.
(e) IR-Aging-4 (amplification and mitigation impacts): Timing guardbands are estimated (using our implementation) under the joint impact of IR-drop and aging. Unlike case (b), BTI recovery due to IR-drop is here additionally considered (i.e., BTI stress with recovery considering the entire V_G waveform under the effects of BTI recovery. Hence, both *amplification* and *mitigation* impacts are analyzed.

In cases (b) and (c), the BTI-induced degradation is mainly governed by IT and OT, as these traps govern the long-term behavior of BTI. In cases (d) and (e), the contribution of IT/OT is altered by strong HT-induced ΔV_{th} as hole traps can capture/emit carriers fast enough to follow the dynamics in voltage waveforms.

In all analysis, a lifetime of 1 year is assumed which results in a ΔV_{th} of 33mV under BTI DC stress in the absence of IR-drops. The switching activity range from 10% to 80% (with a step of 10%) is analyzed to cover various IR-drop scenarios. For more accurate analysis, we, additionally, also investigate the actual IR-drop being occurred due to realistic switching activities caused by various benchmarks when they are executed on top of the processor. The switching activities

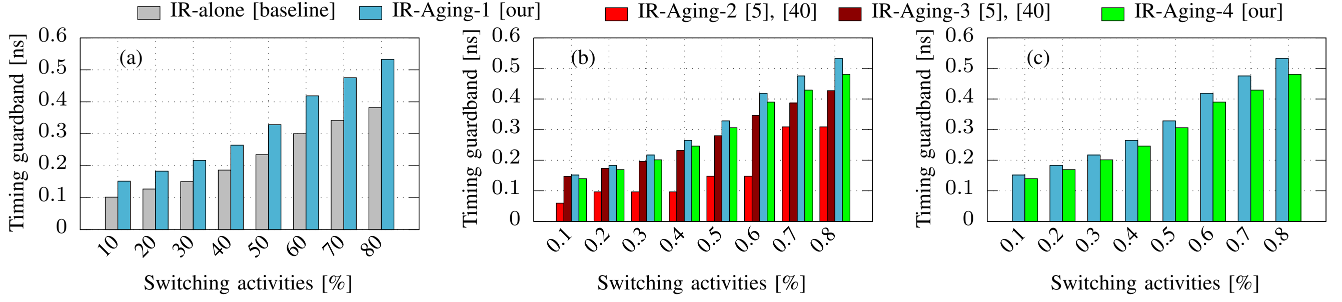

Fig. 12. Analysis under different switching activities. (a) Evaluating the *amplification impact* due to aging, i.e. aging $\rightarrow$ IR-drop. (b) Comparison with state of the art demonstrating how neglecting the amplification impact leads to underestimating guardbands. (c) Evaluating the *mitigation impact* due to IR-drop, i.e. aging $\leftarrow$ IR-drop, demonstrating how considering interdependencies, aging $\leftrightarrow$ IR-drop, is necessary to estimate efficient guardbands.

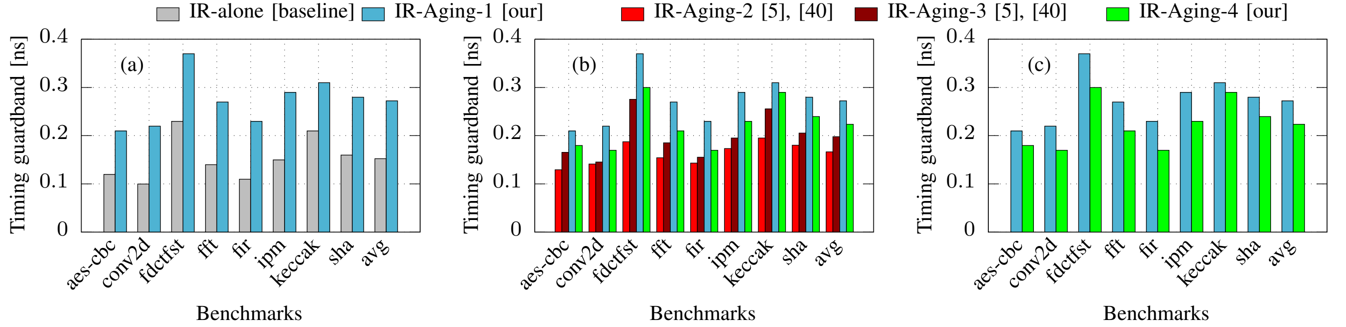

Fig. 13. Analysis under different benchmarks executed on top of the processor. (a) Evaluating the *amplification impact* due to aging, i.e. aging $\rightarrow$ IR-drop. (b) Comparison with state of the art demonstrating how neglecting the amplification impact leads to underestimating guardbands. (c) Evaluating the *mitigation impact* due to IR-drop, i.e. aging $\leftarrow$ IR-drop, demonstrating how considering interdependencies, aging $\leftrightarrow$ IR-drop, is necessary to estimate efficient guardbands.

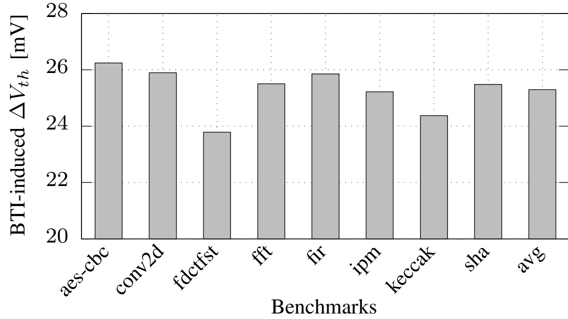

Fig. 14. Resulting BTI-induced ΔV_{th} due to the mitigation effect of IR-drop caused by varied benchmarks. The baseline BTI-induced ΔV_{th} is 33mV, which is the impact of BTI after 1 year lifetime under the operation at the nominal voltage of 1.1V. As shown, IR-drop can lead to around 24% reduction in ΔV_{th} due to the recovery impact associated with voltage reductions.

traces over time, represented by the Value Change Dump (VCD) format, are extracted using the ModelSim tool.

(1) Timing guardband analysis: Fig. 12 summarizes our results w.r.t timing guardband estimations. A timing guardband in this context is the delay increase (i.e. time slack) that is caused by degradation. In Fig. 12(a), we demonstrate how neglecting the role of aging on amplifying the impact that IR-drop has on delay (i.e. aging $\rightarrow$ IR-drop) leads to underestimating the required guardband by 30% on average and up to 49% in the case of switching activity of 10%. Fig. 12(b) shows that state-of-the-art techniques underestimate the required guardband by 12% on average and up to 20% (for the case of IR-Aging-3) and by 53% on average and up to 65% (for the case of IR-Aging-2). A lower guardband than what the processor necessitates leads to unreliable operation during its projected lifetime as the processor becomes subject to timing violations due to unsustainable clock. In Fig. 12(c), we demonstrate the impact of considering BTI recovery, caused by IR-drops, on narrowing the timing guardband. As can be noticed, the mitigation impact reaches around 8%.

In Fig. 13 we demonstrate the analysis under the actual switching activities caused by different running benchmarks on top of the processors. As shown, similar observations and trends to Fig. 12 can be still observed. In this analysis, neglecting the role of aging on amplifying the impact that IR-drop has on delay leads to underestimating the required guardband by 44% (see Fig. 13(a)) and state-of-the-art techniques underestimate the required guardband by 27% and 39%, on average, for the case of IR-Aging-3 and IR-Aging-2, respectively (see Fig. 13(b)). Finally, Fig. 13(c) shows that considering BTI recovery, caused by IR-drops, results in 18% narrower timing guardbands. *Therefore, considering the interdependencies between aging and IR-drop (which is our focus in this work) leads to not only estimating correct timing guardbands but also narrows them and hence reduces the performance overhead.*

(2) Impact of IR-drop on mitigating aging: To clarify more the mitigation impact we show in Fig. 14 the resulting BTI-induced degradation (ΔV_{th}) for every benchmark. Note that the baseline BTI degradation is ΔV_{th} of 33mV, which is the impact of BTI after 1 year lifetime under the operation at the nominal voltage of 1.1V. As can be noticed, the average ΔV_{th} is around 25mV. Hence, BTI recovery caused by IR-drop can lead to around 24% mitigation for the induced ΔV_{th}. In

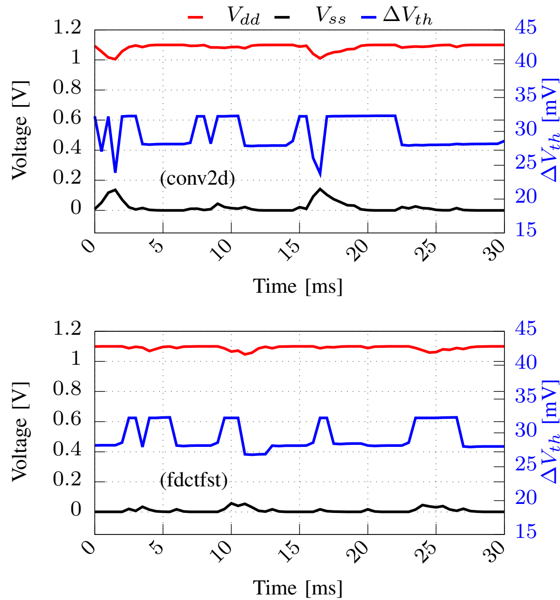

Fig. 15. V_{dd} and V_{ss} fluctuations over time due to IR-drop, caused by two different benchmarks ("conv2d" and "fdctfst"), along with corresponding BTI-induced V_{th} trace. The baseline ΔV_{th} is 33mV, which is the impact of BTI after 1 year lifetime under the operation at 1.1V.

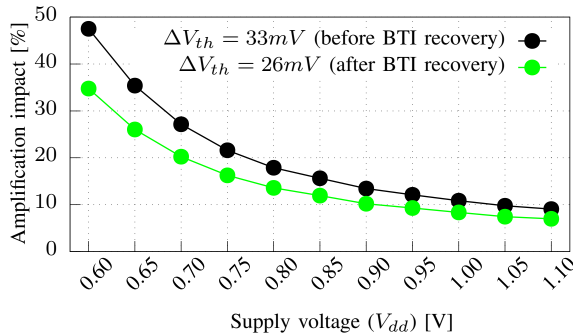

Fig. 16. Impact of aging on amplifying the induced delay increase due to IR-drop. The same ΔV_{th} has a larger impact at lower voltages. Reducing ΔV_{th} due to BTI recovery, when IR drops, mitigates the resulting delay increase.

Fig. 15, we demonstrate examples of the V_{dd} and V_{ss} traces for two different benchmarks along with the resulting ΔV_{th} trace over time. As can be seen, IR-drops result in fluctuations in both V_{dd} and V_{ss}. The larger the IR-drop (i.e. the smaller the V_{win}, see Eq. 4 and Fig. 2), the larger the reductions in ΔV_{th} because more recovery for BTI defects will be possible.

(3) Impact of aging on amplifying IR-drop impact: Finally, we present in Fig. 16 the impact that BTI-induced ΔV_{th} has on the processor's delay. We consider two cases; a ΔV_{th} of 33mV (which is the baseline BTI degradation before considering IR-induced BTI recover) and ΔV_{th} of 26mV (which is the ΔV_{th} after IR drop for the case of 30% switching activities and close to the average ΔV_{th} for analyzed benchmarks). As shown, BTI degradation amplifies the impact that IR-drop has on the processor's delay. Importantly, the mitigation impact when IR-drop occurs has a noticeable effect on mitigating the delay increases and hence narrowing the required timing guardbands (i.e. increasing the efficiency).

VIII. Summary and Conclusions

Reliability-aware circuit design flows, in which the effects of voltage fluctuations and aging are *jointly* considered, do virtually not exist. In this work, we proposed and implemented a novel approach that links physics (where degradation effects do occur) all the way up to the circuit level (where degradation effects manifest themselves as delay increases). We demonstrated, for the first time, the existing interdependencies between aging and voltage fluctuations. We quantified the impact of neglecting these interdependencies on timing guardband estimations. All in all, increasing the efficiency of circuits without sacrificing reliability (i.e. no trade-offs) necessitates accurate estimations of the small, yet sufficient timing guardbands that overcome the effects of aging as well as voltage fluctuations. *Without considering the existing interdependencies, achieving that goal would not be possible.*

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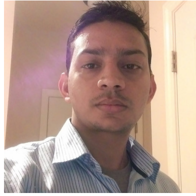

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