Long Life Single Stage PFC/SLC Converter driving LEDs

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Dr. Rainer Kling and his work group provided a fertile soil making this work possible. Special thanks to Christoph Simon for the intense discussions.

Lena, my fiancée, kept teaching me to look deeper - to lift the curtain, to explain the magic.

Without my parents I would not have arrived at this point. My deep trust in them, and theirs in me, encouraged me to accept this challenge.

Zusammenfassung in deutscher Sprache

This section summarizes the presented work in German. The English summary can be found in section 15.1 on page 175.

Licht emittierende Dioden (LEDs) sind heutzutage für Beleuchtungsanwendungen Stand der Technik und daher allgegenwärtig. Langlebige Beleuchtungsanwendungen erfordern allerdings ein robustes Systemdesign. Daher wurde die typische Ausfallursache von LED-Leuchten ermittelt: Die Stromversorgung ist mit 52% die wahrscheinlichste Ausfallursache. In manchen Anwendungen muss der LED Treiber theoretisch zehn Mal ausgetauscht werden, bevor die Lebensdauergrenze des LED-Moduls erreicht wird. Diese Arbeit beschäftigt sich daher mit der Entwicklung eines langlebigen, einstufigen LED Treibers, welcher aus einer Leistungsfaktorkorrektur (PFC) und einem Serien LC (SLC) Wandler besteht.

Ein Großteil der Ausfälle des LED-Treibers wird dabei durch den Elektrolytkondensator verursacht. Durch den Ersatz des Elektrolytkondensators durch einen Filmkondensator wird prognostiziert, dass die Lebensdauer der Leuchte deutlich erhöht werden kann. Im Abschnitt 4 werden verschiedene LED-Treibertechnologien und Topologien analysiert. Nach einer ganzheitlichen Topologieanalyse wurde die PFC/SLC-Topologie gewählt.

Die dabei verwendete diskontinuierliche totem pole Leistungsfaktorkorrektur (PFC) und der Serien LC Wandler wurden im Zeitbereich analysiert. Für beide Wandler wird der durchschnittliche Eingangsstrom bzw. der durchschnittliche Ausgangsstrom bestimmt. Da zwei Stellgrößen gleichzeitig eingestellt werden müssen, der AC-Eingangsstrom und der DC-Ausgangsstrom, sind für die Steuerung zwei Freiheitsgrade erforderlich. Die PFC- und SLC-Übertragungsfunktionen werden jeweils durch Frequenz und Tastgrad gesteuert. Dazu wurde eine Lösungsfunktion entwickelt, welche die Frequenz und den Tastgrad in Abhängigkeit von Eingangsleitwert, Ausgangsstrom und mehreren Messwerten berechnet.

Durch die Erfassung der Zwischenkreisspannung und der Ausgangsspannung wirken sich deren Änderungen nur minimal auf den Ausgangsstrom aus. Dies erlaubt einen höheren Spannungsripple am Zwischenkreiskondensator, und damit den Ersatz von Elektrolytkondensatoren durch Folienkondensatoren. Die Lebensdauer des LED-Treibers wird dadurch deutlich steigert.

Für den verwendeten Regelalgorithmus müssen mehrere Spannungen und Ströme gleichzeitig gemessen und digital gefiltert werden. Beispielsweise wird die Zwischenkreisspannung zuerst analog gefiltert, dann AD gewandelt und erneut digital durch einen resonanten Beobachter gefiltert. So kann die doppelte Netzfrequenz im Zwischenkreiskondensator herausgefiltert werden. Weiterhin wird ein Verfahren zur galvanisch getrennten Spannungsmessung entwickelt. Dadurch kann die Steuerung auf der Primärseite platziert werden, während die Sekundärseite genau gemessen werden kann. Auf Grundlage der vorgeschlagenen Messschaltung werden Schutzkonzepte entwickelt, um eine Selbstzerstörung oder

Schädigung während des Betriebs vorzubeugen.

Um die Anzahl der LEDs in einem LED-Modules zu erhöhen, z. B. um kleinere MidPower-LEDs anstelle von HighPower-LEDs einzusetzen, wird eine neuartige Parallelschaltungskonzept für LEDs entwickelt. Die Schaltung misst die einzelnen Strangströme, bildet dann einen Mittelwert aus den einzelnen Strangströmen, welcher wiederum dann als Vorgabewert genutzt wird. Auf diese Weise können LEDs sicher, und ohne Beeinträchtigung der Effizienz und Lebensdauer parallel geschaltet werden.

Für den Betrieb des LED-Treibers wird ein ausgeklügeltes Hilfsspannungskonzept zur Selbstversorgung entwickelt. Da die Regelung digital implementiert ist, ist ein tiefgreifendes Softwareengineering erforderlich, um die Echtzeitperformance der CPU sicherzustellen. Eine unzureichende Implementierung der Regelungssoftware führt zu einem instabilen Regelkreis.

Die Messungen am Ende der Arbeit zeigen, dass ein langlebiger, flimmerfreier LED-Treiber entwickelt wurde. Der Netzeingangsstrom ist dabei sinusförmig, während der LED Ausgangsstrom nahezu konstant ist. Der maximale Wirkungsgrad des LED-Treibers wurde zu 93% bestimmt.

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1 Motivation

In this section an overview over the light emitting diode (LED) itself, its history and evolution is given. Long living LED drivers are motivated, and the rationale is given why these drivers are the key for maintenance-free LED luminaires. Finally, the required technology for long living LED luminaires and its commercial limits are discussed.

1.1 History, state-of-the-art and the future of LEDs

Visible spectrum LEDs were presented 1962 [14] and were limited to the color red. The luminous power was so low that the LEDs were barely visible. Because of that, early-stage LEDs could only be used for indicators, like status LEDs. Over the years the LED luminous flux increased. Also different colors have been developed, e.g. yellow and green. The breakthrough for general lighting was the invention of the blue LED in 1994 [15]: Based on the blue light, yellow light is generated by the use of a phosphor, which then adds up to white light.

Figure 1 shows the evolution of optic flux denoted in lumen per package [3]. The future can be extrapolated using the so called Haitz law [1, 2], which is similar to the famous Moore's law [16]. Haitz law forecasts that the cost per lumen drops by a factor of 10 every decade while the flux per package increases by a factor of 20. In particular, the white LEDs evolved from very poor efficiencies to the most efficient available light source today.

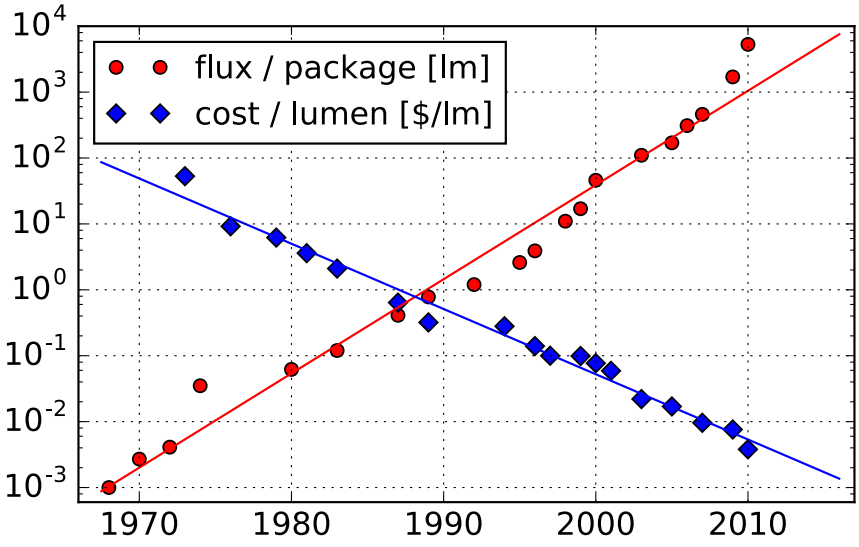


Figure 1: The Haitz law claims that the power per package increases by a factor of 20 every ten years, while the cost per lumen reduces by a factor of ten. [1, 2, 3] (Image Source: Wikimedia Commons)

The latest commercially available invention was introduced by Samsung in 2017 with the presen-

tation of a new LED model "LM301B". It has an efficacy of over 220 lm/W [17]. The limit for a perfectly white light is estimated to be at 250 lm/W [18]. Using 555 nm green, the limit is calculated to 683 lm/W [18]. Hence, LEDs are now close to the theoretical maximum efficiency. Future efficiency improvements above 250 lm/W could be possible, if non-perfect white light would be used.

1.2 LED Power Supply

LED drivers supply LEDs with power [19]. The preferred way to supply the LED chips with power is by providing a constant current [20]. Apart from the pure power supply function, recent LED drivers have several major system requirements to fulfill: A long service life is required for reduced maintenance cost and high efficiencies for reduced energy consumption.

A study by the "Building Technology Office" from the US Government, shows that 52% of all failures are related to the power supply [4] and only 10% are related to the LEDs itself. The respective graphic is depicted in Figure 2. Therefore, a true long-life power supply is required to further increase luminary reliability.

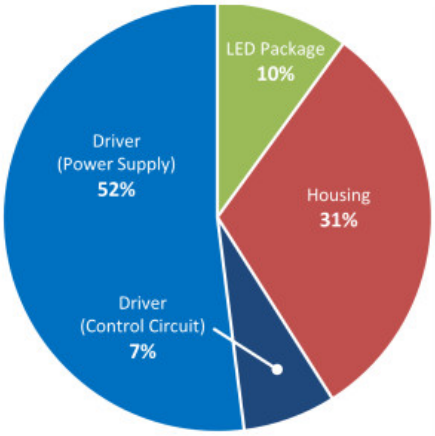


Figure 2: Percentage of failures in outdoor luminares. Graphic by [4].

As the Internet of the Things (IoT) evolution is progressing, a user control option is often designed in. The digital lighting interface (DALI), the DMX standard or wireless options like Bluetooth, Lora, or WiFi could be used. By this interface the light can be controlled and monitored. However, this adds another failure source, and is responsible for 7% of the failures [4]. This dissertation focuses on achieving a long lifetime and thus those interfaces are not further discussed.

1.3 Lifetime of Luminaires

The dominant factor that limits lifetime and accelerates aging is the temperature. Especially the temperature is critical, as the LEDs generate a significant amount of waste heat that increases the

luminare's temperature. The acceleration in aging is described by the law of Arrhenius, stating that with every 10 degrees the temperature is increased, the lifetime is halved [21]. This equation describes the chemical reaction speed. Hence, it is independent for LEDs or drivers. This aging formula can be considered only as a rough rule of thumb. Consequently, the LED luminaires lifetime can be increased by the designer by lowering the components temperature. This can be achieved, for instance, by adequately designing the LED heatsink or by lowering the LEDs electrical power. In the past, the lifetime of LED luminares as a system, were rated by default at 100'000 hours. However, these claims were inadequate estimates and were not based on scientific testing data. "[These] unsubstantiated claims can lead to significant user frustration that hinders the adoption of LED technology." , states [4, page 4]. As it will be shown in this work, the luminary lifetime is mostly limited by the power supply lifetime. Therefore adequate power supply life-testing is required.

1.3.1 LEDs

An optimistic, non standard conforming, approximation for LEDs estimates 200'000 hours of lifetime at a temperature of 65 degrees. This equals 23 years of continuous operation. Thus, for commercial applications, LEDs may be replaced due to technical innovation instead of being replaced due to defects. The details are discussed in section 2.4 on page 29.

1.3.2 Power Supplies

In contrast to the 200'000 hours lifetime of LEDs, the driver service life ranges between 20'000 h and 50'000 h [22, 23, p. 26-27], meaning that a LED power supply has to be exchanged four to ten times, before the LED module reaches its end of life. Therefore, the LED driver is typically constructed to be replaceable, not the LED module. To extend the service life of the LED luminare, a long lasting and efficient power supply is key.

1.4 Scope of the work

The scope of this work is to design a long lasting AC/DC converter that supplies the LEDs with constant current. To reduce running costs and to minimize system cooling requirements, a 90% plus efficiency is targeted. As 52% of all LED outdoor luminare failures are related to the power supply, in this work the focus is on an extended LED driver service life [4].

First a technology review is carried out, analyzing prior topologies. Typical failure issues and components are explained and common design traps are discovered to be avoided in the subsequent design process. The most promising LED driver topology will be chosen and a demonstrator is built in the

scope of this work. Its operation will be judged applying industry-standards in the measurement section 14.

After a topology analysis for power supplies, a series LC converter topology is chosen. It is similar to series resonant converters, however, it operates far above the resonance frequency of the LC filter. Mostly series resonant converters are analyzed by the first harmonic approximation, which is discussed in detail in section 7. In contrast to existing work, the converter is operated far above the LC resonance resonance frequency. As the converter is operated far above the resonance frequency, and to avoid confusion with resonant converters, the converter is renamed as Series LC Converter. This allows the use of linear equations, allowing a complete new time-domain analysis for the Series LC Converter.

The main objective of the topology analysis is to describe the LED output current as a function of the control parameters and the component values. The equations are then solved for the AC input current of the power factor correction circuit and the DC output current of the SLC converter. They can be set quasi-independently by adjusting the control values. As disturbance variables are monitored, e.g. the DC Link voltage, the converter has a high rejection capability. For increased measurement accuracy, basic parameters, like the instantaneous grid voltage, or the DC Link voltage are filtered by resonant observers that have been adopted for this work. Thanks to the detailed prior SLC analysis, the actual control can be based on a simple PI control loop system.

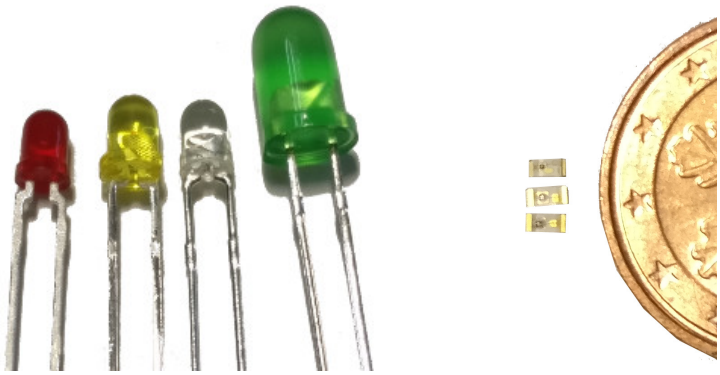
The operation of the converter is demonstrated. Quality indicators for the control are measured and are compared against legal limits. Finally a long lifetime LED driver is presented, which has imperceptible flicker and a sinusoidal grid input current.

2 LED Fundamentals

In this section an overview of typical LED genres is given and their typical applications are discussed. Two genres of LEDs, HighPower and MidPower LEDs, are compared regarding their present typical efficiencies and cost figures. In the last part, the typical construction of LED engines is discussed.

2.1 Types of LEDs

Light emitting diodes can be subdivided into three major power categories that are discussed subsequently:



(a) Through-hole 3mm (left) and 5mm (right) LEDs are shown in different colors.

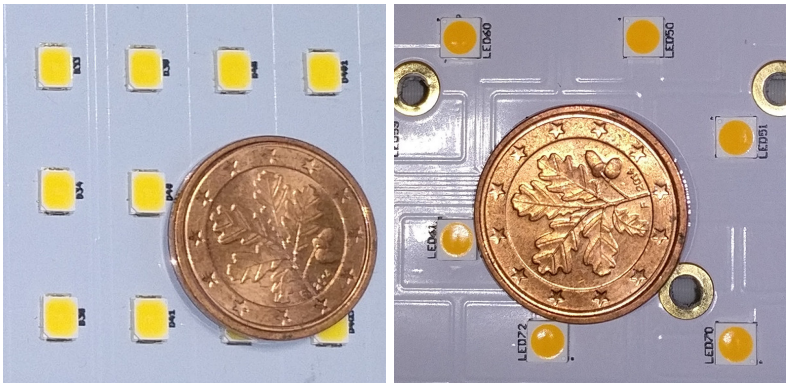
(b) 0603 SMD LEDs in comparison with a coin.

Figure 3: Indicating LEDs are used for status indication, having low optical and electrical power. They are available in through hole and surface mount technology.

Indicators Indicators have low optical power and have a typically non-white color, like red, yellow, green or blue. Indicators are not intended for illumination purposes, and hence have low electrical power, typically sub 50 mW. Examples of indicating LEDs or indicators are shown in Figure 3. Indicators are mostly driven by a constant voltage, where the series resistor limits the LED current. In most applications indication LEDs are connected directly to the IC, for instance a microcontroller.

MidPower MidPower LEDs are defined to have an electrical power of below 1 W. These LEDs can be used for general lighting. A common application is the replacement of fluorescent tubes by LED retrofit tubes. Some rare models of MidPower LEDs are also available in other colors than white. An application that uses colored LEDs are wall washers.

MidPower LEDs also can be used in street lighting, one example is shown in Figure 4. One model of standard MidPower LEDs is the Luxeon 2835. It has a typical 3 V forward voltage and 120 mA



(a) Model "Luxeon 2835" by Lumileds (b) Model "Luxeon 3030HV" by Lumileds

Figure 4: White MidPower LEDs used in general lighting applications.

forward current. Special models, so called high-voltage LEDs, have a relatively low maximum forward current (25 mA-50 mA) but a high forward voltage, typically of 12 V to 24 V.

MidPower LEDs typically have a relatively low power density. Thus, their cooling requirements are relaxed. Also their average luminance is reduced, hence their direct glare is reduced. To build a system for general lighting or street lighting a vast number of LEDs is required. Conventionally, LEDs are series-wired. However, a vast number of series LEDs leads to a high driving voltage. To lower the LED driving voltage, a novel current sharing approach is proposed in section 5 of this work. A large number of MidPower LEDs can then be arranged in an arrays and operated safely at a low voltage.

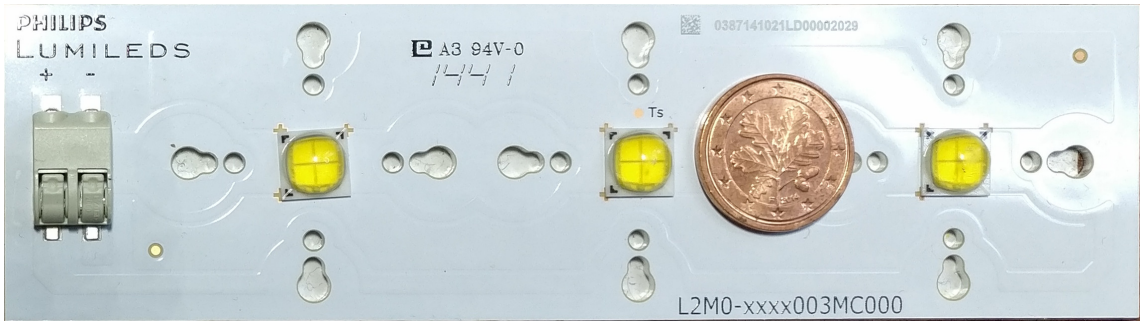


Figure 5: HighPower LED Module with three 10 W Luxeon-M LEDs. The PCB is produced by Philips and is available in a standardized format for easy deployment.

HighPower HighPower LEDs are used, as the name implies, for HighPower applications. Typical applications are flashlights, flood-lights, down-lights or streetlights. HighPower LEDs are mainly available in blue or white color. Street lighting companies may buy the LED panels prefabricated. An example is shown in Figure 5, showing three HighPower LED. The module is produced by Philips-Lumileds.

HighPower LEDs, as the Luxeon-M, use a ceramic body that conducts the heat directly to the PCB. On the PCB special cooling pads are designed-in to reduce thermal resistance to ambient. The ceramic

body is resistant to chemicals and is therefore preferred in harsh environments.

Chip on board (COB) LED describes a special construction technique, which mostly uses high power LEDs. They group several identical high power LEDs, typically densely packed, and they share one common phosphor. This allows a dense packaging of LEDs, resulting in small size LED emitters. However, the construction of optics is quite difficult, as multiple light emitters are present. In street lighting, COB LEDs are rarely observed.

2.2 Comparison of HighPower / MidPower LEDs

LEDs can be compared regarding two criteria: One is the efficacy, measured in lumen per watt (lm/W). The other criteria is the cost per light output, measured in lm per Euro (lm/€). As the market is highly volatile, the situation may change radically within some months or years. As the variety of LEDs is vast, only some few selected LEDs are compared relatively to each other in the following comparison.

2.2.1 Efficacy

The efficacy of LEDs is measured in Lumen/Watt. Two typical models of HighPower- and MidPower LEDs are compared in Table 1. It can be observed that the MidPower LEDs are far more power efficient than the HighPower LEDs.

Type of LED	**HighPower**		**MidPower**	
Partnumber	*Lumileds Luxeon M*	*Cree XP-G2*	*Lumileds 2835*	*Cree J-2835*
$P_{\mathrm{Electric}}[\mathrm{W}]$	8.7	3.87	0.37	0.45
$\Phi_{\mathrm{v}}[\mathrm{lm}]$	920	540	58	75
$\Phi_{\mathrm{v}}/P_{\mathrm{Electric}}[\frac{\mathrm{lm}}{\mathrm{W}}]$	105	139	156	166

Table 1: Efficiency comparison of MidPower LED vs HighPower LEDs: A lower drive current leads generally speaking to a higher efficiency. Efficiency improvements on 40% in terms of lm/W can be achieved, when using MidPower LEDs compared to HighPower LEDs.

2.2.2 Cost per light output

The cost per light output of LEDs is measured in lumen per euro (lm/€). The previous models, as listed in Table 1, are compared in Table 2 regarding the cost per light output. It can be observed that the MidPower LEDs are far more cost effective compared to HighPower LEDs.

Pricing also depends on other non-technical conditions, as customer-relationship or negotiation skills. Therefore, prices should only be compared relatively to each other from a catalog distributor.

Type of LED	**HighPower**		**MidPower**	
Partnumber	*Lumileds Luxeon M*	*Cree XP-G2*	*Lumileds 2835*	*Cree J-2835*
$C_{ost}[\text{Euro}]$	5.3	1.2	0.072	0.025
$\Phi_{\text{v}}[\text{lm}]$	920	540	58	75
$\frac{\Phi_{\text{v}}}{C_{\text{ost}}}[\frac{\text{lm}}{\text{Euro}}]$	173.60	450	806	3000

Table 2: The typical cost per light output of HighPower and MidPower LEDs are compared against each other: The table shows that MidPower LEDs are up more then 6 times more cost efficient than HighPower LEDs.

2.3 Construction of LED Engines

LEDs are wired and mounted on a printed circuit board (PCBs). The PCB ensures mechanical stability and cools the LEDs. These LED-PCBs are designated as "LED engines" [24].

2.3.1 Overview

Most LED engines are constructed in surface-mounted LED technology on a single layer insulated aluminum board [25]. The typical construction technique is shown in Figure 6: It consist of a connector, to which the cables are connected. The copper traces (Cu) connect each LED. An insulator separates the copper from the aluminum base plate underneath.

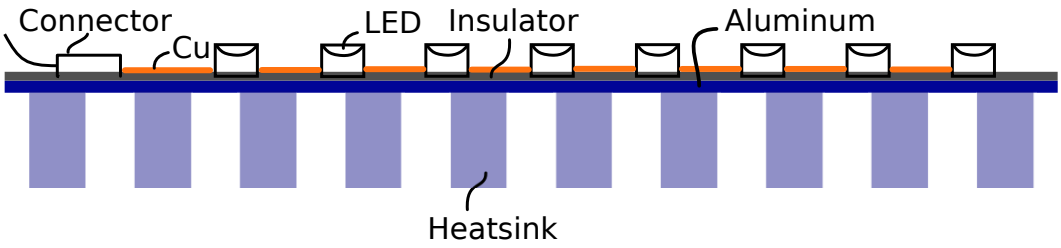


Figure 6: A LED engine consists out of connector, the copper traces for wiring, an insulator and below an aluminum base-plate for mechanical stability and thermal conductivity. Additionally a heatsink is often utilized for maintaining low operating temperatures for long product lifetime.

2.3.2 Thermal influences on LEDs

Even though LEDs are fairly efficient, they produce a significant amount of waste heat that has to be distributed and conducted away. To cool the LED engine, an additional heatsink is placed underneath.

As previously mentioned, the lifetime increases by a factor of 2 with every ten degrees of temperature decrease. Thus, the adequate design of the LED cooler determines the LED engines lifetime. One relatively easy method to achieve low temperature, is by extending the surface area of the PCB copper pour and the adjacent cooler. Novel approaches additionally use natural air ventilation, making use of the chimney-effect.

As depicted in Figure 7, the LEDs light output reduces with an increased temperature. Therefore, to construct the most efficient luminare, a lowest possible operation temperature must be maintained. For instance, operating an LED at 80 °C instead of room temperature (25 °C), reduces the light output by about ten percent.

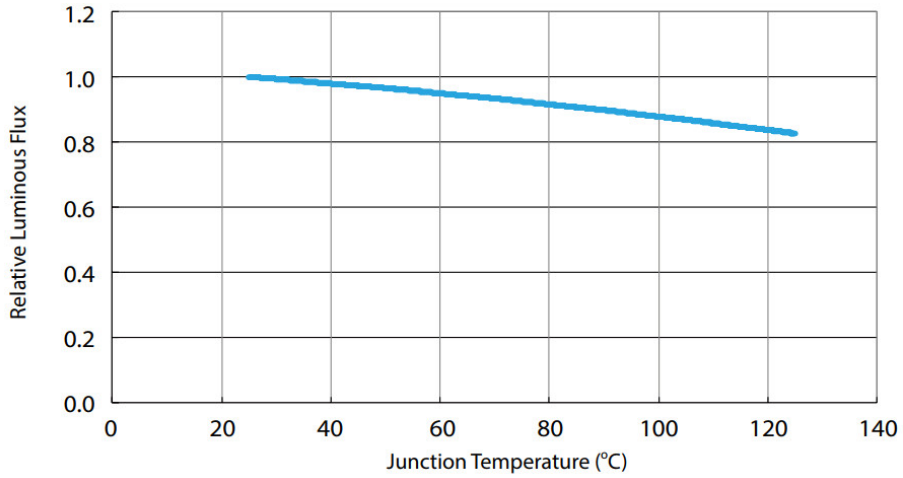


Figure 7: The light output of LEDs decreases with the increase of temperature. Exemplary data of the Edison 2835 LED is shown [5].

In some low end products, low end LED engines with FR4 board material are used. In that case, the aluminum base plate in Figure 6 is replace by the FR4 material, which is a mash of glass fiber filled with epoxy. FR4 has a significantly reduced thermal conductivity, thus the LEDs will work at higher temperatures. Considering Arrhenius lifetime law, this construction technique should not be considered for long life LED engines.

2.4 Lifetime of LED Luminares

Two typical LED models are analyzed regarding their lifetime. It will be observed that LED drivers are the bottleneck for long lasting LED systems.

2.4.1 HighPower LEDs

A study from Lumileds in Figure 8 estimates 148k hours of lifetime for a degradation of 70% [6]. Arrhenius's law states that 10 °C decrease in operating temperature doubles the LED lifetime.

Typical LED junction temperatures range between 40°C and 100°C. Hence, this analysis of the Luxeon Rebel in Figure 8 can be considered close to a worst case scenario.

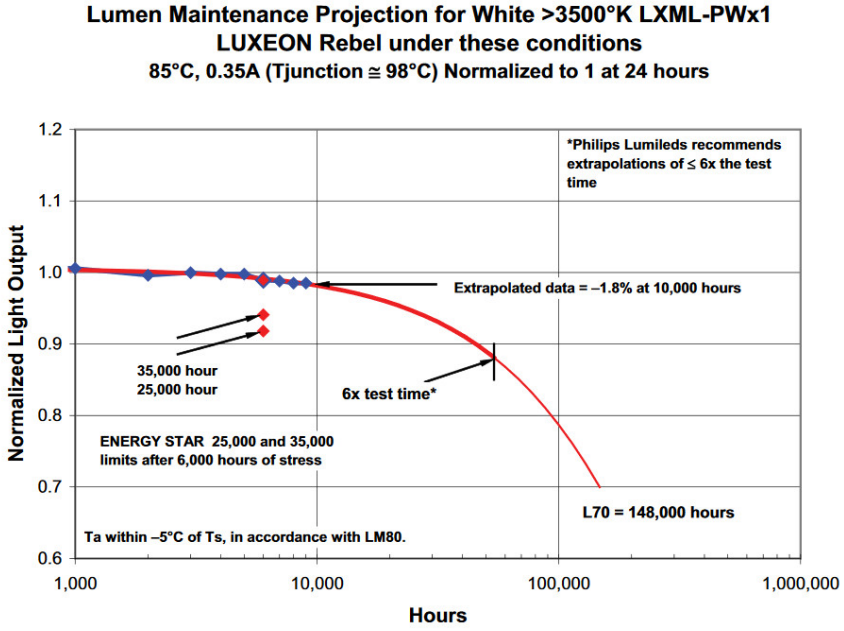


Figure 8: Lifetime of LEDs at high temperature operating conditions, based on a Lumileds study[6].

2.4.2 MidPower LEDs

Typical LED test data for MidPower LEDs shows that for a 10% luminous flux decrease a lifetime of 49'700 hours at 85°C is estimated [26]. Using the law of Arrhenius, at 65°C a lifetime of 198'800 hours is estimated, corresponding 22 years of continuous operation. If a flux decrease of 20% can be tolerated, a further increase in lifetime can be achieved.

2.4.3 Lifetime of LED Drivers

As the LED modules, according to [6], have an estimated lifetime of at least 148,000 hours, long lasting power supplies are also required, reaching at least 150k operating hours. Therefore, in this work, typical failure issues of power supplies are discovered. The discoveries and conclusions are considered in the design process of the long lifetime LED driver.

2.4.4 The Limit of Lifetime

Typically every year to two years a new LED generation is presented: Thus, after 22 years of lifetime, at least eleven product generations will have passed. The improvement during these generations will be significant, so even if LEDs could work longer, their performance will be obsolescent. Thus, a lifetime exceeding 22 years is not commercially required.

2.5 Summary

It has been shown that typical LED engines last up to 22 years. Two major types of LEDs for general illumination were discussed. It was discovered that MidPower LEDs are superior regarding efficiency and cost. During the life of an LED luminare, its power supplies must be exchanged 5 to 10 times. Thus, the bottleneck are long lasting power supplies. These are required to have the same endurance as the LED engines itself. After that improvement, a further extension of lifetimes seems commercially non-attractive, as the technology will have significantly advanced within two decades.

3 Requirements on LED drivers

The section discusses the requirements for LED drivers and motivates why LEDs should be driven with constant current. It covers the selection process of LED drivers, its electric safety and technical requirements.

3.1 Definition LED driver

Every electronic device, capable of lighting up LEDs can be considered as an LED driver. LED drivers supply the LED engine with the required current in the correct shape. LED drivers come in different degrees of maturity, ranging from a single component to digitally controlled power supplies. LED drivers require different types of power sources. Humble LED drivers may require a regulated input, for example a controlled voltage. LED drivers obtain their power typically from the public electric grid. However, also LED drivers, relying on solar energy have been demonstrated.

Further the driver must comply with legal standards. To reduce electric power cost, electrical conversion efficiency should be maximized.

3.2 Driving LEDs

This subsection discusses the fundamentals of LEDs and subsequently their power delivery requirements.

3.2.1 Characteristics of LEDs

Light emitting diodes, as their name implies, have a diode characteristic. A typical LED current-overvoltage curve is shown in Figure 9. At the LEDs operating point, a small change in voltage results in a exponential change in forward current. Thus, the LED power changes drastically with varying input voltage.

The temperature dependence of a typical typical LED is shown in Figure 10. It can be seen that the forward voltage drops when the temperature increases. If the LEDs would be driven by a constant voltage, a decreased forward voltage results in an increased current, resulting in a higher power dissipation, leading to increased heat generation at the LED.

Further, LEDs encounter production spreads. Therefore, LEDs are grouped in so called voltage bins. Typical voltage bins from a commercial product [5] are reproduced in Table 3. Assuming the worst case, a forward voltage variation of one LED to another can be up to 240 mV. As LEDs have an exponential current characteristic, a small change in voltage results to an exponential change in LED forward current. A voltage difference of 240 mV, according to Figure 9, leads to a current mismatch of up to 100%.

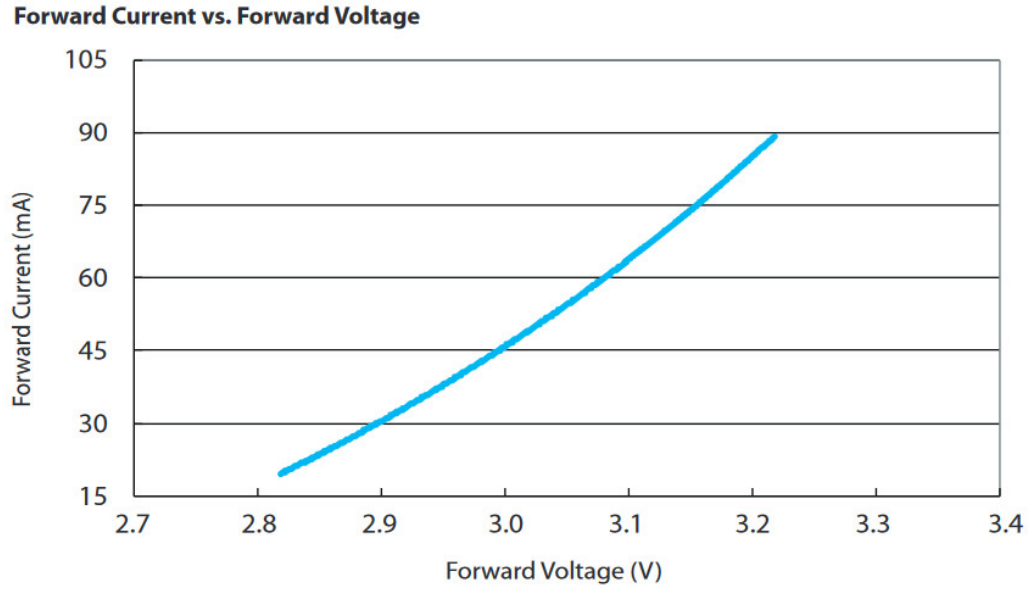


Figure 9: The voltage over current is depicted for the Edison 2835 LED [5]. Clearly the exponential characteristic of the LED forward current can be observed. A small change in voltage leads to a significant change in current.

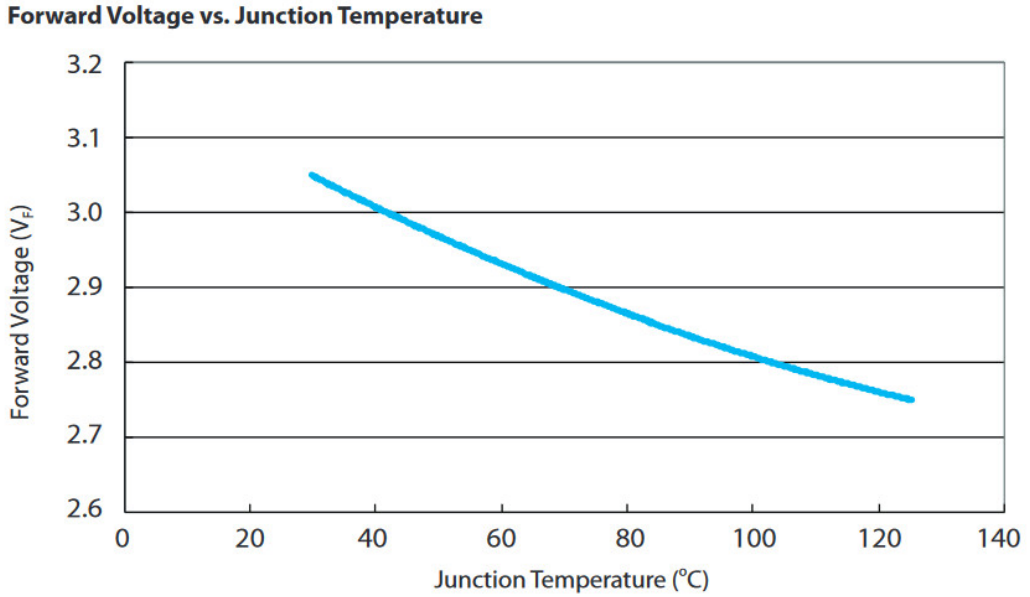


Figure 10: Temperature dependence of the forward voltage over the temperature for the Edison 2835 LED is shown [5]. The higher the LED junction temperature, the lower is its forward voltage.

Group	Min. Voltage [V]	Max. Voltage [V]
VB1	2.9	3.0
VC1	3.0	3.1
VA2	3.1	3.2
VB2	3.2	3.3
VC2	3.3	3.4
VA3	3.4	3.5
VB3	3.5	3.6

Table 3: Forward voltage bins and variation of Edison 2835 LEDs. The voltage measurement uncertainty is plus-minus 0.06V. Data reproduced from [5].

3.2.2 Voltage vicious cycle

When driving LEDs with constant voltage, especially when paralleling two LEDs, a vicious cycle may be observed that is shown in Figure 11. Initially a lower forward voltage is observed that may have its cause in production tolerances or unequal thermal distribution. As the forward voltage decreases, the LED current rises exponentially, as it can be seen in Figure 9. As more power is dissipated in the LED, its temperature rises. A higher temperature leads to a lower forward voltage, as seen in Figure 10, further increasing the current.

If excess power is dissipated in a LED, it ages faster and may fail finally consequently. The failure of flip-chip LEDs in most cases results in a short-circuit. If the LEDs where paralleled or driven in series with constant voltage, the remaining LEDs would encounter an additional voltage. The string forward voltage increases slightly, while the current increases exponentially. This leads to increased power dissipation, lowering the LEDs forward voltage further. The increasing power dissipation accelerates aging, closing the vicious cycle.

Hence, direct paralleling may only be used, if the LEDs where driven with a significant power reserve. The author recommends ten percent of their rated power. However, then, the LED engines power potential cannot be fully utilized. Hence, this approach is discouraged.

To overcome this victorious cycle LED luminary must not share a common voltage. This can be achieved by not paralleling LEDs without special precautions. Hence, LEDs should only be series wired, increasing the total string voltage. However, this approach has also its limits, for instance if 300 LEDs would be used in a luminare, a typical supply voltage of 900 V would be required. In the chapter 5 a special circuit for paralleling LEDs is proposed.

3.2.3 Driving LEDs

LEDs should be driven with constant current [20] for the following reasons:

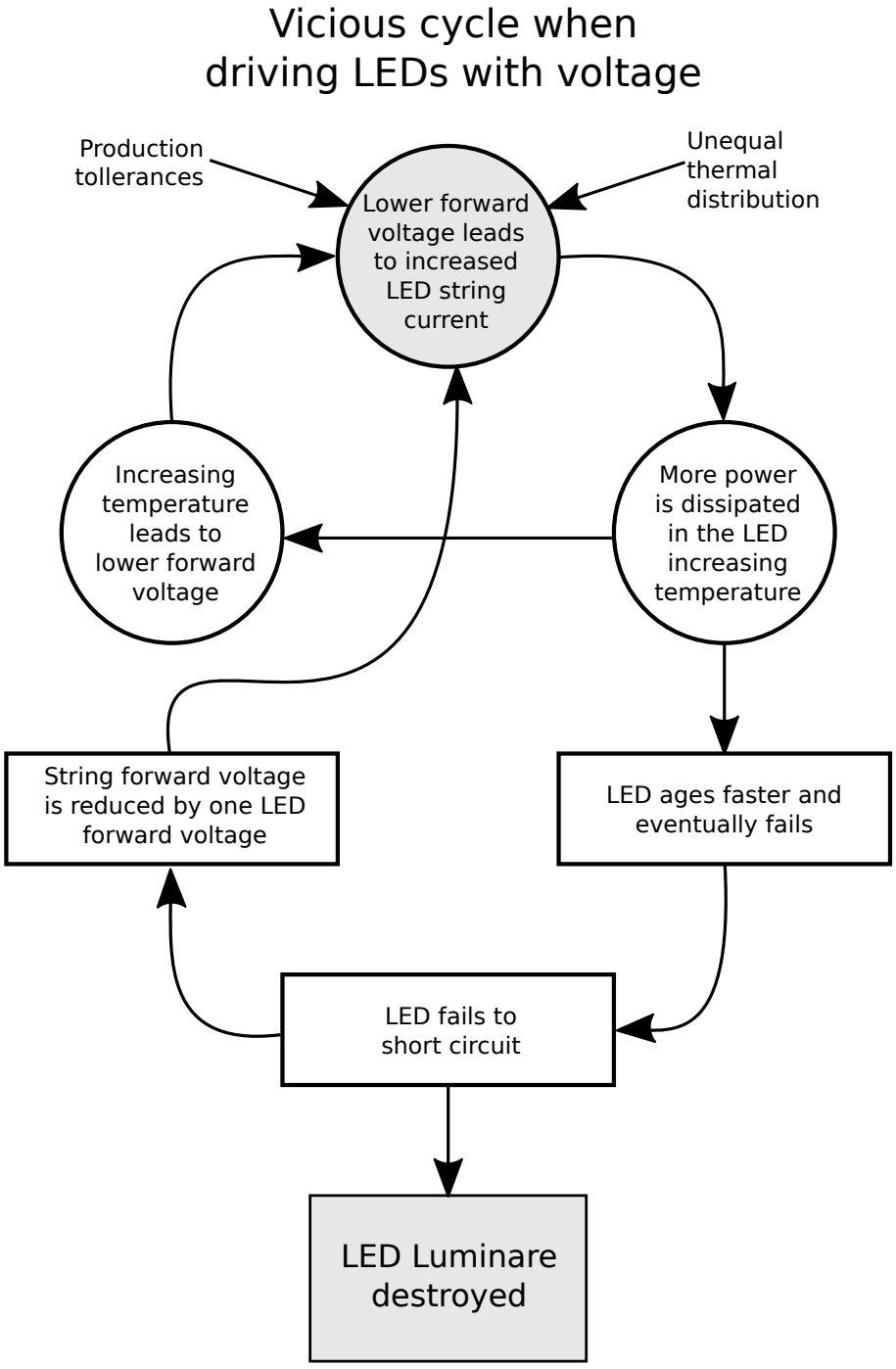


Figure 11: A vicious cycle when driving LEDs with a constant voltage can be observed due to their exponential current characteristic. In the best case, lifetime is reduced, in the worst case the LEDs are destroyed.

- The reliability is increased, by avoiding excess current or power flowing through the LED.
- The luminous intensity is more predictable and controllable when its driven with continuous current.
- Constant current reduces the flicker while dimming when compared to PWM dimming.
- No spectral emission change due to varying LED current.

Hence, LEDs must always have an individual current source. Several LEDs may be driven in series, however, never in parallel. In chapter 5 a solution for efficiently paralleling LEDs is proposed.

Apart from the requirement that the LED current has to be controlled, LEDs are an easy to handle and forgiving load. General switch mode power supplies can easily be adjusted to provide constant current for LEDs.

3.3 Selecting LED drivers

LEDs are available in a vast variety: Different colors, color temperatures, manufacturers, styles, and sizes, to name a few parameters. Also the viewing angle of the LED, mounting style (through-hole or surface-mount), packaging, efficiency and applications may vary over a broad range. Even non-visible wavelengths are available: Ultra-violet (UV) LEDs can be used for curing application or lithography processes, e.g. for etching PCBs. Infrared LEDs can be used for data transmission, for instance in TV remotes.

However, for driving LEDs only two parameters are required to be known, so the design of LED supplies is straight forward.

- The LED forward current, the so called "led drive current": I_{LED}
- The maximum forward voltage: U_{LED}

The driver has to be selected according to the current and the voltage. As only two major criteria have to be considered during the design, selection of LED drivers is easy and straight forward. This flexibility allows a vast number of combination possibilities.

3.3.1 Design Example

The following design example shows the simplicity of LED driver selection procedure. If 10 LEDs with a forward voltage of 3 V are to be supplied with 700 mA, a constant current 700 mA driver with 30 V minimum voltage has to be chosen. Typically some additional voltage headroom is provided.

3.4 Electric Safety

The following section covers the possible protection principles against electric shock.

3.4.1 Protection Categories

The 230 V AC grid, can provide significant amount of power. As the electric body also conducts electricity, it may be harmful to humans. To prevent injuries, two levels of protection are possible:

- Protection by rule: Specific security rules must be obeyed to avoid injuries. E.g. the power must be disconnected before working on a device.
- Protection by design: The device may not harm the human by design, even if the rule is not obeyed. E.g. on an error the device actively shuts down without causing damage to humans.

Obviously, the protection by design should be preferred, as it offers an increased security level. The protection by rule should only be used, if the protection by design cannot be achieved.

3.4.2 Safety low voltage (SELV)

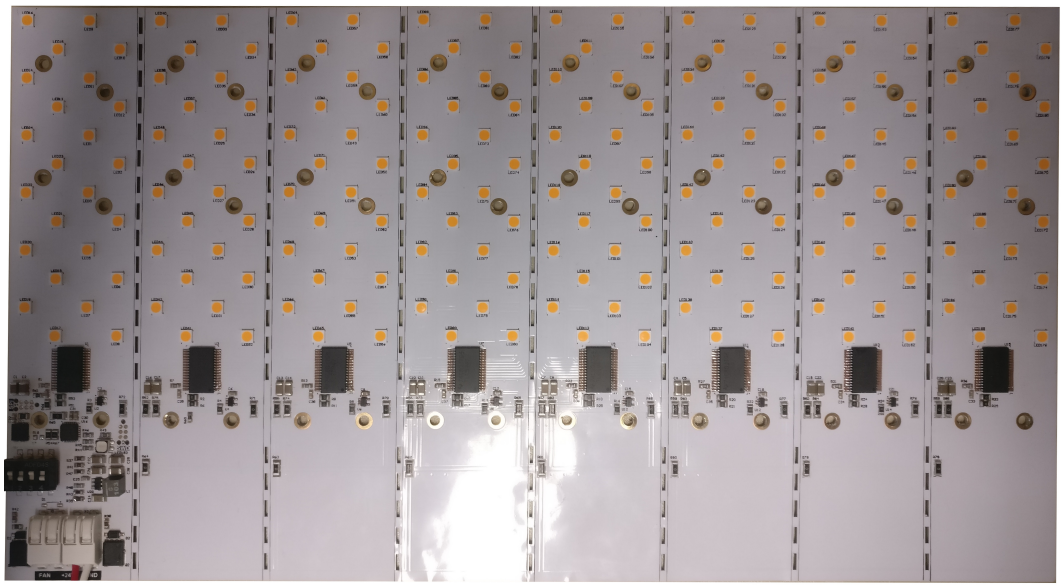


Figure 12: This LED engine is used in LED street light luminaries. It may be directly touched, as safety extra low voltage (SELV) below 60 V is used. Hence, this PCB is inherently safe.

Safety extra low voltage (SELV) means that the maximum voltage is limited to a specific value. SELV is a protection by design and thus is inherently safe. For DC, 120 V is considered as limit according to VDE [27]. Special applications require additional safety margin, considering 60 V DC as the limit.

Typically, LED engines are protected by design: This means, the LED engines can be directly touched when the case is opened by an operator. For that reason, maintaining SELV is always recommended. It

is required by challenging customers, like Deutsche Bahn [28, page 3-4] for their LED drivers. However, maintaining SELV is not mandatory for LED luminaries, if other safety precautions are taken.

3.5 Converter Efficiency

The typical LED driver efficiency ranges between 80% and 95%. If a 50 W LED has to be driven, a power of 53 W up to 62 W is drawn from the grid. A rule of thumb in street lighting states that one watt saved in power equals one 1 Euro per year saved in electricity costs in Germany. Thus, 9 Euro per year can be saved. Assuming a service life of a streetlamp of 20 years, 180 Euro can be saved: The price of a typical LED street lamp.

Therefore, the converter efficiency should be maximized to minimize electric power costs. The cost of electric power is several times higher then the setup cost of the luminare. Thus, optimizing for efficiency reduces the total cost of ownership significantly.

3.6 Grid Compatibility and Safety

The converter must comply with grid standards to be legally operable. Present IEC standards are discussed in the following section.

3.6.1 Power Factor / Total Harmonic Distortion

The power factor, PF, should be as close to one as possible to reduce the stress to the grid. Further, reducing harmonic currents also reduces reactive power. To fulfill this requirement, an active power factor correction is required.

The legal limits for harmonics, that must be fulfilled by a converter are depicted in Figure 13.

3.6.2 Transition During Missing Power

During short time power outages, e.g. a missing period of the grid sinusoidal waveform, the device should continue operation. A switching converter outage would result into flickering of the LED current, which is not desired.

3.6.3 EMC Emissions

The EMC emissions must comply within the legal limits. The corresponding limits are denoted in IEC 61000-3-2 and reproduced in Figure 13.

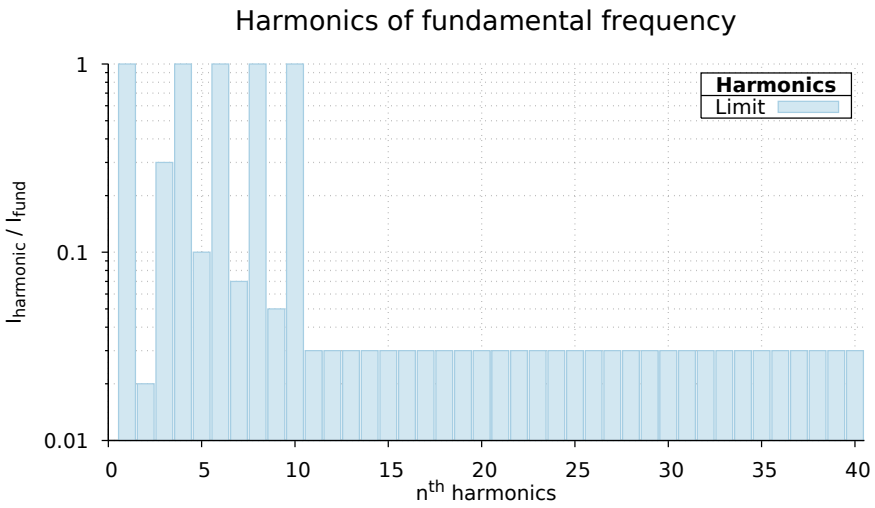


Figure 13: Legal limits of harmonic power consumption relatively to the fundamental frequency[7].

3.7 Lifetime

LED street lamp manufacturers typically guarantee operation for five to ten years. LED street lamps have an utilization time of 20 to 30 years. An average street luminare operates 4'000 hours per year, resulting in a required lifetime of 40'000 hours, when a service life of ten years should be achieved. For a highly reliable power supply, 120'000 hours of operation should be achievable. Details of the lifetime are discussed in section 6.

3.8 Flicker of LED Luminare

Flicker is defined as the rapid and visible change in the luminous flux. The flicker of LED luminaries can cause stroboscopic effects. A moving object can then be seen as separated images. Therefore, the ideal LED driver does change the LED current instantly. Several methods for measuring flicker are known. Only two methods for assessing the flicker are discussed in this dissertation: A simple method, based on the maximal change of flux, not considering flicker frequency. A second method, the compact flicker degree (CFD), additionally considers the flicker frequency.

3.8.1 FluxDelta

LED luminaires should have a minimal flicker. The flicker can be calculated according to the following formula [29, 30].

$$F_p = \frac{\Phi_{max} - \Phi_{\min}}{\Phi_{max} + \Phi_{\min}} \tag{3.1}$$

To achieve zero flicker, the minimal and maximal LED current must be equal. As previously discussed, the flicker calculation formula (3.1) does not include the frequency of the flicker. However, the eye is relatively sensitive to flicker below 100 Hz, less above it.

3.8.2 Flicker based on CFD

A more detailed algorithm for assessing the flicker is the compact flicker degree (CFD). The CFD has been developed by Peter Erwin [31] to distinguish between the different frequencies that are differently observed by the eyes. Obviously, a 30 Hz flicker is more disturbing than a 1 kHz flicker of the same amplitude.

The CFD transforms the signal from the time domain using Laplace to the frequency domain. Then, the grading function g(x) is multiplied with the FFT amplitude. In the time domain this can be expressed as a convolution. The grading function itself is a sectional defined polynomial type function.

From Figure 14 it can be observed that humans are most susceptible to flicker in the range of 5 Hz to 30 Hz. Higher frequency flicker is rated far less severe. However, the observer still can notice it and it may be disturbing to him.

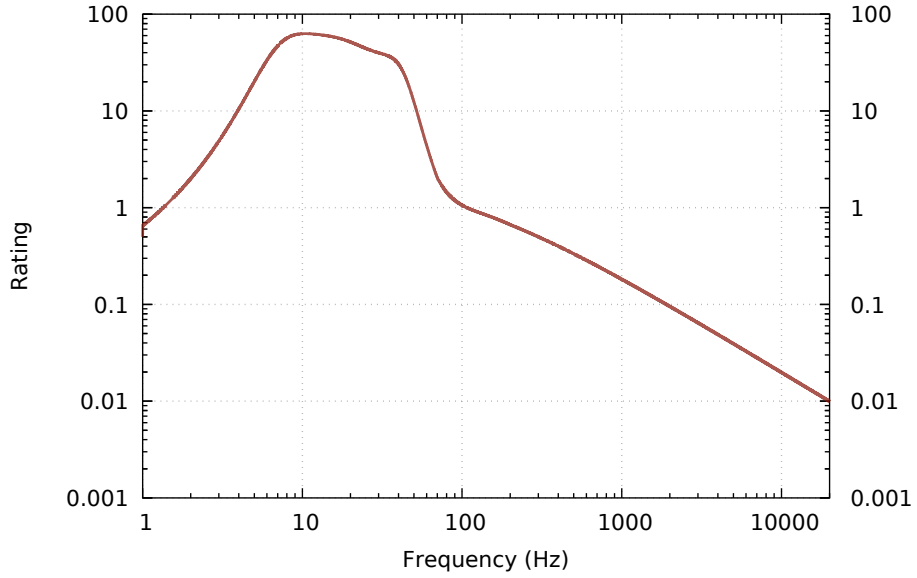


Figure 14: Weighting factor of the CFD

4 Overview Driver Topologies

This section covers common LED driver technologies. The section starts with simple circuits. Each time a circuits drawback is fixed, it is improved by adding additional components. The new circuits operation principle will then be discussed and characteristic equations are derived. Last, their features and drawbacks will be discussed. The optimal solution will be chosen for the subsequent analysis and the LED driver design process.

4.1 Categories

Based on the definition in section 3.1, LED drivers supply the LED engine with the required current of correct shape, typically DC. Every electronic device, capable of lighting LEDs can be considered as an LED driver. Wide variances of LED drivers can be observed, however, two major categories can be observed:

1. Low voltage LED driver are typically sub 100 V converters. An overview of common topologies can be seen in Table 4a. These topologies can be subdivided in linear and switching topologies.
2. Above 100 V converters are considered as high voltage converters and are depicted in Table 4b.

The complexity of switching LED drivers can be measured by the number of stages. A transistor half bridge or a single transistor combined with a diode in one node characterizes a stage.

Low voltage as well as high voltage topologies may or may not accept AC input current. In the considered application range, only AC drivers are considered to accept high input voltages. Low voltage AC converters are not discussed, as they are not typical for lighting applications. Simple high voltage AC LED drivers use a standard full-bridge rectifier, more advanced topologies make use of the totem-pole topology.

4.2 Low voltage linear DC/DC LED driver

Low voltage DC/DC converters are, in general terms, less complex than high voltage LED drivers. As its input voltage is typically safety extra low voltage, no galvanic isolation is required, as it adds no additional safety benefit. The power is typically supplied by a battery. Also the SELV is often generated by a previous high voltage power supply from the AC grid.

topology	current control	operation	stages	section
series resistors	open-loop	linear	0	4.2.1
linear regulator	closed-loop	linear	1	4.2.2
step-up regulator	closed-loop	switching	1	4.4.2
step-down regulator	closed-loop	switching	1	4.4.1

(a) Overview of the typical low voltage LED driver topologies.

topology	current control	operation	pri/sec isolation	PFC	stages
capacitive voltage divider	open-loop	linear	no	no	n/a
step-up regulator	closed-loop	linear	no	no	1
step-down regulator	closed-loop	switching	no	no	1
step-down regulator+PFC	closed-loop	switching	no	yes	2
flyback	closed-loop	switching	yes	no	1
flyback+PFC	closed-loop	switching	yes	yes	2
SRC/LLC	closed-loop	switching	yes	no	1
SRC/LLC+PFC	closed-loop	switching	yes	yes	2
Single Stage PFC/SRC	closed-loop	switching	yes	yes	1

(b) Overview of the common high voltage LED driver topologies.

Table 4: Overview of LED driver topologies for low voltage and high voltage applications

4.2.1 Series Resistor

The straight forward method to drive LEDs is to use a series resistor. It limits the maximum current flowing through the LED. A typical schematic is depicted in Figure 15. This circuit is typically used for LEDs intended for indication applications.

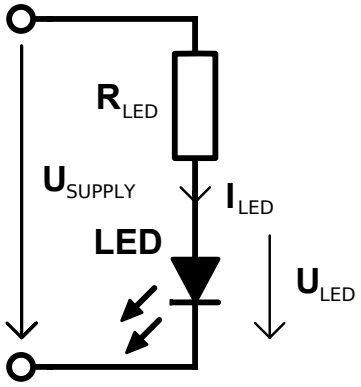


Figure 15: The simplest implementation of a LED driver is to use a series resistor.

The LED series resistor can be calculated using Ohms law and Kirchhoff voltage law.

$$R_{LED} = \frac{U_{\mathrm{SUPPLY}} - U_{\mathrm{LED}}}{I_{\mathrm{LED}}} \tag{4.1}$$

The characteristic curve of a LED driven by a series resistor and constant voltage is shown in Figure 16. The curve is based on a spice simulation with the LED 'NSCW100' and a series resistor $R_{\mathrm{LED}} = 100\,\Omega$. It can be seen that if a supply voltage U_{SUPPLY} larger than the led forward voltage is used, the current rises approximately linear. The slope is limited by the series resistor and the internal LED series resistor. As the internal series resistor typically has a small value, it can be ignored for practical calculations.

For reference, the same LED is plotted without series resistor in Figure 17. It can be observed that without the series resistor, the current slope is significantly steeper.

According to (4.1) and previous plotting, the series resistor LED driver is sensitive to supply voltage variations. The sensitivity of current can be approximated, under the assumption that the LED has no internal series resistor, to:

$$\frac{d}{dU_{\mathrm{SUPPLY}}} I_{LED} = \frac{1}{R_{\mathrm{LED}}} \tag{4.2}$$

According to (4.2), the supply voltage sensitivity reduces, when a higher resistor is chosen. However, the higher the resistor is chosen, the more power is dissipated in the resistor, compromising driver efficiency.

The power dissipated in a resistor can be calculated by the following formula:

$$P_{\mathrm{R}} = R_{\mathrm{LED}} I_{\mathrm{LED}}^2 \tag{4.3}$$

In order to maintain efficiency and safe operation, the supply voltage has to be chosen low while being accurately controlled. If efficiency may be compromised, the supply voltage can be increased so that the resistance can be increased too. A sufficient safety margin to the maximum LED forward current should be provided, if accurate voltage control cannot be guaranteed.

4.2.2 Linear Constant Current Source

To overcome the supply voltage sensitivity of the series resistor, a constant current source could be used, as shown in Figure 18. Various implementations of constant current sources are possible. A precise low cost option of an LED driver is the use of an operational amplifier with a downstream mosfet as shown in Figure 19. The voltage difference between the supply voltage and the LED is dissipated in the mosfet M_1 and the sense resistor R_{S}.

The operational amplifier LED driver, shown in Figure 19 measures continuously the LED current using the sense-resistor R_S. The difference between both voltages, U_{Iset} and U_{Rs} is amplified first by the operational amplifier. Its gain is typically in the range of 60 dB to 120 dB. The operational amplifier

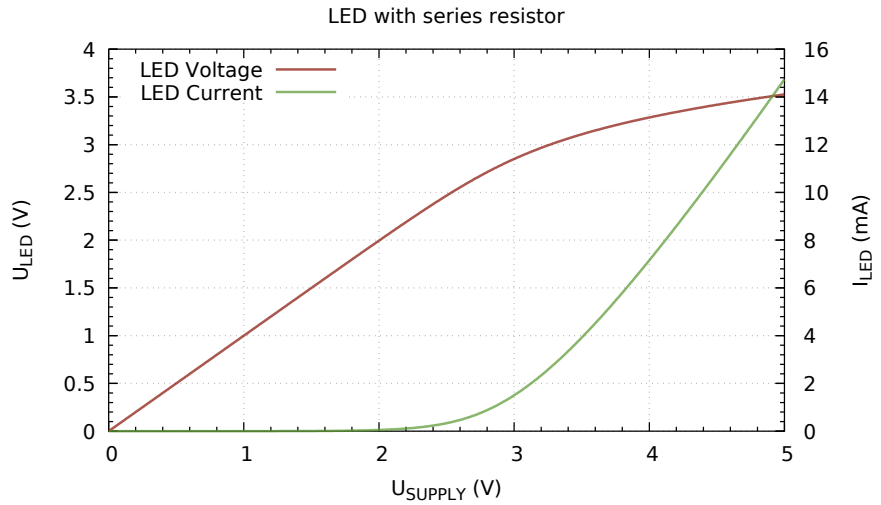


Figure 16: Characteristic curve of a LED driven by a series resistor. A sweep of the DC voltage shows that the current increases approximately linear when the supply voltage is lager than the typical LED forward voltage. This example shows a spice simulation, of the LED 'NSCW100' and a series resistor $R_{\mathrm{LED}} = 100\,\Omega$.

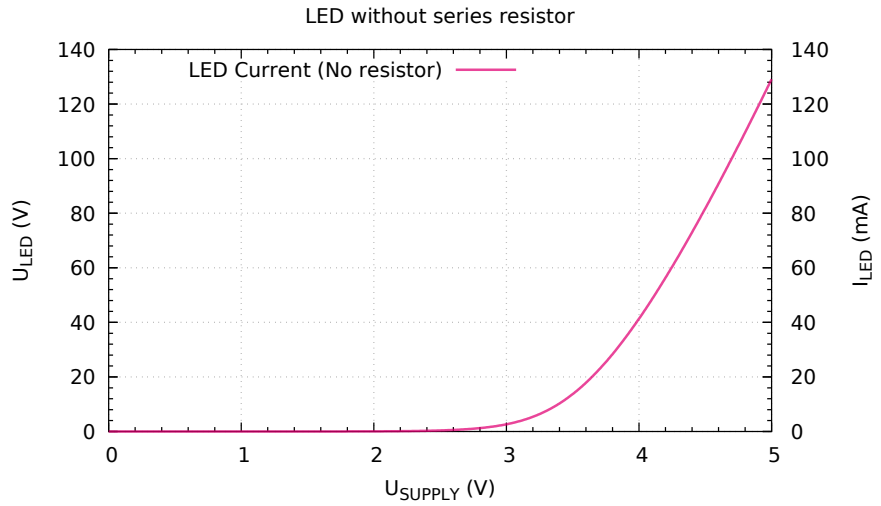


Figure 17: The LED current of the LED 'NSCW100' without series resistor is depicted for reference. Clearly, it can be observed that the LED output current rises exponentially at low voltage differentials.

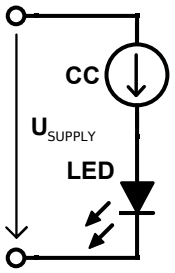


Figure 18: A constant current LED driver ensures a supply voltage invariant LED drive current.

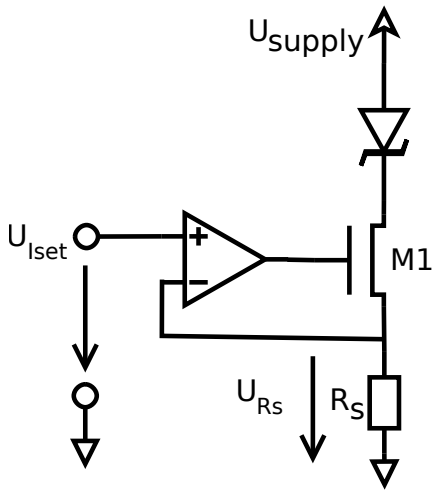


Figure 19: Simplified LED driver implemented using an operational amplifier, mosfet and sense resistor.

controls the gate of mosfet M_1. The mosfet adds another amplification stage. Hence, to maintain stability the high frequency gain of the constant-current circuit must be reduced. This reduction is implemented using a second-order low pass filter as shown in Figure 20, consisting out of R_f and C_f.

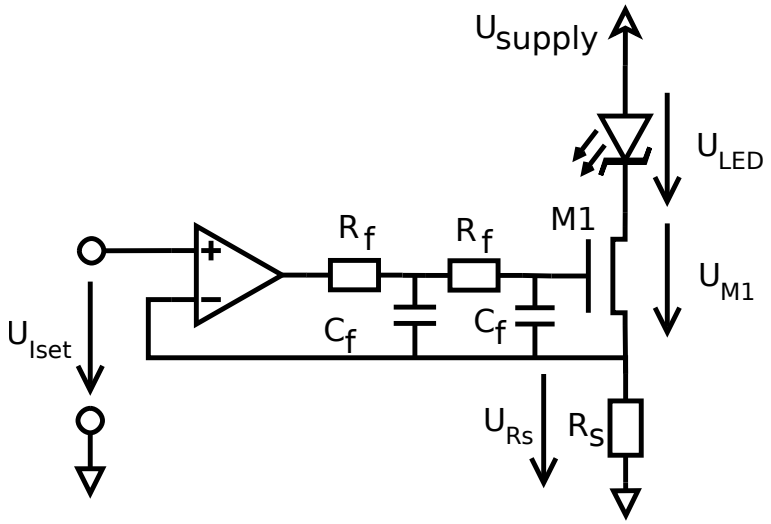


Figure 20: The constant current LED uses an additional low pass filter, to maintain control loop stability.

Simplified loss model: When neglecting the operational amplifiers supply current, the efficiency can be calculated using the following formula:

$$\eta = \frac{U_\mathrm{LED}}{U_\mathrm{supply}} \tag{4.4}$$

As it is can be seen in (4.4), when the LED voltage and supply voltage are close, high efficiencies

can be achieved. However, when a high supply voltage compared to the LEDs voltage is present, the efficiency drastically decreases.

Sophisticated loss model: A more sophisticated loss model is based on a detailed loss analysis. A detailed loss analysis can be done by summing up all losses (P_{sys}), using the following equations.

$$\eta = 1 - \frac{P_{\mathrm{sys}}}{P_{\mathrm{sys}} + P_{\mathrm{LED}}} \tag{4.5}$$

$$P_{\mathrm{sys}} = \sum P_{component} = P_{\mathrm{meas}} + P_{\mathrm{equi}} + P_{\mathrm{opamp}} \tag{4.6}$$

The measurement losses are dissipated in R_{S}. Hence, their losses can be calculated by the following formula:

$$P_{\mathrm{meas}} = R_{\mathrm{S}} I_{\mathrm{LED}}^2 \tag{4.7}$$

The voltage difference between the supply voltage and the LEDs are dissipated in M_1, excluding the sensing resistor losses. These losses are named the equalization losses. The power dissipated at the mosfet can be calculated using the voltage drop U_{M1} over the mosfet M_1:

$$P_{\mathrm{equi}} = U_{\mathrm{M1}} I_{\mathrm{LED}} \tag{4.8}$$

The operational amplifiers power consumption can be calculated based on the supply voltage and the operation amplifiers current consumption.

$$P_{\mathrm{opamp}} = U_{\mathrm{supply}} I_{\mathrm{opamp}} \tag{4.9}$$

Conclusion The linear LED drivers typically can be implemented using basic components. Their application is straight forward. Typically those circuits have little quiescent losses and can be highly efficient when little voltage at the mosfet has to be dissipated. However, their efficiency drops when the LED forward voltage differs significant from the supply voltage.

4.3 Basic Terms of switching converters

Before electrically more efficient switching topologies are discussed, basic terms of switching converters are explained.

4.3.1 Switch-Node

The most important node for the switching of a power converter is the so called switchnode, abbreviated as "SWN". For the Series LC Converter it is the center point of the half bridge, between the two switches S1 and S2. This point has the highest $\frac{d}{dt}U$. Therefore, it is the main emitter of electromagnetic interference. The switchnode is highlighted in Figure 21.

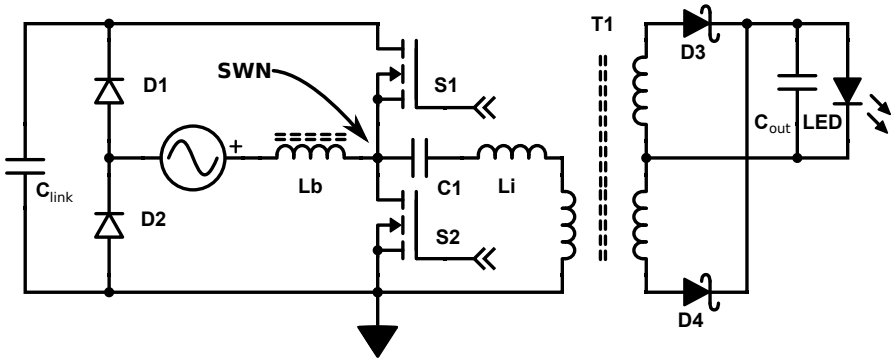


Figure 21: The switchnode (SWN) of the Series LC converter is between the two mosfets S1 and S2.

4.3.2 Online and offline power supplies

Online power supplies are power supplies, where the output is directly connected to the mains. When the LEDs potential is not galvanically isolated from the grid and a conductor is touched by a human, an electric shock may be obtained, despite of a low output voltage. Hence, driver requirements are simplified at the cost of safety.

To increase safety of LED drivers, a galvanic isolation is required: When a galvanic isolation is present, no direct connection between the input and the output node can be observed. Thus, the risk of an electric shock due to a human shorting the output to the ground potential is not present. A galvanic isolation is implemented by adding a transformer to the circuit. The AC connected side is called primary side (PS), while the output connected to the LEDs is called secondary side (SS). The galvanically isolated power supply, is "off-the-line", therefore such power supplies are called offline power supplies.

Primary side and secondary side of a switching power supply are highlighted in Figure 22.

4.3.3 Hardswitching and Softswitching

Online and offline power supplies can be divided into different subcategories: Hard switching power supplies and soft switching power supplies [32, p. 2]. Hard switching voltage topologies actively change the potential of a switching node. Thus, the parasitic drain-source capacitor of the switches is actively

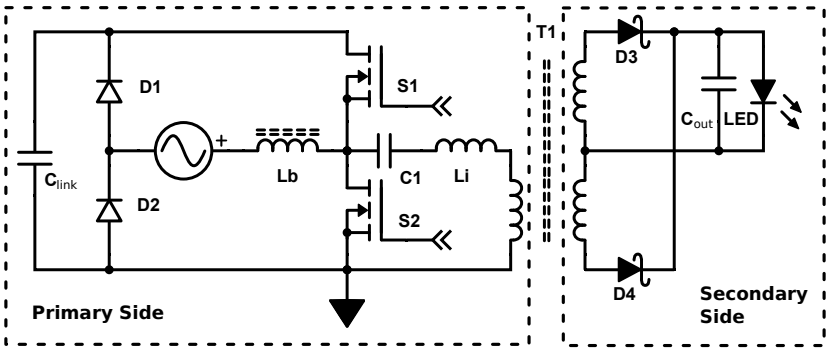


Figure 22: Primary and Secondary Side of a SLC converter.

discharged when it is turned on. In voltage soft switching topologies the capacitor is already discharged, before the switch is turned on. Also, current soft switching may be used, where the current is zero, before the mosfet is turned off.

Hardswitching A hardswitching converter or operation is present, if the switches voltage potential does not have the required potential, before the switch is closed. For example in Figure 21, the SWN potential would be above the ground level, before S2 is closed.

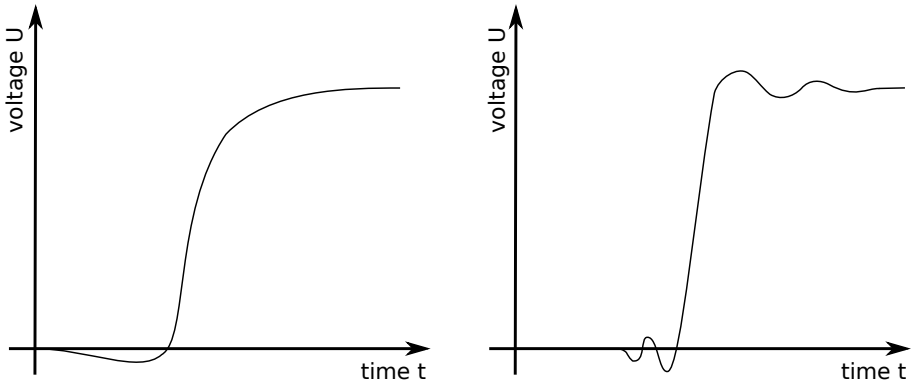
Softswitching The following types of soft-switching can be observed [33]:

- Zero Voltage Switching (ZVS)
- Zero Current Switching (ZCS)
- Zero Current and Voltage Switching (ZCZVS)

For the SLC converter in this work only zero voltage switching is utilized. Under a zero voltage soft-switching behavior it is understood that the corresponding drain-source voltage is ideally zero, before the switch is turned on. An example for a soft waveform is given in Figure 23a.

Quality Factors A basic quality factor for the soft switching is the softness of the switching waveforms. No instant changes of the potential should occur, which is typically indicated by an overshoot.

Another criteria for the switches is the ringing at the switchnode illustrated in Figure 23. The faster the commutation, the higher is the tendency for switch node noise. Therefore, a slow speed is desired. If the slow commutation speed would be forced by the switches, e.g. by using large gate resistor values, the losses at the switches are higher compared to a fast commutation. Further, a slow commutation speed may introduce significant error to the ideal waveform of the converter. This may lead to model inaccuracies.



(a) Soft-switching waveform, which has a soft shape without instant changes.

(b) Hardswitching shows a significant amount of ringing.

Figure 23: Comparison of soft-switching vs hard-switching voltage at the switchnode SWN.

The commutation speed is measured in $\frac{\mathrm{V}}{\mathrm{ns}}$. Typical values for hard switching converters are $10\,\frac{\mathrm{V}}{\mathrm{ns}}$. However, soft-switching converters using $100\,\frac{\mathrm{V}}{\mathrm{ns}}$ have been demonstrated. The commutation speed is measured from 10% to 90% of the amplitude. The following Figure 24 illustrates the commutation speed measurement principle.

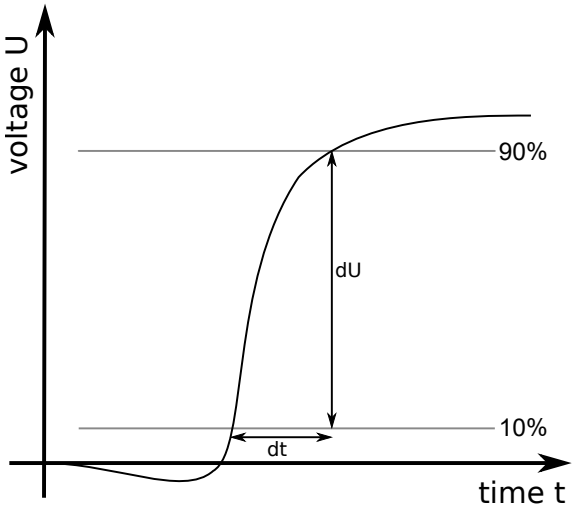


Figure 24: The commutation speed is measured at the switchnode from 10% to 90%.

4.3.4 Resonant / Softswitching disambiguation

A resonant converter is defined as a converter where the resonance has a significant effect. This means that the voltage slope at the capacitor and the current slope in the inductor must have a sinusoidal shape with a significant amplitude.

A DC Link blocking capacitor converter coupled with an inductor is hence not a resonant converter,

as the voltage change at the capacitor is not significant. Nevertheless non-resonant converters can operate in soft-switching mode.

4.3.5 Synchronous rectification

Switching topologies often require diodes for rectifying the previously chopped current. Diodes have a forward voltage drop U_f of 0.5 V to 1.5 V. Hence, its power dissipation can be calculated according to the following formula.

$$P_\mathrm{d} = U_\mathrm{f} I_\mathrm{f} \tag{4.10}$$

Assuming a typical forward voltage of 0.7 V and an output current of ten ampere, a power loss of 7 W occures. This power does not only reduce efficiency, it further must be dissipated at a heatsink, increasing the converters construction size.

To reduce these rectification losses diodes may be replaced by mosfets in forward direction. Mosfets have an intrinsic body diode that may be used. To bridge that intrinsic body diode, a gate voltage must be applied. When a mosfet is conducting, its power losses may be calculated with the mosfet channel resistance $R_\mathrm{DS,on}$ according to the following formula:

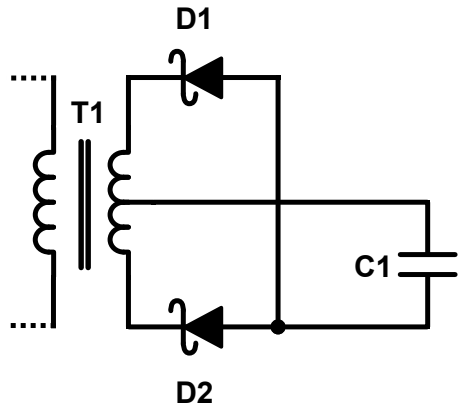
$$P_\mathrm{mos} = R_{DS,on} I_\mathrm{f}^2 \tag{4.11}$$

The typical mosfet channel resistance of a mosfet with a drain source blocking voltage $U_\mathrm{DS} = 150\,\mathrm{V}$ is $R_\mathrm{DS,on} = 10\,m\Omega$. At 10 A, a power loss of 1 Watt is present. Thereby the losses, compared to the diode are lowered by 6 W or 85 %. When decreasing the output current, this difference in power further increases, as the forward current has an exponent of 2 in (4.11). Hence, synchronous rectification will be used in this design. The synchronous rectification is verified in section 14.3.3 on page 162.

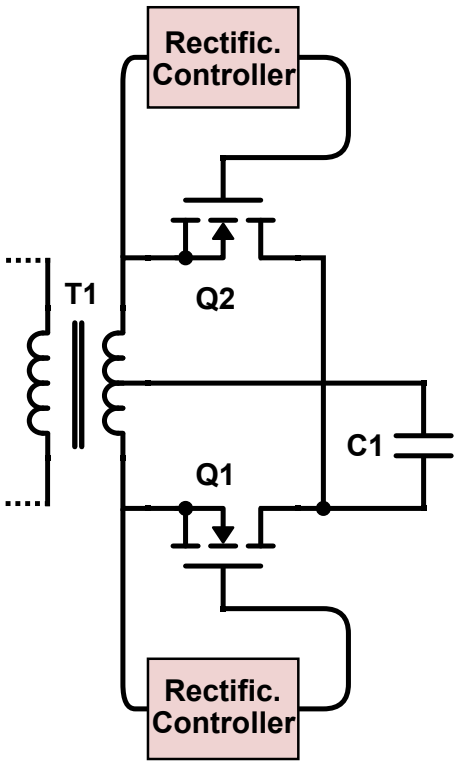
The synchronous controller measures the voltage drop over the mosfet body diode. If a voltage drop in forward direction is measured, the controller turns on the mosfet. Then, the controller can estimate the current flowing over the transistor by measuring the voltage drop over the drain-source resistance. When this voltage falls below a threshold, the synchronous rectifier controller turns off the mosfet.

4.4 Low Voltage Switching Converter

Linear converters produce a significant power loss at high voltage differences between supply voltage and LED forward voltage. Switching converters allow to reduce those losses. Common low voltage switching topologies are discussed in this sub-section.



(a) Diode rectification



(b) Synchronous rectification

Figure 25: Secondary side rectification circuits

4.4.1 Step-down converter

The step-down converter or buck converter is a switching converter that reduces the input voltage and increases the output current. It is used in LED drivers when the supply voltage is higher than the LED forward voltage. One example of a buck converters is shown in Figure 26.

Operational principle A buck converter works in two phases: A charging and a discharging phase. In the charging phase the buck converter uses an inductor to store the energy of the voltage difference between the supply voltage and the voltage of the LED. In the discharging phase the stored energy is released to light up the LEDs.

When the mosfet Q_1 is closed, during $0 \leq t \leq t_{\mathrm{on}}$ the inductor current I_{L1} increases. The typical waveform of a buck converter is shown in Figure 27. The slope of the inductor current can be expressed by the following equation:

$$\frac{d}{dt} I_{\mathrm{L1}} = \frac{U_{\mathrm{in}} - U_{C1}}{L_1} \tag{4.12}$$

By the means of integration the following equation for the on-period can be formulated. The initial current before the turn-on must be known.

$$I_{\mathrm{L1}}(t) = \frac{U_{\mathrm{in}} - U_{C1}}{L_1} t + I_{\mathrm{min}} \tag{4.13}$$

When Q_1 turns off, the current commutates over D_2, as it can be seen in Figure 26. Assuming that the forward voltage of D_2 is zero, the following equation can be formulated:

$$I_{\mathrm{L2}}(t) = -\frac{U_{C1}}{L_1} t + I_{\mathrm{L1}}(t_{\mathrm{on}}) \tag{4.14}$$

The inductor current is continuous. Thus, at t_{on} and t_{off} the inductor currents need to be equal. Hence, the following steady-state equation can be formulated:

$$I_{\mathrm{L1}}(t = t_{\mathrm{on}}) = I_{\mathrm{L2}}(t = 0) \tag{4.15}$$

$$I_{\mathrm{L1}}(t = 0) = I_{\mathrm{L2}}(t = t_{\mathrm{off}}) \tag{4.16}$$

For a simplified calculation, the duty cycle D is defined as follows:

$$D = \frac{t_{\mathrm{on}}}{t_{\mathrm{c}}} \tag{4.17}$$

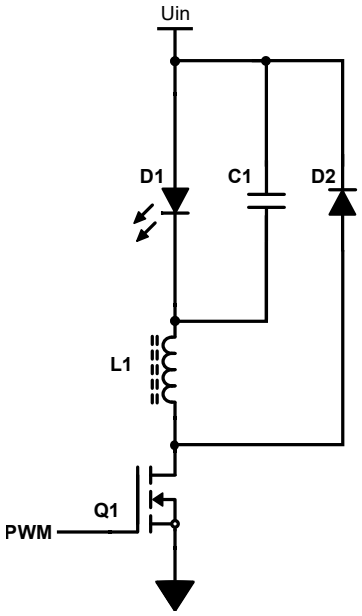


Figure 26: Simplified schematic of an LED buck converter: When the mosfet Q1 is closed, L1 stores the surplus energy. When Q1 turns off and the energy stored in the inductor is used to drive the LED. The current then commutates over the free-wheeling diode D2.

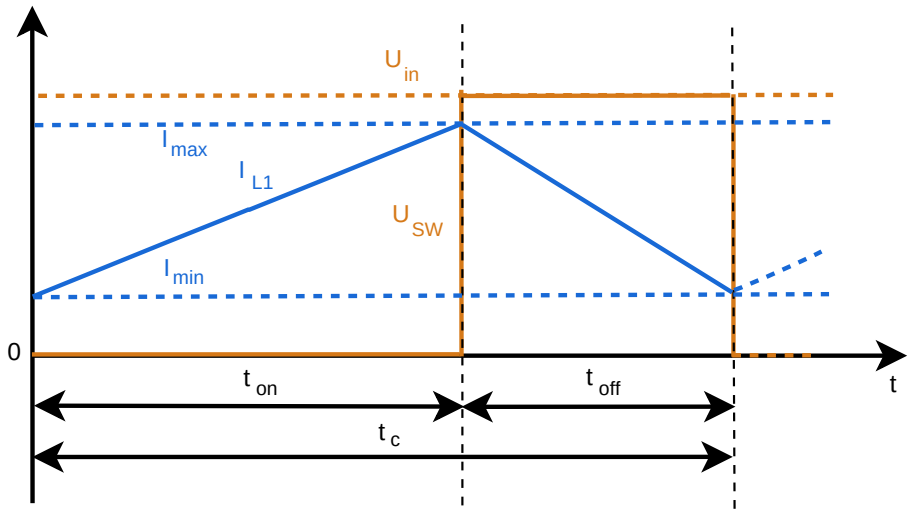


Figure 27: Buck converter waveform showing the inductor current I_{B} and the switch-node voltage U_{SW} over time. The buck converter in this example operates in continuous conduction mode, as $I_{\mathrm{B}}(t) > 0 \,\forall\, t$.

$$t_{\mathrm{on}} + t_{\mathrm{off}} = t_{\mathrm{c}} \tag{4.18}$$

From (4.17) and (4.18) the following equations can be formulated.

$$t_{\mathrm{on}} = D\, t_{\mathrm{c}} \tag{4.19}$$

$$t_{\mathrm{off}} = (1 - D)\ t_{\mathrm{c}} \tag{4.20}$$

A steady state condition is assumed. Hence the initial current and the final current are equal:

$$I_{\mathrm{L1}}(t = 0) = I_{\mathrm{L2}}(t = t_c) \tag{4.21}$$

Based on the previous equations, the steady-state input/output voltage relationship can be formulated.

$$U_{\mathrm{out}} = D\, U_{\mathrm{in}} \tag{4.22}$$

Obviously, the output voltage is always lower than the input voltage. Hence, the maximum number of series-wired LEDs is limited. The capacitor C_1 is used to smooth the current ripple over the LED. By this forward current filtering, flicker can be reduced.

The average current $\overline{I_{\mathrm{avg}}}$ flowing through the converter is the average of I_{min} and I_{max}:

$$\overline{I_{\mathrm{avg}}} = \frac{I_{\mathrm{min}} + I_{\mathrm{max}}}{2} \tag{4.23}$$

Control methods As the LED current in continuous conduction mode depends on the prior switching cycle, a continuous monitoring of the LED current I_{D1} is required. The current sensing is typically implemented by using a shunt resistor, for example R_1 is used in Figure 28 as a shunt resistor.

One stable and resilient control principle, for example used in the integrated LED Driver IC AL8805[34], is the hysteresis mode control. The current is continuously measured by the shunt resistor R_{S}. If the current in Figure 27 is lower than I_{min}, Q_1 is turned on. If the current is higher than I_{max}, Q_1 is turned off. By this approach the PWM signals can be generated with little hardware requirements with an inherent stable control loop.

The simplified electric circuit and the implementation of the previously described control method is depicted in Figure 28.

Summary The buck converter is a well known low voltage LED driver. It features good efficiency and a stable control. This topology is a hard-switching topology, hence especially at high voltages, switching losses might reduce efficiency. Further, hard-switching increases EMC compliance complexity. One limitation is that the maximum number of series LEDs is limited.

4.4.2 Boost converter

When the supply voltage is lower then the LED forward voltage, a boost converter as shown in Figure 29a can be used to increase the voltage. The boost converter is a switching topology, operating in a two or three step process. Assuming no forward voltage drop of the diode, the input voltage U_{in} of a boost converter is always lower or equal than the output voltage U_{out}. The boost converter increases the output voltage and lowers the output current relative to the input current.

The boost converter can operate in two operation modes: continuous or discontinuous. The discontinuous mode is typically used at low load and is discussed in the subsequent PFC section. In this calculation only the continuous mode is considered. The operational waveform for the boost converter operating in continuous conduction mode is shown in Figure 30.

Charging state (Q1 turned on) The inductor is charged by closing Q_1, as it can be seen in Figure 29b. The current passing through the inductor L_1 is rising linearly and the inductor current change can be expressed by the following equation:

$$\frac{d}{dt} I_{\mathrm{L1},on} = \frac{U_{in}}{L_1} \tag{4.24}$$

As the input voltage is held constant by an input capacitor, it can be approximated as a constant voltage. The inductor current can be calculated using integration. As Q_1 is on for the time t_{on}, the following formula can be denoted:

$$\int_{t=0}^{t=t_{on}} \frac{d}{dt} I_{\mathrm{L1},on} dt = I_{\mathrm{L1,on}} = \frac{U_{in}}{L_1} t_{\mathrm{on}} + I_{\mathrm{L1}}(t=0) \tag{4.25}$$

For a simplified calculation, the duty cycle D is defined. The duty-cycle describes thereby the fraction of the switching period t_{c}, the switch is turned on:

$$D = \frac{t_{\mathrm{on}}}{t_{\mathrm{c}}} \tag{4.26}$$

The duty cycle may range from zero to one. However, referring to Figure 28, a duty cycle of 100% is not possible, as it would result in a short circuit. Mathematically, the duty cycle D domain of definition

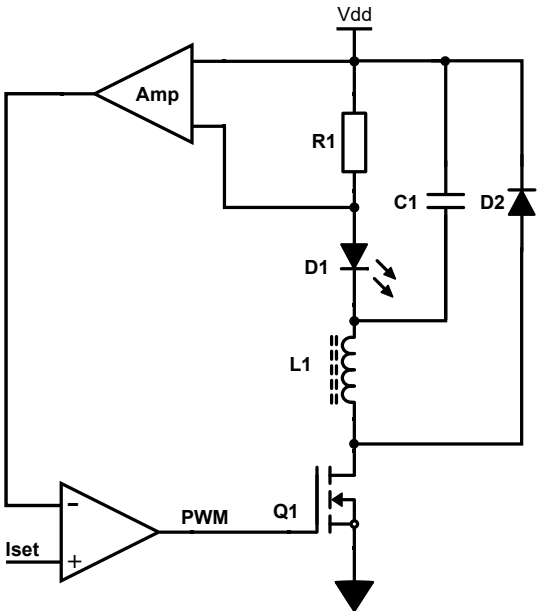
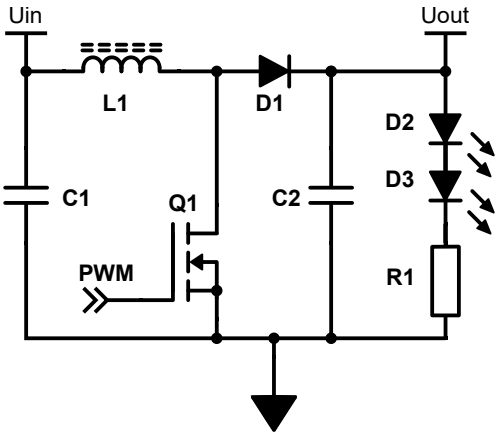
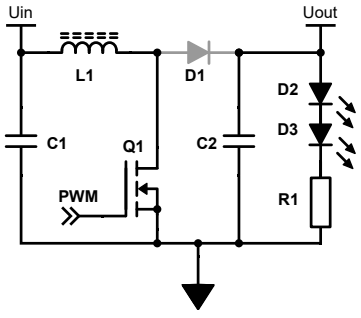


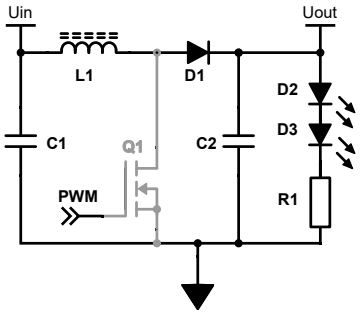
Figure 28: Hysteresis mode controller implementation: The LED current is measured by means of the sense resistor R1. The current sense voltage is amplified and passed to the hysteresis comparator that switches on when the minimum threshold is reached and switches off when the maximum threshold is reached.



(a) Topology



(b) Charging state



(c) The inductor is discharged

Figure 29: Simplified LED boost converter, showing the the two phase operation principle of a boost converter. A boost converter increases the output voltage.

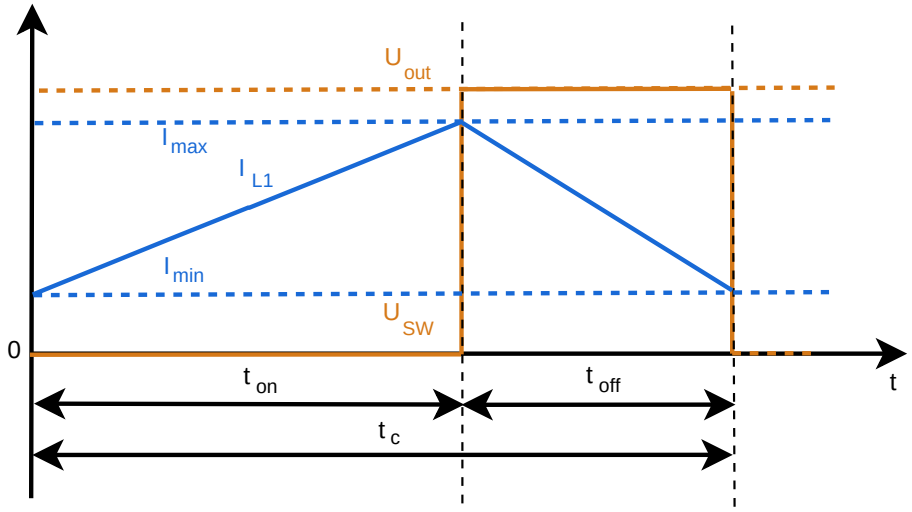


Figure 30: The Boost converter is operating in continuous mode and it is operating waveform is shown. The inductor current I_{B} rises when the switch is closed to GND, thus $U_{\mathrm{SW}} = 0$. When the switch opens, the inductor releases its energy to the output, supplying it with power.

can be expressed as follows:

$$D \in [0, 1) \tag{4.27}$$

Discharging state (Q1 turned off) When Q1 is switched off, the inductor current flows over C_1, D_1 and C_2 as it can be seen in Figure 29c. Therefore, the inductor current during the off-state can be formulated accordingly:

$$\frac{d}{dt} I_{\mathrm{L1},off} = \frac{U_{in} - U_{\mathrm{out}}}{L_1} \tag{4.28}$$

As the input and output voltages are both quasi-constant voltages, the inductor current at the end of t_{off} can be expressed by the following equation:

$$I_{\mathrm{L1,off}}(t = t_{\mathrm{off}}) = \frac{U_{in} - U_{\mathrm{out}}}{L_1} t + I_{\mathrm{L1,on}}(t_{on}) \tag{4.29}$$

The assumption is made that the steady-state condition is reached and that the boost converter operates in continuous conduction mode. The steady state condition is defined that the waveforms of two consecutive switching cycles match. The discontinuous operation is also possible and is discussed in section 7.3.

Based on Figure 30, the following equation can be formulated:

$$t_{\mathrm{c}} = t_{\mathrm{on}} + t_{\mathrm{off}} \tag{4.30}$$

For the off-time the duty cycle definition of (4.26) can also be expressed as:

$$t_{\mathrm{off}} = (1 - D)\, t_{\mathrm{c}} \tag{4.31}$$

Voltage to Voltage converter From equations (4.25), (4.29) and the duty cycle definition (4.26) and (4.31) a steady-state voltage to voltage converter formula can be derived:

$$\frac{U_{\mathrm{in}}}{U_{\mathrm{out}}} = 1 - D \tag{4.32}$$

From (4.32) it can be seen that the output voltage can be as low as the input voltage. It can also be observed that a duty cycle $D = 1$ is not possible, if an input voltage is present.

LED current sensing and control To sense the current flowing through the LED, a resistor R_1 is used as a shunt, referring to Figure 29. The measured current is used for control. The PWM waveform typically is generated by a fixed frequency PWM with variable duty cycle. The duty cycle typically is determined by a PID controller.

Summary The boost converter is a well known topology for increasing the output voltage. The efficiency of the boost converter highly depends on the increase in voltage. For the most efficient design, the output voltage should only be increased slightly. As the boost converter ratio increases, it efficiency typically decreases. Despite the number of LEDs is not limited theoretically, efficiency wise the maximal number of LEDs is limited.

4.5 High Voltage Topologies without Galvanic Isolation

High voltage power supplies typically are used in grid connected LED luminaires. The metal case of non-galvanic isolated LED drivers should be directly connected to ground for safety reasons.

4.5.1 Capacitive Power Supply

A low cost option for driving LED luminaries is the use of a capacitive power supply. A typical circuit diagram is shown in Figure 31.

Operation principle In Figure 31, the AC power line voltage is reduced by the reactance of C_1. R_2 is used for to limit the circuits inrush current. The AC input current is rectified by the diode bridge DB_1 and the double mains frequency ripple is smoothed by C_2. D_1 is used to protect C_2 against over

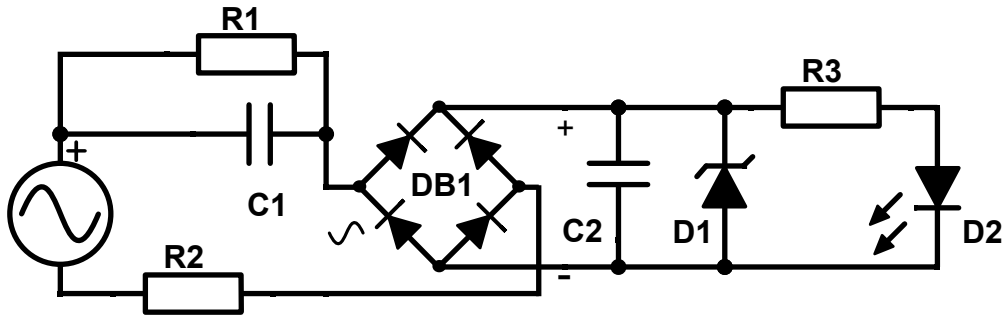


Figure 31: Capacitive voltage dropper for driving LEDs. The voltage is lowered by the capacitor C1 and R2.

voltages. R_3 limits the current flowing through the LED D_2. R_1 is required to discharge the capacitor C_1, when the LED luminary is removed from the socket.

Lifetime In this solution the C_1 capacitor faces surges of the AC grid. As self-healing class X safety capacitors are used, they will not be destroyed. However, an overvoltage event reduces its capacitance. Thus, the reactance increases, leading to lower LED supply current. Therefore, series capacitor power supplies tend to reduce the LED drive current over time.

Further, as DC link capacitor C_2 in most cases an electrolytic capacitor is used. As LED PCBs tend to get hot, the electrolytic capacitor aging is accelerated and it fails subsequently. The fundamentals of lifetime calculus are discussed in section 6.

Summary As a capacitor is used for voltage reduction, this solution requires a significant amount of reactive power. Further, the LED current cannot be controlled actively by using semiconductor devices. Thus, a changing grid frequency or grid voltage may change the LED current. When the LEDs forward voltage decreases, e.g. one LED of the string fails to short circuit, the LED current will increase.

If more output current is required a physically larger capacitor must be used. Typically this limits the feasible power density.

4.5.2 Buck Converter

The AC buck converter shown in Figure 32 is similar to the DC buck converter shown in Figure 28 on page 56. The circuit is extended with an AC rectifier and a larger DC link capacitor C_2. Except from that, the operation and control principle is equal to the conventional buck converter.

Compared to the capacitive power supply, the LED current is directly controlled. However, its construction is more complex.

This circuit does not require a high value series-resistor for LED ripple current rejection. Therefore,

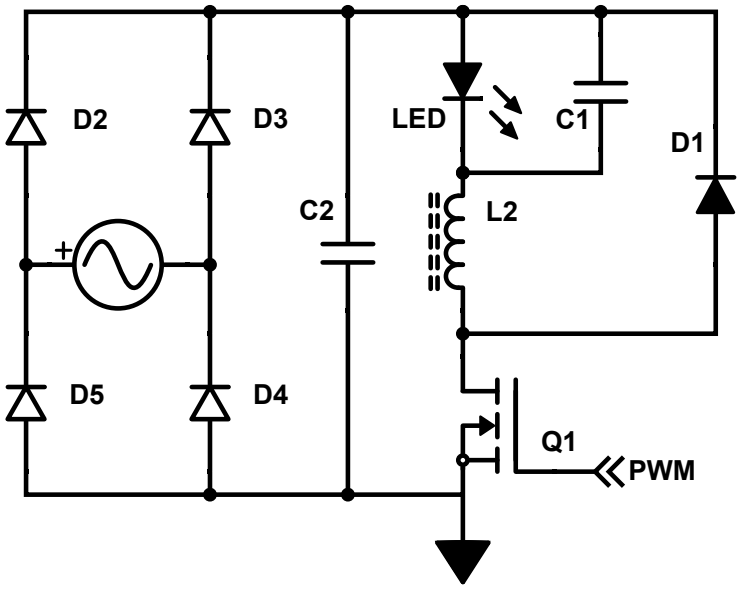


Figure 32: An AC buck converter is a classic LED driver topology. The upstream full bridge rectifier is connected to the AC grid.

the overall converter efficiency typically is higher. One drawback of this solution is the still low power factor of typically 0.55 due to reactive power that is caused by the AC/DC bridge rectifier: Power from the grid is only taken at peak values, as it can be seen in Figure 33. It is known as displacement power. To obtain an unity power factor, an additional power factor correction circuit must be added upstream. This will be discussed in the subsequent subsection.

4.5.3 Boost Converter

Instead of a buck converter, a boost converter with the previous full-bridge rectifier could be used as well. As the boost converter always increases the output voltage, referring to section 4.4.2, this leads to a very high output voltage. Assuming a 250V grid, the minimal feasible output voltage would be 353V. Not only this requires a significant number of series LEDs, an additional risk of electric shock is present at the LEDs. For that reason, a voltage increasing topology is rarely used in grid connected LED lighting.

4.5.4 PFC/Buck

To achieve a power factor close to one, a power factor correction (PFC) is added upfront. The LED driver now consists out of two stages.

The PFC converter shown in Figure 34 starts by rectifying the AC using the full bridge (D_2-D_5) which is connected to a boost converter, consisting out of L_3, Q_2 and D_6. The converter operates in a two stage process: First, transistor Q_2 is closed, the inductor current of L_3, I_{L3} increases. Next, Q_2

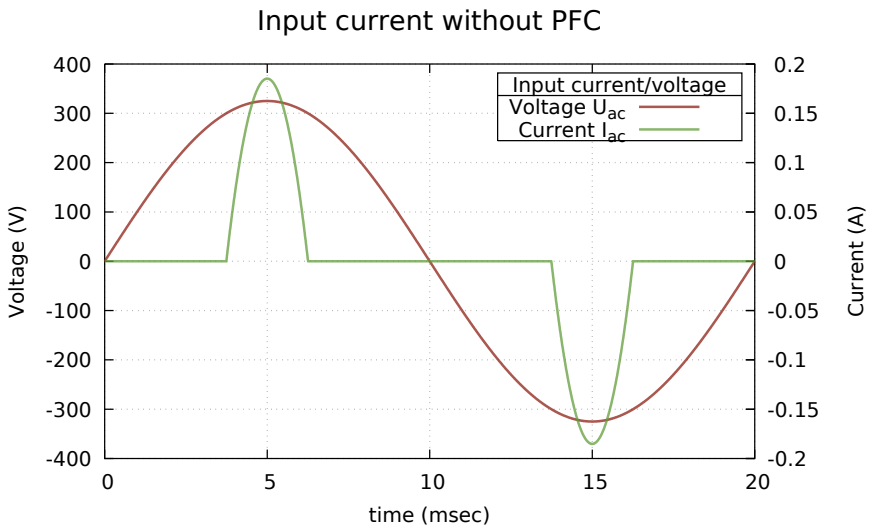


Figure 33: Without an PFC, AC current is only taken from the grid at peak values. Therefore, a relatively high current flows when the grid voltage peaks, otherwise no current is taken from the grid. This introduces reactive power, resulting in a low power factor. The actual current shape may differ from load to load. This Figure as only an illustration of a possible grid current caused by a full bridge rectifier.

is opened. The energy that is stored now in L_3, is transferred to the DC link capacitor C_2.

The buck converter, shown on the right hand side, operates in the same manner as discussed in section 4.4.1.

An ideal PFC appears to the grid as an equivalent resistor. It ensures that the voltage and the current have non significant phase lag or lead. The control algorithm generates a PWM signal in such manner that the circuit appears to the grid as an ideal resistor. Therefore, the input current, as shown in Figure 35, is directly proportional to U_{ac}.

4.6 Topologies with galvanic isolation

This section discusses LED driver topologies with galvanic isolation. Active power factor correction topologies, hard- and soft-switching topologies are discussed.

4.6.1 PFC/Flyback

A PFC/Flyback has a PFC stage at the input, similar to the PFC buck converter. The PFC feeds the DC link capacitor C_2. The flyback converter (mainly Q_1, T_1) is used for galvanic isolation. Galvanic isolation is required for enhanced safety of the converter.

For example, if the secondary side output is touched without galvanic isolation, an electric hazard is present, despite only low voltage is used. The LED output may have a significant voltage potential to the ground level. With galvanic isolation, no direct connection between the secondary side and

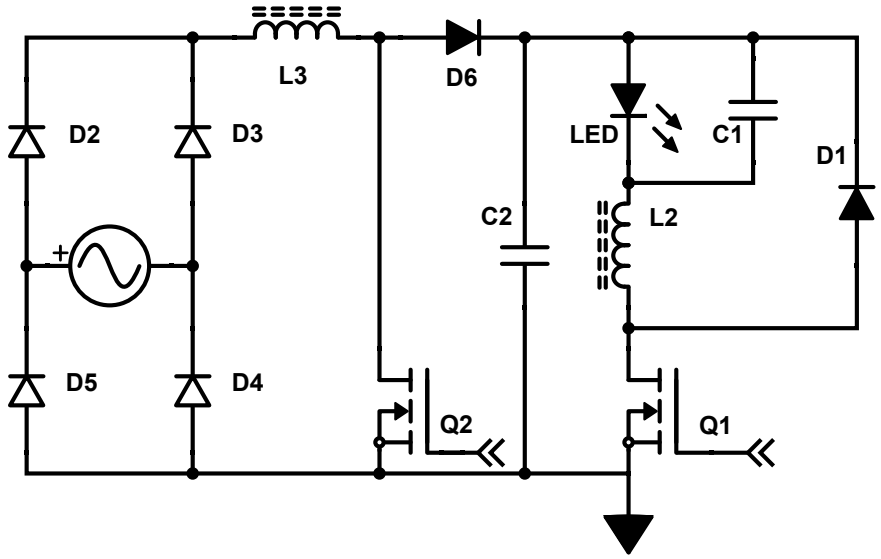


Figure 34: The PFC generates a sinusoidal input current waveform to obtain a power factor close to one. The PFC is an additional circuit, which is placed upstream to the buck converter.

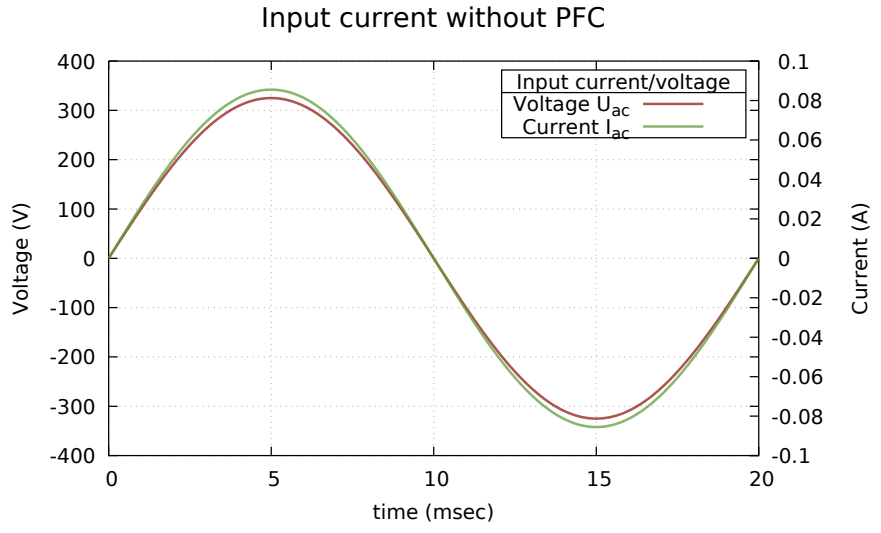


Figure 35: The ideal input current of an ideal PFC converter has a perfectly sinusoidal shape. No phase lag or lead of the current can be observed.

the human is possible. This safety measure increases electric safety significantly. Thus it is highly recommended for all LED power supplies, where the outputs may be touched by humans.

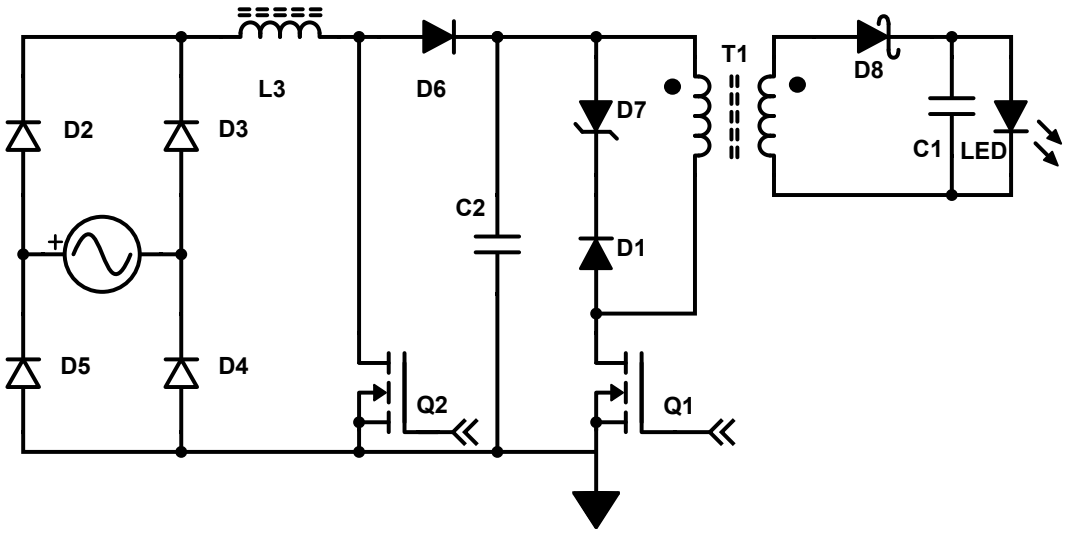


Figure 36: PFC/Flyback topology consists out of a standard PFC with a downstream flyback converter.

Operation principle The switch Q_1 is closed by applying a PWM signal, the transformers inductor, which is included in T_1, is charged. As D_8 faces a negative voltage, it is blocking. The energy is stored inside the transformers magnetizing inductance and primary side stray inductance. The current rises linearly until it crosses a specified threshold. Q_1 is then turned off and the energy stored in the stray inductance is dissipated at the zener diode D_7. The energy stored in the magnetizing-inductance is transferred to C_1 - which then smooths the output current for the LEDs.

The transformer's magnetizing inductor can store positive and negative currents. However, the flyback topology uses only positive currents. This is why only half of the cores potential is used. Therefore, the required core size will be larger.

Control One possible control method is the so called peak current mode. Every period, t_c, the switching cycle is started, until the turnoff current flowing over Q_1 is crossed. The energy stored in the main inductance of the transformer can be calculated using the following equation:

$$E = \frac{L_\mathrm{main} I_\mathrm{T1}^2}{2} \tag{4.33}$$

As this procedure is repeated every switching period t_c, the power transferred to the secondary side can be calculated to:

$$P_\mathrm{sec} = \frac{L_\mathrm{main} I_\mathrm{T1}^2}{2 t_\mathrm{c}} \tag{4.34}$$

From (4.34) it can be observed that the power transfer is set by the square of the peak inductor current and the switching frequency. This means, the output power can be set and controlled by those two parameters.

Requirements for switches The switch utilized in a flyback converter must block the a significant reverse voltage when the energy is transferred from the primary side by T_1 to the secondary side: The switch must withstand the DC link voltage, the reflected voltage and the voltage induced by stray inductance. This means that typically a fairly high blocking voltage is required. If the blocking voltage of a switch is doubled, the typical on resistance increases over-proportionally. Thus, switching and conduction losses are high in this converter topology.

Loss sources In this converter different loss sources are present. Some are individually discussed. One loss source is the stray or leakage inductance. The loss of the stray inductance can be calculated analog to (4.34):

$$P_{\mathrm{Loss,Leakage}} = \frac{L_{leak} I_{\mathrm{P}}^2}{2t_{\mathrm{c}}} \tag{4.35}$$

The relative stray inductor losses are independent of the transferred current and are exclusively defined by the inductors. This can be shown by the following calculus:

$$p_{\mathrm{Loss,Leakage,rel}} = \frac{P_{\mathrm{Loss,Leakage}}}{P_{\mathrm{sec}}} = \frac{L_{leak}}{L_{\mathrm{main}}} \tag{4.36}$$

The parasitic winding capacitance of the transformer is shorted, when Q1 is turned on. The capacitor losses can be calculated using the following equation:

$$P_{\mathrm{Loss,TCap}} = \frac{C_{\mathrm{T}} U_{\mathrm{C2}}^2}{2t_{\mathrm{c}}} \tag{4.37}$$

This means that the transformer capacitance C_{T} and the capacitor voltage U_{C2} should be chosen minimal to reduce losses.

Another loss source, which is comparatively high at low output voltages, is the losses of the secondary side output diode. The power loss of a diode can be calculated by the simplified equation:

$$P_{\mathrm{Loss,Diode}} = U_{\mathrm{D8}} I_{\mathrm{out}} \tag{4.38}$$

To reduce this type of loss, a low forward voltage schottky diode is used. However, to reduce secondary diode losses, so called secondary synchronous rectifiers are available that replace the diode

by a mosfet. For this a special control IC is required. A significant improvement of efficiency can then be observed.

Typical efficiencies of flyback converters ranges from 70% to 93%. An example of typical efficiencies for a flyback/PFC converter is shown in Figure 37 [8]. It shows the efficiency over the output current at an output voltage of 24 V measured at a low line input voltages V_{I}.

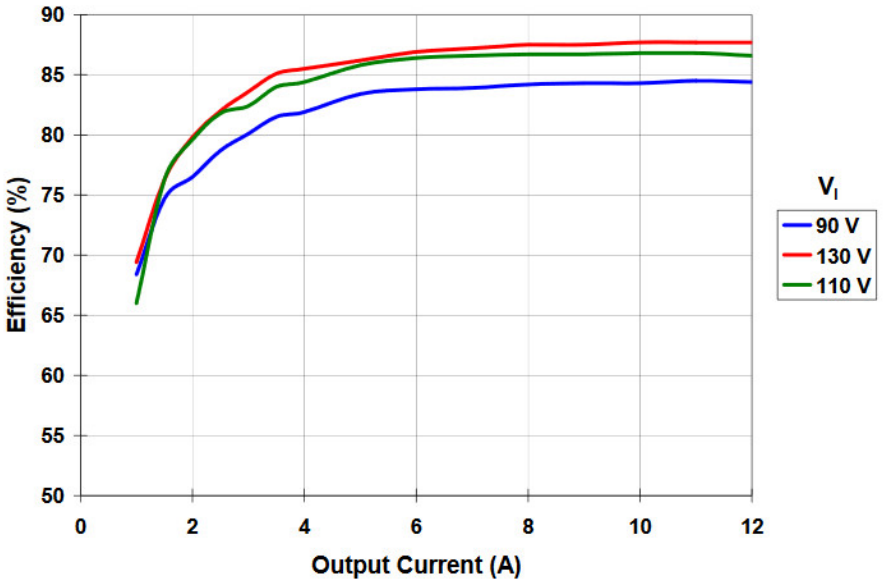


Figure 37: Efficiency of a flyback converter used for LED TVs. The efficiency increases with increasing output power. The higher the input voltage, the higher the efficiency. The measurement is reproduced from the reference design [8].

4.6.2 PFC/SRC

The PFC/SRC converter, shown in Figure 38, has on the AC side a standard full bridge rectifier with a standard boost converter utilized as a PFC. The control signals for Q_2 are generated in such manner that the input current has a sinusoidal shape. The voltage at the DC-Link capacitor has a double mains frequency ripple. Actually, the grid input power has a $sin^2(\omega t)$ shape. It can be reformulated by the use of addition theorems to a sine with the doubled grid frequency and a constant offset. While the consumed power is constant, the DC link capacitor C_2 has to average out the energy difference, between the energy taken from the grid and the energy consumed by the load. Therefore, to provide this energy storing function, the capacitor encounters the double mains grid frequency ripple.

The PFC converter consists of the AC input that is rectified by the diodes D_2-D_5. A subsequent boost converter, consisting out of L_3, Q_2 and D_6 generates a higher DC-Link voltage. Q_3 and Q_4 form a half-bridge and are driven with a symmetric duty cycle of D=0.5. The capacitor C_1 adds an DC offset where the following relationship for a duty cycle of 0.5 holds true. The resonance capacitor C_1

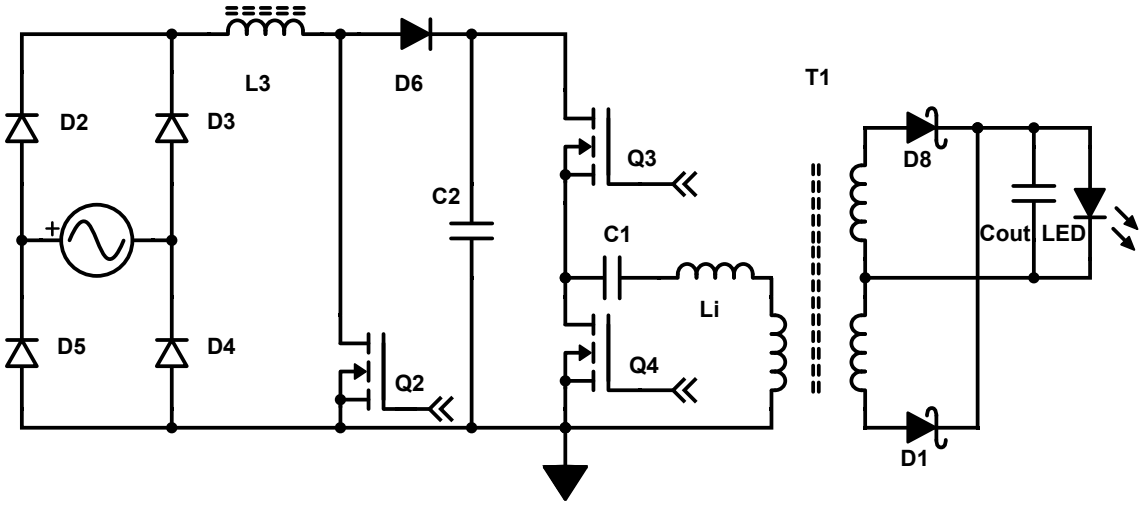


Figure 38: Series resonant converter with a standard boost PFC: Q2 is used to control the input current from the grid, where as Q3/Q4 are driven with a constant duty-cycle of D=0.5 and the frequency is changed.

has an overlaid sinusoidal waveform.

$$U_{\mathrm{C2}} = 2\overline{U_{\mathrm{C1}}} \tag{4.39}$$

4.6.3 Series LC Converter

If the converter is operated far above its resonance frequency, it is not operating in resonant mode. Despite of being the same topology, it then cannot be considered as a series resonant converter. Hence, the converter was renamed to series LC converter (SLCC). Therefore, if the topology shown in Figure 38 is operated at resonance frequency, it is considered a SRC. If it is operated far above the resonant frequency, it is designated SLCC. The operational waveform of an SLC converter is shown in Figure 39.

At the beginning of the SLC converters cycle, Q_3 is closed. First, the current I_{i} is negative with a positive vector. C_1 subtracts half of the DC links supply voltage. When Q_4 is closed, C_1 provides half the DC link voltage as a negative voltage.

By adding the capacitor C_1, the DC voltage offset from the half bridge is removed. Therefore, transformer T_1 works with positive and negative currents, so that the full potential of the magnetic core is utilized.

The secondary side of the converter consists out of a mid-point rectifier, implemented by D_1 and D_8, where the pulsating output current is smoothed by the output capacitor C_{out}. The current is then consumed in the LED, which operates as the load.

The timing sections t_{n}, where $n \in [1, 2, 3, 4]$, are highlighted in Figure 39. In the odd time sections, the output voltage U_{out} has the inverse polarity as the transformer voltage U_{i}, hence the current returns

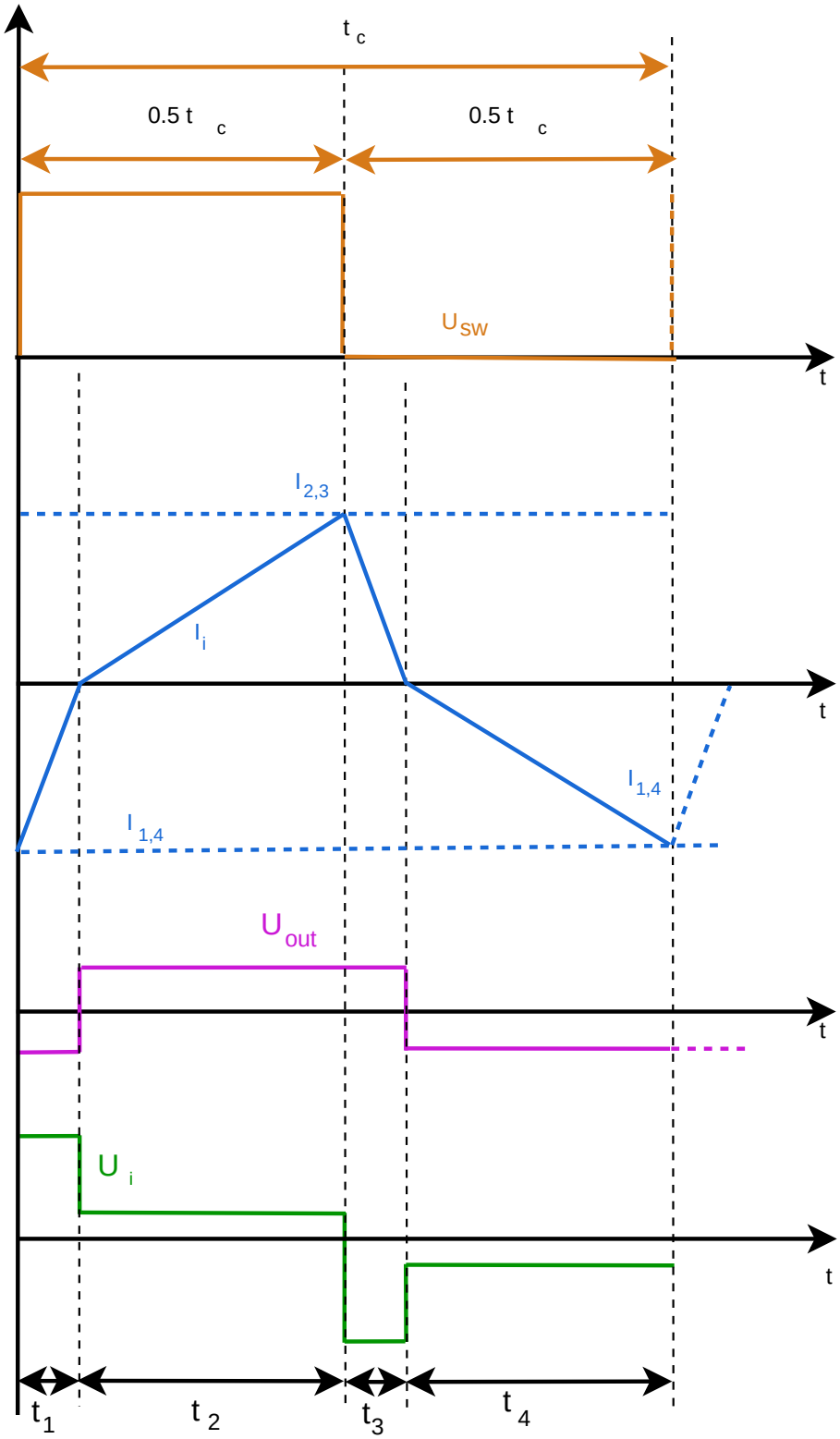


Figure 39: Operational waveforms of the SLC converter operating at a duty cycle of 0.5. The positive and the negative waveform are perfectly symmetric. Therefore, the maximum inductor currents are equal ($I_{1,4} = I_{2,3}$).

fast to zero. In the even time sections, the polarity is equal, thus the absolute current increases slower from zero.

A detailed discussion of this topology and the development of equations can be found in section 7.

Losses As the PFC input stage is identical to previous solutions, the losses will be equal. The series resonant converter and series LC converter thus are superior regarding energy losses, as soft-switching can be used. The energy stored in the previously used flyback transformer stray inductance (Figure 36) is not dissipated in the snubbed network. Instead, the energy stored in L_i of the series LC converter will be used to charge the half bridge parasitic capacitor to the required value, achieving zero voltage switching. Therefore, losses are decreased and efficiency is increased.

Control The SLC converter control will be discussed in section 7.5.3. It is a challenge to reject the double-mains-frequency-ripple directly from the DC link, therefore a secondary side DC/DC converter typically is added to reject this ripple [9]. This dissertation presents a novel control algorithm that operates the SLC converter as a true single stage converter.

4.6.4 Totem Pole PFC/SLC Converter

The losses in a PFC may be reduced by replacing the standard bridge rectification and downstream PFC by a totem pole PFC as shown in Figure 40. The totem pole PFC requires only two diodes. Compared to the bridge rectification, two diode voltage drops may be saved, increasing the PFC converter efficiency.

The totem pole PFC replaces one diode halfbridge by an active halfbridge. The second active halfbridge is driven with PWM signals to operate as a boost converter. By that rectification conduction losses can be reduced.

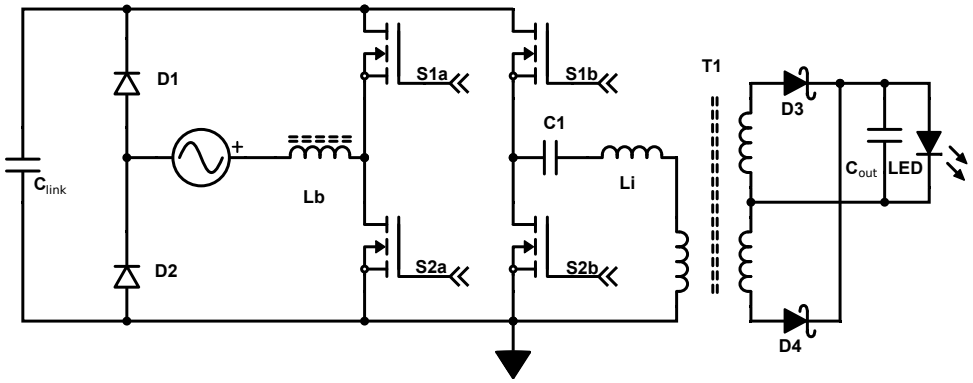


Figure 40: By replacing the bridge rectification by a totem pole PFC topologies, two diode voltage drop may be saved.

4.6.5 Single Stage PFC/SLCC

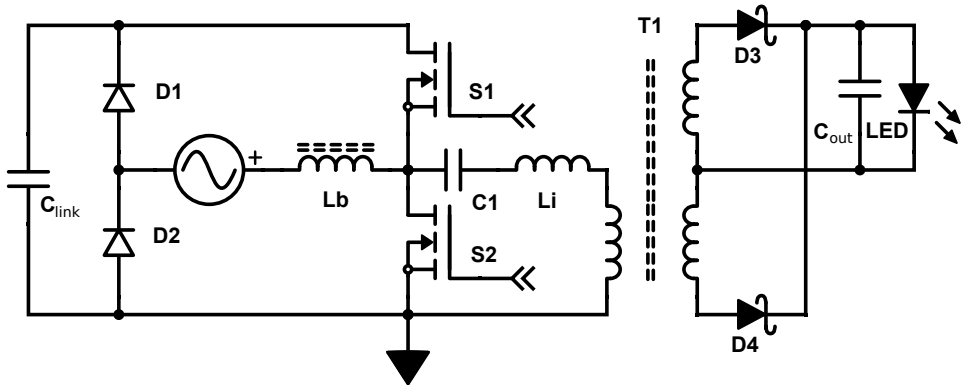


Figure 41: Integrated PFC/SLC converter: The boost stage and the SLCC share the switchnode.

The single stage PFC/SLC converter is shown in Figure 41. The PFC input stage consists out of D_1 and D_2, AC, L_b and the two switches, S_1 and S_2. The energy is then stored in the DC link capacitor, C_{link}.

The SLC converter shares the half bridge mosfets S1/S2 and the DC link capacitor C_{link} with the PFC input stage. Right hand side to the half bridge the DC offset capacitor C_1 is placed. The series inductor L_{i} smooths the transformer current. The secondary side is rectified by a mid-point rectifier, consisting out of D_3 and D_4. C_{out} smooths the output voltage and current ripple flowing over the LEDs.

This topology is required to control the input- and the output current to the LED by means of a single half-bridge. For controlling two set variables, two actuating variables are required. Hence, the control of this topology will be implemented by using the duty cycle D and the switching period t_{c} as control variables. The topology is discussed in detail in the sub-section 7.5.

Losses In the boost converter, the input current has to pass two diodes less than in the conventional PFC/SLC converter. This increases the efficiency of the boost PFC converter. Compared to the totem pole PFC/SLC converter, one half bridge less is required. The SLC converter allows for soft-switching at the switchnode (SWN). Therefore, a high efficiency for this converter topology is expected.

Complexity The PFC/SLC topology has a reduced hardware complexity, as the minimum number of switches is used. However, the analysis and the control of the topology are difficult.

4.7 Topology Selection

There is a vast variety of topologies for different application requirements. The range starts with simple, very low power converters and ranges up to complex, high power converters. The objective of this work is to construct the best possible solution with the minimum number of power components. This can be achieved by using the PFC/SLCC topology. However, the reduced number of components requires a far more complex control. Hence, a standard PWM controller cannot be used. Therefore, a microcontroller is chosen for digital control. This work models and describes the converter topology.

First, the topology is used, then the control system is designed. The control will require several variables to be measured. Based on the control system requirements, the control principle is designed in section 7 starting at page 96.

The major advantage of this technology is the minimal number of components. Further this topology promises a high converter efficiency.

5 Driving multiple LED Strings

This section presents a novel paralleling technique for LEDs that is applied on LED streetlamps: A master high current source can be divided equally with the novel proposed circuit to several constant sources. Thereby LED tolerances can be regulated out and a safe operation is guaranteed.

This section is based on a paper published at PCIM 2017 [35]. Most sections of this paper are reproduced for the understanding of the concept. Further, this section is expanded with news regarding its commercial implementation.

5.1 Motivation

The nominal output power of LED lights is rising with recent development. For optimal performance, LED strings connected in parallel should be driven with matched current [36]. Currently paralleling is avoided by series-wiring all LEDs [37]. But that approach has safety limits: SELV limits the total DC voltage to 120 V [38]. Some LED lamp manufacturers even have decided to allow only 60 V. Assuming 3 V forward voltage per LED, the maximum number of series LEDs is limited to 20.

Another industry trend in LED flood lighting is to use mid-power LEDs [39]. HighPower LEDs tend to glare. As the luminescence per area of mid-power LEDs is comparatively low, they promise to be meeting anti-glare-requirements without lenses. Omitting lenses reduces cost and increases efficacy, but then no optical distribution can be set.

To achieve high luminescence output with many mid power LEDs, present single channel LED drivers require high output voltages and are not SELV compliant. In this section a simple, safe and cost-effective solution for paralleling LEDs is proposed, which allows to use a standard single channel constant current LED driver for parallel connection of LEDs. As the current is divided equally with respect to a variable input current, the proposed circuit allows for dimming. The circuit is implemented with state-of-the-art analog components, that are easily available.

5.2 State of the art

The state-of-the-art approach is to separate the LED driver into AC-to-DC stage and low voltage DC-to-DC stage, as shown in Figure 42. The current sharing stage is responsible for providing the appropriate currents to each LED string.

5.2.1 Resistors

The resistor paralleling approach in Figure 43 is widely used, e.g. in LED stripes. This paralleling approach can compensate the LED string currents, however, LED string currents can only be compen-

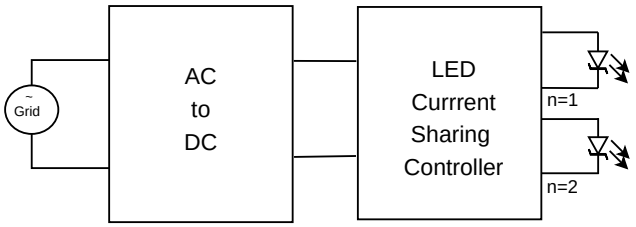


Figure 42: Generic LED driver topology for paralleling LED strings.

sated, but not matched. To achieve a decent and reliable equalization high resistances must be used. However, using a high resistance value introduces losses, lowering the modules efficacy.

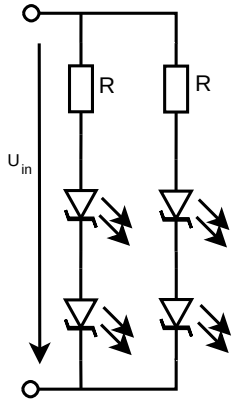
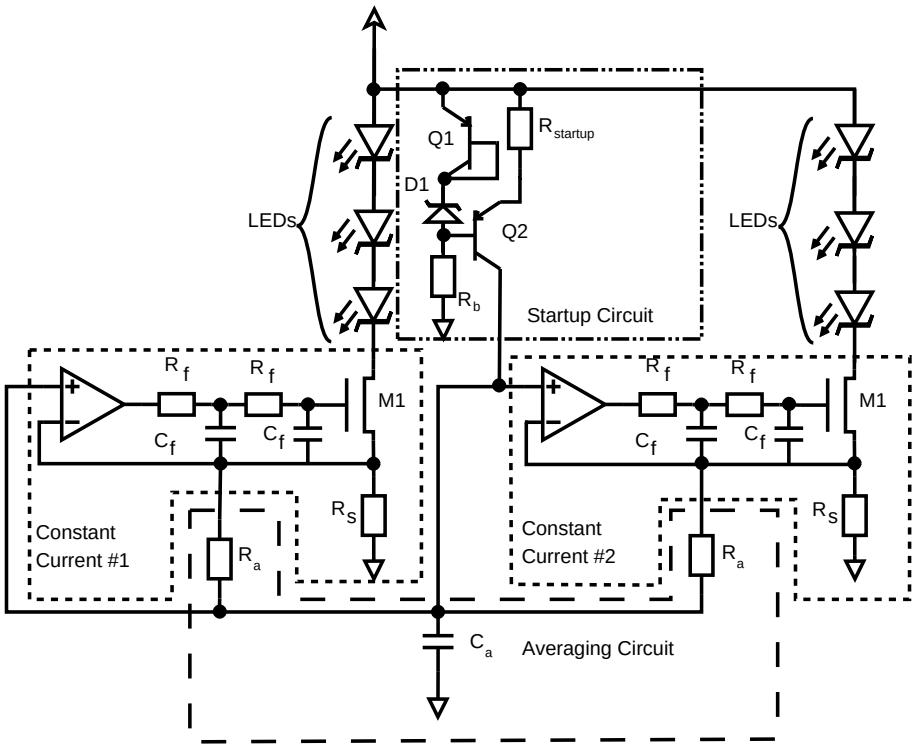


Figure 43: LEDs can be paralleled in the simplest manner by using resistors. While being simple and straight forward that approach has high electric losses.

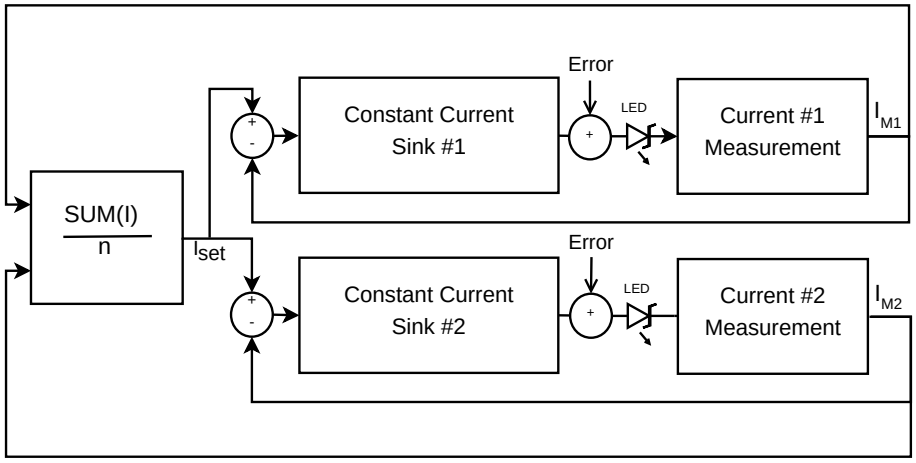
5.2.2 Buck Converter

Another option for paralleling is the use of a regulated buck converter for each string. In case one or several LEDs fail by short circuit, the buck converter can compensate for the lower string voltage. Using this approach the LEDs do not need to be matched by forward voltage. Thus the driver is more versatile. This flexibility comes at increased cost – especially when tens or hundreds of parallel channels are required. This approach is only possible if a higher entity, like a microcontroller, defines the desired forward current. Therefore, this approach utilizes only a fixed value. Hence, a dimming option is typically not supported by this approach.

To replace a 2.8 A high-power LED by 120 mA mid-power LED, up to 24 parallel strings are required. That's why the state-of-the-art constant current approach is highly costly and impracticable for mid-power LEDs.



(a) Circuit Diagram



(b) Control Diagram without startup circuit

Figure 44: Proposed novel current matching topology, based on a dissipative current limiter with self-determining set current. For startup an additional startup circuit is required.

5.3 Self Averaging Topology

5.3.1 Overview

A new averaging regulation topology targeted for low cost is proposed in Figure 44. The schematic is shown for two LED strings, but may be extended to $n \in \mathbb{N}$. The paralleling controller distributes a constant current equally to the LED strings. Therefore, it measures all string currents, averages them, and provides that value as a reference to the dissipative constant-current sink of each string. It feeds back its own average as a set value to allow for the dimming of the LED modules.

If an LED fails to short circuit, the string current does not change, as the additional voltage is dissipated in the constant current sink. The average current will also not change.

This simple paralleling approach is easy to use and does not require a predefined reference value by the circuit or from a microcontroller. Hence, it can follow the linear dimming of the primary constant current source while achieving good equalization of the LED string currents at any operating point.

5.3.2 Constant current regulation

The main constant current functionality is implemented using an operational amplifier combined with a mosfet, as shown in Figure 45. The operational amplifier adjusts U_{RS} that is equal to U_{Iset}.

$$U_{\mathrm{Iset}} = R_{\mathrm{S}} I_{\mathrm{LED}} \tag{5.1}$$

The second order low pass filter reduces the gain at high frequencies. The additional gain G_{CS} of the mosfet and sense resistor can be calculated to:

$$G_{\mathrm{CS}} = g_{\mathrm{M1}} R_{\mathrm{S}} \tag{5.2}$$

For a simplified calculation it is assumed that the additional gain is frequency independent. For a stable operation the following equation must be fulfilled.

$$G_{\mathrm{CS}}\, G_{\mathrm{OPV}}(f)\, G_{\mathrm{filter}}(f) < 1 \tag{5.3}$$

The additional required damping of G_{filter} at high frequencies is done by using a second order low pass filter, however, also lower and higher orders could be used. The second order low pass filter G_{filter} has 40 dB attenuation per decade. The compensated constant current source is shown in Figure 45.

The cutoff frequency f_{B} of the second order low pass is calculated, so that the systems gain at the operational amplifiers GBW frequency is less than 1.

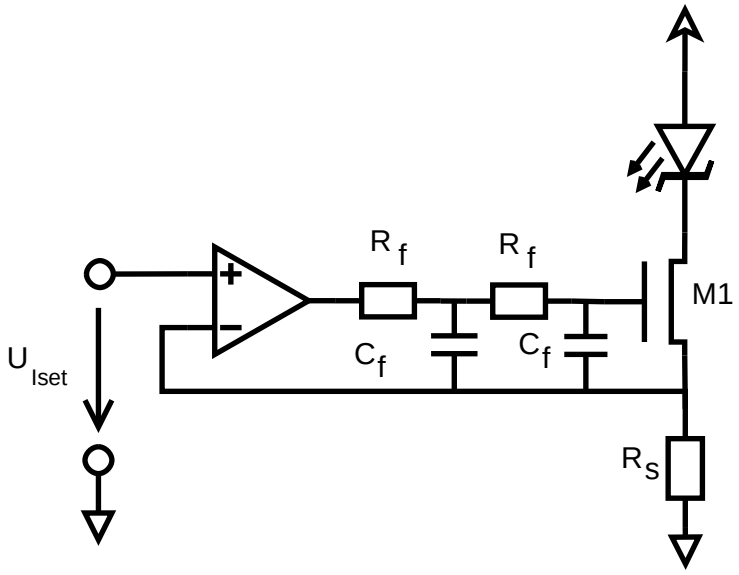


Figure 45: Compensated constant current source, in this example using a second order low pass filter.

$$f_{\mathrm{B}} = GBW \left(10^{-\frac{G_{\mathrm{CS}}[dB]}{G_{\mathrm{Filter}}[dB]}}\right) \tag{5.4}$$

The cutoff frequency f_{B} of a coupled second order low pass filter can be calculated using the following formula. By this, the values of R_{f} and C_{f} are chosen.

$$f_{\mathrm{B}} = \frac{1}{4\pi\sqrt{2}R_{\mathrm{f}}C_{\mathrm{f}}} \tag{5.5}$$

The mosfet M1 switches only in dissipative mode if the individual string current is above the average current, to maintain a safe current. However, when all LED strings have the same forward voltage, negligible conduction loss by the current measurement and by the mosfet can be observed.

Constant current filter design example For M1 the NTTFS4930 is chosen. From the datasheet a forward transconductance of $S = 19\frac{\mathrm{A}}{\mathrm{V}}$ is denoted. The sense resistor is chosen to $R_S = 1\Omega$ and calculate the gain.

$$G = R_{\mathrm{S}}S = 19 \tag{5.6}$$

The amplification is converted into log-scale:

$$20\log(G) = 26\,dB \tag{5.7}$$

To determine the number of decades of damping the system gain is set in relation to the used

second order low pass filter, with an attenuation of 40dB per decade.

$$\frac{26\,\mathrm{dB}}{40\,\mathrm{dB}} = 0.65\,dec \tag{5.8}$$

As an operational amplifier the IC LM324 is chosen. From the datasheet of the LM324 it is known that the Gain-Bandwidth-Product (GBP) is 1MHz. With this the boarder frequency for the damping network calculates to.

$$f_\mathrm{B} = 1\mathrm{MHz}\,10^{-0.65} = 223\,\mathrm{kHz} \tag{5.9}$$

The boarder frequency for the converter can be calculated using (5.5). Choosing $C_\mathrm{f} = 1\,\mathrm{nF}$, $R_\mathrm{f} = 281\,\Omega$. For a practical value $R_\mathrm{f} = 330\,\Omega$ is chosen.

5.3.3 Averaging Circuit

Conventionally a set current, represented by U_Iset, is determined by a higher entity. This approach has two drawbacks: First, a higher instance is required to determine the current if dimming should be used. Second, a connection is needed for transporting this information.

Therefore, a new method is proposed to determine the set current. Each LED-String current is measured at $R_{\mathrm{S_x}}$ and produces the voltage U_Sx. These currents are averaged over the samples and filtered to determine the U_Iset voltage. The filter cutoff frequency f_f of the averaging circuit should be chosen to be lower than the cutoff frequency $\mathrm{f_B}$ to prevent oscillation, recommended is a factor of 5 to 10.

The filter cutoff frequency can be tuned with the capacitor C_a. It can be calculated with the following formula, where n is the number of parallel strings.

$$C_\mathrm{a} = \frac{n}{2\pi f_\mathrm{f} R_\mathrm{a}} \tag{5.10}$$

Figure 46 shows the averaging circuit. The circuit shown is implemented in this setup as first order averaging circuit, but a higher order is also possible. The calculated average current is then used as set value U_Iset.

Note that the AC/DC power supply from Figure 42 must operate in constant current mode, to determine the overall LED module current.

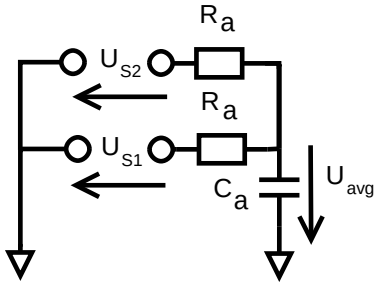


Figure 46: Averaging circuit determining the set current U_{Iset} using the individual sense voltages.

5.3.4 Startup Circuit

As U_{avg} is fed back to U_{Iset}, the circuit has two stable operating points. The initial operating point is at 0 A and the second at equally shared current. To ensure that the second operating point is used, the startup circuit forces a slightly higher current than the current the averaging circuit determines. This is done by adding a voltage offset, which is produced by a current source. The required current can be calculated to:

$$I_{\mathrm{startup}} = \frac{U_{\mathrm{Offset}} n}{R_{\mathrm{A}}} \tag{5.11}$$

In case an increased mismatch current should be accepted by the circuit the following formula can be used.

$$I_{\mathrm{startup}} = \frac{R_{\mathrm{S}} I_{\mathrm{mismatch}} n}{R_{\mathrm{A}}} \tag{5.12}$$

To generate the startup current, two possible solutions are analyzed, a dual transistor approach and a zener diode approach.

Transistor approach The transistor approach is shown in Figure 47. This approach uses two PNP transistors. The following formula can be used to calculate the startup resistor:

$$R_{\mathrm{startup}} = \frac{U_{\mathrm{BE}}}{I_{\mathrm{startup}}} \tag{5.13}$$

The bias resistor R_{b} is chosen to provide always a minimum operating current for the startup circuit.

This approach is highly temperature sensitive, as the bipolar transistors base emitter voltage U_{BE} changes with temperature.

Zener / Transistor approach As LED lamps generate heat, it is important to have an improved temperature stability of the startup circuit. The zener constant current approach, shown in Figure 48,

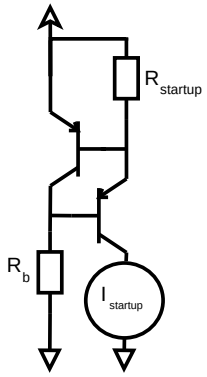


Figure 47: Transistor constant current source, using two transistors. This constant current approach is known to be temperature sensitive.

is designed for advanced temperature stability.

Q1 and D1 produce a voltage offset, where R_b is used to bias Q1 and D1. Q2 mirrors the voltage of only D1, which translates the voltage to a current. As the transistor Q2 has a fairly high amplification, the following equation holds true:

$$I_\mathrm{SRC} \approx I_\mathrm{Rstartup} \tag{5.14}$$

A bipolar transistor has a temperature coefficient of $-2\ \frac{mV}{K}$ [40]. By subtracting this temperature coefficient again, the transistors temperature drift is compensated. As the dual transistors are fabricated on the same die, both temperature coefficients and temperature are likely to be matched. The additional required zener diode should ideally have no temperature variation, thus a 5.6V zener diode [41] is ideal, as temperature drift is centered around $0\ \frac{mV}{K}$.

For the design the following equations hold true:

$$R_\mathrm{src} = \frac{U_\mathrm{D1}}{I_\mathrm{src}} \tag{5.15}$$

$$R_\mathrm{b} = \frac{U_\mathrm{supply} - U_\mathrm{Q1} - U_\mathrm{D1}}{I_\mathrm{bias}} \tag{5.16}$$

I_bias is the minimum cathode current of the zener diode specified by the datasheet.

Comparison The following simulation results of Figure 49 compare the two solutions. It can be observed that the dual transistor solution has a significant temperature drift, while the zener transistor solution offers decent temperature stability. Therefore, the zener transistor solution is favored in the complete design and verified in the section 5.4.6.

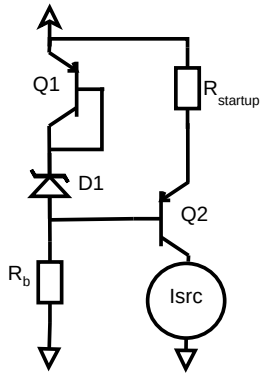


Figure 48: Zener constant current source, which is temperature compensated using matched Q1 and Q2 same die transistors.

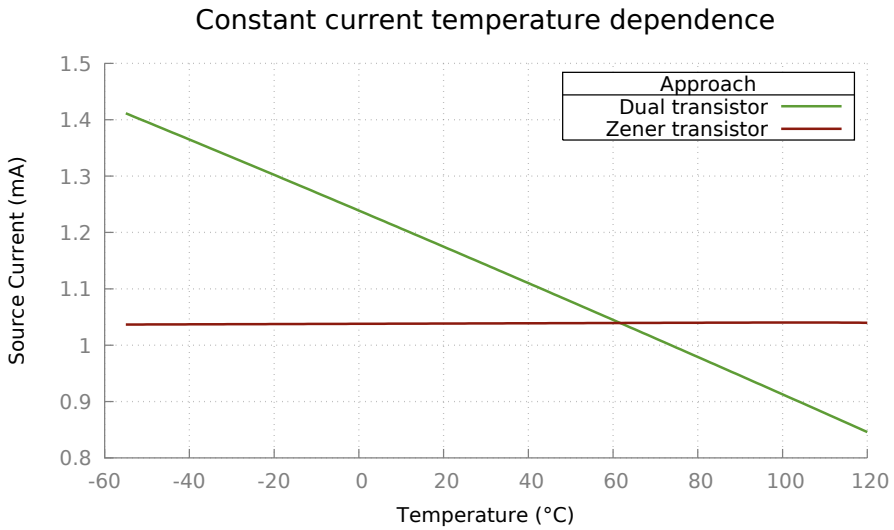


Figure 49: Temperature dependence of the two constant current sources (spice simulation). It can be observed that the zener transistor solution offers improved temperature stability.

5.4 Measurements

The design and its equations are validated by a prototype to prove the proper operational behavior of the circuit.

5.4.1 Measurement conditions

The measurements where done under the conditions stated in Table 5, unless not otherwise noted. The used measurement equipment is stated in Table 6.

5.4.2 Current Distribution

The current distribution over one module is depicted in Figure 50. It can be observed that the LED currents are matched within a distribution of 7 mA.

Parameter	Value
Number of parallel LED strings	24
Number of series LEDs	6
LED forward current	0.12A
LED type used	Lumiled 2835C
Op-amp	LM324
Mosfet	NTTFS4930
R_{sense}	1Ω
R_{f}	330Ω
C_{f}	1nF
R_a	4700Ω
C_a	1µF
Dual transistor (Q1,Q2)	BC857S
Zener diode	MM3Z5V6
R_{b}	150k
R_{startup}	220k
T_{amb}	20°C

Table 5: Component values and measurement conditions

Type	Model number
Multimeter	Pico Test M3500A
Power Supply	Korad KA3005D

Table 6: Used measurement equipment.

As a fairly low current sensing resistor is used to save power ($1\,\Omega$), the current distribution is within allowable limits. The typical operational amplifier offset of up to 5 mV can be observed in Figure 50. A voltage difference between different ground points can be observed: Though a solid ground plane is used, potential differences of up to 3 mV on the ground plane could be measured. Therefore, strong attention must be given to obtain a solid strong ground plane.

Also the startup circuit allows an additional mismatch current for the LEDs. For a better matching of LED currents the sense resistors could be increased, compromising efficiency. Using lower offset operational amplifiers can reduce mismatch.

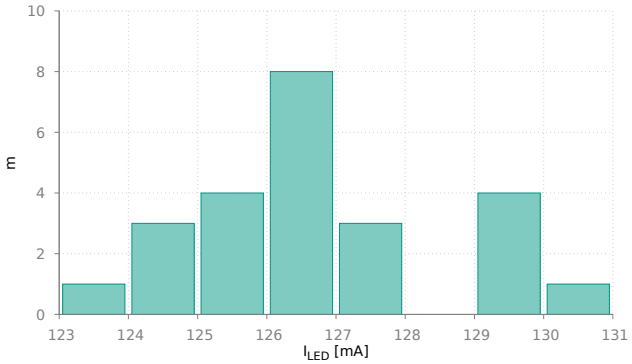


Figure 50: LED current distribution in the range of 123 mA to 131 mA, shows that the LEDs are sufficiently matched.

5.4.3 Voltage Drop over mosfet

The dropout voltage over the mosfet without the sense resistor voltage is depicted in Figure 51. The average drain-source voltage drop in this sample was measured to 105 mV. A higher voltage drop indicates that the circuit has to take more action to balance the strings. It can be observed that two out of 3 strings require active, dissipative regulation. The better the LED strings are matched, the less power loss can be observed. However, as previously discussed in section 3.2 on page 32, LEDs are typically regrouped in 100 mV bins.

5.4.4 Quiescent Current

As additional circuits are required for control, current for the regulation is required that is intended for lighting. The currents are listed in Table 7. However, the quiescent currents are fairly low ($<$4.4 mA) compared to 2.88 A total LED drive current. Therefore, the efficiency loss by quiescent currents can be neglected.

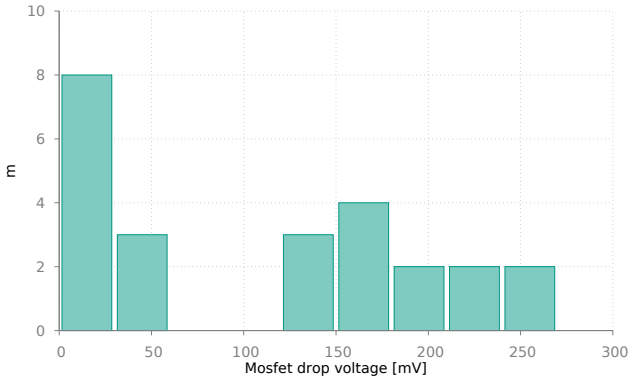


Figure 51: The voltage drop measured over the mosfet without the sense resistor voltage is depicted. It can be observed that even though one batch of LEDs is used, a significant difference in voltage drop can be observed.

Type	Quiescent current	Total
1/4 LM324	175 µA	4.2 mA
Startup circuit	140 µA	0.14 mA
Total		4.4 mA

Table 7: Quiescent current of each individual functional part and the sum of all loss sources.

5.4.5 Efficiency

The Table 8 depicts the losses. The sensing resistors are the most significant loss source followed by the equalization losses.

Loss source	Value
Quiescent losses	90 mW
Equalizing losses	302 mW
Sensing losses	345 mW
Total	750 mW

Table 8: Loss calculation of each functional part. The sensing resistors are the most significant loss source followed by the equalization losses.

5.4.6 Constant Current Source temperature drift

The constant current source for the startup circuit drifts by heat generated by the LEDs. For a stable performance, the constant current source should have a minimal sensitivity to the LEDs temperature. Figure 52 demonstrates the temperature dependency of the constant current source I_{src}. A typical drift is 2.5% over 60 K, which equals to a temperature drift of 417 ppm/K.

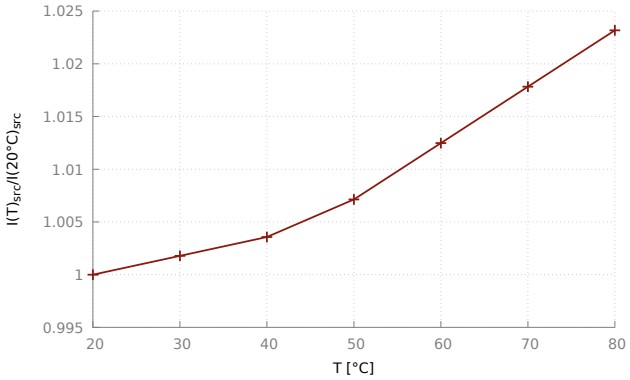


Figure 52: I_{SRC} temperature drift of the zener transistor startup circuit. (Section 5.4.6).

5.4.7 Reliability

So called catastrophic failures of LEDs are rare [42], and if so, typically a short circuit can be observed. When a short circuit failure occurs the additional voltage drop is taken by the mosfet, demonstrated in Figure 53.

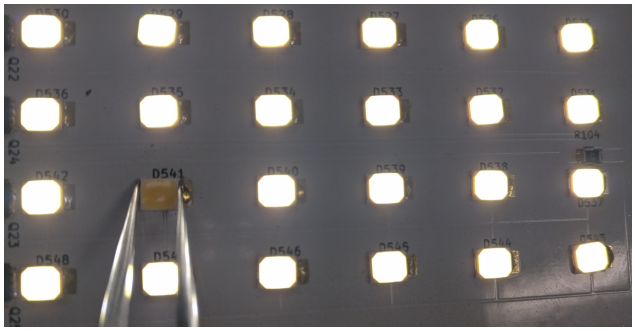


Figure 53: A short circuit of a LED is compensated without affecting the LED drive current of the other LEDs in the string.

Open circuit failure is not covered by the presented circuit diagram in Figure 44, as it is not likely. However, if open circuit failure should be covered additional zener diodes anti-parallel to the LEDs may be used.

5.5 Integration in street lamps

This technology was further developed to be deployed in LED streetlamps. A module was constructed for the project partner "Gratz Luminance", as shown in Figure 54. The project partner integrated this module to a die-cast aluminum cooler, which is IP56 proof. To proof the water-tightness of the case, the module is submerged in water, as shown in Figure 55.

To proof the operation of the LED modules in the field, 24 street lamps where equipped with this novel technology. The KIT innovation department and the inventors of this patent cooperated with

the company Gratz, supplying the LED system with the enterprise "Pfalzwerke", which is responsible for the LED installations in Maxdorf. The installed luminaries in Maxdorf are shown in Figure 56.

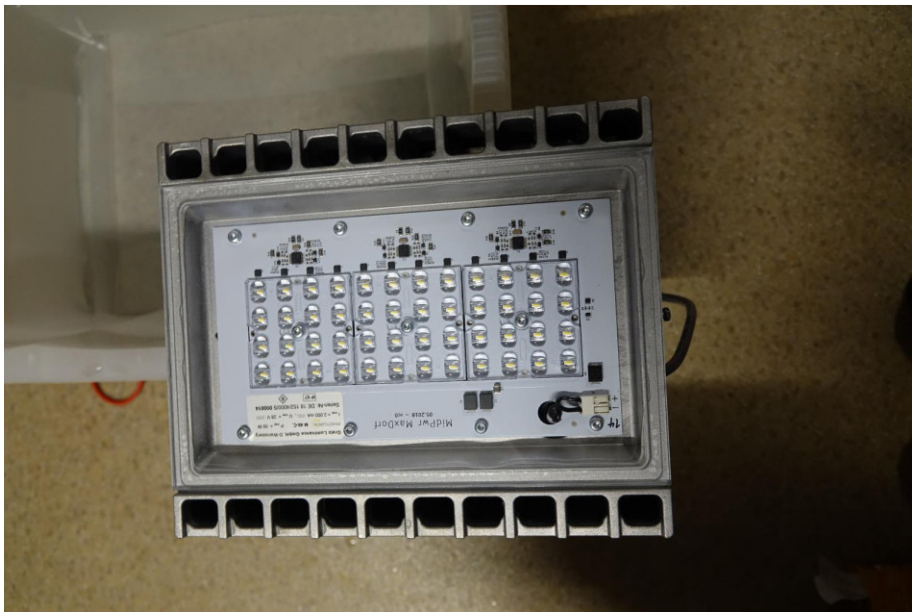


Figure 54: LED Module is integrated in a die cast case.

Figure 55: The LED module can be operated under water.

Figure 56: The novel street lighting technology is applied in Maxdorf, Rhineland-Palatinate, Germany

6 Lifetime Calculus

This section covers the theory of lifetime calculus. The theory is then applied on LED power supplies, which is practically verified in section 12.

6.1 Introduction

Recent statistics for LED streetlamps show that 52% of all failures are caused by the electronic power supply [4], referring to Figure 2 on page 22 in the introduction. For demanding applications, e.g. industrial control, telecommunication or safety critical areas, redundancy is often implemented by the N+1 scheme [43].

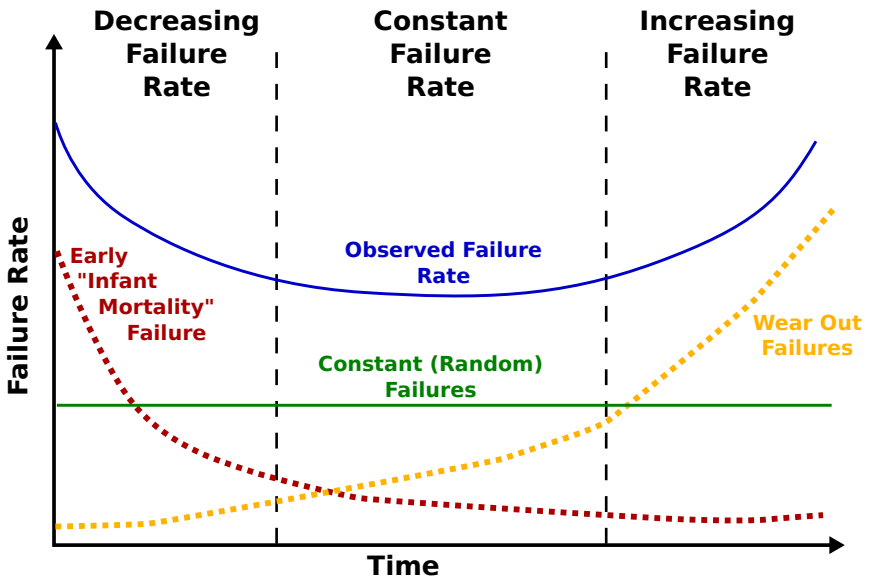


Figure 57: Bathtub curve with failure types. Image by the US Army, McSush.

Several failure types are known that often happen with a specific probability rate over time, referred to as the bathtub-curve [44, 45, 46], as shown in Figure 57.

- Infant-mortality failures are characterized as the failure rate dropping over time [46]. The infant mortality may have its cause in low manufacturing quality. It is assumed, that a burn-in is done to overcome infant mortality at the customer.
- Constant statistical failures happen randomly at a constant probability rate [46]. They are represented by the failure in time (FIT) rate. 1 FIT equals 1 failure every billion operation hours [5].

- Lifetime failures happen due to the wear out of components [45]. Their statistical probability to fail rises exponentially over operating time.

6.2 Thermal Cycling

Thermal cycling may lead to cracking solder joints [47, 48]. For reducing thermal stress, it is recommended to have a minimal temperature change. Primarily this can be achieved by ensuring a cool design. This means that the losses are minimized, while the thermal sink capabilities are maximized.

Figure 58 shows an Osram retrofit, where the inductor soldering pad encountered a crack, which caused the bulb failure. The other non-connected pin of the inductor is not a failure, it was damaged during removing of the PCB case. On the other side of the PCB, thermal marks indicated that the PCB was thermally stressed. This means that the component itself did not fail, its solder joint to the PCB failed. This lead to a full destruction of the LED retrofit. Hence, the limit for the component lifetime was limited by the device temperature. In particular in this case, the driver was the limiting factor of the LED retrofit.

Hence, the converter should be operated at an operating temperature as low as possible, while the temperature change during a cycle should be minimal.

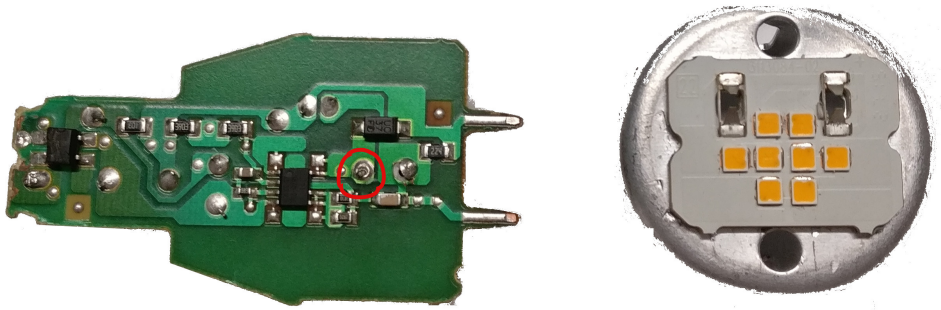


Figure 58: Example of a cracked solder in an Osram buck-converter LED retrofit

Figure 59 shows a cracked solder joint in more detail. Figure 59 shows the backside of an old CRT-TV set. The amplifying transistor Q901 is used to dissipate heat to the PCB by its pins. The thermal expansion and retraction lead to the crack in the PCB, finally leading to the break in the solder joints. Q901 controlled the RED channel of the cathode ray tube.

Apart from the obvious measures against cracking solder joints, in the literature counter-intuitive measures are reported. E.g. For ICs packaged in QFN, it is recommended to use thinner boards to reduce thermal stress [48].

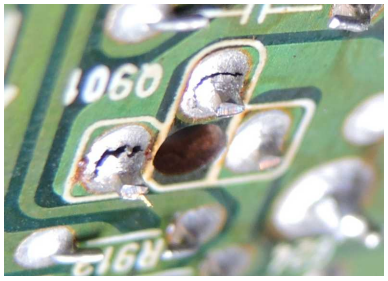


Figure 59: Cracked solder joint of a TV set.

6.3 Susceptible components for wear-out

The following section analyzes components that are susceptible to wear-out failures. Possible strategies for reducing the wear-out are presented.

6.3.1 Electrolytic capacitors

Based on the capacitor manufacturer analysis, electrolytic capacitors wear out due to drying electrolyte [49]. The probability of wear-out failure can be modeled as a bell-shaped curve with its peak at 1.2 times of the rated life with a standard deviation of 0.1 [50]. At the rated lifetime, 2.3% of all electrolytic capacitors will already have failed. For this analysis, it's assumed that 2.3% failure can be tolerated before end of life.

Furthermore, a temperature reduction by 10 degrees doubles the lifetime. If an operating voltage U_o below the rated voltage U_r is used, lifetime is also prolonged with an exponent of up to 4.4. If the capacitor is self-heated, it additionally reduces the lifetime by a factor of 2 for every 5 degree temperature rise. Illinois capacitors proposes the following formula to calculate the lifetime[51].

$$t = 2^{\frac{T_\mathrm{r}-T}{10}} 2^{\frac{-\Delta T}{5}} t_0 \left(\frac{U_\mathrm{o}}{U_r}\right)^{-4.4} \tag{6.1}$$

The construction of an electrolytic capacitor is shown in Figure 60. From the outside to the inside the capacitor consists out of an insulating sleeve that protects against electric contact of surrounding components to the aluminum can. It houses the wound cell, consisting of an anode aluminum foil that is etched and then covered with aluminum oxide to increase its surface area. Paper, impregnated with electrolyte is used between the aluminum foil layers.

The electrolyte, in which the paper is impregnated is typically calcium hydroxide, which tends to evaporate at high temperature [49]. Thus, typical operating temperature of such capacitors is 85°C. Special high temperature capacitors typically allow 105°C. For specific applications also temperature up to 130°C have been demonstrated. Measurements of 105°C capacitors at nominal operating temperature have shown a lifetime of 4'000 hours [52]. However, also capacitors with higher life expectancy are

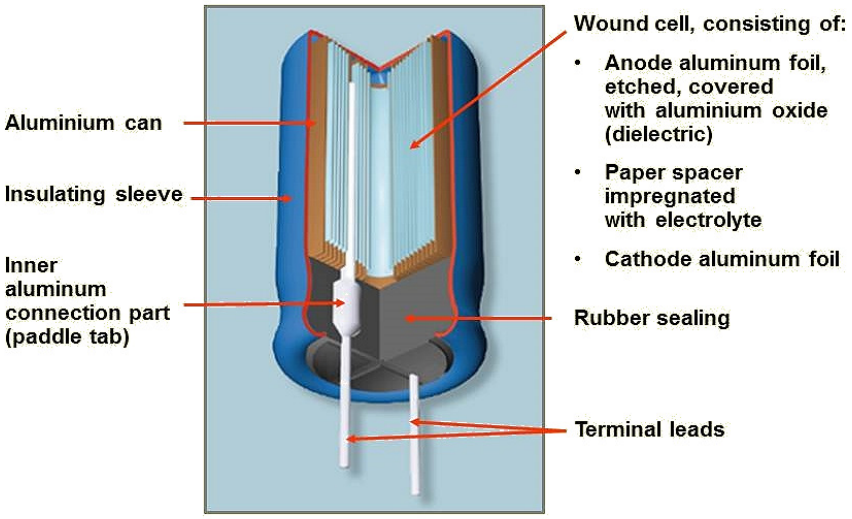


Figure 60: Electrolytic capacitor construction. Public domain graphics from Elcap.

available.

6.3.2 Film Capacitors

Film capacitors have a significantly increased nominal lifetime (30'000 hours) compared to electrolytic capacitors [53]. Illinois Capacitors proposes a lifetime formula that includes the effect of voltage stress [54], which is similar to the to (6.1).

$$t = 2^{\frac{T_\mathrm{r}-T}{10}} t_0 \left(\frac{U_\mathrm{o}}{U_r}\right)^{-7} \tag{6.2}$$

From (6.2) it can be seen, a self heating term as seen for the electrolytic capacitor is not present.

Because of the high exponent of 7 for the voltage term, lifetime increases highly if the rated voltage U_r is chosen larger than the operating voltage U_o. Some resources propose even an exponent of 8 [55]. This means, by choosing an 800 V capacitor for a 600 V DC Link, the lifetime is prolonged by a factor of 7.5. When operated at 85 °C, lifetime increases by an additional factor of 4: A lifetime of 900'000 hours for the film capacitor is possible, which equals a lifetime of 102 years. It may be questionable, if such a long lifetime is required, as discussed in section 2.4.4. However, it can be summarized that when a electrolytic capacitor is replaced by a properly selected film capacitor, the converter lifetime should not be limited by the capacitor.

The capacitor manufacturer Vishay is more conservative regarding their product lifetime estimation. Figure 61 shows the lifetime of a film capacitor that can be used at 105°C up to 10'000 hours. However, at 70°C and 60% voltage Vishay estimates a lifetime of 1 Million hours.

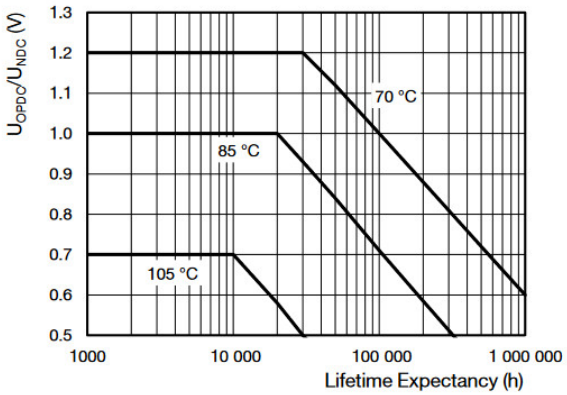


Figure 61: Lifetime of a film capacitor. Extracted from capacitor datasheet Vishay MKP1848.

Despite the lifetime advantage of film capacitors, they require an increased build volume. As this increase would be significant, typically a smaller value capacitor for the DC-Link is required. To accept these high voltage ripples on the DC link, a new modulation scheme is required that will be presented in section 7.

6.3.3 Mosfet

Other components, like power Mosfets may also wear out, e.g. when the maximal avalanche energy stress is exceeded [56]. However, manufacturer data indicates that FIT rate is extremely low (0.2 FIT) [57] when limiting parameters are respected. Significant efforts by manufacturers have been undertaken to improve quality [57, 58]. Especially the following parameters must be observed:

Device Temperature A high device temperature increases the mosfets drain source resistance, producing additional heat. Additional heat also increases thermal stress.

Maximum Blocking Voltage The maximum mosfet blocking voltage must be chosen with significant safety margin. Infineon recommends a 10% - 30% increased voltage rating for long life applications [59]. Power mosfets burn out can be caused by high energy neutrons [60]. This failure issue is more likely at high altitude.

Infineon reports that the breakdown voltage at 100 °C to 120 °C is about 7% higher than at room temperature [59]. If a cool and reliable design should be obtained, this safety margin should not be used.

Gate Drive A slow gate voltage change, may produce additional switching losses. A fast switch-over can be ensured by using high current drive gate driver. Switching frequencies for SiC mosfets as high

as 2.5MHz have been demonstrated [61].

6.3.4 Crystal Oscillators

Crystals are an additional failure source. According to [62], failure sources are wide spread. Typical failure issues can be variation out of:

1. Crystal substrate
2. Wire connection
3. Poor adhesion to the substrate
4. Contamination of the crystal
5. Poor adhesion to the crystal
6. Faulty hermetic sealing

Therefore, for this design the internal silicon oscillator of the chip was used to avoid this problem. It is pretested by the MCU manufacturer.

6.3.5 Fuses

Fuses may be susceptible to inrush currents, when temperature derating is not observed correctly [63]. Therefore, slow blowing fuses are recommended and used in this design.

6.3.6 Metal Oxide Varistor

Metal Oxide Varistors are used to protect against surges, as shown in Figure 62. Surges are defined as fast voltage spikes above the nominal voltage. They are tested with respect to the 8/20 µsec test pulse [64]. Hence, surges are fast events that only occur rarely for a short period. One typical cause may be a voltage spike caused by a lightning. Other more or less likely issues, like tripped circuit breakers or a electromagnetic pulses may cause the transients too.

For the SLC converter Metal Oxide Varistors are used, as shown in the schematic in Figure 63. Metal oxide varistors can dissipate a significant higher amount of energy compared to transient voltage suppressors.

After a specific amount of energy is absorbed, the varistor encounters a short-circuit catastrophic failure. Then the fuse S_1 is required to not short the upstream supply voltage. A non-catastrophic transient absorption may undeliberately trigger the fuse. Thus, the fuse S1 should be chosen with overhead. As overvoltage events are short-term events, a slow-blowing fuse is recommended.

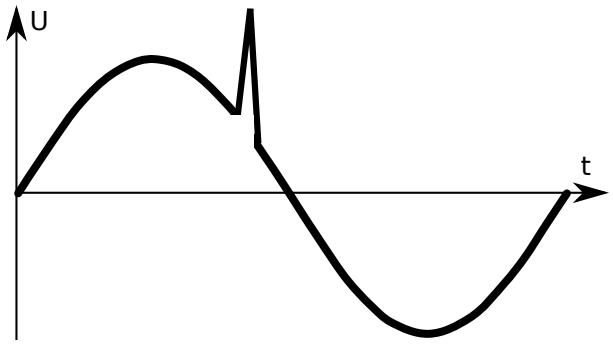


Figure 62: Example of a surge on a sinusoidal voltage.

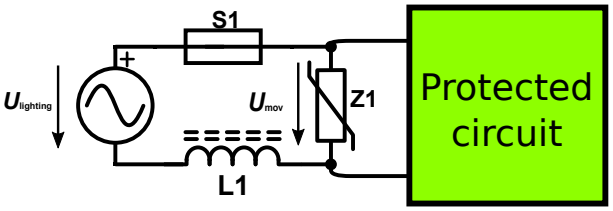


Figure 63: A metal oxide varistors Z_1 is placed directly after the fuse to absorb incoming overvoltage. The subsequent circuits are protected by the metal oxide varistor.

To design-in a Metal Oxide varistor [65], the peak current is calculated by the complex input impedance. To increase the complex inductance, a series inductor is placed upstream, as shown in Figure 63.

$$I_{\mathrm{mov}} = \frac{U_{lighting} - U_{\mathrm{mov}}}{Z_{\mathrm{in}}} \tag{6.3}$$

The energy for a $t_{lighting} = 20\,\mu\mathrm{sec}$ pulse can be calculated by the following formula:

$$E = \frac{I_{\mathrm{mov}} U_{\mathrm{mov}} t_{lighting}}{2} \tag{6.4}$$

The absorbed energy should be far less than the maximum tolerable surge energy. Wen and Zhou propose the following lifetime aging formula [66] for MOV voltage stress under non-clamping conditions:

$$t = t_o\,(2.5)^{\frac{T_{\mathrm{u}} - T_0}{10}} \tag{6.5}$$

The formula indicates, that with every 10 °C temperature increase, the MOV ages approximately 2.5 faster.

6.4 Energy Density Considerations

Currently, electrolytic capacitors are favored in designs due to their more then 10 times higher energy density than film capacitors. An example is shown in Table 9.

Capacitor / Partnumber	Voltage / Capacitance	Energy	Volume	Energy Density
Long Life Electrolytic Capacitor EKXL451ELL470MK30S	450V 47uF	4.7J	3680 mm3	0.0012 J/mm3
Film Capacitor MKP1848C61290JP2	900V 12uF	4.86J	28240 mm3	0.00017 J/mm3

Table 9: Energy Density of Capacitors: Film vs electrolytic capacitors

Assuming that an electrolytic DC link capacitor requires 3% - 5% board space on the PCB, the build volume of a power supply with film capacitors and the same capacitance will increase by 27% - 45%. However, the electrolytic capacitor ripple current rating is typically the bottleneck and not the capacitance. Referring to Table 10, film capacitors typically accept 20 - 40 times higher ripple current compared to electrolytic capacitors. Thus, the additional required size will be less than calculated, typically in the range of 10% to 20%.

Capacitor	Voltage / Capacitance	Current Capability
Long Life Electrolytic EKXL451ELL470MK30S	450V 47uF	440mA
Film Capacitor MKP1848C61290JP2	900V 12uF	9A

Table 10: Peak current capability of capacitors

Further, DC link capacitors are oversized due to slow regulation. A typical application would be a power factor correction with a downstream series LC converter. However, new algorithms using digital control are developing, allowing high DC-Link voltage tolerance and reduced capacitance value requirements [67].

6.5 Predictive Maintenance

Predictive maintenance issues a repair or replacement of the component, before the component is broken [68]. The health of electrolytic capacitors in UPS or inverters is currently online monitored by impedance analysis [69]. This is based on the principle that the electrolytic capacitor equivalent series resistance (ESR) increases while the capacitance decreases [70]. Film capacitors show also an exponential ESR increase [71]. However, their internal resistance is comparatively low and thus hard to measure. Considering that a load is known, it is proposed to focus on the capacitance itself. Its

decrease is linear with time [71]. Thus, their remaining work hours can be extrapolated by using the following formula:

$$t = \frac{C_{\text{measured}} - C_{min}}{c} \tag{6.6}$$

Where c is the decrease of capacity per hour.

6.6 Failure in Time

Typical FIT rates are shown in Table 11. The typical electrolytic capacitor failure rate is shown only for reference.

Component	FIT-Rate
Electrolytic Capacitor	200
Film Capacitor	50
MCU	20 @ 85°C
SIC Diode	0.2
SIC Mosfet	23

Table 11: FIT Rate of electronic components used in power supplies

In accordance with Table 11, assuming a system FIT rate of 200 FIT, one device will fail every 5 million hours. This means that one in five products will fail during the lifespan of 100 years. If electrolytic capacitors would be used, FIT rate would be significantly increased.

6.7 Power Supply Lifetime Calculation

The total lifetime can be calculated according to the following formula:

$$L^{-1} = \sum L_i^{-1} \tag{6.7}$$

Based on the analysis, the film capacitor has a lifetime of 108 years. According to the statistics, based on the failure over time, 1 in 5 products will fail early during this period. Based on (6.7), the lifetime of the converter is estimated to 88 years. However, this result may be treated with caution, as it cannot be verified.

6.8 Total cost of ownership

The total cost of ownership estimates, how much money the operation of the equipment costs over its lifetime. Examples of this cost are:

- Setup costs are the cost of the power supply and the installation cost.
- Operating cost occur during operation of the equipment. One example e.g. is the electric power consumption or the cost of an air conditioner if utilized for the equipment.
- Maintenance or service cost cover the repair and service of the device.
- Lost production cost estimate how much money is lost, when the equipment is not operational.
- Disposal fees are the cost for the disposal of the equipment.

To optimize the total cost of ownership, the sum of all cost should be minimal.

The outtime cost caused by one damaged power supply in a factory is now estimated. One hour of a factory has a productivity of typically 1'000 to 10'000 Euro. Assuming a productivity of 10'000 Euro per hour with one outage of 1h with an 100 Euro / 10 year power supply costs are 11.6 ct per operational hour over a ten year lifespan. This calculation does not include the servicing fee.

If instead a 500 Euro - 88 year power supply is operated over 10 years would be used, the total cost of ownership calculates to 0.57 ct per hour. This shows that high reliably power supplies can drastically reduce missing quality cost in high productivity environments.

However, LED street lighting may not be considered as such high productivity application. Hence, the costs of missing quality are mostly less severe. Based on previous research, it is assumed that a power supply costs 20 Euro and has to be replaced 5 times over the luminaires lifetime. A servicing fee of 200 Euro is estimated. Hence, the total replacement costs over a twenty year lifespan are 1100 Euro.

A quality power supply will cost 200 Euros. Hence, the total cost of ownership can drastically be reduced even for low productivity environments. Despite of the significant saving potential, the initial costs have a major influence on sales. A total cost of ownership argumentation is commercially not yet utilized by the LED luminaires manufacturers.

7 PFC/SLC Topology Analysis

In this section the previously selected PFC/SLC topology will be analyzed in the time domain. The converter will be modeled as a controlled current source. The equations are solved for the governing factors, to obtain an open-loop model for each converter section. By this new kind of modulation technique, applied on the PFC/SLC topology, the input current as well as the output current can be controlled solely with a single half bridge.

Early stage research of this topic was published on EPE Warsaw 2017[72]. Parts of the corresponding paper may be reproduced for enhanced understanding.

7.1 Topology Overview

AC to DC power supplies are typically constructed using a two stages [73, 9] topology: The first power factor correction (PFC) stage sets the sinusoidal input current and controls the energy demand from the AC grid. The energy is used to charge a DC-link capacitor. The second stage consists of a galvanic-isolating DC-DC converter, converting the high DC-link voltage with double grid frequency ripple to a stable DC output voltage.

Recent work has been published combining those two stages: A bridgeless totem-pole PFC with a series resonant converter [9, 74]. The proposed topology in this paper is modified from series resonant converter to a series inductor capacitor converter (SLCC) shown in Figure 64.

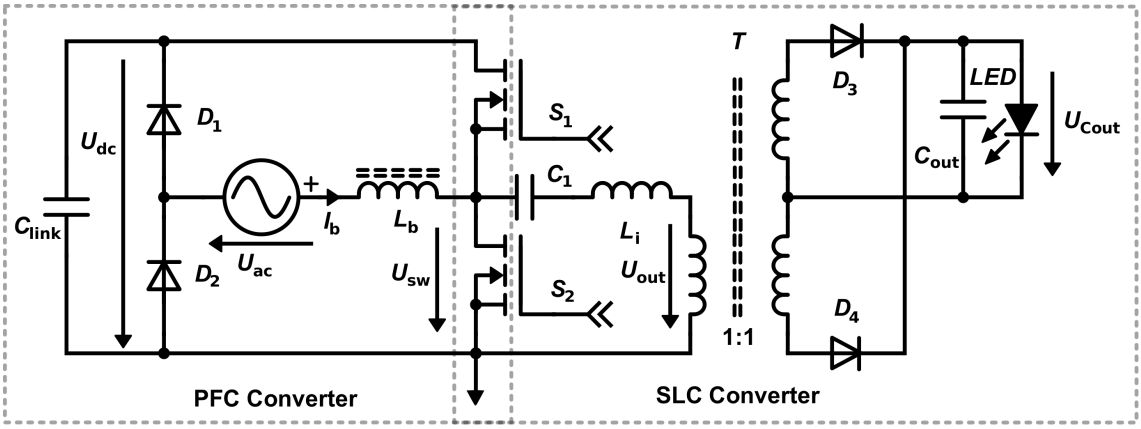


Figure 64: A power factor correction (PFC) circuit and a SLC converter share a single half bridge. State-of-the-art modulation techniques do not filter the double mains frequency on the secondary side [9]. A novel modulation technology will be used to separate the C_{link} ripple from the secondary side.

The advantage of this topology is the reduced number of switches. However, with state-of-the-art modulation techniques [9], the double mains frequency DC-link ripple still can be observed on the secondary side output voltage. Previous work [9] yielded an improvement by adding a secondary side buck converter, achieving only a quasi single stage converter. Thereby the advantage of a single stage

AC-DC converter is lost.

To achieve a true single stage converter two set variables are required: The input AC current I_{ac} and the output current I_{out} [72]. As two controlling factors are desired, at least two actuating variables are required. State-of-the-art SLC converters typically alter the switching frequency to control the output voltage. Boost converters typically change the duty cycle to regulate the desired input current. Therefore, it is self-evident to use both set variables for modulation.

However, both parameters are influencing each other. This means that changing the period t_{c} of the boost converter changes the grid input current, but also the output current of the SLC converter. Therefore, an equation must be developed that calculates the duty cycle and the frequency for a given grid input current and a given LED output current. The corresponding calculus is done in the control section 8, using the findings of this analysis section.

In contrast to previous work [9, 75, 76, 77], the converter is modeled in the time domain and not in the frequency domain. Further, resonant converters are mostly modeled as voltage to voltage converter [75, 76, 77, 78, 79, 80, 81, 82]. However, LEDs must be controlled by current: Therefore, the converter is modeled as an averaged current source.

For C_1 a large value is chosen so that a linear, time dependent formula for the inductor current L_{i} can be formulated. The modulation technique is based on a deep mathematical analysis of the topology, describing the mean AC input current $\overline{I_{\mathrm{ac}}}$ and the mean DC output currents $\overline{I_{\mathrm{out}}}$ averaged over the switching period t_{c}. The equations are then solved to obtain the duty cycle D and switching period t_{c}, as a function of the required current and measured voltages.

7.2 Topology Description

The functional blocks of the topology are depicted in Figure 64. The totem-pole PFC can be observed on the left-hand side, consisting out of an active half bridge (S_1, S_2), the dc link capacitor C_{link}, boost inductor L_{b} and passive diode half bridge (D_1, D_2). On the right hand side the SLC topology is shown, which shares the active half bridge and the DC-link capacitor C_{link}. On the secondary side a rectifier (D_3, D_4) converts the high frequency AC current to DC, which is filtered by the output capacitor C_{out} and consumed by the LED.

7.2.1 Boost Converter

For a positive AC voltage, referring to Figure 64, the boost converter's inductor L_{b} is charged from the AC input, over S_2 and D_2. In the next switching period L_{b} is discharged into C_{link} over S_1 and D_2 and the AC source. The PFC is configured as a bridge-less totem-pole PFC. Therefore, the duty cycle has to be inverted according to the grids voltage phase [83].

The PFC boost converter is operated in discontinuous mode [9]. As the current always returns to zero, an open-loop control can be implemented to set the input AC current. In continuous conduction mode, an open loop control function could not be formulated, as the start value of the inductor current I_{B} depends on the previous switching cycle.

7.2.2 SLC Converter

The SLC converter configuration can be observed on the right hand side in Figure 64. The converter is operated above the resonance frequency [72]. The transformer's stray inductance L_{i} is integrated into the single transformer T1, where the transformer's magnetizing inductance is designed to have a large value. Therefore, the current flowing through the magnetizing inductance is considered to be low and is disregarded. The SLC converters current will have a linear shape while the converter is operated far above its resonance frequency. The current can be described as a linear equation, using the sinusoidal small angle approximation:

$$sin\,(x) \approx x \quad \forall \quad x \to 0 \tag{7.1}$$

To achieve this, C_1 has to be large [72]. As the converter is operated in the inductive region, zero voltage switching (ZVS) of the power switches (S_1 and S_2) can be realized.

7.3 Boost Converter Analysis

This section analyses the PFC boost converter in detail. At the end of the analysis, the average converter input current is formulated.

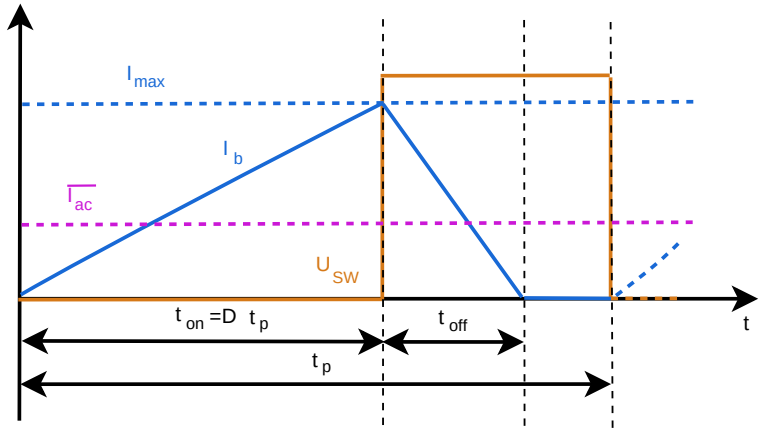


Figure 65: The boost converter waveform shows the three time steps t_{on}, t_{off} and t_{p} of the boost PFC converter.

The discontinuous boost converter waveform is shown in Figure 65 for a positive AC voltage [72]. As

it operates in discontinuous mode, three phases are present. The charging phase (t_{on}), the discharging phase (t_{off}) and the zero phase. The switching period is designated t_{c}. The variables are named with respect to Figure 64.

7.3.1 Charge State

The charge state ($0 \leq t \leq t_{\mathrm{on}}$) is present, while S_1 is opened and S_2 is closed [72], assuming a positive grid voltage. Current will flow over D_2, AC, L_{b} and S_2. The grid voltage U_{ac} is treated as a quasi constant. Quasi-constants must be measured continuously by the controller. However, these variables can be treated as a constant value for the calculation during one switching cycle. Based on the inductor's formula the current in the boost inductor is linear with time:

$$I_{\mathrm{B1}}(t) = \frac{U_{\mathrm{ac}}}{L_{\mathrm{b}}} t \tag{7.2}$$

The ontime t_{on} is given by the duty cycle definition and Figure 65.

$$t_{\mathrm{on}} = t_{\mathrm{p}} D \tag{7.3}$$

7.3.2 Discharge State

The discharge state ($t_{\mathrm{on}} < t \leq (t_{\mathrm{on}} + t_{\mathrm{off}})$) is present, while S_1 is closed and S_2 is opened. Current in the discharge state will flow over D_2, AC, $\mathrm{L_b}$, S_1 and $\mathrm{C_{link}}$, with respect to Figure 64. In the beginning of the discharge stage, the current equals to the current at the end of the charge state. The grid voltage U_{ac} is considered constant again. Thus, the following linear equation can be formulated:

$$I_{\mathrm{B2}}(t) = I_{\mathrm{B1}}(t_{\mathrm{on}}) + \frac{U_{\mathrm{ac}} - U_{\mathrm{dc}}}{L_{\mathrm{b}}} t \tag{7.4}$$

Based on the discontinuous operation property of the PFC $I_{B2}(t_{\mathrm{on}} + t_{\mathrm{off}}) = 0$ and (7.3) the off-time t_{off} can be calculated as:

$$t_{\mathrm{off}} = \frac{U_{\mathrm{ac}} t_{\mathrm{p}} D}{U_{\mathrm{dc}} - U_{\mathrm{ac}}} \tag{7.5}$$

7.3.3 Average Charge Current

The arithmetic average current flowing through the inductor is calculated by the arithmetic mean formula and refers to Figure 65.

$$\overline{I_{\mathrm{ac}}} = \frac{1}{t_{\mathrm{c}}} \left(\int_{t=0}^{t=t_{\mathrm{on}}} I_{\mathrm{B1}}(t)dt + \int_{t=0}^{t=t_{\mathrm{off}}} I_{\mathrm{B2}}(t)dt \right) \tag{7.6}$$

$$\overline{I_{\mathrm{ac}}} = \frac{I_{max}}{2t_{\mathrm{p}}} \left(t_{\mathrm{on}} + t_{\mathrm{off}} \right) \tag{7.7}$$

Equation (7.3) and (7.5) are inserted into (7.7) to obtain (7.8).

$$\overline{I_{\mathrm{ac}}} = \frac{I_{\mathrm{max}} D}{2} \left(1 + \frac{U_{\mathrm{ac}}}{U_{\mathrm{dc}} - U_{\mathrm{ac}}} \right) \tag{7.8}$$

The maximum current flowing through the inductor can be calculated with (7.2) to:

$$I_{\mathrm{max}} = I_{\mathrm{B1}} \left(t_{\mathrm{on}} \right) = \frac{U_{\mathrm{ac}}}{L_{\mathrm{b}}} t_{\mathrm{on}} \tag{7.9}$$

With (7.9) the average AC input current $\overline{I_{\mathrm{ac}}}$ can be calculated.

$$\boxed{\overline{I_{\mathrm{ac}}} = \frac{D^2 t_{\mathrm{p}} U_{\mathrm{ac}} U_{\mathrm{dc}}}{2L_b \left(U_{\mathrm{dc}} - U_{\mathrm{ac}} \right)}} \tag{7.10}$$

The average input current $\overline{I_{\mathrm{ac}}}$ is directly proportional to D^2, t_{p} and $\frac{1}{L_{\mathrm{b}}}$. U_{ac} and U_{dc} can be treated as quasi-constants. The equation will be used again for the open-loop controller.

As a PFC should appear to the grid as a resistive element, it can be modeled as a conductance. Based on the conductance definition (7.11) and on the AC input current equation (7.10) the average input conductance $\overline{g_{\mathrm{in}}}$ can be calculated:

$$g_{\mathrm{in}} = \frac{I}{U} \tag{7.11}$$

$$\overline{g_{\mathrm{in}}} = \frac{U_{\mathrm{dc}} t_{\mathrm{p}} D^2}{2L_b \left(U_{\mathrm{dc}} - U_{\mathrm{ac}} \right)} \tag{7.12}$$

7.4 Duty cycle inversion

As a totem-pole PFC is used, the actual duty cycle D^{T} must be adjusted according to U_{grid} polarity [83]. The adjustment rule is shown in (7.13). The transition must be continuous in order not to trigger the overcurrent protection. Therefore, the duty cycle inversion is implemented in a continuous matter in software, further explained in section 8.3 on page 113.

$$D^{\mathrm{T}} = \begin{cases} 1 - D & U_{\mathrm{grid}} \geqq 0 \\ D & U_{\mathrm{grid}} < 0 \end{cases} \tag{7.13}$$

The speed of the capacitor voltage change U_{C1} must be limited, as the utilized film capacitors allow only a specific voltage change over the time. As a rule of thumb, the higher the capacitance, the smaller the allowable RMS specific voltage change over time. For example a 470nF 630V DC allows only a RMS voltage ripple of 20V at 100kHz [84].

7.5 SLC converter analysis

7.5.1 Introduction

In conventional approaches the series resonant converter (SRC) shown in Figure 66 is modeled as a voltage-to-voltage converter [75, 76, 77, 78, 79, 80, 81, 82]. Switching of the converter can be studied in the literature [85, 86]. Three major design methods can be identified [87] for the voltage to voltage converter topology: (1) First Harmonic Approximation (FHA) in the frequency domain [88, 89], (2) extended FHA [90, 91] and (3) time domain analysis [85, 86]. Time domain analysis minimizes approximations, thus promises the best results. Hence, this analysis is chosen for the considered converter. As it is then not operating in resonant mode, it is designated as a series LC (SLC) converter.

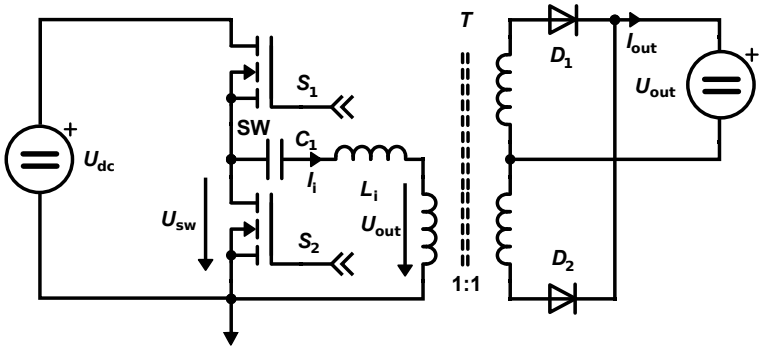


Figure 66: Series resonant converter topology.

SRC can employ the following control methods: (1) frequency [77, 88, 92], (2) phase when two half bridges are present [93, 94], (3) duty cycle using fixed frequency [95, 96, 97], or (4) modulation of frequency and duty cycle at the same time [98]. Last control method has two degrees of freedom, which are necessary when one additional converter, e.g. a boost converter working as a power factor correction (PFC), is connected to the half bridge [99, 72].

The controller typically is a PID controller [100]. However, fuzzy logic [101], non-linear control [102, 103] or neural control [104] have been demonstrated as well. A novel SLC feed forward control

equation with disturbance rejection is proposed. The disturbances of the input- and output voltage on the average output current are described. Control of a state-of-the-art SRC can be achieved using an off-the-shelf frequency modulation IC [105, 106] or a digital signal processor (DSP) [107, 108, 109]. As non-linear calculations are used for the proposed control method, a DSP is highly recommended.

Conventional voltage-to-voltage controlled converters tend to have light load stability problems [77] and slow transient responses [78], which may lead to overcurrent events [110, 111]. Direct feed forward current control (DFFCC) is employed in this case, which is shown to be stable. For this purpose, the SLC open-loop output current is averaged over one switching period to obtain the desired output current. However, parameter variations may lead to inaccuracies. To compensate for transfer function inaccuracies, an outer closed loop control is utilized. It consists of a closed-loop PID regulator.

A non-linear, steady-state, analytically solvable open-loop current control equation is presented in this work, which offers two degrees of freedom, i.e. the duty cycle and the frequency. To simplify circuit analysis and obtain linear equations, the converter is operated far above the resonance frequency. In this way zero-voltage switching can be achieved with respect to the switch node [112].

7.5.2 Analysis Domains

The SLC output current transfer function is developed in the time domain. While frequency analysis is possible and is in general use, the circuit must be greatly simplified. At extreme duty cycles close to zero and one, the waveforms of the approximation change drastically.

7.5.3 Drawbacks of frequency analysis

In the frequency domain First Harmonic Approximation (FHA) the diode bridge rectifier is omitted and the voltage sink is replaced by an equivalent load resistor as shown in Figure 67 [77, 88, 92].

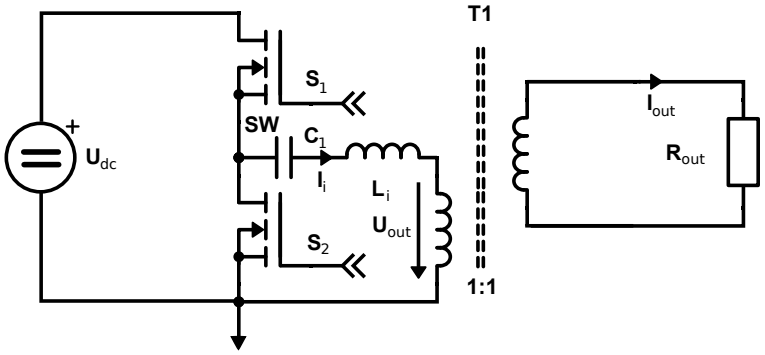


Figure 67: The SLCs output rectifier and capacitor are replaced by a load resistor for FHA.

Both circuits shown in Figure 66 and Figure 67 are simulated within Spice simulation. Especially at low $(0 < D \lll 0.5)$ or high $(0.5 \lll D < 1)$ duty cycles, the waveform is distorted significantly,

as shown in Figure 68. Circuit simplification significantly changes the transformer current, and the converter cannot be modeled accurately.

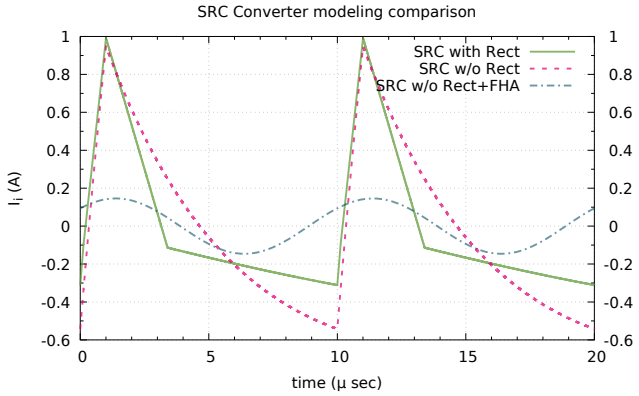


Figure 68: Spice simulation of the inductor current according to topologies in Figure 66 and Figure 67 at $f_{\mathrm{sw}} = 100\mathrm{kHz}$ and $D = 0.3$.

The FHA implies additional simplification: As only the first harmonic is used, other harmonics are ignored [89]. However, the FFT of the simulated inductor current, I_{i}, in Figure 69 shows that, especially at higher duty cycle, a significant amount of energy can be observed when the converter is operated at high and low duty cycles. If low and high duty cycles are used, the FHA will show a considerable deviation between model and reality, as shown in Figure 68. So current FHA analysis is inadequate when high or low duty cycles above resonance frequency should be used.

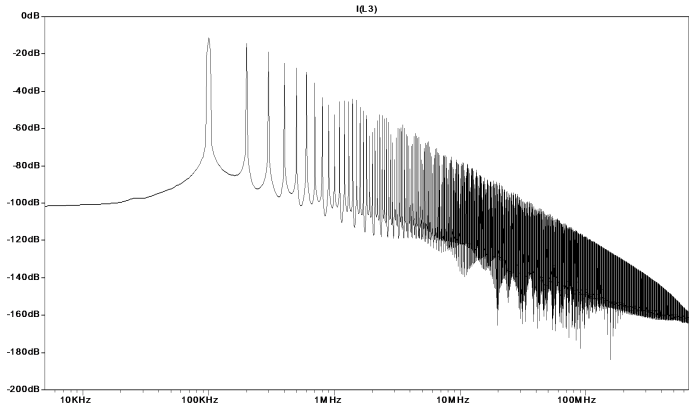


Figure 69: SLC inductor current FFT at $f_{\mathrm{sw}} = 100\mathrm{kHz}$ and $D = 0.3$.

7.5.4 Time domain analysis

Accurate SLC modeling requires a time domain analysis without inappropriate approximations. Several time domain analyses have been conducted so far [85, 86], in which a voltage-to-voltage converter

served as a model. However, no simple equations were given for the absolute output current. A simple analytically solvable open-loop output current equation is presented in this work for the first time. For accurate modeling, a linear time domain analysis for switching frequencies above the resonance frequency will be conducted in the next section. The output current of the SLC can be set, by adjusting the duty cycle and/or frequency.

Typically, an SLC converter will have sinusoidal inductor current. However, when a high enough operating frequency is used, the first Taylor approximation of a sinusoidal waveform can be used with acceptable error. The voltage change at the resonance capacitor should be minimal for an appropriate approximation. The change in the capacitor voltage U_{C1} can be calculated by using

$$\frac{d}{dt}U_{\mathrm{C1}} = \frac{I_i}{C_1} \tag{7.14}$$

Hence, C_1 should be chosen large. The subsequent modulation technique is based on an in-depth mathematical analysis of the topology. The dc output current, $\overline{I_{\mathrm{out}}}$, is averaged over the switching period, t_{p}, as an open-loop transfer function. The equations are then solved to obtain the duty cycle, D, and switching period, t_{p}, resulting in a function of the required current and the measured voltages. All waveforms required for the SLC converter are summarized in Figure 70.

7.5.5 Waveform description

The following section analyses the switching waveform over time.

The inductor current, I_{i}, of the SLC converter is shown in blue in Figure 70. The inductor current change can be described by the equation

$$\frac{d}{dt}I_{\mathrm{i}} = \frac{U_{\mathrm{Li}}}{L_{\mathrm{i}}} = \frac{U_{\mathrm{sw}} - U_{\mathrm{C1}} - U_{\mathrm{out}}}{L_{\mathrm{i}}} \tag{7.15}$$

The derivative of the inductor current is determined by three voltages: U_{sw}, U_{C1}, and U_{out} . U_{sw} is set by the duty cycle, as it can be seen in Figure 70a.

$$U_{\mathrm{sw}} = \begin{cases} U_{\mathrm{dc}} & 0 \leq t \leq t_{\mathrm{c}}D \\ 0 & t_{\mathrm{c}}D < t \leq t_{\mathrm{c}} \end{cases} \tag{7.16}$$

The output voltage polarity, U_{out}, is a function of the inductor current. The absolute magnitude is set by the output capacitor voltage, U_{Cout}. The mid-point bridge rectifier ensures a positive capacitor voltage. The output voltage sign U_{out} is determined by the inductor current I_{i}.

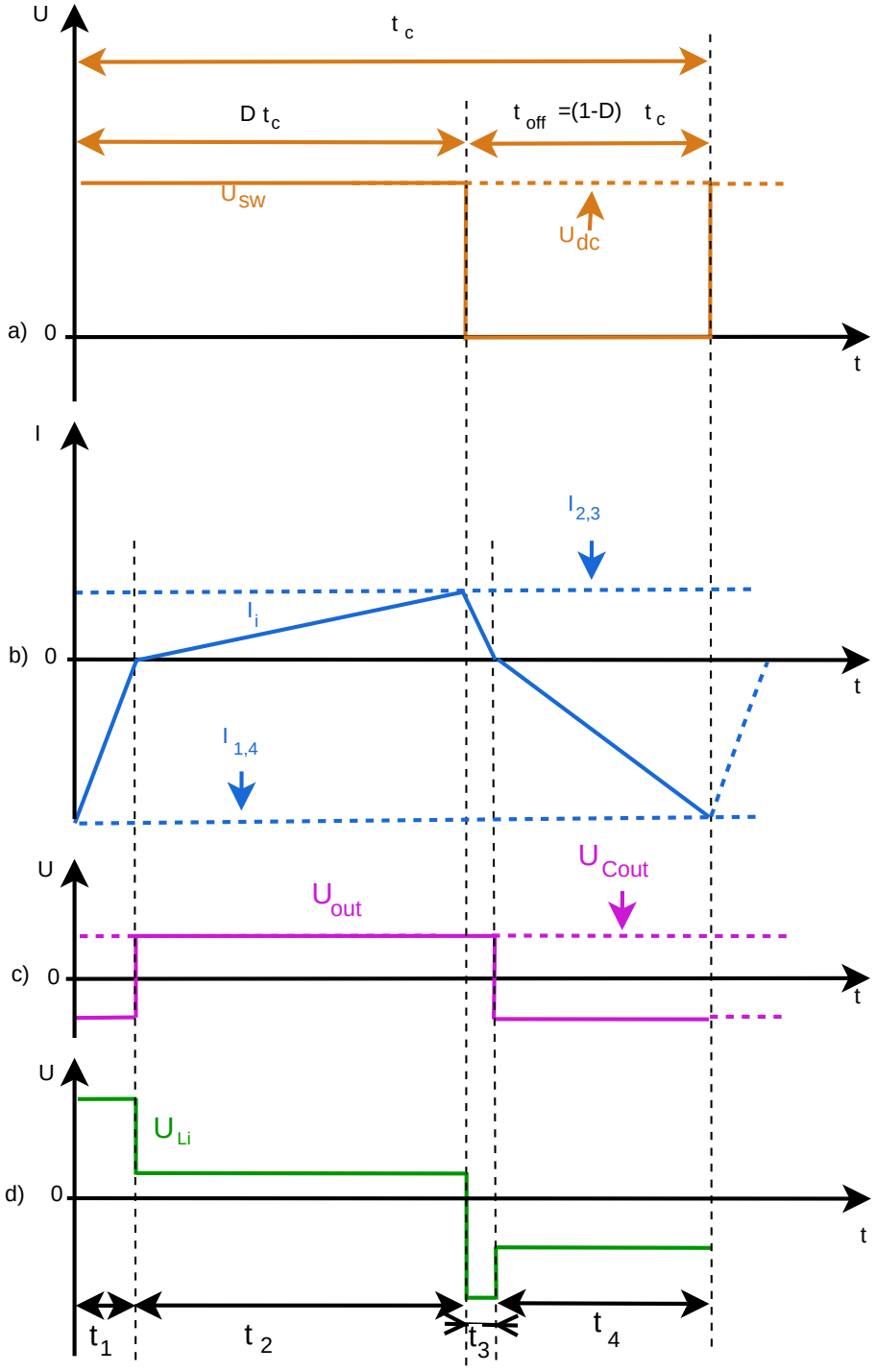


Figure 70: SLC converter switching waveform.

$$U_{\mathrm{out}} = U_{Cout}\, sign(I_i) \tag{7.17}$$

As U_{out} and U_{i} change polarity at different times, shown in Figure 70c and 70d, four different states $n \in [1, 2, 3, 4]$ have to be analyzed. The respective times are named t_n.

t_1 The switching voltage, $U_{\mathrm{sw}} = U_{\mathrm{dc}}$, is positive during t_1, while the output voltage, U_{out}, is negative. The inductor current, I_{i}, rises fast from a negative value to zero.

t_2 I_{i} is positive during t_2, thus U_{out} is positive and the current rises slowly according to (7.15).

t_3 When the switching voltage is zero, the capacitor provides a negative voltage. The inductor current, I_{i}, drops fast from a positive value towards zero.

t_4 I_{i} is negative in t_4, thus U_{out} is negative and and the current decreases slowly.

All values are summarized for the corresponding steps in Table 12. The values of $U_{\mathrm{out,n}}$ and $U_{\mathrm{sw,n}}$ are based on Figure 70.

7.5.6 Output current analysis

The average output current is calculated over the switching period interval. The interval $0 \leq t \leq t_{\mathrm{c}}$ is split into subsections, t_{n}. Zero time is moved to the beginning of each interval for the ease of calculation. The overall average can be expressed as follows:

$$\overline{I_{\mathrm{out}}} = \frac{1}{t_{\mathrm{c}}} \left(\int_{t=0}^{t=t_1} I_{\mathrm{n}=1}\,(t)\, dt + \int_{t=0}^{t=t_2} I_{n=2}\,(t)\, dt + \int_{t=0}^{t=t_3} I_{n=3}\,(t)\, dt + \int_{t=0}^{t=t_4} I_{n=4}\,(t)\, dt \right) \tag{7.18}$$

The momentary current in the inductor, L_{i}, can be calculated as:

$$I_{\mathrm{n}}\,(t) = s_{\mathrm{n}} \frac{U_{\mathrm{sw,n}} - U_{C1} - U_{\mathrm{out,n}}}{L_{\mathrm{i}}} t \tag{7.19}$$

Each contribution to the average output current within t_{n} can be calculated by this formula:

$$\int_{t=0}^{t=t_n} I_{\mathrm{n}}\,(t)\, dt = s_{\mathrm{n}} \frac{U_{\mathrm{sw,n}} - U_{C1} - U_{\mathrm{out,n}}}{2L_{\mathrm{i}}} t_n^2 \tag{7.20}$$

The specific values for t_n, $U_{\mathrm{out,n}}$, $U_{\mathrm{sw,n}}$ can be derived from Figure 70. The sign s_{n} is chosen to fulfill (7.21). All values are summarized in Table 12. The values of $U_{\mathrm{out,n}}$ and $U_{\mathrm{sw,n}}$ are based on Figure 70.

$$\int_{t=0}^{t=t_n} I_{\mathrm{n}}\left(t\right) dt \geqq 0 \tag{7.21}$$

Time step	Output voltage polarity	Switchnode voltage	Polarity
t_{n}	$U_{\mathrm{out,n}}$	$U_{\mathrm{sw,n}}$	s_{n}
t_1	$-U_{\mathrm{Cout}}$	U_{dc}	$+1$
t_2	$+U_{\mathrm{Cout}}$	U_{dc}	$+1$
t_3	$+U_{\mathrm{Cout}}$	0	-1
t_4	$-U_{\mathrm{Cout}}$	0	-1

Table 12: Variables for each time step, t_{n}.

7.5.7 Timing analysis

The average output current, $\overline{I_{\mathrm{out}}}$, on the secondary side is calculated by using (7.18), (7.19) and the parameters of Table 12. As a 1:1 transformer ratio is assumed in Figure 66, primary side and secondary side currents are equal.

The timing equations (7.22) and (7.23) can be formulated [72] based on Figure 70a:

$$t_1 + t_2 = Dt_{\mathrm{c}} \tag{7.22}$$

$$t_3 + t_4 = \left(1 - D\right) t_c \tag{7.23}$$

The voltage relations (7.25, 7.26) are based on (7.19) and the continuity property (7.24) of the inductor current shown in Figure 70b at the interval borders.

$$lim_{t \to t_n^+}(I_i\left(t\right)) = lim_{t \to t_n^-}(I_i\left(t\right)) \tag{7.24}$$

$$\frac{U_{\mathrm{dc}} - U_{C1} + U_{\mathrm{Cout}}}{U_{\mathrm{C1}} - U_{\mathrm{Cout}}} = \frac{t_4}{t_1} \tag{7.25}$$

$$\frac{U_{\mathrm{dc}} - U_{C1} - U_{\mathrm{Cout}}}{U_{\mathrm{C1}} + U_{\mathrm{Cout}}} = \frac{t_3}{t_2} \tag{7.26}$$

The times t_{n} can be calculated by using (7.22) - (7.26):

$$t_1 = \frac{(+U_{\mathrm{C1}} - U_{\mathrm{Cout}})\,(U_{\mathrm{Cout}} - DU_{\mathrm{dc}} + U_{C1})}{2U_{\mathrm{dc}}U_{\mathrm{Cout}}} t_{\mathrm{c}} \tag{7.27}$$

$$t_2 = \frac{(+U_{\mathrm{C1}} + U_{\mathrm{Cout}})\,(U_{\mathrm{Cout}} + DU_{\mathrm{dc}} - U_{C1})}{2U_{\mathrm{dc}}U_{\mathrm{Cout}}} t_{\mathrm{c}} \tag{7.28}$$

$$t_3 = \frac{(-U_{\mathrm{Cout}} + U_{\mathrm{dc}} - U_{\mathrm{C1}})\,(U_{\mathrm{Cout}} + DU_{\mathrm{dc}} - U_{\mathrm{C1}})}{2U_{\mathrm{dc}}U_{\mathrm{Cout}}} t_{\mathrm{c}} \tag{7.29}$$

$$t_4 = \frac{(+U_{\mathrm{Cout}} + U_{dc} - U_{\mathrm{C1}})\,(U_{\mathrm{Cout}} - DU_{\mathrm{dc}} + U_{\mathrm{C1}})}{2U_{\mathrm{dc}}U_{\mathrm{Cout}}} t_{\mathrm{c}} \tag{7.30}$$

Capacitor voltage estimation The average voltage of the dc blocking capacitor, C_1, is directly proportional to the duty cycle, D, for steady-state conditions, as the inductor acts shortened at low frequencies. Equation (7.31) allows the previous timing equations to be simplified greatly.

$$U_{\mathrm{C1}} = DU_{\mathrm{dc}} \tag{7.31}$$

This results in:

$$t_1 = \frac{DU_{\mathrm{dc}} - U_{\mathrm{Cout}}}{2U_{\mathrm{dc}}} t_c \tag{7.32}$$

$$t_2 = \frac{DU_{\mathrm{dc}} + U_{\mathrm{Cout}}}{2U_{\mathrm{dc}}} t_{\mathrm{c}} \tag{7.33}$$

$$t_3 = \frac{(1-D)\,U_{\mathrm{dc}} - U_{\mathrm{Cout}}}{2U_{\mathrm{dc}}} t_{\mathrm{c}} \tag{7.34}$$

$$t_4 = \frac{(1-D)\,U_{\mathrm{dc}} + U_{\mathrm{Cout}}}{2U_{\mathrm{dc}}} t_c \tag{7.35}$$

Output current formula The average output current formula is formulated based on (7.18), (7.20), Table 12 and the timings according to (7.32) - (7.35).

$$\boxed{\overline{I_{\mathrm{out}}} = \frac{D\,(1-D)\,U_{\mathrm{dc}}^2 - U_{\mathrm{Cout}}^2}{4L_{\mathrm{i}}U_{\mathrm{dc}}} t_{\mathrm{c}}} \tag{7.36}$$

The controller requires for the calculation two additional quasi-constant voltages. Hence, the following voltages must to be measured continuously by the controller to set the average output current:

The dc link voltage, U_{dc}, and output voltage, U_{Cout}. The output current can never be reduced to zero as the switching frequency would have to be infinite. This is the first time that the dependency on frequency and duty cycle is formulated for the SLC by one equation.

7.6 Summary

For the boost converter, operating as a power factor correction, and the series LC converter average input- and output currents were formulated. Both share the duty cycle D and the period t_{c}. The PFC and SLC equations will be used in the control section 8 to set the input- and output current at the same time.

8 Control System Design

The SLC/PFC control system is responsible for a graceful and stable converter operation. First an overview over the control topology is given. Next, each individual control section next discussed in detail.

8.1 Overview

An overview over the converter structure is given in Figure 71 on page 111. From the PFC/SLC analysis in section 7, more specific, equation (7.10) and (7.36), it is obvious that several measurement values are required. For regulation several measurement values are first filtered, i.e. the output current I_{out} or the grid voltage U_{grid}, are low pass filtered with hardware and software. The low pass filter is shown on the left hand side in Figure 71. This is required to reduce the measurement noise. For non-sinusoidal waveform sinc-averaging, for sinusoidal waveforms resonant observers are used. The corresponding filters are depicted in Figure 71.

A slow integrating regulator is utilized (see Figure 71) to set the average output current. The grid voltage is filtered in resonant observers, to determine the grid amplitude. It is shown as 'Primary Power Estimator' in Figure 71. To determine the primary side input power, the power consumed at the secondary side is estimated. To maintain DC-Link stability, the power balance over one period should be zero. Based on the calculated power and measured grid amplitude, the input conductance is calculated.

The central part of the converter is the to be developed D-tc separator in Figure 71 in gray. Based on both major set-values, input conductance and output conductance, the D-tc separator calculates the duty cycle D and the switching period t_{c}, which is then passed to the PWM modulator. The PWM modulator adjusts the duty cycle polarity depending on the grid voltage polarity. The modulator generates a dual channel PWM waveform for a half bridge, low side and high side respectively. It drives the PFC/SLC converter, which is performing the actual power conversion.

8.2 D-tc separator

The D-tc separator calculates the duty cycle D and switching period t_{c} based on the grid input conductance and the DC output current.

For its calculation additional measurement values, U_{ac}, U_{dc} and U_{Cout} are required. The calculation is based on (7.10) and (7.36). Both set values g_{ac} and $\overline{I_{\mathrm{out}}}$ depend on the actuating variables t_{c} and D. So, in theory, two variables can be set at the same time. To calculate the two actuating variables, a separator is developed in this section.

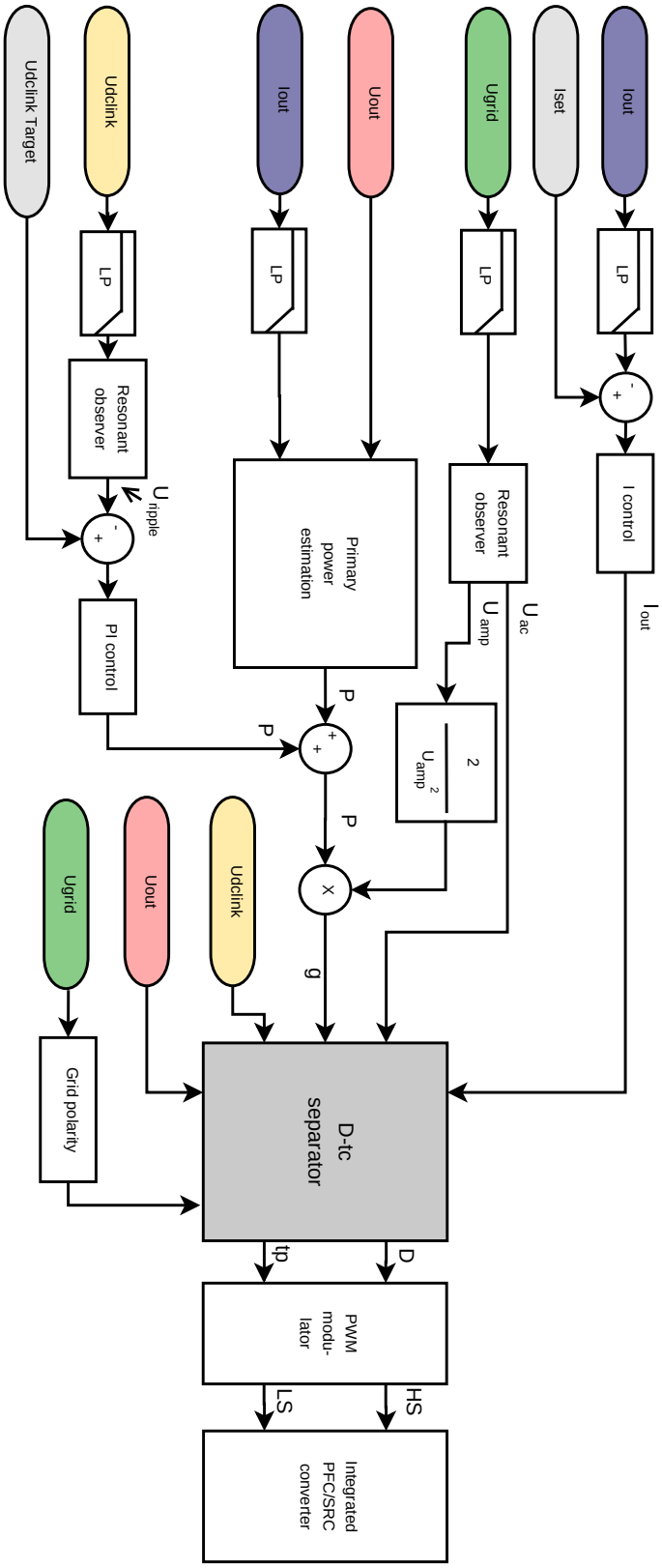


Figure 71: The converter control structure is shown in an overview. For a detailed description please refer to the description in the overview section.

For a simplified calculation a substitution of (7.10) is done:

$$\overline{I_{\mathrm{ac}}} = m_{\mathrm{ac,I}} t_{\mathrm{p}} D^2 \tag{8.1}$$

$$m_{\mathrm{ac,I}} = \frac{U_{\mathrm{dc}} U_{\mathrm{ac}}}{2L_b \left(U_{\mathrm{dc}} - U_{\mathrm{ac}}\right)} \tag{8.2}$$

The PFC is modeled as a constant conductance over one switching period t_{c}. Again a substitution is used:

$$g_{\mathrm{in}} = m_{\mathrm{ac,g}} t_{\mathrm{p}} D^2 \tag{8.3}$$

As the DC link voltage of a PFC is always higher than the maximum ac voltage, $m_{\mathrm{ac},g}$ is always positive. $m_{\mathrm{ac,g}}$ equals to:

$$m_{\mathrm{ac,g}} = \frac{U_{\mathrm{dc}}}{2L_b \left(U_{\mathrm{dc}} - U_{\mathrm{ac}}\right)} > 0 \tag{8.4}$$

The output current equation (7.36) is written as:

$$\overline{I_{\mathrm{out}}} = m_{\mathrm{dc}} D \left(1 - D\right) t_{\mathrm{p}} + k_{\mathrm{dc}} t_{\mathrm{p}} \tag{8.5}$$

where m_{dc} is equal to:

$$m_{\mathrm{dc}} = \frac{U_{\mathrm{dc}}}{4L_i} > 0 \tag{8.6}$$

and k_{dc}, the influence of the output voltage, equals to:

$$k_{\mathrm{dc}} = \frac{-U_{\mathrm{out}}^2}{4L_{\mathrm{i}} U_{\mathrm{dc}}} \leq 0 \tag{8.7}$$

Based on (8.3) and (8.5) the duty cycle can be calculated:

$$D\left(1 - D\right) + \underbrace{\frac{k_{\mathrm{dc}}}{m_{\mathrm{dc}}}}_{-K} - \underbrace{\frac{m_{\mathrm{ac,g}} I_{\mathrm{out}}}{g_{\mathrm{in}} m_{\mathrm{dc}}}}_{m} D^2 = 0 \tag{8.8}$$

The duty cycle can be calculated to:

$$2D_{1,2} = \frac{1}{m+1} \pm \sqrt{\frac{1 - 4K\left(m+1\right)}{\left(m+1\right)^2}} \tag{8.9}$$

As $m + 1 \geq 0$, also the solution with the minus returns a positive duty cycle. Equation (8.9) is

back-substituted to:

$$\boxed{D_{1,2} = \frac{\pm\sqrt{g_{in}^2 m_{dc}^2 + 4g_{\mathrm{in}}^2 k_{\mathrm{dc}} m_{\mathrm{dc}} + 4g_{\mathrm{in}} I_{\mathrm{out}} k_{\mathrm{dc}} m_{\mathrm{ac,g}}} + g_{\mathrm{in}} m_{dc}}{2\left(g_{\mathrm{in}} m_{\mathrm{dc}} + I_{\mathrm{out}} m_{\mathrm{ac.g}}\right)}} \tag{8.10}$$

Theoretically both solutions could be used. However in this design only the more positive sign solution was used for the experiments. For a safe operation of the SLC the duty cycle is limited between 0.1 and 0.9. This means the following condition must hold true. The limit was set empirically.

$$0.1 \leq D \leq 0.9 \tag{8.11}$$

In case a limiting condition is applied, only one set-value can be maintained. Therefore, a decision must be made, which parameter has to be maintained and which must be compromised: The AC input current or the DC output current. For a typical power supply maintaining the output current $\overline{I_{\mathrm{out}}}$ is more important than to achieve the ideal input current. Therefore, typically equation (8.13) is used.

$$t_{\mathrm{p}} = \frac{\overline{I_{\mathrm{ac}}}}{m_{\mathrm{ac,I}} D^2} \tag{8.12}$$

$$\boxed{t_{\mathrm{p}} = \frac{\overline{I_{\mathrm{out}}}}{k_{\mathrm{dc}} + (D - D^2) m_{dc}}} \tag{8.13}$$

The analytic D-tc separator calculates the D-tc values for every switching cycle. This means that both $\overline{I_{\mathrm{out}}}$ or $\overline{I_{\mathrm{ac}}}$ can be set using the switching period t_{p} and the duty cycle D, allowing for fast control. However, at the same time a significant amount of calculus is required.

8.3 Duty Cycle polarity

According to Figure 71, the half bridge must adjust its duty cycle (D) according to the input voltage polarity [83]. This is explained in detail in section 7.4. An instant duty cycle change causes a significant peak current and the over-current detection is triggered. In order to prevent this triggering, an algorithm for smoothing the transition is presented.

8.3.1 Theory

The reason for overcurrent during polarity inversion is due to the potential change in the capacitor C_1 of the series LC converter. The theory is explained in the following section.

The capacitor current I_{c} can be calculated by the following equation:

$$I_{\mathrm{c}} = C_1 \frac{\mathrm{d}}{\mathrm{dt}} U_{\mathrm{c}} \tag{8.14}$$

As previously mentioned, the static capacitor voltage can be estimated to:

$$U_{\mathrm{c}} = D U_{\mathrm{dc}} \tag{8.15}$$

Thus, the displacement current can be calculated as follows:

$$I_{\mathrm{c}} = U_{\mathrm{c}} C_1 \frac{\mathrm{d}}{\mathrm{dt}} D \tag{8.16}$$

Hence, peak currents can be limited by applying a transition period. Therefore, the maximum allowable duty cycle step size is limited.

8.3.2 Software implementation

The transition period implementation is implemented using a counter c_{nt}, that has a positive and negative limit, $-s_{\max}$ and $s_{\max}$. The effective duty cycle, D_{eff}, is calculated according to the following formula:

$$D_{\mathrm{eff}} = 0.5 - (0.5 - D) \left(\frac{c_{nt}}{s_{\max}} \right) \tag{8.17}$$

The effective duty cycle determination algorithm, shown in Figure 72, is executed for each grid voltage (U_{ac}) measurement. First, the grid voltage U_{ac} is compared against a fixed control voltage U_{ctr}. If its lower than the control voltage, the maximum count variable is checked for a negative limiting number $s_{\max}$. If the limit is not yet reached, the count variable is decremented. This is indicated by '$c_{\mathrm{nt}} - -$' and next the duty cycle is updated. If the negative limit $-s_{\max}$ is reached, no duty cycle update is required. The same procedure applies for the negative grid voltage respectively. In this case a positive limit applies and the count variable is increased. This is indicated by '$c_{\mathrm{nt}} + +$'.

In case the grid voltage is in-between the control voltage, U_{ctr}, the voltage is centered around zero and the duty cycle is updated. The algorithm must be computational efficient, as it is executed for every ADC sample. Therefore, this section is highly optimized for execution speed.

8.3.3 Output current error during transition period

During the transition period, the D-tc separator's generated duty cycle is intentionally overwritten by the duty cycle ac polarity adjustment. This means that the SLC/PFC converters input and output currents are distorted.

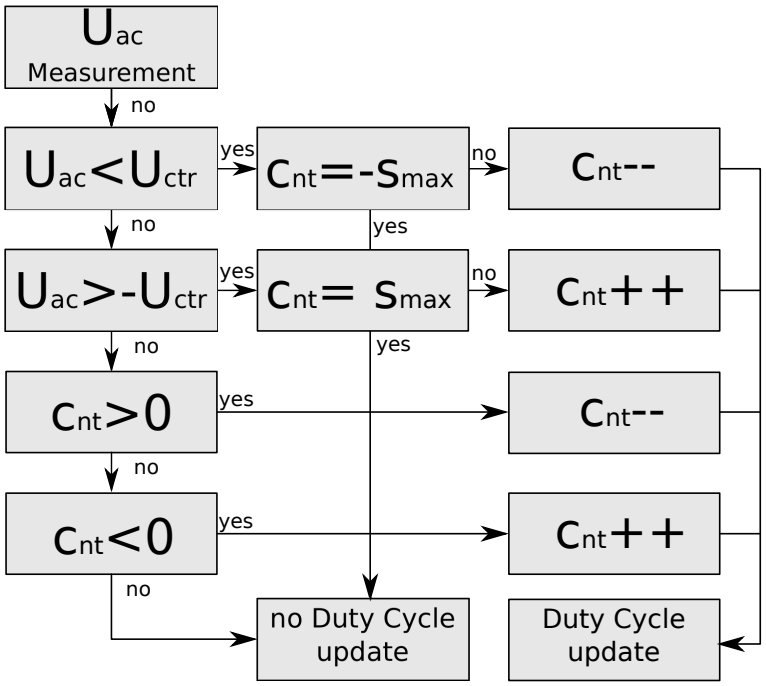


Figure 72: Determination algorithm for the grid voltage polarity, represented in the count variable c_{nt}.

To minimize the occurring error, the transition period should be chosen as small as possible. The error of the input power is insignificant as the AC voltage U_{ac} is low. However, the LED output current may be distorted. The change in U_{C1} may further lead to erratic output current.

8.4 DC-Link Balancing

The DC-Link balancer ensures that the desired average dc voltage U_{dc} is maintained. It is shown in Figure 73 and is a subset of Figure 71. From an energy standpoint, the bridge-less totem-pole PFC stage supplies energy to the DC-Link. The SLC converter demands energy from the DC-Link. To maintain a stable voltage the PFC has to deliver the same average power as the SLC converter consumes. To compensate for losses and inaccuracies, a PI regulator is used.

First the DC Link voltage U_{dc}, the output voltage U_{out} and the grid voltage U_{ac} are measured. Resonant observers, described in section 9.7, are used to remove the double mains frequency content of the DC Link and to measure the grid amplitude U_{amp}. The PFC requires this ripple for maintaining a sinusoidal input current

The previously explained control mechanism visualized in Figure 73. The load estimator (LE) calculates the secondary side load, by the measurement values of U_{out} and I_{out} . This equals power consumed by the load.

$$P_{\mathrm{LE}} = U_{\mathrm{out}} I_{\mathrm{out}} \tag{8.18}$$

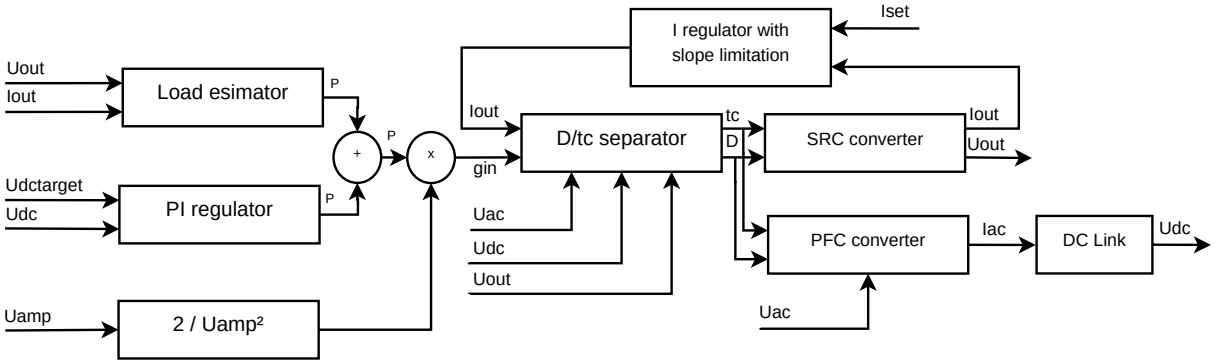


Figure 73: The D-tc separator obtains the input conductance g_{in} from a load estimator and a PI regulator. The DC output current I_{out} is measured on the secondary side and offsets are corrected with an I regulator.

The PI regulator is used to balance the DC link to the desired target value, U_{dctarget}. It calculates the power required to balance the DC link according to the following formula:

$$P_{PI} = U_{dc}(k_{\mathrm{p}}(U_{dc} - U_{\mathrm{dctarget}}) + k_i \int_0^t (U_{dc} - U_{dctarget})dt) \tag{8.19}$$

Both powers are added and the input conductance g_{in} is calculated using (8.20). The measurement of U_{ac} is discussed in section 9.7. The factor of two is required, as the peak power is two times the average power in a sinusoidal AC system.

$$g_{\mathrm{in}} = \frac{2\,(P_{\mathrm{LE}} + P_{\mathrm{PI}})}{U_{\mathrm{amp}}^2} \tag{8.20}$$

The secondary side output current is regulated by a slow I regulator with slope limit and anti-windup. This regulator adds additional accuracy and compensates for errors.

Both set-values, g_{in} and I_{out}, are passed to the D-tc separator (section 8.2). The separator returns the switching period t_{c} and D, which is passed to the half bridge PWM waveform generator.

9 Data Acquisition

Clean measurement values are required for an accurate jitter-free control. The following section discusses state-of-the-art analog-to-digital converter (ADC) driver circuits that are used for accurate measurements. Further, hardware and software implementations are discussed to reduce the noise passed to the control.

9.1 ADC Driver Circuits

Analog to Digital converters (ADCs) convert, as their name implies, an analog value to a digital value. While several ADC technologies are possible, this work will focus on the utilized sample and reset ADC (SAR-ADC). Sample and Reset ADCs have a sample capacitor, which is initially charged with sample voltage. Then, charges are added and removed in a switching pattern. A comparator then compares the resulting voltage to a reference value.

For a voltage measurement the ADC sample capacitor has to be charged. Therefore, the sample and reset ADC requires input voltage drivers so that an accurate and fast data acquisition can be achieved. Mostly such ADC drivers are implemented by means of operational amplifiers. The ADC is typically integrated in the MCU, however, also a separate ADC may be used. First, the ADC equivalent circuit is discussed and developed. Based on the equivalent circuit, the ADC driver is built, that ensures accurate measurements.

9.1.1 ADC Equivalent Circuit

A sample and reset analog to digital conversion works by sampling the signal voltage U_{sig} to a sample capacitor C_{S}. For sampling, S1 in Figure 74 is closed. After the sampling time has passed it is opened again. Then, charge is added or removed to the capacitor. In each step it is compared to a reference voltage [113, p. 241]. Therefore, the equivalent sampling circuit for an analog to digital converter can be described as a capacitive load that is connected for a sampling time t_{sample}.

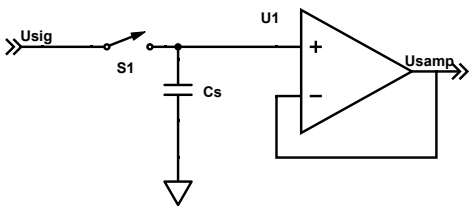


Figure 74: The equivalent input of an ADC sampling circuit. When the switch is closed, the voltage is sampled. When the switch is opened, the signal is on hold.

To start the conversion, the ADC closes S1 for sampling. The sampling capacitor is charged. After

the sampling time has passed, it opens again. If the source impedance is high, a long sampling interval is required. Obviously, this increases the total conversion time. Thus, techniques for reducing the sample time are developed subsequently.

9.1.2 Bypass Capacitors with infinite source resistance

To bypass the high source impedance of Figure 74, an additional capacitor is added, as shown in the Figure 75.

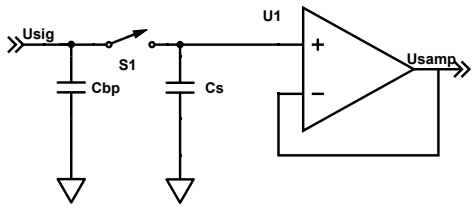


Figure 75: An additional bypass capacitor delivers the peak current required for charging the sampling capacitor.

The bypass capacitor during the sampling is calculated based on the principle that the error should be lower than the least significant bit. Further its assumed that the source impedance is indefinitely large. This means, according to the model, an additional sample time would not increase the measurement accuracy, which is not true in practice. Therefore, this calculation must be considered as a rough estimate.

The sample capacitance of the ADC converter can typically be found in the datasheet of the corresponding ADC converter. The following paragraphs develops an equation for calculating the bypass capacitor C_{bp} of Figure 75. The equivalent circuit in Figure 75 forms a capacitive voltage divider:

$$\frac{U_{\mathrm{error}}}{U_{ADC}} = \frac{C_{\mathrm{S}}}{C_{\mathrm{bp}} + C_{\mathrm{S}}} \tag{9.1}$$

Based on the requirement that the error should be half the least significant bit (1/2 LSB) the following equation can be formulated. The variable b represents the number ADC resolution measured in number of bits.

$$\frac{U_{\mathrm{error}}}{U_{ADC}} = 2^{b+1} \tag{9.2}$$

$$C_{\mathrm{bp}} \geq C_{\mathrm{S}} \left(2^{b+1} - 1\right) \tag{9.3}$$

Typically, the resulting capacitor value is relatively high. In case a lower bypass capacitor value is required, the source impedance can be considered in the calculation. An approach for lowering the

source impedance is presented in the next section.

9.1.3 Bypass Capacitors with finite source resistance

As the previous calculation did not consider the sampling time and the source resistance R. This results in large bypass capacitor values. As above, the design requirement is that the error must be smaller than half LSB.

The required sampling capacitor C_{bp} must be chosen to fulfill the following inequation:

$$\frac{C_{\mathrm{s}}}{C_{\mathrm{bp}} + C_{\mathrm{s}}} e^{-\frac{t}{RC_{\mathrm{bp}}}} \leq 2^{-b-1} \tag{9.4}$$

To reduce the source resistance, an operational amplifier configured as an impedance converter can be used.

9.1.4 High Voltage Measurements

For measuring higher voltages, a voltage divider is added. In the following section, two possible approaches are presented.

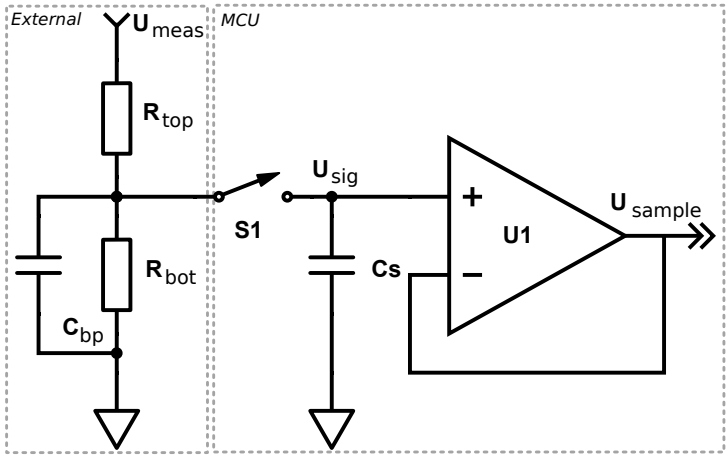


Figure 76: Direct drive of ADC using a resistive divider.

Direct Source Drive The converter is directly connected to the source, as shown in Figure 76. This is a simple and straight-forward solution for reducing source impedance. To be able to supply the energy to C_{s}, a stabilizing capacitor C_{bp} is added. If the source impedance R_{src} is high, the bandwidth of the converter is limited. The source impedance of a voltage divider can be calculated using the AC model and connecting all stable sources to ground.

$$R_{\mathrm{src}} = R_{\mathrm{top}} || R_{\mathrm{bot}} = \frac{R_{\mathrm{bot}} R_{\mathrm{top}}}{R_{\mathrm{top}} + R_{\mathrm{bot}}} \tag{9.5}$$

In case one of the resistors is significantly lower, only the lower value resistor may be considered as an approximation. Assuming the bottom resistor R_{bot} is significantly lower than the the top resistor R_{top}, the source resistance may be approximated by the following formula:

$$R_{\mathrm{src}} \approx R_{\mathrm{bot}} \tag{9.6}$$

The effective bandwidth is calculated by (9.7). In case the bandwidth limitations of the previous converter cannot be met, the resistance could be decreased. However, this would increase power losses, especially if a high voltage DC rail should be measured. Therefore, an alternative solution is proposed.

Impedance Converter The effective input resistance can be decreased by using an impedance converter. In Figure 77, the high source impedance of the voltage divider is converted to a low source impedance by an operational amplifier configured as an impedance converter. As the input resistance of the ADC is significantly decreased, its bandwidth is increased. Some operational amplifiers may have stability problems when driving capacitive loads. Hence, resistor R_{op} is placed for oscillation damping. The damping resistor, if required, is specified in the operational amplifiers datasheet.

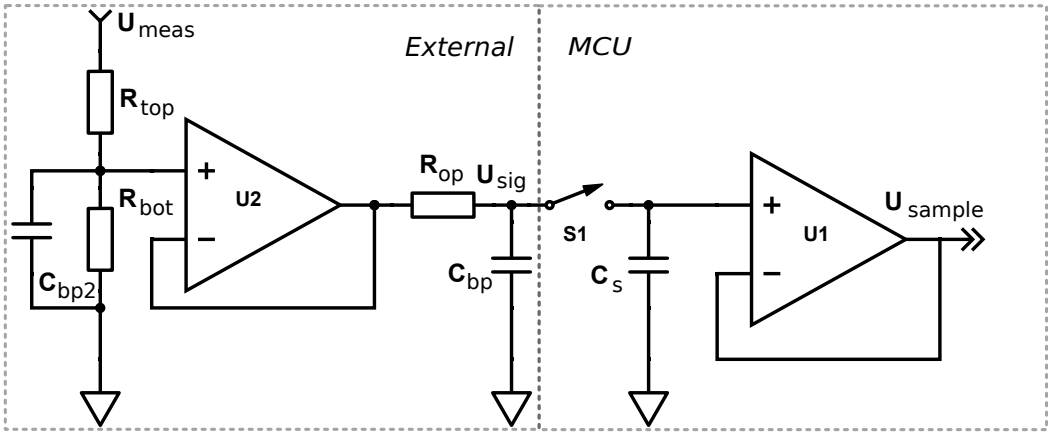


Figure 77: The ADC is driven by an operational amplifier that is configured as an impedance converter. By having a cascaded RC filter a second order low pass filter is implemented.

Operational amplifier error The operational preamplifier (U2, Figure 77) decreases the source resistance. However, it may introduce an error, changing the measurement value. The most common errors are:

- Offset: A constant offset is added to the output voltage. A typical value is 5 mV, however, state of the art amplifiers can go to sub 5 µV [114].
- Input Bias-Current may load the amplifiers resistor network. When a CMOS operational amplifier

is used, this error is typically insignificant [114].

- Bandwidth limitations: If a high speed signal should be measured, the operational amplifier must have the correct available bandwidth.

Bandwidth calculus The 3dB bandwidth f_{bw} of the ADC can be calculated using the first order low pass filter formula:

$$f_{\mathrm{bw}} = \frac{1}{2\pi R_{\mathrm{src}} C_{\mathrm{bp}}} \tag{9.7}$$

In case a high voltage should be measured, a high resistance must be used for energy efficiency. Assuming a source impedance of $R_{\mathrm{src}} = 1\,\mathrm{M\Omega}$, and a bypass capacitor of 10 nF, a bandwidth of approximately 16 Hz is present. Therefore, for general applications, it is recommended to use an impedance converter.

9.1.5 Bandwidth Considerations

The measurement of single ended signals is typically implemented by a resistive voltage divider, as shown in Figure 76 and 77. The white noise of resistors can be calculated using the following formula:

$$v_{\mathrm{n}} = \sqrt{4 k_{\mathrm{b}} T\, R\, \Delta f} \tag{9.8}$$

Assuming no bandwidth limitation, meaning $f \to \infty$, the noise voltage would also be infinite. However, this assumption is not valid in practice, as the parasitic elements, especially capacitors limit the bandwidth.

To have a minimal noise, the capacitor C_{bp} should be chosen according to (9.7) so that the signal component with the maximum available frequency can be measured, while noise influences can be reduced.

9.2 Nyquist Sampling Theorem

According to the Nyquist-Theorem, the sampling frequency must be at least two times the frequency bandwidth of the signal[10, p. 68ff]. This can be expressed by the following formula:

$$f_{\mathrm{sample}} \geq 2\, f_{\mathrm{bw}} \tag{9.9}$$

In case the signal contains higher frequency content, this frequency spectrum must be attenuated to meet the nyquist criteria. This so called anti-aliasing filter is implemented based on the previous

bandwidth limitation circuit, as it can be seen in Figure 77.

The signal contents of an exemplary waveform is shown in the frequency domain in Figure 78. The bandwidth in a typical application is from zero to the bandwidth frequency f_{bw}. For converted signals above half the sampling frequency, $f_{\mathrm{sample}}/2$, aliasing noise occurs. This noise can be avoided by previously filtering the sampled signal by means of an anti-aliasing filter. If the sampling frequency is chosen double the bandwidth, an infinite steep filter, a so called brick-wall-filter, would be required. As real input filters can only have a finite slope, the sampling frequency must be chosen higher than $2\,f_{\mathrm{bw}}$. For practical applications a significantly higher factor is recommended.

Next, an example for designing an anti-aliasing filter is given. If a ten times higher frequency signal than the configured bandwidth would be present at the input, the ideal anti-aliasing filter should reduce this amplitude to zero. Let's assume, the circuit uses a first order low pass filter. It has an attenuation of 20 dB/decade. Hence, the signal aliasing amplitude is reduced to 10%. This means that a first order low pass filter may have a too little attenuation for the presented signal. If instead a second order low pass filter would be used, the signal aliasing amplitude would be reduced down to 1%. Hence, for this converter at least a second order low pass filter should be used.

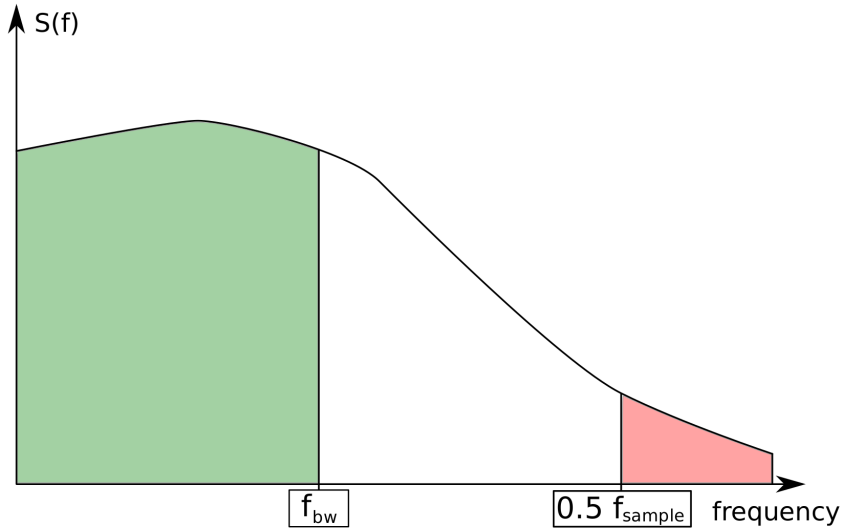


Figure 78: An arbitrary signal over the sampling frequency, based on [10, p. 70], is depicted. The green area is the signal part, the red area would introduce anti-aliasing noise. Hence, for a good reproduction a filter has to be designed that attenuates this aliasing noise.

In practical design considerations, the sampling frequency should be as high as possible, as it can be used for averaging, resulting in noise reduction. However, the obtained samples have to be processed in the MCU. Therefore, the sampling frequency should be chosen with respect to the processing power of the computational logic.

9.3 Current Measurement circuits

Special loads, like for example LEDs, are required to be driven current controlled. Therefore, the converter output current must be directly measured. The following section explains the current measurement circuits used.

Currents can be unipolar or bipolar. Unipolar currents are measured in only one direction, in our case only in the positive direction. Bipolar measurements can measure in both, negative and positive current directions.

9.3.1 Unipolar current measurement

Some currents, e.g. the LED load current, have only a positive sign. Those currents measurements are designated unipolar current measurements. The current is measured by a shunt resistor. The power dissipation in a shunt resistor can be calculated by the following formula:

$$P_{\mathrm{shunt}} = R_{\mathrm{shunt}} I_{\mathrm{m}}^2 \tag{9.10}$$

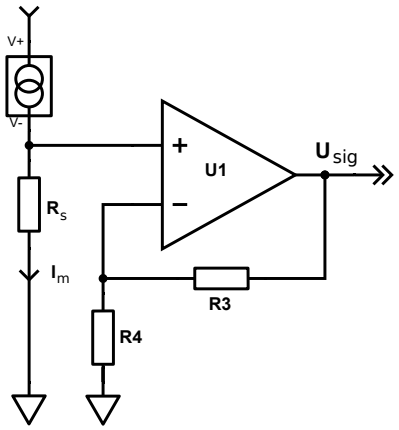


Figure 79: Standard op-amp current shunt amplifier without offset generation.

To minimize losses, a low shunt resistor value should be used. Therefore, a non-inverting amplifier configuration, as shown in Figure 79 is used. However, a negative operational amplifier offset in U1 may lead to the inability of measuring low currents. Therefore, a special circuit may be implemented, as shown in Figure 80, that adds an offset to the measurement value. Before the converter is started, zero current flows through the output shunt resistor R_{S}. This can be used to calibrate the current measurement.

Calculation procedure The following section covers the calculation procedure of the current measurement circuit shown in Figure 80.

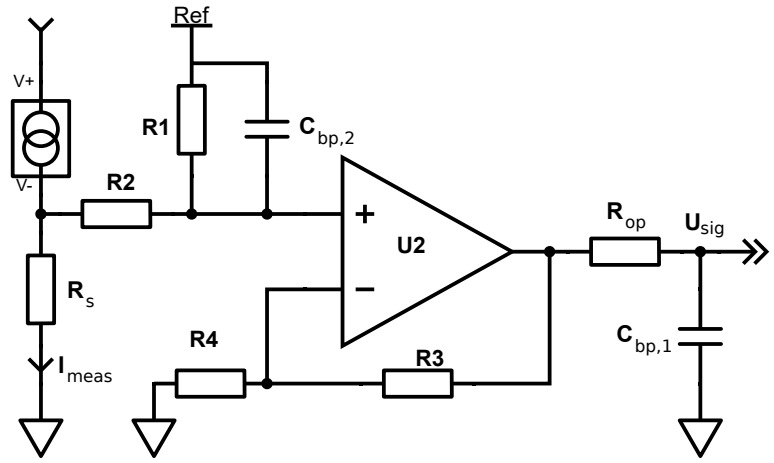


Figure 80: The operational amplifier circuit adds an offset to the sensed current. This allows to measure low currents, where the voltage drop over the sense resistor is below the operational amplifiers offset voltage.

The voltage at the current shunt can be calculated using Ohms law:

$$U_{\mathrm{S}} = R_{\mathrm{S}} I_{\mathrm{meas}} \tag{9.11}$$

The gain of the operational amplifier can be calculated using the non-inverting operational amplifiers formula:

$$G_{\mathrm{op}} = \left(1 + \frac{R_3}{R_4}\right) \tag{9.12}$$

The gain of the resistor network can be calculated using the voltage divider formula:

$$G_{\mathrm{vd}} = \left(\frac{R_1}{R_1 + R_2}\right) \tag{9.13}$$

Therefore, the overall gain can be calculated:

$$G = G_{\mathrm{op}} G_{\mathrm{vd}} = \left(1 + \frac{R_3}{R_4}\right)\left(\frac{R_1}{R_1 + R_2}\right) \tag{9.14}$$

R_1 and R_2 should be chosen so that the voltage divider voltage is larger than the maximal offset voltage U_{OS}. The R_1 / R_2 biasing voltage divider reduces the effective gain. It must be compensated by choosing G_{op} higher.

9.3.2 Bipolar current measurement

As previously discoussed, a bipolar current measurement can measure positive and negative currents. The bipolar current measurement can be implemented using the circuit shown in Figure 80. However,

in contrast to the unipolar current measurements, the resistances must be chosen differently. The R_1/R_2 biasing voltage divider is chosen so that the zero current voltage is half the reference voltage.

$$U_{\mathrm{ref}} \left(\frac{R_2}{R_1 + R_2} \right) \left(1 + \frac{R_3}{R_4} \right) = \frac{U_{\mathrm{ref}}}{2} \tag{9.15}$$

The gain of the operational amplifier can be described by the same formula as for the unipolar current measurement (9.14). Based on the equations, for the relation R_1/R_2 and R_3/R_4 results:

$$\frac{R_1}{R_2} = 2G \tag{9.16}$$

$$\frac{R_3}{R_4} = G - \frac{1}{2} \tag{9.17}$$

Application This circuit is used for measuring the primary side transformer current in the SLC inductor, addressed as I_i in Figure 70 on page 105. Despite the inductor current is not used for regulation, it will be used for overcurrent detection of the SLC converter.

9.4 Quasi Isolated Bipolar Differential Voltage Measurements

Some signals may not be referenced to the signal ground, for example the AC voltage of the grid. It is referenced to a floating offset voltage. Quasi-isolation is achieved by using high value resistors.

The differential high voltage signal can be measured with the circuit shown in Figure 81. The circuit consists of an AC voltage that is divided down by two voltage dividers. The negative voltage divider, on the left, consists of R_{top} and R_{bot}. $C_{\mathrm{bw},1}$ is used to limit the bandwidth of the converter. The second voltage divider, consists also of R_{top} and R_{bot}. In contrast to the negative voltage divider, the positive voltage divider has a split bottom resistor (R_{bot}), generating the reference voltage. One resistor is connected to GND, the other resistor is connected to U_{ref}. By this, a zero voltage offset of $U_{\mathrm{ref}}/2$ is generated.

This circuit shown in Figure 81 can be susceptible to noise caused by an offset voltage U_{off} transient. This high voltage transient propagates over $C_{\mathrm{bw},1}$ and so to the output. To limit these influences on the measurement, a second side order low pass filter, consisting out of R_{bw} and $C_{\mathrm{bw},2}$ is used, to limit the offset voltage transient noise.

When no differential voltage measurement is required, U_{ref} may be connected to GND.

9.5 Hardware Noise Reduction Technique

The following section discusses hardware design techniques for reducing measurement noise.

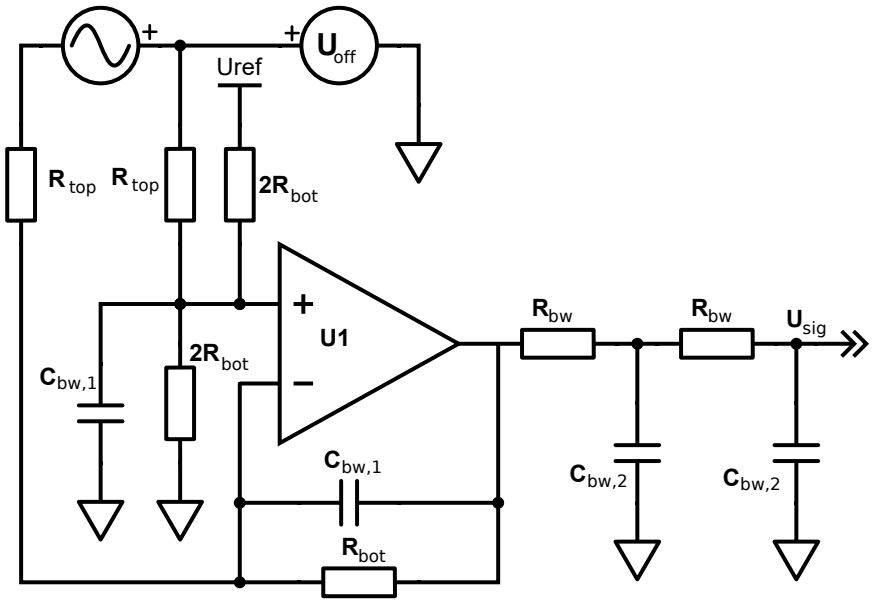


Figure 81: Differential quasi isolated high voltage current sense circuit.

9.5.1 PCB design for noise reduction

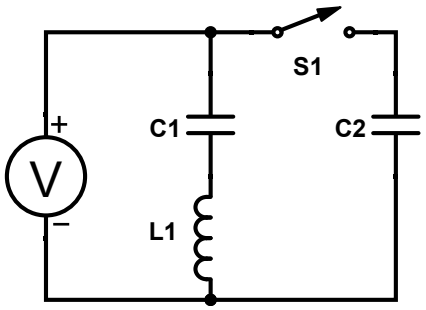
Analog-digital converters are sensitive against supply voltage noise. Power supplies are generally considered as noisy areas: E.g. the hard switching of a capacitor can introduce noise that can couple into the measured value. Therefore, the power converter circuit, especially the transistor half bridge of the SRC should be decoupled from the analog to digital converter.

The following example explains the noise source. Figure 82, shows a big bulk capacitor C_1. Its voltage should be measured. Due to the switching of power transistors, C_2 is instantly connected by S_1. The high current change over time ($\frac{d}{dt}I$) generates a voltage spike over the supply lines, generated by the parasitic trace inductance L_1. Hence, not the correct value would be measured.

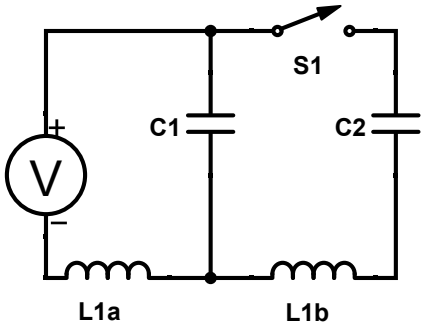
When the power and sensing wires are separated, as shown in Figure 82b, so called star sensing is used. It can help to reduce measurement error. As no switching transients are present on the measurement lines, its inductor L_{1a}, is not introducing switching noise. So, the actual, non-distorted voltage of C_1 can be measured.

The PCB design has to separate the power section from the signal section. Both planes must be linked in a single star point of the common bulk potential. The bulk capacitor negative node is typically a good choice, as it keeps the negative node stable. In case a differential signal has to be measured, separated ground sensing wires, so called star sensing, should be used.

A star sensing example is shown in Figure 83 for a star sensing of a current shunt. Two separate wires are connected to the sense resistor so that no inductance or resistance between the power path and the sensing paths are shared.



(a) Non-Separated ground noise



(b) Separated ground noise

Figure 82: Measurement noise in power converters has often its issue in switching noise that is caused by switching.

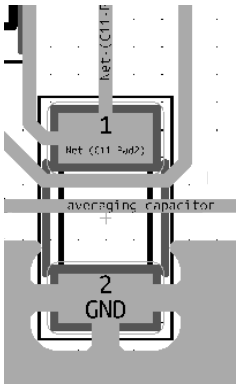


Figure 83: Star sensing of a resistor: The wire resistance and inductance can be excluded from the measurement by using separate sensing wires. As sensing wires do not conduct a significant amount of current nor current change, their parasitic components, like inductance or resistance, can be ignored.

9.5.2 Galvanic isolation of analog signal using digital isolators

The PFC/SLCC control requires the precise measurement of secondary side current and voltage. However, in offline power supplies, the primary side must not be connected directly to the secondary side. Hence, it is not possible to measure on the secondary side directly; a galvanic isolation to the primary side is required. Analog isolation, e.g. by using optocouplers, is generally used. However, it is known to add measurement inaccuracies like offsets, drift or nonlinearities.

Digital Isolators do not suffer from these issues. Further, they provide high data rates, up to 640 MBit/sec have been demonstrated [115, 116, 117]. Therefore, the following system design is proposed: The MCU requests data using the serial peripheral interface: The SPI signals are galvanically isolated. As the signals are digital, digital isolators can be used. This reduces inaccuracies and prevents optocoupler aging. The actual ADC is placed on the secondary side for signal conversion, as shown in Figure 84.

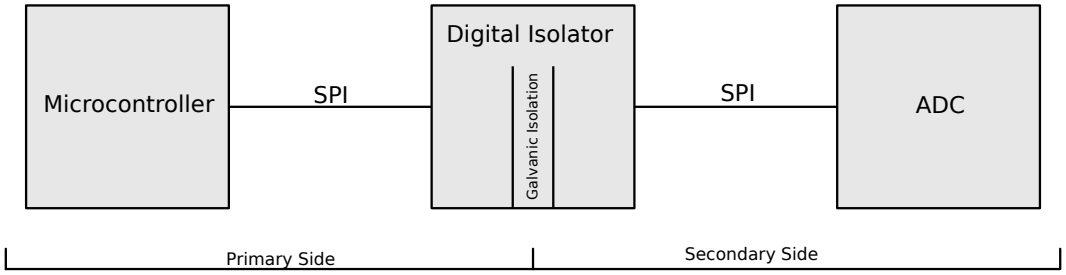


Figure 84: The MCU requests data over the digitally isolated SPI bus from the secondary side ADC.

9.6 Software Noise Reduction Techniques

Noise that could not be fully suppressed by hardware can further be reduced by software techniques.

9.6.1 Software Averaging

The straight-forward approach for filtering is averaging. Thereby several measurements are added and then divided by the number of samples s. This can be expressed by the following equation.

$$a = \frac{1}{n} \sum_{x=0}^{n} s[x] \tag{9.18}$$

To obtain a continuous stream of value, the newly obtained sample acquired is added and the oldest sample is removed. In the frequency domain this averaging method can be represented as a sin(x)/x function, as shown in Figure 85, as sin(x)/x is often designated as sinc. Hence, these filters are commonly referred to as sinc-filters.

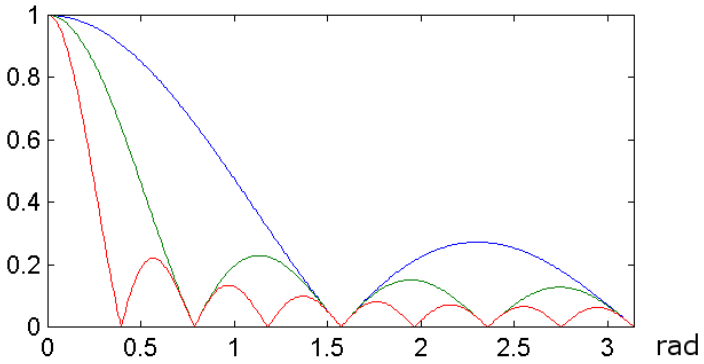


Figure 85: Low pass characteristic of a sinc filter for averages of 16 (red), 8 (green), and 4 (blue), based on [11].

Sinc filters have a low computational requirement. In an iteration loop, all values are added and then divided by the number of samples. A division takes 12 cycles in the MCU while a shift of one bit is only one cycle. To increase speed, a division by the factor 2^n, where n is the number of shifts, may be used.

By this approach the effective number of bits (ENOB) can be increased. If additional n bits should be sampled, the required sampling frequency with oversampling f_{os} can be calculated using the following formula [118]:

$$f_{\mathrm{os}} = 4^n \, f_{\mathrm{sig}} \tag{9.19}$$

9.6.2 Finite impulse response (FIR) filter

A finite impulse response filter is a more generic version of the moving average filter. In contrast to the averaging sinc-formula, each sample is differently weighted by adding a specific weighting factor. Every time t_{sample} a new sample is added, the old samples are moved one step back. As for each sample an additional multiplication is required, a significant increased amount of signal processing power is required compared to the moving average.

A fourth order FIR filter is shown in Figure 86, where every sample is multiplied by a weighting factor and is then delayed by one cycle. This principle can be extended to $n \in \mathbb{N}$, increasing precision and making the frequency response more accurate.

The minimal number n_{s} of FIR stages for low pass filters is one period of the filtered signal, t_{signal}.

$$n_{\mathrm{s}} t_{\mathrm{sample}} \geq t_{\mathrm{signal}} \tag{9.20}$$

For example if a signal is sampled with $f_{\mathrm{sample}} = 20\ \mathrm{kHz}$ and a low pass filter of $f_{\mathrm{signal}} = 50\ \mathrm{Hz}$

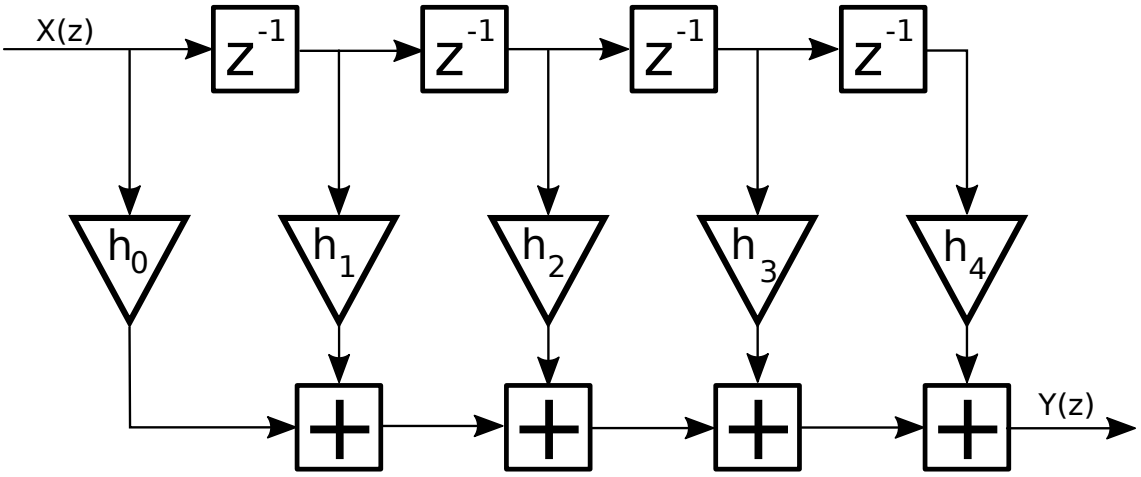


Figure 86: A fourth order FIR filter topology is shown: Every sample is multiplied with a weighting factor and is then delayed by one cycle.

should be implemented, at least a 400 th order FIR filter is required. This means, by a higher sampling frequency, not only the processing time slot is reduced, also the required number of CPU operations is increased. To reduce computational requirements, a prior averaging filter can be used.

9.7 Resonant Observers

Resonant observers are shown in Figure 87 and used for observing constant values, amplitudes and phases of known sinusoidal frequencies. For the proposed PFC/SLC regulation topology the amplitude of the following sinusoidal signals have to be measured.

- The AC amplitude of the grid frequency
- Suppression of the double mains frequency at the DC link for the downstream DC-link voltage control algorithm.

The regulation diagram of resonant observers shown in Figure 87 is based on [12]. A resonant observer is a closed loop controller with a directly closed control path. It can estimate a constant value by means of an integrator, shown in the top of Figure 87. Further, it can observe the amplitude and phases to a known fixed reference frequency. For this, the control signal is transformed into another space: The reference waveform space of a known frequency. Therefore, the signal is multiplied with a $cos(x)$ and a $-sin(x)$. Both signals are then passed to an integrator with the gain K_{rn}. By this the I regulator can adjust the amplitude and the phase of both signals. Both signals are then transformed back by the means of multiplication.

The amplitude of AC signals can be calculated by reading the two integrator values, with the value $v_{\cos}$ and $v_{\sin}$, using the following formula. The corresponding variables are highlighted in Figure 87.

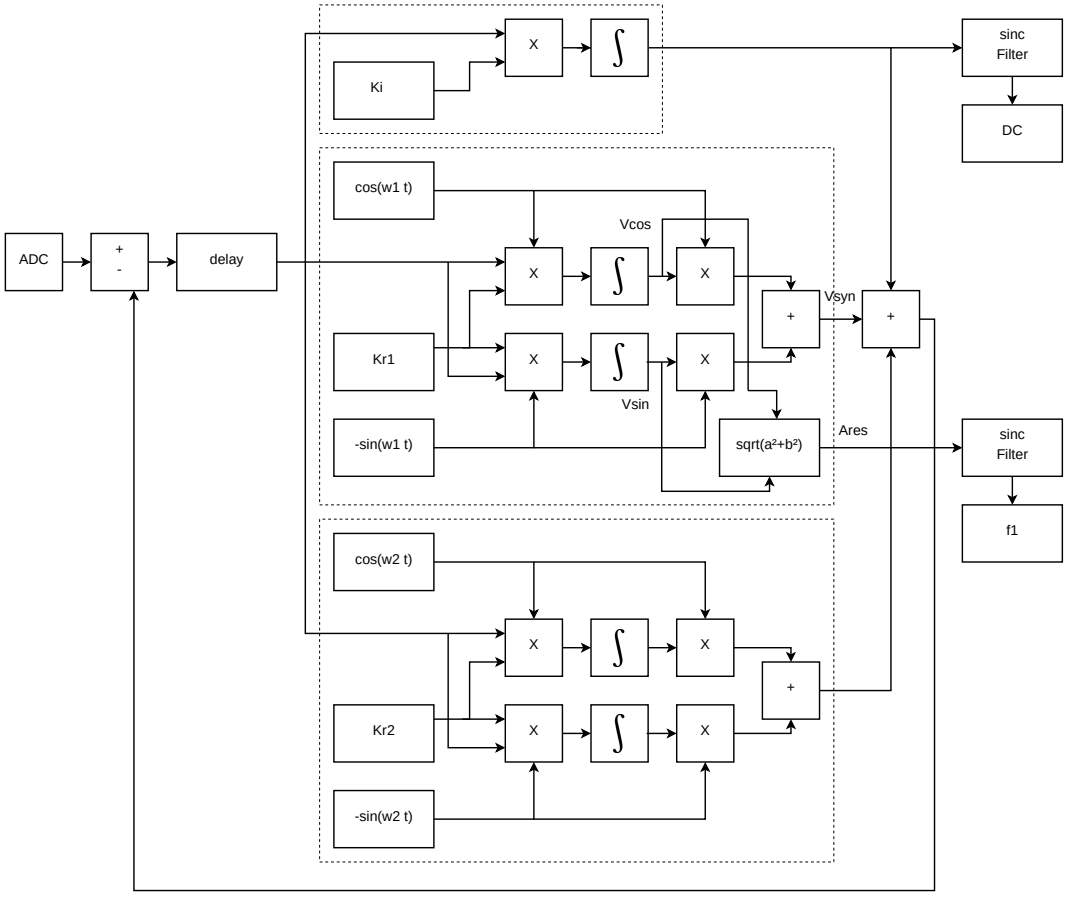


Figure 87: The filter topology is based on [12]. The separator is a control loop consisting out of an integrator tuned to the measurement frequencies. The bandwidth of the resonant observers can be determined by Kr_n.

$$A_{res} = \sqrt{v_{\sin}^2 + v_{\cos}^2} \tag{9.21}$$

The virtual phase ϕ can be calculated by the following formula:

$$tan\,(\phi) = -\frac{v_{\cos}}{v_{\sin}} \tag{9.22}$$

One estimator is limited to one specific center-frequency. To accept and observe multiple frequencies, resonant observers may be paralleled. Thereby several frequencies can be estimated at the same time. The paralleling of resonant observers is shown in Figure 87, where two parallel resonant observers are used.

Further, resonant observers allow to synthesize ideal waveforms. For example, if only the 50 Hz amplitude of the grid should be used for calculus, the output value of the resonant observer, v_{out} can be used. The variable is shown in the control diagram in Figure 87.

9.7.1 AC amplitude measurement

To measure the grid (AC) frequency, the first regulator is tuned to the grid frequency, which is 50 Hz in Europe. To accommodate 60 Hz, a second integrator could be added [12]. The DC integrator measures the DC grid offset, which results from measurement inaccuracies. Typically, this value is close to zero.

The amplitude of the AC measurement can be calculated using the following formula:

$$U_{\mathrm{amp}} = \sqrt{U_{sinint}^2 + U_{cosint}^2} \tag{9.23}$$

9.7.2 DC link average voltage measurement

The resonant observer is used as a notch to suppress the desired 100 Hz DC-Link ripple. Thereby the average voltage of the DC-link is observed by a DC integrator and a resonant 100 Hz filter.

As the 100 Hz ripple should be rejected, the momentary value can be obtained by subtracting the measured signal from the observed 100 Hz signal part. This can be expressed by the following formula:

$$U_{\mathrm{notch}} = U_{\mathrm{meas}} - U_{\mathrm{syn}} \tag{9.24}$$

10 Protection Concept

Power supplies must be resilient to harsh environments. Therefore, possible failure issues are analyzed and a corresponding protection feature is proposed. The protection concept also protects against software errors, that occur especially during the development stage. This section covers the corresponding protection for the failure issue and its recovery methodology. First the hardware failure protection is covered, followed by the software protection.

10.1 DC Link Overvoltage Protection

The overvoltage at the DC Link can be fatal to the converter: Overvoltage may destroy the half bridge. When one switch of the half bridge fails due to overvoltage, a short circuit results in a total unrecoverable loss of the converter. Therefore, the DC Link capacitor (HV) is closely monitored by a voltage sensing network as shown in Figure 88. The cause of overvoltage is typically an error in the control loop, supplying too much energy to the DC link capacitor. This error can be resolved by a PWM turnoff. The turnoff level is set to 800 V in this design, where the switches can handle a maximum voltage of 900 V.

A voltage divider (R_1 and R_2) is used to divide the voltage to MCU acceptable levels. It is filtered by a bypass capacitor C_1 to suppress noise. If the voltage sense exceeds the predefined digital to analog converter (DAC) value in Figure 88, an overvoltage signal is passed to a digital filter. After several consecutive events, the PWM signal is turned off. The PWM unit then shuts down the half bridge.

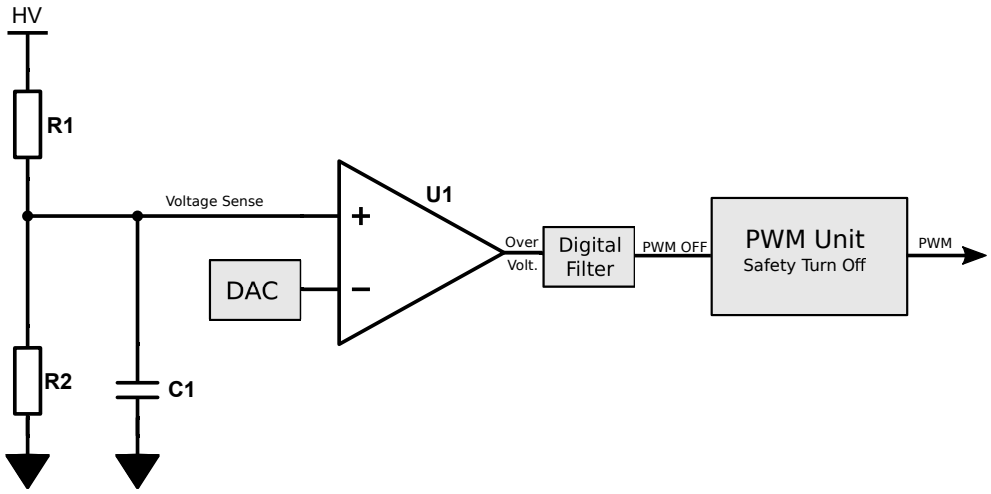


Figure 88: An overvoltage comparator turns off the PWM waveform generator. The overvoltage is filtered analog and digitally.

Short term overvoltage events that are not covered by the protection can be dissipated in transient voltage suppressor diodes (TVS) or Metal Oxide Varistors (MOV), as discussed in section 6.3.6 on page

91. Those devices are designed to absorb a significant amount of energy for a very short time. By this clamping, high voltage transients are absorbed, to prevent harm to the converter components.

10.2 Overcurrent Protection

A common failure issue in the firmware development process is the setting of wrong PWM values. A software error may cause an erratic set of duty cycle D or switching period t_{c}. This may lead to overcurrent in the SLC converter, leading to fatal failure. If S_1 in Figure 89 would conduct continuously, a too high current may be observed at the SLC converter. Therefore, a similar circuit as in Figure 88 is implemented, that checks for the maximum voltage of a current shunt.

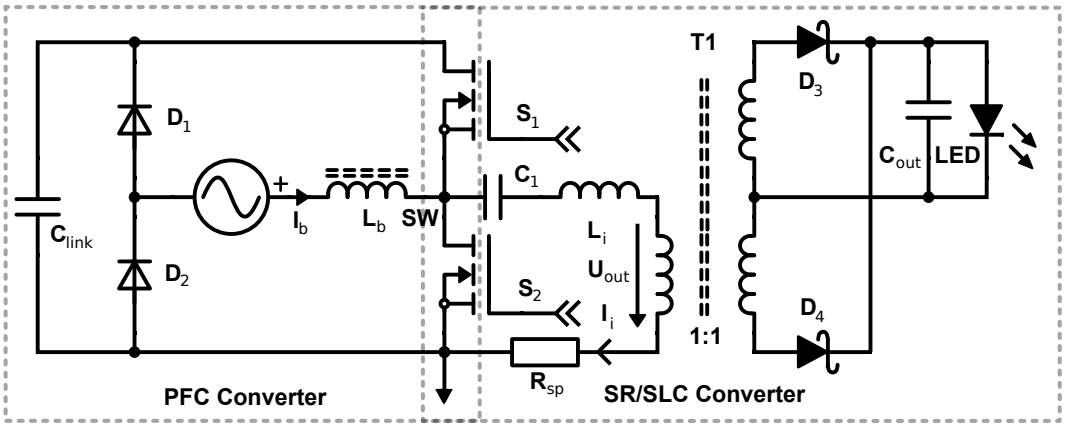


Figure 89: The SLCC current I_{i} is sensed by the shunt resistor R_{sp} that is connected to an overcurrent protection.

If an excess negative current would occur at high duty cycles, this error is not covered instantly. A window comparator would allow a more secure protection. However, the series capacitor limits the power that can be transferred.

Further, this overcurrent protection only covers the SLC, and does not cover failures of the PFC converter. A PFC failure indicates itself by an increased dc link voltage that is observed by the previous overvoltage protection.

10.3 Software Monitoring

The software monitoring is implemented to safely shut down the system on an occurring error. If typical operating conditions are left, this is an indicator for erratic PWM values or failed regulation. A indicator for erratic regulation is that the typical operating conditions are left. Typically, such errors are not highly time critical, where a turn-off within milliseconds is sufficient. Examples of typical protection events are listed below:

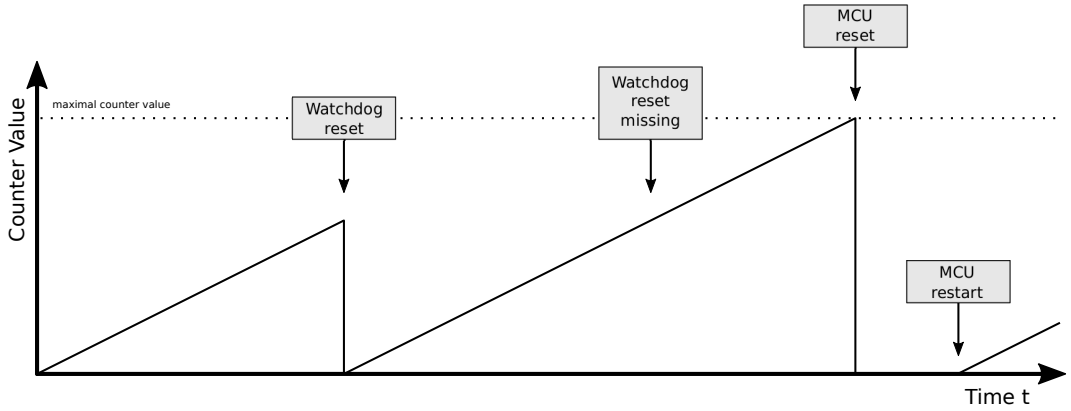
1. Secondary Overvoltage
2. Secondary Overcurrent
3. Excess noise / ripple
4. Over temperature: Typically over temperature event occurs when the ambient temperature is too hot or the converter is overpowered.

Software tests are easy to implement. However, its response time is always slower than the hardware implementation. Therefore, this approach should only be used for less safety critical parameters. Highly time critical events, for instance primary over-current or primary overvoltage could not be supervised by software monitoring. For these kind of applications active hardware monitoring as described in section 10.1 should be used.

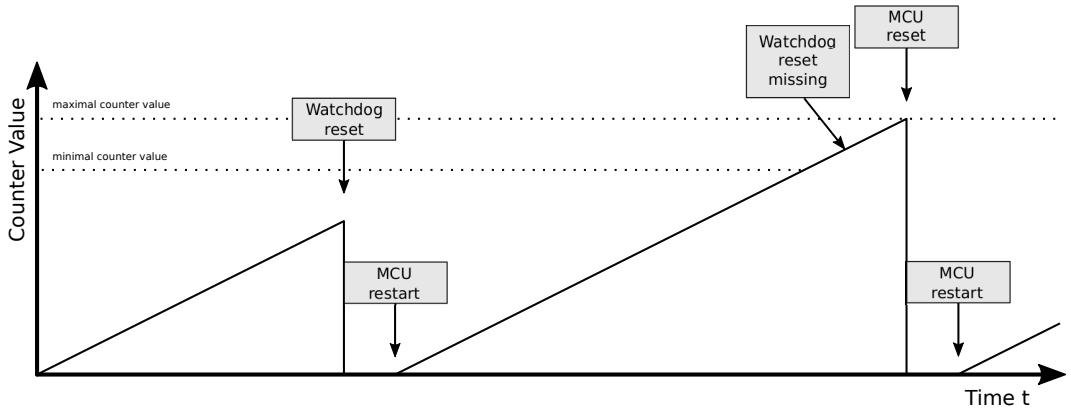
10.4 Operation Monitoring of the MCU

The operation of a MCU is monitored by the use of a watchdog [119]. Thereby the watchdog must be reset by MCU within a specific time, otherwise a reset is issued, as illustrated in Figure 90a. Also the watchdog can be extended by a window mode, where the reset must not occur before a specified time, as shown in Figure 90b. By this, the windowed watchdog supervises that the software loop is not stuck in a continuously issued watchdog reset.

The watchdog may be used externally or internally. External watchdogs offer an increased level of safety, as the clock and power supply domain is independent of the MCU. An internal implementation reduces the software- and hardware requirements. The MKE14F256 microcontroller used in this design, includes a watchdog [120]. For this design, the internal watchdog is used.



(a) Standard Watchdog



(b) Windowed Watchdog

Figure 90: Operation principle of a standard and windowed watchdog and their operational behavior in comparison.

11 Auxiliary Power Supply

The operating power for the CPU, gate drivers and analog measurement is supplied by the auxiliary power supply. This chapter discusses the corresponding design methodology. It includes techniques for achieving accurate measurements by proper filtering of the auxiliary power supply.

11.1 Auxiliary winding

For the supply of the auxiliary power, an auxiliary transformer winding is placed on the primary and secondary side, as shown in Figure 91. The AC is rectified by a full bridge DB1 and DB2 respectively. The auxiliary voltage is influenced by the DC Link voltage and the output voltage and hence varies. Therefore, this voltage has to be adjusted to a defined voltage level by a point of load converter. Point of load converters (POLC) are switching converters and operate with a high efficiency over a broad input voltage range.

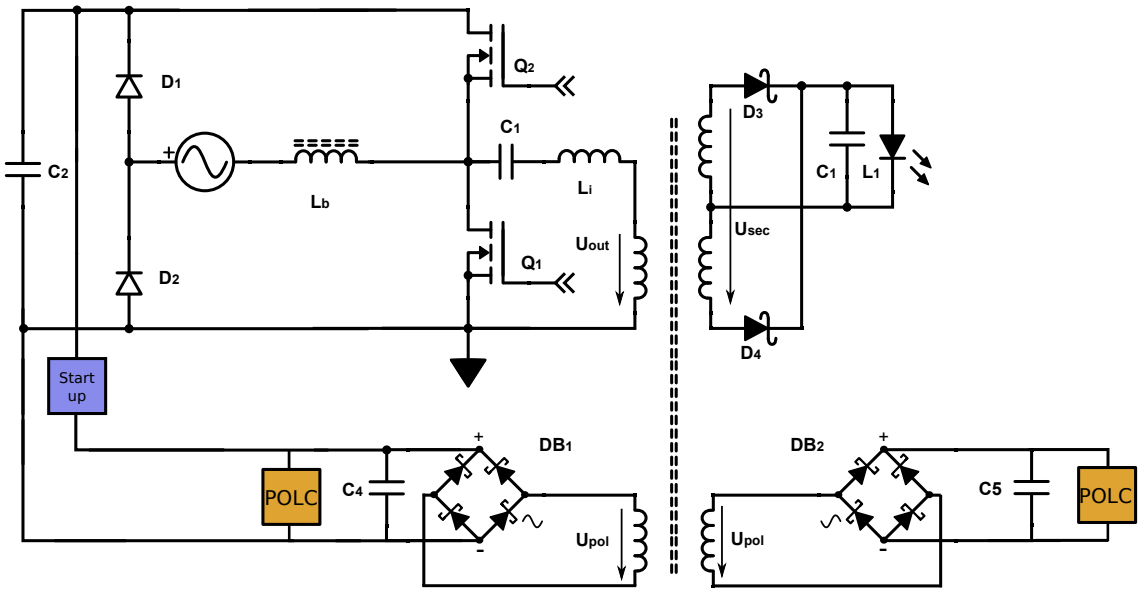


Figure 91: The SLC topology is extended by two auxiliary windings: One on the primary side, one on the secondary side to supply point of load (POL) DC/DC converters that generate all internal voltages.

For this design, the POLCs on the primary and secondary side can accept voltages from 5 V to 30 V.

The self supply topology for the primary and secondary side is depicted in Figure 92. The POLC voltage is set to 3.6 V. The gates are supplied by a boost converter that converts the 3.6 V rail to 16 V. First down-converting the voltage from a high voltage and then up-converting to a higher voltage may not be the most efficient approach. However, it allows a wide input voltage range. At high and low POLC supply voltages, e.g. from 5 V to 30 V, a stable gate driver voltage of 16V can still be

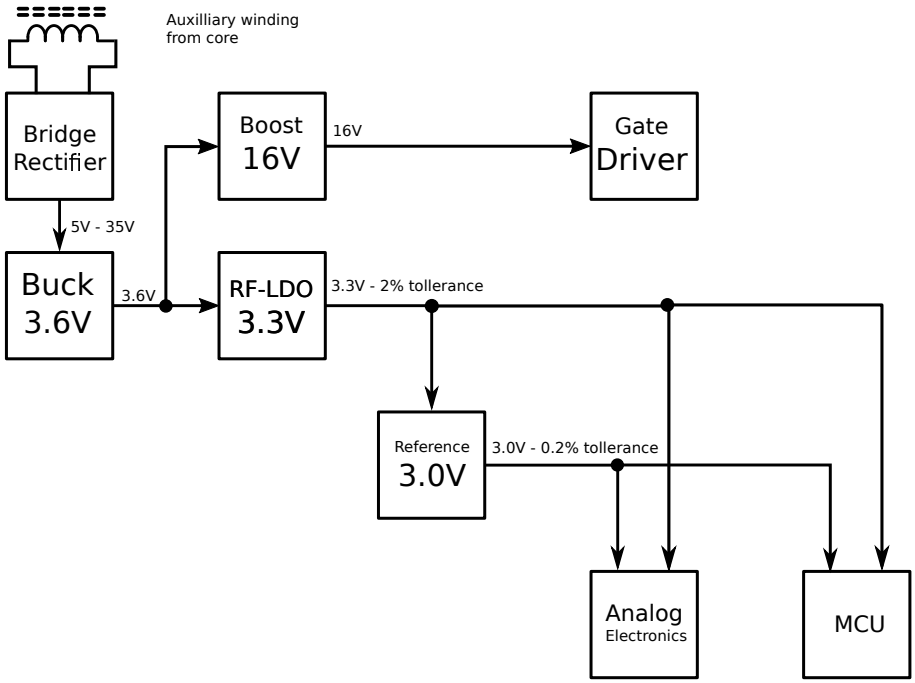


Figure 92: The self supply voltage converter supplies the converters auxiliary power. The auxiliary winding is used to obtain this power, then the power is rectified, down-converted to a 3.6 V rail by a POLC. The 16 V gate driver supply and the 3.3 V internal operation voltage are generated out of this supply. For accurate measurements, a +-0.2% 3.0 V reference is used. For an accurate measurement, analog electronics, like Op-amps, and digital MCU are decoupled by low pass filters.

guaranteed. E.g. with a direct boost converter, without previous down conversion, a stable gate drive voltage of e.g. 16 V is not possible, when a high input voltage is present. Further, the required gate driver power is minimal. Therefore, a wide input voltage range is preferred over a high efficiency.

To generate the microprocessor power with attenuated noise, a 3.3 V linear RF low dropout regulator (LDO) is used. The RF LDO is specially designed to filter voltage spikes of the supply voltage rail to suppress noise to the MCU and analog electronics. Analog electronics is more susceptible to supply voltage noise. Therefore, its supply is separated from the digital rail by a resistive/capacitive low pass filter.

Without the RF LDO, at some rare events, transients may have issued a reset at the MCU. Additionally the analog noise while measuring is reduced.

For accurate measurements of the ADC the REF3030 voltage reference with $\pm 0.2\%$ accuracy is used [121]. The reference voltage is also used for the bidirectional voltage and current measurement as accurate offset. The microcontroller uses the reference voltage for its ADC measurements. Even though the microcontroller offers an integrated reference voltage, it is not precise enough for our application. The major issue of the internal reference is its low reference voltage of 1.0V [120, p.50]. Thus, it was highly susceptible to noise. Additionally the MCUs reference voltage features an accuracy of only $\pm 3\%$.

11.2 Startup Circuit

The startup circuit is required for initial power-up of the LED driver. During power-up the converter is not switching, thus the transformers auxiliary winding cannot supply power. To generate the required initial power, a so called startup circuit is used.

11.2.1 Circuit Discussion

This startup circuit is basically a high voltage linear converter that drops the voltage difference between the high DC link voltage and the low control voltage.

The circuit diagram is shown in Figure 93. The startup circuit is a high voltage linear constant current converter. In its default state it is turned on, and can be actively turned-off by the MCU. Depletion mosfet Q_1 is configured by means of resistor R_1 and R_3 as a constant current source. The capacitor C_1 buffers the voltage, where D_2 limits the maximum voltage to prevent overvoltage. To limit the power requirements of Q_1 a series resistor R_4 is added. Additionally it can limit the peak current of Q_1.

When the transformer auxiliary winding is operating, the startup circuit is not required. It can be disabled by turning on Q_2. R_2 is used to limit the current flow, where D_1 ensures that a maximum gate voltage is not exceeded. The zener diode D_2 is used to limit the maximum supply voltage V_{dd}. Thereby it is protected against overvoltage. The output capacitor C_1 is used to stabilize the converters supply voltage.

11.2.2 Loss analysis

As the linear converter is supplied with a high voltage, it is highly inefficient. Assuming a 600 V DC Link voltage, that is dropped to low voltage varying between 5 V and 30 V, only 5 % of the energy is used in the best case. Therefore, the mosfet Q_1 must have a big enough thermal capacitance to accommodate the heat during startup. By the knowledge of current and voltage drop the average power during startup can be calculated.

$$P_{\mathrm{m}} = U_{Q1} I_{\mathrm{Q1}} \tag{11.1}$$

Thermal resistance is calculated using the power, and the allowable temperature increase.

$$R_{\mathrm{tm}} \leq \frac{P_{\mathrm{m}}}{\Delta T} \tag{11.2}$$

For the calculation of the maximum allowable time the thermal impedance chart for the correspon-

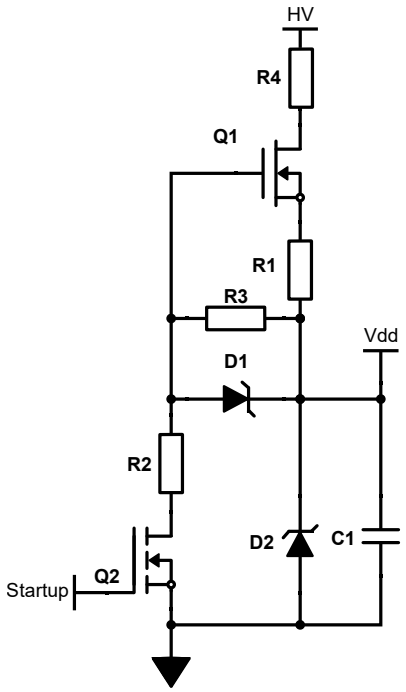


Figure 93: The startup circuit consists of a constant current depletion mosfet Q2 that charges the capacitor C1. A zener/TVS diode is used to limited the maximal voltage for the downstream buck converter.

ding case can be used. In this design the SOT223 package is used and the corresponding chart is shown in Figure 94. As the startup typically happens very rarely, the single pulse chart is used.

To further decrease the temperature increase, cooling planes may be added, as shown in Figure 95. The manufacturers thermal impedance chart depicts a worst case scenario. In measurements it was observed, that the device could be far more stressed than specified in the thermal impedance graph.

By reducing the voltage drop the mosfets power dissipation may be decreased. TVS diodes and wire wound resistors are known and designed to be resilient against overstress. TVS diodes may be used to limit the maximum voltage. Therefore, a TVS diode in series reduces the mosfets stress. Series resistors may be added to reduce power stresses during turn-on.

However, when the power of the mosfet is not turned off it might be damaged and the complete converter can be destroyed. Generally speaking strong attention must be payed in the software to reduce the risk of overstressing Q_1. A good practice during design testing is adding a fusible resistor, that cuts connection when it is overpowered. By that the complete destruction of the circuit and the complete replacement of all components can be avoided. Although the LED driver will not be operational then, the damage is limited to the fusible resistor.

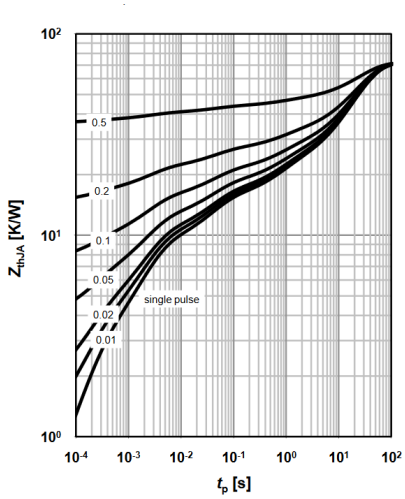


Figure 94: Thermal impedance of the BSP135 depletion mosfet, reproduced from the datasheet [13].

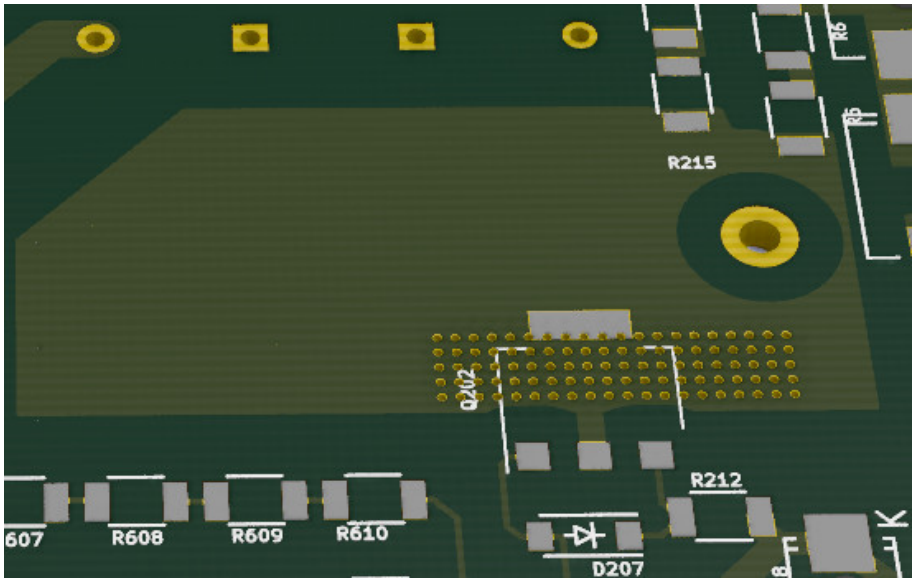


Figure 95: Power planes may be used for cooling power devices: Depletion mosfet Q202 is cooled via a significant power plane, the heat is also conducted to the other side of the PCB by the use of thermal vias.

12 Reliability measurements

To confirm a reliable operation, two endurance tests are carried out. The first endurance test operates the LED driver continuously, while the second test pattern switches on and off the LED driver repetitively. The endurance tests discover major design flaws.

12.1 Test Setup

The test setup can be subdivided into two sections, which cover the typical failure issues.

1. Continuous operation tests the long-term operation capability of the converter.
2. The switch-on test tests the resilience of the converter against switch on/off operation.

12.1.1 Continuous Operation

The test setup for continuous operation is shown in Figure 96. The device is tested under ambient temperature.

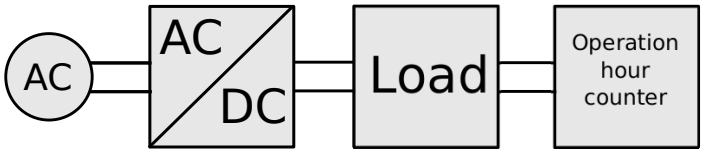


Figure 96: Test setup for continuous operation.

The operation-hour test stand is constructed inside a Din-Rails fuse box, shown in Figure 97. If the load is supplied with power, the operation -hour counter is running.

Figure 97: Continuous operation test jig for demonstrating long time operation.

12.1.2 Switching Operation

The switching operating tests should demonstrate that the converter may tolerate a significant number of switch on/off cycles. LED lamps have shown to be susceptible to this operation mode due to the inrush current or increased startup load. Therefore, a test setup according to Figure 98 was built.

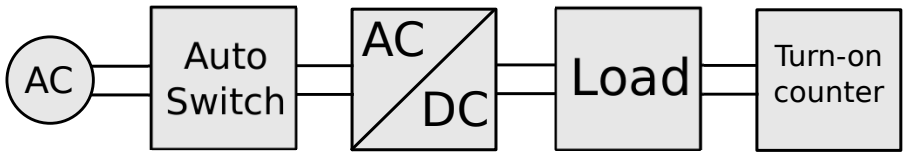


Figure 98: Testing setup for switch on/off test switches the converter on, operates it, and switches it off. A counter measures the repeated cycles.

Figure 99: The on/off switching test jig turns the LED driver on for 30 seconds and then turns the LED driver off for 30 seconds. The counter increments with every successful LED driver turn-on.

Test conditions As a converter is switched-on typically once a day, thus typically 365 times a year. To ensure 20 years of operation, 7300 switching cycles have to be demonstrated. A typical switching operation takes 1 minute: 30 seconds the driver is switched on, 30 sec the driver is switched off. Consequently, the tests can be completed in roughly 5 days.

Test results The converter was operated continuously for approximately 1 month under the specified test conditions. After 46 000 on/off cycles the converter was still operational.

12.2 Discovered Failure Sources

Failure issues are traced down to the power converter part of the series LC converter, especially the high voltage ceramic capacitors were susceptible.

12.2.1 Multi Level Ceramic Capacitors

Multi Layer Ceramic Capacitor Self Heating at 50 Hz It was discovered that 1000 V X7R Ceramic Capacitors have a significantly increased series resistance at 50 Hz. Thus, they significantly heat up at 50 Hz or 100 Hz grid voltage with a voltage ripple of $625\,V_{\mathrm{Peak2Peak}}$. Therefore, MLCCs are highly discouraged in low frequency applications.

Multi Layer Ceramic Capacitor Breakdown During the early lifetime tests it was discovered that the capacitors C1 of the SLC topology may encounter an internal break due to high speed voltage transients. C1 can be observed in Figure 64 on page 96. Therefore, multi layer ceramic capacitors in series LC converter operations have to be avoided.

Multi Layer Ceramic Capacitor Acoustic noise Additionally MLCC capacitors may produce acoustic noise. Typically this can be observed at high voltage, high capacitance MLCCs. The piezoelectric effect may introduce a humming sound that may disturb the user.

12.2.2 Film Capacitors

Before the endurance test, it was discovered that the film capacitors have a limited voltage slope capability. Therefore, the capacitor has to be adequately sized in terms of voltage ripple. Further, the voltage slope has to be limited during the duty cycle inversion. The duty cycle inversion is covered in section 7.4.

12.2.3 Transformers

The switch-on test showed that the transformer can suffer from high voltage spikes. Thus, a conformal coating was applied to the transformer for enhanced dielectric isolation. Further, kapton tape was added between each winding layer to further strengthen the insulation.

12.2.4 Gate Driver Pull Down

Despite a pull-down resistor is already integrated in the gate driver, an explicit pull down resistor was added to the gate. It avoids capacitive self-turn on and resulting shot-through.

12.3 Summary

The lifetime testing showed that the converter is resilient against switch-on behavior. Degradation test under nominal temperature were conducted. However, the test period was too short to cause any failure. In the measurement section it could be demonstrated that self-heating of the converter is minimal, ensuring a long lifetime of the LED driver. Theoretic lifetime calculation in section 6 prove this.

13 Software Engineering

The software engineering section covers the control and protection algorithms applied on the MCU. One aspect is that the timing of the control must be maintained under all conditions. This section describes the utilized technological steps for adequate software performance.

13.1 Hardware offloads Software

The general strategy in software engineering is to offload the software by using hardware accelerators. Especially repetitive tasks, i.e. moving data or managing timing functions, are ideally completely handled by hardware accelerators. The ideal software function is designed in such manner, that it is only executed once at startup. All subsequent iterations are handled without CPU intervention. Further, all time-critical CPU operations should be buffered in SRAM for zero-wait-state-reads. In case the software is busy with another task, the values can be read later from the RAM, and are not overwritten by the new value. This reduces the risk of data corruption.

The software should be reserved for complex calculations that cannot be offloaded to hardware. These operations are especially control and math calculations.

13.2 Direct-memory-access for Data Acquisitions

Data transfers inside the MCU are implemented by the method of direct memory access (DMA). A direct memory access has a hardware trigger, e.g. a PWM unit. When the corresponding trigger is received, data is transferred from a source address to a destination address in a so called major loop. Start-addresses and stop addresses may be configured with an increment for each trigger event. This means, after each iteration, the source or the destination address can be increased by a fixed integer.

A so called minor loop allows to execute several data transfers, e.g. multiple bytes, within one trigger event. A major loop, as illustrated in Figure 100, requires a trigger event to execute the minor loop. After the major loop is completed, the DMA can be optionally halted. Also an interrupt can be generated in which the acquired data can be processed.

The DMA operates completely without CPU intervention. The DMA shares the same data bus as the MCU. Thus, one CPU clock cycle is required for the transfer. The DMA therefore waits until the CPU does not require the memory bus. Hence, for data transfers no CPU processing time is required.

Generally speaking, the following generalized acquisition structure, illustrated in Figure 101, can be observed. Data is acquired repetitively by the responsible unit, e.g. an ADC. Each measurement result is transferred to SRAM. After a specific number of transfers, an interrupt service routine (ISR) is triggered. Within the ISR data is processed by the processors hardware: Typically the acquired values

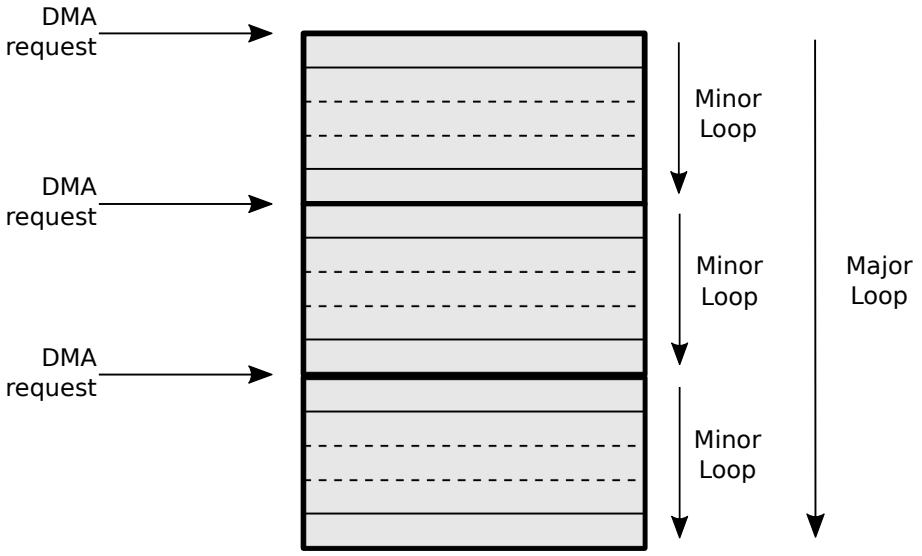


Figure 100: DMA acquisition structure: The data is acquired automatically by the responsible unit. Each data-element is transferred to SRAM by the DMA. After a specific number of transfers an interrupt is issued and the data is processed.

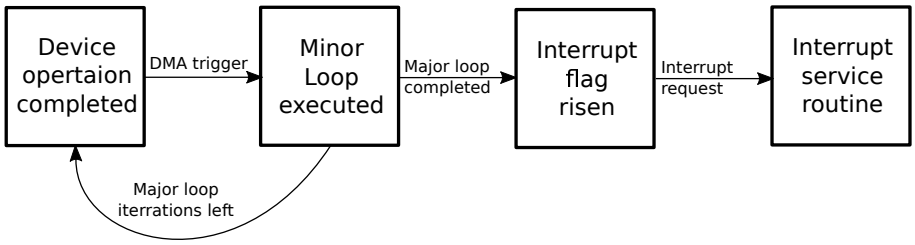


Figure 101: Data transfer flow from acquisition units, e.g. ADCs, is illustrated: When a device operation is complete its data is transferred within the minor loop. When the major loop is completed after several transfers, a interrupt flag is risen. The CPU can perform its calculations based on the acquired data in the interrupt service routine.

are integers that are scaled in software to human-readable floating point variables. A downstream plausibility check ensures that only valid numbers are used for the subsequent control. An obvious non-plausible result, e.g. a negative output voltage, would trigger the software protection, discussed in section 10.3.

13.2.1 ADC DMA Data Acquisition

The used MCU, MKE14F256 from NXP, integrates three simultaneous operating ADCs [120]. They can be configured to work at up to 1 Mega-Samples-per-Second (MSpS). Thus, a significant amount of data, 2 MByte/sec must be transferred from each ADC to the memory. When an ADC conversion is completed, the DMA transfers the acquired result from the result register to the SRAM. As only 16 Bits must be transferred, the minor loop requires only one iteration. The major loop, specifies how many samples are acquired until an interrupt is triggered. Assuming an ADC conversion rate of 1 MSpS and a major loop of 10, the interrupt is triggered at a rate of 100kHz. In the interrupt service routine the ADC conversion result is converted to a human-readable floating point value. The ADC itself can also raise an interrupt flag. This is used in the software to trigger a CPU conversion interrupt routine. For example this can be used to convert the measurement value of the grid voltage to a float value instantaneously.

As seen in the equation (8.3) and (8.6), two major primary side results must be measured continuously: The DC Link voltage U_{dc} and the momentary AC voltage U_{ac}. The output voltage on the secondary side, U_{out}, is measured isolated and is covered in the next section.

13.2.2 External SPI DATA Acquisition

The secondary side voltage must be measured isolated, as primary side and secondary side must be galvanically isolated. For this propose, digital signals are isolated, as discussed in section 9.5.2 on page 128. The DMA continuously requests data from the secondary side ADC over the Serial Peripheral Interface (SPI) interface. After twenty data samples have been acquired, data is averaged, converted to the human-readable form and then passed to the control loop.

The SPI acquisition routine is configured to request data of two values repetitively: The DC output voltage U_{out} on one channel and the DC output current I_{out} on the other channel. The SPI acquisition procedure is shown in Figure 102. The acquisition channel is selected by the corresponding MOSI line. The MOSI line is connected to the acquisition select line of the ADC. The sampling starts by pulling the chip select $\overline{CS}$ line low. The ADC is clocked by the CLK line and transmits the conversion results back to the MCU using the MISO line. The first DMA channel repetitively puts these two consecutive requests to the transmit buffer of the SPI unit. The received data is copied by a second

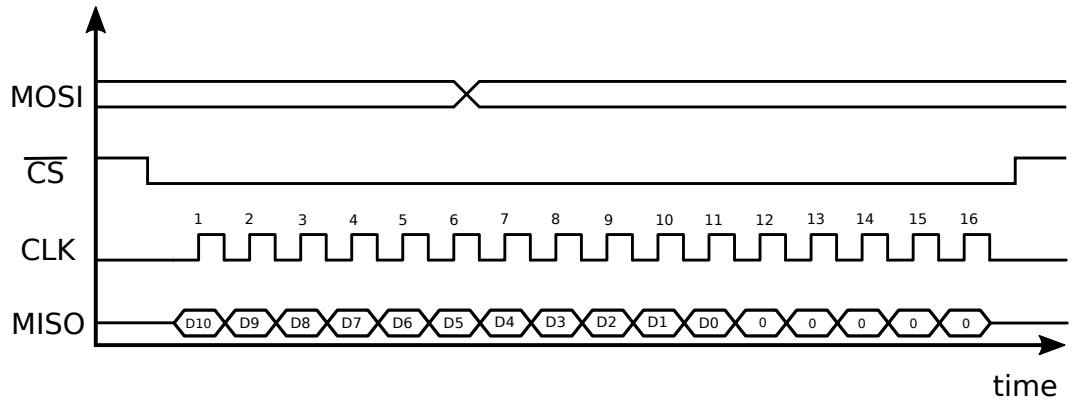


Figure 102: Data acquisition from the ADC using the SPI interface. The DMA requests ADC data in an infinite loop for channel one and two alternatively.

DMA channel from the receive register to the SRAM. After a specific number of iterations, the DMA issues an interrupt service request (ISR).

In the ISR the values are checked for plausibility and then are passed to regulation. It verifies that the 4 least significant bits are zero. If e.g. the secondary side ADC is not powered, the isolator outputs all transferred bits to one. Using this principle, a non-functioning ADC can be discovered.

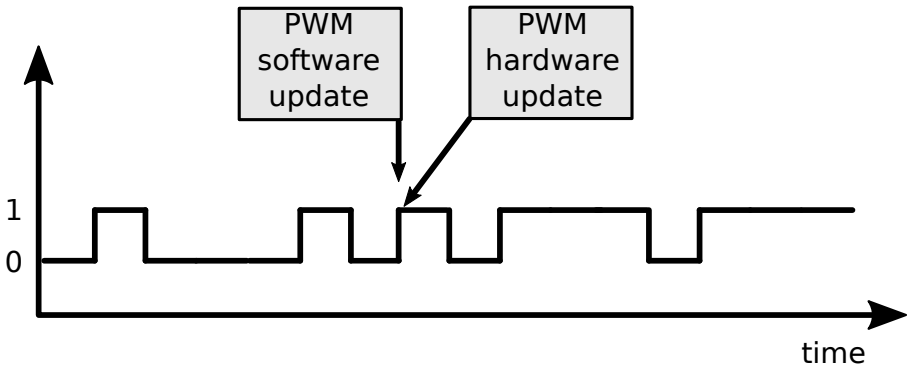
13.3 Buffered Data Writes for PWM

The PWM waveform for the converter could be distorted by updating with new values: When a novel computation result is available and it would directly be written to the timer, the timer would output an undefined waveform. Therefore, it is important that the timer registers are double-buffered. First, the novel computed parameters are copied to the buffer. Then the writing is enabled and the novel value is used when a fresh PWM cycle is started. By this synchronization a distorted PWM waveform can be avoided.

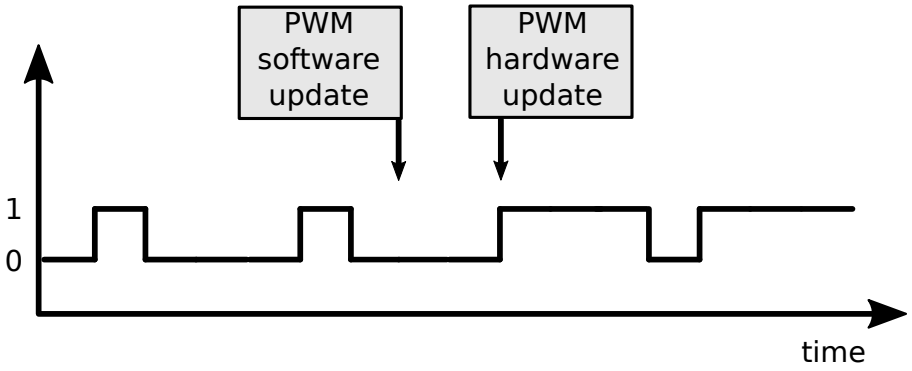
13.4 Interrupt driven Regulation

The timing in control applications is highly critical. It is a well known issue that a jitter in the control period of the control loop may cause instabilities. One example are integrators that are used in closed loop control. Typically a constant time is assumed. If now the time jitters, the integration weighting factor changes.

Therefore, each control function is separately triggered by a timer. If the specific time has passed, an interrupt is triggered and the control loop with the highest priority is instantly executed.



(a) Distorted waveform due to asynchronous write to the PWM register



(b) First one waveform is fully issued, then the next waveform is transmitted.

Figure 103: A distorted PWM waveform can occur when a value is directly written to the PWM register. The distortion is avoided by allowing only a transfer at a fully carried-out PWM cycle.

13.5 Using FPU for Control

The utilized MCU includes a floating point unit. The floating point unit in the Cortex M4 allows to execute multiplications and additions on floats within one clock cycle. This means, floating point calculations can be used for control. Even a division or a square-root can be calculated within 12 clock cycles. This very efficient CPU core is therefore ideal to implement the complicated control algorithms evaluated in the previous section.
The FPU is very easy to handle from the software side. Except from its activation no additional steps are required.

13.6 MCU Tracer for Data Entry, Checking and Control

For the analysis of parameters, a self-written analysis tool is used, which is named MCU Tracer. It uses an isolated USART protocol for data transmission. Using the MCU Tracer, data can be read or modified as shown in Figure 104. Also error and debug messages from the debugger can be received, as shown in Figure 105.

To execute tasks, functions are implemented within MCU tracer. For example, a function to turn on the PWM can be written, as shown in Figure 104.

13.7 Diagnosis of Errors

To prevent bad regulation due to erratic data, a self-checking function for testing the MCUs components is implemented. By this, data can be checked using a self-test. Several parameters are checked within the self-test function:

- Supply voltages
- Gate supply voltage
- ADC noise

If an error occurs, it is reported by the means of MCU tracer text output, as shown in Figure 105.

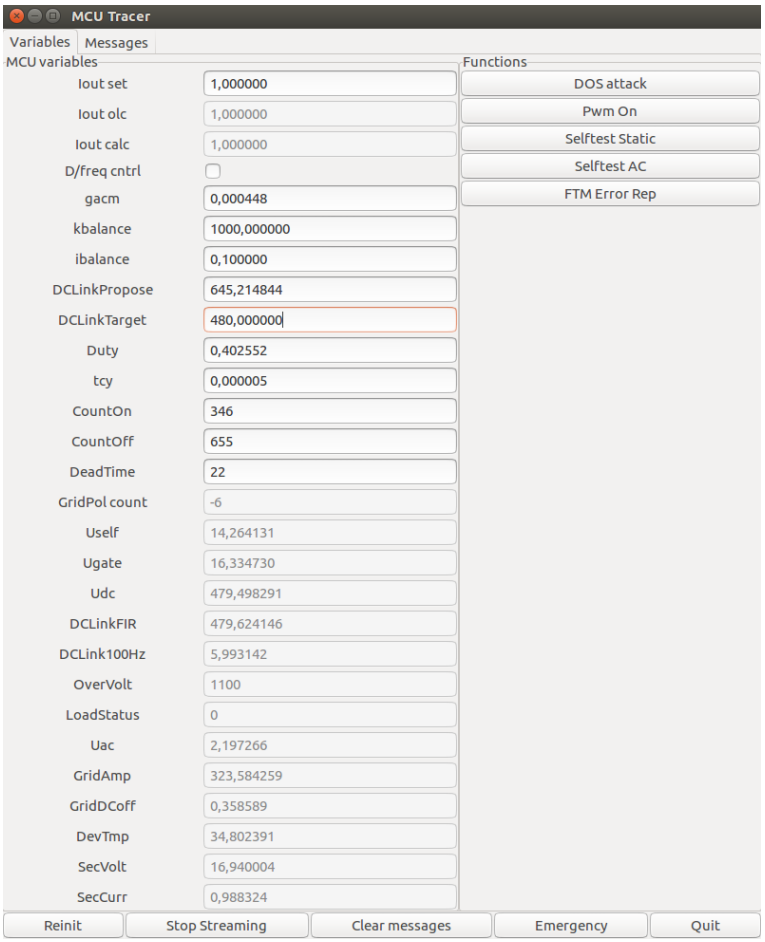


Figure 104: The MCU Tracer can be used to read data from the MCU. Data may be modified using the MCU Tracer. By this, parameters can be adjusted actively during software operation. Functions can be executed by clicking on the corresponding button.

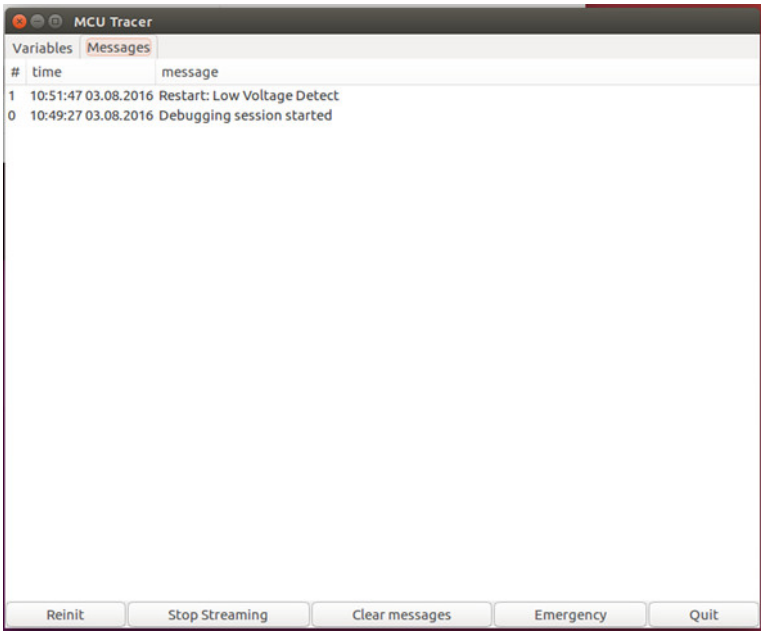


Figure 105: The MCU tracer can display debug messages to the user. It helps to identify failure issues.

14 Measurements & Verification

First the construction technique of the prototype platform is discussed. Major quality factors that were previously defined, are measured to confirm the adequate operation of the converter. In the first part, the construction technique is explained and fundamental operation is confirmed. Second, the correct operation of the series LC converter is verified. In the third part, the SLC is extended with a PFC and this operation is demonstrated.

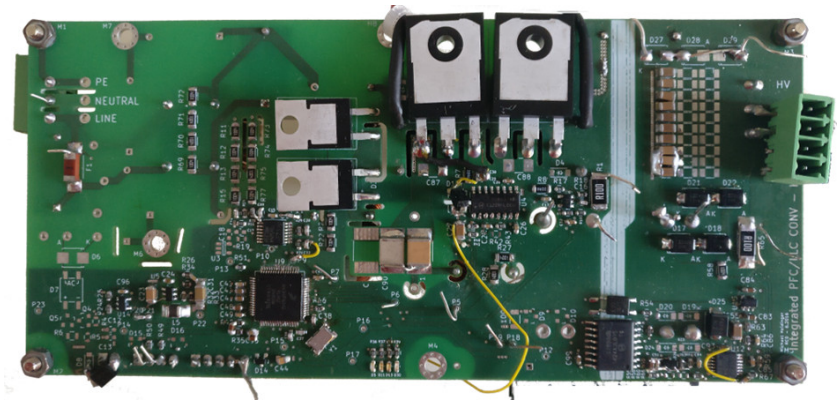
14.1 Construction Technique

The analysis platform is built on a four layer PCB. It includes the power electronics and the control on the common PCB. The three major prototyping platforms are shown in Figure 106. A Cortex M4F with floating point unit is used as DSP. All major components and testing configurations are denoted in Table 13.

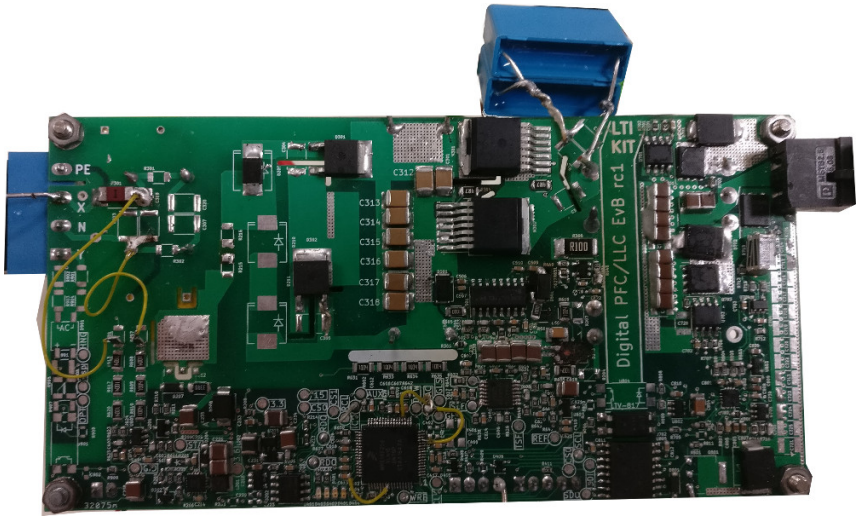
For a stable implementation of the proposed algorithm, it is mandatory to have accurate measurement with minimal noise and good accuracy. The topology can be operated using secondary side rectification to increase the efficiency. Therefore, mid-point rectification is used.

Type	Value
Switches	C3M0280090J
Diodes	C4D02120E
Gate Driver	Si8237
MCU	MKE14F256 - CortexM4F
Secondary Side ADC	ADS7947
SPI Isolation	Si8641
Reference	REF3030
U_{ac}	230Vrms
L_{I}	614µH
$n_{\mathrm{pri}}/n_{\mathrm{sec}}$	70:16
C_{1}	300nF
C_{link}	10µF 1200V
$\overline{U_{\mathrm{dc}}}$	400 V
U_{out}	15 V
$\overline{I_{out}}$	1 A

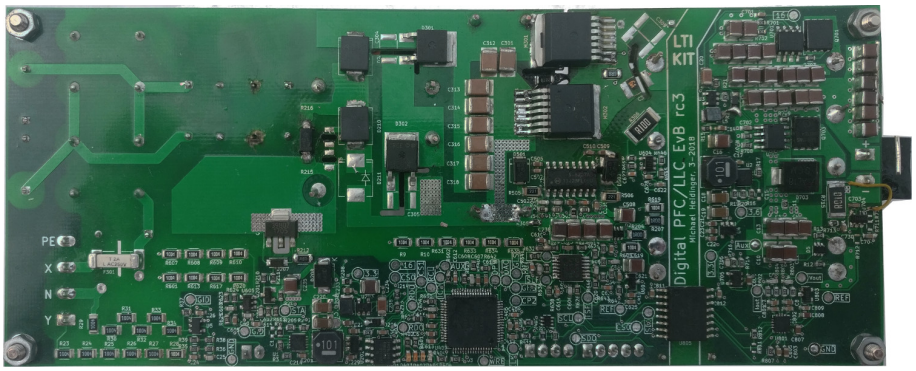
Table 13: SLC converter components, configuration and default test conditions.



(a) First generation



(b) Second generation



(c) Third generation

Figure 106: Analysis platform of different generations

14.2 Fundamental Measurements

As shown in the control section 8, the output current accuracy of the converter highly depends on the accuracy of the measurements. These measurements are: The DC Link voltage U_{dc}, the grid voltage U_{ac} and the output voltage $U_{\mathrm{C,out}}$. The internal measurements have to be accurate and need to have little noise. If internal measurements are inaccurate or noisy, this error would propagate through the transfer function and result in an inaccurate and noisy output current.

14.2.1 Measurement Setup for DC measurements

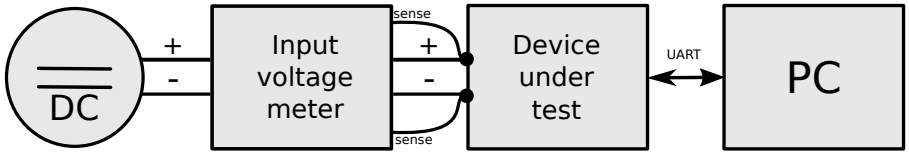


Figure 107: Basic measurement setup: The internal values are measured at the input with a voltmeter. The internal values are monitored using UART by the MCU Tracer. Both measurements values are compared with each other to calculate the measurement accuracy.

The measurement setup is shown in Figure 107. A constant voltage is fed to the tested variable. It's value is measured by a precision voltage meter, model Keithley 2100. The device under test, in this case the PFC/SLC measures the corresponding voltages. Both measurement variables are compared with each other and the measurement error is determined.

14.2.2 MCU Test

Before the actual measurements can be performed, the operation of the MCU must be verified. First, the board supply voltages are verified. Second, the operator verifies that the MCU can be programmed. Third, the controller is programmed to blink LEDs, next an RTOS is set up. It's supply voltage is verified, in our case 3.3 V. Then an RTOS "blink"-task is written that verifies the RTOS operation. The previously presented control algorithms are then one-after-another implemented.

14.2.3 Reference Voltage Accuracy

The reference voltage on the primary side and the secondary side have a nominal value of 3.0 V, as shown in Figure 92 on page 138. The ADC requires this measurement for an accurate conversion. As reference IC, the 'REF3030' is chosen, which has an initial accuracy of 0.2% [121]. The reference voltage is measured with two precision voltage meters (both Keithley 2100) and compared to the setvalue. The corresponding measurement results are depicted in Table 14.

Multimeter	Ideal Value	Primary Side	Secondary Side	Absolute Error PS	Absolute Error SS
Multimeter 1	3.0V	2.9990	2.9981	1.0 mV	1.9 mV
Multimeter 2	3.0V	2.9991	2.9981	0.9 mV	1.9 mV

Table 14: Reference voltage accuracy on primary side (PS) and secondary side (SS).

From the measurement it can be seen that the error is in the one to two millivolt range. The maximal measured error on one reference is 634 ppm. This means that the reference is highly accurate.

14.2.4 DC Link voltage accuracy

The SLC DC Link voltage U_{DC} is measured using a voltage divider, as shown in the voltage measurement section 9.1.4. In Figure 108, the error over the operating range is depicted absolutely and relatively to the measurement.

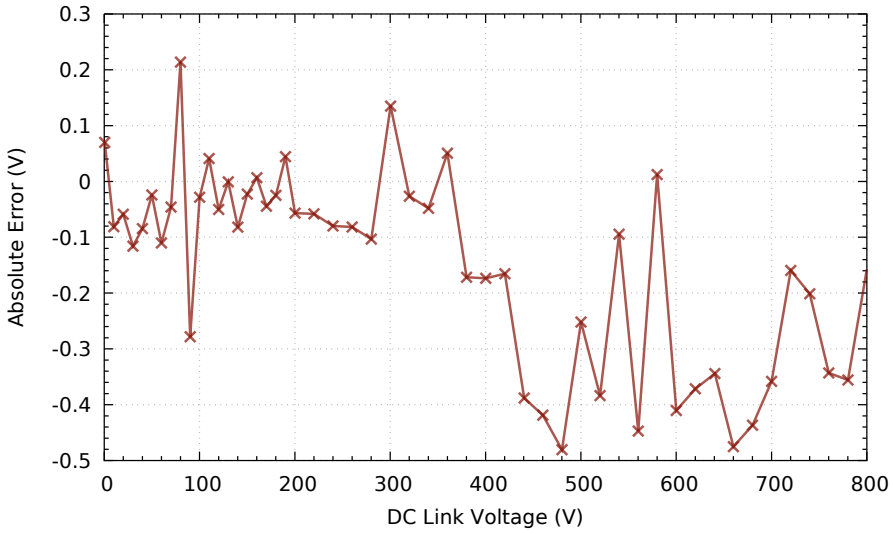
The absolute error is calculated by the following formula (14.1):

$$U_{\mathrm{err,abs}} = U_{\mathrm{DC,multimeter}} - U_{\mathrm{DC,ADC}} \tag{14.1}$$

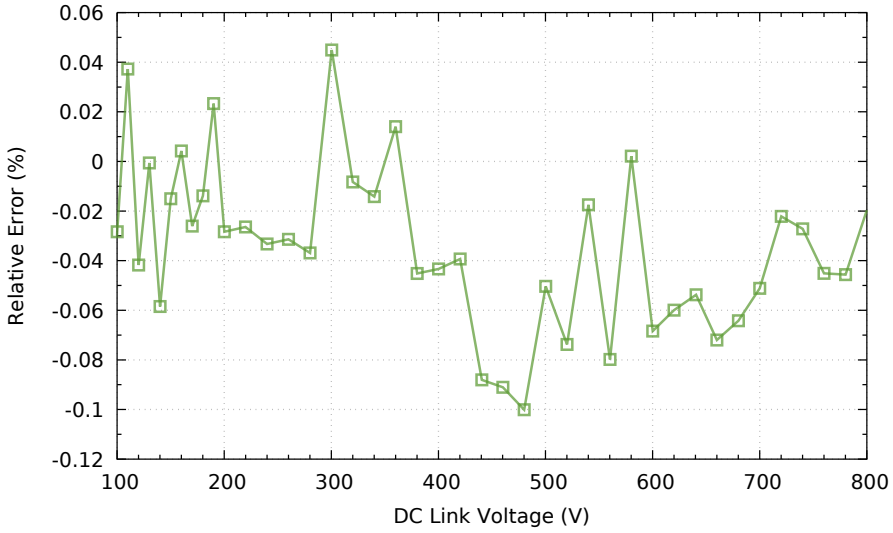
The relative error is calculated by the following formula (14.2):

$$U_{\mathrm{err,rel}} = \frac{U_{\mathrm{DC,multimeter}} - U_{\mathrm{DC,ADC}}}{U_{\mathrm{DC,multimeter}}} \tag{14.2}$$

The DC link is measured with a low noise source from 0 V to 410 V. Above 410 V to 800 V, the power supply is switched to a more noisy power supply. This can be observed in reduced accuracy. Considering a maximum voltage of 900 V, the measurement error is 0.055%. Overall, the measurement is very accurate. The overall absolute error is smaller than 0.5 V. As one voltage step equals 0.22 V, the effective accuracy is 2 LSB.



(a) Absolute voltage measurement error.

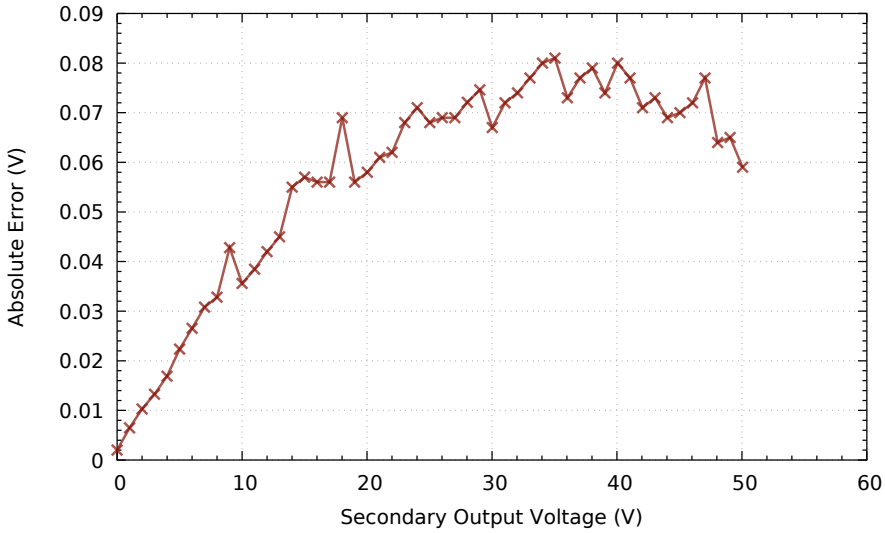


(b) Relative voltage measurement error.

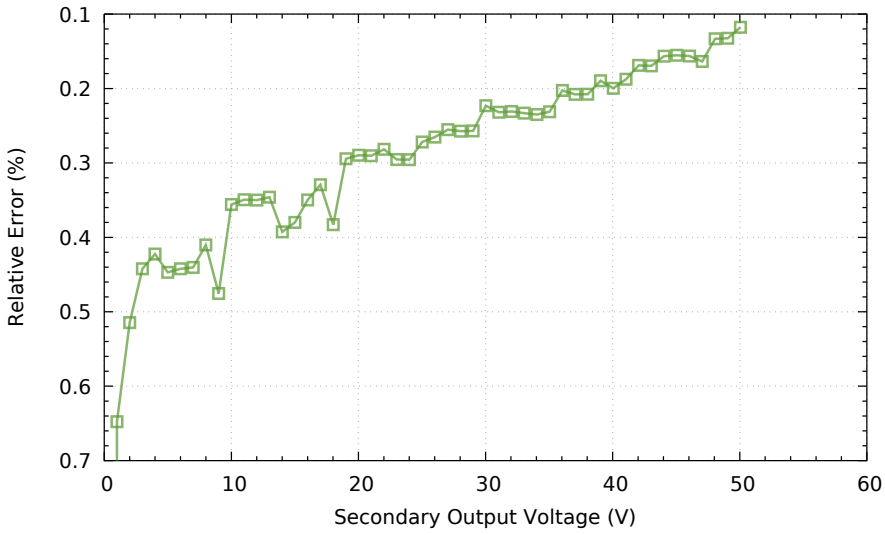
Figure 108: DC Link voltage measurement accuracy. Figure (a) shows the absolute voltage measurement error, while (b) shows the relative voltage measurement error. Above 410 V a high voltage power supply with increased noise is used that increases the measurement error.

14.2.5 DC output voltage accuracy

The output voltage U_{out} is measured using a voltage divider, as shown in the voltage measurement section 9.1.4. The MCU measures the output voltage over the isolated SPI interface, as discussed in section 9.4 on page 125. The actual conversion is done with the secondary side ADC ADS7947. It is a 12 bit ADC that samples with 2 MSPS [122].



(a) Absolute voltage measurement error.



(b) Relative voltage measurement error.

Figure 109: Output voltage measurement accuracy. Figure (a) shows the absolute voltage measurement error, while (b) shows the relative voltage measurement error.

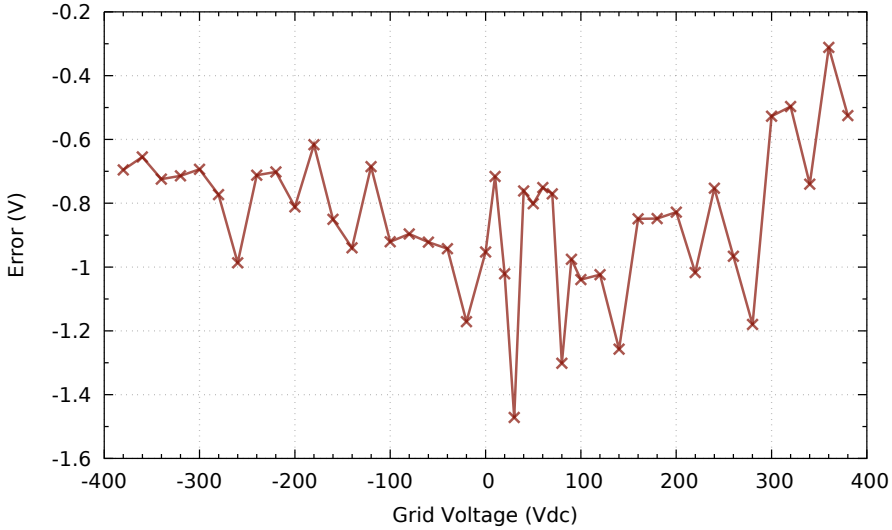
The DC output voltage in Figure 109 has a maximal error of less then 90 mV at the output. At an output voltage of 50 V, this equals 0.18%. In the low output voltage range, the relative error is relatively large, as the offset error is more significant. However, the absolute error indicates that also a

gain error is present. This gain error may result from the use of only 1% accurate resistors that were used for the design. Overall, the maximum relative voltage measurement error in the operation range is even in the low output voltage range below 0.7%, as can be seen in Figure 109.

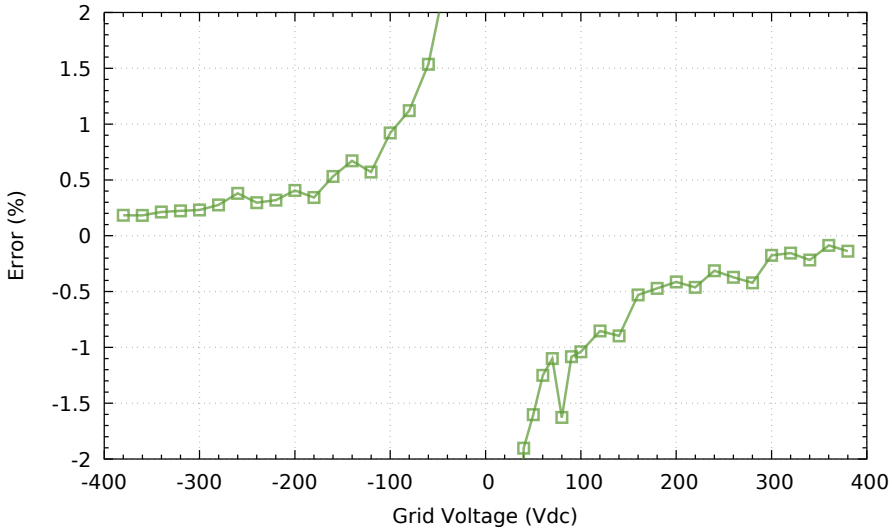
To further increase precision, 0.1% precision resistors could be used. However, for the current application the measurement accuracy is sufficient for the control loop.

14.2.6 AC Voltage accuracy applying DC at the input

The AC input voltage is measured with a differential amplifier according to Figure 81 on page 126 in section 9.4. From the absolute voltage measurement It can be observed, that an average negative offset of about 0.8 V is present. This constant offset is caused by the biasing circuit. For this circuit, no precision resistors were used. This error is filtered out by the downstream resonant observer, as discussed in section 9.7.



(a) Absolute voltage measurement error.

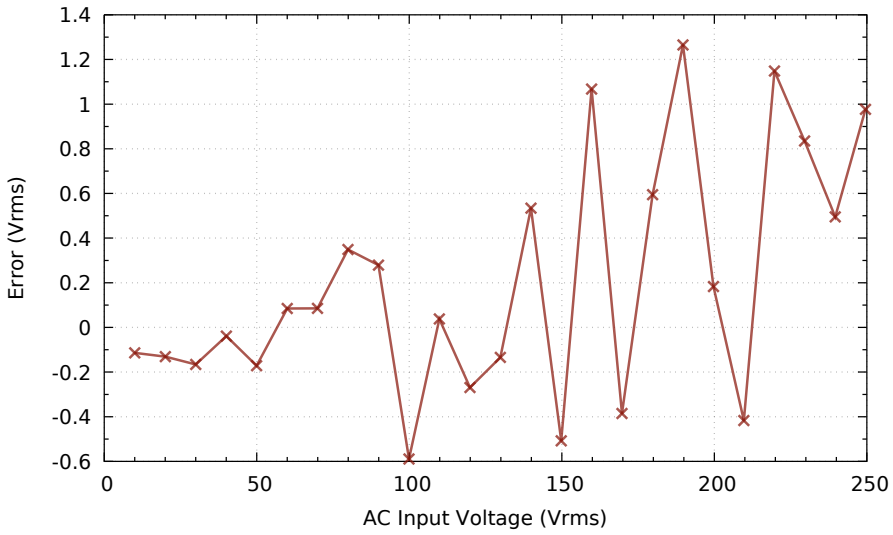


(b) Relative AC voltage measurement error.

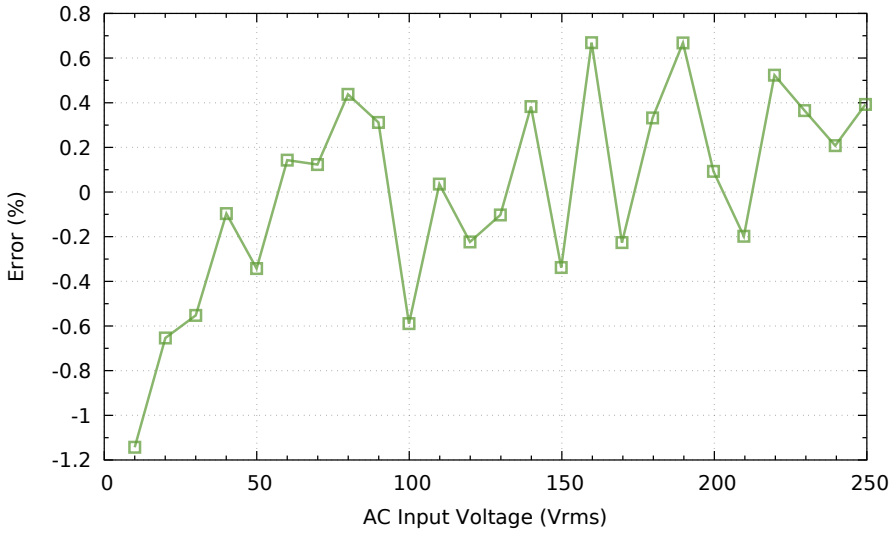
Figure 110: AC voltage measurement accuracy

14.2.7 Grid resonant observer accuracy

The grid simulator HBS Power source is used to synthesize an ideal grid. The AC voltage is measured with the voltage meter (Keithley 2100). It can be seen, that the grid voltage can be measured to plus-minus 0.7% accuracy in the typical operation range.



(a) Absolute voltage measurement error.



(b) Relative voltage measurement error.

Figure 111: The grid resonant observer voltage measurements accuracy is measured over the typical input voltage range

14.3 Series LC Converter

In this section only the series LC converter is analyzed, while in the next section the overall system is analyzed.

14.3.1 Test Setup

The test setup is shown in the following Figure 112. Time domain measurements are recorded with the LeCroy HRO66Zi 12Bit 500MHz oscilloscope. Average input- and output currents are measured by two Zimmer LM90 power meters.

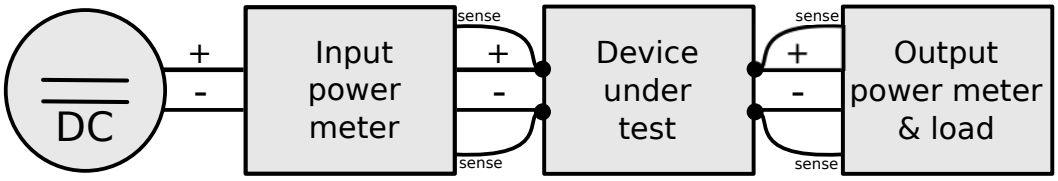


Figure 112: Measurement setup

14.3.2 Switching Waveform

The switching converter waveforms have been recorded by the means of an oscilloscope. The most important node for the switching behavior of the converter is the so called switchnode, abbreviated to "SWN". It is the center point of the half bridge, between the two switches S1 and S2. The switchnode is defined in Figure 21 on page 47. The theoretic operational waveform of the SLC converter is shown in Figure 70 on page 105.

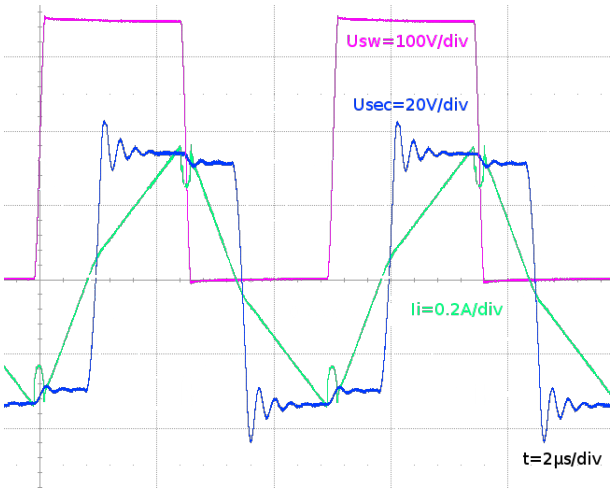


Figure 113: Switching waveform at switching frequency of 200 kHz.

An additional basic quality factor is the softness of the switching waveforms. No instant changes

should happen, which will cause high frequency noise. Additional details were discussed in section 4.3.1 on page 47.

For this switching waveform test the converter was supplied with a DC link voltage of 450 V, while the grid is not connected. The switching frequency was fixed at 200 kHz and the duty cycle at 0.5.

The switching waveform at $f_\mathrm{s} = 200\,\mathrm{kHz}$ is shown in Figure 113. Soft switching can be observed at the switchnode, reducing switching losses and noise. The U shaped current soft switching deformation of the inductor current is not considered in the prior analysis in Figure 70 and leads to subsequent error. The corresponding variables are named with respect to Figure 64.

14.3.3 Synchronous Rectification

Synchronous rectification is used to replace diodes by switched mosfets, as described in section 4.3.5 on page 50. Its efficiency depends on the correct setting of the gate pulses. The ideal synchronous rectification controller turns the gate drive signals on, when the current flows in the mosfets direction.

When the mosfets gate signal turns on too early, the mosfet may conduct in the opposite direction, resulting in increased transformer losses. When the mosfet is turned on too late, not the full energy saving potential is used. If in doubt, the controller should deactivate the mosfet gate, which then acts as a diode.

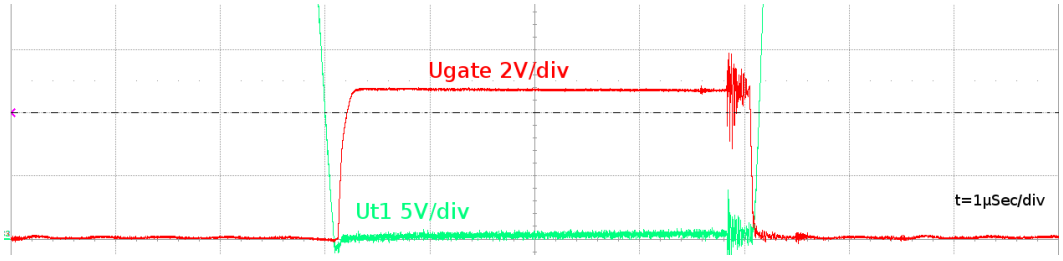


Figure 114: Synchronous rectification gate signals and transformer signals.

The synchronous rectification gate signal (U_gate) and the transformer output voltage tap (U_t1) are shown in Figure 114. When the transformer output voltage becomes slightly negative, the gate signal is turned on. With a delay less than 100 ns, this happens nearly instantly. A gate voltage controller that limits the output voltage to 5 V is chosen in this design. This proofs the proper operation of the synchronous rectification controller.

14.3.4 Current variation over output voltage

The output voltage is set by a variable load while the converter is operated in open-loop current mode with parameters according to Table 13. The input voltage U_dc was chosen to be a fixed voltage and

the output current I_{out} was chosen to a fixed value while the output voltage U_{Cout} was varied. For the subsequent test, the following test parameters are used:

$$U_{\mathrm{dc}} = 400\,\mathrm{V} \tag{14.3}$$

$$\overline{I_{\mathrm{out}}} = 1\,\mathrm{A} \tag{14.4}$$

For the green curve in Figure 115 the duty cycle is adjusted, while the switching period $t_{\mathrm{c}} = 10\,\mu\mathrm{sec}$ is held constant. The transformer transfer ratio was calibrated for the duty cycle adjustment and hence has less error.

For the blue curve the duty cycle is held constant at $D = 0.5$, while the frequency is adjusted. It can be seen that output voltage changes the output current at maximum 70 mA using frequency modulation. The rising output current slope can be explained by the impact of the deadtime that is not considered in the presented equation. When the switching period increases, the deadtime has less impact. As an increased output voltage requires a larger switching period, the output current finally increases. Then however, for the falling slope the previously assumed Taylor approximation is less accurate.

Using duty cycle modulation only 5 mA variation is observed, as the soft-switching has no influence on the output current.

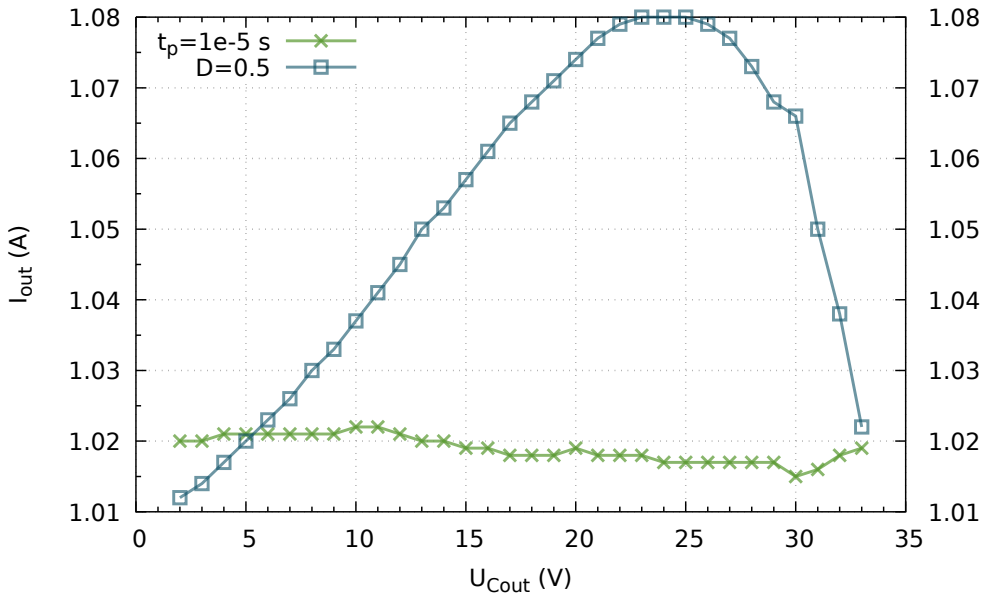


Figure 115: Output current variation over output voltage for duty cycle and frequency modulation.

14.3.5 Current variation over dc link input voltage

The input voltage is varied by means of a power supply while the converter is operated according to the conditions stated in Table 13. The input voltage U_{dc} was varied, while the set output current I_{out} and output voltage U_{Cout} was chosen to a fixed value.

$$U_{\mathrm{Cout}} = 15\,\mathrm{V} \tag{14.5}$$

$$\overline{I_{\mathrm{out}}} = 1\,\mathrm{A} \tag{14.6}$$

For the green curve in Figure 116, the duty cycle is adjusted, while the switching period $t_{\mathrm{c}} = 10\,\mu\mathrm{sec}$ is held constant. It can be observed that the higher the input voltage, the lower the output current.

The blue curve in Figure 116 shows the output current when the duty cycle is held constant at $D = 0.5$, while the frequency is adjusted. It can be seen that varying the input voltage introduces a relative error of up to 60 mA to the output current, when duty cycle modulation is used. On both curves an offset current can be observed.

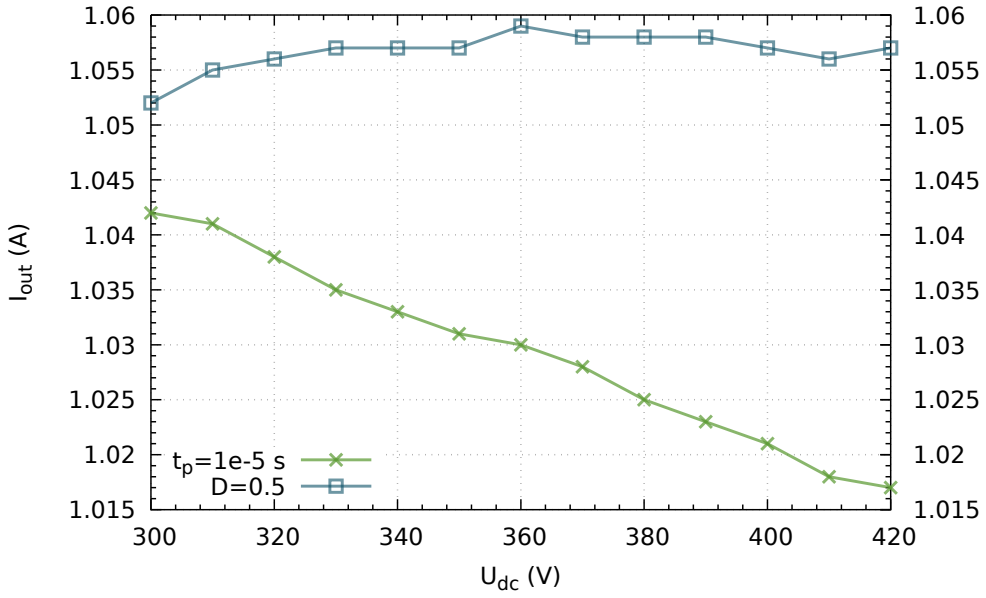


Figure 116: Output current over input voltage for duty cycle and frequency modulation.

14.3.6 DC Link Ripple

Typically a series LC converter obtains its power from a upstream PFC stage. The single-phase power factor correction requires rectification and thus double mains grid frequency ripple to operate. To

demonstrate the capabilities of the SLC converter to reject DC Link disturbances, the DC Link is fed with a varying DC Link voltage.

$$U_{\mathrm{dc}}(t) = 350\mathrm{V} + 100\mathrm{V}\sin(\omega \mathrm{t}) \tag{14.7}$$

The output current is controlled via the calibrated duty cycle and both waveforms are depicted in Figure 117. It can be seen that the duty cycle modulation rejects the dc link ripple variations. The measured relative open loop current error is only approx. 60 mA. The capability to reject high DC-Link disturbances allows the use of small value capacitors. This allows to replace electrolytic capacitors by film capacitors, allowing to increase lifetime significantly, as shown in section 6.

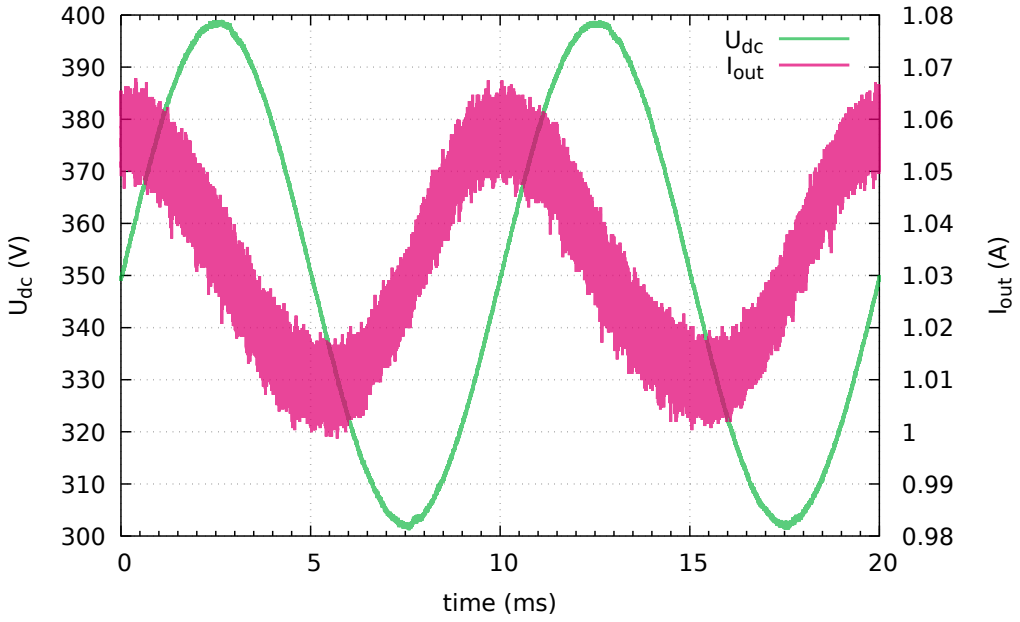
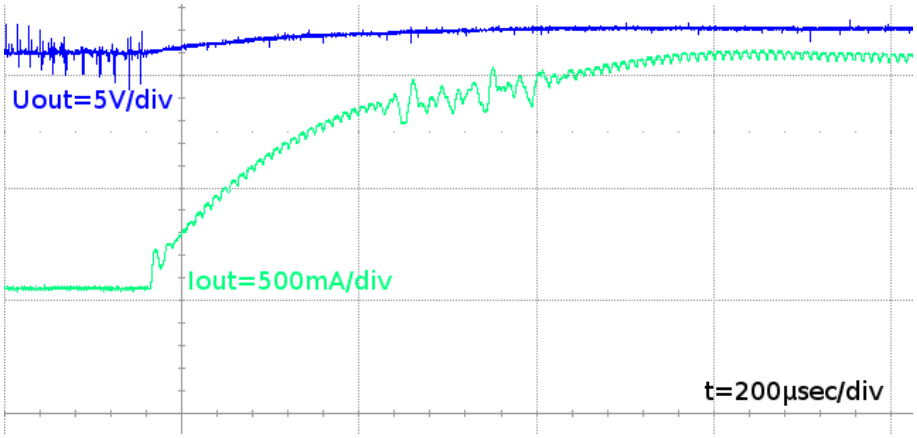


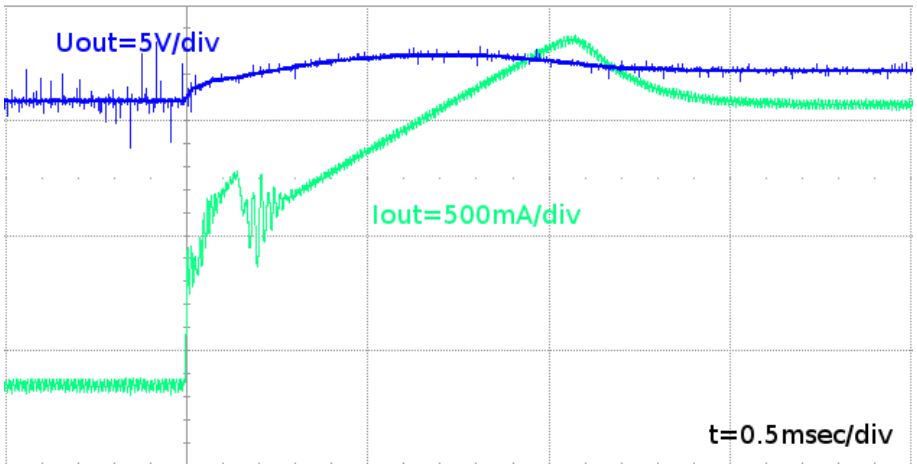
Figure 117: DC Link introduced current variations.

14.3.7 Open-Loop Step response

In Figure 118 the output current is increased from 0.5 A to 1.5 A. As a load a LED engine with a typical forward voltage between 17 V - 20 V is used. Two different approaches are analyzed: In 118a the switching period is modulated. The inductor current has a PT1 characteristic and reaches its set value within 600 µsec. The duty cycle adjustment is shown in Figure 118b. The adjustment is slower and an over-swing is present. It is assumed that the over-swing results from previous output voltage calibration. To reduce this overshoot, the output voltage calibration must be removed.



(a) $D = 0.5$



(b) $t_{\mathrm{p}} = 10\mu sec$

Figure 118: Open loop step response.

14.3.8 Efficiency

The converter efficiency is measured according to the specifications in Table 13 excluding the control power of 0.48 W. The green curve in Figure 119 and 120 shows the efficiency for duty cycle adjustment, while the blue curve shows the efficiency for the switching frequency adjustment. Switching frequency adjustment has a lower efficiency especially at lower loads. This can be explained by the switching frequency itself, as this modulation strategy requires higher switching frequencies at low load. Hence, additional switching losses are generated. Therefore, efficiency-wise, the converter should be operated using duty cycle modulation.

The peak efficiency of the SLC converter was measured to 97.8 %. However, the current parameters are not yet optimized for efficiency. If a lower input voltage and a higher output voltage were chosen, the efficiency could be increased. At high output voltages, the frequency control may reduce the output power slightly, reducing transferred power and thus efficiency.

All measurements are aquiered at one ampere output current, thus the output power is maximal 35 W. With 97.8% peak efficiency, the converter is highly efficient.

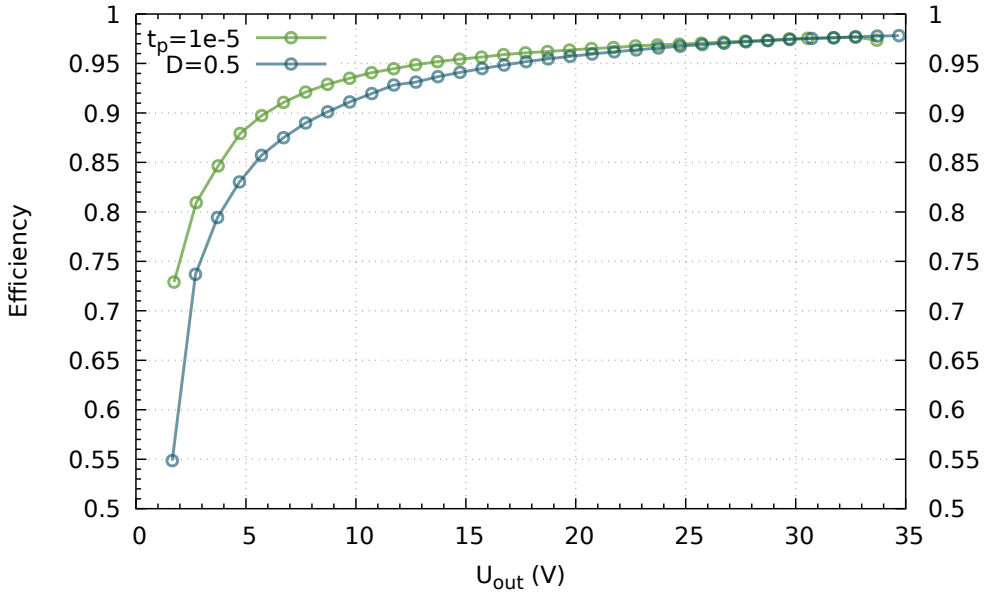


Figure 119: The efficiency is measured over the output voltage range at an output current of $I_{\mathrm{out}} = 1\,\mathrm{A}$.

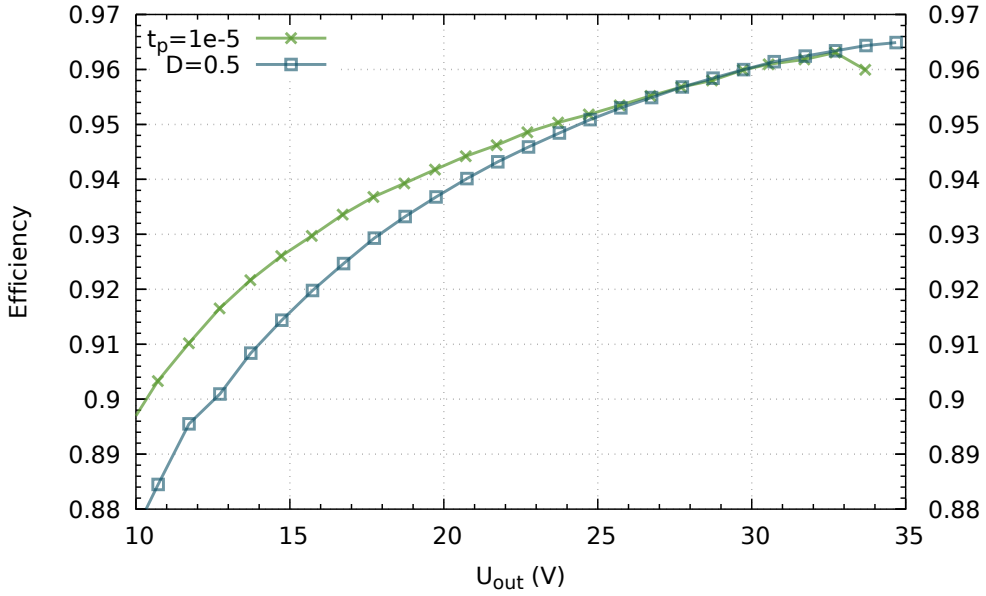


Figure 120: Efficiency at typical operating conditions at an output current of $I_{\text{out}} = 1\,\text{A}$.

14.4 PFC/SLC

The combined PFC/SLC converter measurements are summarized in this section.

14.4.1 Grid input current and LED output current

The typical grid input waveform is shown in Figure 121. It can be observed that an almost constant current is supplied to the LEDs, while the input current has a sinusoidal shape.

14.4.2 THD and Power Factor

The harmonics are measured according to IEC61000-3-2 Class C [7] and are shown in Figure 122. Class C applies for LED lighting devices. It can be clearly seen that all requirements are met.

The power factor is adequate, as it can be seen in Table 16. The measurements are made according to the specifications denoted in Table 15.

Additionally the power factor is plotted for different operating powers in Figure 123. It can be seen that at high load conditions the power factor is close to unity. The lower power factor at low load is explained by the EMC filter.

14.4.3 Efficiency

The efficiency of the converter is measured at different operating points. The measurement results are shown in Figure 124. The output voltage is varied, thereby simulating the different numbers of LEDs

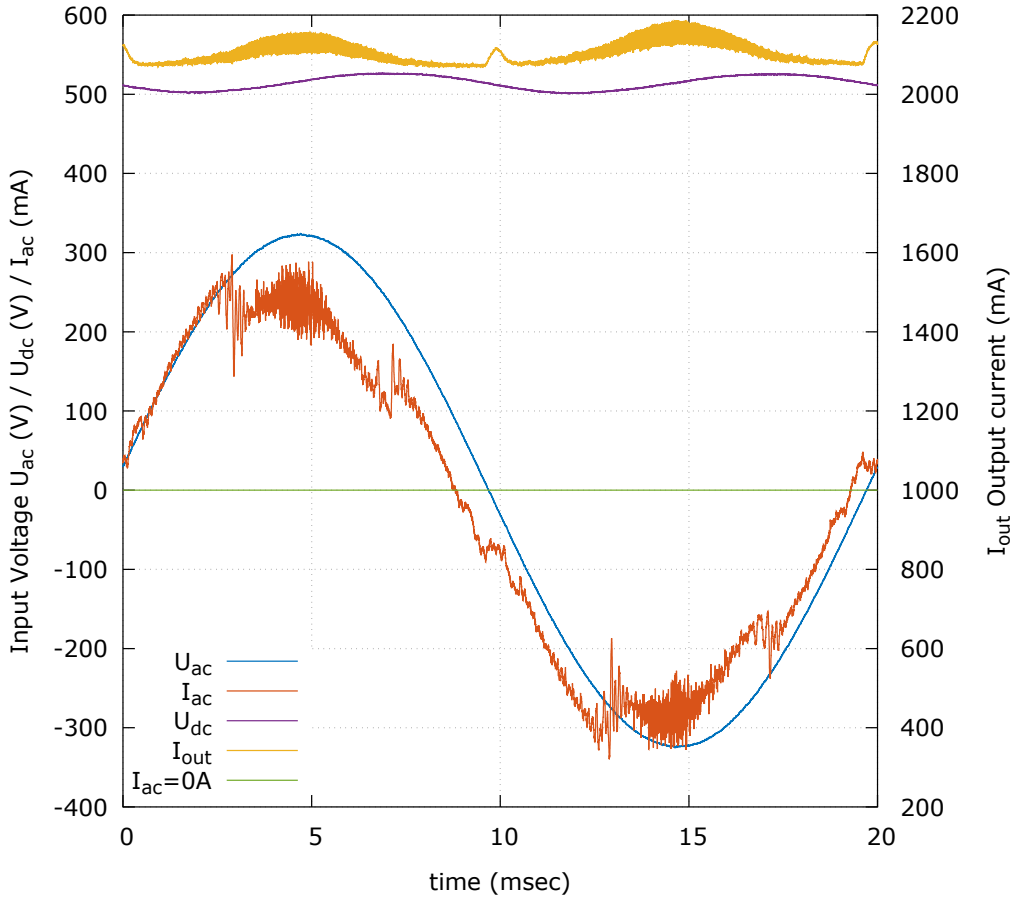


Figure 121: Waveforms of the PFC-SLC Converter

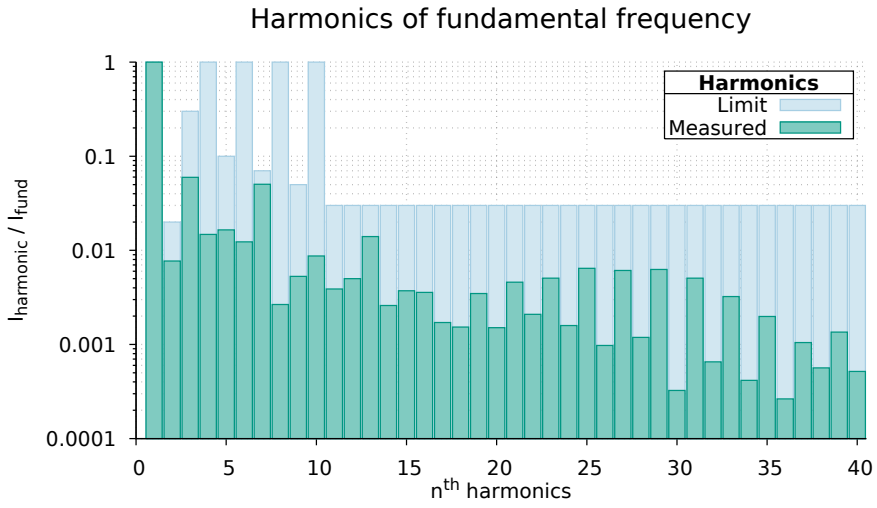


Figure 122: Harmonic measurements according to IEC6100-3-2 Class C

Type	Value
U_{ac}	230 Vrms
L_{I}	614 µH
C_1	100 nF
U_{DC}	520 V
U_{out}	18 V
I_{out}	2.3 A

Table 15: Measurement conditions for PFC/SLC converter THD measurement

Type	Value
S	46.4 VA
P	45.8 W
PF	0.978

Table 16: Apparent, real power and power factor measured for the SLC/PFC converter.

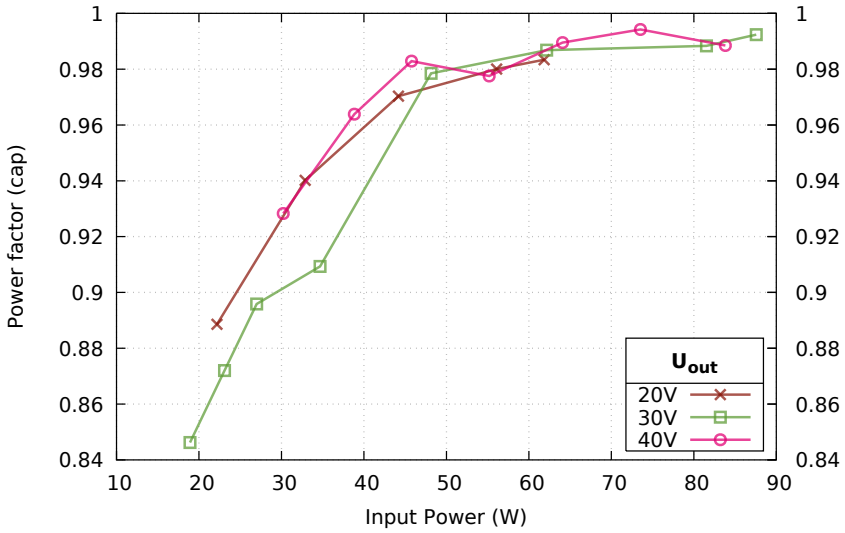


Figure 123: Power Factor of the PFC/SLC converter.

in a string. The individual string current is varied to simulate different dimming conditions.

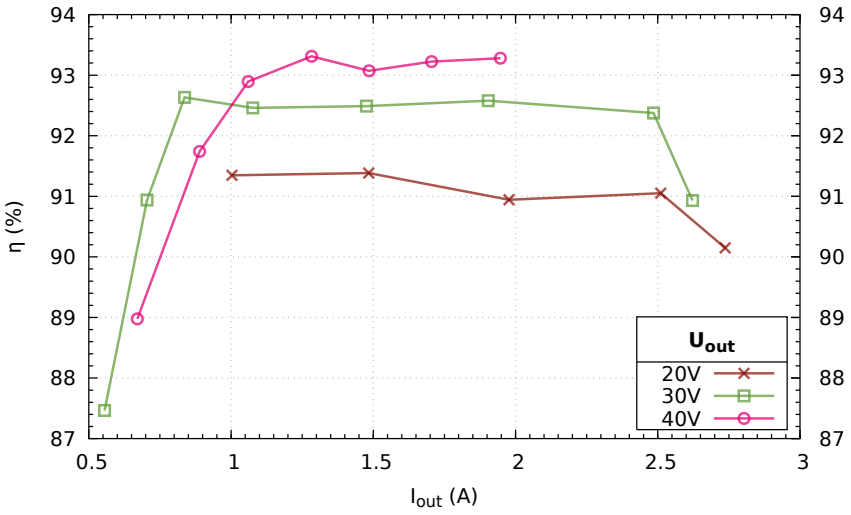


Figure 124: Efficiency of the PFC/SLC converter over output current.

14.4.4 Flicker based on Fluxdelta

Flicker is calculated based on the following formula:

$$F_p = \frac{\Phi_{max} - \Phi_{\min}}{\Phi_{max} + \Phi_{\min}} \tag{14.8}$$

Using the current measurement of Figure 121, a flicker level of 2.2% can be calculated. An observation did not show any visual flicker.

14.4.5 Flicker based on CFD

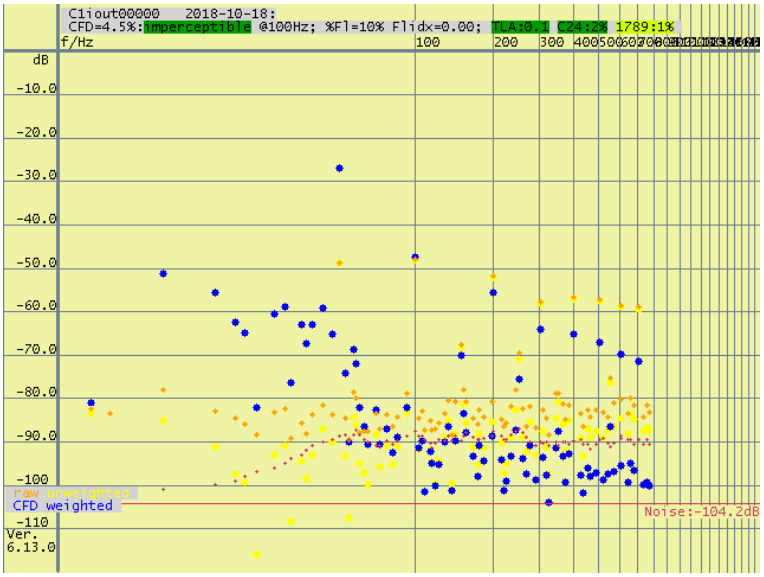
As the previous fluxdelta measurement does not consider the frequency, the CFD was used. The LEDs current is measured with an oscilloscope. The data is then transferred to the computer for the CFDWin analysis program.

According to Figure 125 a CFD of 4.5% was measured, which is categorized as “imperceptible”.

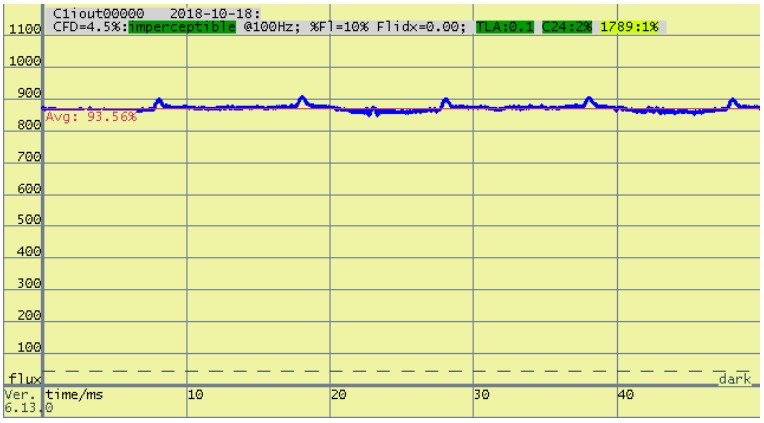
14.4.6 Thermal analysis

As previously discussed, heat accelerates the aging by a factor of two for every ten degrees in temperature increase. To identify susceptible components on the PCB, a thermal imaging camera is used to analyze the heat distribution of the SLC/PFC converter. The thermal image is reproduced in Figure 126.

The mosfet is identified as the hottest point in the thermal image. Next, the hotspot is measured by an accurate temperature sensor. The measurement concluded 44.2°C at ambient temperature of 23°C.

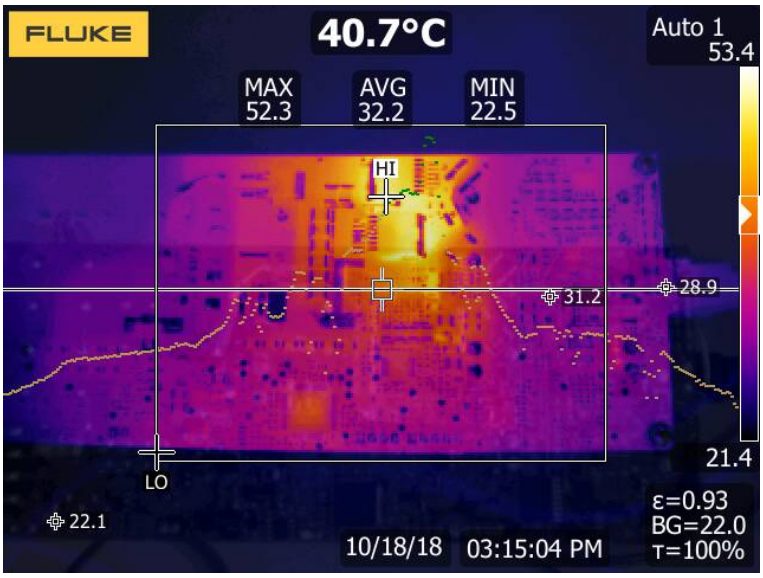


(a) Frequency Domain Analysis

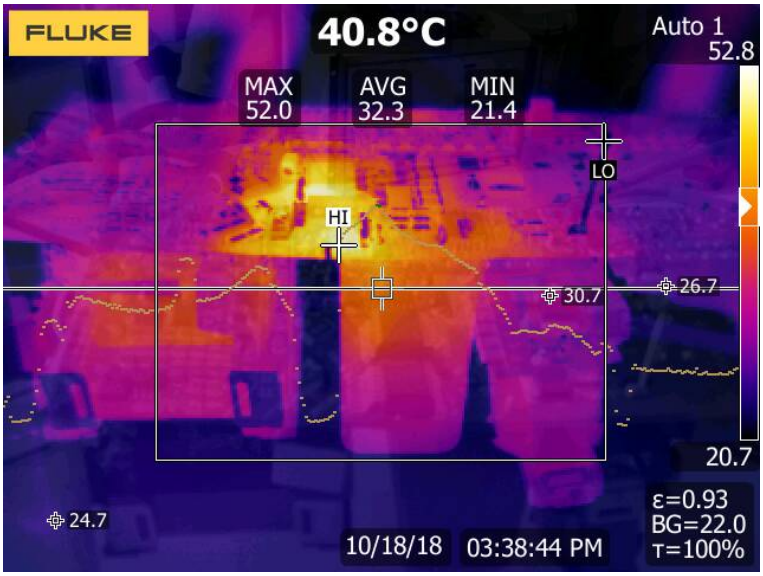


(b) Time Domain Analysis

Figure 125: CFD measurement results show that the flicker is imperceptible.



(a) Top View



(b) Top Side View

Figure 126: Heat distribution of the DC/DC converter

A temperature increase of 21 degrees over the ambient temperature shows that the thermal camera measurement is inaccurate. This is explained by the setting of an inaccurate emission coefficient. As it is denoted in Figure 126, the emission coefficient was chosen to be $\epsilon = 0.93$.

With the presented design, a cool operation of the converter could be demonstrated. Therefore, a long life of the converter should be possible.

15 Conclusion

The results of the work are summarized and the novelty of the work is emphasized.

15.1 Summary

After a historical introduction, the future of LED development was extrapolated using Haitz Law: The average light output per package increases by a factor of 10 every 20 years. LEDs are nowadays omnipresent for lighting. Long lasting lighting applications require a robust system design. Therefore, the typical failure issue of LED luminares was investigated: The power supply is with 52% of all failures the most likely issue. In some situations, it has to be exchanged 10 times before the lifetime limit of the LED module is reached.

A majority of LED driver failures are caused by the electrolytic capacitor. By the design-out of this electrolytic capacitor, it is estimated that the lifetime can be increased significantly. An estimation suggests a LED driver service life of 80 years. As these claims cannot be verified, they have to be treated with caution. A multitude of LED driver technologies and topologies were analyzed in section 4 and finally, after a holistic topology analysis, the SLC topology was chosen.

A sophisticated analysis of the discontinuous PFC and the series LC converter was conducted in the time domain. Thereby, each operation step was analyzed in detail. For both functional blocks, the author determined the average input current and the average output current respectively. As two variables have to be set, the AC input current and the DC output current at the same time, two degrees of freedom are required for control. The PFC and the SLC transfer functions are controlled by frequency and duty cycle. So, a solving algorithm was derived that calculates the frequency and the duty cycle as a function of input conductance, output current, and multiple measurement values. By monitoring the DC Link voltage for control, a high rejection against input voltage and output voltage changes is achieved. Thus, it was possible to use lower value film capacitors, extending the converter's lifetime significantly.

For the proposed specialized control algorithm several voltages and currents must be measured and digitally conditioned. E.g. the DC Link voltage is measured and filtered first analog and then digitally by a resonant observer to cancel the double mains grid frequency ripple. Further, a method for galvanically isolated voltage measurements is proposed. It has a high sample rate of currently up to 2 megasamples per second. By this, the controller can be placed on the primary side, while the secondary side can be measured accurately. Based on the measurements, protection concepts are proposed to avoid fatal failures during development and operation.

To increase the number of LEDs in an LED engine, for instance, to use smaller MidPower LEDs

instead of HighPower LEDs, a novel circuit for paralleling LEDs was presented. It measures the individual string currents, creates an average of the individual string currents and feeds it back to the paralleling controllers. By that, LEDs can be safely paralleled without compromising efficiency.

For the operation of the converter, a sophisticated auxiliary power supply concept is developed. As all controls are implemented in the digital domain, in-depth software engineering is required to ensure real-time performance of the CPU. Non-adequate control implementation results in glitches that lead to an unstable control loop.

The measurement section demonstrates that a long-lasting, flicker-free LED driver has been developed. Its grid input current has a sinusoidal shape, while providing a virtually constant output current to the LED. The PFC/SLC converter's efficiency is measured to 93%.

15.2 Innovations and discoveries

In this work, well tempered operation of series LC converters was realized. A precise, fast and beneficial DC transfer function for the open-loop current control was demonstrated. The digital control rejects DC link disturbances and thus allows the use of small value capacitors. By this new control technique the required DC-link capacitance value may be chosen smaller. As electrolytic capacitors have approximately a ten times higher energy density, they can be replaced by physically larger film capacitors, without significantly increasing the overall build volume. Film capacitors in general allow a significant lifetime increase compared to electrolytic capacitors.

Additionally, a novel circuit for efficiently sharing the LED current is presented. This circuit allows to construct high-efficient streetlamps using MidPower LEDs.

15.3 Patents

Two applications for patents were submitted based on the present work:

- The paralleling of LEDs is described in section 5: The patent has the following registration number DE 10 2017 203 801 B3 2018.03.08.
- The series LC converter regulation formula by duty cycle and frequency, including the high DC Link ripple rejection, which was discussed in section 7. The patent has the following registration number DE 10 2018 216 749.4 entitled "Verfahren zur Steuerung eines Serien - Resonanz - Wandlers"

15.4 Challenges for the future

Currently the topology requires a significant number of components. Therefore, the system design risks to be cost-intensive. However, the author believes that the functional integration will keep moving forward and that this issue will be negligible in the near future.

15.5 Acknowledgment

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