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CZTSe solar cells prepared by co-evaporation of multilayer Cu–Sn/Cu,Zn,Sn, Se/ZnSe/Cu,Zn,Sn,Se stacks

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Abstract

In this work, thin-film kesterite $\text{Cu}_2\text{ZnSnSe}_4$ (CZTSe) solar cells were prepared using a novel precursor configuration employing co-evaporated layer stacks of Mo/Cu–Sn/Cu,Zn,Sn,Se/ZnSe/Cu,Zn,Sn,Se. It is found that this sequential deposition of the constituents leads to the formation of large CZTSe grains on the surface and fine grains at the Mo interface of the absorber, respectively. Prototype CZTSe solar cells using this stacked approach achieve power conversion efficiencies of up to 7.9% at an open-circuit voltage of 430 mV and a fill-factor of 62%. The analysis of temperature-dependent current density–voltage characteristics indicates that bulk Schottky–Read–Hall recombination is the dominant recombination mechanism for the devices fabricated from the proposed stack. In addition, the influence of pre-annealing of each stacked layer on the absorber growth and device performance is examined and discussed.

Supplementary material for this article is available [online](#)

Keywords: thin-film solar cells, kesterite, open-circuit voltage, fill-factor

(Some figures may appear in colour only in the online journal)

1. Introduction

As a result of the United Nations climate summit in Paris, an agreement to decrease CO_2 emission, the main contributor to global warming, was approved in 2016. Special attention was paid to the electrical sector and urgent actions were set to cut down the utilization of carbon-based fuel. The required measures are enabled through the development of robust renewable energy technologies such as wind energy and

photovoltaics (PV). The latter provides more than 1% of the global energy, with around 7%–8% in some of the developed countries [1]. Commercially, silicon (Si) based PV technologies contribute more than 94% to the PV market share while the share of thin-film technologies is below 6% [2]. Despite the highly optimized fabrication process of Si-based devices with laboratory efficiencies (η) up to 26.9% for monocrystalline Si and 22.3% for multicrystalline Si, respectively [3], this approach suffers from poor light absorption due to the indirect bandgap of the Si absorber. Consequently, a high absorber thickness is required in order to achieve good efficiencies, thus limiting the utilization of Si technology for flexible applications. Thin-film technologies such as cadmium telluride (CdTe), $\text{Cu}(\text{In,Ga})(\text{S,Se})_2$ (CIGS), and more recently

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hybrid organic–inorganic perovskites have been developed to overcome this limitation [4]. However, considering the recent classification of some of the elements used in these approaches as critical raw materials (CRM) [5, 6] by the European Commission, there is an interest in the development of environmentally friendly CRM-free PV materials [6]. Kesterite $\text{Cu}_2\text{ZnSn}(\text{S},\text{Se})_4$ (CZTSSe) and $\text{Cu}_2\text{ZnSnSe}_4$ (CZTSe) are a cost-effective approach in this category (see table S1, available online at stacks.iop.org/PS/94/105007/mmedia) and promising to challenge the current dominance of the well-established CIGS and CdTe thin-film PV technologies. To date, power conversion η of up to 12.6% [7] and 11.6% [8] were demonstrated for CZTSSe and CZTSe, respectively, which is still significantly lower than the record η reported for CIGS solar cells (22.9% [9]) and CdTe solar cells (22.1% [3]). Narrowing this gap requires a better control of absorber growth and defect formation at both the front and rear interfaces [10].

Commonly, a CZTSe or CZTSSe absorber is prepared via a two-step process, where (i) a precursor is deposited by either a wet-chemical or a vacuum-based process, followed by (ii) a high-temperature ($>500^\circ\text{C}$) re-crystallization step in a high-pressure chalcogen atmosphere [7, 11]. The high pressure chalcogen atmosphere is utilized to suppress decomposition of the absorber at the surface [11]. As a result of the annealing process, a thicker layer of MoSe_2 or $\text{Mo}(\text{S}, \text{Se})_2$ is formed between the absorber and Mo back contact that can lead to a high series resistance (R_s) [12]. Moreover, it is reported that a reaction between CZTSe and Mo back contact promotes (i) the formation of a thicker MoSe_2 layer as well as (ii) unwanted phases and defects, which lead to enhanced non-radiative recombination [13]. The latter reduces the η , primarily the open-circuit voltage (V_{oc}) and fill-factor (FF).

In order to improve the quality of the Mo/CZTSe interface, it is crucial to minimize the interaction between Mo and CZTSe [12, 14]. For instance, Li *et al* proposed a temporary barrier formed by pre-annealing of Mo/Zn/Cu/Sn/Cu metal precursors before selenization to suppress the interaction of CZTSe and Mo back-contact and, at the same time, act as a Se diffusion barrier [12]. The pre-annealing process provides a precursor configuration with a depth composition gradient such as Zn, $\text{Cu}_5\text{Zn}_8/\text{Cu}_6\text{Sn}_5$. We interpret these findings such that the presence of different alloys in the precursor might not only act as a temporary barrier but also trigger a different reaction path towards the formation of the CZTSe absorber. Furthermore, Brammertz *et al* [15] and Lai *et al* [16] experimentally revealed the importance of the precursor configuration for CZTSe growth and device performance. Brammertz *et al* [15] utilized a $\text{Cu}_{10}\text{Sn}_{90}/\text{Zn}/\text{Cu}$ configuration, demonstrating a device with η up to 9.7%. Based on those considerations, in this study we introduced a precursor stack utilizing a configuration of Mo/Cu–Sn/Cu, Zn, Sn, Se/ZnSe/Cu, Zn, Sn, Se (see figure 1) with the motivation of: (i) allowing formation of CZTSe via a ternary path due to the presence of a Cu–Sn alloy at the back interface; and (ii) a delayed formation of CZTSe at the Mo back contact to mitigate an early interaction of CZTSe and Mo, consequently possibly reducing the decomposition of CZTSe



Figure 1. Schematic diagram for a stacked precursor sample.

at the rear interface. Using the proposed precursor configuration, devices with η up to 7.9% could be demonstrated. Moreover, we investigated the influence of pre-annealing of each stacked layer on the absorber growth and device performance.

2. Materials and methods

2.1. Fabrication

Mo/Cu–Sn/Cu,Zn,Sn,Se/ZnSe/Cu,Zn,Sn,Se precursors were deposited via co-evaporation at a temperature of approximately 100°C onto Mo-coated soda lime glass (Mo/SLG) substrates coated with a 550 nm Mo back contact. Low deposition temperatures were used in order to minimize the volatilization of Sn and Se during precursor growth. The precursors were prepared using a deposition rate of 1.35 nm min^{-1} for Cu, 1.25 nm min^{-1} for Zn, 2.15 nm min^{-1} for Sn, and 3.7 nm min^{-1} for Se, targeting a precursor with an average bulk elemental composition of $[\text{Cu}]/([\text{Zn}] + [\text{Sn}]) \sim 0.71$, $[\text{Zn}]/[\text{Sn}] \sim 1.01$, and $[\text{Se}]/([\text{Cu}] + [\text{Zn}] + [\text{Sn}]) \sim 0.50$. This precursor composition was chosen, since it could be expected to lead to efficient devices as from our previous studies utilizing a co-evaporated homogeneous precursors [11] as well as reported in the literature [8, 17]. The precursor architecture is depicted in figure 1. The Cu–Sn seed layer with metal ratio $[\text{Cu}]/[\text{Sn}] = 1.44$ was alloyed *in situ* at a temperature of 250°C for 15 min before deposition of the Cu, Zn, Sn, Se/ZnSe/Cu, Zn, Sn, Se stack. In order to obtain CZTSe absorber layers, the precursors were thermally annealed in a Se + N_2 atmosphere utilizing a semi-sealed graphite box containing 180 mg of Se placed in a custom-built rapid thermal annealing tube furnace. Prior to annealing, the furnace was evacuated to a base pressure of 10^{-6} mbar and subsequently flooded with N_2 up to a pressure of 250 mbar. Using a ramp rate of $40^\circ\text{C min}^{-1}$, the furnace was heated to a temperature of 540°C , held for 10 min and cooled down to room temperature. Finally, devices were fabricated by depositing 50 nm CdS via chemical bath deposition, followed by sputtering of 50 nm *i*-ZnO and a 400 nm ZnO:Al transparent conducting oxide. Finally, the total active area of 0.16 cm^2 was defined by mechanical scribing.

2.2. Characterisation

X-ray diffractometry (XRD) analysis was carried out using Cu-K α radiation ($\lambda = 1.54184 \text{ \AA}$) in a Bragg-Brentano geometry (Bruker D8 Discover). The absorber morphology was analysed using a scanning electron microscope (SEM, Carl Zeiss SUPRA-55VP) with 2 kV acceleration voltage. The bulk composition was measured using energy-dispersive x-ray spectroscopy, attached to a SEM (XL30 SFEG Sirion, FEI) with 10 kV acceleration voltage. The depth-dependent composition profile was measured using glow-discharge optical emission spectroscopy (GDOES, GDA750, Spectra) with the radio frequency (RF) power of 26 W and an Ar gas pressure of 500 Pa.

Current density–voltage (J – V) characteristics were measured using a sourcemeter (Keithley 2400) and a solar simulator (WACOM single Xe lamp, class AAA) at an intensity of 100 mW cm^{-2} . R_s was evaluated by a linear fit to the slope of the J – V curve under illumination. Other diode parameters, such as the dark saturation current density (J_0) and diode ideality factor (n_{id}), were extracted from the dark J – V data as described by Neuwirth *et al* [17]. Temperature-dependent current density–voltage (J – V – T) measurements were performed in a cryostat (KONTI-IT-Cryostats, CryoVac) between $T = 300$ and 150 K in 10 K intervals. To investigate the bandgap of the CZTSe absorber, electroreflectance (ER) measurements were performed on the complete devices using a custom-built system. Light from a 250 W quartz tungsten-halogen lamp was dispersed in a 0.32 m focal-length monochromator with a 6001 mm^{-1} grating. Diffuse reflected light was collected via lens system and detected by a thermoelectrically cooled InGaAs photodiode. Using a function generator, a square wave modulation in reverse bias ($f \sim 223 \text{ Hz}$, $U \sim -1.5 \text{ V}$) was applied and the relative change of the reflected intensity ($\Delta R/R$) under an angle of incidence of 30° and an angle of detection of 0° was measured utilizing a lock-in technique. Further details may be found in our previous publication [18].

3. Results and discussion

In order to evaluate the main material phases of the precursors, XRD measurements were performed (see figure 2). As can be seen, the *in situ* alloyed Cu–Sn seed layer (black line) is composed of the alloys of CuSn (PDF-number 00-045-1488), $\text{Cu}_{10}\text{Sn}_3$ (PDF-number 03-065-2064), and Cu_6Sn_5 (PDF-number 00-047-1575). The XRD scan after deposition of the full stack is shown in figure 2 (red line). For comparison, the corresponding scan of a simple co-evaporated (Cu, Zn, Sn, Se) layer is shown in figure S1. Based on the peaks and positions, we observed that both layers contain the selenide compounds ZnSe (PDF-number 01-080-0021), Cu_2SnSe_3 (PDF-number 01-070-8930), SnSe_2 , (PDF-number 01-089-3197), and CuSe, together with the alloys Cu_6Sn_5 , Cu_5Zn_8 (PDF-number 00-025-1228), $\text{Cu}_{10}\text{Sn}_3$, and Cu_3Sn (PDF-number 00-001-1240). The presence of the alloys in both precursors further indicates that the alloying process already starts during precursor growth. Furthermore, we

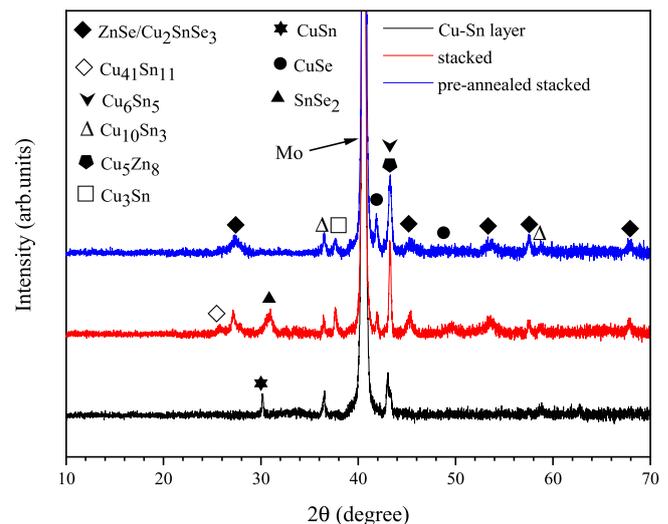


Figure 2. XRD scans of a Cu–Sn seed layer, a stacked, and a pre-annealed stacked precursor, respectively.

noticed an additional peak in the XRD scan of the stacked precursor, which is related to the alloy $\text{Cu}_{41}\text{Sn}_{11}$ (PDF-number 00-030-01510). Since the $\text{Cu}_{41}\text{Sn}_{11}$ peak is not visible in the simple co-evaporated precursor (see figure S1), it could be created from the Cu–Sn seed layer due to the diffusion of Se in the stacked precursor.

For some samples, we intentionally *in situ* pre-annealed each individual layer of the stack (‘pre-annealed stacked precursor’). The pre-annealing conditions of each layer are the same as for the Cu–Sn seed layer (temperature of 250°C for 15 min). As illustrated in figure 1, the XRD scan of these structures is somewhat different compared to the unannealed stacked precursor. As displayed in figure 2 (blue line), the XRD peak related to $\text{Cu}_{41}\text{Sn}_{11}$ and SnSe_2 disappeared and a very weak peak related to the CuSn phase re-emerged. Based on this observation, we conclude that pre-annealing of each stack lead to the formation of a different precursor configuration compared to the unannealed stacked case.

In order to study the effect of initial precursor composition on the resulting absorber morphology, SEM cross-sectional images were taken of the complete CZTSe devices prepared from stacked and pre-annealed precursors, respectively (figures 3(a) and (b)). Both absorbers are very compact and associated with a 1200 nm thick layer of MoSe_2 at the Mo interface. This demonstrates that utilizing a 100 nm thick Cu–Sn alloyed seed layer can at best delay but not fully prevent Se diffusion to the Mo rear contact. The thickness of the CZTSe absorber was found to be $1 \mu\text{m}$. Concerning grain size, the absorber prepared from the stacked precursor showed a mixture of larger grains at the surface and fine grains at the interface to the MoSe_2 layer, respectively, suggesting that grain growth starts at the surface in the stacked precursor with non-uniform element distribution. This agrees with similar findings of Zhang *et al* [13]. In contrast to that, the absorber prepared from the pre-annealed stack shows a more uniform and homogeneous morphology.

To investigate the influence of pre-annealing of each stack on the elemental composition distribution in the CZTSe

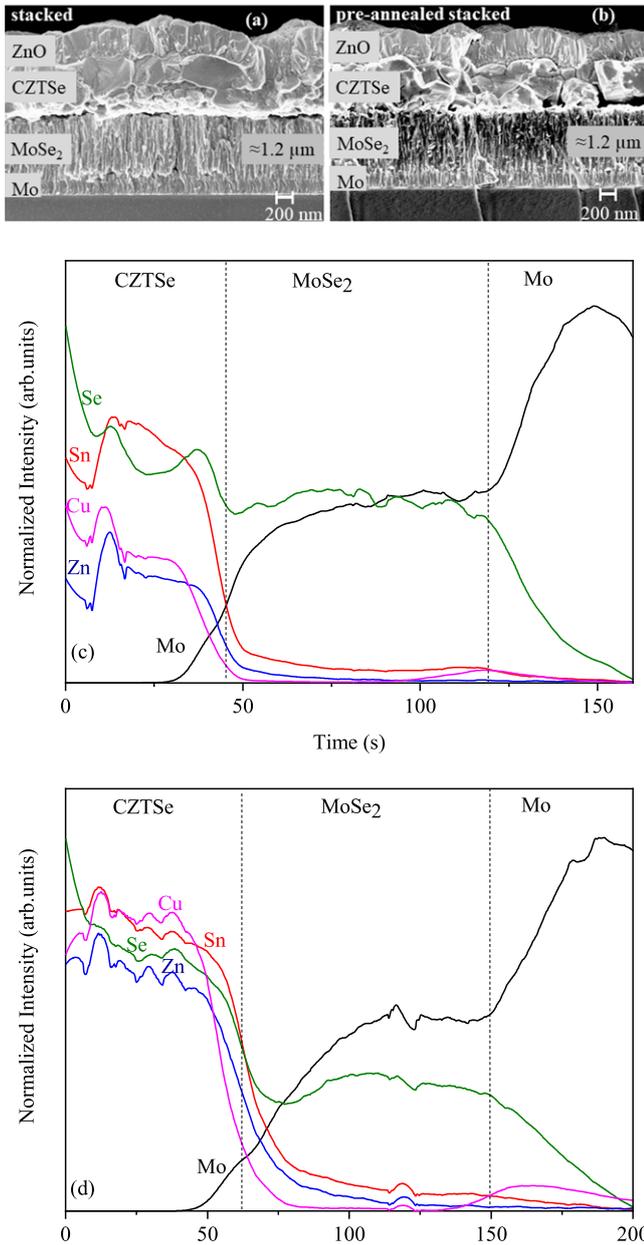


Figure 3. Cross-sectional SEM images of CZTSe solar cells (a), (b) and GDOES depth profiles of absorbers (c), (d) for samples based on stacked (a), (c) and pre-annealed stacked precursors (b), (d), respectively.

absorber layer, GDOES measurements were performed on the CZTSe layer prepared from both approaches. As presented in figures 3(c) and (d), the elemental distribution is more homogeneous for the CZTSe absorber prepared from the pre-annealed stacked compared to the stacked absorber. Consistent with the morphology studies, this suggests that pre-annealing leads to an improved homogeneity.

The dark and illuminated J - V curves for the champion solar cells prepared from stacked precursors and pre-annealed precursors—both from a total of 6 solar cells with an active area of 0.16 cm^2 , (full data shown in table S2)—are displayed in figure 4 with the corresponding diode parameters in table 1. The champion solar cell from the stacked precursor demonstrated a

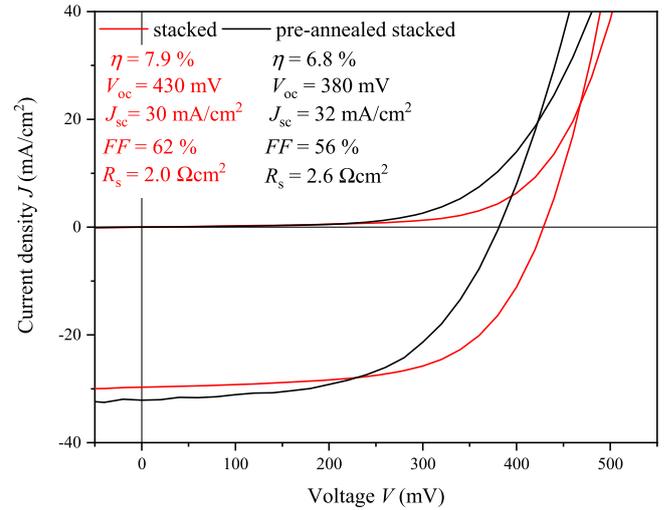


Figure 4. Comparison of the dark and illuminated J - V curves for the champion solar cells fabricated from stacked and pre-annealed stacked precursors, respectively.

Table 1. Extracted dark diode parameters from fits to experimental J - V data and the bandgap for two devices prepared from stacked and pre-annealed precursors, respectively.

Sample	n_{id}	J_o (mA cm^{-2})	R_s ($\Omega \text{ cm}^2$)	E_g (eV)
Stacked	1.7	1.1×10^{-6}	2.0	1.04
Pre-annealed stacked	1.8	2.8×10^{-6}	2.6	1.02

maximum η of 7.9% with V_{oc} , FF, and J_{sc} of 430 mV, 62%, and 30 mA cm^{-2} , respectively. The J_{sc} of our champion solar cell is somewhat lower than that of the high-efficiency pure-Se-based kesterite solar cells reported in the literature [8, 19]. We account this to the fine grains at the Mo interface of the device shown in figure 3(a), which can act as leakage pathway for the generated photocurrent, consequently reducing the photogenerated current within the device [20]. This hypothesis is supported by the fact that the J_{sc} of devices prepared from pre-annealed stacked precursors is somewhat higher (here 32 mA cm^{-2}) than that of the stacked precursor (see figure 4). However, the V_{oc} and FF of the cell decreased to 380 mV and 56%, respectively. We hypothesize that this decrease might be related to the decrease in grain size of the pre-annealed stacked sample compared to the stacked sample as shown in figures 3(a) and (b). It is known that smaller grains, resulting in a higher density of grain boundaries, can lead to a higher defect density, thus promoting recombination losses and contributing to a V_{oc} loss [21]. The solar cells prepared from stacked precursors achieved a minimum V_{oc} deficit of 610 mV and those from pre-annealed stacked precursors demonstrated a V_{oc} deficit of 640 mV. This indicates that the device performance from both approaches is limited by either the CdS/CZTSe interface, bulk recombination, or Mo/MoSe₂/CZTSe back-contact recombination [19, 22]. In order to investigate this aspect, J - V - T measurements were performed to analyse the nature of the dominant recombination mechanism in our devices. We investigated V_{oc} versus temperature (see figure 5), which is a well-established route to determine the activation energy (E_A) of

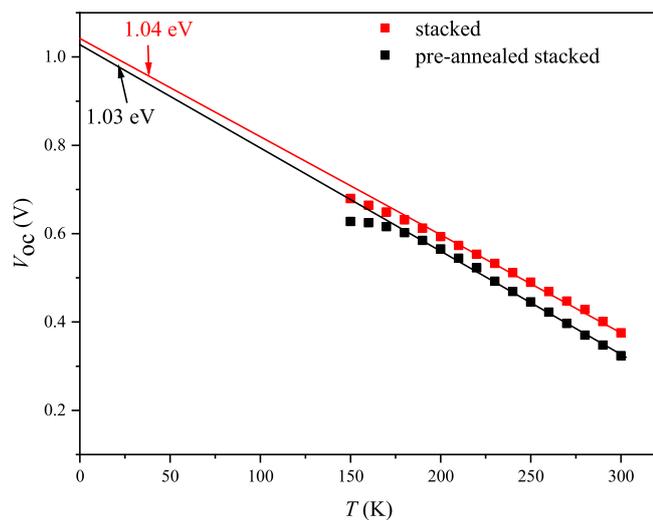


Figure 5. Temperature-dependence of V_{oc} for the devices from stacked and pre-annealed precursor devices, respectively.

the main recombination mechanism. As it can be seen in figure 5, V_{oc} significantly deviated from the ideally expected linear behaviour at low temperature. This effect is commonly observed in our devices (not shown here) and also in literature [12, 15, 19, 23]. It can mainly be related to a carrier freeze-out at low temperatures [19, 23] (that also enhances the detrimental effect of possible potential barriers) but additionally to the general temperature dependence of the material parameters involved. Based on equation S1, the linear extrapolation of the temperature dependence of V_{oc} to $T = 0$ K yields $E_A = 1.04$ and 1.03 eV for the devices prepared from the stacked and pre-annealed stacked precursors, respectively (figure 5). The E_A of the devices is very close to the bandgap (E_g) extracted from ER measurements (see table 1). Furthermore, the diode ideality factor for all devices is close to two. From these findings, we conclude that bulk Schottky–Read–Hall (SRH) recombination is the dominant recombination mechanism in our devices. This is in agreement with other reports from the literature [19]. Additionally, there is a significant lattice mismatch between the layers at the interfaces. For instance, the lattice mismatch between CZTSe and CdS is around 2.4% [24]. This can be expected to induce the formation of misfit dislocations and corresponding defect-related recombination losses, it should not currently limit our device performance. On the one hand, efficiencies above 11% could be achieved for CZTSe/CdS devices by other group [8, 19, 23]. Thus, further optimization (individual layers thickness and selenization parameters) are expected to lead to higher efficient devices.

4. Conclusions

We demonstrated an approach for fabricating CZTSe thin-film based solar cells via annealing of co-evaporated stacked precursors (Cu–Sn/Cu, Zn, Sn, Se/ZnSe/Cu, Zn, Sn, Se). The proposed configuration exhibited an η up to 7.9% with a V_{oc} and FF up to 429 mV and 62%, respectively. The

investigation of the absorber morphology showed the co-existence of larger grains at the surface of the absorber and fine grains at the Mo/CZTSe interface. It was found that pre-annealing of each individual stacked layer could suppress this effect. Moreover, J – V – T analyses revealed that bulk SRH recombination and a relatively high value for R_s still deteriorate device performance for the investigated solar cells. Therefore, we expect that a further optimization of the presented Cu–Sn seed layer approach should lead to a significantly higher efficiency.

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