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Tailoring Threshold Voltages of Printed Electrolyte-Gated Field-Effect Transistors by Chromium Doping of Indium Oxide Channels

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Supporting Information

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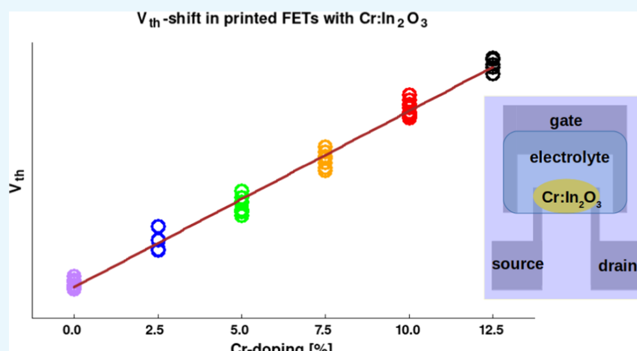
ABSTRACT: Printed systems spark immense interest in industry, and for several parts such as solar cells or radio frequency identification antennas, printed products are already available on the market. This has led to intense research; however, printed field-effect transistors (FETs) and logics derived thereof still have not been sufficiently developed to be adapted by industry. Among others, one of the reasons for this is the lack of control of the threshold voltage during production. In this work, we show an approach to adjust the threshold voltage (V_{th}) in printed electrolyte-gated FETs (EGFETs) with high accuracy by doping indium-oxide semiconducting channels with chromium. Despite high doping concentrations achieved by a wet chemical process during precursor ink preparation, good on/off-ratios of more than five orders of magnitude could be demonstrated. The synthesis process is simple, inexpensive, and easily scalable and leads to depletion-mode EGFETs, which are fully functional at operation potentials below 2 V and allows us to increase V_{th} by approximately 0.5 V.



■ INTRODUCTION

Because of an increasing interest in printed devices utilized in a variety of applications for the "Internet of Things", research efforts in this field have been rapidly growing in the last decade leading to substantial advances in the field. Several components, such as printed radio frequency identification (RFID) antennas, printed organic light emitting diodes, printed displays, or printed solar cells, have already been in use for many years by now or are on the verge to replace their traditionally produced analogs. For other components and devices, especially printed logics, it has not yet been possible to fulfill the requirements in synthesis and processing and in properties of the printed materials for a transfer to industrial use.[1] There are many issues in the way of reaching this level, including low-temperature processability, use of low-cost materials, applicability to flexible substrates, tailorability of properties of the active materials, long-term stability, and reliability of yield and properties, to name a few. The complexity of printed field-effect transistor (FET) devices and the sensitivity of their properties with printing process changes can be seen as a major hurdle when it comes to the last point: the necessity to print many devices with predictable and reliable performance parameters as the basis for circuits. Therefore, on a device level, the active and passive parts would greatly benefit from a possibility to be individually tailored toward their performance parameters to adapt to the complete printed device or circuit. One of these performance parameters is the threshold voltage (V_{th}), which indicates the transition of an electrically insulating channel (off-state) to an electrically conducting channel (on-state) after a sufficient gate potential is applied. To tailor the semiconducting channel regarding a defined V_{th}, several approaches can be used, including the utilization of different channel materials, different thicknesses or permittivities of the dielectric, organic monolayered dielectrics, adjusted surface carrier densities, or channel layouts, that is, aspect ratios.[2−7] Another prominent method to control the V_{th} is chemical doping of the channel material in order to change its electronic band structure.[8−10]

To adapt to the demands of low power applications, printed electronic circuits, which are operational at low potentials, are

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required. Printed electrolyte-gated FETs (EGFETs) can fulfill such specifications because the electrolyte gating paired with an indium oxide semiconducting channel renders the device operational at working potentials below 2 V. These inorganic printed transistors have been proven to be reliable and to show remarkable performances.[11] Additionally, studies on indium tin oxide (ITO) have shown that the electrical properties of In_2O_3 can be well adjusted using dopants. Doping In_2O_3 with chromium is known to form a stable single-phase system in thin films for up to 15 at. % of Cr (relative to In).[12,13] In addition $Cr:In_2O_3$ has been intensively studied as a possible dilute magnetic semiconductor candidate material.[14−16]

In the present work, we report on wet-chemistry processing of $Cr:In_2O_3$ channels in EFGETs and demonstrate that the V_{th} of single transistors can be tailored. The new and simple processing technology toward printed electronics provides the basis for more complex circuit designs. The doping concept has been applied to a well-established production process for the preparation of in-plane, indium oxide-based, EGFETs resulting in a reliable and predictable increase of V_{th} from −0.63 to −0.15 V with increasing dopant concentrations.

■ RESULTS AND DISCUSSION

The focus of the current research is on the tailoring of V_{th} in FET devices by doping of the In_2O_3 channels with chromium. A series of six different chromium dopant concentrations, listed in Table 1, was examined.

Table 1. Cr-Doping Contents as Atom Percentage of Cations in the Channel Material

composition	dopant content (corresponding sample names) (%)
In_2O_3	0
$In_{1.95}Cr_{0.05}O_3$	2.5
$In_{1.90}Cr_{0.10}O_3$	5.0
$In_{1.85}Cr_{0.15}O_3$	7.5
$In_{1.80}Cr_{0.20}O_3$	10.0
$In_{1.75}Cr_{0.25}O_3$	12.5

The experiments were performed using in-plane EGFETs with displaced gate design and channel lengths and widths of 50 μm and approximately 100 μm, respectively. The preparation followed an established process for pure In_2O_3 channels, simply replacing pure In_2O_3 by the doped compounds.[17] The doping was performed by creating mother solutions of pure $In(NO_3)_3$, pure $Cr(NO_3)_3$, and pure solvent mixed in the appropriate volume ratios. The gating relies on a composite solid polymer electrolyte (CSPE), well-known and thoroughly examined by our group, and electrical testing has been performed at room temperature and constant humidity.[18] Detailed descriptions of each production step and the measurements can be found in the experimental part. A schematic of the overall process and a microscopic view of a typical FET are shown in the Supporting Information (Figures S1 and S2).

To ensure a controlled doping process, the as-synthesized materials were characterized via powder X-ray diffraction (XRD). As can be seen in the XRD-patterns (Figure 1a), a single-phase is observed even at higher dopant concentrations.

While the positions of reflexes for the pure In_2O_3 sample match the database reference pattern, shifting of all reflexes toward larger angles is observed with increased Cr-concentrations, which indicates a smaller lattice parameter coinciding with the decreased ionic radius of Cr^{3+} and Cr^{2+} compared to In^{3+} (Cr^{3+} ≈ 62 pm, Cr^{2+} ≈ 80 pm, and In^{3+} ≈ 92 pm).[19] In Figure 1b, this shift is clarified for the (222) reflexes. With this continuous shift and no secondary phase found in any of the doped samples, a homogeneous substitution of In by Cr in the crystal system can be assumed. Consequently, any changes in electrical behavior are most likely resulting from doping effects.

For each doping concentration, ten FETs were produced and device characteristics were measured for all functional devices. Nonfunctional devices arose from printing errors, leading to the channel material short circuiting with the gate electrode. Final set sizes range from 5 to 10 devices. To exclude any electrochemical side reactions and to show the functionality at low voltages, both gate (V_{GS}) and drain (V_{DS})

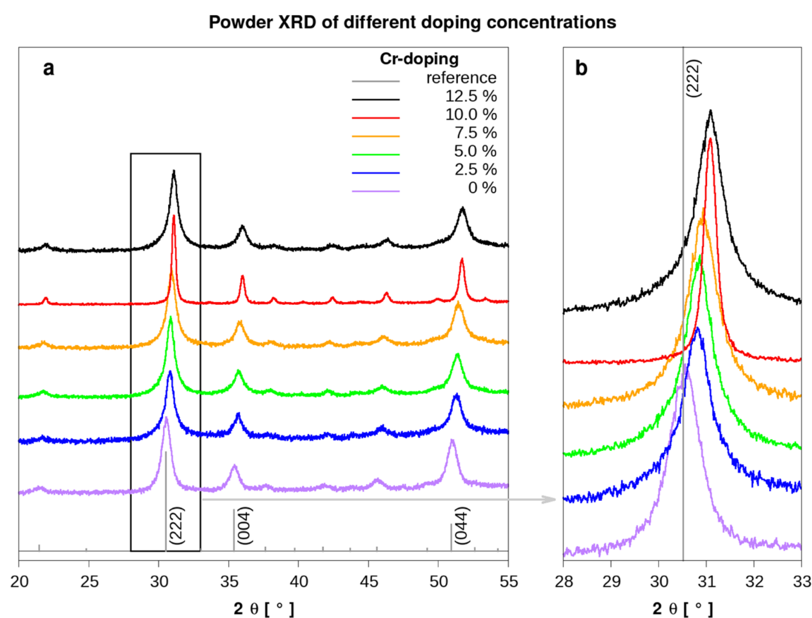

Figure 1. Powder XRD patterns of the channels for 0−12.5% $Cr:In_2O_3$, (a) patterns in the range of 20° to 55°, and (b) magnification of the (222) reflexes in the range of 28° to 33° for better visibility of the shifts; reference pattern of In_2O_3: ICSD 169420.

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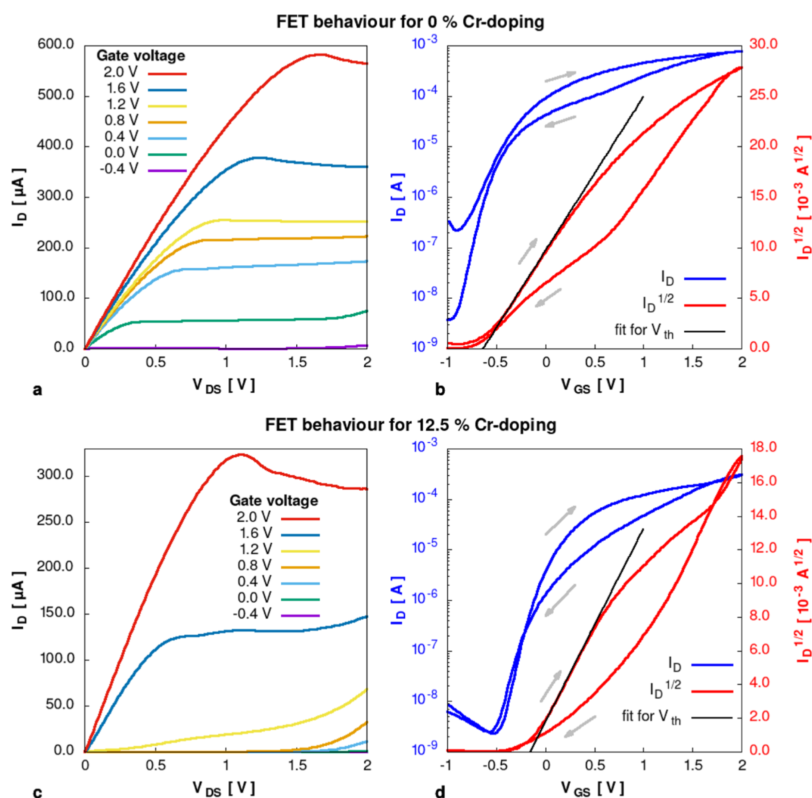

Figure 2. (a,b) output and transfer curves for undoped indium oxide and (c,d) output and transfer curves for 12.5% Cr-doping; transfer curves are measured at V_{DS} = 2 V.

voltages were kept below 2 V. In Figure 2, output and transfer curves of both an FET with an undoped and one with a highly Cr-enriched channel, respectively, are shown. We assume the hysteresis behavior to arise from mainly two factors, surface trap states and the comparably slow ion mobility in the CSPE lagging behind the V_{GS} sweeping speed. Notably the negative differential resistance (NDR) behavior, that is, visible bumps, in the output characteristics increases. Imperfect contacts between the channel and leads or internal material defects are often assumed to be the cause for trap states resulting in NDR.[20] Because of the production approach, the channel films are not monocrystalline, so many grain boundaries which are prone to lattice defects—and thus resulting trap states—exist. Additionally, the Cr-atoms can be assumed to further disturb the lattice and add more trap states. In both cases, diode behavior becomes apparent at V_{DS} > 1.5 V. As the output currents saturate before that and good $I_{D,on}$ is given at V_{GS} = 1.5 V in the transfer curves, limiting the operation voltages to 1.5 V in future applications should be considered.

The device characteristics for other dopant concentrations can be found in the Supporting Information (Figures S3−S6): in all cases a typical FET-behavior is given. Notably all gate (leakage) currents (I_G) are in the range of −11.0 to 7.0 nA and doping has no systematic influence on their behavior, as shown in Figure 3 by an overlay of leakage currents for FETs with different Cr-doping concentrations. Most importantly, V_{th} levels continuously shift to higher values.

An extensive study on Cr:In_2O_3 has been done by Wang et al. showing that Cr is mostly present in the Cr^{2+}-state and as such compensates the oxygen vacancies, which leads to lower carrier concentrations effectively being a hole doping process.[21] A direct influence of carrier concentrations on the

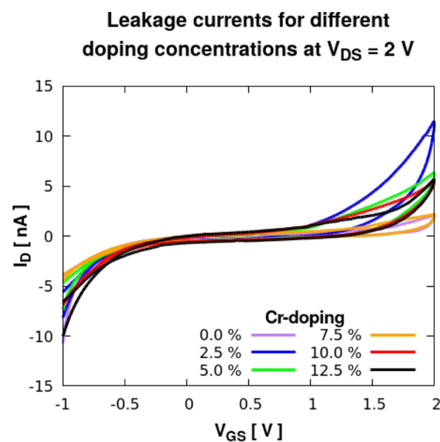

Figure 3. Overlay of leakage behavior for devices at each doping concentration.

threshold voltage has been observed in many FETs with metal oxide channels.[22−24]

Threshold voltages V_{th} of all devices have been extracted exploiting the direct correlation $I_D^{1/2} \propto (V_{GS} - V_{th})$ given in eq 2 as derived from the standard metal-oxide semiconductor field-effect transistor equation eq 1 in the saturation regime (i.e. $V_{DS} > V_{GS} - V_{th}$), where V_{DS} and V_{GS} are drain and gate voltages, W and L, the gate width and length, $C_{ch,ar}$, the areal capacitance of the channel, and I_D the drain current, respectively. V_{th} is given as the value of V_{GS} at I_D = 0 for the fit to the linear region of the square rooted output currents in the transfer curves (Figure 2b,d). In all cases, the forward curves of the transfer curve hystereses have been used.

$$I_D = \mu_{FET} \frac{WC_{ch,ar}}{2L} (V_{GS} - V_{th})^2 \quad (1)$$

$$\sqrt{I_D} = x(V_{GS} - V_{th}) \qquad \text{with: } x = \sqrt{\mu_{FET} \frac{WC_{ch,ar}}{2L}} \quad (2)$$

The obtained values for V_{th} are shown in Figure 4a. As can be seen, the threshold voltages linearly increase with increasing

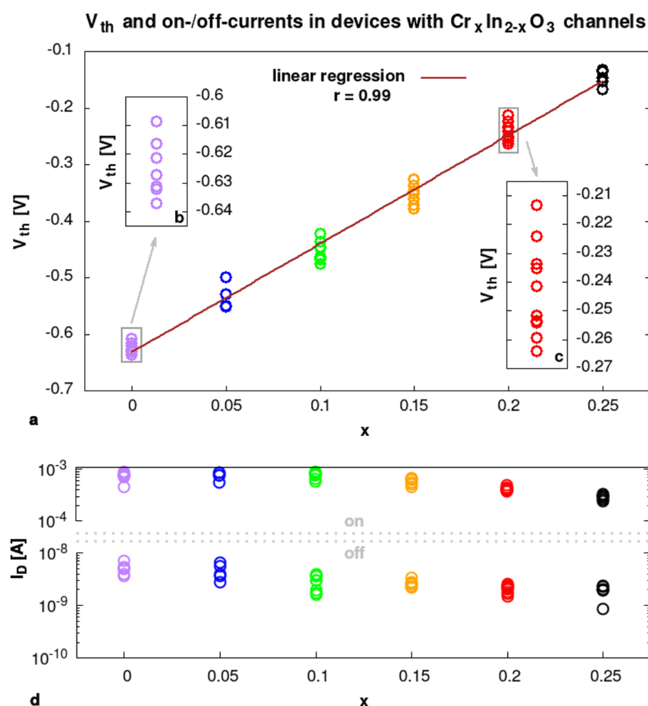

Figure 4. (a) Values for V_{th} for all devices with insets (b,c) as magnifications of the sets with 0 and 10% doping, respectively and (d) corresponding values of $I_{D,on}$ and $I_{D,off}$.

dopant concentrations, and the regression coefficient of the linear fit is close to 1, that is, a direct correlation between V_{th} and Cr-doping is observed. The increase in V_{th} at each doping step has been statistically analyzed, as described in the experimental part, and all neighboring sets are independent at a 95% confidence interval. On average, the threshold voltage is shifted by approx +0.5 V from −0.63 to −0.15 V between 0 and 12.5% Cr-doping. Along with this, $I_{D,on}$ and $I_{D,off}$ show a general decrease but not with as strict linearity as for the threshold voltages. This can be explained with a larger variation in the channel widths arising from different spreading behavior of the ink between the source and drain leads, as can be seen in the two example devices in Figure S2 in the Supporting Information. In general, the on-currents for the highest doped samples are approximately reduced to 40% relative to the undoped samples. All but three devices span five orders of magnitude in the $I_{D,on}/I_{D,off}$-ratio. A full list of all values for V_{th}, $I_{D,on}$, and $I_{D,off}$ of each device can be found in Table S1 in the Supporting Information. Substhreshold slopes for all devices have been determined as the maximum slope below these V_{th}. They are in the range of 90−210 mV/dec without any systematic dependence on the doping.

In Figure 5a, a comparison of the output curves for one device from each doping concentration at a gate bias of 2 V is shown on a linear scale. As can be seen, the currents decrease with increased doping of the channel material but are still in the same order of magnitude. The trend in the currents can mainly be traced back to two aspects: on the one hand eq 1 can be regarded. With V_{th} increasing, the factor $(V_{GS} - V_{th})^2$—and thus I_D—will be reduced. With the average V_{th} change from −0.63 to −0.15 V and the given gate voltage of 2 V, this factor alone can account for a 33% decrease in $I_{D,on}$ between the undoped and 12.5% Cr-doped samples.

On the other hand, the increasing dopant concentration will introduce more scattering centers into the semiconductor, well known from the literature to lower the field-effect mobility μ_{FET}.[12,25,26] To prove this effect in our devices, the field-effect mobilities of two transistors of each doping batch have been determined using eq 3 which is derived from eq 1.[27] x is already given in eq 2 as the slope of the linear fit used for determining V_{th}. This approach is numerically more stable in comparison to using extracted values for $I_{D,sat}$ and V_{th} in eq 1 because instead of numerically finding two single point values, the slope relies on a fit to a large range of measurement points and a least squares optimization. The specific areal channel capacitances have been extracted from capacitor measurements with source and drain (short circuited) on the one side and gate on the other side as electrodes. The approach is explained in detail in the Supporting Information.

$$\mu_{FET} = \frac{2Lx^2}{WC_{ch,ar}} \qquad \text{where: } x = \frac{\sqrt{I_D}}{(V_{GS} - V_{th})} \quad (3)$$

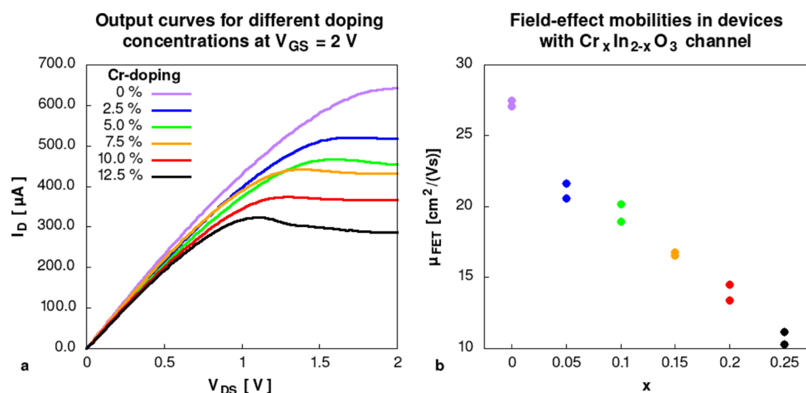

Figure 5. (a) output curves at V_{GS} = 2 V and (b) field-effect mobilities for different Cr-doping concentrations; the samples in (a) are identical to the ones in Figures 2 and S3−S6.

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In Figure 5b, the trend of decreasing mobilities with increasing Cr-content is clearly visible. Mobilities shrink by about 60% between the samples with 0 and 12.5% Cr-doping and add another major factor to the loss in $I_{D,on}$.

When considering applications in larger logical arrays using FETs with different V_{th}-values, the simplest application would be an NMOS-inverter with a load transistor. The respectively necessary printed FETs with indium oxide channels and positive threshold voltages are well known systems.[17,28] Our approach allows the precise predefinition of the threshold voltage with very good accuracy.

OUTLINE

Tailoring of the V_{th} of Cr:In_2O_3 channels for EFGETs could be achieved by adjusting the chromium concentration between 0 and 12.5%. A clear trend toward increased V_{th} with increased chromium concentration has been observed, accompanied by a saturation current decrease of about 60% at the high chromium concentrations. Despite the limitations of the printing technique, a clear change of V_{th} with a highly linear character was obtained. The doping process was conducted using a wet chemical approach, which can be directly applied in ink-jet printed electronics. Our approach allows us to almost pinpoint V_{th}, and thus, a central parameter in circuit design could be well managed. On the other hand, the advantage of tailoring V_{th} occurs at the cost of $I_{D,on}$; however, that loss assumingly could be made up by design changes, for example, increased channel widths. The major advantage of the current approach is its simplicity, which is of direct interest for low-cost printed electronics. With the vast variety of possible dopants for In_2O_3, this approach promises a full branch of tailored FET properties in inorganic printed electronics using simple wet chemical methods.[26]

EXPERIMENTAL SECTION

Channel Ink Preparation. Three parent solutions of 0.1 M $In(NO_3)_3 \cdot xH_2O$ (99.99% Sigma-Aldrich), 0.025 M $Cr(NO_3)_3 \cdot 9H_2O$ (99.99%, Alfa Aesar), in a 4:1-mixture of deionized water and glycerol, and a solvent-only solution with the same makeup have been prepared by applying 5 min of ultrasonication (salt solutions only) followed by at least 30 min of stirring. The final printing inks have been obtained by mixing the indium parent solution with varying amounts of the chromium and solvent-only parent solutions followed by at least 30 min of intense stirring to ensure a homogeneous distribution of the dopant according to Table 2.

Effectively, 2 mL of each ink with a fixed indium concentration of 0.05 M and varying amounts of the Cr-dopants have been made. The indium concentration and the solvent mixture has been successfully applied earlier. The preparation route is a variation of an established method for undoped In_2O_3 channels.[17]

Table 2. Volume Ratios for Different Doping Concentrations

ink	V_{In} [mL]	V_{Cr} [mL]	$V_{solvent}$ [mL]	doping ratio [In:Cr]	$n_{Cr}/(n_{Cr} + n_{In})$ [%]
1	1	0	1	40:0	0
2	1	0.1	0.9	40:1	2.5
3	1	0.2	0.8	40:2	5.0
4	1	0.3	0.7	40:3	7.5
5	1	0.4	0.6	40:4	10.0
6	1	0.5	0.5	40:5	12.5

Device Production. For creating the passive structures, commercially available glass substrates with sputtered ITO coating (pgo GmbH, $R \leq 20\ \Omega/\square$) were taken as the basis and structured using a TRUMPF TruMicro 5000 laser ablation system. Coating removal was done at a laser frequency of 800 MHz and a power of 3 W in a grid pattern. Before printing, all substrates were thoroughly cleaned by 5 min of ultrasonication in *i*PrOH followed by rinsing twice with water and *i*PrOH and blow-drying.

The channel inks were applied with a Dimatix DMP 2831 materials printer system using cartridges with 10 pL nozzles. Printing was done on the day of ink preparation using four layers of ink at a drop spacing of 30 μm. Annealing was done in a box furnace. During this process, the devices were heated to 400 °C within 2 h, kept at this temperature for 2 h, and cooled down to room temperature overnight.

The substrates of reference samples without a channel for capacitance measurement underwent the same temperature treatment before being printed with the electrolyte.

In the last step, eight layers of the CSPE were applied with the same printing system, and the FETs were allowed to dry for about 2 h before measurement.

Composite Solid Polymer Electrolyte. The CSPE was prepared using an established method of this group:[18] 0.3 g of poly(vinylalcohol) is dissolved in 6 g of DMSO under stirring at 80 °C. A separate solution of 70 mg of $LiClO_4$ was solved in 0.63 g of propylene carbonate under stirring. Once fully dissolved, the polyvinyl alcohol solution is added to the salt solution and stirred overnight at 60 °C. The resulting clear liquid is filtered through 0.45 μm PTFE syringe filters and then directly used in the printing.

Reference Powders and XRDs. Approx. 1 mL of each solution was placed in glass Petri dishes and received the same temperature treatment as the channels: heating to 400 °C in 2 h, level keeping for 2 h, and cooling down overnight. After cooling, the powders were scratched off and powder XRD-patterns were measured with a Bruker D8 ADVANCE diffractometer using copper Kα radiation.

Device Characterization. Electrical measurements were done on a SUSS MicroTec MLC-150C probe station with an Agilent 4156C precision semiconductor parameter analyzer as a measuring unit. Transfer curves were measured at fixed drain voltages of 2.0 V and a gate voltage sweep of −1.0 to 2.0 V, and output curves at fixed gate voltages of −0.4 to 2.0 V in 0.4 V steps and a drain voltage sweep of 0.0−2.0 V. Capacitances have been measured by short-circuiting the source and drain leads and keeping them at 0.0 V, while sweeping the gate voltage from −1.0 to 2.0 V.

Statistical Analysis. Shapiro−Wilk tests for normal distribution have been performed on each set and *F*- and *t*-tests for neighboring sets, where the *t*-test has been chosen according to the result of the *F*-test. All tests were run as implemented in the R programming language version 3.5.2 with a confidence level of 95%.[29]

The correlation coefficient has been extracted with gnuplot, which was also used for creating all graphs in this work.[30]

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsomega.9b02513.

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Schematic of the device production steps, microscopic view of two FETs as produced, FET characteristics for devices with 2.5, 5.0, 7.5, and 10.0% Cr-doping, V_{th}, $I_{D,on}$, $I_{D,off}$, and $\log_{10}(I_{D,on}/I_{D,off})$ for each device, and detailed descriptions of the approach for determining $C_{ch,ar}$ (PDF)

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Notes

The authors declare no competing financial interest.

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