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Quasi-Two-Level Flying-Capacitor-Converter for Medium Voltage Grid Applications

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***Abstract*—Medium voltage converters are becoming more relevant in future grid applications. Especially more wind and PV generation systems will be have to added and integrated into the grid in order to achieve the required reduction in CO2 emissions. High power generation units will be integrated into the grid at medium voltage level. Furthermore meshed MV grids will require interties based on MV converter technology. Today's standard medium voltage converters are either based on the MMC technology or us 3L/5L approaches operated at low switching frequencies and containing bulky filters. Both concepts still lead to relatively high costs and low efficiencies which are major reasons for the slow spread of power converters in medium voltage grid applications.. Future grid applications demand less distortion, higher reliability and lower costs for converter systems at each voltage level. The Quasi-Two-Level operation of the flying capacitor multilevel converter with silicone-carbide (SiC) based semiconductors is a method for achieving these requirements for medium voltage converters. This paper presents a new concept for minimizing capacitance and balancing the capacitors with fast switching semiconductors. Moreover, a novel approach for limiting the overvoltage stress caused by the Quasi-Two-Level modulation of a flying capacitor converter is presented.**

***Index Terms*—Quasi-Two-Level-Operation, Flying Capacitor, Multilevel-Converter, Medium voltage converter**

I. Introduction

The two-level converter is state-of-the-art for most low voltage (LV) applications. However, this topology is not suitable for MV applications because of the significant power-semiconductor losses and the high $\mathrm{d}v/\mathrm{d}t$ stress of passive components, leading to a limited operating range of the converter system. In LV applications the next generation of fast switching semiconductors based on silicone-carbide (SiC) has already been introduced, allowing the use of increased switching frequencies due to significantly reduced switching losses. High voltage blocking SiC-semiconductors ($\geq 3.3\,\mathrm{kV}$) are in development and investigated for drain source voltages up to $15\,\mathrm{kV}$ [1], but are not yet commercially available at a reasonable cost level. Furthermore, the high $\mathrm{d}v/\mathrm{d}t$ and the resulting overvoltage stress result in important challenges associated with SiC-semiconductors in medium voltage (MV) applications.

For this reason, insulated-gate bipolar transistors (IGBTs) are commonly used in conventional MV applications. As a result of significant IGBT switching losses, the switching frequencies of commercial medium voltage converter systems are typically limited to below 1 kHz. Therefore, fast switching high blocking semiconductors are promising for increasing the switching frequencies and thereby reducing the required filter components, however they cause a significantly increased $\mathrm{d}v/\mathrm{d}t$. Currently, there are no two-level converters commercially available for applications in the voltage range $> 2\,\mathrm{kV}$.

For MV applications, multilevel converters with a minimum of three output voltage levels were introduced, e.g the Modular-Multilevel-Converter (MMC) [2], the Cascaded H-bridge Converter (CHB) [3], the Neutral Point Clamped-converter (NPC) [4] and Flying-Capacitor-converter (FC) [5]. Compared to a two-level converter, these topologies are more complex and usually more expensive. Depending on the design the cell based concepts already allow the use of low loss and cost effective LV power semiconductors. However, some drawbacks like high cell numbers (MMC), large capacitors (MMC, CHB), special transformers (CHB) overcompensate this effect. However, the multilevel approach is necessary to operate in the medium voltage range. The goal of this contribution is to find a topology that is capable of utilizing low voltage hardware at MV level without increasing the system complexity and costs. In this regard, the trade-off between design and operation of the multilevel converter is challenging in order to fulfill the requirements for MV applications.

The Quasi-Two-Level operation of a multilevel converter is a promising solution of this optimization problem. A Quasi-Two-Level operation of a MMC is presented in [6]–[8]. For NPC-converter the operation is presented in [9]. Silicon-carbide metal-oxide-semiconductor field-effect transistors (SiC-MOSFETs) are used for a Quasi-Two-Level operation of the flying capacitor converter for low voltage applications in [10]. Therein, the achievable primary cost reduction is investigated using an optimization algorithm and the minimum capacitances of the flying capacitors are shown for operation without an active balancing algorithm. The challenge of the flying capacitor converter is the determination of the required cell capacitances and the capacitor voltage balancing. In addition, the voltage stress of the passive components has to be balanced in the whole converter system.

In this paper, the basics of the flying capacitor converter topology are first explained in section II. In section III the principle of the Quasi-Two-Level-Operation, is presented. Therein, the impact of this modulation strategy on the FC characteristics is investigated. In section IV, the capacitor balancing is discussed in detail and a new algorithm is presented. In section V, the capacitor design with respect to a stable operation is described. In section VI the simulation

environment and in section VII the results of the simulation are presented. In the near future, a full scale prototype will be built to validate the concept in a laboratory test.

II. Fundamentals

The concept of the flying capacitor converter topology was introduced in [5]. For higher DC voltages, an enhanced topology – the stacked multicell converter (SMC) – has been introduced [11]. The difference between these topologies is that the flying capacitor converter has a vector placement of semiconductors and flying capacitors, where as the stacked multicell converter has a matrix placement of semiconductors and flying capacitors. These converters generate the multilevel output voltage level based by switching flying capacitors in the active current path. At different capacitor voltages, this leads to different output voltages dependent on the combinations of the interconnection. This paper focuses on the flying capacitor converter as described in [5] as a less complex multilevel topology for MV converters than other multilevel converter with more power semiconductors. Figure 1 depicts the basic structure of a 5-level flying capacitor (FC) topology. An n-level flying capacitor converter ($n \in \mathbb{N}$) is made of $2 \cdot (n-1)$ power semiconductors and $(n-2)$ capacitors in addition to the DC link capacitor. Each half of the power semiconductors are connected in series to the high side (H) and the remaining to the low side (L). Only one switch in each pair of semiconductors (commutation cell) can be turn on at a time to prevent short circuits between the capacitors, because each capacitor C_i has got a different nominal voltage $v_{c,nom,i}$.

$$v_{c,nom,i} = v_{dc} \cdot \frac{n-1-i}{n-1} \quad i \in \{[1...(n-2)] \cap \mathbb{N}\} \qquad (1)$$

Each commutation cell connects one of the capacitors to the output terminal to generate the multilevel output voltage. The commutation path is between the high side and the low side semiconductor of each pair including the capacitors. For short switching times and small overvoltage stress, it is necessary to design the commutation path with a minimum stray inductance. In order to get an optimal solution, the approach is to build the converter using modular components - Power Electronic Building Blocks (PEBB). The concept of PEBB's is to separate and concentrate the power electronics of the converter in modules with the same construction. In this case, two semiconductors and one capacitor are integrated in one PEBB to achieve minimal stray inductances within the commutation paths. Likewise, the low inductive connection between the PEBB's is also important. A n-level converter requires $(n-1)$ PEBBs. The nominal voltage for the semiconductors in a PEBB can be calculated with eq. (2).

$$v_{PEBB,nom} = \frac{v_{dc}}{n-1} \quad n \in \mathbb{N} \qquad (2)$$

In operation, the applied voltage across the semiconductors always deviates from the nominal voltage, because the capacitor voltages also differ during operation from the nominal voltages. The deviations of the capacitor voltages arise when the output current flows through the flying capacitors. This happens at all multilevel output voltage levels between

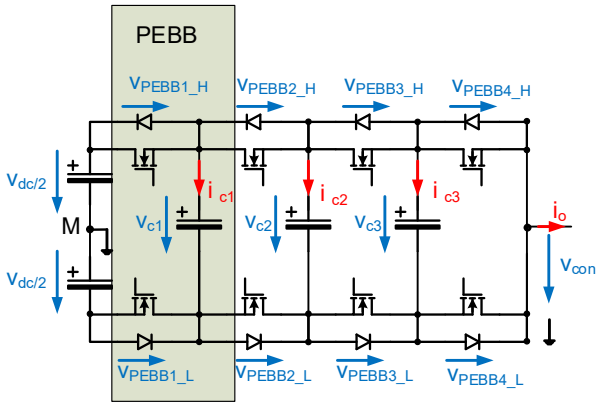

Fig. 1. 5-level flying capacitor converter, single phase design (SP FC)

$+\frac{v_{dc}}{2}$ and $-\frac{v_{dc}}{2}$. In recent years, this topology has become interesting for research as new semiconductors could provide new benefits. [12] presents new possibilities for this topology and shows the compatibility with low voltage, fast switching, SiC-based semiconductors. Thus higher switching frequencies can be achieved with the flying capacitor converter, even in medium voltage.

III. Quasi Two-Level-Operation

The basic idea of the Quasi-Two-Level modulation is to use the multilevel topology in combination with a two-level modulation scheme. On the one hand, the control and modulation strategies are very similar as the ones used for a standard two-level converter. But on the other hand, the characteristic benefits of multilevel converters in terms of reduced $\mathrm{d}v/\mathrm{d}t$ and small overvoltage stress at high voltage levels for the output can be used as well. The voltage-trajectory across the inductances is the same compared to the two-level modulation. Figure 2 shows a simplified output voltage (red line) of the Quasi-Two-Level modulation. For comparison, it shows the output voltage of a two-level converter (dashed green line).

Instead of switching all devices at the same time, each step is delayed by $t_{p\,i} = t_c/(n-2)$ where t_c describes the transient switching time for the output voltage from $+\frac{v_{dc}}{2}$ to $-\frac{v_{dc}}{2}$ and vice versa. For two-level converters the transient switching time is $t_{c,2Lvl} \approx 0$ because the transition only requires the switching time of the semiconductors t_s. The blue lines in fig. 2 shows the delayed switching signals for the different PEBB's of the converter. The shifted switching scheme and the resulting reduced voltage steps mitigate the overvoltage stress of the components. The output voltage changes from $+\frac{v_{dc}}{2}$ to $-\frac{v_{dc}}{2}$ and back during each carrier-modulation period t_m.

In general, the transient switching time t_c is $\sum_1^{n-2} t_{p\,i} \quad i \in \{[1...(n-2)] \cap \mathbb{N}\}$. The delay time $t_{p\,i}$ can be variable for each PEBB. For the simple balancing algorithm presented in chapter IV, all $t_{p\,i}$ are equal and constant. The transient output voltage level time $t_{p\,i}$ must be longer than the switching time of the semiconductors $t_s < t_{p,i}$. Otherwise, more than one PEBB changes its state at the same time. In this case, the commutation path and the stray inductances are not minimized.

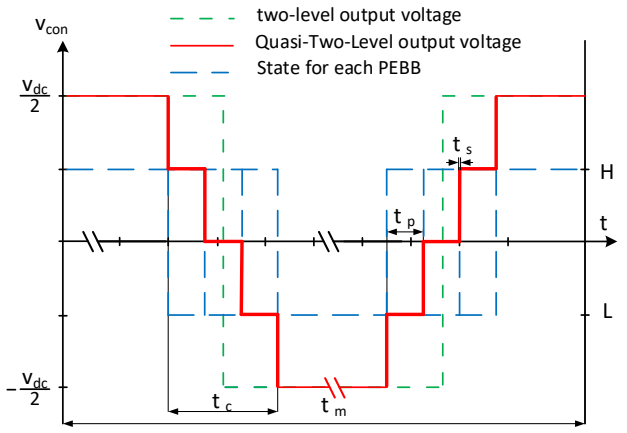

Fig. 2. Quasi-Two-Level modulation of a 5-level converter

A degree of freedom of the Quasi-Two-Level modulation is the transient switching time t_c. The current flows through the PEBB capacitors only during switching, i.e. during t_c. By using conventional modulation, the current flows through one or more of the capacitors for most of the modulation period. These times intervals significantly influence the sizes of the capacitors and are discussed in chapter V. Generally speaking, the capacity can be designed smaller with fast switching semiconductors and a short switching time t_c.

A further degree of freedom is the carrier frequency of the power semiconductors. The carrier frequency has no influence on the capacitor voltage balancing. However, the carrier frequency influences the output filter design and the overall efficiency of the converter. To fulfill the requirements of efficiency, grid code and output voltage spectrum, the carrier frequency can be optimized as compared to a two-level converter. The output voltage spectrum of the Quasi-Two-Level modulation has a higher harmonic content than a conventional n-level modulation as presented in [13]. The losses and stress of all components (converter and output-filter) has to be considered for each application.

IV. Simple Balancing Algorithm

Most multilevel-converters (except the CHB with multi winding transformer) require active balancing of capacitor voltages. This also applies for the Quasi-Two-Level operation of a FC. For some multi-level converters, there are existing control methods for balancing the capacitor voltages by quasi-two-level operation. For example, a control scheme for a Quasi-Two-Level operation of a MMC is presented in [7] and [8]. A capacitor voltage balancing algorithm for Quasi-Two-Level operation of a NPC converter is shown in [14].

This paper describes an algorithm for balancing the capacitor voltages when using Quasi-Two-Level operation in the FC converter. This simple balancing algorithm is based on a development in [15], where a balancing algorithm for a conventional multilevel operation of the FC converter is described. In conventional multilevel operation, only a few semiconductors change their state during each carrier modulation period. In Quasi-Two-Level operation, all semiconductors change their state in each period. If only one PEBB changes its state at the same time, the commutation path and the voltage overshoot caused by the fast switching semiconductor is minimized. The balancing algorithm chooses a sequence of switching states to change the output voltage from $+\frac{v_{dc}}{2}$ to $-\frac{v_{dc}}{2}$ and vice versa.

Figure 4 shows all possible transitions for $n = 5$. As an example, two possible switching sequences are highlighted in green and blue. Each switching sequence has a different impact on the voltage of the capacitors. H means the high side switch of a PEBB is active, L means the low side switch of a PEBB is active. In each state, except the $\pm\frac{v_{dc}}{2}$ states $HHHH$ and $LLLL$, the output current flows through the PEBBs' capacitors. The sign of each capacitor current in the figure describes if the output current flows in the same direction (+) or the opposite direction (-) of the respective capacitor current. As an example, the capacitor currents in state $HLHH$ are $i_{c1} = +i_O$, $i_{c2} = -i_O$, $i_{c3} = 0$ and $i_{c4} = 0$, where i_O is the output current of the converter (all currents are shown in fig. 1). A positive current results in a positive power charging the capacitor. Likewise, a negative current leads to a negative power discharging the capacitor. In order to ensure stable operation and keep the capacitor voltage within the operating range, the time average of the capacitor power has to be zero.

A. Calculation and sorting of the capacitor voltages

Choosing the switching sequence requires a measurement of each capacitor voltage. The voltages must be measured before the switching event, since the sequence can not be changed during the switching time t_c. This limitation is implemented because the sequence of switching states is determined in advance. The algorithm calculates the voltage deviation $\Delta v_{c,i} \quad i \in [1,(n-2)]$ for each capacitor compared to its nominal value (eq. (1)).

$$\Delta v_{c,i} = v_{c,i} - v_{c,nom,i} \quad i \in \{[1...(n-2)] \cap \mathbb{N}\} \qquad (3)$$

The capacitor voltages are sorted regarding the voltage deviation $|\Delta v_{c,i}|$. This generates a vector with the index $[i]$, deviation $[|\Delta v_c|]$ and sign of the voltage deviation. The sorting vector is called dominant voltage deviation vector $[\Delta v_{i,do}]$ or dominant capacitor vector $[c_{i,do}]$. The algorithm is shown in fig. 3.

B. Selection of switching sequences for balancing of the flying capacitor

The next step analyzes the sorting vector from chapter IV-A. The complete switching state chart for a 5-level FC converter is shown in fig. 4. The algorithm starts at one of the states $HHHH$ or $LLLL$. Each capacitor can be influenced by multiple states. These states are reached by switching only one PEBB at a time. In each step, the algorithm chooses the next state corresponding to $\Delta v_{1\,do}$. This influences the first dominant capacitor $c_{1,do}$, i.e. the capacitor with the largest voltage deviation. In some states, there is more than one

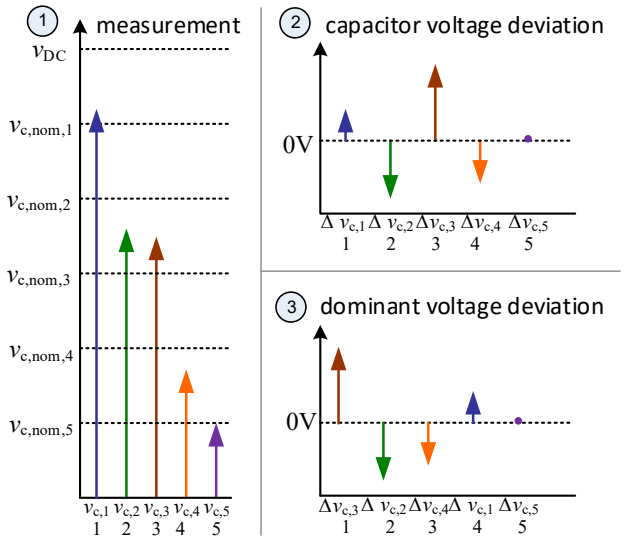

Fig. 3. Algorithms for calculation and sorting of the capacitor voltages

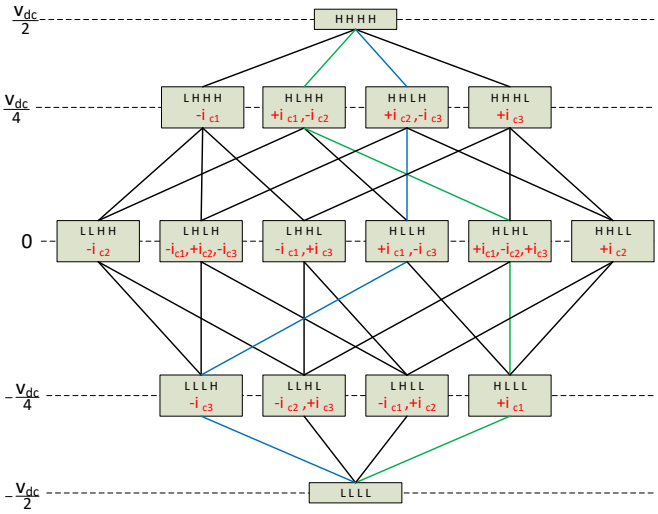

Fig. 4. Switching state chart for a 5-level flying capacitor, two possible switching sequences are highlighted in green and blue.

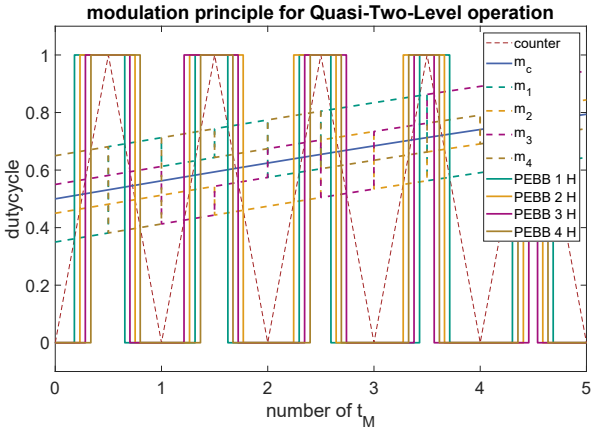

Fig. 5. The Modulation principle for quasi-two-level operation of a 5-level flying capacitor converter with $n_s = 2$

subsequent state that positively influence $c_{1,do}$. In this case, the algorithm chooses the state which influences the next available $c_{i\,do}$. In some states and possible vectors, there is no positive subsequent state. The algorithm chooses the state which influences the last $c_{i,do}$ to achieve minimal deviation. The algorithm terminates when the complementary maximum output voltage level is reached. If the algorithm is finished, a balancing switching sequence from $HHHH$ to $LLLL$ has been determined for the actual flying capacitor voltages. As an example the blue sequence from fig. 4 has got the switching states $HHHH$, $HHLH$, $HLLH$, $LLLH$ and $LLLL$. The transition $HHHH$ to $HHLH$ is performed by PEBB number 3, corresponding to the first element of the switching sequence. Likewise, the change between $HHLH$ and $HLLH$ is performed by PEBB number 2, corresponding to the second element of the switching sequence. The full sequence is $[3;2;1;4]$ from $HHHH$ to $LLLL$ and can be passed in both directions and equally influences the capacitors voltages. This algorithm can be executed online or the sequence can be selected from a look up table (LUT).

C. Modulation of the Quasi-Two-Level operation

The principle of the modulation is based on the two-level modulation. The modulation index m_c is calculated by the control algorithm. A separate sine triangle pulse-width modulation (PWM) is used for each PEBB. The switching sequence changes the modulation index for each PEBB, so it can balance the voltages of the flying capacitors. The position p_x at the switching sequence is important for calculating the individual modulation indices m_x for each PEBB. For example, the sequence $[3;2;1;4]$ leads to $p_3 = 1$ for PEBB 3 and to $p_4 = 4$ for PEBB 4. The positions are complementary for positive and negative switching. The individual modulation index m_x are defined for positive switching (from $-\frac{v_{dc}}{2}$ to $+\frac{v_{dc}}{2}$) while it is different for negative switching (from $+\frac{v_{dc}}{2}$ to $-\frac{v_{dc}}{2}$). The individual modulation index m_x for each PEBB is calculated with eq. (4).

$$m_x = m_c - \frac{(n - p_x + 1) \cdot t_p}{2 \cdot n \cdot t_m}, \quad x \in \{[1...(n-1)] \cap \mathbb{N}\} \quad (4)$$

Figure 5 shows how the gate signals of the high-side power semiconductors of the PEBB of a 5-level FC converter are generated for the given modulation-index m_c. Only the high-side gate signal is shown for reasons of clarity. The individual modulations indices m_x are shown, which change twice per modulation period due to the balancing algorithm. The algorithm can be executed less often and then the individual modulation indices m_x would change less often. The high-side power semiconductors are switched on if the counter is greater than the individual modulation index m_x, as is usual with a sine triangle modulation.

V. Design of the capacitor

The average capacitor power has to be zero, but not the instantaneous power. During operation, the capacitor can be charged or discharged. The maximum change in charge can be calculated with $\Delta Q_{c,max} = C \cdot \Delta v_{c,max}$. Thus, the capacity of the capacitors can be calculated with $C = \frac{\Delta Q_{c,max}}{\Delta v_{c,max}}$.

The maximum change of charge and maximum voltage deviation is also important in operation. When using a Quasi-Two-Level operation, the maximum change of charge can be calculated with $\Delta Q_{c,max} = t_c \cdot \hat{i}_o$. The transient switching time t_c depends on the switching time of the semiconductors and influences the maximum change of charge. The maximum output current $\hat{i}_o$ also influences the maximum change of charge. For conventional operation, the maximum voltage deviation $\Delta v_{c,max}$ is assumed to be in a range of $\pm 10\%$ of the nominal PEBB voltage. This results from the splitting of the semiconductor forward blocking voltage into PEBB voltage, deviation of the capacitor voltages, transient overvoltage and enough reserve up to the breakdown voltage of the semiconductors. The same assumption can be made for the Quasi-Two-Level operation, since here an equal partitioning results. For the quasi-two-level operation it is important how often the voltage deviation can change its trend. This happens maximum at most twice per carrier-modulation period t_m if the switching sequence is recalculated before every high-level switching event, although fewer calculations are possible. n_s is defined as the number of algorithm computations per carrier-modulation period: $n_s \in \{[t_m \cdot f_{out} ... 2] \cap \mathbb{R}\}$. The lower limit is $t_m \cdot f_{out}$ and exists because the capacitors voltages in grid applications are slowly balanced naturally by sinusoidal output currents. If no new switching sequence is generated during a grid period, the output current always flows through the capacitors in the same way. Due to the sinusoidal current, there is the same amount of charging and discharging in the capacitors during a grid period. Flying capacitors with capacitances be greater than defined by this limit do not need active balancing, because the actual deviation will always be smaller than the permissible deviation. The capacitance of the flying capacitors for Quasi-Two-Level operation is calculated using eq. (5). When comparing conventional and Quasi-Two-Level operation, the capacitances can be smaller by a factor of $\frac{t_m}{t_c}$ when using two-level operation assuming equal carrier frequency $f_{carrier}$ and equal transient switching time t_c of the semiconductors. A parameter comparison for a 5-level flying capacitor converter is shown in table I. The capacitance c_{APOD} for APOD- (Alternative Phase Opposition Disposition) modulation as an example for conventional operation was calculated with eq. (6). The carrier frequency $f_{carrier} = \frac{1}{t_m}$ for APOD modulation is equal to the switching frequency for one PEBB. The equation applies only to APOD and the capacitors are similar in size to other conventional modulations. The energy contents in the different capacitors $E_{nom,i}$ were calculated for comparison with eq. (7). This comparison shows that the energy content is distributed unevenly in the converter and that the smaller capacitance has a direct influence on the energy content.

TABLE I
Parameter comparison of operations for a 5-level flying capacitor converter

	Quasi-Two-Level operation			conventional operation		
capacitor	C_1	C_2	C_3	C_1	C_2	C_3
i_C	200 A	200 A	200 A	200 A	200 A	200 A
v_{nom}	3.3 kV	2.2 kV	1.1 kV	3.3 kV	2.2 kV	1.1 kV
c	1 µF	1 µF	1 µF	3.4 mF	3.4 mF	3.4 mF
E_{nom}	5.45 J	2.42 J	0.6 J	1.87 kJ	833.14 J	112.04 J

$$c_{quasi} = \frac{t_c \cdot \hat{i}_o}{n_s \cdot \Delta v_{c,max}} \quad n_s \in \{[t_m \cdot f_{out} ... 2] \cap \mathbb{R}\} \tag{5}$$

$$c_{APOD} = \frac{\hat{i}_o}{(n-1) \cdot f_{carrier} \cdot \Delta v_{c,max}} \qquad n \in \mathbb{N} \tag{6}$$

$$E_{nom,i} = \frac{1}{2} \cdot c_i \cdot v_{nom,i}^2 \quad i \in \{[1 ... (n-2)] \cap \mathbb{N}\} \tag{7}$$

VI. Simulation Environment

The electrical circuit, semiconductors and grid were implemented in PLECS as simulation environment. The control algorithm and the modulation is calculated in Matlab Simulink. The block diagram of the simulation model is shown in fig. 6. The single phase flying capacitor converter (SP FC) and Quasi-Two-Level modulation exist separately for each phase, because the balancing algorithm and the modulation influence one phase, only. The measured grid voltages and currents are used as inputs for the current control, which generates the modulation indices m_C for each phase. The current control uses a conventional PI-controller in a grid synchronous reference frame. The Quasi-Two-Level modulation includes the simple balancing algorithm described in section IV and the two-level modulator for each PEBB of the single phase flying capacitor. The feedback loop between the single phase flying capacitor converter and the Quasi-Two-Level modulation exist because the simple balancing algorithm is required it. The balancing algorithm uses the measured capacitor voltages for the determination of future switching sequences. The output of the Quasi-Two-Level modulation are the gate signals for each PEBB.

VII. Simulations Results

The operation principle of the Quasi-Two-Level FC converter presented in this paper is verified with the following simulation results. Figure 7 depicts the results of the balancing algorithm for a single phase of the flying capacitor for four fundamental periods of the grid voltage. Only the stationary operating point with maximum grid current is shown. The individual modulation indices m_x are changed twice per modulation period $n_s = 2$. In the upper diagram, the grid voltage is shown. The second diagram shows the grid current. The third diagram shows the different capacitor voltages. The last diagram shows the capacitor currents. The size of the flying capacitors is designed according to eq. (5). It can be seen that the deviations of the capacitor voltages depend on

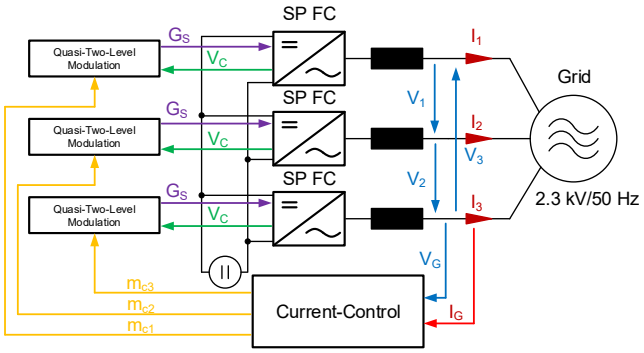

Fig. 6. Simulation model for the Quasi-Two-Level operation of the flying capacitor converter system with control, modulation and electrical circuit

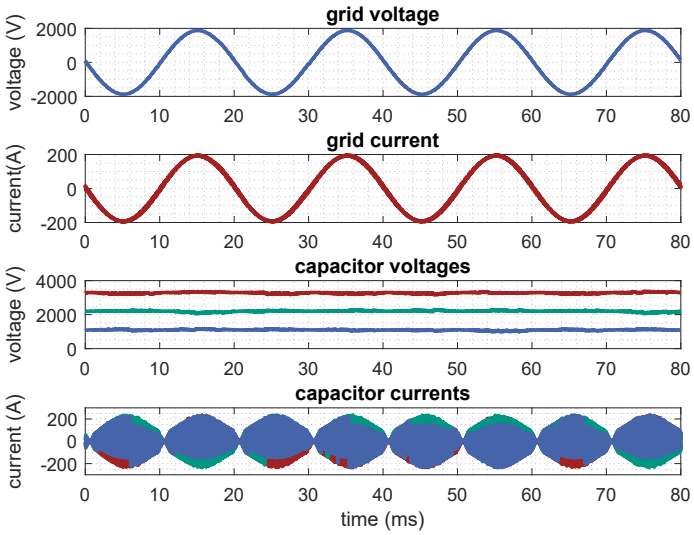

Fig. 7. The balancing results for four grid periods with maximum grid current for Quasi-Two-Level operation of a 5 level single phase flying capacitor converter, it shows the grid voltage, the grid current, the capacitor voltages and currents (red, green and blue are $C_1 - C_3$)

the current. The largest deviation occurs at maximum grid current. The deviation of the capacitor voltages also depends on which capacitor is used longest by the algorithm, that is the first dominant capacitor $c1, do$. This can be detected exactly in the change of the capacitor currents. If the dominant capacitor vector changes, the distribution changes. The stationary case is not a challenge for the algorithm, therefore other cases are shown in the following paragraphs.

Figure 8 depicts a negative switching sequence with the capacitor current and the voltage stress of the MOSFET's near the maximum grid current of fig. 9. The time axis corresponds to the axis from fig. 7. In the upper diagram, the converter output voltage is shown. The second diagram shows the capacitor currents. The different currents flow through the capacitors during a switching sequence, leading to an unequal charging of the capacitors. The time of the current flow and the direction can be different for each capacitor. The third plot shows the drain-source voltages across the power semiconductors. Therein, the different voltage stress for the

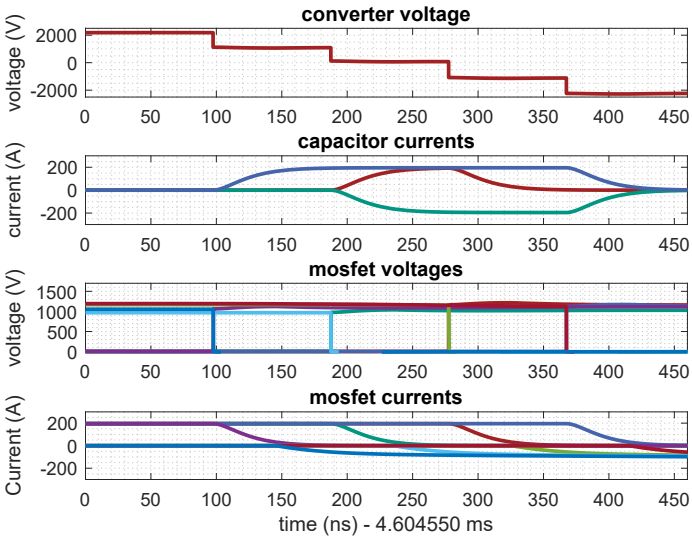

Fig. 8. Quasi-Two-Level operation for one negative switching sequence for a 5-level single phase flying capacitor converter, it shows the converter voltage, the capacitor currents (red, green and blue are $C_1 - C_3$) and the eight MOSFET voltages and eight MOSFET currents.

semiconductors caused by deviations of the capacitor voltages can clearly be seen. The deviance of the nominal voltage can be up to $2 \cdot \Delta v_{c,max}$, since the deviance of the capacitor voltage can be opposite. The small overvoltage stress is due to the sequential switching and the smallest possible commutation path. The last plot shows the drain currents of the power semiconductors. It can be seen that the MOSFET current becomes zero before the next MOSFET is switched. This indicates that the commutation is complete before the next one begins. If this wouldn't be the case, the commutation path would not be inside a PEBB. The MOSFET current is larger for positive current than for negative current, since positive current is only flowing through the MOSFET and negative current is distributed among MOSFET and intrinsic diode.

Figure 9 presents the results of the balancing algorithm with a delayed activation of the algorithm at maximum grid current. The balancing algorithm is activated at $t = 3\,\mathrm{ms}$. Without balancing, the switching sequences are constant and the capacitor current are not symmetrical. This results in deviations of the capacitor voltages, which would normally lead to a shutdown during operation, as the deviations would be too large for the semiconductors. The algorithm balances the capacitor voltages and reaches the nominal voltages after several grid periods. Every time a capacitor voltage has the largest deviation, the distribution of the capacitor currents between the capacitors changes fundamentally. This shows that the algorithm can achieve and maintain capacitor voltage balancing.

Figure 10 shows the results of increase an output power of the flying capacitor converter. The first diagram shows the three phase grid voltages. The second diagram depicts the three phase grid currents. The reference currents are linearly increased and thereby lead to a higher active and reactive output power of the converter. The third diagramm shows the nine capacitor voltages of the three-phase converter. The

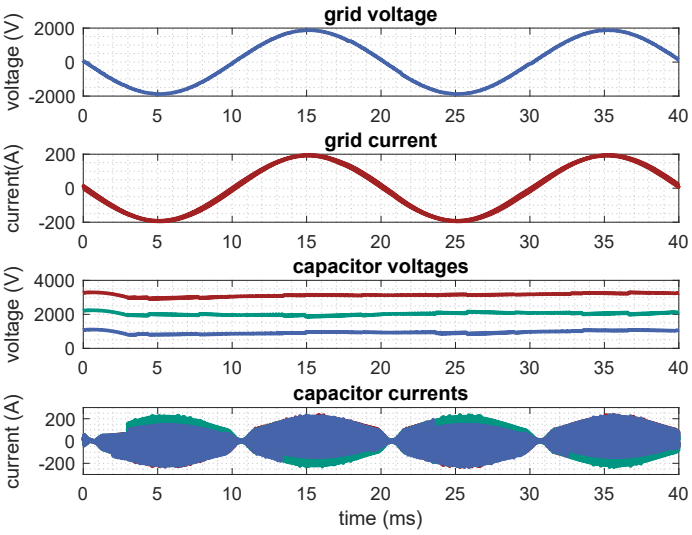

Fig. 9. The balancing results with a delayed activation of the algorithm for Quasi-Two-Level operation of a 5 level single phase flying capacitor converter, it shows the grid voltage, grid current, the capacitor voltages and currents (red, green and blue are $C_1 - C_3$)

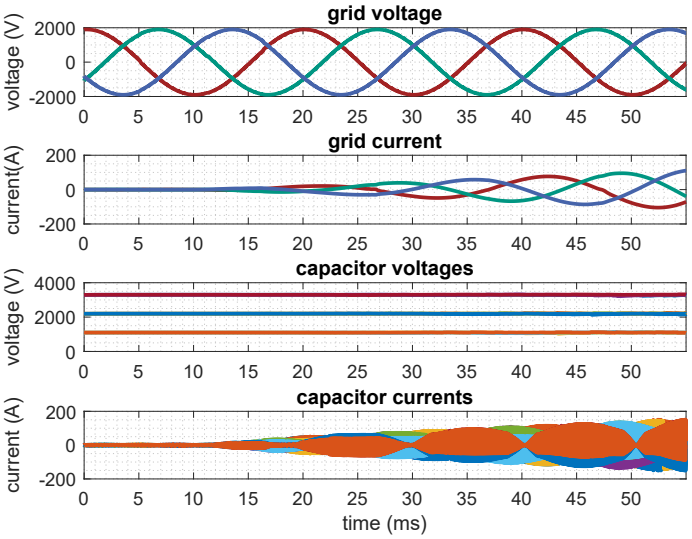

Fig. 10. Increasing output power of Quasi-Two-Level operation of a 5-level three-phase flying capacitor converter, it shows the grid voltage (red, green and blue are phase 1,2 and 3), the grid current (red, green and blue are phase 1,2 and 3), the nine capacitor voltages (red, blue and orange are the voltage level of $C_1 - C_3$) and the nine capacitor currents.

algorithm keeps the capacitor voltages in the range of their nominal voltages $v_{c,nom,i}$.. The last plot depicts the nine capacitor currents, showing that the capacitor currents are phase-symmetrically distributed among the nine capacitors.

Figure 11 shows the different voltage and current loads of the power semiconductors. First, the grid voltages is shown. The second diagram shows the nine capacitor voltages. Likewise, the increase in current causes only a small deviation of the capacitor voltages, however it is only slightly seen in the chosen scale. The voltage stress varies in the range from zero to around 1100 volts, but it is different between the individual MOSFETs. Furthermore, it can be seen that the voltage stress of individual semiconductors increase with

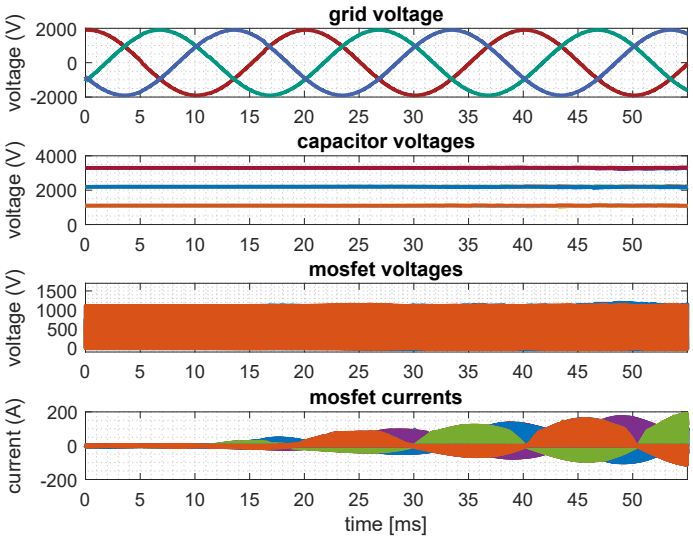

Fig. 11. Increasing output power of Quasi-Two-Level operation of a 5-level three-phase flying capacitor converter. it shows the grid voltage (red, green and blue are phase 1,2 and 3), the nine capacitor voltages (red, blue and orange are the voltage level of $C_1 - C_3$), the 24 MOSFET voltages and the 24 MOSFET voltages.

higher output currents. The distribution of the currents into the individual phases is clearly visible in the 24 MOSFET Currents.

VIII. Conclusion

This paper presents a new operation principle for medium voltage flying capacitor (FC) converters. The Quasi-Two-Level operation allows the utilization of fast switching semiconductors with reduced blocking voltage in medium voltage applications and the mode of operation can directly benefit from the advantages. A concept of modularization is proposed that facilitates fast switching through compact design and thus low-inductance commutation paths. When using a Quasi-Two-Level operation of the flying capacitors, the size of the flying capacitors does not depend on the carrier frequency, but on the switching time of the power semiconductors. Moreover, the switching frequency of the power semiconductors can be adjusted to optimize the losses of the converter system or the size of the output filter. This paper presents a new and simple algorithm for capacitor voltage balancing for Quasi-Two-Level operation and a way to minimize the capacitances by using fast switching semiconductors. It was also shown how much smaller the capacities can be compared to the conventional operating mode. The simulation results verify the algorithm for sinusoidal symmetrical grid voltages and sinusoidal symmetrical grid currents. It has been shown that the algorithm can achieve and maintain capacitor voltage balancing during steady-state and transient operation. This concept fulfills the requirements of the medium voltage level for future grid applications. In the near future, a full scale prototype will be built to validate the concept in a laboratory test.

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