50 GBit/s PAM-4 Driver Circuit Based on Variable Gain Distributed Power Combiner

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***Abstract*— In this work an analog driver circuit for pulse amplitude modulated data signals with four amplitude levels (PAM-4) is investigated. The driver circuit is based on a distributed combining cell, which performs the PAM-4 generation from binary input data streams. Due to the distributed topology, the driver core provides a high analog bandwidth and is well suited for high-speed operation. Since the amplification of both combiner paths can be adjusted individually, the combiner circuit offers predistortion capabilities when driving loads with a nonlinear transfer function. A one-stage prototype circuit using heterojunction bipolar transistors (HBTs) is implemented in a 130 nm SiGe BiCMOS technology. Time-domain measurements prove PAM-4 signal generation at an output bitrate of 50 GBit/s, while the driver consumes a DC power of 63 mW. Additionally, predistortion of the circuit is demonstrated at 25 GBit/s, leading to a variable vertical spacing of the amplitude levels.**

***Index Terms*— Distributed combiner, PAM-4, SiGe.**

I. Introduction

To increase the spectral efficiency of communication systems, the transmission of PAM signals instead of binary signals is of great interest. To convert multiple binary data streams into a PAM signal typically digital-to-analog converters (DAC) are used. At high data rates the implementation of conventional DAC topologies becomes challenging due to tight timing requirements [1] and limited bandwidth, especially in topologies using a lumped output stage [2]. In [3] a time-interleaving DAC using distributed clock and output lines to overcome bandwidth limitations is presented, demonstrating a 50 GBaud PAM-4 signal. A completely distributed DAC approach featuring high bandwidth and high output power is presented in [2]. Another technique to overcome bandwidth limitations is frequency band interleaving, realized with multiple DACs connected to mixer circuits and a passive multiplexer which combines the individual frequency spectra to a very broadband signal [4]. In addition to multi-purpose DACs, in CMOS technologies also the implementation of synchronous PAM-4 transmitters including equalization circuitry is popular to overcome bandwidth limitations (e.g. [5]). Since the benefits of synchronous circuits like the retiming capabilities are not necessary in all applications, the use of low-complexity PAM drivers operating without a clock signal becomes quite attractive, thus eliminating the power consumption of the clock circuitry. A simple way to create a PAM-4 signal from binary input signals is a passive power combiner with one input signal attenuated by 6 dB [6]. To overcome disadvantages of this passive solution like combiner losses and low isolation, transistor based PAM driver circuits have been proposed, especially in the area of vertical-cavity surface-emitting lasers [7] [8]. Similar to current summing DAC circuits, these PAM drivers are typically based on lumped amplifying and combining stages, leading to limited suitability for applications which demand both high bandwidth and high output power. To overcome this limitation a distributed power combining topology has been proposed to create PAM-4 signals, and a prototype circuit implemented with surface-mount devices on a printed circuit board has been shown in [9].

In this work the realization of a distributed power combiner on chip level is presented, clearly demonstrating the potential of this approach for high-speed operation.

II. Circuit design

The schematic of the investigated PAM-4 driver circuit is depicted in Fig. 1. The prototype circuit is essentially a one-stage distributed power combiner with common-emitter amplifying stages. Similar to the well known circuit topology of the distributed amplifier with only one input, high-ohmic transmission lines are loaded with the capacitive input and output impedances of the gain cells.

Since for PAM-4 generation ideally a 6 dB gain difference has to be established between the two combiner paths, this has to be reflected by different gain magnitudes of the two amplifying cells. To adjust the gain difference of the two combiner paths, the base bias voltages V_{B1} and V_{B2} can be changed, which are provided by off-chip bias tees. If the base voltage is reduced, also the collector current is reduced, which leads to a decrease of the transistor's transconductance and therefore the gain of the amplifying cell.

The circuit is implemented in IHP's SG13S SiGe BiCMOS technology, which provides HBTs having a transit frequency of 240 GHz and a seven layer metal stack. The input and output lines are implemented as microstrip lines with the signal conductor located in the uppermost thick metal layer, and the ground plane located in the lowermost

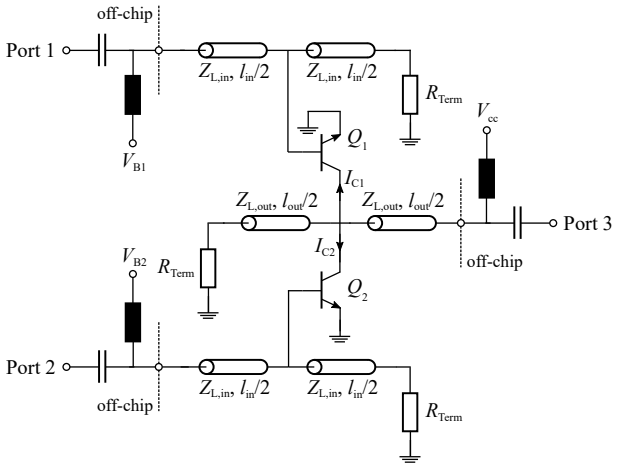

Fig. 1. Schematic of the one-stage distributed combiner. Emitter areas of Q_1, Q_2 are $A_E = 6 \times 0.12 \times 0.48\,\mu\text{m}^2$. At ≈ 6 dB gain difference the simulated DC bias values are $V_{B1} = 962$ mV, $V_{B2} = 886$ mV, $V_{cc} = 1$ V, $I_{C1} = 8.0$ mA, $I_{C2} = 2.0$ mA. $|Z_{L,in}| = 95\,\Omega$, $|Z_{L,out}| = 89\,\Omega$, $l_{in} = 533\,\mu$m, $l_{out} = 587\,\mu$m, $R_{Term} = 50\,\Omega$.

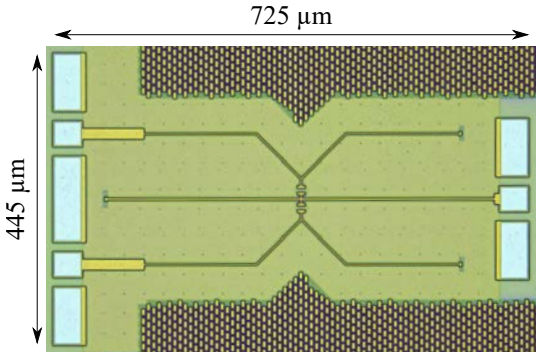

Fig. 2. Photograph of the fabricated circuit. The given dimensions refer to the outer boundaries of the probing pads.

metal layer. In this way high-ohmic transmission lines can be created with high isolation to the lossy silicon substrate. While the input lines exhibit the minimum possible width of $2\,\mu$m, the width of the output line is increased to $3\,\mu$m to account for the higher DC current. The characteristic impedances of the input and output microstrip lines extracted from EM simulations at 50 GHz are $|Z_{L,in}| = 95\,\Omega$ and $|Z_{L,out}| = 89\,\Omega$. Both input and output lines are terminated with $50\,\Omega$ resistors to ensure a flat gain response of the driver down to DC.

III. Measurement Results

A photograph of the fabricated circuit can be seen in Fig. 2. The chip contains probing pads for a ground-signal-ground (GSG) probe at the output and a GSGSG probe at the input.

The measured scattering parameters with varying V_{B2} and constant V_{B1} are shown in Figs. 3 and 4. In the

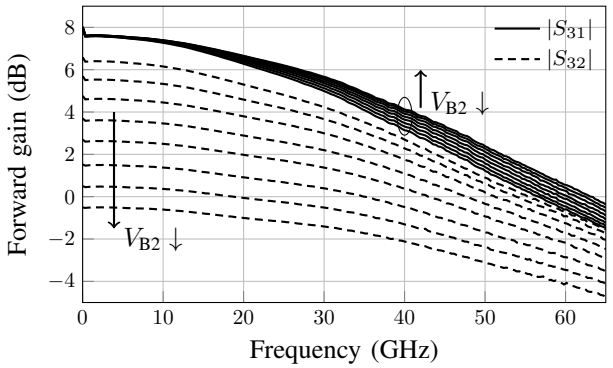

Fig. 3. Measured forward gain of the combiner circuit with varying V_{B2} and constant V_{B1}.

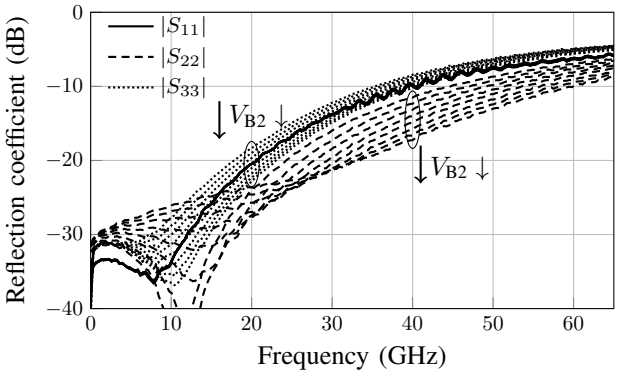

Fig. 4. Measured reflection coefficients of the combiner circuit with varying V_{B2} and constant V_{B1}.

bias state with about 6 dB gain difference the bandwidth is 36 GHz in the high gain path and 48 GHz in the low gain path. From the measured group delay depicted in Fig. 5 one can observe a delay difference smaller than 1.4 ps from 0.5 to 64 GHz in the bias state with about 6 dB gain difference. The group delay data have been averaged using five frequency points for frequencies larger than 2 GHz to reduce the impact of the noisy phase measurement data.

Time-domain measurements were performed using a MP1758A pulse pattern generator delivering pseudo-random binary sequence data signals with order 31 (PRBS-31), and the circuit's output signal was captured by a DCA-J 86100C sampling oscilloscope. In Fig. 6 the driver's PAM-4 output eye diagram at a baudrate of 25 GBaud is shown, corresponding to a bitrate of 50 GBit/s. Besides the amplitude levels with nearly equidistant spacing shown in Fig. 6, the analog predistortion capability of the combiner is shown in Fig. 7 at a bitrate of 25 GBit/s, where the gain difference between the two combiner paths is changed. By applying predistortion, nonlinear transfer functions of the following component in a communication system, e.g. a Mach-Zehnder modulator, can be equalized. In the bias state corresponding to the 50 GBit/s measurement, the

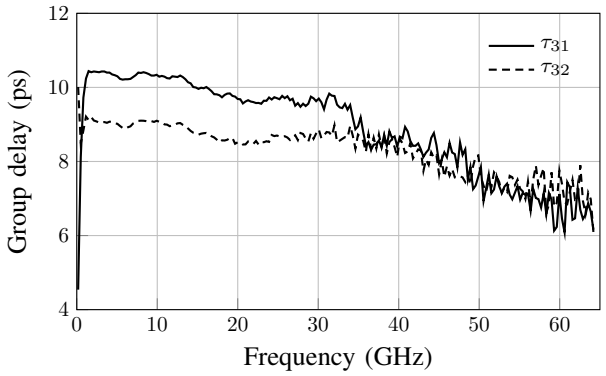

Fig. 5. Measured group delay of the combiner circuit at ≈ 6 dB gain difference between the paths.

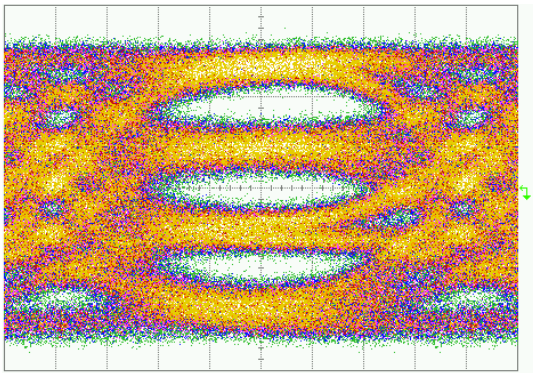

Fig. 6. Output eye diagram of the driver circuit when driven with two 25 GBit/s PRBS-31 input signals. Horizontal scale: 5 ps/div, vertical scale: 30 mV/div.

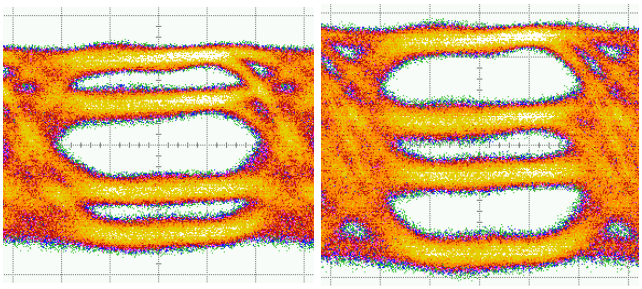

Fig. 7. 25 GBit/s output eye diagrams of the driver circuit with (a) increased and (b) decreased gain difference of the two combiner paths. Horizontal scale: 15 ps/div, vertical scale: 50 mV/div.

circuit has a DC power consumption of 63 mW. Since about 80% of the DC power are dissipated from the line termination resistors, there is a great potential to reduce the power consumption with terminations consisting of a series resistor and a large bypass capacitor. Thus, also the biasing of the circuit could be realized via the ends of the lines without the need for bias-tees.

IV. Conclusion

In this work the implementation of a PAM-4 driver circuit based on a distributed combining cell in a SiGe BiCMOS technology has been succesfully demonstrated. Despite the simplified topology using only one stage and a common-emitter amplifying cell, the circuit shows high analog bandwidth and the PAM-4 signal generation is verified by time-domain measurements. The investigated distributed combining cell is therefore a candidate with high potential for ultra-high bandwidth applications.

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