Karlsruher Institut für Technologie

Implementation and Characterisation of Monolithic CMOS Pixel Sensors for the CLIC Vertex and Tracking Detectors

Zur Erlangung des akademischen Grades eines

DOKTOR-INGENIEURS

von der KIT-Fakultät für
Elektrotechnik und Informationstechnik
des Karlsruher Instituts für Technologie (KIT)
genehmigte

DISSERTATION

von

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geb. in: Cholargos, GR

Tag der mündlichen Prüfung: 27.01.2020

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Abstract

Different CMOS technologies are being considered for the vertex and tracking layers of the detector at the proposed high-energy e^+e^- Compact Linear Collider (CLIC). CMOS processes have been proven to be suitable for building high granularity, large area detector systems with low material budget and low power consumption. An effort is put on implementing detectors capable of performing precise timing measurements. Two Application-Specific Integrated Circuits (ASICs) for particle detection have been developed in the framework of this thesis, following the specifications of the CLIC vertex and tracking detectors. The process choice was based on a study of the features of each of the different available technologies and an evaluation of their suitability for each application.

The CLICpix Capacitively Coupled Pixel Detector (C3PD) is a pixelated detector chip designed to be used in capacitively coupled assemblies with the CLICpix2 readout chip, in the framework of the vertex detector at CLIC. The chip comprises a matrix of 128×128 square pixels with 25 μm pitch. A commercial 180 nm High-Voltage (HV) CMOS process was used for the C3PD design. The charge is collected with a large deep N-well, while each pixel includes a preamplifier placed on top of the collecting electrode. The C3PD chip was produced on wafers with different values for the substrate resistivity ($\sim$ 20, 80, 200 and 1000 Ωcm) and has been extensively tested through laboratory measurements and beam tests. The design details and characterisation results of the C3PD chip will be presented.

The CLIC Tracker Detector (CLICTD) is a novel monolithic detector chip developed in the context of the silicon tracker at CLIC. The CLICTD chip combines high density, mixed mode circuits on the same substrate, while it performs a fast time-tagging measurement with 10 ns time bins. The chip is produced in a 180 nm CMOS imaging process with a High-Resistivity (HR) epitaxial layer. A matrix of 16×128 detecting cells, each measuring 300×30 μm^2, is included. A small N-well is used to collect the charge generated in the sensor volume, while an additional deep N-type implant is used to fully deplete the epitaxial layer. Using a process split, additional wafers are produced with a segmented deep N-type implant, a modification that has been simulated to result in a faster charge collection time. Each detecting cell is segmented into eight front-ends to ensure prompt charge collection in the sensor diodes. A simultaneous 8-bit timing and 5-bit energy measurement is performed

in each detecting cell. A detailed description of the CLICTD design will be given, followed by the first measurement results.

Zusammenfassung

Verschiedene CMOS-Technologien werden für die Vertex- und Tracking-Detektoren des Multi-TeV e^+e^- Compact Linear Collider (CLIC) Projekts in Betracht gezogen. CMOS-Prozesse sind hierfür besonders geeignet, da sie es ermöglichen, hochgranulare und großflächige Detektorsysteme mit geringem Materialbudget und niedrigem Stromverbrauch zu bauen. Derzeit werden Detektoren entwickelt, die darüber hinaus auch präzise Zeitmessungen ermöglichen sollen. Im Rahmen dieser Arbeit wurden zwei anwendungsspezifische integrierte Schaltungen (ASICs) zur Detektion von ionisierenden Teilchen entwickelt, die den Spezifikationen der CLIC-Vertex- und Tracking-Detektoren genügen. Die Wahl der Prozesse basiert auf einer umfassenden Studie der Eigenschaften verschiedener verfügbarer Technologien sowie einer Bewertung ihrer Eignung für die jeweilige Anwendung.

Der CLICpix Capacitively Coupled Pixel Detector (C3PD) ist ein Pixeldetektor-Chip, der für den Einsatz als Sensor in kapazitiv gekoppelten Detektoren mit dem Auslesechip CLICpix2 für den CLIC Vertexdetektor entwickelt wurde. Der C3PD-Chip verfügt über eine Matrix von 128×128 quadratischen Pixeln mit einer Seitenlänge von 25 µm und wurde in einem 180 nm High-Voltage (HV)-CMOS-Prozess implementiert. Die Ladung wird mithilfe einer großen N-dotierten Elektrode gesammelt, die den in jedem Pixel implementierten Vorverstärker umgibt. Der C3PD-Chip wurde auf Wafern mit unterschiedlichen Substratwiderständen hergestellt ($\sim$ 20, 80, 200 und 1000 Ωcm) und mithilfe von Labormessungen sowie Messungen an Teststrahlen umfassend getestet. In der vorliegenden Arbeit werden Details zum Chip-Design sowie Charakterisierungsergebnisse des C3PD-Chips vorgestellt.

Der CLIC Tracker Detector (CLICTD) ist ein innovativer monolithischer Detektorchip, der für den CLIC Silizum-Trackingdetektor entwickelt wurde. Der CLICTD-Chip kombiniert analoge und digitale Schaltkreise auf dem gleichen Substrat und ermöglicht eine präzise Messung der Ankunftszeit von Teilchen mit einer Genauigkeit von unter 10 ns. Der Chip wird in einem 180 nm CMOS-Imaging-Prozess mit einer hochohmigen (HR) epitaktischen Siliziumschicht hergestellt und umfasst eine Matrix aus 16×128 Detektorzellen mit einer Größe von jeweils 300×30 µm^2. Eine kleine N-dotierte Elektrode wird verwendet, um die erzeugten Ladungsträger zu sammeln, während ein zusätzliches, tiefes N-Implantat eine voll-

ständige Ladungsträgerverarmung der epitaktischen Schicht ermöglicht. Durch einen sogenannten Prozess-Split werden zusätzliche Wafer mit einem segmentierten tiefen N-Implantat hergestellt, für das Simulationen eine Beschleunigung der Ladungssammlung vorhersagen. Jedes der Pixel ist in acht Sensor-Segmente unterteilt, um eine schnelle Ladungssammlung in den einzelnen Zellen zu gewährleisten. Der Chip ermöglicht eine simultane 8-Bit-Zeit- und 5-Bit-Energiemessung in jeder Detektorzelle. Die vorliegende Arbeit enthält eine detaillierte Beschreibung des CLICTD-Designs sowie erster Messergebnisse.

Acknowledgements

At this point I would like to thank and acknowledge everyone who contributed to this work. Completing this PhD thesis would not have been possible without their assistance and collaboration.

First, I would like to thank my supervisor at CERN, Rafael Ballabriga, for his overall help, support and collaboration while I was working on my thesis. I would also like to thank him for the design of the C3PD analog front-end and the CLICTD analog front-end and analog periphery.

I would also like to thank my supervisor at KIT, Ivan Peric, for accepting me as a PhD student under his supervision, for his guidance during these years, and for sharing the CCPDv3 design, which was the starting point for the design of the C3PD chip.

I would like to express my gratitude to Lucie Linssen, Michael Campbell and Dominik Dannheim for their trust and support during the years that I was working on my thesis.

Special thanks to all my colleagues at CERN who contributed to this work. Xavi Llopart for always being available to help and answer my questions on the digital design, timing analysis and chip integration. Szymon Kulis for his overall help with the C3PD chip design and characterisation. Andreas Nurnberg, Simon Spannagel and Tomas Vanat for their help with the DAQ systems. Matthew Buckland and Daniel Hynds for their input on the C3PD design. Adrian Fiergolski for verifying the digital logic of the C3PD chip. Walter Snoeys, Thanushan Kugathasan and Magdalena Munker for their valuable input on the CLICTD chip design. Nuria Egidos for verifying the CLICTD chip. Jerome Alozy for his advice on my PCB designs. Katharina Dort for her contribution to the CLICTD characterisation.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 654168.

I first came to CERN in 2014 as a Technical Student. Thanks to Sandro Bonacini and Kostas Kloukinas for giving me the chance to join the CERN microelectronics section.

I would also like to thank Grigorios Kalyvas and the dearly departed Kostas Efstathiou for supervising my diploma thesis during my studies in the University of Patras.

Finally, I would like to thank my family for their support over these years, the friends I made during my stay in the area of Geneva, and my friends from Keratsini and Patra.

Ηρακλής Κρεμαστιώτης

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Chapter 1

Introduction

A question that has intrigued the humanity and was the subject of philosophical quests since the ancient times is the understanding of the elements which compose the matter. The ancient Greek philosopher Democritus believed that the matter is composed of discrete, indestructible, invisible to the human eye elements, the "atoms". It took several centuries for this idea to move from the theoretical wording to the field of natural sciences. The Standard Model of particle physics is the current description of the subatomic particles and their interactions. It has been a subject of study for decades, with the Higgs boson (discovered at the CERN LHC in 2012) being the last piece of this model.

One of the instruments that are being used during the past decades in High Energy Physics (HEP) experiments in search of new particles is the particle accelerator. In such a machine, beams of particles are accelerated to very high speeds and energies. The particle beams are then collided and the products of each collision are studied and analysed to potentially discover new particles. Based on the nature of the particles that are collided, the particle accelerators can be divided in two categories: the lepton colliders and the hadron colliders.

In a lepton (or electron-positron - e^+e^-) collider, electrons are collided with positrons (the antimatter complement of the electron). Lepton colliders are suitable for highly precise measurements, thanks to the fact that fundamental particles are collided. They are therefore appropriate for measuring the properties of a particle, such as the Higgs boson, with very good precision. On the other hand, one limitation in lepton colliders is that when an electron is accelerated in a circle, it emits electromagnetic radiation (known as the synchrotron radiation) and is gradually losing its energy. Thus, it is challenging to achieve very high collision energies in a lepton collider. As an example, the Large Electron-Positron (LEP) collider, a circular collider with 27 km circumference, operated at CERN between the years 1989 and 2000, reached a maximum energy of 209 GeV. LEP allowed for precise measurements of the

W and Z bosons (first discovered in the CERN Super Proton Synchrotron - SPS) and helped in understanding the nature of the weak nuclear force.

In a hadron collider, the particle beams consist of hadrons, which are particles composed by quarks. The Large Hadron Collider (LHC) [1] at CERN is the world's largest and most powerful particle accelerator, with a collision energy up to 13 TeV, and the biggest scientific instrument built up to this day. The LHC, which includes four large detector experiments, started its operation in 2008 and is responsible for the discovery of the Higgs boson, which was first described in 1964. The LHC operation is foreseen to continue until the year 2035, with several upgrades through the years. In the LHC, and generally in hadron colliders, the particle beams consist primarily by protons. Heavy ions, such as lead particles, are also collided in hadron accelerators. Protons, and hadrons in general, are not elementary particles as they are composed by quarks. They are a lot heavier compared to the electrons (or positrons) and they emit lower synchrotron radiation. Consequently, higher collision energies can be reached in hadron colliders, which can potentially lead to the production of more massive particles. On the other hand, since hadrons are not fundamental particles, they result in a higher background which imposes further challenges in the data analysis. Another limitation is the fact that strong, and costly, magnets are needed in order to bend the particle beam around the accelerator's ring.

Particle accelerators have so far contributed to momentous discoveries in the physics worlds, with the latest being the discovery of the Higgs boson at the CERN LHC. Although the Higgs boson was the last missing piece of the physics Standard Model, there are still further challenges to be investigated in the physics world. The LHC programme is foreseen to keep running until 2035, however, it is unlikely it will provide explanations to all questions that current physics cannot answer. Future experiments, with higher precision, or with larger collision energies, are currently under study in order to investigate the open questions in the future decades.

Different future accelerators have been proposed for the post-LHC era. The Future Linear Collider (FCC) [2] is a proposed circular collider with a circumference of 100 km and a collision energy up to 100 TeV. It is foreseen to be operated in two stages: first as an electron-positron collider (FCC-ee) and later as a hadron collider (FCC-hh). The losses resulting from synchrotron radiation in electron-positron colliders are eliminated in linear colliders. The International Linear Collider (ILC) [3] and the Compact Linear Collider (CLIC, further described in Chapter 2) [4] are two proposed future linear electron-positron accelerators.

A very important component of such machines is the detector. One or more detectors are placed in caverns along the accelerator tunnel. The detector can be described as a large-scale

three-dimensional digital camera, that records what happens during the particle collisions. Analysing the data stored in the detector can provide information on the particles produced from the collision and potentially lead to the discovery of new particles. A chain of electronic circuits is installed inside the detector in order to collect and store the data from the collisions. The information can be first processed by the front-end electronics (the level of processing depends on the requirements of the detector) before being transmitted and stored externally. Therefore, reliable electronic circuits are crucial for the successful operation of the detector. Developments in electronics are being investigated for a large variety of applications in the different parts of the detector, such as front-end electronics, signal processing, trigger systems and high-speed links.

This thesis presents the design and characterisation of two Application Specific Integrated Circuits (ASICs) targeted at the CLIC detector. The first ASIC was designed in the context of the CLIC vertex detector study, and the second for the CLIC silicon tracker. In Chapter 2, a brief introduction to the CLIC experiment and a synopsis of the CLIC detector are given. Chapter 3 presents an overview of the different technologies used for implementing integrated circuits for particle detectors. The design of a HV-CMOS chip, the CLICpix Capacitively Coupled Pixel Detector (C3PD), in view of the CLIC vertex detector is explained in Chapter 5. Characterisation results with the C3PD chip are presented in Chapter 6. Next, the design of a monolithic HR-CMOS chip, the CLIC Tracker Detector (CLICTD), targeted at the CLIC silicon tracker is described in Chapter 7. This is followed by the first measurement results with the CLICTD chip in Chapter 8. Last, a summary of the two chip designs and conclusions based on the measurement results are given in Chapter 9.

Chapter 2

The Compact Linear Collider

The work presented in this thesis was carried out in the framework of the Compact Linear Collider (CLIC) study. CLIC is a proposed linear electron-positron (e^+e^-) collider with a centre-of-mass energy up to 3 TeV [4]. The collider, which is currently in the Research and Development (R&D) phase, is envisaged to be built near the European Organisation for Nuclear Research (CERN) facilities in the area of Geneva, as presented in Figure 2.1.

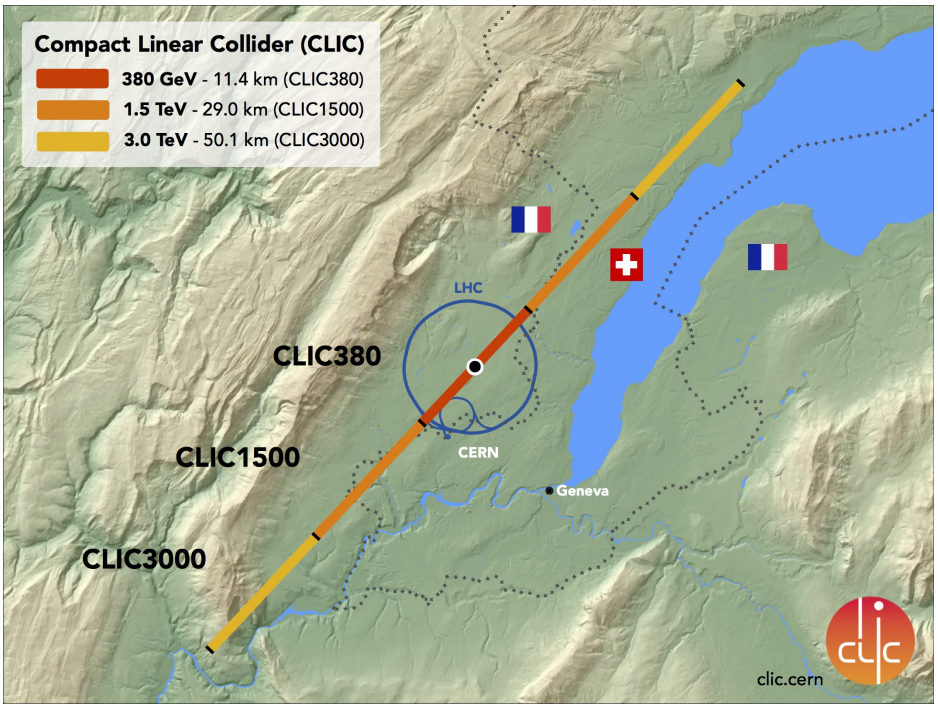


Figure 2.1 The CLIC accelerator footprint near CERN. The three foreseen energy stages are presented. From [5].

2.1 The stages of the CLIC accelerator

Taking advantage of its linearity, the CLIC machine can be modular and its operation can be extended in different stages. Three stages are currently foreseen for the operation of the CLIC accelerator, based on various studies for exploiting the physics potential [6]. First, a shorter linear accelerator (11.4 km) will be built, delivering collisions at a centre-of-mass energy of 380 GeV. The second stage will be a 29.0 km long accelerator with a centre-of-mass energy of 1.5 TeV, before implementing the final upgrade which will be a 50.1 km long accelerator with a centre-of-mass energy of 3 TeV. The layout of the three stages of the CLIC accelerator near CERN and the area of Geneva is presented in Figure 2.1.

The target for the integrated luminosity at each stage is: 500 fb^{-1} at 380 GeV, 1.5 ab^{-1} at 1.5 GeV and 3 ab^{-1} at 3 GeV. The main parameters of the three energy stages of the CLIC accelerator are presented in Table 2.1.

Table 2.1 Main parameters of the three energy stages for CLIC. From [6].

Parameter	**Symbol**	**Unit**	**Stage 1**	**Stage 2**	**Stage 3**
Centre-of-mass energy	$\sqrt{s}$	GeV	380	1500	3000
Repetition frequency	f_{rep}	Hz	50	50	50
Number of bunches per train	n_b		352	312	312
Bunch separation	Δt	ns	0.5	0.5	0.5
Accelerating gradient	G	MV/m	72	72/100	72/100
Total luminosity	$\mathscr{L}$	$10^{34}\text{cm}^{-2}\text{s}^{-1}$	1.5	3.7	5.9
Luminosity above 99% of $\sqrt{s}$	$\mathscr{L}_{0.01}$	$10^{34}\text{cm}^{-2}\text{s}^{-1}$	0.9	1.4	2
Main tunnel length		km	11.4	29.0	50.1
Number of particles per bunch	N	10^9	5.2	3.7	3.7
Bunch length	σ_z	µm	70	44	44
IP beam size	σ_x/σ_y	nm	149/2.9	$\sim 60/1.5$	$\sim 40/1$
Estimated power consumption	P_{wall}	MW	252	364	589

2.2 The CLIC beam structure

The beam in the CLIC machine is composed of 312 bunches of electrons or positrons forming a bunch train. The bunches are separated by 0.5 ns for a total bunch train duration of 156 ns. Subsequent bunch trains are repeated every 20 ms. This 50 Hz repetition frequency of the CLIC beam leads to a low duty cycle (156 ns / 20 ms), as illustrated in Figure 2.2. As no collision will be produced during the inactive time, it can be used for reading out the data acquired during the collisions. A trigger-less readout is therefore planned for the CLIC

detector, as the acquired data can be read out between two subsequent bunch trains. In addition, part of the front-end electronics implemented in the different detecting layers can be switched off between acquisitions in order to lower the average power consumption in the detector.

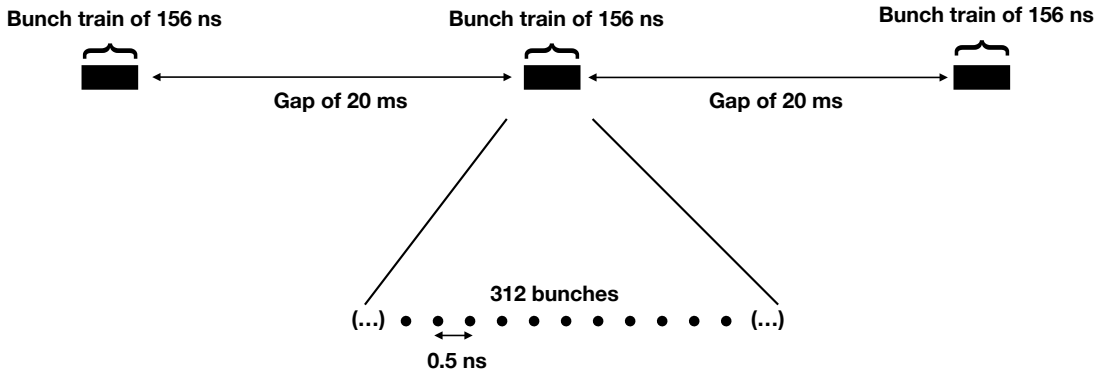


Figure 2.2 The CLIC beam structure (not to scale). From [7].

2.3 Overview of the CLIC detector

The CLIC detector, presented in Figure 2.3, has a cylindrical shape with 12.8 m height and 11.4 m length [8]. The interaction point is at the centre of the detector, and different layers are installed in order to extract the information from the collisions.

The CLIC detector consists of the following six concentric cylindrical layers (from innermost to outermost layer):

- Vertex detector
- Silicon tracker
- Electromagnetic calorimeter
- Hadronic calorimeter
- Superconducting solenoid magnet
- Yoke and muon detectors

In addition, two more calorimeters are installed in the very forward region: the luminosity calorimeter (LumiCal) and the beam calorimeter (BeamCal).

A detailed description of the different building blocks of the CLIC detector is presented in the section below, where more emphasis is put on the vertex and tracking detectors, as the work carried out for this dissertation is focused on these two detecting layers.

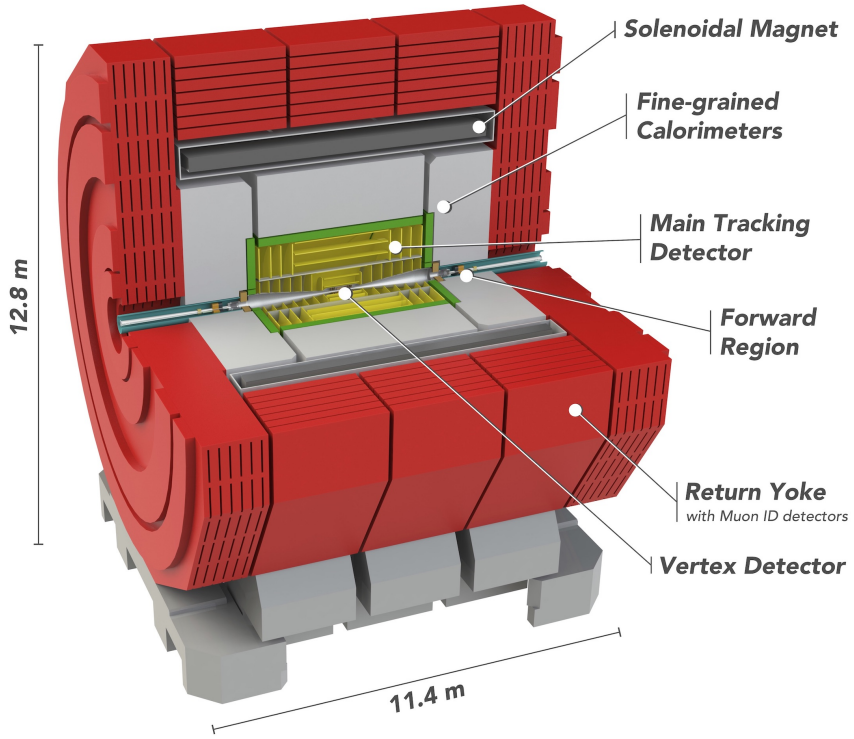


Figure 2.3 The CLIC detector. From [9].

2.3.1 Vertex detector

The vertex detector in the CLIC experiment, is primarily used for delivering efficient tagging of decays involving heavy quarks or tau-leptons by reconstructing their displaced vertices [4]. In addition, along with the tracking system, it provides information for precise and efficient track reconstruction, in particular for low-momentum tracks.

As illustrated in Figure 2.4, the vertex detector consists of three cylindrical barrel layers installed around the interaction point [8]. The inner radius of the barrel layers varies from 31 mm (inner layer) to 60 mm (outer layer). The length of the barrel layers is 260 mm, for a total sensor area of 0.487 m^2. In the forward region, three "disks" are installed in each side of the barrel, perpendicular to the beam pipe. The disks are arranged such that they create a spiral, to facilitate the air-flow cooling. The total sensor area of all disks is 0.351 m^2. In both barrel and forward region each layer is double-sided, meaning that sensitive layers are placed on both sides of the layer. In the barrel layers, the detector electronics are arranged in staves, while the disks in the forward region are built using trapezoid petals.

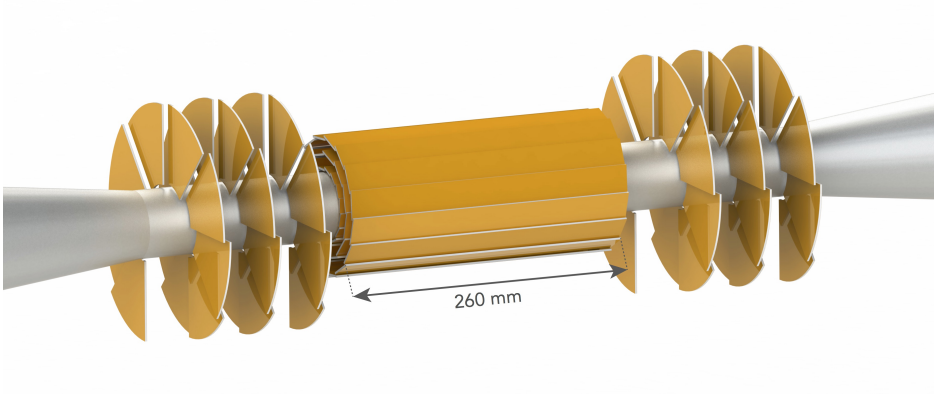


Figure 2.4 3-D model of the CLIC vertex detector. From [9].

To achieve the required precision for the physics measurements, a single point resolution of 3 µm is aimed for in both directions. Based on simulations, this resolution can be reached with 25×25 μm^2 pixels, after extrapolating the information from the charge sharing in the sensor. Regarding the material budget, it is limited to 0.2% of the radiation length (X_0) for each of the detection layers (ie. 0.4% X_0 per double layer). This very low material budget impacts the thickness of the silicon layers. Taking into account the material used for support structures and connectivity, each sensor layer should be assembled using 50 µm thick sensors on 50 µm thick readout ASICs. The required material budget implies that no additional cooling structures can be installed in the vertex detector layers. Thus, a forced air flow cooling is foreseen for dissipating the heat produced by the detector electronics. To avoid overheating, the power consumption of the detector electronics should be limited to

$50\,\mathrm{mW/cm^2}$. It is possible to achieve this power consumption without compromising the performance of the detector by powering off part of the electronics between bunch trains of the CLIC beam (power pulsing). Additionally, a time-tagging resolution of 10 ns is required for suppressing the background hits in the detector layers.

Regarding the radiation levels expected for the CLIC vertex detector, the expected Total Ionising Dose (TID) and Non-Ionising Energy Loss (NIEL) are < 1 kGy and $< 10^{11}$ $\mathrm{n_{eq}/cm^2/year}$ respectively. These values are much lower than the ones for the LHC experiment and therefore no radiation-hard electronics are foreseen for the CLIC detector.

2.3.2 Silicon tracker

The purpose of the tracking system is to precisely measure the momentum and trajectory of charged particles resulting from the collisions. The foreseen silicon tracker at CLIC has a radius of 1.5 m and a half-length of 2.2 m [8, 10]. The tracker, presented in Figure 2.5, is split into two regions: the "Inner Tracker" and the "Outer Tracker", divided by the support tube. The Inner Tracker comprises three barrel layers, plus seven disks on each side of the barrel. In the Outer Tracker, three barrel layers are installed, with four disks on each side. The total foreseen area of the tracking detector is approximately $100\,\mathrm{m^2}$.

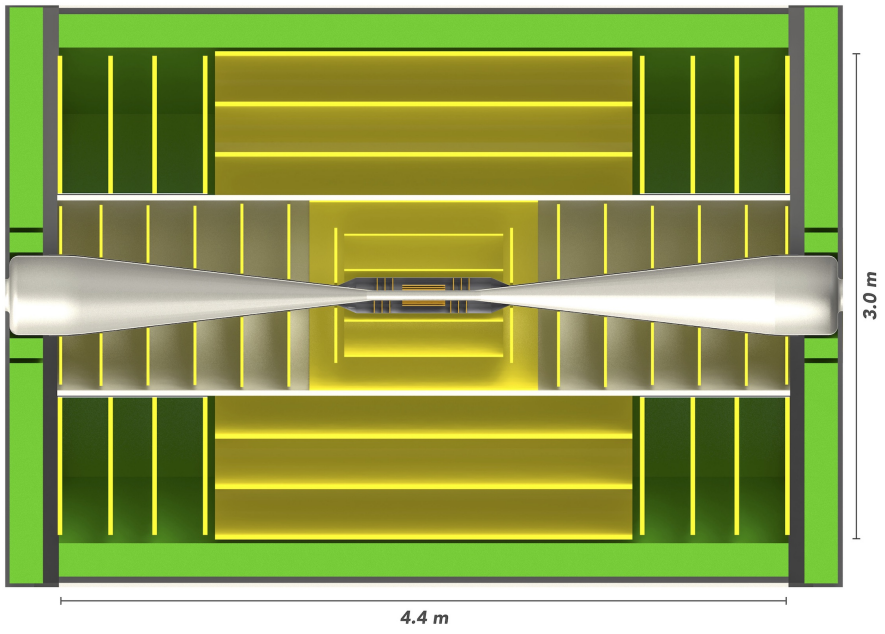


Figure 2.5 3-D model of the CLIC tracking detector. From [9].

To meet the physics requirements, a single point resolution of $7\,\mu\mathrm{m}$ is needed in the transverse plane. In order to cover the large detector area, and given the relaxed requirement

for spatial resolution, monolithic technologies are foreseen for the detector electronics in the CLIC silicon tracker. The detecting cell dimension in the transverse plane is therefore imposed by the required single point resolution, depending also on the amount of charge sharing between neighbouring cells. The cell area is defined by the target cell occupancy of $\leq 3\%$. Table 2.2 summarizes the cell sizes for the different layers of the CLIC tracker. Although the "Inner disc 1" is part of the tracking detector, it should follow the technology of the vertex detector layers to achieve the required performance.

Table 2.2 Cell sizes in the CLIC tracker. From [10].

Detector layers	**Cell length [mm]**	**Cell width [mm]**
Inner barrel 1–2	1	0.050
Inner barrel 3	5	0.050
Outer barrel 1–3	10	0.050
Inner disk 1	0.025	0.025
Inner disks 2–7	1	0.050
Outer disks 1–4	10	0.050

The material budget in the tracking region is $1 - 1.5\%$ X_0 per detection layer. This includes the sensors and readout ASICs, supports, cables and cooling, allowing for a total thickness of ~ 200 µm for the detector electronics. The required thickness could be effortlessly achieved, especially since monolithic technologies are considered for the electronics. Given the more relaxed material budget (compared to the vertex detector), water cooling is foreseen for the CLIC tracker. The requirement for power consumption of the electronics is now less constraint, and can be up to $150\,\mathrm{mW/cm^2}$. Power pulsed operation is also envisaged for the electronics in the tracking layers. Same as for the vertex detector, a 10 ns time-tagging resolution is needed for suppressing out-of-time background hits.

In the CLIC silicon tracker a TID of < 1 Gy and a NIEL of $< 10^{10}$ n_{eq}/cm^2/year are expected.

2.3.3 Electromagnetic and hadronic calorimeter

Two cylindrical, high granularity, calorimeters are installed in the CLIC detector: the electromagnetic calorimeter (ECAL - drawn in green in Figure 2.3) and the hadronic calorimeter (HCAL - in light grey in Figure 2.3) [8].

The purpose of the ECAL is to measure the energies of photons, electrons and positrons. It is installed around the tracking layers and is based on tungsten absorbers and silicon pad

readout with 5×5 mm^2 cells. The ECAL consists of 40 layers of tungsten absorbers for a total thickness of around 22 X_0, and the barrel radius extends from 1.5 m to 1.7 m.

The next layer in the CLIC detector, the HCAL, is used for measuring the energy of hadrons. The HCAL consists of 60 steel absorber plates with 30×30 mm^2 cells, and extends from 1.74 m to 3.33 m in radius. The scintillator tiles are read out by Silicon Photomultipliers (SiPMs).

2.3.4 Magnet system and muon detection

A superconducting solenoid (in dark grey in Figure 2.3) is foreseen to surround the HCAL in the CLIC detector. In the presence of the magnetic field, the trajectories of the particles produced during the collisions are curved and their momentum can be measured using the trajectory information. The magnetic field strength was chosen to be 4 T, based on simulations [8]. An iron return yoke will be installed around the solenoid (in red in Figure 2.3), while the muon detectors are placed within the yoke. The purpose of the yoke is to contain the magnetic field inside the detector.

Regarding the muon detection, 6 detector layers for muon identification are interleaved within the yoke and an additional layer is located in the barrel, close to the coil. The muon detectors are used for identifying muons with an efficiency $> 90\%$ [4]. Resistive plate chambers (RPCs) with cells measuring 30×30 mm^2 are foreseen for the readout of the muon layers.

2.3.5 Forward region

As introduced above, two additional calorimeters are installed in the very forward region of the CLIC detector. The first is the LumiCal, positioned behind the ECAL endcap and used for luminosity measurements. The second is the BeamCal, which is installed behind the LumicCal and used for monitoring of the beam. Due to the higher expected radiation dose (up to 1 MGy per year), the sensor material in the BeamCal needs to be radiation hard. A zoom in the forward region of the CLIC detector is presented in Figure 2.6.

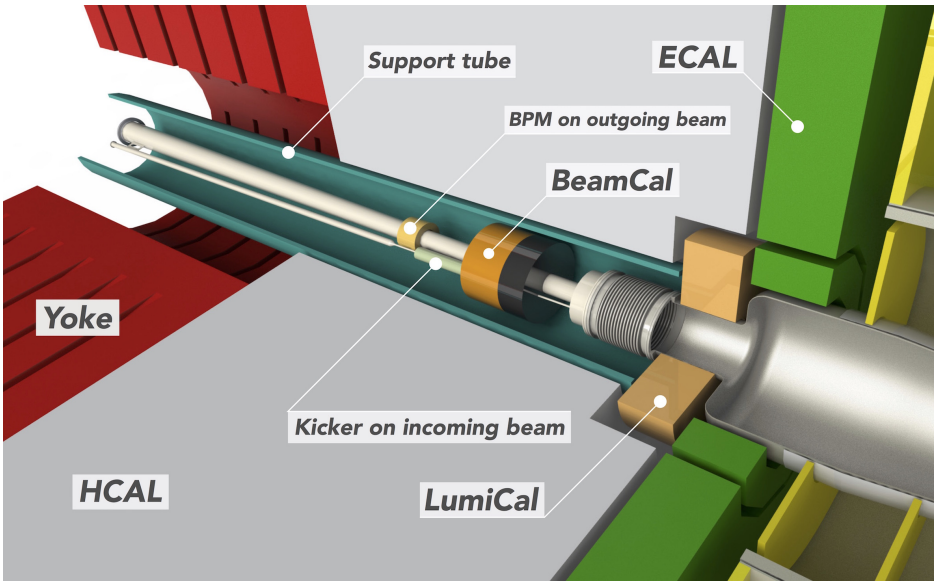


Figure 2.6 A zoom in the CLIC detector forward region. From [9].

Chapter 3

Radiation detectors

The continuously high and rising demands of modern High Energy Physics (HEP) experiments dictated the need for using fast and precise two-dimensional arrays for particle detection [11]. Silicon pixel detectors have been introduced as an efficient way to track particles. Silicon is widely used in the microelectronics industry as it is a commonly found material (being the second in abundance element in the Earth's crust), available at low cost, homogeneous and with well known properties. Two major approaches have been studied, implemented and characterised over the years: monolithic and hybrid devices. Monolithic devices offer an all-in-one-chip solution, where the readout electronics are implemented in the same wafer as the sensor. On the other hand, hybrid devices require an interconnection between their two composites which are placed on different substrates: the sensor and the readout electronics.

Section 3.1 provides general information on the working principle, properties and operation of pixel detectors. In Section 3.2, the hybrid pixel detectors are presented, while Section 3.3 gives an overview of the monolithic technologies. The main aspects of the two approaches will be discussed, and an overview of the different technologies, processes, design considerations, advantages and disadvantages will be presented. Section 3.4 presents a comparison of the different technologies, in the form of general guidelines for selecting the most suitable approach for a given detector application.

3.1 Working principle and operation of pixel detectors

3.1.1 Interaction of radiation with matter

Electromagnetic radiation (photons)

The interaction mechanism of electromagnetic radiation with a detector material varies depending on the energy of the incident photon and the atomic number Z of the absorbing material. The main interaction mechanisms are: the photoelectric effect, the Compton scattering effect, and the pair production. During the interaction, the photon may be absorbed in the sensor material (photoelectric effect or pair production) or scattered and deflected (Compton). The dominant interaction mechanism for a given atomic number and photon energy is presented in Figure 3.1. The probability for an interaction between the incoming photon and a particle in the absorbing material is given by a quantity called cross-section.

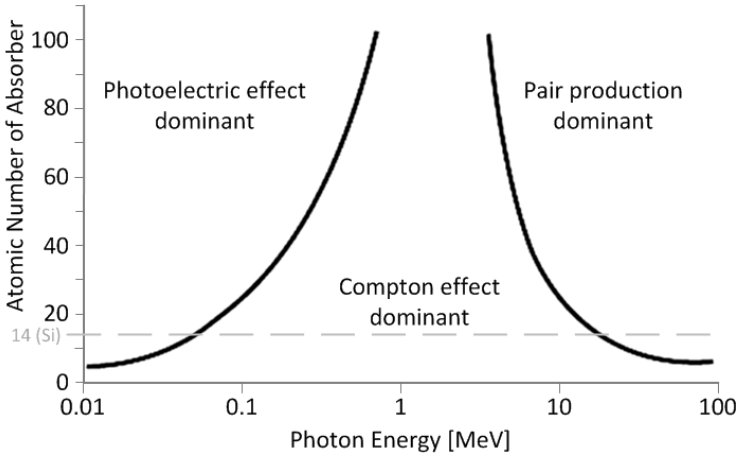


Figure 3.1 Interaction of photons with matter. From [12].

In the photoelectric effect (or photoelectric absorption), an incoming photon is absorbed by an atomic electron in the absorbing material. This will cause the photon to disappear, while a photoelectron is ejected from the atom. The energy of the ejected photoelectron will be equal to the photon energy minus the binding energy of the electron. The resulting photoelectron will interact with the material. This effect is dominant in lower photon energies (below 57 keV for the case of silicon absorbers) and its cross-section is proportional to Z^n, where Z is the atomic number of the absorbing material and n a factor between 4 and 5, depending on the energy of the photon. For this reason, silicon is used for photon detection for energies up to $\sim$ 20 keV, while higher Z materials are preferred for detecting higher energy photons.

In Compton scattering, the photon interacts with an electron in the detector material that is considered free for the transfer of energy. The assumption that the electron is free can be true only in higher energies. In this mechanism, the impinging photon will lose part of its energy to an electron. The scattered photon, which will keep part of its initial energy, may leave the material without interacting or may interact again with another particle. The cross-section of this mechanism is linearly proportional to the atomic number Z of the material.

For energies above 1.022 MeV, the pair production mechanism becomes relevant. In this mechanism, the photon interacts with a nucleus (or electron) and its energy is fully transformed to an electron-positron pair. This is the only important interaction mechanism for photon energies above 10 MeV and its cross-section is proportional to Z^2.

The average number of electron-hole pairs created by a single photon in a detector material, when interacting through photoelectric effect and depositing all its energy in the material, is given by Equation 3.1:

$$N = \frac{E_{ph}}{E_{eh}} \tag{3.1}$$

where E_{ph} is the single photon energy and E_{eh} the energy required to create one electron hole pair (ionisation energy). The ionisation energy in silicon is 3.62 eV at 300 K [13]. This number (N) is subject to statistical variations, as described by Equation 3.2:

$$\langle \Delta N^2 \rangle = FN = F\frac{E_{ph}}{E_{eh}} \tag{3.2}$$

where F is the Fano factor [14]. The Fano factor is a function of the temperature and, for low energies (below 1 keV), of the energy of the photon, and for silicon its value is between 0.07 and 0.16.

Charged particles

When a charged particle interacts with the detector medium, it deposits part of its energy on the material. This deposited energy is translated into electrical signal in the sensor material, which is then processed and read out by the detector electronics. Estimating the properties of the generated electrical signal is therefore important for the detector design. The mean rate of energy loss due to ionisation is described by the Bethe-Bloch formula [15]:

$$-\left\langle \frac{dE}{dx} \right\rangle = Kz^2 \frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\frac{2m_e c^2\beta^2\gamma^2 W_{max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right] \tag{3.3}$$

where:

K	$4\pi N_{Av} r_e^2 m_e c^2 = 0.307075$ MeV cm^2
N_{Av}	Avogadro's number
r_e	classical electron radius
m_e	electron mass
c	speed of light
z	charge of the incident particle in electrons
Z	atomic number of absorption medium
A	atomic mass of absorption medium
β	velocity of the traversing particle in units of the speed of light
γ	Lorentz factor
W_{max}	the kinetic maximum energy which can be transferred to an electron by a charged particle
I	mean excitation energy
δ	density-effect correction

A Minimum Ionising Particle (MIP) is a particle whose energy loss is close to the minimum of the Bethe-Bloch formula in Equation 3.3, which is slightly higher than 1 MeV. In thick silicon sensors, an impinging MIP produces around 80 electron-hole pairs per µm traversed.

The Bethe-Bloch formula in Equation 3.3 returns the average value of the energy loss. However, the energy loss is subject to statistical fluctuations described by the Landau distribution [16]. An important parameter of the Landau distribution is the Most Probable Value (MPV) of the energy loss. Due to the asymmetry of the Landau distribution, there is a significant probability of high signals.

The thickness of the material also impacts the distribution: the thinner the sensor material, the wider the distribution. For thin silicon sensor layers (thinner than a few hundreds of µm), deviations are also observed in the deposited energy per traversed µm [17]. The MPV for the energy deposited on a 10 µm thin silicon sensor can be as low as 50 electron-hole pairs per µm.

3.1.2 The diode

A diode (or p-n junction) is formed by bringing two parts of a semiconductor to contact, where one is P-type doped (anode) and the other is N-type doped (cathode) [18]. N-type doped semiconductor means that the number of the free negative charge carriers (electrons) is higher than the number of the free positive charge carriers (holes) in the material. The opposite (more free holes than free electrons) is a P-type doped semiconductor. The diode is formed at the contact area between the two adjacent parts.

Due to the gradient in charge carrier concentration, electrons in the N-type semiconductor diffuse to the P-type and recombine with holes. Similarly, holes in the P-type semiconductor diffuse to the N-type side, where they recombine with electrons. This diffusion creates a region of space charge, where the free charge carriers are removed. This space charge region is called the depletion region and has a built-in voltage potential due to the fixed ions in it.

If the voltage potential at the cathode of a silicon diode is higher than the voltage in the anode, the diode is then in reverse bias. Increasing the applied reverse bias voltage results in expanding the depletion region even further. By expanding the depletion region, the junction capacitance is decreased.

3.1.3 The sensor

The sensor is the component of the detector system where the electrical signal is generated by a particle that interacts with the detector's volume. A particle depositing energy in the semiconductor sensor material will generate electron-hole pairs which are detected as electrical signals. The generated signal is then transferred to the readout chip for further processing.

Although silicon is the most commonly used material in semiconductor detectors, other materials can also be connected to external readout chips. Materials that are suitable for detectors include Germanium (Ge), Gallium Arsenide (GaAs), Cadmium Telluride (CdTe), Cadmium Zinc Telluride (CdZnTe) and Diamond [19]. Choosing the detector material depends on parameters such as the energy of the detected particle. While silicon is capable of detecting low energy photons (up to ~ 20 keV), other materials can be more suitable for detecting high energy photons. However, silicon is a mainstream material for charged particle detector applications due to the fact that its properties have been intensively studied. Since silicon is widely used in developing industrial electronics, it is available in large quantities at low cost, and its processing is well advanced meaning that the doping profiles and the growth of silicon crystals are nowadays well-controlled.

In a silicon detector, the detecting element is a reverse biased p-n junction. As introduced in Section 3.1.2, the p-n junction is created by bringing a P-type and an N-type semiconductor to contact. In a pixelated sensor, this is done by adding N-type implants on a P-type substrate (or the opposite: P-type implants on an N-type substrate), following the geometrical segmentation required for the detector. The applied reverse voltage bias in a semiconductor sensor is usually high enough to fully deplete the sensor volume.

Collection mechanisms

The two mechanisms for charge carrier transport in a semiconductor material are drift and diffusion.

In the presence of an electric field, like in the case of the depletion region, the electrons and holes move parallel to the electric field with a drift velocity given by Equations 3.4 (for electrons) and 3.5 (for holes), where v_n is the average drift velocity for electrons, v_p for holes, E the electric field and μ_n and μ_p the mobilities for electrons and holes respectively.

$$v_n = -\mu_n \cdot E \tag{3.4}$$

$$v_p = \mu_p \cdot E \tag{3.5}$$

The above equations apply for low values of the electric field, where the mobility in silicon is constant (1350 cm^2/Vs for electrons and 480 cm^2/Vs for holes). For higher values of the electric field ($E > 10^5$ V/cm), the drift velocity increases more slowly up to approximately 10^7 cm/s (velocity saturation effect) [19].

In regions where there is a gradient in the carrier concentration, the carriers are more probable to move towards a lower carrier concentration region. This effect is called diffusion and is described by Equations 3.6 and 3.7 for electrons and holes respectively, where $J_{n,diff}$ and $J_{p,diff}$ are the diffusion currents per unit area for electrons and holes, ∇n and ∇p the concentration gradients and D_n and D_p the diffusion constants [20].

$$J_{n,diff} = -D_n \cdot \nabla n \tag{3.6}$$

$$J_{p,diff} = D_p \cdot \nabla p \tag{3.7}$$

Due to this effect, charge generated in the sensor volume can diffuse to two (or more) neighbouring pixels (charge sharing). Despite the fact that charge sharing results in a reduced signal read out by each pixel, it can be conducive to improving the spatial resolution in the detector by applying a position correction based on the portion of the charge deposited in each pixel.

Signal formation

The presence of electric field forces the generated electrons and holes to move in the detector volume. This movement of charge carriers induces a current pulse on the detector electrodes. As described by the Ramo theorem [21], the instantaneous current induced on a detector

electrode by the movement of a charge q with a drift velocity $\vec{v}$ and a weighting field $\vec{E_w}$ is given by Equation 3.8:

$$i(t) = q\vec{v} \cdot \vec{E_w}, \tag{3.8}$$

In order to calculate the weighting field $\vec{E_w}$, the electrode of interest should be raised to unit potential, while all other electrodes are set to zero potential (grounded).

The shape of the current pulse depends on various factors such as the initial distribution of electrons and holes in the detecting medium, the geometry and the electric field distribution in the detector [19].

3.1.4 The processing chain

Since pixel detectors started being studied for use in HEP experiments, front-end electronics started being designed specifically for particle detector applications [22, 23]. Special requirements and complications are often posed in such designs, such as fast signal collection and radiation tolerance. Requirements which imply the need of an on-pixel signal processing chain.

As illustrated in Figure 3.2, the typical processing chain in a particle detector usually consists of a charge sensitive amplifier (CSA), a shaper, a discriminator and local storage of the signal information that has been detected.

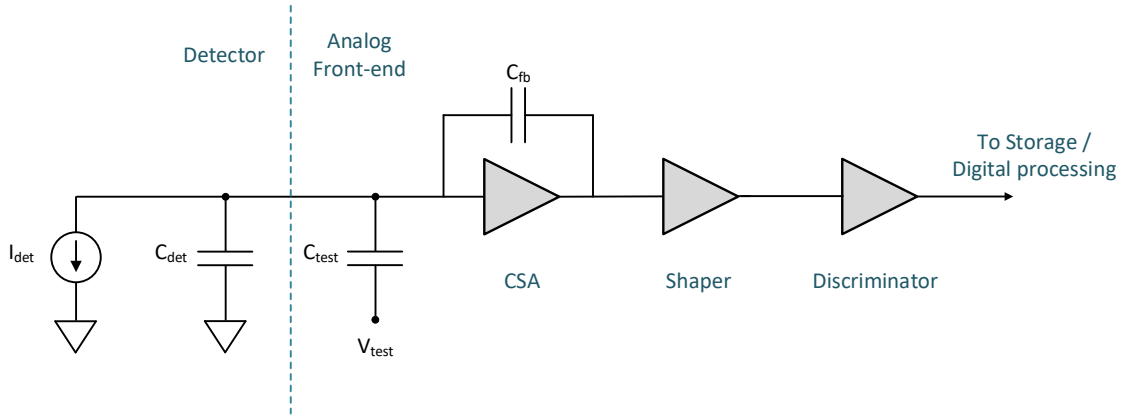


Figure 3.2 Block diagram of a typical processing chain in a particle detector.

First, the sensor provides a current pulse that is injected to the input of the CSA. The current signal is then integrated in the CSA, which will generate at its output a voltage step pulse with amplitude proportional to the amount of the charge collected in the sensor.

In addition, the gain of the CSA (and therefore the amplitude at the output) is inversely proportional to the feedback capacitance, as described in Equation 3.9.

$$\Delta V = \frac{Q_{in}}{C_f} \tag{3.9}$$

The feedback capacitor should be discharged by a continuous reset. Compensation for the sensor's leakage current is also needed in such architectures. Depending on the application and the sensor type, the CSA may need to be able to handle both positive and negative input charges such that the readout chip can be used with different types of sensors (electron or hole collection). To electrically test the front-end, a common solution is to add a test pulse injection circuit at the input of the CSA. This way, a voltage pulse can be injected to a test capacitance (C_{test} in Figure 3.2) and generate a charge at the amplifier's input.

As a next stage of the processing chain, many front-ends feature a shaper, responsible for shaping the step voltage generated in the CSA according to the timing requirements of the application. The pulse duration is usually shortened in order to reduce pile-up of subsequent events. In addition, the shaper might include additional gain stages and filters at an effort to maximise the Signal-to-Noise ratio of the signal.

To digitize the signal, a discriminator is added between the amplification stages and the readout logic. Here, the signal is compared to an applied threshold that can be set either from the periphery of the chip, or using an external reference. Signals below the minimum energy defined by the threshold will be excluded from further processing, while signals above the threshold will be handled by the logic. By setting the threshold high enough, and provided that the CSA gain is sufficiently high, the noise hits can be eliminated resulting in a noise hit free data acquisition. A local threshold trimming can be applied to the discriminator by an on-pixel DAC (usually with only a few bits resolution) in order to compensate for pixel-to-pixel threshold mismatch.

Different approaches can be used to read out the output of the on-pixel processing chain. It can be directly read out, or stored in a local memory for further processing.

In the case where the signal (discriminator output) is processed using digital logic implemented in the chip, the logic can be placed on-pixel or in the periphery. The information on the position of the hit is given by the address of the pixel where the charge was generated. The spatial resolution (accuracy of the hit position information) of the detector depends on the pixel pitch and factors such as the charge sharing between neighbouring pixels and the selected readout architecture [20]. The simplest case would be to assume a binary readout, where the only information stored in the pixel is whether a hit was detected or not, and no charge sharing between pixels (each hit is detected by only a single pixel). The spatial resolution of the detector is then given by Equation 3.10, where p is the pixel pitch:

$$\sigma_{position} = \frac{p}{\sqrt{12}} \tag{3.10}$$

Equation 3.10 gives an upper limit for the spatial resolution of a detector with a given pixel pitch. To improve the spatial resolution and to obtain more information about the timing and energy of the detected charged particle, further processing can take place. Information on the time when the hit occurred can be stored either by using a global time-stamp provided to the chip, or by employing a shutter signal as a time reference (Time of Arrival - ToA measurement). A timing diagram of a ToA measurement, where the time-stamp is given by counting the number of clock pulses from the time the signal was detected to the falling edge of the shutter, is illustrated in Figure 3.3.

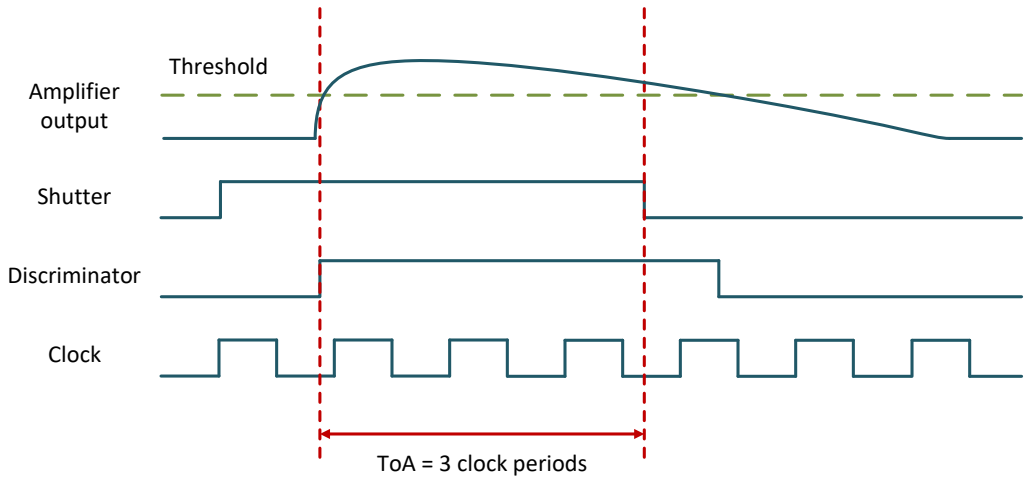


Figure 3.3 Timing diagram of a ToA measurement.

The energy of the signal can be extracted by measuring the time while the output of the amplification stage stays above the applied threshold, and therefore the output of the discriminator remains high (Time over Threshold - ToT measurement), as shown in Figure 3.4. This amount of time is proportional to the amount of charge generated in the sensor. By having information on the energy of the signal, the charge sharing can be studied. Analysing the amount of charge detected by each pixel at an event where the signal is induced to two (or more) neighbouring pixels, can provide more information on the position of the hit, thus achieving sub-pixel spatial resolution.

Another benefit from storing the energy information of the signal, is that the "time walk" can be corrected using the ToT measurement. Time walk is the effect where different ToA is recorded depending on the amount of the input charge. The time walk results from the fact that pulses at the output of the amplification stage with different amplitudes will cross the

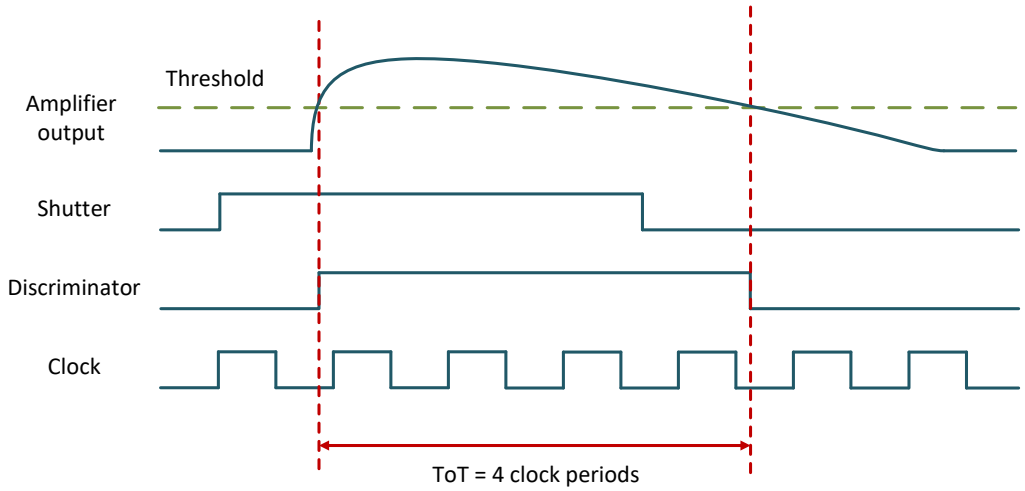


Figure 3.4 Timing diagram of a ToT measurement.

threshold at different times [24]. Consequently, for two hits occurring at the same time, the one with lower energy will appear to arrive later in the time measurement, as presented in Figure 3.5. The delay for the signal to cross the threshold, which is inversely proportional to the energy, can be extracted by the ToT information. Thus, time walk correction can be performed, improving the accuracy of the timing measurement in the detector.

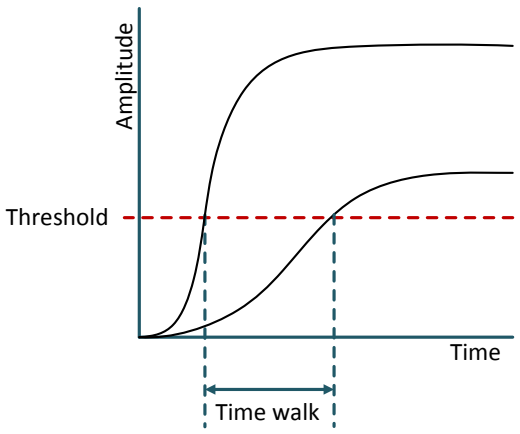


Figure 3.5 Time walk in a detector.

Alternatively, the energy of the signal could be measured with an ADC placed in the pixel. For applications that do not require information on the time and energy of the signal, but the number of detected particles is important, the photon counting measurement would be suitable. In photon counting, the number of hits above the applied threshold is counted.

Once the data are acquired, they can be shifted out of the chip to be further analysed. Three readout architectures are widely used in particle detector chips: the frame-based, the

data-driven and the trigger-based readout. In a frame-based readout, such as in the case of the Medipix3 chip [25], a shutter signal controls when the signal is acquired and when the data can be read out. While the shutter signal is high, the chip is ready to acquire data. Once the shutter is closed, a readout command can be sent to the chip in order to shift the acquired data out of the pixel matrix. Another approach for shifting the data out of a detector chip is the data-driven readout. This approach has been implemented in the Timepix3 chip [26], where the chip sends data outside as fast as possible, without the need for an external command. An architecture that has been employed in several detector chips developed in the framework of HEP experiments, such as the FE-I4 readout chip which was designed for the ATLAS experiment at the CERN LHC [27], is the trigger-based readout. In this approach, the acquired data stored in the chip are kept for a given latency interval. If a trigger signal is sent to the chip within this latency interval, the data will be shifted out of the chip, otherwise they will be erased.

Several complications arise during the design of the above-mentioned blocks. The designed circuitry shall fit in a relatively small area as the pixels used in particle detection applications usually measure a few tens of μm per side. Mismatch parameters also need to be taken into consideration in order to achieve a uniform pixel response over the matrix.

3.2 Hybrid pixel detectors

The requirements for HEP experiments for particle detection motivated the development of dedicated readout electronics for semiconductor sensors segmented in numerous small channels in both dimensions. The benefits of segmentation include lower electronics noise (due to the lower input capacitance) and higher spatial resolution. Each of the channels is referred to as "pixel" (from "picture element", following the terminology in digital imaging), and the detectors are called hybrid pixel detectors, due to the fact that they consist of a combination of two components (semiconductor sensor and readout electronics) electrically connected together. One of the advantages of this approach is that detectors with high timing performance can be built thanks to the fast charge collection by drift. Modern hybrid pixel detectors are capable of performing timing measurements with ns precision, while the latest developments aim for sub-ns time resolution [28]. In addition, hybrid pixel detectors offer the possibility to use different sensor materials. Segmenting the detector can result in a spatial resolution of a few μm, and thanks to the use of modern CMOS processes, the particle flux which can be handled by the detector is increasing. A cross-section of a pixel in a hybrid pixel detector assembly is presented in Figure 3.6.

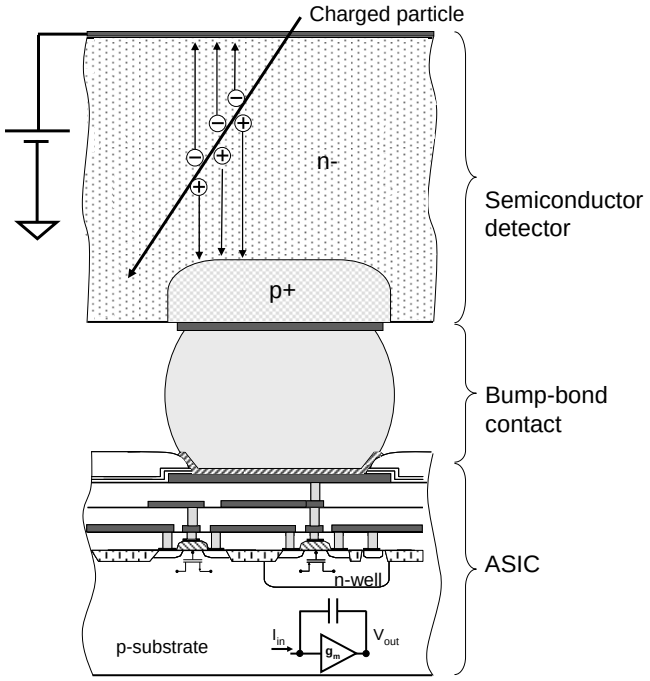


Figure 3.6 Schematic cross-section of a hybrid pixel detector (not to scale). From [29].

Figure 3.7 presents the photo of a hybrid pixel detector mounted on a PCB. A silicon sensor is bump-bonded on top of the readout chip.

In the following sections, the different developments that took place in the past decades, as well as the main aspects of the design and assembly of a complete hybrid pixel detector, are discussed.

3.2.1 Developments in hybrid pixel detectors

Early developments

Pixel detectors were evolved from the strip detectors that were used in the past decades. In a strip detector, the position resolution is given by building strip-shaped reverse biased diodes on top of the silicon. By processing both sides of the material, the position information can be extended to two dimensions. The first silicon detector, with a double-sided strip pattern, was developed in the late sixties by Philips [30]. The strips of the two sides of this detector were forming squares with 1.37 mm pitch. In the years to follow to the present day, the innovation in designing silicon detectors advanced in many different aspects of the design. Not only the sensor technology progressed in how the material is processed, but the readout technologies grew remarkably following the novelties and downscaling in CMOS processes.

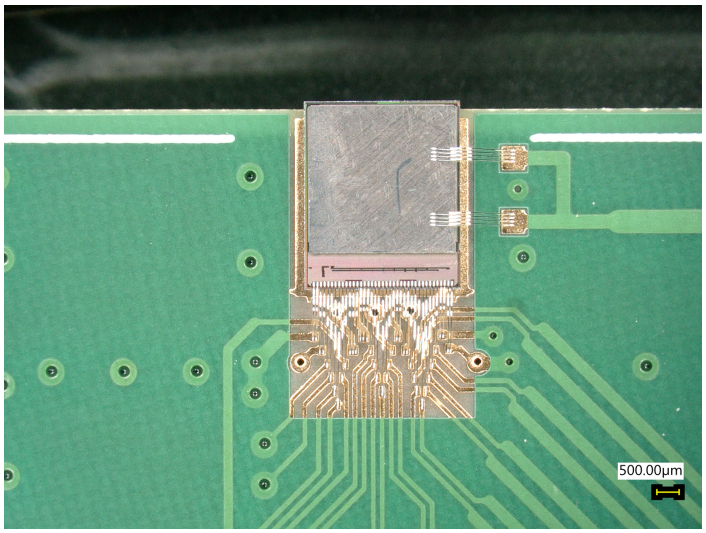


Figure 3.7 Photo of a hybrid pixel detector mounted on a PCB, with a silicon sensor bump-bonded on the CLICpix2 readout chip.

In addition, as the applications became more and more demanding, larger detector systems with need for complex data processing and analysis are being built.

The breakthrough in the field of silicon detectors happened in the early eighties, when small area electronic circuits were used to build highly segmented detectors. Silicon microstrip detectors started being developed in the context of particle physics applications [31, 32]. As the developments in silicon detectors were progressing, the segmentation was becoming finer in order to achieve better position resolution in two dimensions. Given the increasing number of channels, the use CMOS integrated circuits for reading out the data from the detector was required and gradually chip design took an important part in HEP experiments. Before the development of complete hybrid pixel detectors, the microstrip detectors were read out by having their outputs connected to the front-end electronics using standard wire-bonding techniques. The same applies for the first generations of detectors segmented in two dimensions. In the first chips, where the number of channels in the detector was limited, the outputs were wire-bonded to the readout. The latter generation of detectors is often referred to as "pad detectors" to differentiate them from the complete hybrid pixel detectors. In a hybrid pixel detector, the large number of channels (tens of thousands in modern applications) implies the need for more elaborate interconnect techniques, as will be described later.

In the late eighties, silicon microstrip detectors were installed in several HEP experiments, including large area detectors in the CERN Large Electron-Positron (LEP) collider. As the area available for the electronics was decreasing and the number of channels was increasing, it was clear from early developments that the capability to multiplex different signals had

to be included in the readout electronics as the area would not allow routing all signals individually [33]. The first chip for readout of silicon strip detectors used in a collider experiment was the AMPLEX chip, installed in the detector of the UA2 experiment at the CERN Super Proton Synchrotron (SPS) collider [34]. This novel chip, designed in a commercial 3 µm CMOS process, included 16 channels, each comprising a CSA, a shaper and a track-and-hold circuit that would store the pulse height at the output of the amplification stages.

Later, in the CERN LEP era, different chips have been fabricated to read out silicon strip detectors. The increasing demands of the detectors for reading out multiple channels with low noise and low power electronics, along with the restrictions on material budget, motivated the design of readout chips capable of reading out high density detector systems. In order to keep the power consumption as low as possible (and thus dissipate minimal heat and avoid high volume cooling systems), the concept of powering down the front-end electronics between the detector cycles was studied since the development of the first readout chips [35]. Several experiments in the CERN LEP collider, such as the DELPHI [36] and ALEPH [37] detectors, employed silicon microstrip detectors for their inner layers. An example of a readout chip for double sided silicon strip detectors is the CAMEX64 chip [37], designed in the context of the ALEPH Minivertex detector at LEP [38]. The chip consists of 64 channels with 100 µm pitch. Each of the channels includes an amplifier, noise filtering, storage and readout of the analog signals, which would then be digitised outside the ASIC.

Complete hybrid pixel detectors

Following the successful integration of silicon strip detectors with VLSI readout circuits in HEP experiments, innovation proceeded towards the design of complete hybrid pixel detectors. In contrast to previous generations, the pixel detector is no more limited by the number of detecting channels that can be wire-bonded to its inputs. Instead, the sensor and the readout ASIC are stacked on top of each other and each sensor pixel is connected to one pixel in the readout chip. The pixels in the sensor and the readout chip need therefore to have the same segmentation geometry. The electrical connection between the two pixels is normally done with a bump-bonding process [20], which will be further explained in Section 3.2.2.

Downscaling of CMOS processes lead to pixel detectors capable of fitting the signal processing electronics in a small (square or rectangular) pixel area. High granularity and precise position measurement could now be achieved in both dimensions. Depending on the application, a pixel detector might have pixels measuring from tens to a few hundreds of µm per side.

The first hybrid pixel detectors, developed in the early nineties, were designed in view of particle physics experiments with detectors covering areas of several m^2, where the use of low power, high density electronics is required to tackle the constantly increasing luminosity of such experiments. The first generation of pixel detectors developed at CERN in a 3 µm CMOS process, comprised small matrices of square pixels with 200 µm pitch [39], [40]. In each pixel, the charge delivered from the detector is amplified and then compared to an applied threshold. A local memory cell stores one bit of information in the pixel (indicating whether the pixel detected a hit or not).

In view of the detectors at the CERN LHC, more complex ASICs were being designed in order to demonstrate the suitability of the hybrid detector architecture for the experiments. One example is the LHC1 ASIC which featured a matrix of 128×16 rectangular pixels, each measuring 50×500 µm^2 [41]. The chip was designed in a 1 µm CMOS process and can be operated in different modes. Electrical test of individual pixels, as well as the option to mask any faulty pixels, was included in the chip. A 300 µm thick silicon sensor was bump-bonded on the chip in order to carry out tests with particles.

Currently, pixel detectors are installed in large area detectors at the LHC and are also considered for future upgrades. These experiments include the CMS (Compact Muon Solenoid) [42, 43], ATLAS (A Toroidal LHC ApparatuS) [44] and ALICE (A Large Ion Collider Experiment) [45]. The VeloPix chip has been developed at CERN in view of the upgrade of the vertex detector at the LHCb (Large Hadron Collider beauty) experiment [46].

Apart from HEP experiments, silicon pixel detectors have found application in different fields, among which space experiments. The Alpha Magnetic Spectrometer (AMS-02) on the International Space Station (ISS) [47], used for detecting high energy particles in space, employs a silicon tracking detector. Hybrid pixel detectors are used for radiation measurements performed in satellites, like ESA's Proba-V satellite [48], as well as to monitor the radiation field in the ISS, providing valuable input about the possible risks for humans and electronics on the station [49]. The Timepix2 ASIC, developed at CERN, is a highly programmable pixel detector readout chip intended for particle physics applications, including characterisation of radiation in space [50]. Other applications of hybrid pixel detectors include spectroscopic imaging, where typically sensor materials with high atomic number (Z) (such as GaAs, CdTe, CdZnTe) are used, and dosimetry [51, 52].

Design considerations

Modern hybrid pixel detector readout chips include a large number of small area pixels, with complex on-pixel electronics. The chips are designed in sub-micron process nodes, with 130 and 65 nm being the mainstream nodes for current ASIC developments in particle detection

applications. Highly configurable, versatile chips with multiple functions and precise timing and energy measurements have been successfully designed. As an example, the Timepix3 chip, a versatile chip for particle detection applications, can record a time-stamp measurement with a resolution of 1.5625 ns [26]. Digital design is advancing in industrial applications, and readout chips for particle detectors follow the trend by integrating faster and more complex readout architectures in order to make the readout more robust and efficient. Communication standards with data encoding, compression algorithms and data rates of the order of Gbits are currently used in state-of-the-art readout chips.

As the density of transistors in the design becomes higher and higher, special attention should be taken concerning the power consumption of the different circuits, and the way the power is distributed in the chip. High-performance chips may include more than 100 million transistors in an area of only a few cm^2, while using fast clocks running in the digital logic. Lower power consumption per unit area is always preferable in particle detector applications, as it can simplify the full detector system. Low power electronics could be operated with less complex power distribution schemes in the detector modules and with simpler cooling structures compared to what would be required for higher power electronics. The power consumption of the chip is directly proportional to the capabilities of the electronics in terms of count rate and timing resolution. Alternative ways of achieving sharp time-stamp resolution while keeping the power consumption low have been studied, focused on performing the measurement without having to distribute a very fast clock signal to all pixels [53].

Future perspectives

Regarding the future trends in the field of hybrid pixel detectors, the design of more complex integrated circuits is needed for tackling the challenges in modern HEP experiments. The expected data rates in the experiments keep increasing, and a faster timing and finer position resolution is often required along with more complex signal processing in the pixel. This indicates that, following "Moore's Law" [54, 55], CMOS readout circuits in particle detectors will eventually move to lower process nodes, such as 28 or 14 nm. The advantages from using a more downscaled CMOS process are numerous, starting from the smaller pitch that can be achieved. By decreasing the pixel area, not only the position resolution is improved, but also the detector capacitance is reduced. The front-end design can benefit from the lower input capacitance, resulting to lower noise and lower power front-end electronics. In addition, modern CMOS processes open the possibilities for processing faster signals in the chip, and consequently better time-stamp resolution. Already, the trend in modern detectors is to move to a time resolution of the order of tens of ps [28].

A typical (hybrid or monolithic) pixel detector chip consists of the pixel matrix and the periphery electronics. The periphery may include different blocks, such as biasing circuits, control and readout logic, as well as the I/O pads. The pixel matrix is usually placed on top of the periphery, and the periphery electronics and wire-bond pads are located on the one side (bottom) of the chip, at an effort to minimise the inactive area around the matrix [56]. As the periphery area is inactive (unresponsive to particles), it is desirable to minimise it in order to increase the ratio of active to inactive area in the detector. By eliminating the inactive periphery area, the full chip area will be sensitive to particles, and the chips can be tiled on four sides to create large area detectors without insensitive regions, such as the Medipix4 and Timepix4 chips that are currently in the design phase [28]. To realise such a chip, the periphery blocks would have to be laid out among the pixel circuitry. Connections with the readout system can be done using Through Silicon Vias (TSVs), in order to eliminate the area used by the wire-bond pads [57].

Taking advantage of the TSV processing, multiple chips can be stacked to create a "pillar" matrix [58]. In such a scheme, the analog and digital circuitry are realised in separate silicon wafers in order to be further isolated. The sensor, analog and digital chips are then stacked together. The interconnection between the different chips, as well as between the readout chip and the PCB, is implemented using either a bump-bonding process or TSVs. Several benefits can result from such an assembly, as the analog front-end and digital logic can be implemented in different processes and thus be further optimised. However, the complexity and cost of designing and manufacturing the detector increase significantly. Using different complex processes for designing the chips and realising the interconnects, can impact the design effort and yield of such detectors. Another example, this time with all electronics implemented on the same substrate, is the TSV processing of the Medipix3 chip [28]. As shown in Figure 3.8, the chip can be connected to the data acquisition system using wire-bonds. After the TSV processing, the region in the periphery of the chip occupied by the wire-bond pads can be diced off, in order to suppress the inactive area.

3.2.2 Bump-bonding

The need for numerous and dense electrical connections between the pixelated sensor and the readout chip motivated the study of different interconnection techniques in hybrid pixel detectors, in order to overcome the limitations resulting from the wire-bonding technique. Bump-bonding is the process where the outputs of the sensor pixels are electrically connected to the inputs of the pixels in the readout chip using spherical solder bumps [20]. During this flip-chip interconnection, the sensor and readout chip are connected with bumps deposited between the pads of the two detector components.

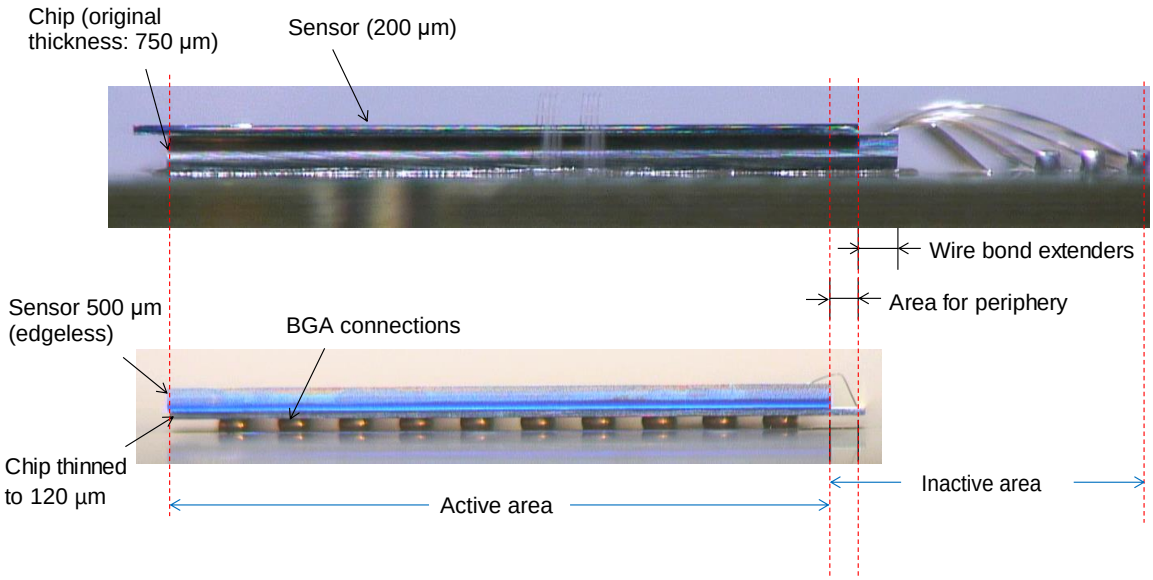


Figure 3.8 The Medipix3 chip, connected to the data acquisition system using wire-bonds (top) and TSVs (bottom).

This process has been originally developed for flip-chip interconnection in industrial electronics and was later proven suitable for particle detector applications. The bump deposition is usually performed at wafer level (depositing bumps at once on all dies), although bump-bonding single dies is also possible. High density bump-bonding is feasible, and hybrid pixel detectors with pixel pitch as short as 25 µm have been assembled and successfully tested [59].

It is clear that the bump-bonding process has been highly conducive in assembling state-of-the art pixel detectors, as it opens the possibility to realise a theoretically unlimited number of interconnects between the sensor and readout chip. On the other hand, the flip-chip process can complicate the detector assembly as it requires further process steps and can significantly increase the cost of the module, especially in low production volumes.

3.3 Monolithic pixel sensors

In a monolithic pixel sensor, both the sensor and the readout electronics are build on the same substrate. This way of designing was motivated from the fact that in different applications the sensor and readout chip were both produced on silicon wafers. Therefore, the idea of using a single, commercial VLSI process was appealing for applications in particle detection. By using a single wafer for sensor and readout, the complications and cost from the high-density

bump-bonding process are overcome. As will be described in the coming sections, in certain monolithic processes the pixel capacitance can be reduced, leading to a low noise and low power detector.

In visible light detection applications, such as digital cameras, the first developments were based on the Charge Coupled Devices (CCDs). Such an example is the first digital camera, designed by Kodak in 1975, which was based on a CCD sensor with 100×100 pixels. CCDs were, however, gradually replaced by CMOS image sensors, as the latter would be conducive for building lower power and lower cost systems with VLSI processing electronics on the same chip as the sensor [60]. The same trend was followed a few years later in monolithic particle detector applications, where the CCDs started being replaced by CMOS-based systems which offer the possibility for including complex processing circuit on the chip [61].

As will be described in the following sections, different challenges arise when designing a monolithic pixel sensor. Challenges that result from the effort to design a fully efficient sensor with small pixel area and prompt charge collection in order to meet the requirements in modern particle detection applications. Meanwhile, the need for electronics on top of the sensor adds complexity to the design. Another challenge is that since commercial processes are often not optimised for particle detection and target to different applications, the different features of the technology have to be exploited in special, non standard, ways for detector applications.

3.3.1 Developments in monolithic pixel sensors

The first generations of monolithic pixel detectors proved that the collecting volume and the readout circuit can be integrated in the same piece of silicon. Early developments featured a P-type substrate which was depleted by adding an N-type diffusion at the back side of the wafer. Prototypes demonstrated the feasibility of designing monolithic detectors, while revealing some of the drawbacks of this technology (mainly due to the fact that double-sided processing of the wafer was required). In one of the first prototypes [62], a small P-type collection electrode was used, with the electronics placed in an N-well on top of the P-type substrate. This chip featured a matrix of 30 rows and 10 columns, with pixels measuring 125×34 μm^2, and a Signal-to-Noise ratio of 150 was achieved.

As high-resistivity silicon (> 100 Ωcm) is more expensive, commercial CMOS processes use standard, low-resistivity silicon ($10 \sim 20$ Ωcm) as their substrate. Charge collection on low-resistivity silicon is not optimal, which lead to the use of an epitaxial high-resistivity silicon layer, available in some processes (with thickness of the order of ~ 10 μm), between the substrate and the electronics [61]. This epitaxial layer consists of higher purity silicon than the silicon in the substrate. The sensitive detector volume in this case is the partially depleted

epitaxial silicon layer. The charge generated in the (P-type) epitaxial layer is collected at the N-well collection diode, as presented in Figure 3.9. However, the charge is collected by both the drift and diffusion mechanisms, making the collection time slow compared to fully depleted sensors. This collected charge is relatively small (usually ~ 1 ke$^-$) and the slow collection time can be limiting to many detector applications. In addition, a slower charge collection means that the detector is more vulnerable to radiation effects, which further slow down the charge collection. The small signal implies the need for a low noise circuit in order to keep the Signal-to-Noise ratio as high as possible. Further, as the signal was collected on an N-well, for processes where deep wells were not available, every other N-well containing electronics would compete with the collecting electrode. As this would reduce even further the detected charge and compromise the detector's efficiency, all circuitry was designed using only NMOS devices placed in the P-well, without any N-wells other than the collection electrode. This motivated the design of monolithic sensors in processes with buried wells, as will be described in the coming sections. Additional challenges are implied for the design in such processes due to the fact that process details like the implant geometry and doping profiles are often not accessible by the designer. Consequently, it is hard to accurately predict the signal generation in the sensor as some parameters can only be approximated during the design phases.

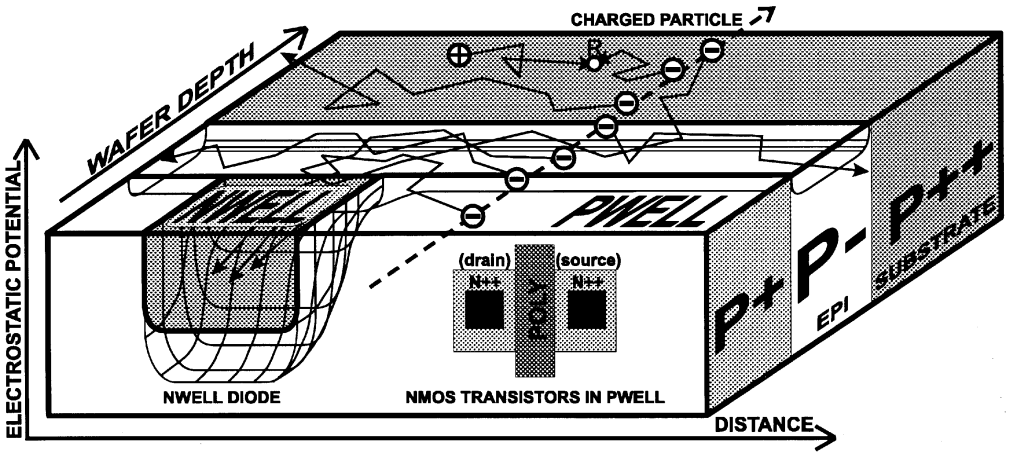


Figure 3.9 Schematic cross-section of a monolithic sensor pixel with charge collection on epitaxial layer. From [61].

Due to the limitations of the process and the need to use only NMOS devices, the circuitry in such monolithic detectors was kept as simple as possible. A common scheme used for the front-end in the pixel of such detectors was the one implemented in the MIMOSA chip [61].

In this chip, each pixel includes a three-transistor circuit including a reset transistor, a transistor which is the input of a source follower, and a switch for row selection. Four matrices of 64×64 square pixels with 20 µm pitch where included, each with a different number of collection diodes (1 or 4) or with modified layout. All pixels in each of the matrices where multiplexed to a single source follower in order to be read out. Other, more complex, functionality (e.g. amplification, signal processing on-pixel) was later added, following the downscaling of the monolithic processes and the use of buried wells. The MIMOSA chip was the predecessor of the ULTIMATE chip, a monolithic pixel detector ASIC which is currently installed in the pixel detector in the STAR experiment [63].

The simple readout schemes and the slow collection time would not allow the efficient use of monolithic pixel sensors in applications with high expected data rates, inspired the study and development of monolithic processes that can overcome these limitations.

Several CMOS processes offer a triple-well structure by means of using a deep N-well. The P-well where the NMOS transistors are placed, can be placed on top of the deep N-well, while an additional N-well containing PMOS transistors can be placed outside the deep N-well, as illustrated in Figure 3.10. In this case, the signal is collected in the large deep N-well. The area of the N-well containing the PMOS devices should be kept minimum as it competes with the collecting electrode and can reduce the detector's efficiency. Such a solution allows a more complex on-pixel circuitry and a typical processing chain can be implemented in the pixel. This approach has been used in the Apsel0 and Apsel1 chips [64]. The Apsel1 chip features a small matrix of 8×8 square pixels with 50 µm, where a preamplifier, a shaper, a discriminator and a latch for storing the hit information are included in each pixel. The Apsel1 chip achieves a gain of ~ 70 mV/ke$^-$, however, a relatively high power consumption (60 µW per pixel) is needed due to the large sensor capacitance of 460 fF.

Although this approach allows the use of both NMOS and PMOS devices in the pixel, it is still not optimal as the number of PMOS devices used in the circuit should be minimised and cover the smallest area possible. The limitations in terms of collected charge and collection time described above are not overcome by simply adding the triple-well structure.

The above developments indicated that the effort for designing high-performance monolithic pixel sensors should focus on two different paths. First, to increase the collected charge and reduce the collection time. Second, to isolate the collection electrode from the circuitry and enable the use of complex, complementary, on-pixel circuitry able to meet the demanding requirements of modern large scale detectors.

To allow the use of PMOS devices in the monolithic pixel, processes with epitaxial layer and an additional deep P-well have been studied. Such an example is the TPAC1.0 chip presented in [65]. The deep P-well is now enclosing the N-well where the PMOS transistors

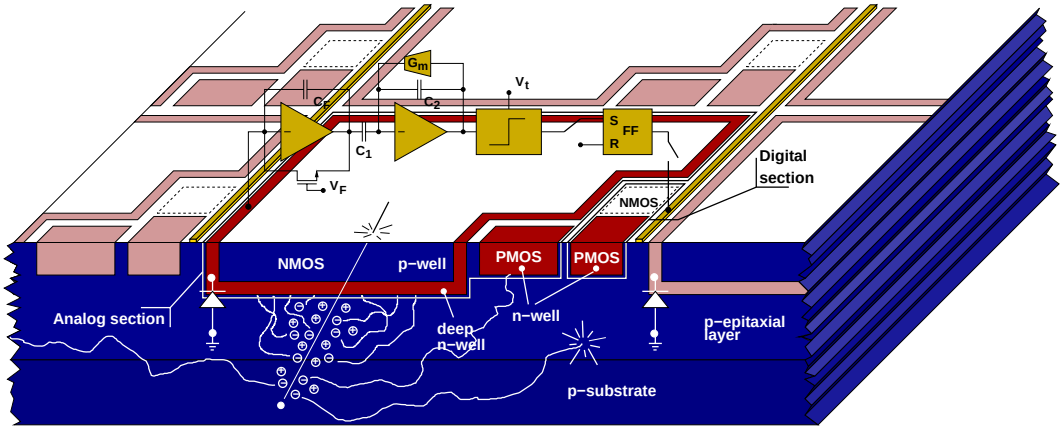


Figure 3.10 Schematic cross-section of a triple-well monolithic pixel. From [64].

are placed, such that no other wells compete with the collecting N-well, which is now isolated, as shown in Figure 3.11. The 50 µm pixel in this chip has more than 150 NMOS and PMOS transistors and features an on-pixel pixel processing chain including a preamplifier, shaper and comparator. A efficiency close to 100% was maintained in the TPAC1.0 chip while implementing a complex on-pixel circuit. So far, the use of complementary circuitry in a monolithic sensor pixel would either result to a compromised charge collection (and thus reduced efficiency) or to unwanted signal coupling to the sensor. By adding the deep P-well, the use of PMOS devices is now possible without implications for the sensor.

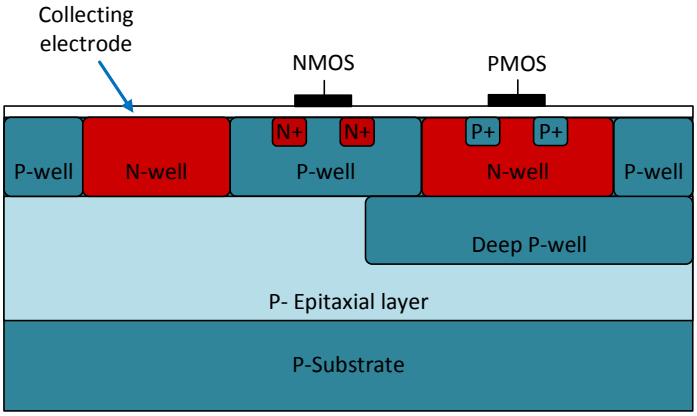


Figure 3.11 Schematic cross-section of a monolithic pixel in a process with an additional deep P-well.

Although this approach does still have some drawbacks when it comes to charge collection time and area available for placing the electronics, it offers several interesting advantages and some modifications of it will be further investigated in the coming sections.

3.3.2 High-Voltage monolithic pixel sensors

High-Voltage (HV) CMOS technologies have been introduced as a way to improve the performance and charge collection of monolithic pixel detectors [66]. Similarly to the triple-well detector described in Section 3.3.1, all electronics in the pixel are placed inside a deep N-well. The deep N-well simultaneously acts as the sensor cathode and the substrate for the PMOS transistors. A cross-section of the HV-CMOS process is presented in Figure 3.12.

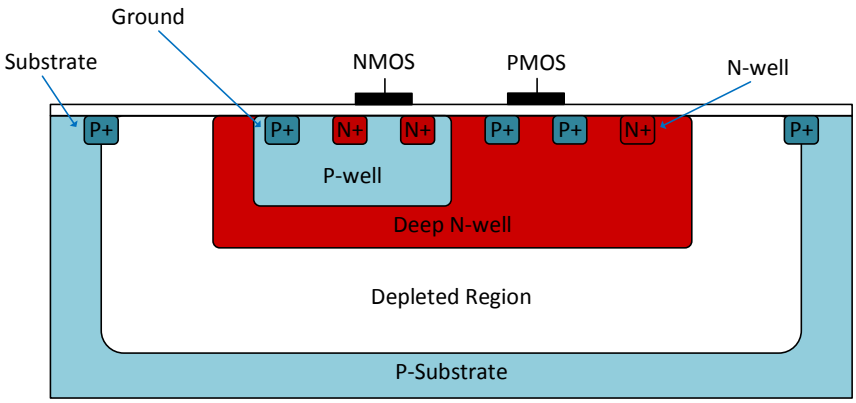


Figure 3.12 Schematic cross-section of a HV-CMOS process.

In CMOS processes, the term high voltage refers to voltages higher by an order of magnitude than the ones used in standard CMOS circuits (i.e. several tens of Volts). Triple-well technologies allow the use of standard CMOS devices, all implemented within the deep N-well, while the P-type substrate is biased to a reverse high voltage.

Due to the applied high voltage, the p-n junction between the substrate and the deep N-well is strongly reverse biased. This leads to the creation of a depleted volume, between the substrate and deep N-well, much larger compared to the one in monolithic sensors implemented in standard, low voltage, CMOS processes. Unlike the planar sensors described in Section 3.1.3, the sensor volume in a HV-CMOS sensor may not be fully depleted. The thickness of the depleted region depends on the resistivity of the substrate and the applied voltage, as described by Equation 3.11, and is typically at the tens of μm [67]. A Minimum Ionising Particle (MIP) passing through the sensor material deposits $\sim$ 80 electron-hole pairs per μm of material. As introduced in Section 3.1.1, this number depends on the thickness of the detecting layer and can be significantly smaller for thin ($\sim$ 10 μm) layers. The portion of the charge which is generated in the depletion region will be collected by drift, making the detector potentially suitable for applications where a fast timing is required. This indicates that the use of higher resistivity substrate can be beneficial for designing HV-CMOS sensors.

Depleting the sensor volume not only results in fast charge collection, but also leads to a reduced detector capacitance [68].

$$d = 0.3 \cdot \sqrt{U_{bias} \cdot \rho_{sub}} \tag{3.11}$$

In contrast to the triple-well monolithic sensor discussed in Section 3.3.1, in a HV-CMOS detector all electronics are placed in the collecting deep N-well, in order to not have other N-wells competing in the signal collection. This indicates that proper attention needs to be taken during the design, as every P+ diffusion is now capacitively coupled to the deep N-well. As the collecting deep N-well is also the input of the preamplifier in the pixel, every P+ diffusion can be a source of unwanted cross-talk, as can be seen in Figure 3.12. The use of PMOS devices, although allowed by the process, should still be kept as minimum as possible in order to minimise the cross-talk. When PMOS transistors are used, the designer should make sure that no noise is injected to the collection electrode (for example, in the case of fast switching transistors). An additional reason that the use of PMOS transistors should be limited is that they contribute to the capacitive feedback, which implies a reduced gain in the amplification stage.

In a monolithic HV-CMOS sensor, the detector capacitance is dominated by the capacitance between substrate and deep N-well and the one between deep N-well and P-well. Although the area of the P-well is normally small compared to the deep N-well, its contribution to the detector capacitance can be quite high due to the fact that the junction between the deep N-well and the P-well is reverse biased at the power supply of the circuit (typically $1.8 - 3.3$ V) and therefore the depleted region around it is relatively thin. When operating a HV-CMOS sensor, the p-n junction between the substrate and the deep N-well is biased close to its breakdown voltage, and therefore the capacitance per unit area is kept low.

Apart from the preamplifier, the different electronics (such as shaper, discriminator and possibly digital logic) can either be placed on-pixel or in the periphery. When the processing chain is placed in the pixel, such as the HV-CMOS demonstrator chip presented in [66], effort should be put during the circuit design in order to minimise the coupling to the sensor input. However, a processing chain including a CSA, a shaper, a discriminator, a 4-bit threshold tuning DAC and a digital latch can be implemented in a relatively small pixel area, such as the 50×50 µm^2 of the studied example which was designed in a 350 nm HV-CMOS process [66]. A fully efficient detector chip can be realised following this approach, with some limitations in the use of complex, fast-switching, digital circuitry in the pixel. In the case where part of the processing chain is placed in the periphery, more complex readout circuitry using complementary logic can be implemented as there is no coupling to the sensor input. One example is the MuPix7, a monolithic HV-CMOS sensor chip designed in a 180 nm

HV-CMOS process in the framework of the Mu3e experiment [69]. In the MuPix7 chip, the preamplifier is placed inside the pixel, with its output driven to the periphery. The amplified signal is fed to a second amplification stage in the periphery and then to a discriminator before being processed by the readout state machine. This approach offers the possibility to use more complex digital logic in order to process the signal from each pixel. On the other hand, other complications, such as the connections from the pixel matrix to the periphery, have to be addressed.

Despite the limitations resulting from the coupling of P+ diffusions to the sensor cathode, prototypes of monolithic pixel sensors in the triple-well HV-CMOS process have been successfully tested and are performing within the requirements of different detector applications.

To overcome the above limitations, and allow the use of complementary circuitry in the pixel, processes with quadruple wells have been studied in the context of the HV-CMOS sensors R&D [70]. Such a process offers multiple nested wells (both deep N-wells and deep P-wells), as presented in Figure 3.13. The collecting electrode is again a deep N-well on the P-type substrate. All on-pixel electronics are then placed in the deep N-well. The use of an additional deep P-well to isolate the N-well where the PMOS transistors are laid out from the collecting deep N-well, enables the placement of both NMOS and PMOS devices in the pixel, without coupling to the sensor. The N-well and P-well with the transistors, are placed on a deep P-well which is in turn surrounded by the deep N-well.

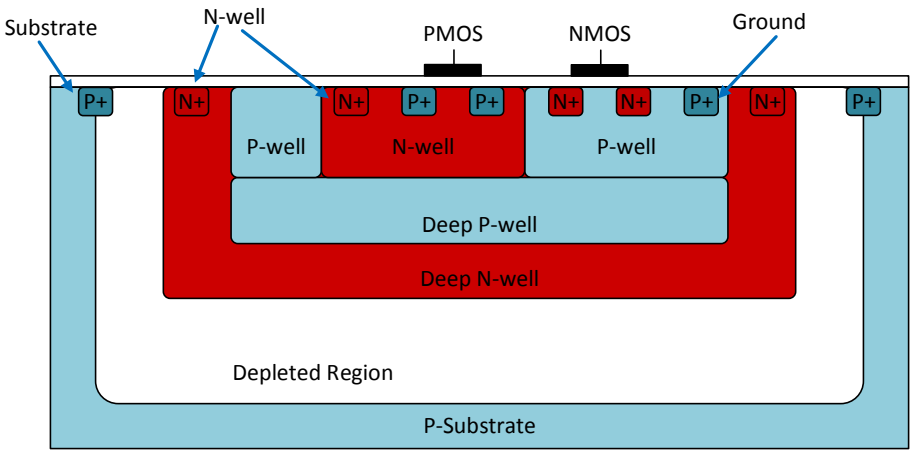


Figure 3.13 Schematic cross-section of a quadruple-well HV-CMOS process.

The advantages of using nested wells, in combination with the high voltage option and the featured high resistivity substrate (a few kΩcm), constitute a process that is quite promising for developing high performance monolithic HV-CMOS sensors. Thanks to the applied high voltage and the high resistivity of the substrate, a depleted region as thick as $\sim$ 100 µm can

be formed. The high voltage can be either a positive voltage applied to the deep N-well, or a negative voltage applied to the P-type substrate.

Among the drawbacks of such a process are the high detector capacitance (at the order of 100 fF, which implies a higher power consumption of the front-end electronics) as well as some limitations in designing circuits in a small pixel area. The well structures should respect the design rules of the process and, for small pixel pitch, a significant portion of the area is occupied by the well contacts or the well-to-well spacing. Thus, the area remaining available for placing the electronics may not be large enough to include complex systems with on-pixel digital processing of the signal.

3.3.3 Capacitively coupled HV-CMOS sensors

Taking the monolithic sensor chips designed in HV-CMOS processes as a starting point, a different approach has been tested where an active HV-CMOS sensor chip is connected to a second, readout chip. An assembly of the two chips is produced by gluing them together using a thin (a few μm) layer of epoxy glue. Instead of the electrical contact in the case of a hybrid pixel detector, in a capacitively coupled assembly the amplified charge is transferred from the sensor to the readout chip through the capacitance formed between the HV-CMOS sensor and the readout chip, as presented in Figure 3.14. Although this approach should be considered as a hybrid solution (due to the fact that the sensor and readout electronics are connected together), it is included in this section as the process used for the active sensor chip is the same as for the monolithic HV-CMOS sensors. This concept is aimed at reducing the cost of the system by means of eliminating the need for fine pitch bump-bonding, which can be costly, especially in low production volumes.

In a typical capacitively coupled assembly [71], the sensor and readout chip have the same pixel geometry. The collected diode, as described in Section 3.3.2, is included in the HV-CMOS sensor pixel. A CSA, with its input connected to the collecting deep N-well, is used to generate a voltage pulse that is injected to the coupling capacitance formed by the two metal pads and the glue between the two chips. The charge is therefore transferred to a readout chip and processed by the typical processing chain described in Section 3.1.4.

Apart from the standard one-to-one mapping of the sensor's pixels to the ones of the readout chip, assemblies with different pixel geometries in the sensor and readout chips have been studied [72]. This opens the possibility of having smaller pixels on the sensor side and larger on the readout chip. Consequently, the detector can benefit from the complex circuitry that can be placed in the readout chip area and from the fine spatial resolution resulting from the small pixel pitch on the sensor side.

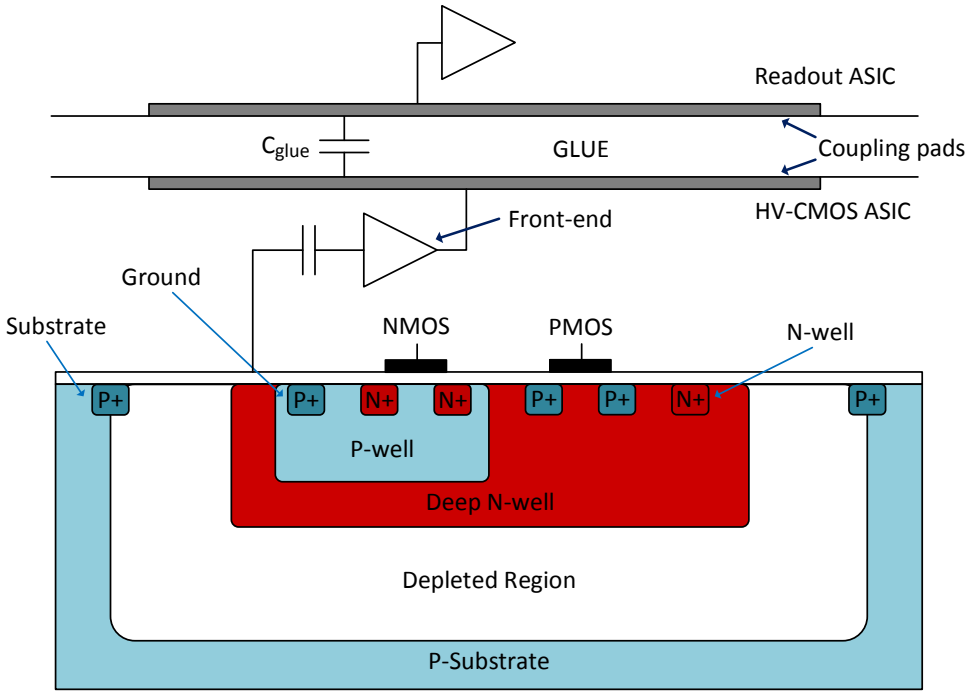


Figure 3.14 Schematic cross-section of a capacitively coupled assembly with an active HV-CMOS sensor.

The use of capacitively coupled assemblies with HV-CMOS sensors has several advantages as it offers a sensor with fast charge collection time that can be connected to the readout chip without the expensive and complex bump-bonding process. The sensor and readout chips can be independently optimised in order to achieve a high-end performance.

Because of its benefits, this concept has been considered as a candidate for the CLIC vertex detector and after a first generation of chips [71], a second generation has been designed, produced and extensively tested in the framework of the CLIC vertex detector study [73, 74]. The design and characterisation of the HV-CMOS sensor used in the latter assemblies is presented in detail in Chapters 5 and 6.

On the other hand, capacitive coupling adds to the system complexity as now two chips are operating at the same time. As will be shown in Chapter 6, the gluing process can introduce significant inhomogeneities to the detector. In addition, the sensor chip may now consume a considerable portion of the system's power budget.

3.3.4 Monolithic pixel sensors with charge collection on epitaxial layer

As introduced in Section 3.3.1, processes with a deep P-well shielding the N-well where the electronics are placed and a high resistivity epitaxial layer have been studied for developing

monolithic pixel sensors. A process with charge collection on a highly resistive epitaxial layer has been extensively studied in the context of the ALICE Inner Tracker System Upgrade [75, 76]. Because of the high resistivity of the substrate, sensor chips designed in such processes are often referred to as High-Resistivity CMOS sensors (HR-CMOS).

The junction between the non-shielded N-well and the P-type epitaxial layer acts as the collecting diode. In order to reduce the sensor capacitance and to speed up the charge collection time, the collecting diode is now reversely biased. The depletion region then grows around the collecting N-well. A cross-section of this process is illustrated in Figure 3.15.

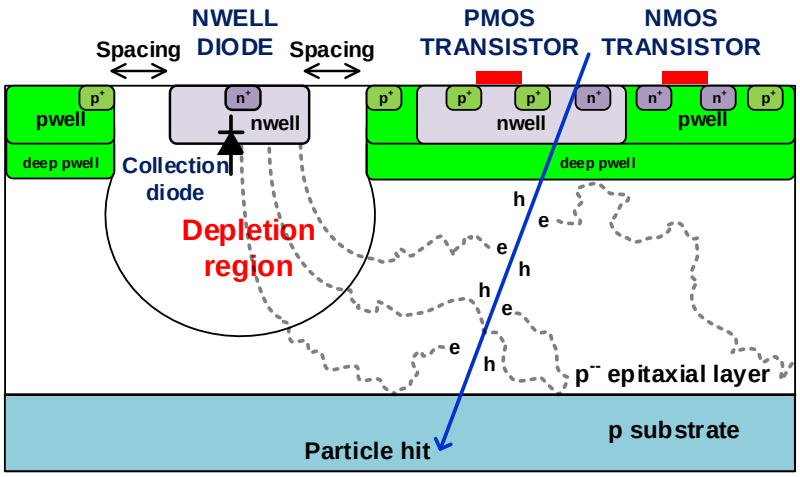


Figure 3.15 Schematic cross-section of a monolithic pixel in a process with an additional deep P-well and charge collection on epitaxial layer. From [75].

The ALPIDE chip is a monolithic pixel detector chip that has been developed using this process targeting the requirements of the ALICE ITS. The requirements for the ALICE ITS include a power consumption below $100\,\mathrm{mW/cm^2}$, a pixel pitch of $\sim 30\,\mu\mathrm{m}$ and a sensor thickness of $50\,\mu\mathrm{m}$. About 12.5 billion pixels (or 24000 ALPIDE chips, each with 512×1024 pixels) are needed to cover the total sensitive surface of $\sim 10\,\mathrm{m^2}$. The ALPIDE pixel contains the N-well collection diode, a reset circuit, the analog front-end (an amplification stage followed by a comparator) and local digital logic for latching the hit information.

Among the advantages of such a process are the possibility to use both NMOS and PMOS devices in the pixel (and potentially CMOS digital logic) without coupling to the sensor, and the small detector capacitance. Typically, the collecting N-well is an octagonal shape with a diameter of $\sim 2\,\mu\mathrm{m}$, resulting in a sensor capacitance of only a few fF. A small sensor capacitance indicates a lower analog power consumption for the front-end, for a given

SNR and bandwidth, as described by Equation 3.12, where the analog power (P) is directly proportional to the ratio of the input signal charge (Q) over the input capacitance (C) [77]:

$$P \sim \left\{ \frac{Q}{C} \right\}^{-m} \quad \text{with } 2 \leqslant m \leqslant 4 \tag{3.12}$$

where the factor m equals 2 when the input transistor is in weak inversion and 4 when the input transistor is in strong inversion.

The study and design of monolithic HR-CMOS sensors was therefore appealing for particle physics applications where the (usually limited) material budget does not allow for complex cooling structures and the use of low power electronics is essential. In the case of the ALPIDE pixel, the power consumption is as low as 40 nW per pixel, for an input capacitance below 5 fF.

Since this process offers the option for having on-pixel digital logic, and the small input capacitance of the pixel is expected to allow for designing a low power front-end, it was considered as an option for the ASICs in the CLIC tracking detector. In addition, the already acquired experience in this process through the developments for other HEP experiments was important for selecting this process. The design of a monolithic detector chip for the CLIC tracker will be extensively presented in Chapter 7.

3.3.5 Monolithic SOI pixel detectors

A different process that has been used for the design of monolithic pixel sensors is the silicon-on-insulator (SOI) technology. This technology features a buried silicon oxide inter-dielectric layer (BOX) which is used to isolate the on-pixel electronics from the substrate and the collection diode, as illustrated in Figure 3.16. The collection electrode is an N-well placed on the highly resistive P-type substrate. All electronics are placed on top of the buried oxide layer and are therefore isolated from the substrate. Consequently, this technology can be suitable for designing monolithic pixel sensors with both NMOS and PMOS transistors in the pixel.

Different variations of the SOI process have been studied in the context of the monolithic pixel sensor design. One example is the high-voltage SOI (HV-SOI) process, where additional wells are added between the transistors and the oxide layer [78].

The SOI process has been investigated as an option for the CLIC vertex and tracking detectors. A prototype chip has been fabricated in the context of the CLIC detector study [79]. This monolithic pixel detector chip is designed in a 200 nm SOI CMOS process and features a matrix of 8×36 pixels. The pixel size is 30×30 μm^2 and 11 different versions have been included in the matrix for prototyping reasons. Measurement results have shown a noise

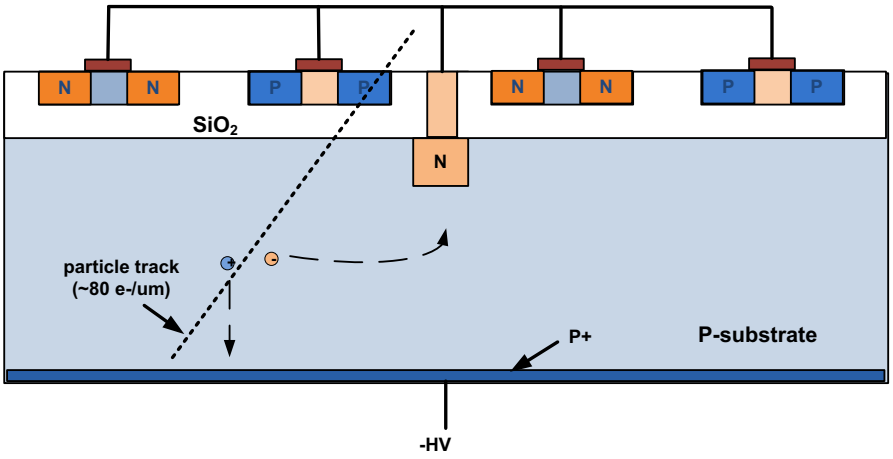


Figure 3.16 Schematic cross-section of a monolithic pixel in a SOI process. From [78].

of 120 to 320 e^- (depending on the pixel version) and an Signal-to-Noise ratio above 100, while the input capacitance of the pixel is about 15 fF.

3.3.6 Charged Coupled Devices

As introduced in Section 3.3, Charge Coupled Devices (CCDs) have initially been used as imaging devices [80]. The device consists of a matrix of potential wells created on top of a semiconductor. Charge carriers generated in the semiconductor are accumulated in the depletion region which extends several µm around the potential well. To read out the generated signal, the charge is shifted to the end of the column by moving the potential minimum along the device's surface. A CCD detector has a low input capacitance and therefore low noise can be expected. However, the way the signal is shifted out of the device to be processed limits the readout rate of the detector.

The pixel in a CCD detector is passive, meaning that the collected charge needs to be shifted out of the matrix to be read out, and no processing takes place on-pixel. Consequently, no timing information can be extracted from a CCD detector. For this reason, the CCD technology in particle detection applications was gradually replaced by CMOS where each pixel contains an analog front-end and possibly digital processing logic.

Nevertheless, CCDs have been used in past detector applications, among which in the SLD detector at the SLAC Linear Collider. In the SLD, a CCD-based vertex detector, consisted of 3.2 million pixels of 20×20 µm^2, was implemented and used for reconstruction of the tracks [81].

3.3.7 DEPFETs

The DEpleted P-channel Field Effect Transistor (DEPFET) technology has also been employed for implementing monolithic pixel detectors [82]. The Field Effect Transistor (FET) is placed on top of the high resistivity N-type substrate. On the bottom surface, a P-type contact is placed creating a large area diode (Figure 3.17). An additional, sidewards located, N-type contact is used to fully deplete the N-type bulk, by applying a high positive voltage bias. By choosing the appropriate doping profile and applied bias, a potential maximum, called internal gate, can be created underneath the transistor channel [83]. Electrons generated by a charged particle penetrating the detector volume are collected in the internal gate. The charge in the internal gate influences a mirror charge in the gate of the FET device. Therefore, the detector provides both position and energy information since the current in the transistor is modulated by the collected charge.

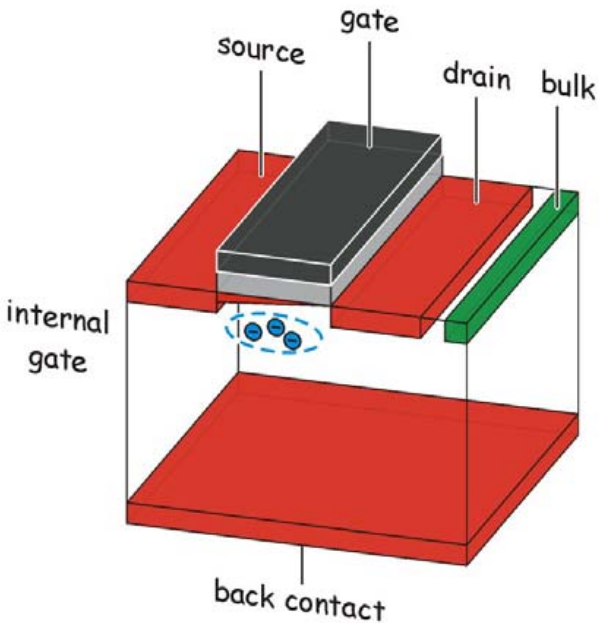


Figure 3.17 Schematic cross-section of a DEPFET pixel (from [83]).

DEPFET sensors developed in the framework of particle detector applications have demonstrated that the device can be suitable for building a monolithic detector. In the Belle II vertex detector [84], DEPFET technology is used, with a charge to current conversion gain of ~ 400 pA/e$^-$, a Signal-to-Noise ratio over 30, low input capacitance and non-destructive readout.

3.3.8 Trends and future perspectives

From the developments discussed in the previous sections, it is clear that the effort put into designing monolithic detectors is largely focused on isolating the on-pixel electronics from the collection electrode. This is realised either by placing the electronics in a separate well, or by using multiple, nested well structures to avoid coupling to the sensor volume. In addition, the charge collection by drift should be optimised in order to achieve a faster timing and improved radiation hardness in the detector.

Over the years, monolithic technologies have taken advantage of special features of certain processes, such as epitaxial layers, nested wells, high resistivity substrates etc. Although the principle of operation of a monolithic pixel detector could be applied to any CMOS process with a deep N-well to isolate the electronics from the substrate [85], other characteristics are required for building an efficient detector for HEP experiments. For example, standard CMOS processes are normally produced on low resistivity silicon wafers, which would not allow the creation of a large depletion region. Before starting the design in a certain process, the charge generation in the collection electrode should be studied by finite element simulations. The applicability of the process design rules to the desired pixel geometry should also be confirmed.

In Figure 3.18, monolithic detector chips designed in different process nodes over the years are presented. Although the general trend to use more downscaled technologies is observed, it is also clear that this is not always the case, for the reasons explained above. Other reasons, like the production cost of a chip are also taken into account.

Table 3.1 presents an overview of monolithic detector ASICs, which are representative of different processes. The process used to implement each ASIC is included in the table, along with the matrix size and the pixel dimensions. In Table 3.2, the main design parameters of the different ASICs are presented.

3.4 Selecting the process

Different criteria need to be taken into account when selecting a technology for a particle detector. Hybrid pixel detectors can benefit from the use of the latest CMOS processes. By employing a modern, deep sub-micron, CMOS process, complex signal processing logic can be included in a small pixel area and high data rates can be handled by the electronics. In addition, they can be more versatile compared to monolithic detectors as different sensor materials can be chosen. The sensor and the readout chip can be separately optimised, while in a monolithic process several limitations may arise from the fact that the sensor is placed on the same substrate with the electronics.

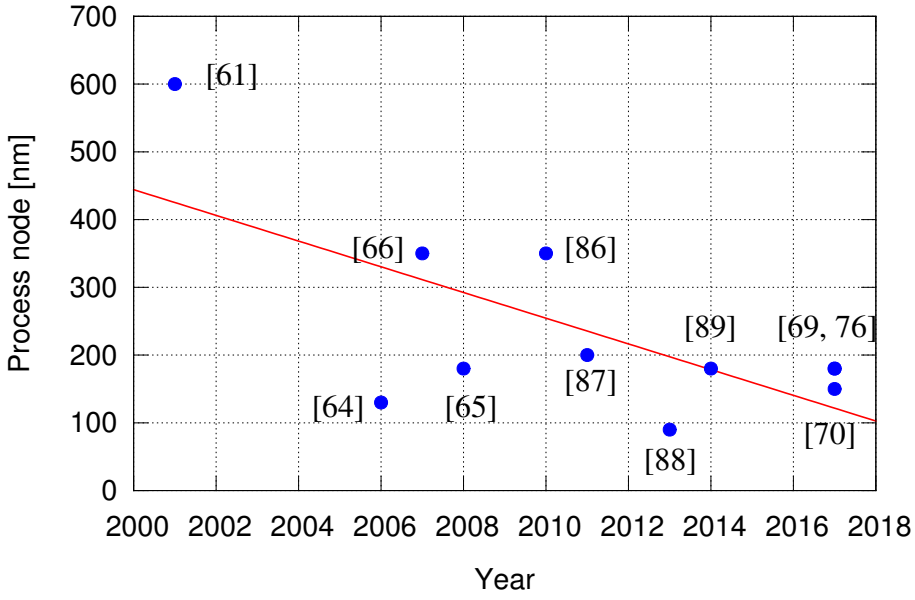


Figure 3.18 Different process nodes used for designing monolithic detectors over the years.

Table 3.1 Overview of monolithic detector ASICs, representative of the available technologies.

ASIC	**Year**	**Process**	**Matrix size**	**Pixel size** (μm^2)	**Ref.**
MIMOSA	2001	0.6 µm CMOS	64×64	20×20	[61]
Apsel1	2006	0.13 µm CMOS	8×8	50×50	[64]
HV-CMOS demonstrator	2007	0.35 µm HV-CMOS	4×10	50×50	[66]
TPAC1.0	2008	0.18 µm CMOS	168×168	50×50	[65]
ULTIMATE	2011	0.35 µm CMOS	960×928	20.7×20.7	[63]
ALPIDE	2016	0.18 µm HR-CMOS	512×1024	29.24×26.88	[76]
LF-Monopix01	2017	0.15 µm HV-CMOS	129×36	250×50	[70]
MuPix7	2017	0.18 µm HV-CMOS	32×40	103×80	[69]
SOI demonstrator	2018	0.2 µm FD-SOI	8×36	30×30	[79]

Table 3.2 Design parameters of monolithic detector ASICs.

ASIC	Cin (fF)	Power (mW/cm^2)	Noise (e^-)	Comments
MIMOSA	3.1	NS [a]	15 [b]	3 transistors per pixel Analog pixel outputs.
Apsel1	460	2400	40	On-pixel processing chain. Binary readout.
HV-CMOS demonstrator	180	1188 [c]	85	On-pixel processing chain. Binary readout.
TPAC1.0	NS [a]	400	23	150 transistors per pixel. On-pixel processing chain. Binary readout.
ULTIMATE	NS [a]	15	150	On-pixel front-end. Pulse digitised in periphery.
ALPIDE	< 5	5	10	On-pixel processing chain. Binary readout.
LF-Monopix01	400	216 [c]	125	On-pixel processing chain. 8-bit time-stamp and energy information.
MuPix7	NS [a]	300	NS [a]	On-pixel preamplifier. Discriminator and logic in periphery. 8-bit time-stamp
SOI demonstrator	15	NS [a]	$120 - 320$ [d]	On-pixel front-end. Analog pixel outputs.

[a] NS: data not specified in the reference.
[b] Pixel version with 1 collection diode.
[c] Power consumption of preamplifier only.
[d] Different pixel versions.

On the other hand, monolithic pixel detectors provide a lower material budget, as both the sensor and the readout electronics are placed on the same piece of silicon. The complexity of the modules is significantly reduced by avoiding the additional production steps needed for the bump-bonding process, while the cost of the detector can be as well decreased considerably. In addition, monolithic processes with a small collecting electrode can be used to achieve a small detector capacitance and thus a low power consumption [77].

Selecting a process requires a thorough evaluation of various parameters such as the required complexity of the on-pixel logic, the data rate that the detector will need to deal with and the restrictions in the geometry of the detecting elements. The required material budget and the limitations in power consumption are also critical for the process choice. In addition, the cost of producing the detectors in a certain process needs to be evaluated, as well as the long-term availability of the process.

Monolithic technologies, which are the main subject of this dissertation, usually require special attention to the custom features of each process, such as the collecting electrode geometry, the process cross-section and the well structures. The geometry of the collecting electrode is critical to the detector and must be carefully selected. From the technologies presented in the above section, we can distinguish two main categories of collecting electrode. First the large area electrode, with the electronics placed on it (Section 3.3.2), and second the small area electrode, with the electronics placed on a separate well (Section 3.3.4). A large collection electrode offers the advantage of having a larger depleted volume and thus faster charge collection in the whole pixel area. The detector capacitance in this case is of the order of 100 fF or higher, depending on the pixel size. On the other hand, a detector can benefit from the smaller detector capacitance (< 10 fF) and lower noise that can be achieved using a small collection electrode. Isolating the collecting well from the rest of the electronics is also vital for the design.

Another important parameter in selecting and designing integrated circuits for detectors in HEP experiments is the radiation hardness of the electronics. In modern collider experiments, the electronics placed close to the detector's interaction point, where the particle fluence is high, may suffer damage due to radiation-induced effects. The behaviour of the process under irradiation has therefore to be extensively characterised to verify whether it is suitable for the environment of the detector. This can be a time consuming procedure, and different design techniques have been developed to tackle this problem [90]. However, as described in Section 1, radiation effects are not a concern for the environment of the CLIC detector and their study is beyond the scope of this dissertation.

In general, nowadays a higher performance can be achieved with hybrid pixel detectors, with more complex circuitry, due to the fact that smaller process nodes can be used and the

sensor is not integrated in the same substrate as the electronics. The fully depleted sensor allows for a fast charge collection. Monolithic technologies can offer a more cost-effective solution, with lower material budget (the detector can be as thin as 50 µm). In monolithic processes with a small collection diode, a lower power consumption and lower noise can be achieved, thanks to the low detector capacitance.

Chapter 4

Requirements for the ASICs in the CLIC vertex and tracking detector layers

4.1 Requirements for the CLIC vertex detector

Given its location close to the interaction point, the CLIC vertex detector requirements [4] are highly demanding, both in terms of performance and the challenging material budget. The material budget is limited to 0.2% of the radiation length (X_0) per detection layer (including the sensor and readout electronics, supports and connectivity), which corresponds to only 100 µm of silicon, for both the sensor and readout technology. This requirement indicates that both the sensor and the readout ASICs have to be thinned down to about 50 µm each. The radiation length (X_0) is a characteristic of a material, defined as the mean distance over which a high-energy electron loses all but $1/e$ of its initial energy when interacting with that material. The value of the radiation length in silicon is about 10 cm.

In addition, as only air-flow cooling can be provided due to these material constraints, the power consumption of the system is limited to $50\,\mathrm{mW/cm^2}$. This can be achieved by taking advantage of the low duty cycle of the CLIC beam, allowing the introduction of a pulsed powering scheme in order to keep the main driving stages of the front-end in a standby state most of the time, from which they can be powered on quickly for the duration of the bunch train.

The required spatial resolution for the CLIC vertex detector is ~ 3 µm (in both directions), which limits the size of the detecting cells. To reach this spatial resolution, a pixel size of 25×25 µm^2 is needed, along with the energy information per pixel.

Regarding the timing measurement, a time-tagging with 10 ns bins is needed in order to achieve the required 5 ns accuracy. As no multi-hit processing capability is foreseen, the timing measurement will be performed only for the first hit per pixel and bunch train [91].

The pixel occupancy per bunch train is expected to reach up to 3%. A trigger-less, frame-based readout is foreseen for reading out the chip between subsequent bunch trains. Compression algorithms can be implemented in order to reduce the amount of data that is shifted out of the chip.

In view of the above requirements, a readout chip has been produced and it is foreseen to operate with either passive sensors bump-bonded on it or with active capacitively coupled HV-CMOS sensors. Design challenges occur due to the fact that a simultaneous, on-pixel timing and energy measurement is required and the processing chain will need to fit in a very small pixel area. The design and characterisation of a capacitively coupled HV-CMOS sensor developed in the framework of the CLIC vertex detector will be presented in Chapters 5 and 6. The main requirements for the electronics in the CLIC vertex detector are presented in Table 4.1.

Table 4.1 Requirements for the CLIC vertex detector.

Requirement	**Value**
Single point resolution	3 µm (both dimensions)
Pixel size	25×25 µm^2
Time measurement (ToA)	8 bits, 10 ns bin
Energy measurement (ToT)	5 bits
Hit detection efficiency	$> 99.7 - 99.9\%$
Silicon thickness	$\sim$ 100 µm (total)
Power consumption	$<$50 mW/cm^2 (after power pulsing)

4.2 Requirements for the CLIC silicon tracker

The requirement for single point spatial resolution in the different layers of the CLIC silicon tracker is 7 µm in the transverse plane, less stringent compared to the 3 µm for the vertex detector [10]. The detecting cell pitch in the transverse plane is therefore limited by this requirement. In the long direction, the cell area is limited by the expected hit rates. The maximum expected hit rates from beam-induced background particles in the innermost tracker layers, including safety factors, are approximately 0.6 hits/mm^2/bunch train. Frame-based readout of the entire bunch train, without multi-hit capability, is therefore feasible

for pixel areas not exceeding a few percent of $0.6\,\mathrm{mm}^2$. This is first due to the fact that no multiple hits are expected in the same cell during a bunch train, and second thanks to the low duty cycle of the CLIC beam that allows for a full readout of the chip during the inactive period.

Thanks to the liquid cooling foreseen for the tracking layers of the CLIC detector, the average power consumption can be higher compared to the one for the vertex detector, up to $150\,\mathrm{mW/cm}^2$. Similar to the vertex detector, a power pulsing scheme is applied, setting the circuit to a standby mode between subsequent bunch trains.

The total material budget should be limited to $1-1.5\%\ \mathrm{X}_0$ per detection layer, depending on the position of the layer in the tracker. This material budget includes the sensor and readout ASICs, supports, cables and cooling. The amount of the material budget corresponding to the silicon layers (sensor and readout electronics) allows for a total thickness of ~ 200 µm.

Regarding the timing measurement, a time-tagging resolution of 10 ns is required for the ASICs in the CLIC tracking layers (same as for the vertex detector). For the prototype chip, a time measurement (Time of Arrival - ToA) with 8 bits range and 10 ns time-tagging and an energy measurement (Time over Threshold - ToT) with 5 bits precision are proposed. For operation at the CLIC beam, 4 bits of ToA measurement would be sufficient for the 156 ns of the bunch train. However, an 8 bit ToA measurement would facilitate laboratory and beam tests, as it can cover data taking for longer periods. The ToT measurement will let the user apply time-walk correction algorithms and help to improve the spatial resolution by analysing the charge sharing between neighbouring detecting cells.

The need for a low mass and large area tracking detector motivated the development of a novel monolithic detector chip, which will be presented in Chapters 7 and 8. The monolithic technology was selected as it is more cost effective and the assembly will be less complicated. As described above, the requirements for the CLIC silicon tracker call for a pixelated chip with high density processing electronics (both analog and digital) placed on the same substrate. Effort has been put on carefully separating the two domains (analog and digital) in order to implement an efficient chip with fast timing measurement and on-pixel signal processing. Table 4.2 summarises the requirements for a prototype chip for the CLIC silicon tracker.

Table 4.2 Requirements for a chip for the CLIC silicon tracker.

Requirement	**Value**
Single point resolution	7 µm (transverse plane)
Maximum strip length	$1-10$ mm
Time measurement (ToA)	8 bits, 10 ns bin
Energy measurement (ToT)	5 bits
Hit detection efficiency	$>99.7-99.9\%$
Silicon thickness	~ 200 µm
Power consumption	$<150\,\mathrm{mW/cm^2}$ (after power pulsing)

Chapter 5

Design of the C3PD HV-CMOS active sensor chip

5.1 The selected process for the C3PD design

As described in Section 3.3.2, designing HV-CMOS devices involves placing all of the on-pixel functionality inside a deep N-well, which both shields the electronics from the P-type substrate (allowing the application of a relatively high bias voltage, up to several tens of Volts) and acts as the charge collection node. This substrate bias allows the formation of a relatively thick ($\sim$ 10 µm, depending also on the wafer resistivity) depletion region. The detector can thus benefit from the fact that the drift component is collected quickly due to the strong electric field in the depleted region. Charge collected on the N-well can be processed on-pixel by a preamplifier, and can then be digitised and read out either on the same chip (monolithic detector [66]), or through capacitive coupling to a readout chip [92], as introduced in Section 3.3.3. In the latter case, the collected charge is amplified and then transferred through a thin (a few µm) layer of glue to the readout chip for further processing. The two chips are precisely aligned and glued together by applying a thin layer of epoxy glue between them.

The benefit of this approach compared to a monolithic detector is that the digital circuitry can be decoupled from the sensor by means of placing all the (fast-switching) digital logic in the readout chip. Thus, noise injection to the sensor due to the digital circuitry can be avoided. Compared to hybrid pixel detectors with planar sensors, the complications and cost of bump-bonding the sensor to the readout chip are overcome by glueing the two chips together. However, the trade-off is that complications are added at readout system

level (compared to hybrid assemblies with passive sensors), as this approach requires more elaborate PCBs and wire-bonding schemes, due to the two ASICs operating simultaneously.

The concept of capacitive coupling between a HV-CMOS sensor and a readout chip has been investigated in the context of the vertex detector studies for the proposed high-energy CLIC collider. A readout chip (CLICpix [93]) has been designed, fabricated and tested extensively with a first-generation of capacitively coupled HV-CMOS sensors [71].

In this chapter, the design of a new sensor chip, the CLICpix Capacitively Coupled Pixel Detector (C3PD), is presented. The design was based on the requirements for the CLIC vertex detector, as presented in Section 4.1. The C3PD is designed to be compatible with the CLICpix2 [94] readout chip, which is the successor of CLICpix and is based on the same front-end architecture as described in [93]. In order to match the footprint of the CLICpix2, C3PD contains a matrix of 128×128 pixels measuring 25×25 µm^2, for a total matrix area of 3.2×3.2 mm^2. The chip was fabricated in a commercial 180 nm HV-CMOS process, using the standard substrate resistivity of ~ 20 Ωcm, as well as higher resistivity wafers (80, 200 and 1000 Ωcm). This is a triple-well process, with all PMOS and NMOS transistors enclosed within the deep N-well.

Parts of the work presented in Chapters 5 and 6 have also been published by the author in [73] and [74] and are quoted verbatim.

5.2 The C3PD chip design

5.2.1 The C3PD pixel

Design considerations

According to finite element Technology Computer Aided Design (TCAD) simulations [68], a thickness of the order of ~ 10 µm is expected for the depletion region with the standard substrate resistivity and a reverse bias of -60 V. The input of the front-end is coupled to the deep N-well, so that the collected charge is integrated in the charge sensitive amplifier. The output of the amplifying circuit is routed to the coupling pad in order to be injected to the readout chip. A schematic cross-section of the assembly, including the P-well and deep N-well where the NMOS and PMOS transistors are placed, as well as the coupling between the sensor and readout chip, is shown in Figure 7.1.

As introduced in Section 3.3.2, a limitation of the technology used for the C3PD sensor circuit design is that any P+ diffusion in the N-well is coupled to the preamplifier input. The use of PMOS transistors is therefore minimised in order to avoid this parasitic coupling and to reduce undesired signal injection into the sensor.

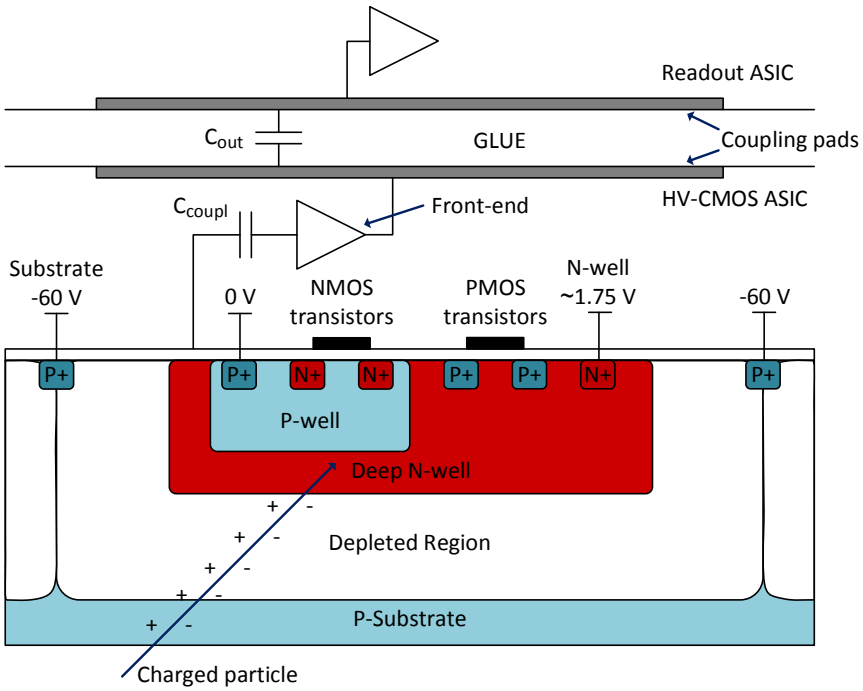


Figure 5.1 Schematic cross-section of a capacitively coupled assembly.

In order to suppress out-of-time background hits in the detector, a time slicing of hits with 10 ns time bins is required for the readout chip [4]. To ensure that the output signal from the HV-CMOS sensor will be fully integrated within the integration time of the CLICpix2 readout chip ($\sim$ 50 ns), a fast charge injection is needed and therefore a rise time of the order of 20 ns is aimed for.

Simulations of the coupling capacitance between the two chips (C_{out} in Figure 7.1) have shown that the expected capacitance is $\sim$ 3 fF, for a measured pad distance of 3 µm. The space between the pads is mainly occupied by the passivation layer of the C3PD chip, with a thin layer of glue between the two chips [95].

A most probable charge of 800 e^- was assumed to be deposited by a Minimum Ionising Particle in the 10 µm thick depletion region, with collection via drift (without taking into account the charge collected via diffusion). The charge gain of the amplifier should therefore be high enough to transfer a charge well above the minimum that can be detected by the readout chip, in order to compensate for charge sharing, statistical fluctuations and to account for the expected noise levels of a few tens of electrons (simulated, as well as measured noise levels will be discussed in section 6.1.3) and possible uncertainty in the values expected from simulations. For a collected charge of 800 e^- and a charge gain of 120 mV/ke^-, the pulse amplitude at the output of the sensor chip will be 96 mV. Assuming a coupling capacitance of

3 fF, this pulse will inject ~ 1.8 ke$^-$ at the input of the readout chip, well above the simulated minimum threshold for the readout chip (~ 600 e$^-$). The detector is therefore expected to be fully efficient.

The main requirements for the C3PD design are summarised in Table 5.1.

Table 5.1 Requirements for the C3PD prototype.

Requirement	**Value**
Pixel size	25×25 µm^2
Sensor thickness	50 µm (after thinning)
Rise time	~ 20 ns
Charge gain	> 120 mV/ke$^-$
Power consumption	$< 50\,\mathrm{mW/cm^2}$ (after power pulsing)

Pixel design

The C3PD pixel was designed following the specifications listed above. A block diagram of the pixel is shown in Figure 5.2 and the detailed pixel schematic is illustrated in Figure 5.3. The charge deposited in the diode is amplified by a charge sensitive amplifier (CSA) (transistors M0−M3 in Figure 5.3), which is followed by a unity gain buffer (transistors M4, M5) placed inside the feedback loop in order to maintain a fast rise time after loading the circuit with a capacitance, and to improve the pixel-to-pixel homogeneity. The phase margin for this design is $> 75°$ (as simulated for different corners). A single power supply is used for the front-end, where an NMOS device (M0 in Figure 5.3) is used as input transistor. An NMOS transistor was selected for the input as it is expected to have better performance in terms of power supply rejection ratio. The sensor capacitance for such a pixel size in this process is expected to be up to 40 fF, taken as a conservative (worst case) value.

A power pulsing scheme has been introduced, where the most power consuming nodes of the analog front-end (CSA and unity gain buffer) can be set to a "power-off" state between subsequent bunch trains. This is realised by means of multiplexing "power-on" and "power-off" biasing DACs for each node, in order to switch between the two states. The possibility to inject test pulses with a programmable amplitude to individual pixels was also implemented for the C3PD chip.

As mentioned above, the number of PMOS transistors has been kept as low as possible. Aside from the ones in the sensor biasing circuit (transistors M9, M10 in Figure 5.3), only 2 PMOS transistors (M2, M3) are used, which have their common diffusion merged in the

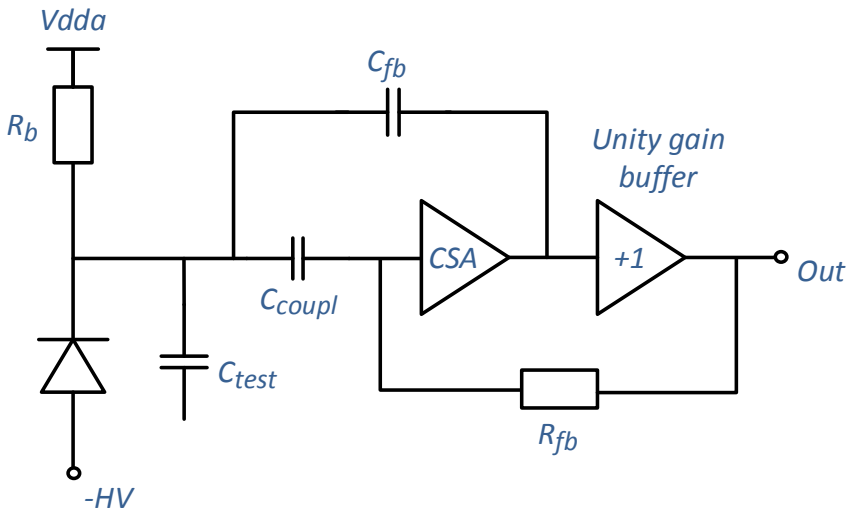


Figure 5.2 C3PD pixel block diagram.

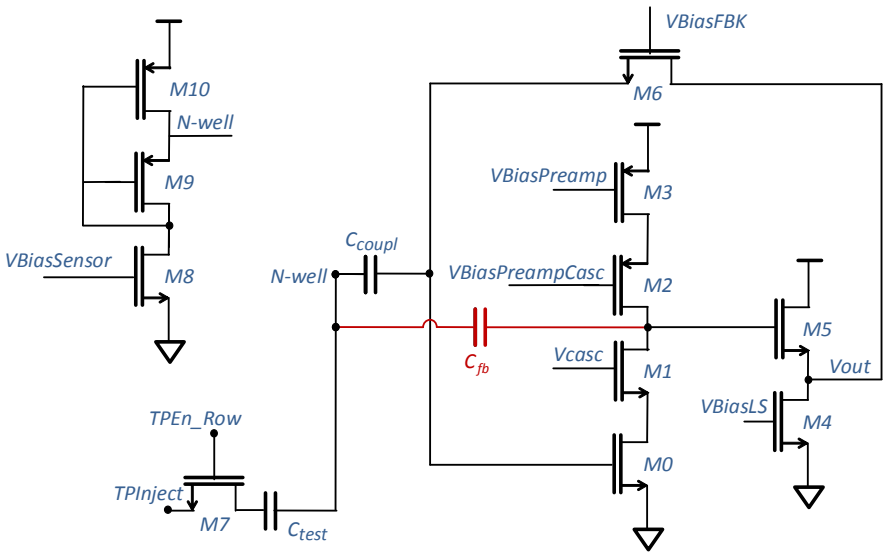


Figure 5.3 C3PD pixel schematic. The parasitic feedback capacitance is shown in red colour.

layout, thus minimising the circuit area covered by P+ diffusion. The parasitic feedback capacitance (C_{fb}, shown in red in Figure 5.3) is the drain to N-well capacitance of M2. The transistor M6 serves as the resistive feedback (R_{fb} in figure 5.2), providing a continuous reset for the circuit. Care was put into optimising the pixel layout, since such a design is sensitive to parasitic capacitances and different ways of placing the devices and routing the signals would likely result in significant performance variations. The pixel was therefore simulated systematically using the extracted layout view, in order to take into account the parasitic capacitances. In this way the layout was optimised by means of minimising the parasitic coupling to the sensor. The pixels are organised in a double column structure where adjacent pixels share common biasing lines. The layout of a double pixel is shown in Figure 7.4.

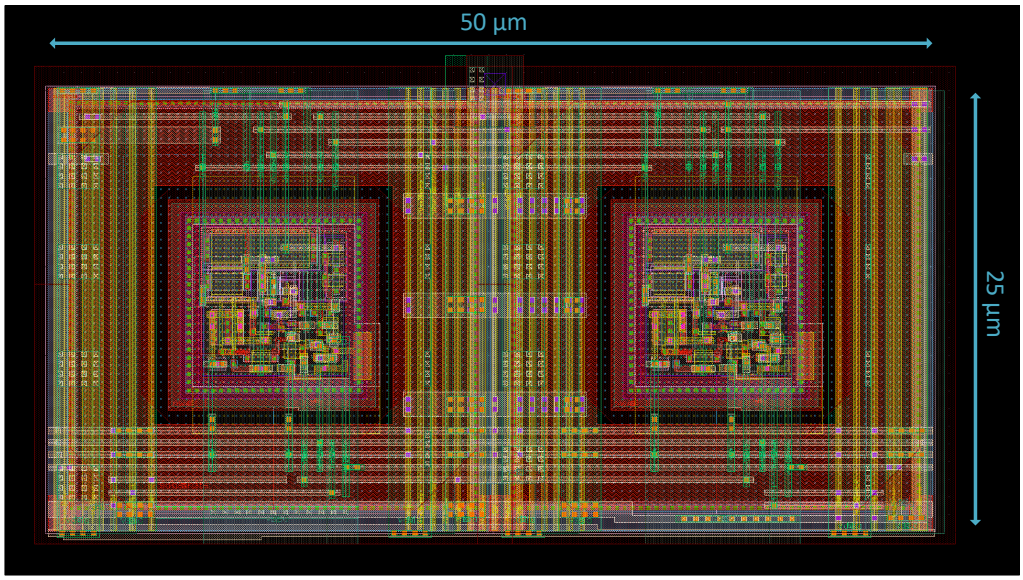


Figure 5.4 C3PD double pixel layout. The pixels are shown to the left and the right side. The biasing lines are routed between the pixels.

5.2.2 The C3PD periphery and interface

The C3PD matrix consists of 128×128 square pixels, arranged in 64 double columns, with 25 µm pitch. Three slightly different variations of the pixel can be found within the matrix for prototyping purposes. The main part of the matrix (62 double columns) consists of regular pixels, while the two rightmost double columns include structures for testing different flavours of pixels. The first of the testing columns comprises pixels with a metal-to-metal coupling capacitance (C_{coupl} in Figure 5.3) instead of a CMOS gate capacitance. The expected benefits of the metal-to-metal capacitor are its linearity and the fact that the circuit

can have a larger coupling capacitance while making more area available for active devices. The second testing column features a modified sensor biasing scheme, with a single PMOS transistor used to bias the sensor in order to simplify the design. The performance of these test structures will be studied using capacitively coupled assemblies with the readout chip. The C3PD matrix also features alignment marks, matching those on the readout chip. This will allow precise alignment of the two chips during flip-chip assembly.

A block diagram of the chip is presented in Figure 5.5. In the digital domain, a standard I^2C interface has been implemented which is responsible for controlling the biasing DACs, the power pulsing and the test pulse generation [96, 97]. Two address pins are used in order to define different chip addresses on the I^2C bus, opening the possibility of multi-chip modules. In the analog periphery, the biasing block comprises 8-bit DACs designed using binary weighted current source architecture. A list of the DACs in the analog periphery is presented in Table 5.2. The possibility to monitor voltages produced by the on-chip DACs has been implemented. Similarly, any of the voltages produced by on-chip DACs can be overwritten by an external source (only one voltage can be monitored or overwritten at a time).

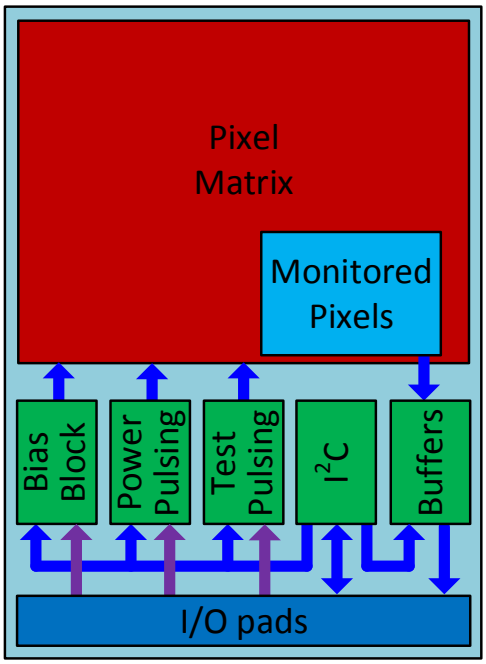


Figure 5.5 C3PD chip block diagram.

In order to study the analog performance in standalone mode, a 3×3 cluster of pixels with direct analog readout of the preamplifier output has been implemented, with the outputs multiplexed in order to read them out in different configurations. The cluster is placed at

Table 5.2 List of DACs in the C3PD analog periphery

DAC	Resolution	Biasing node
VBPRE	8 bits	Preamplifier current source
VBPCAS	8 bits	Low voltage current mirror
VBOALF	8 bits	Low Frequency Operational Amplifier
VBOAHF	8 bits	High Frequency Operational Amplifier
VBLS	8 bits	Level shifter
VBFBK	8 bits	Feedback transistor
VBS	8 bits	Regular sensor bias
VBSP	8 bits	Sensor bias circuit with PMOS transistor
VBPREOFF	8 bits	Preamplifier current source - standby
VBLSOFF	8 bits	Level shifter - standby
VBTP	8 bits	Test pulse voltage amplitude

the bottom-right edge of the 62 regular double columns. Four out of the nine pixels are monitored each time, and depending on the selected configuration the pixels connected to the outputs can be in the same row, in the same column, or forming a square. This would allow to study whether any pixel-to-pixel variations are a result of the way the pixels are laid out in the matrix. Figure 5.6 presents the possible patterns that the pixels in the monitored cluster can be connected to the output pads, depending on the value written to the "PMC" register in the digital periphery. The pixels that are monitored each time are highlighted in green. Unity gain buffers have been placed in the analog periphery in order to drive these signals to the wire-bond pads. A dedicated pixel (pixel "7" in Figure 5.6) has also been implemented where the test pulse voltage injected into the pixel (that would typically reach the test pulse injection capacitance, C_{test}, in Figure 5.3) is directly connected to the coupling pad. This can be used to directly measure the capacitance between the C3PD and the readout chip, using the known voltage on this pad and measuring the calibrated charge deposited on the readout ASIC.

5.2.3 Integration and verification of the C3PD chip

The digital-on-top approach was used for integrating the C3PD design. Following this approach, all analog and digital blocks in the chip are described by Verilog modules which are instantiated in a Verilog file describing the full chip (RTL netlist). All connections between the different blocks are defined in this file. The design is then synthesized, taking

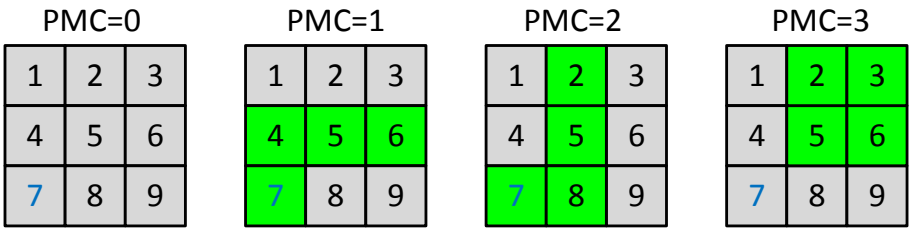
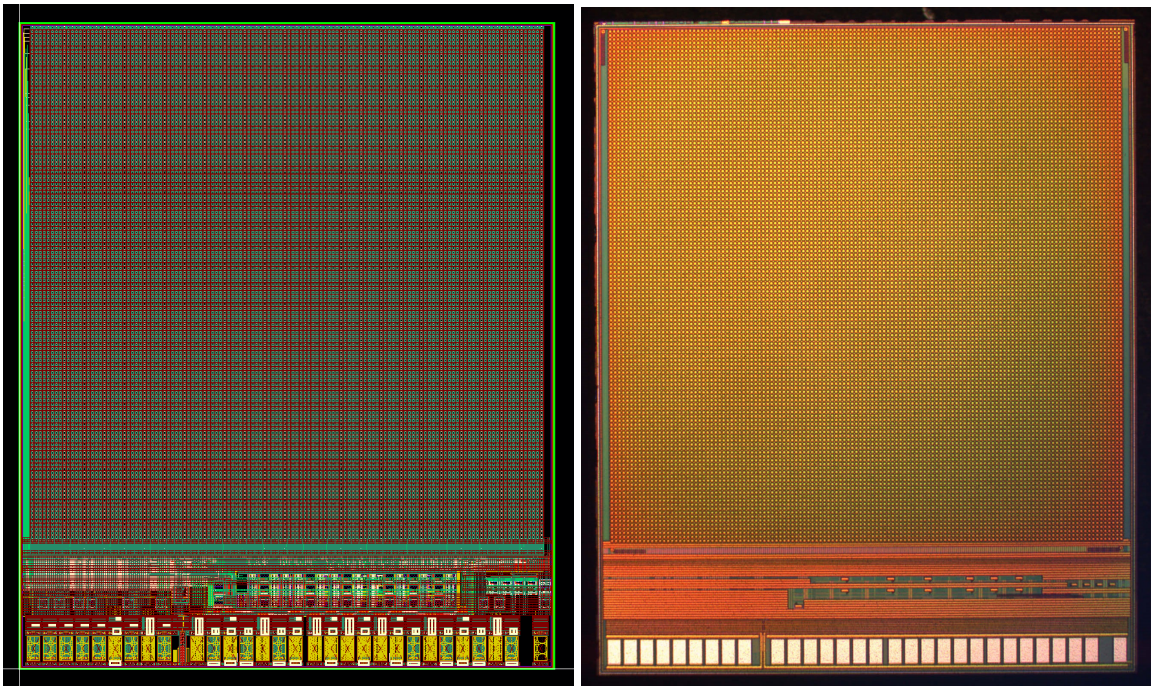


Figure 5.6 Configurations of the C3PD monitored pixel cluster. The monitored pixels in each configuration are marked in green. Pixel "7" is used for monitoring the test pulse voltage amplitude.

into account different constraints applied based on the various parameters of the design. Such constraints include clock domains, switching activity, load for the output pins, definitions of synchronous and asynchronous signals etc. The output of the synthesis is a Verilog file where all behavioural code has been translated to gates from the digital library used in the process. The design is now ready to be placed and routed. This generated netlist is input to the "place and route" tool, where the chip layout is defined. Placement of the blocks, clock tree synthesis, routing of the signals and power, are all implemented using scripts that are executed by the place and route tool. At the end of the placement and routing flow, the tool generates another Verilog netlist including all blocks that have been added during the implementation of the design (e.g. clock buffers, delay cells etc.). A file including the delays for all signals due to the parasitic capacitances of the lines is also generated. These two last files can be used to verify the post-layout generated netlist and detect any functional or timing-related issues that may have occurred during placement and routing of the circuit.

For verifying the C3PD design, the Universal Verification Methodology (UVM) [98] was used. The verification was focussed on the digital periphery of the chip (slow control interface). The C3PD slow control was extensively verified in different corners using both the RTL and the post-layout extracted netlist.

Following the functional verification, the physical verification of the C3PD chip took place. There, the Design Rules Check (DRC) and the Layout Versus Schematic (LVS) tests were run in order to verify that the layout is ready for submission. The complete layout, as well as a microscope photo of the C3PD chip, are presented in Figure 5.7. A list of the C3PD I/O pins is presented in Table 5.3.



(a) (b)

Figure 5.7 (a) Layout and (b) microscope photo of the C3PD chip.

Table 5.3 List of I/O pins in the C3PD prototype.

Pin	**Dir.**	**Description**
SDA	CMOS I/O	I^2C data line
SCL	CMOS In	I^2C clock line
ADDR[1:0]	CMOS In	I^2C address LSBs
PWRE	CMOS In	Power pulsing signal
TPS	CMOS In	External test pulse signal
RSTN	CMOS In	Reset signal (active low)
ANALOG_IN	Analog In	Analog input
REF	Analog In	Reference voltage
ANALOG_OUT	Analog Out	Analog output
PIX[3:0]	Analog Out	Monitored pixel outputs
VDDA	Power	Analog power supply (1.8 V, 6 pins)
GNDA	Ground	Analog ground (7 pins)
VDDD	Power	Digital power supply (1.8 V, 1 pin)
GNDD	Ground	Digital ground (1 pin)
HV	Reverse bias	High-Voltage bias (-60 V, 1 pin)

5.3 Submission with higher resistivity wafers

The C3PD chip was first submitted and produced with the standard substrate resistivity provided by the foundry ($\sim$ 20 Ωcm). Following this first submission, a second one took place with higher values for the substrate resistivity. The C3PD sensor chip was then produced on more wafers with $\sim$ 80, 200 and 1000 Ωcm resistivity. The effects of using the higher substrate resistivity are expected to be beneficial for the sensor, as the depleted volume will increase. This will subsequently lead to a larger amount of charge collected quickly, due to the augmented drift component, along with a decreased sensor capacitance [68]. In addition to the higher resistivity, a layout modification took place, in order to achieve a higher breakdown voltage. The metal contact of the HV-guardring surrounding the pixel was shrunk from 4.8 µm to 2.6 µm width. This modification is illustrated in Figure 5.8. According to TCAD simulations, presented in Figure 5.9, this modification is expected to contribute to increasing the breakdown voltage and thus allowing a higher sensor bias [99]. The higher applied bias along with the increased substrate resistivity will result in a larger depleted volume.

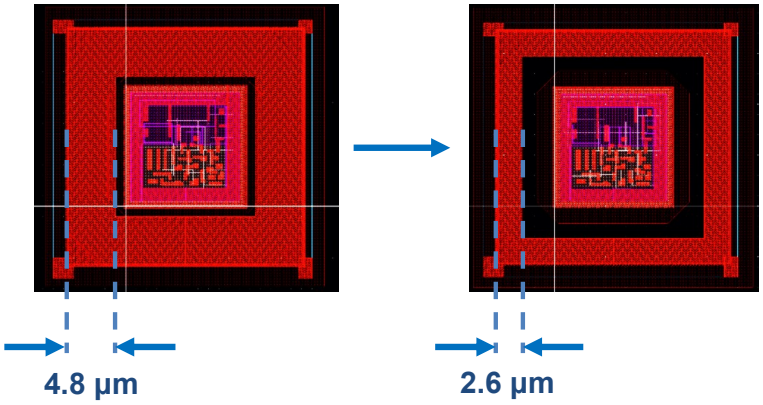


Figure 5.8 Modification in the metal contact of the HV-guardring in the C3PD pixel.

Capacitively coupled assemblies were produced and characterised in beam tests in order to confirm the expected benefits of using higher resistivity wafers.

5.4 Summary

The CLICpix Capacitively Coupled Pixel Detector (C3PD) is a pixelated active HV-CMOS sensor chip designed in the framework of the CLIC vertex detector. The prototype chip

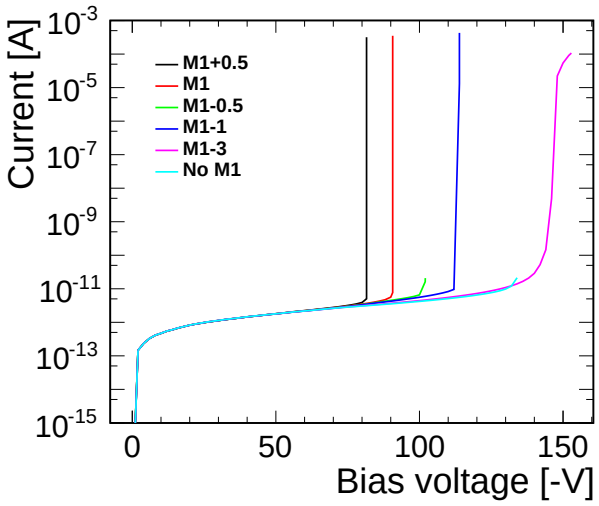


Figure 5.9 Leakage current as a function of the reverse bias voltage for different width of the metal contact. M1 is the original width of 4.8 µm. From [99].

will be used in capacitively coupled assemblies with the CLICpix2 readout chip. Therefore, the C3PD pixel matrix matches the one of CLICpix2, featuring 128×128 square pixels with 25 µm pitch. A monitored cluster of pixels is included to allow standalone tests of the C3PD front-end.

The prototype was produced with wafers with different substrate resistivity ($\sim$ 20, 80, 200 and 1000 Ωcm) and tested in standalone mode as well as in capacitively coupled assemblies with the readout chip. Characterisation results, based on both standalone tests and measurements with capacitively coupled assemblies, are presented in Chapter 6.

Chapter 6

Characterisation of the C3PD chip

After production, the C3PD chip was characterised in two steps. First, C3PD samples were measured using a standalone setup without the readout chip. These tests were focused on the monitored pixel cluster and the front-end performance was studied. Once capacitively coupled assemblies with the readout chip were available, the chips were tested with electrical test pulses and in beam tests. The results for both stages of the C3PD characterisation are presented in the following sections.

6.1 Standalone characterisation

6.1.1 Measurement setup

For the standalone characterisation of the C3PD samples, a measurement setup based on the micro-ASIC (uASIC) readout system was developed [100]. The uASIC is a multi-purpose readout system built around an FPGA development board with a Xilinx Spartan-6 FPGA [101]. The uASIC interface board is connected to the FPGA board and provides all signals needed to communicate with the chip. Power supplies, voltage inputs, CMOS inputs and the I^2C bus are all provided by the interface board. The option to monitor a voltage from the chip is also available using an ADC on the uASIC. The reverse high voltage bias is connected using an external power supply.

An additional, custom designed, PCB was produced for mounting the C3PD samples on it (see Appendix A.1). This chip-board is connected to the interface board and is where the chip is soldered and wire-bonded on. Apart from the chip, this board includes a level translator for the I^2C bus in order to match the 1.8 V power supply of the C3PD chip and a temperature sensor with 0.25°C accuracy. The outputs of the C3PD monitored pixel cluster are connected to operational amplifiers and then routed to connectors such that they can

be monitored using an oscilloscope. A 20 GSa/s sampling oscilloscope was used for the measurements described in the following sections. Rail-to-rail operational amplifiers with a fast rise time were selected for monitoring the pixel outputs, in order to not compromise the measurement of the C3PD preamplifier output.

A photo of the standalone C3PD setup with the uASIC readout system is presented in Figure 6.1.

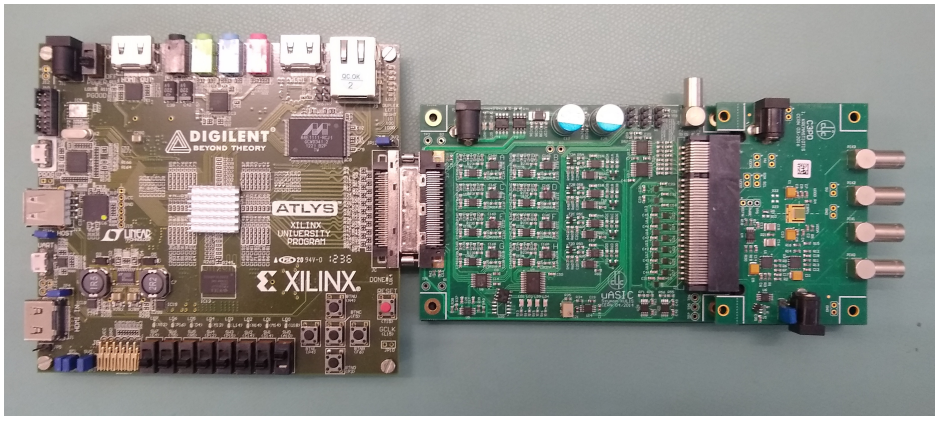


Figure 6.1 Photo of the uASIC setup. From left to right: FPGA development board, uASIC interface board, chip-board with C3PD mounted on it.

Standalone characterisation of the C3PD chip was initiated right after the first wafers, with the standard substrate resistivity, have been produced. The characterisation was focused on the monitored cluster of pixels and was performed using electrical test pulses and a ^{55}Fe source. In addition to the first samples with the standard thickness of 250 µm, C3PD samples have been thinned down to 50 µm and measured. The purpose of this test was to confirm that the functionality of the chip is not compromised when it is thinned down to the thickness needed for complying with the required material budget. Figure 6.2 shows a 50 µm thin C3PD sample wire-bonded on the chip-board.

In the following sections, the measurements for characterising the C3PD chip in standalone mode are described. During the measurements, the chip was powered continuously (without power pulsing), apart from the measurement of the average power consumption. All measurements were taken in room temperature, which is also the foreseen operating temperature in the experiment.

6.1.2 I-V characteristic

Once the sensor chips were produced and wire-bonded on the chip-board, the sensor leakage current was measured as a function of the applied reverse high voltage bias. The I-V

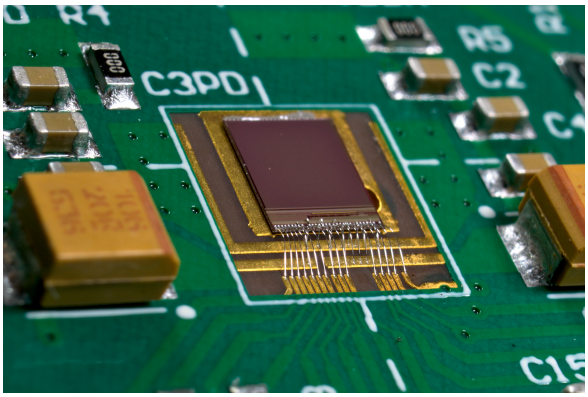


Figure 6.2 C3PD chip thinned down to 50 µm, mounted and wire-bonded on the PCB.

scan was performed for four samples with the standard thickness (250 µm) and two more samples thinned down to 50 µm. As presented in Figure 6.3, all samples show similar I-V characteristics, with the mean value of the sensor leakage current at the nominal reverse bias of -60 V at ~ 40 nA, measured for the full chip (thus corresponding to less than 2.5 pA per pixel). This leakage current is negligible compared to the total current consumed by the chip.

As expected, the leakage current of the reverse biased diode increases with the square root of the applied voltage, until the breakdown voltage, where a large increase is observed in the leakage current [99]. The fit of a square root function on the measured leakage current for one of the assemblies is shown in Figure 6.4.

For all measured samples, the diode breakdown voltage was between -68 and -70 V, value which is suitable for operating the chip at the nominal reverse bias (-60 V).

6.1.3 Measurements with test pulses

As mentioned in Section 5.2.1, the possibility to inject electrical test pulses to the inputs of selected pixels is implemented in the C3PD prototype. A voltage pulse is applied to a test pulse injection capacitance (C_{test}) which is connected to the input of the front-end, in parallel with the collection diode. The amplitude of the voltage pulse is set by a programmable 8-bit DAC in the analog periphery. Registers in the slow control interface allow the user to enable test pulse injection to selected pixels. Simultaneous test pulse injection to multiple pixels is foreseen.

Electrical test pulse injection was used to study the performance of the analog front-end. The operating point was configured scanning the biasing DACs in the analog periphery in order to tune the different nodes of the front-end (in particular the preamplifier, the unity gain buffer and the feedback transistor). Interpreting the results of such scans resulted in selecting the optimum settings for biasing the circuit with respect to the main performance parameters

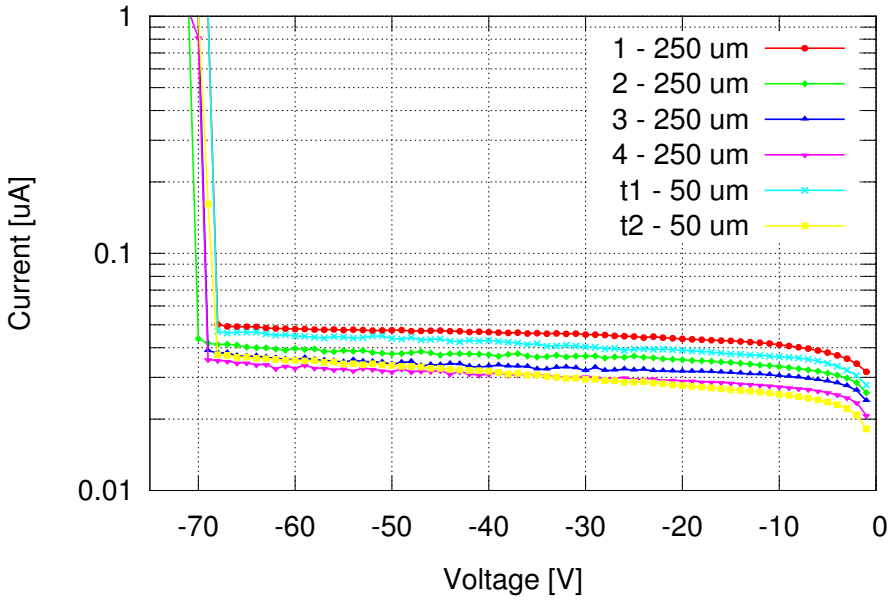


Figure 6.3 I-V curves of the measured C3PD chips. Samples with standard substrate resistivity ($\sim 20\ \Omega$cm).

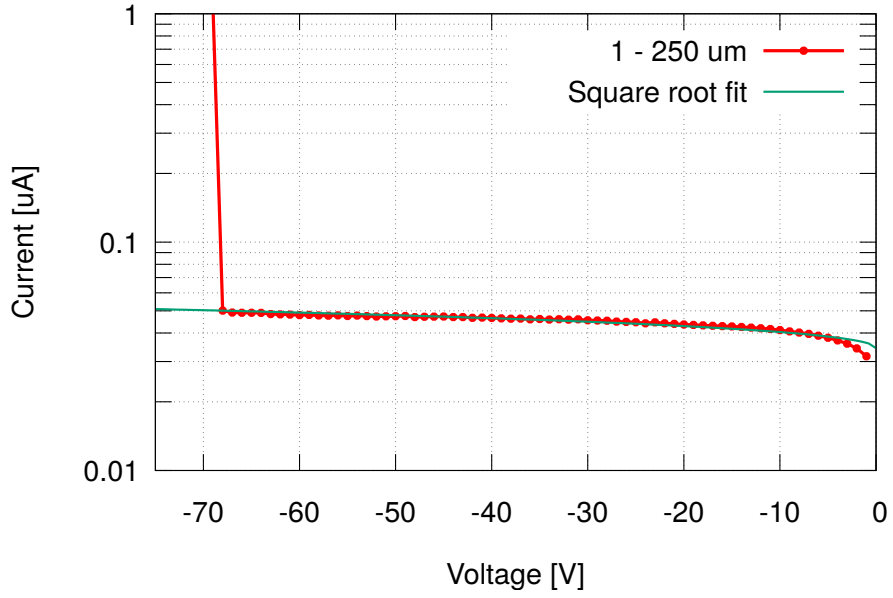
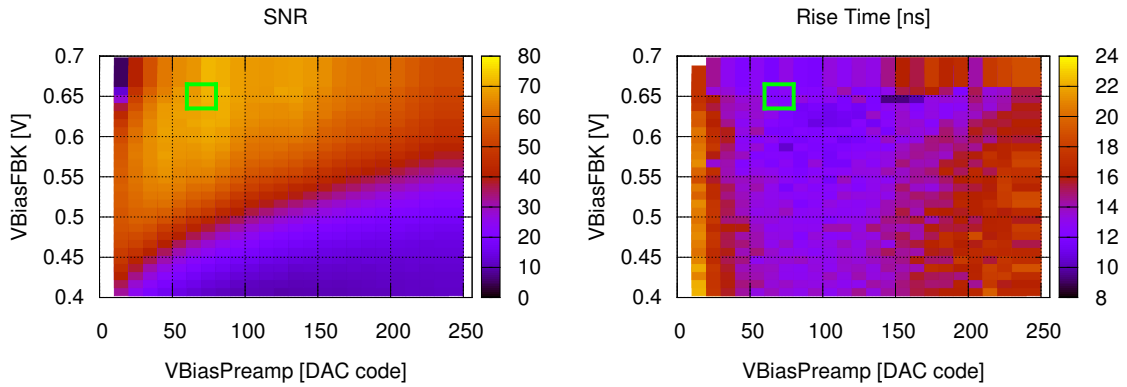


Figure 6.4 Fit of a square root function on the measured leakage current for one of the assemblies.

of the chip (amplitude, noise, rise time of the pixel output pulse and power consumption). During these calibration measurements, test pulses were injected to individual pixels in the monitored cluster. An example of the calibration measurements is presented in Figure 6.5, where the measured Signal-to-Noise ratio and rise time are plotted as a function of the biasing point for the preamplifier (DAC code in x-axis) and the feedback transistor (biasing voltage in y-axis). Scanning the feedback transistor biasing was done using an external voltage source (overwriting the internal DAC) in order to achieve a higher range for the voltage provided to the feedback transistor. The operating point was selected such that the SNR is maximised, while a fast rise time and a relatively low power consumption are maintained.



(a) (b)

Figure 6.5 (a) Signal-to-noise ratio and (b) rise time as measured for different biasing points of the preamplifier and the feedback. The chosen operating point is marked in green.

The measured amplitude at the pixel output as a function of the charge injected from the test pulse is presented in Figure 6.6. The amplitude is measured as the mean of 64 injected pulses and the corresponding DAC code is shown in the second x-axis. The injected charge was extracted knowing the test capacitance (see Section 6.1.5) and monitoring the voltage level of the test pulse as a function of the DAC code. As indicated in Figure 6.6, the dependence of the pixel output amplitude on the injected input charge is linear for an injected charge up to about 1.5 ke^-. This dependence was simulated to be linear for an injected charge up to 2 ke^-. The difference in linearity can be explained due to the difference between the measured and simulated charge gain (which is consistent with the disagreement in the feedback capacitance, as described in Section 6.1.5).

In Figure 6.7 the measured time walk is plotted as a function of the injected charge. To obtain this measurement, the trigger threshold of the oscilloscope was set to 33 mV, which corresponds to the amplitude which will inject the minimum detectable charge to the readout

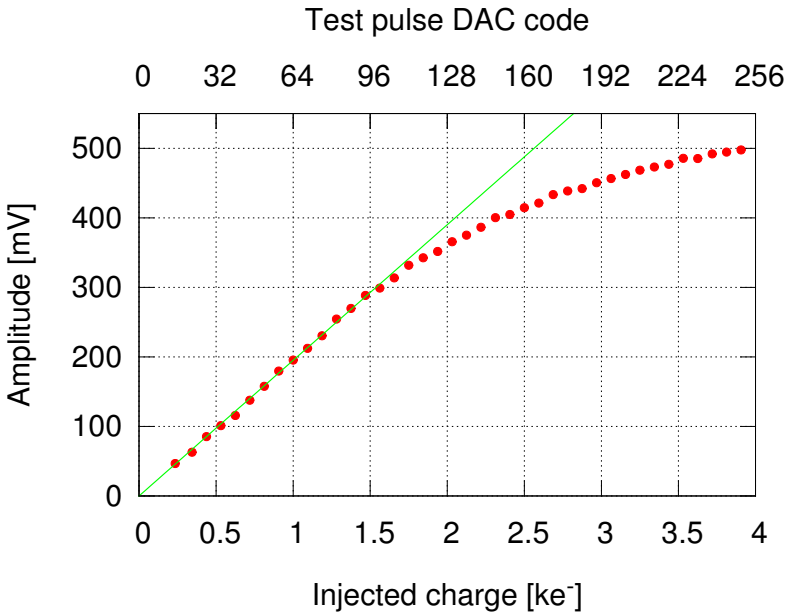


Figure 6.6 Output amplitude, averaged over 64 pulses, as a function of the injected test pulse DAC code and corresponding injected charge.

chip as explained in section 5.2.1. The time was measured between the moment when the test pulse strobe was sent and when the output signal crossed the threshold value. The vertical line at 800 e^- represents the expected average charge deposited by a MIP in the depletion region. In this plot, the offset resulting from the delay of the cables has been subtracted, in order to have a better view on the threshold crossing time depending on the input charge. As shown in Figure 6.7, the time walk for charges above 500 e^- is within the 10 ns time-stamping requirement. For charges below that value time walk correction can be applied using the energy information (Time-over-Threshold) provided by the readout chip.

For the above settings the average current consumption per pixel was measured at 2.67 µA, of which 2.44 µA is consumed by the preamplifier, and 0.23 µA by the unity gain buffer. The nominal operating voltage for the C3PD chip is 1.8 V. Introducing the power pulsing scheme can set the main driving nodes of the analog front-end to a "power-off" mode, resulting in an average current consumption of only 53 nA per pixel. A delay of about 15 µs after the power enable signal has been measured (by injecting test pulses with a controlled delay after the power enable signal) to be sufficient for the circuit to be ready to detect particles, without any noticeable effect on noise. Therefore, assuming a duty cycle length of 30 µs (following a conservative approach and providing a duty cycle twice as long as the measured power-up time) over the 20 ms between subsequent bunch trains of the CLIC accelerator, the average power consumption for the matrix over the 50 Hz cycle will be $\sim$ 16 mW/cm^2. The average

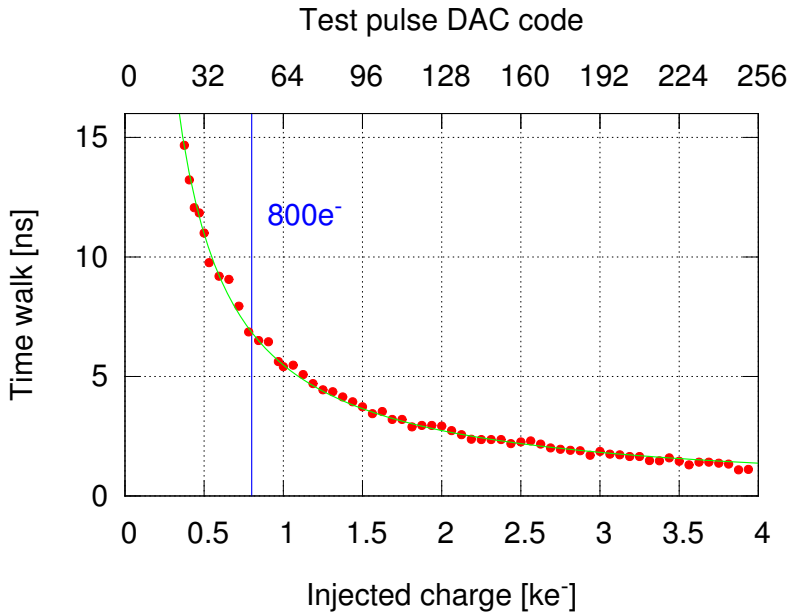


Figure 6.7 Time walk, averaged over 64 pulses, as a function of the injected test pulse DAC code and corresponding injected charge.

power consumption during the experiment conditions is dominated by the "power-off" state, and could be minimised in future versions by optimising the range of the power-off DACs. A reasonably low power consumption during the "power-on" state is required in order to match the instantaneous power consumption that can be delivered to the detector, which is foreseen to reach a few W/cm^2 [102], and also to have the possibility to operate the chip in laboratory and beam tests with continuous power and without the use of additional cooling. Additionally, in view of future HV-CMOS developments, the power consumption can be used as a reference for applications with different powering schemes.

Table 6.1 summarises the average values and standard deviations of the main pixel characteristics for all monitored pixels from four samples with standard thickness and two thinned down to 50 µm. A test pulse of 1.63 ke$^-$ (charge equivalent to the most probable energy of the photons from an ^{55}Fe source, as will be explained in Section 6.1.5) was injected for the amplitude and rise time measurements. No systematic difference has been observed between standard and thinned samples which is promising in view of assemblies with 50 µm sensor thickness, as indicated by the material budget for the CLIC vertex detector.

Simulations of the front-end were performed under the same biasing conditions and the simulated values are presented in the rightmost column of Table 6.1. The observed mismatch between the simulated and the measured rise time, can be attributed to a convolution of different factors, from which the dominant one is believed to be additional parasitic

capacitances loading the monitored outputs. The buffers which are driving the signal to the readout have a bandwidth of 150 MHz and are simulated to have a rise time of ~ 2 ns. They are therefore expected to have negligible contribution to the degradation of rise time. The measured rise time is, according to Monte Carlo simulations, close to the three-sigma value. Measured, as well as simulated values presented in Table 6.1 refer to the monitored pixels. For the regular pixels in the matrix the rise time was simulated to be $\sim 30\%$ faster. The feedback capacitance depends on the drain voltage of transistor M2, which is set by the V_{gs} of M4, the V_{ds} of M6 and the V_{gs} of M0 in Figure 5.3. Uncertainties in these values can result to an extracted C_{fb} different than the one present in the circuit. As the charge gain is inversely proportional to the feedback capacitance [20], a difference in C_{fb} can explain the discrepancy between the simulated and the measured charge gain.

Table 6.1 Pixel characteristics for monitored pixels, averaged over 6 assemblies, measured with test pulses of 1.63 ke$^-$ charge. The simulated values are shown in the rightmost column.

Parameter	**Average**	**Standard deviation**	**Simulated**
Amplitude [mV]	302	30.9	210
Noise RMS [e$^-$]	40	3.8	45
Rise time [ns]	20.8	3.75	11
Power/pixel, on state [µW]	4.8	0.41	4.6
Power/pixel, off state [µW]	0.095	0.03	0.107

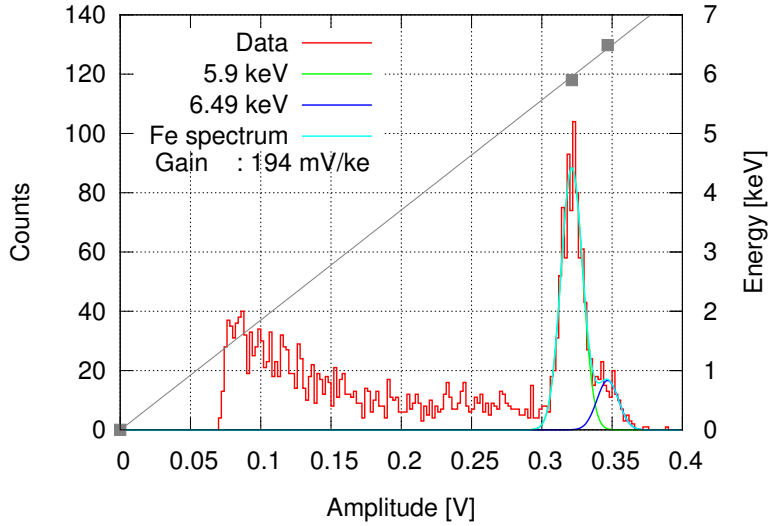
6.1.4 Measurements with a radiation source

Figure 6.8a presents the measured pulse amplitude spectrum from a ^{55}Fe source. The sum of two Gaussian distributions is fitted to the sampled amplitudes. As shown, the two peaks of the Gaussian fit correspond to the two most probable energies deposited by the photons from the ^{55}Fe source (5.9 keV and 6.49 keV). The gain of the preamplifier in the C3PD pixel is therefore ~ 190 mV/ke$^-$. A tail due to charge sharing can be seen in the measured spectrum, which is the result of measurements from only a single monitored pixel.

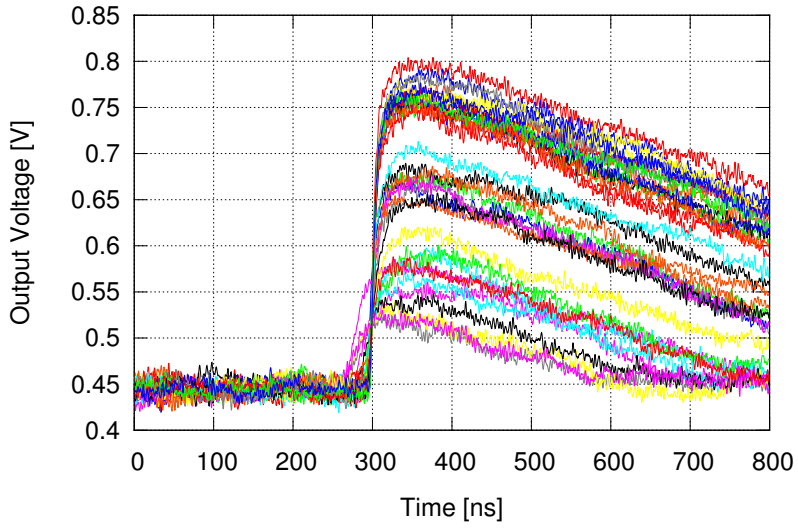
A sample of the measured output pulse shapes is presented in Figure 6.8b. The measured amplitude of these pulses was binned to create the resulting spectrum.

6.1.5 Feedback and test capacitance calculation

The results from the measurement with the ^{55}Fe source were used to calculate the values of the feedback and test pulse injection capacitances in the C3PD front-end. With a known



(a)



(b)

Figure 6.8 (a) Resulting amplitude spectrum and double Gaussian fit for one of the monitored pixels and (b) sample pulses from a ^{55}Fe source.

^{55}Fe deposited energy of 5.9 keV and electron-hole pair creation energy in silicon of 3.62 eV, we can expect a deposited charge in the detecting volume equal to 0.26 fC (or 1.63 ke$^-$). The voltage peak corresponding to this energy is at $\sim$ 320 mV (for the measured sample presented in Figure 6.8a), as taken from the mean value of the first Gaussian in Figure 6.8, which gives a charge gain of $\sim$ 190 mV/ke$^-$. From the voltage peak, we can estimate a value for the feedback capacitance:

$$C_{fb} = \frac{0.26fC}{320mV} \approx 0.81fF \tag{6.1}$$

In order to estimate the test pulse injection capacitance, C_{test}, a scan of the test pulse DAC code was performed while monitoring the pixel output (Figure 6.6). From this, the slope of the output voltage amplitude as a function of the test pulse DAC code was extracted. At the DAC code for which the measured output voltage is close to the 320 mV corresponding to the first peak of the ^{55}Fe source spectrum, one can assume that a charge of 1.63 ke$^-$ is injected at the input of the preamplifier. Once this DAC code was measured, it was possible to monitor the dedicated pixel where the injected test pulse is output (see Section 5.2.2) to determine the amplitude of the injected test pulse. It was observed that an injected test pulse of 370 mV results in an output amplitude close to the one measured during tests with the ^{55}Fe source. It is therefore a good approximation that a 370 mV test pulse will inject 1.63 ke$^-$, resulting in an injection capacitance of $\sim$ 0.70 fF.

The above procedure was followed for several other samples in order to characterise their performance with the ^{55}Fe source and estimate their feedback and test capacitances. The results give average values of $C_{fb} = 0.83$ fF $\pm 15\%$ and $C_{test} = 0.70$ fF $\pm 2\%$, which are in good agreement with the simulated post-layout extracted values (1.2 fF for C_{fb} and 0.8 fF for C_{test}). The analysis followed for estimating the C_{fb} assumes an infinite open loop gain and no continuous reset. As calculated, this assumption leads to a feedback capacitance overestimated by $\sim$ 7.5%, mainly due to the continuous reset that is present in the circuit (provided by transistor M6, as described in section 5.2.1).

6.1.6 Samples with higher substrate resistivity

Samples with higher substrate resistivity ($\sim$ 80, 200 and 1000 Ωcm) were received after the samples from the first production (with standard substrate resistivity) were characterised. Since the number of received samples with higher substrate resistivity was limited, they were mainly reserved for use in capacitively coupled assemblies. The standalone test was therefore based on results with standard resistivity chips.

One of the higher resistivity chips (1 kΩcm) was wire-bonded on a chip-board for standalone measurements, to confirm that the electrical performance is similar to the samples with standard substrate resistivity. A photo of the wire-bonded chip is shown in Figure 6.9.

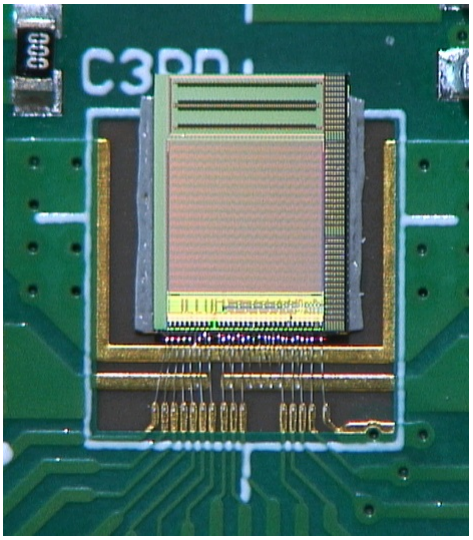


Figure 6.9 High resistivity C3PD chip mounted and wire-bonded on the PCB.

As mentioned in Section 6.1.3, the DAC in the C3PD analog periphery for biasing the feedback transistor in the front-end was measured to not have enough dynamic range for the tests that were performed. Thus, before submitting the design for production with higher resistivity wafers, the range of this DAC was increased in order to not need to use an externally provided bias voltage for the feedback transistor. The measurement plotted in Figure 6.10 confirms that the range of the feedback biasing DAC has been increased to 720 mV (compared to the 550 mV for the first production).

Table 6.2 summarises the measured parameters for the high resistivity sample and compares to the ones for the 20 Ωcm chips (values for the 20 Ωcm chips are averaged over six measured samples). The difference in gain can be explained due to the different values of the feedback capacitances in the two production lots. Although only this one sample was calibrated with a ^{55}Fe source, this difference is consistent with the measured performance of other high resistivity C3PD chips in capacitively coupled assemblies.

As described in Section 5.3, a modification was done in the metal contact of the High-Voltage guard-ring around the pixel in order to allow for a higher reverse bias before the diode breaks down. However, this modification was not effective, most likely due to the fact that the substrate contacts in the periphery blocks follow the layout of the first version and the breakdown happens close to these diodes. The maximum reverse bias that can be applied is therefore similar to the one for the standard resistivity C3PD samples.

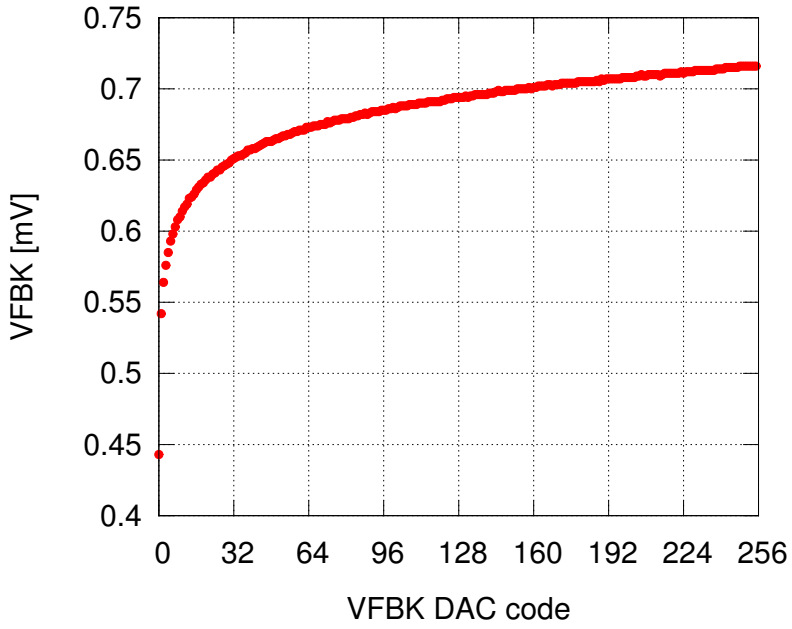


Figure 6.10 Bias voltage of the feedback transistor as a function of the DAC code.

Table 6.2 Pixel characteristics for the measured higher resistivity C3PD chip, compared to the standard resistivity samples.

Parameter	**Standard resistivity**	**High resistivity**
Output voltage (^{55}Fe peak) [mV]	302	276
Noise RMS [e$^-$]	40	38
Gain [mv/ke$^-$]	190	166
Rise time [ns]	20.8	21
Leakage current at -60 V (full chip) [nA]	40	30
Breakdown voltage [V]	-69	-72
C_{fb} [fF]	0.83 $\pm$15%	0.94
C_{test} [fF]	0.70 $\pm$2%	0.58

The measured pulse amplitude spectrum from a ^{55}Fe source for the high resistivity C3PD sample is plotted in Figure 6.11.

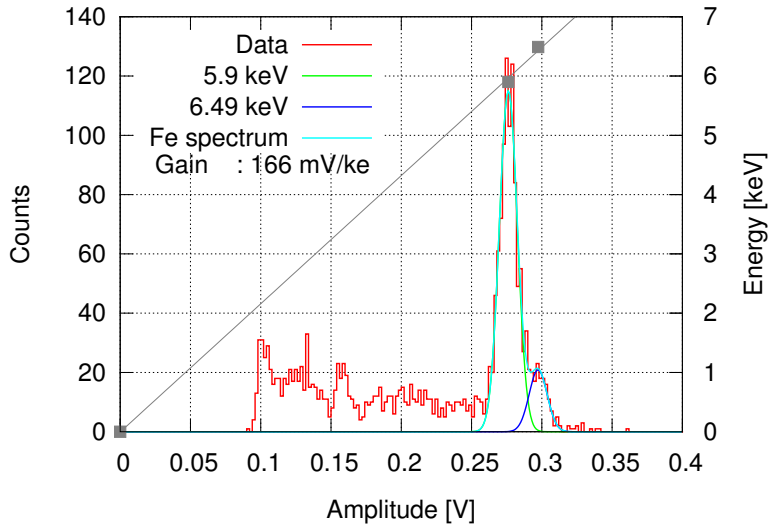


Figure 6.11 Resulting amplitude spectrum and double Gaussian fit from a ^{55}Fe source, for one of the monitored pixels of a high resistivity C3PD chip.

6.2 Characterisation of capacitively coupled assemblies

Once produced, the CLICpix2 readout chip was first tested with electrical test pulses, without sensor. Following the successful first tests with bare readout chips, capacitively coupled assemblies with the C3PD HV-CMOS sensor chip were produced in order to study the effects of coupling the two chips together.

6.2.1 Measurement setup

The measurement setup for the capacitively coupled assemblies is based on the Control and Readout Inner tracking BOard (CaRIBOu) readout system [103]. This versatile readout system was developed to support multiple applications with different devices. It is based on the ZC-706 evaluation kit [104] which features an ARM processor and a Kintex-7 FPGA. The Control and Readout (CaR) interface board, is connected to the evaluation kit and is responsible for providing power supplies, communication standards and other signals to the ASICs [105]. The sensor and readout chips are glued together and mounted on a custom designed PCB, which allows a two-sided wire-bonding (for more details, see Appendix A.2). A photo of a capacitively coupled assembly is shown in Figure 6.12, and the measurement setup in Figure 6.13.

The capacitively coupled assemblies were produced at the University of Geneva using an SET Accura 100 flip-chip machine.

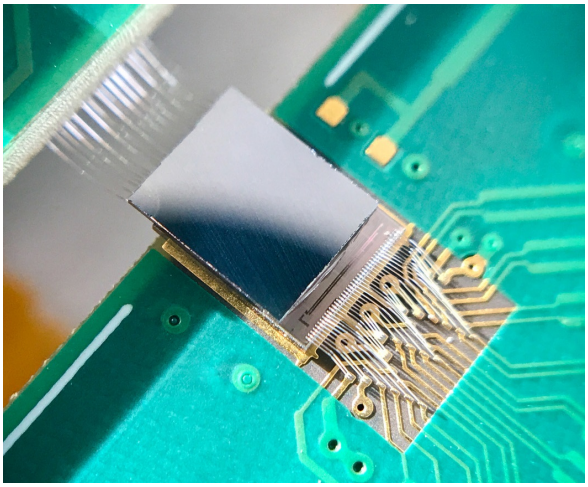


Figure 6.12 Capacitively coupled assembly of C3PD (top) and CLICpix2 (bottom), wire bonded on the PCB.

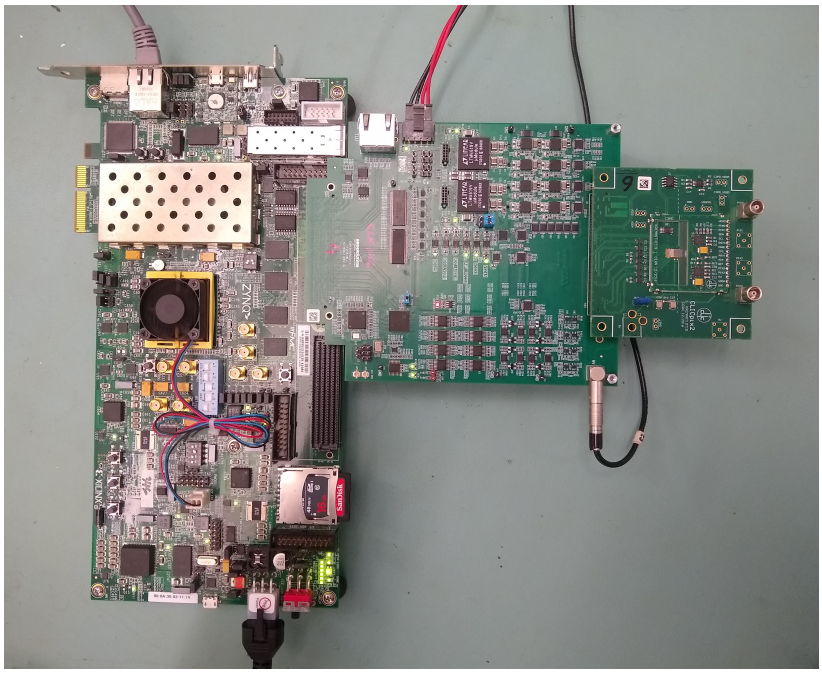


Figure 6.13 Photo of the CaRIBOu readout system for testing capacitively coupled assemblies with the CLICpix2 and C3PD chips. From left to right: evaluation kit, CaR board, chip-board with CLICpix2/C3PD assembly mounted on it.

6.2.2 I-V characteristic

The initial step after the first capacitively coupled assembly was wire-bonded on the PCB was to measure the sensor leakage current as a function of the applied reverse bias in order to confirm that glueing the two chips together does not affect the sensor's I-V characteristic. As expected, the sensor shows a very similar performance compared to the ones that were measured in a standalone test, with the breakdown occurring close to -70 V and the leakage current for the nominal bias (-60 V) being ~ 40 nA. Figure 6.14 presents the scan of the leakage current as a function of the reverse high voltage bias for one sensor in a capacitively coupled assembly, compared to two bare sensor chips (one 50 µm and one 250 µm thick). The thickness of the C3PD sensor chip used in the capacitively coupled assembly is 250 µm.

Following the I-V measurement, the noise at the output of the C3PD amplifier was scanned as a function of the applied reverse bias, measuring the output of one of the monitored pixels. As presented in Figure 6.15, the noise is suppressed when applying a higher reverse bias, due to the fact that the depletion depth becomes larger and thus the sensor capacitance is minimised.

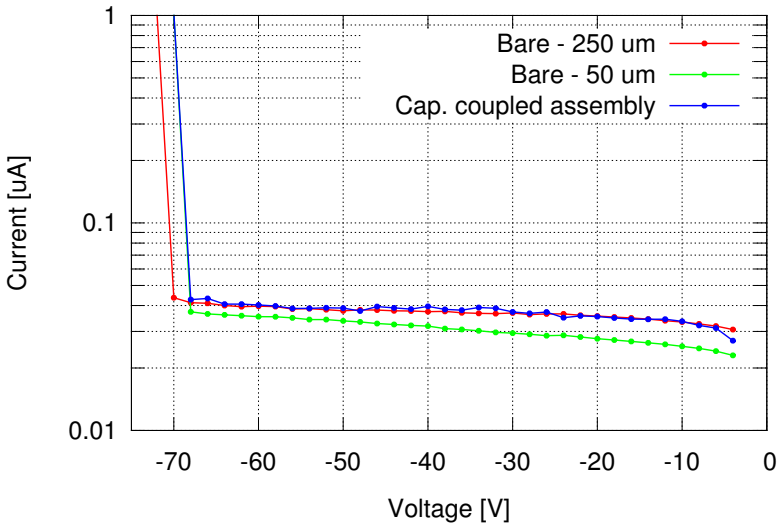


Figure 6.14 I-V curve for a C3PD chip in a capacitively coupled assembly, compared to the I-V curves for two bare chips: one 250 µm thick and one thinned down to 50 µm.

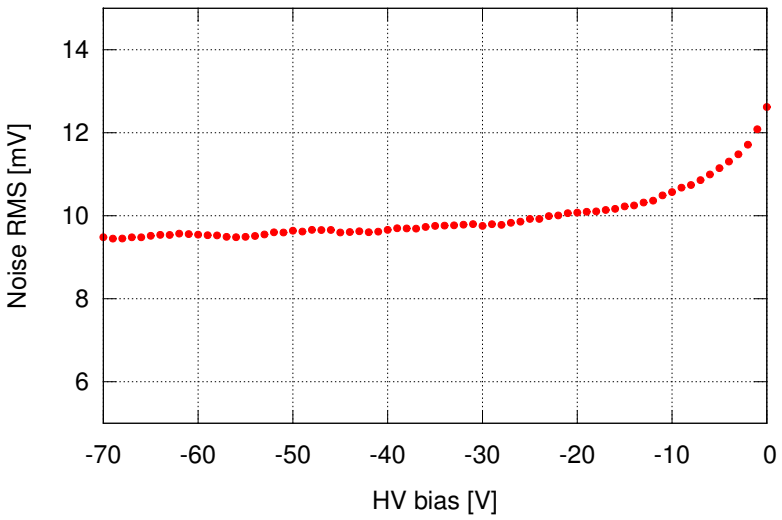
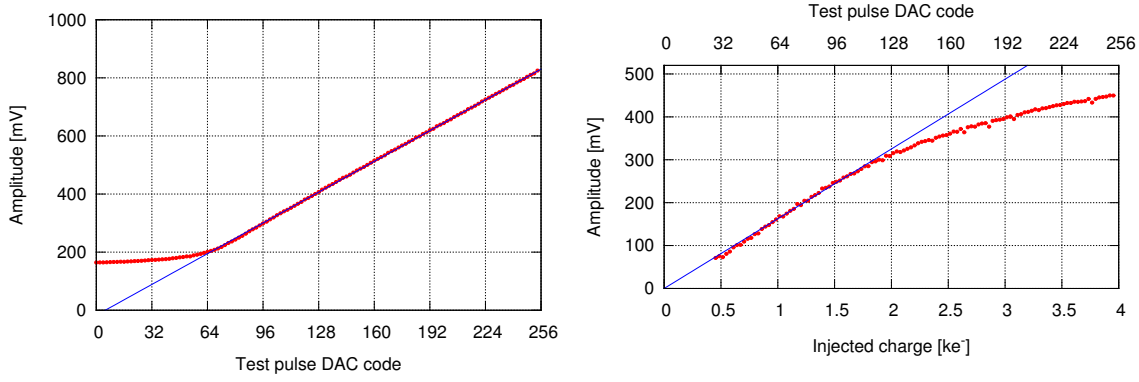


Figure 6.15 Noise at the amplifier output as a function of the high voltage bias. From [74].

6.2.3 Calibration of the sensor chip with test pulses

Before acquiring data from the CLICpix2 readout chip, the C3PD sensor was measured to confirm that the additional capacitance at the output of the pixels does not affect the performance of the circuit. The additional capacitance is estimated to be ~ 20 fF (including the coupling capacitance of the glue and the input capacitance of the CLICpix2 front-end).

The performance of the amplifier was measured using two pixels in the monitored cluster. First, the output of the pixel with direct test pulse monitoring was measured as a function of the injected test pulse DAC code. Then, the amplitude at the preamplifier output was scanned, again as a function of the injected test pulse DAC code. The measured voltage amplitudes for the test pulse and preamplifier output are presented in Figures 6.16a and 6.16b respectively. The non-linearity observed in the lower DAC codes of the test pulse measurement results from the buffer in the C3PD analog periphery, which is used to drive the signal to the wire-bond pad (an effect which has been confirmed with simulations). The injected charge in Figure 6.16b is calculated based on the design value of 0.8 fF for the test pulse injection capacitance in the C3PD front-end.



(a) (b)

Figure 6.16 (a) Injected test pulse amplitude and (b) output amplitude (averaged over 16 samples) as a function of the test pulse DAC code. From [74].

To confirm that a fast rise time is maintained after glueing the two chips together, the rise time was measured for different input charges injected using the internal test pulse. As presented in Figure 6.17, the rise time is not compromised after producing the capacitively coupled assembly. In addition, the slow return to baseline helps to ensure that the charge will not be removed before being integrated in the CLICpix2 front-end.

The process described in Section 6.1.3 for finding the optimal operating point for the C3PD front-end was repeated for the sensor chip in the capacitively coupled assembly. The biasing point of different nodes in the front-end was scanned in order to find the operating

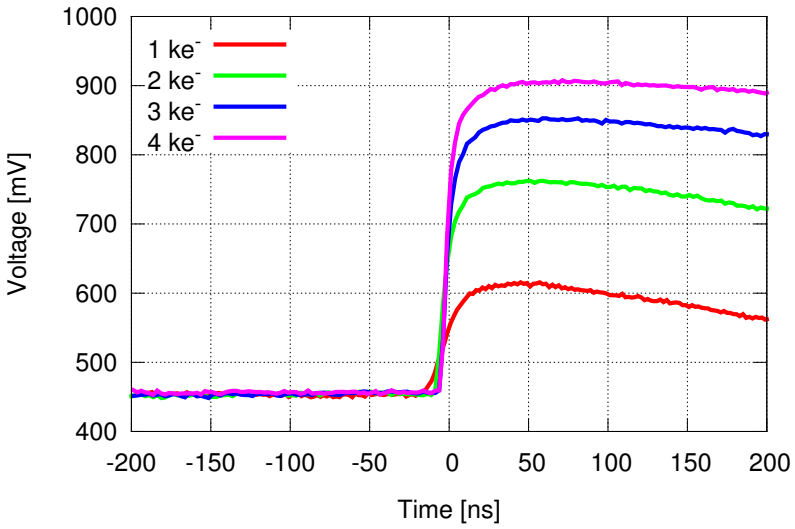


Figure 6.17 Output pulses (averaged over 16 samples) for different charge injected using test pulse. From [74].

point with the best compromise in terms of Signal-to-Noise ratio, signal rise time and power consumption. Compared to Section 6.1.3, additional load is connected at the output of the C3PD pixel, from having the sensor chip capacitively coupled to the readout ASIC. Figure 6.18 presents some example plots of the DAC scans that were performed in order to optimise the C3PD operating point for the capacitively coupled assembly. The plots presented concern the parameters of the main biasing nodes of the circuit (preamplifier, unity gain buffer, feedback transistor) and were used to decide the operating point for the C3PD chip in capacitively coupled assemblies.

The measured characteristics of the C3PD pixel (output amplitude, noise and rise time), for the selected operating point, are presented in Table 6.3. Test pulses with a charge equivalent to the most probable energy of the photons from an ^{55}Fe source (1.63 ke^{-}) were injected for the presented measurements. The output amplitude and the rise time were measured as the mean value of 16 samples, while the RMS noise is the mean RMS value over 10 seconds of sampling with the oscilloscope. The power consumption is similar to the one measured for bare chips, resulting to an average of $\sim$ 16 mW/cm^2 over the 50 Hz duty cycle of the CLIC collider, as described in Section 6.1.3.

Compared to the bare chips, the main difference observed was in the noise performance of the front-end when using the two chips together. This noise could possibly be a result of coupling from the lines in the CLICpix2 chip to the C3PD matrix. However, after optimising the operating point, the output noise can be adjusted to comparable levels to those observed for bare chips. Other characteristics of the front-end, such as gain, rise time and power

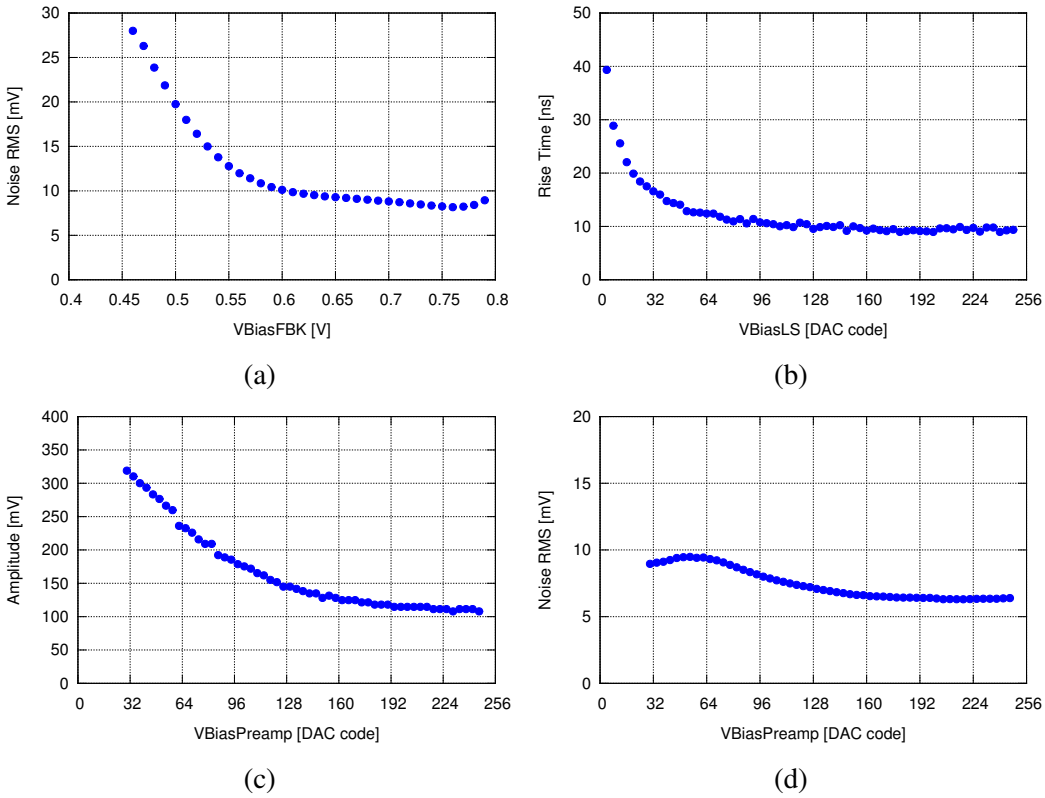


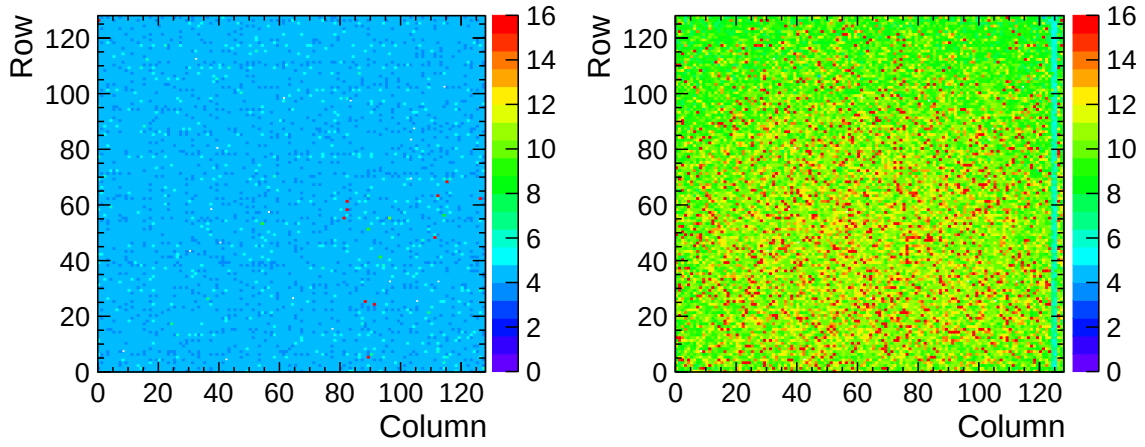
Figure 6.18 (a) Noise as a function of the feedback bias, (b) rise time as a function of the unity gain buffer bias, (c) output amplitude and (d) noise as a function of the charge sensitive amplifier bias for the measured C3PD chip. From [74].

consumption are within the variations observed during the characterisation of bare C3PD chips.

Table 6.3 Pixel characteristics, averaged for all monitored pixels of the measured assembly, measured with test pulses of 1.63 ke$^-$ (charge equivalent to the most probable energy of the photons from an ^{55}Fe source).

Parameter	Average	Standard deviation
Amplitude [mV]	278	6.44
Gain [mV/ke$^-$]	170	3.9
Noise RMS [e$^-$]	41	8.2
SNR	42	7.4
Rise time [ns]	17.6	0.8

During the first measurements with capacitively coupled assemblies, it was observed that the noise in the CLICpix2 front-end is increased by a factor of ~ 2 when the C3PD chip is powered on. This is expected due to the fact that the noise at the output of the C3PD chip is coupled to the CLICpix2 input. In Figure 6.19, the noise in the CLICpix2 front-end is presented, before and after powering up the C3PD chip. The measurement was performed after equalising the threshold over the CLICpix2 pixel matrix.



(a) (b)

Figure 6.19 Noise width measured (in threshold DAC LSBs) in the CLICpix2 chip, with the C3PD sensor chip powered off (a) and on (b). From [106].

6.2.4 Test pulses with the readout chip

After the operating point for the C3PD sensor chip was selected by studying the signal at the outputs of the monitored pixels, test pulses were injected into the full C3PD pixel matrix and read out by the CLICpix2 readout chip. Such measurements can provide information on the strength of the coupling between the two chips, and therefore the uniformity of the glue deposition.

As presented in Figure 6.20, variations have been observed in different assemblies. Here, the measured ToT in the CLICpix2 was measured as the average ToT for 200 test pulses with fixed amplitude injected in the C3PD front-end. The inhomogeneities observed in some of the assemblies indicate that the gluing process needs to be further optimised to achieve a strong and uniform coupling along the full pixel matrix area.

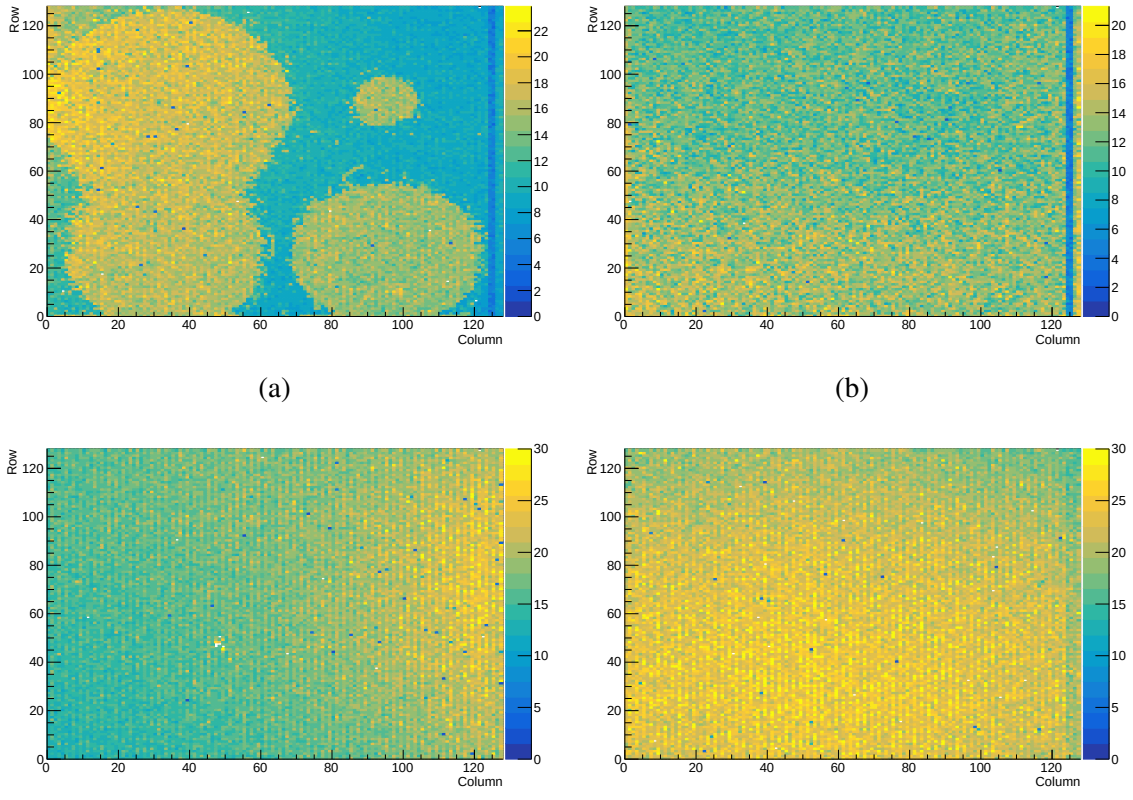


Figure 6.20 Hit maps acquired with the CLICpix2 readout chip, after injecting test pulses in the C3PD front-end. Figures (a) and (b) present two capacitively coupled assemblies with 20 Ωcm C3PD sensor chips and Figures (c) and (d) present two assemblies with 1 kΩcm C3PD chips.

In addition, a systematic difference between the response of pixels in the odd and even columns can be observed in the plots in Figure 6.20. This can be attributed to the fact that a double column structure has been used to lay out the pixels in the C3PD chip, as presented in Figure 5.4, with a slightly different layout for the pixels in the odd and even columns. A similar double-pixel approach has been used in the CLICpix2 matrix.

6.2.5 Coupling capacitance calculation

Following destructive cross-section measurements on two mechanical samples, the pad-to-pad distance was measured to be ~ 3 µm, largely dominated by the passivation layers of the two chips. A photo with the cross-section of one of the mechanical samples is presented in Figure 6.21. The simulated value for the coupling (glue) capacitance for this distance was ~ 3.5 fF [95].

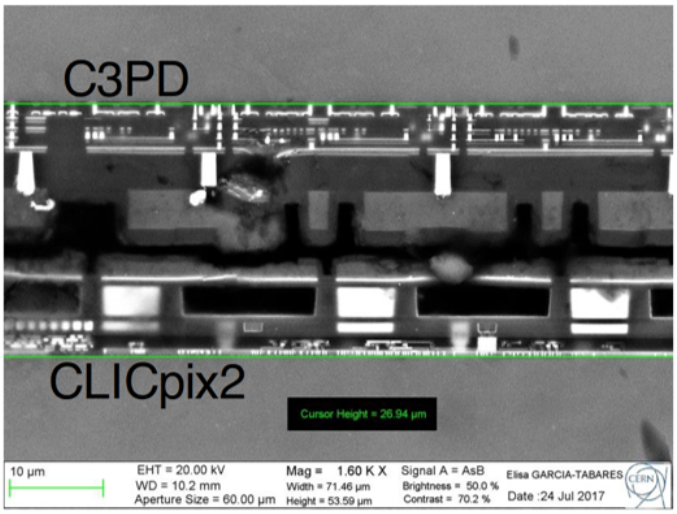


Figure 6.21 Cross-section of a capacitively coupled assembly with the CLICpix2 (bottom) and C3PD (top) chips (© CERN).

The special C3PD pixel, where the injected test pulse signal is connected directly to the coupling pad, was used to measure the glue capacitance and compare it with the simulated value. First, the ToT was measured in CLICpix2 as a function of the injected pulse amplitude. The slope of ToT as a function of the injected charge is given by Equation 6.2, where c_1 is the slope of ToT as a function of the injected pulse amplitude in the linear region of the ToT measurement.

$$ToT = c_1 \cdot V_{inj} = c_1 \cdot \frac{Q_{inj}}{C_{coupl}} \tag{6.2}$$

Next, the ToT of the same CLICpix2 pixel was measured again, this time with the internal CLICpix2 test pulse injection. The ToT as a function of the injected charge is now given by Equation 6.3, where C_{test} is the test pulse injection capacitor in the CLICpix2 front-end with a design value of 10 fF.

$$ToT = c_2 \cdot V_{inj} = c_2 \cdot \frac{Q_{inj}}{C_{test}} \tag{6.3}$$

Combining Equations 6.2 and 6.3, gives a value for the glue capacitance between the sensor and readout chips. The extracted values for different assemblies are presented in Table 6.4. The variations observed in glue uniformity and alignment can explain the variations in the glue capacitance. For assemblies where a good and uniform coupling is observed with C3PD pulses, the measured value of the glue capacitance is close to the simulated one. However, this is not always the case as the C3PD pixel with direct test pulse monitoring is located at one edge of the matrix, a region where a weaker coupling is more likely due to the glue deposition.

Table 6.4 Glue capacitance for different CLICpix2 and C3PD assemblies, extracted from ToT measurements in the CLICpix2 readout chip.

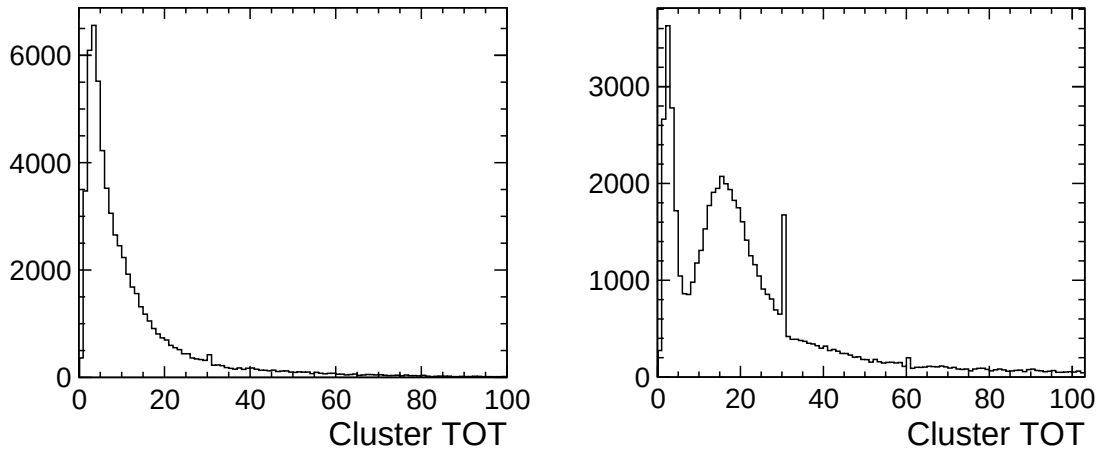
Assembly	**C3PD substrate resistivity [Ωcm]**	**C_{glue} [fF]**
1	20	3.66
6	20	1.43
7	20	2.95
9	1000	2.72
10	1000	2.63
17	200	3.20

6.2.6 Radiation sources

Due to the flip-chip assembly, it was not possible to measure the chips with the ^{55}Fe source. The C3PD sensor chip is flipped and glued on the CLICpix2 readout chip. For the standard thickness of the sensor chip (250 µm), more than 200 µm of silicon would prevent the photons from the ^{55}Fe source from penetrating through the back side of the sensor into the (around 10 µm deep) depletion region. It was therefore not feasible to illuminate the pixels with a ^{55}Fe source with this setup.

A measurement with a ^{90}Sr source was performed. Figure 6.22a presents the resulting pulse amplitude spectrum measured for an assembly with a standard resistivity (20 Ωcm)

C3PD sensor, and Figure 6.22b the same spectrum for an assembly with 1000 Ωcm sensor. This measurement is not conclusive due to charge sharing events and the statistical fluctuations of the Landau distribution. However, comparing the two resulting spectra indicates that the spectrum peak is shifted to the right and can be clearly observed for the higher resistivity chip, while for the lower resistivity chip the spectrum peak is not observed in the plot. This observation is in agreement with the expected larger depleted volume (and thus larger portion of the generated charge collected by drift) for higher substrate resistivity.



(a) (b)

Figure 6.22 Resulting amplitude spectrum from a ^{90}Sr source, for a capacitively coupled assembly with (a) a 20 Ωcm and (b) a 1000 Ωcm C3PD sensor. The peaks observed for the ToT value of 30 are resulting from single cluster hits where the ToT counter has saturated.

6.2.7 Beam tests

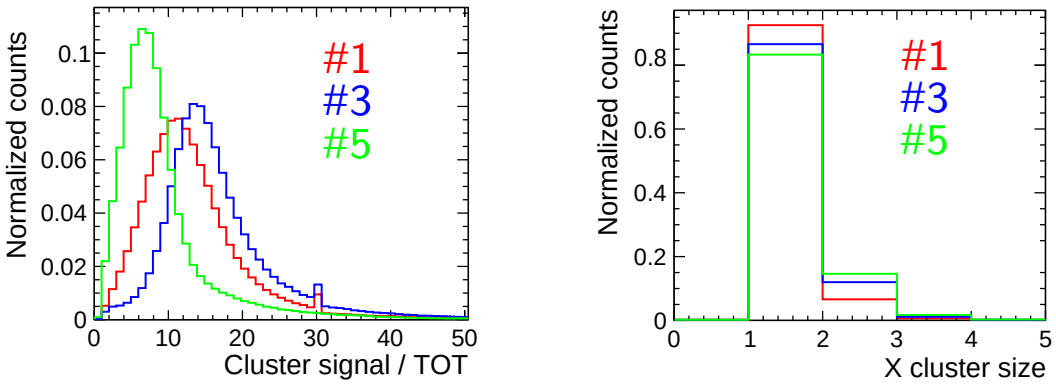
The CLICdp Timepix3 telescope, operated in the CERN SPS beamline, was used for taking data with the CLICpix2 and C3PD chips in capacitively coupled assemblies. The telescope consists of seven planes of Timepix3 assemblies with planar sensors for reference tracking. The Timepix3 chip [26] features square pixels with 55 µm pitch. To optimise the charge sharing, and therefore the spatial resolution, the telescope planes are slightly rotated. The resulting spatial resolution on the Device Under Test (DUT) is ~ 2 µm. A time-tagging with 1.56 ns binning is performed in the Timepix3 pixels, resulting to a timing resolution of ~ 1 ns on the DUT. The DUT can be rotated in order to perform measurements with different angles. A photo of the Timepix3 telescope with a CLICpix2 / C3PD capacitively coupled assembly is presented in Figure 6.23.

Figure 6.23 Measurement setup using the CLICdp Timepix3 telescope in the CERN SPS beamline. The DUT is shown in the middle, with four Timepix3 planes on the left and three on the right (© CERN).

The measured cluster signal and cluster size are presented in Figures 6.24a and 6.24b respectively. Each measurement is presented for three different assemblies (all of which include sensor chips with the standard substrate resistivity). As expected from the variations in the glue uniformity, the cluster signal measured with the readout chip varies from assembly to assembly. The resulting position resolution is ~ 7 µm, with limited charge sharing as mostly single pixel hits are observed.

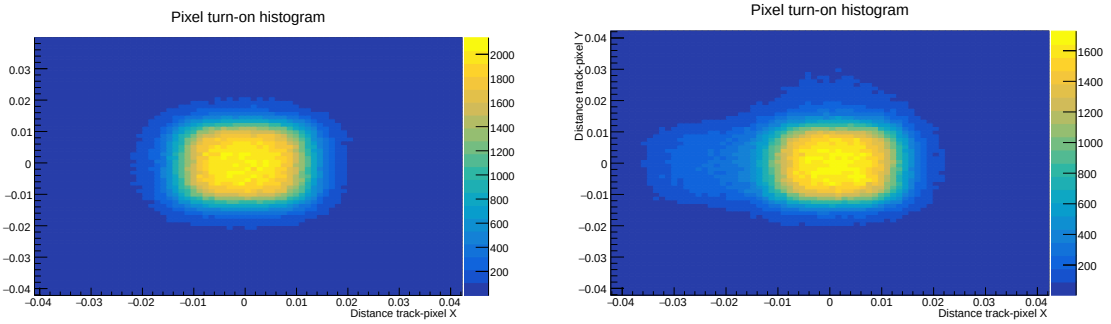
Further, cross-talk was observed between neighbouring pixels in some of the assemblies, which can be explained due to asymmetric coupling. As presented in Figure 6.25, while some assemblies show a clean coupling from the C3PD pixel to the corresponding CLICpix2 pixel (Figure 6.25a), in other assemblies a coupling to neighbouring pixels was observed as well (Figure 6.25b). This is attributed to possible slight misalignments during the flip-chip assembly.

The ToA counter in the CLICpix2 pixel is 8-bit long with 10 ns time-tagging. The time difference between the reconstructed hit and the track before and after using the ToT information to correct for time walk are presented in Figure 6.26a. As shown, the width of the Gaussian fit of the time residuals is reduced from ~ 9 ns to 7 ns after correcting for time walk. The time walk in the capacitively coupled assembly used for this measurement is plotted in Figure 6.26b.



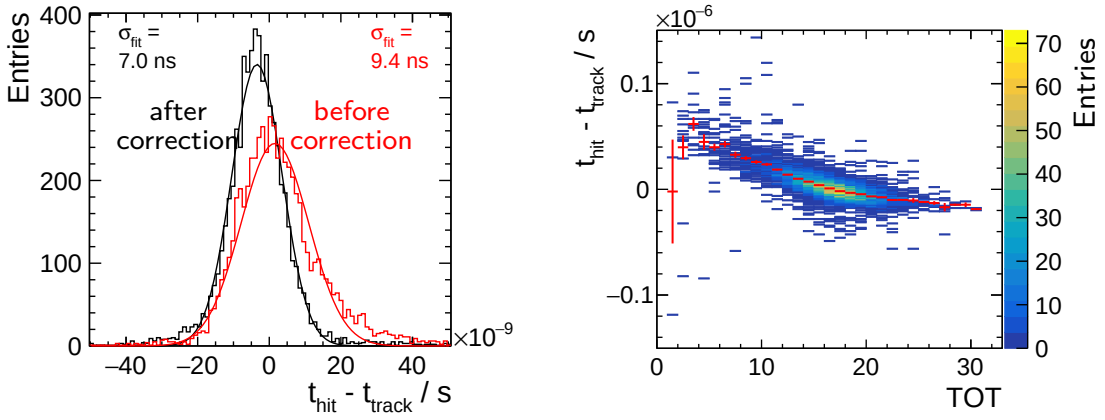
(a) (b)

Figure 6.24 (a) Cluster signal and (b) cluster size as measured in beam tests with three different capacitively coupled assemblies. From [91].



(a) (b)

Figure 6.25 A histogram for the CLICpix2 pixel response, produced by scanning the tracks over the pixel and plotting the pixel response. (a) Assembly with good flip-chip alignment and (b) slightly misaligned assembly. From [106].



(a) (b)

Figure 6.26 (a) Time difference between the reconstructed hit and the track and (b) ToT information used to correct for the time walk effect. From [91].

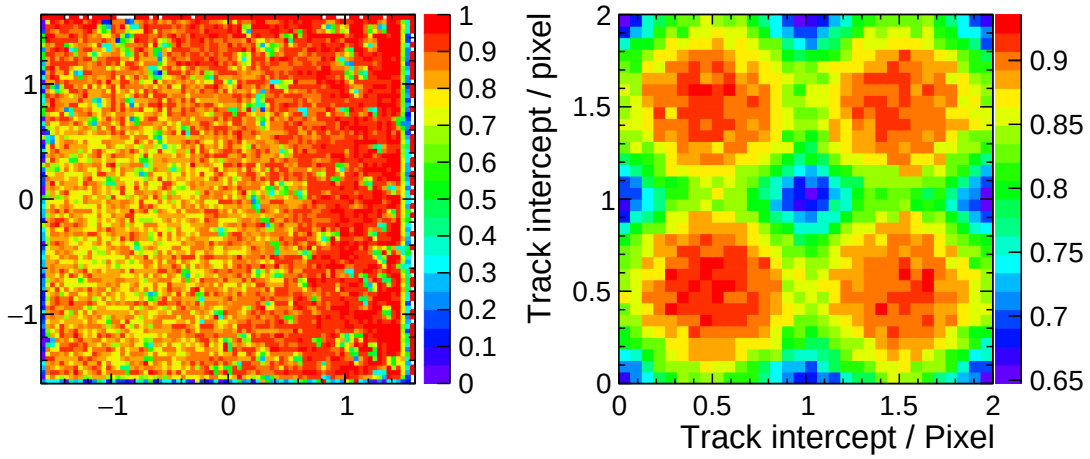
The time resolution resulting from beam tests with the CLICpix2 readout chip with planar sensors bump-bonded on it was ~ 4 ns. Assuming that the contribution of the planar, fully depleted, sensor to the time resolution is negligible, we can then extrapolate the contribution of the C3PD HV-CMOS sensor chip to the degradation of the time resolution. Given the CLICpix2 time resolution $\sigma_{CP2} = 4$ ns and the time resolution of the capacitively coupled assembly $\sigma_{CC} = 7$ ns, the contribution of C3PD, σ_{C3PD}, is given by Equation 6.4:

$$\sigma_{C3PD} = \sqrt{\sigma_{CC}^2 - \sigma_{CP2}^2} \tag{6.4}$$

Therefore, the C3PD chip contributes to the resulting time resolution by 5.7 ns. The time resolution of the system could be further optimised by studying the power allocated to the C3PD and CLICpix2 front-ends and finding the best compromise in order to improve the timing of the complete detector chain.

Regarding the efficiency of the assembly, Figure 6.27a presents the efficiency across the full pixel matrix area of one capacitively coupled assembly and Figure 6.27b presents the same efficiency folded into a 2×2 pixel array. The overall efficiency of the assembly was measured to be $\sim 85\%$. As illustrated in Figure 6.27b, most of the losses come from the regions between the pixels. This indicates that the coupled signal might not be strong enough and that further optimisation of the signal transfer chain would be needed for producing fully efficient assemblies. The glueing process, the increased noise in the CLICpix2 front-end after powering on the C3PD chip which leads to a need for higher threshold in the CLICpix2

pixel, as well as uncertainties in design parameters such as the dielectric constant of the glue can lead to a reduced efficiency.



(a) (b)

Figure 6.27 Efficiency measurement (a) across the matrix and (b) folded into a 2×2 pixel array. From [106].

6.3 Summary

The C3PD front-end performance was first studied in standalone mode using a setup with bare C3PD sensor chips, before producing capacitively coupled assemblies with the readout chip. The measurement results with bare chips show an average gain of 190 mV/ke$^-$ with an RMS noise of 40 e$^-$. A pulse rise time of the order of 20 ns was measured at the output of the pixel. These results match the requirements for the design of the C3PD prototype. The power consumption per pixel is 4.8 µW and, taking into account the applied power pulsing scheme, the average power consumption for the matrix over the 50 Hz cycle is $\sim$ 16.4 mW/cm^2.

Samples of the C3PD chip have also been thinned down to 50 µm, and have been successfully tested along with the standard 250 µm thick chips with no observed changes in their performance. All measured samples have shown only small variations between devices in terms of rise time, power consumption, Signal-to-Noise ratio and leakage current.

Following the first production, with the standard substrate resistivity ($\sim$ 20 Ωcm), the C3PD chip has been produced on wafers with higher substrate resistivity ($\sim$ 80, 200 and 1000 Ωcm). Due to the limited number of higher resistivity samples received, the test was limited to one bare chip, while other chips were reserved for producing capacitively coupled assemblies.

Capacitively coupled assemblies were tested over laboratory measurements and beam tests. The main limitation in the performance of the capacitively coupled assemblies seems to be the uniformity of the glue deposition along the surface of the two chips. Variations (either gradient or only partial glue deposition) have been observed, indicating that the gluing process needs to be further optimised. Nevertheless, the assemblies were successfully operated and used for particle detection both in laboratory measurements with radiation sources and in beam tests.

Regarding the requirements for the CLIC vertex detector, the time tagging resolution of ≤ 10 ns is met and the successful testing of 50 µm thick sensor chips is promising in view of the required material budget. Of course, additional mechanical constraints will need to be addressed for the production of capacitively coupled assemblies with 50 µm sensor and 50 µm readout chip. The resulting average power consumption of the C3PD chip provides enough margin for the readout chip in view of the target of 50 mW/cm^2 total average power consumption of the capacitively coupled assemblies. The detecting efficiency of the assemblies should be improved by further optimising the signal transfer chain and studying the properties of the dielectric. Last, based on this study of capacitively coupled assemblies, the most challenging requirement is the aim for a 3 µm spatial resolution. Smaller pixel area or sensors with higher charge sharing should be studied in order to meet this requirement.

Chapter 7

The CLICTD chip design

In this chapter, the design of a monolithic detector chip for the CLIC silicon tracker is presented. The CLIC Tracker Detector (CLICTD) prototype chip, designed following the requirements presented in Section 4.2, features a matrix of 16×128 elongated pixels of 300×30 µm^2, for a total sensitive area of 4.8×3.84 mm^2. As will be described in the coming sections, each pixel includes 8 collection diodes, spaced by 37.5 µm in the long dimension, in order to maintain a fast charge collection. Although the design of this chip was motivated by the studies for the CLIC silicon tracker and followed the above-mentioned specifications, it is expected to serve as a test vehicle for other detector applications that could benefit from the features of the selected process technology and the architecture that will be described in the following pages. Parts of this chapter have also been covered by the author in [107] and are quoted verbatim.

7.1 The selected process

The process selected for the design of the CLICTD prototype chip is the 180 nm CMOS imaging process with a High-Resistivity (HR) epitaxial layer, described in details in Section 3.3.4. The main motivations for selecting this process for a detector chip were the possibility to have on-pixel CMOS logic, the lower cost and material budget (compared to hybrid solutions) and the small collection electrode.

Thanks to the deep P-well offered by the process, the on-pixel digital logic can be isolated from the collection electrode. The use of CMOS digital logic in the sensitive area is therefore possible without injecting noise in the collection electrode.

Choosing a monolithic technology over a hybrid (or capacitively coupled) was based on the requirements for this application. With a monolithic process, the material budget can be easily met as samples from different chips in this same process have been tested with their

bulk thinned down to ~ 50 µm. In addition, it will be a more cost effective way to cover the total sensor area of above 100 m^2 in the CLIC silicon tracker.

In the selected process, a tiny collection electrode (with a diameter of 2 µm) is used for collecting the signal. The small volume of the collection electrode suggests a very small detector capacitance (a few fF), which minimises the noise in the front-end. The process is being prototyped in the context of particle detector applications and modifications are studied in order to optimise the speed of the charge collection and its radiation hardness [108]. A modification of this process, presented in Figure 7.1, includes an additional N-type implant that allows for a full lateral depletion under the deep P-well [109].

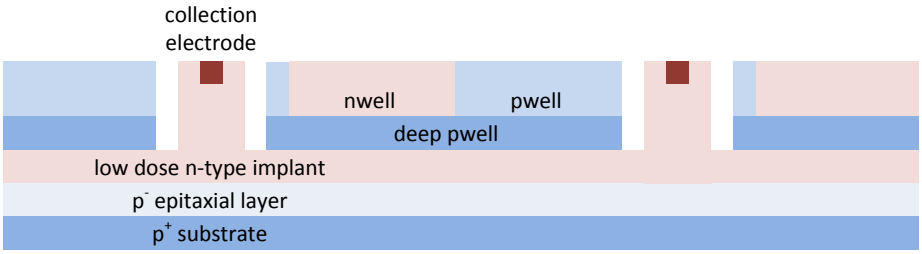


Figure 7.1 Process cross-section - continuous N-implant (not to scale).

Although this process modification results in a faster signal collection compared to the standard process, the signal collection for particles that hit between two neighbouring diodes has been simulated to remain limiting in view of the required time-stamping of 10 ns, for pixel pitches longer than 30 µm. Thus, a further modification of the process was developed following TCAD simulations, where the N-implant is segmented between neighbouring diodes [110]. A cross-section of this process modification is presented in Figure 7.2. This gap in the N-implant increases the electric field from the edge of the pixel to the diode, forcing the collected charge to drift towards the electrode. On the other hand, the charge sharing and, consequently, the spatial resolution are expected to be reduced due to the fact that charges generated between two pixels are more likely to drift quickly to the closest electrode.

For the CLICTD chip, the N-implant was segmented only along the long pixel dimension, in order to enhance the timing performance within the detecting channel. The N-implant was not segmented between adjacent detecting cells, in order to maintain the benefits from the charge sharing. The top view of the N-implant for three channels in the CLICTD pixel matrix is illustrated in Figure 7.3.

Selecting between the two process options requires a compromise between charge collection time and spatial resolution. In order to study these effects and better evaluate the process options, samples of the CLICTD prototype were produced on wafers with both process

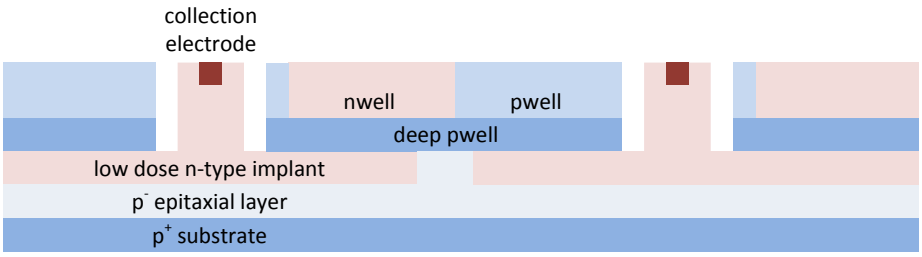


Figure 7.2 Process cross-section - gap in N-implant (not to scale).

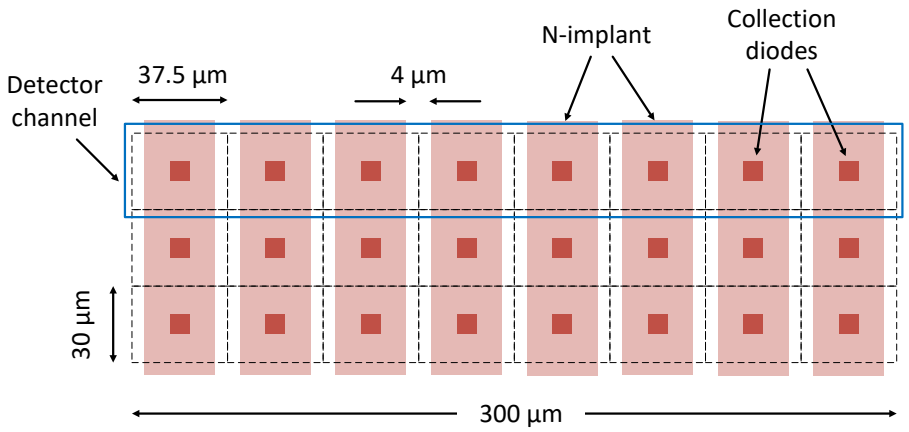


Figure 7.3 Top view of the segmentation of the deep N-implant in the CLICTD pixel matrix (not to scale).

variants. This study will not only stimulate the process selection for a future successor of the chip, but will also provide input to other applications where a similar design approach is followed.

7.2 The CLICTD detector channel

The CLICTD detector channel is an elongated pixel of 300×30 µm^2. Based on simulations and measurements with chips produced in the same process, keeping a 30 µm pitch in the transverse plane is sufficient for achieving the required single point resolution of 7 µm [111]. In the long dimension, the size of the pixel is constrained to $1 - 10$ mm, mainly by the expected hit rate. The length of 300 µm was selected for the prototype based on the area available to place and route the on-pixel digital logic. 8 front-ends are placed in each detecting cell, with a spacing of 37.5 µm between neighbouring collection diodes in the long direction. This segmentation is required in order to maintain a fast charge collection.

7.2.1 Analog front-end

In the analog part, the CLICTD detecting cell is segmented in eight front-ends, each one comprising the collecting diode, a level shifter, a voltage amplifier, a discriminator and a 3-bit DAC used for local threshold tuning. As illustrated in Figure 7.4, the pitch of the collecting diodes is 30 µm in the transverse plane and 37.5 µm pitch in the long direction. The 37.5 µm pitch in the long direction has been simulated to allow for a prompt charge collection without compromising the timing performance of the chip.

The charge is collected in an octagonal N-well diode with a diameter of 2 µm. A reset transistor provides a continuous reset to the sensor. The input node is connected to a level shifter and then amplified by means of a voltage amplifier.

The voltage pulse at the output of the voltage amplifier is compared to a global threshold at the input of the discriminator. If the collected charge is above the applied threshold, a positive pulse will be generated at the output of the discriminator and will be further processed by the on-pixel digital logic. The DAC for local threshold tuning is implemented as a 3-bit binary weighted current source and is connected to the discriminator internal nodes. By tuning this DAC, the user can compensate for mismatch variations and thus achieve a lower minimum threshold.

Based on simulation results, the front-end has a gain of 550 mV/ke$^-$, a noise of 14 e$^-$ RMS and a minimum detectable charge (after threshold equalisation) of 93 e$^-$, for an analog power consumption of 1.125 µW per front-end, or 100 mW/cm^2 for operation with

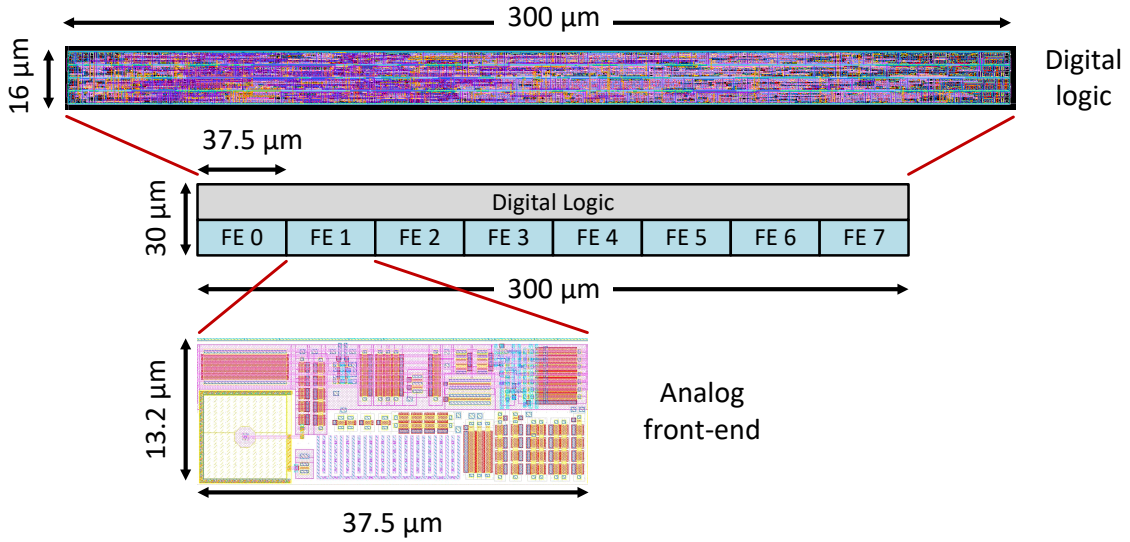


Figure 7.4 Layout of the CLICTD pixel, where the analog part is segmented in eight front-ends.

continuous power (before power pulsing). The power consumption of the analog front-end can be controlled by DACs in the analog periphery, to explore operation points suitable for different applications (e.g. particle tracking, dosimetry or imaging applications).

7.2.2 Digital logic

The on-pixel digital logic, presented in the block diagram in Figure 7.5, consists of two parts. The first part stores binary hit information for each individual front-end in eight flip-flops connected at the outputs of the discriminators (hit map). Each front-end output can be masked and therefore excluded from any further processing. Test pulses can be injected to the input of each individual front-end. The bits stored in the digital logic of each CLICTD pixel are summarised in Figure 7.6 (MSB on the left).

In the second part of the digital logic, the logic "OR" of the discriminated outputs from all eight front-ends is performed. Front-end outputs that have been masked are excluded from this operation. All further processing of the signal (e.g. ToA, ToT measurement) is performed using the combined output. In its nominal operation, the CLICTD digital pixel performs a simultaneous time and energy measurement. The ToA is measured using a 100 MHz clock distributed in the pixel, and the result is stored in an 8-bit counter. A programmable clock divider is placed in the CLICTD pixel, where the 100 MHz clock can be divided by a factor of $2 - 16$, to generate the clock used for the ToT measurement, as described in Table 7.1. This enables the option to adjust the range of the energy measurement. The division factor is

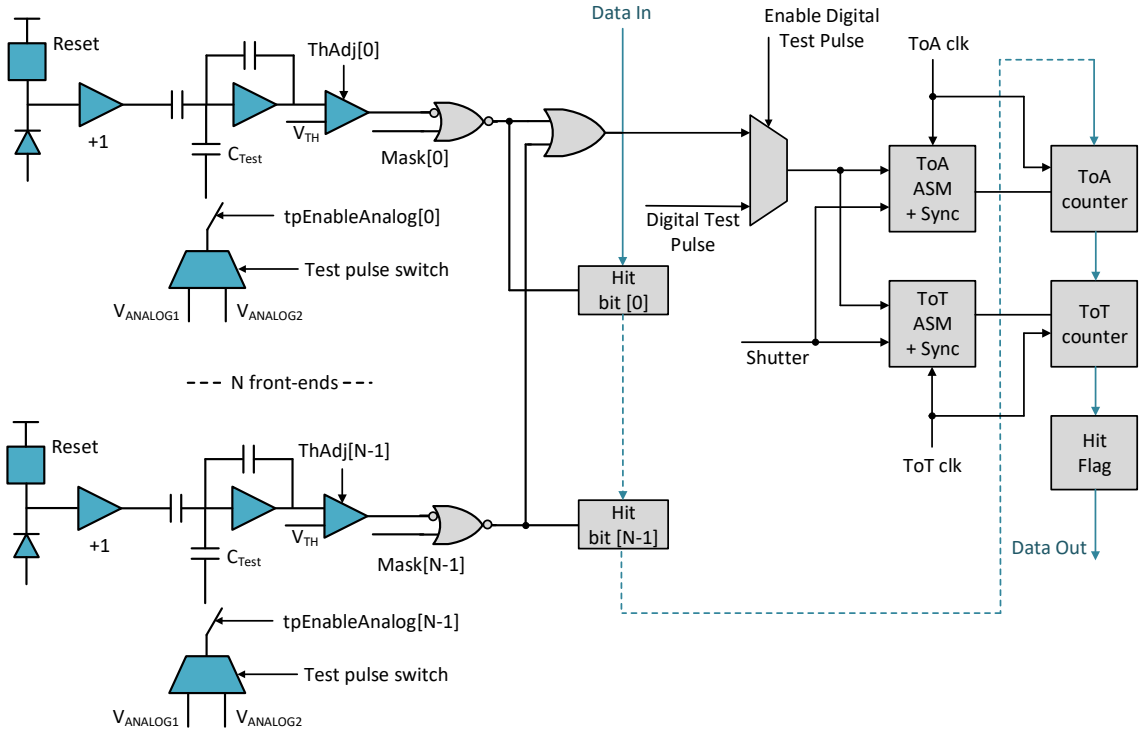


Figure 7.5 Block diagram of the CLICTD channel.

HF	ToT[4:0]	ToA[7:0]	HitBits[7:0]

Figure 7.6 Data stored in one CLICTD pixel.

programmable through the slow control of the chip, and is common for all pixels. The ToT measurement counts the time when the preamplifier output stays above the applied threshold, and stores the result in a 5-bit counter.

Table 7.1 ToT clock frequency.

totDiv[1]	totDiv[0]	ToT clock frequency [MHz]	ToT range [µs]
0	0	50	0.6
0	1	25	1.2
1	0	12.5	2.4
1	1	6.25	4.8

The counters in the digital logic are designed using the Linear Feedback Shift Register architecture (LFSR), implemented with XNOR gates. The advantage of LFSRs is that they occupy less area compared to different architectures (such as binary ripple counters or Gray code counters). As the counter result is not a binary value, the data needs to be decoded off-line using look-up tables. During the (frame-based) readout, the flip-flops in the counters, along with the hit map that contains the binary hit information for the front-ends, are connected as a shift register in order to shift the data out.

In addition to the nominal measurement, the on-pixel digital logic can be configured to perform two different types of measurements. First, the two counters (8-bit and 5-bit) are connected as one, 13-bit long, counter, which can be used to perform a ToA measurement with higher range (80 µs instead of 2.5 µs for the nominal measurement mode). A longer measurement window can facilitate operation in beam tests with longer shutter length. Second, a photon counting mode can be selected, again using the 13-bit long counter. In this mode, the logic accumulates the number of events that crossed the applied threshold within the same shutter frame. This measurement can be used for different phases of the chip debugging, as well as for threshold equalisation.

A summary of the different measurements that can be performed with the CLICTD pixel is presented in Table 7.2.

Last, the final piece of information stored in the CLICTD pixel is a bit called "hit-flag" ("HF" in Figure 7.5). The hit-flag flip-flop has its input tied to the LSB of the ToA ASM, and will go high once the digital logic detects a hit. This bit is used for applying a zero compression algorithm in the readout data, as will be explained in Section 7.3. In short, when the hit-flag is high (i.e. when the pixel detected a hit) and the compression algorithm is activated, all bits stored in the digital logic will be shifted out of the pixel. If the hit-flag is low (no hit detected), the pixel will only shift out the hit-flag bit, in order to reduce the

Table 7.2 Measurement modes of the CLICTD pixel.

Mode	Description
Nominal	8 bits time-stamping (ToA) + 5 bits energy (ToT)
Long counter	13 bits time-stamping (ToA)
Photon counting	13 bits photon counting (number of hits above threshold)

total amount of data shifted out of the chip. The frame can then be reconstructed off-line by reverting the compression algorithm.

Test pulsing

Injecting a test pulse either to the input of the analog front-end or directly to the input of the digital logic is foreseen for the CLICTD pixel.

In order to inject an analog test pulse (simulating a hit detected at the input of the front-end), the user needs to enable the analog test pulse injection in the front-end during the matrix configuration. The test pulse can be injected to selected front-ends in the pixel. Simultaneous test pulse injection to multiple front-ends is possible. When the test pulse is enabled, the test pulse signal (which is propagated along the column) is applied to the switch of an analog multiplexer in the front-end. The multiplexer will then switch between two voltage values (fine and coarse), generated in the analog periphery DACs (VANALOG1 and VANALOG2 in Table 7.3). A voltage pulse is then generated at the output of the multiplexer with amplitude equal to the difference of the two voltage DAC values. This pulse is applied to a test pulse injection capacitor connected at the input of the voltage amplifier. The charge on the capacitor simulates a charge collected on the diode and is then processed by the front-end and digital logic.

Similar to the analog, the digital test pulse can be selected for individual pixels, during the matrix configuration. In this case, the digital test pulse signal is multiplexed with the output of the "OR" function among the eight discriminator outputs from the front-ends. Consequently, all analog front-end outputs are overwritten by the digital test pulse signal, allowing the user to decouple and test separately the analog and digital parts of the detector cell.

A block diagram illustrating the analog and digital test pulse injection in the CLICTD pixel is presented in Figure 7.7.

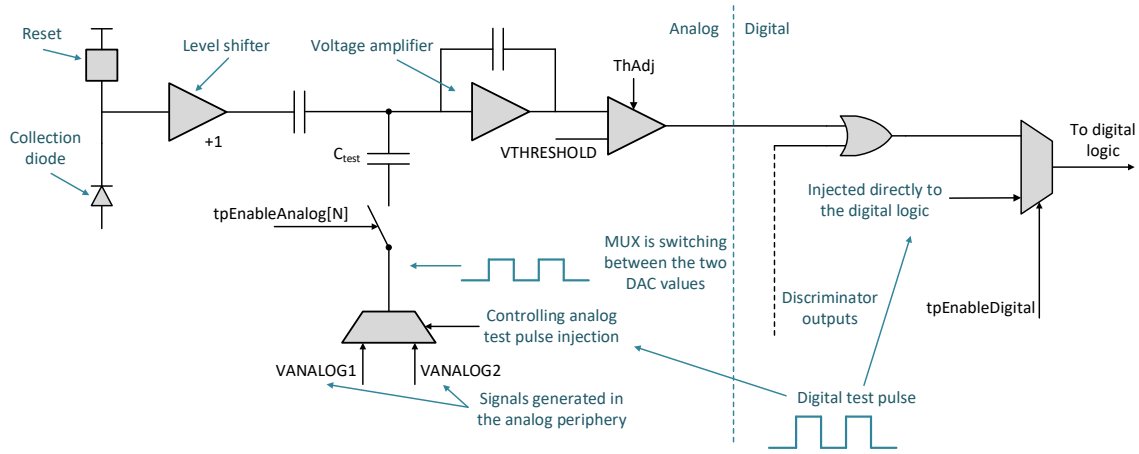


Figure 7.7 Test pulse injection in the CLICTD cell.

Asynchronous State Machines in the CLICTD detector cell

Asynchronous state machines are implemented in the digital logic to process the signals before they arrive to the counters. The motivation for using Asynchronous State Machines (ASMs) instead of synchronous was first the fact that ASMs occupy less area, as they don't contain flip-flops, and second the reduced power consumption. A clocked flip-flop would consume power for as long as the clock was running in the pixel, while the ASM is designed in such a way that the logic will consume only when a hit is detected (and therefore the clock is enabled in the counter). The procedure which was followed for designing the asynchronous state machines is described in [112].

A first state machine at the input of the digital logic (right after the multiplexer for digital test pulse injection) is used to ensure that only valid hits are processed by the digital logic. To be processed as valid, a hit rising edge should take place during the time interval when the shutter is open. The falling edge of the hit can take place either while the shutter is open or after it closes. This state machine will discard hits that arrive before the rising edge of the shutter, or after its falling edge.

The operation of the ToA state machine is presented in Figure 7.8. The state machine for the ToA measurement controls the signal that arrives to the ToA counter. This signal is the logic "AND" between the discriminator output and the shutter signal. It will therefore rise with the rising edge of the discriminator and fall with the falling edge of the shutter. The state machine is responsible for synchronising this signal to the measurement clock, such that no glitches or short clock pulses could be injected to the flip-flops in the counters, which could potentially cause unpredictable behaviour. The synchronised signal will always rise

with the rise edge and fall with the falling edge of the clock. When it reaches its maximum value, the counter saturates.

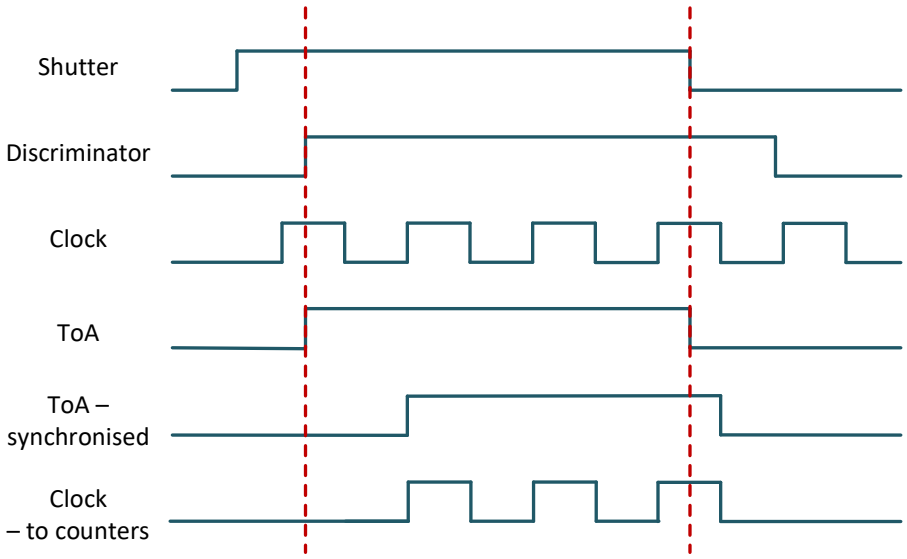


Figure 7.8 ToA measurement in the CLICTD cell.

Similarly, the state machine for the ToT measurement will synchronise the discriminator output to the measurement clock, for controlling the ToT counter. Figure 7.9 presents a timing diagram of the operation of the ToT state machine. When the photon counting mode is enabled, the synchronised discriminator signal is the one used as an input to the counters, in order to accumulate the number of events within the shutter frame. Same as the ToA counter, the ToT counter will saturate once it reaches its maximum value.

As mentioned in Section 4.2, no multi-hit capability is foreseen for the CLICTD prototype, meaning that only the first valid hit within the shutter frame will be processed. Any further hits within the same frame will be ignored by the digital logic.

Clock distribution

Two clocks arrive to the CLICTD matrix: a 100 MHz acquisition clock and a 40 MHz readout clock. A special block, the End-of-Column, is placed at the bottom of each column and is responsible for multiplexing between the two clock domains. In order to have a clean multiplexing, both clocks are gated while switching between clock domains. The clock at the output of this multiplexer is the 100 MHz clock when the chip is ready to acquire data and the 40 MHz clock when a matrix readout or configuration is enabled (data shifted out of or in the chip).

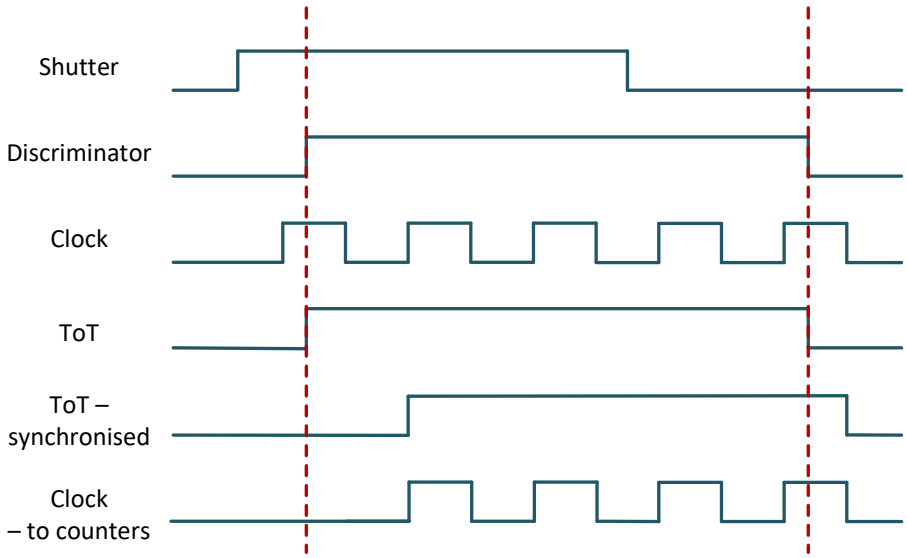


Figure 7.9 ToT measurement in the CLICTD cell.

This way, only one clock line is routed along the column. In order to fulfil the 10 ns time-stamping requirement, the propagation time of the clock should remain shorter than the bin size. A clock buffer is included in one every eight pixels in the column, which was selected such that the propagation delay for the clock would be below 10 ns for a column of 1.5 cm (in view of a future, full-scale chip). The remaining seven pixels use the clock output from the first one, and this eight pixel structure is what is replicated to construct the column. The same approach was followed for distributing the shutter signal along the pixel column.

During readout, the End-of-Column block is responsible for counting the number of pixels and the number of bits per pixel that are shifted out of the column. A diagram of the logic in the End-of-Column state machine is presented in Figure 7.10. Due to the applied compression algorithm, the amount of data shifted out is not fixed but it depends on the cell occupancy. The state machine in the End-of-Column takes into account the compression algorithm and ensures that all data have been shifted out before the readout proceeds to the next column.

7.3 The CLICTD periphery and chip interface

7.3.1 The CLICTD analog periphery

A total of 20 Digital to Analog Converters (DACs) for biasing the analog front-end are placed in the CLICTD analog periphery. The biasing DACs are designed following the

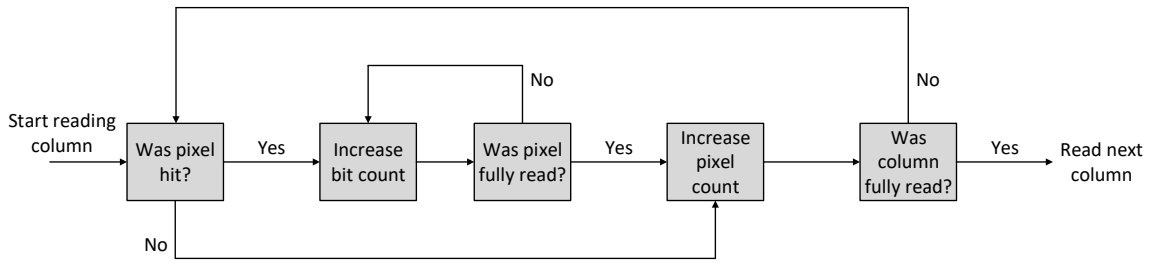


Figure 7.10 Algorithm diagram of the CLICTD End-of-Column block.

binary-weighted current source architecture. A low frequency unity gain buffer is used to drive each of these signals to the pixel matrix. This buffer is biased by an additional DAC in the periphery.

The CLICTD periphery features two differential receivers and three differential drivers that are used for the clock inputs and outputs and for reading out the data after acquisition. The use of these blocks is further explained in Section 7.3.4. A programmable 4-bit DAC is used for biasing the differential drivers. The differential receivers are biased to a constant current, to ensure that the clock inputs will always reach the core of the chip, without depending on the reset state of the registers. A list of the DACs in the analog periphery is presented in Table 7.3.

Last, the voltage reference in the chip is provided by a bandgap circuit in the periphery. The generated voltage reference is translated to a current which is used to bias the current sources in the DACs. This current, and therefore the range of the DACs, can be tuned through a slow control register.

7.3.2 The CLICTD digital periphery

In the digital domain, the CLICTD periphery is based on a slow control interface which is used for programming the different parts of the chip, and a readout logic which is responsible for shifting the acquired data out of the chip. A block diagram of the chip periphery is illustrated in Figure 7.3

7.3.3 Slow control

A standard I^2C interface was selected for the slow control of the CLICTD chip. The I^2C bus provides a 2-line communication between different ICs or modules using a serial data (SDA) and a serial clock line (SCL) [97]. The I^2C fast mode with a speed of 400 kbit/s is implemented for this design. The slow control is used for writing and reading all internal

Table 7.3 List of DACs in the CLICTD analog periphery

DAC	**Resolution**	**Biasing node**
VBIASResetTransistor	8 bits	Transistor resetting the input node
VRESET	8 bits	Reset reference
VBIASLevelShift	6 bits	Current source in input level shifter
VANALOG1	9 bits	Test Pulse analog voltage 1
VANALOG2	8 bits	Test Pulse analog voltage 2
VBIASPREAMPN	6 bits	Current source in amplifier
VNCASC	8 bits	NMOS cascode in amplifier and comparator
VPCASC	8 bits	PMOS cascode in the amplifier
VFBK	8 bits	Baseline voltage at the amplifier output
VBIASIKRUM	6 bits	IKRUM current source
VBIASDISCN	6 bits	NMOS current source in discriminator
VBIASDISCP	6 bits	PMOS current source in discriminator
VBIASDAC	6 bits	Threshold equalisation DAC
VTHRESHOLD	9 bits	Threshold voltage value
VNCASCCOMP	8 bits	Comparator output cascode
VBIASLevelShiftstby	6 bits	Current source in input level shifter - standby
VBIASPREAMPNstby	6 bits	Current source in amplifier - standby
VBIASDISCNstby	6 bits	NMOS current source in discriminator - standby
VBIASDISCPstby	6 bits	PMOS current source in discriminator - standby
VBIASDACstby	6 bits	Threshold equalisation DAC - standby
VBIASSlowBuffer	8 bits	Slow buffer
VLVDSD	4 bits	Bias LVDS driver

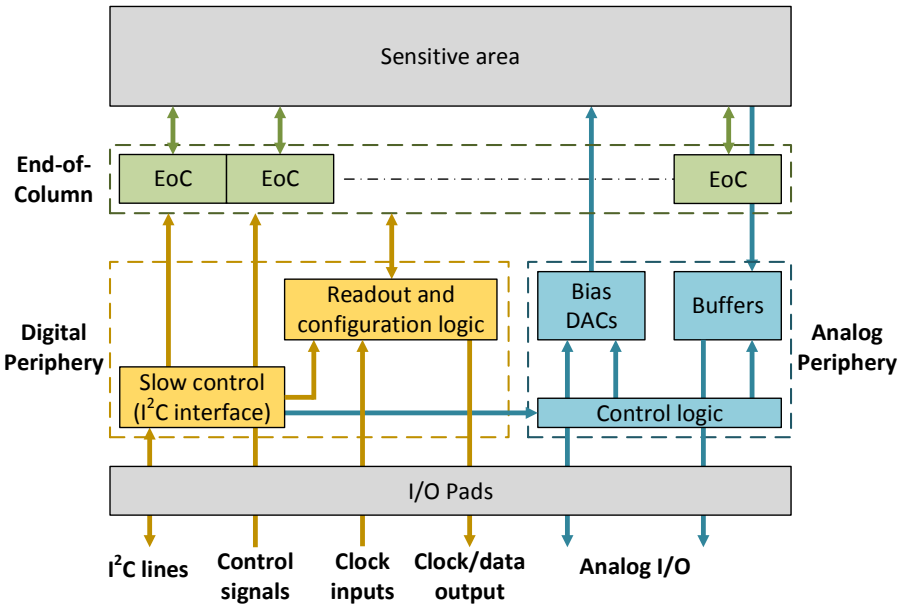


Figure 7.11 Block diagram of the CLICTD periphery.

registers, in order to perform actions such as: configuring analog periphery DACs, programming the pixel matrix, sending test pulses, enabling or disabling the power pulsing scheme and initiating a readout. These operations will be described in more details in the following paragraphs.

Enabling or disabling the analog and digital test pulse injection in the CLICTD chip is controlled by the slow control interface. Test pulsing can be enabled for the full chip, or for selected columns. In order to enable the (analog or digital) test pulse injection in certain pixels, the user sets the corresponding bits during the programming phase of the matrix. The test pulse signal can be injected either by programming a slow control register or by applying an external signal to one of the CLICTD pads. Applying the external signal offers better control of the signal's timing, since the slow control register is limited by the transmission speed of the slow control interface.

A similar approach is followed for the signals that control the power pulsing and the start of a readout. These signals can also be applied either by the slow control interface or by external signals.

The option to overwrite or monitor one of the voltages generated in the analog periphery DACs is foreseen for the CLICTD slow control. For overwriting an internal DAC, a pad connected to a voltage generated in the data acquisition system is used. The pad used for monitoring the internal DAC value is connected to an ADC outside the chip. Last, the voltage reference generated in the internal bandgap circuit can also be overwritten or monitored.

Other functions of the slow control interface are related to the configuration of the pixel matrix. First, features that are common for all pixels in the matrix are selected through a slow control register. Such features include the measurement mode (nominal, long ToA, photon counting), the value of the ToT clock frequency and enabling or disabling the compression algorithm. The specific configuration for each pixel is also shifted in the matrix using the slow control interface. The values of the configuration bits are stored in a register and are shifted in the matrix. One bit per column is shifted in at a time, using a 16-bit slow control register. For each pixel, a total of 41 configuration bits is needed: five (one for masking, one for enabling test pulse, three for local threshold trimming) for each of the eight front-ends (40 bits in total), plus one for enabling the digital test pulse injection. As the number of bits that can be shifted in the cell is limited by the number of flip-flops (22) in the digital logic, the configuration needs to be repeated twice ($21 + 20$ configuration bits) in order to fully configure the matrix, each time latching the data to the appropriate front-end inputs. For further information on the matrix features, refer to Section 7.2.

7.3.4 Readout architecture

In order to shift the acquired data out of the chip, a serial readout running at a 40 MHz clock is implemented. The data are shifted out column by column, starting from the leftmost one, and the clock is enabled only for the column that is being read out at each time in order to keep the average power consumption low.

A header is added at the start of each column readout, as well as at the start and end of the frame, such that it will be easier to identify when the frame starts or stops and when the readout switches between columns. The header is constructed in a way that it would not be possible to appear in the real data corresponding to a CLICTD pixel. The header contains a hit flag set to high, followed by all ones in the ToT and ToA bits. This is done such that the header data match the illegal state of the XNOR LFSR counters (a state that cannot appear in the real acquired data). For the hit map bits, the two MSBs are set to "01" and the following four bits contain the address of the column that will be shifted out (bits marked with "X" in Figure 7.12). The remaining two LSBs are set to "00". The CLICTD data stream is shown in Figure 7.13.

Three differential signals are sent to the output pads of the CLICTD during readout: the clock output (CLK_OUT), the data output (DATA_OUT) and the enable output (ENABLE_OUT). The enable output signal goes high at the start of the transmitted frame and low once all data are shifted out of the chip. Along with the clock output, this signal is used to synchronise from the data acquisition system and sample the output data. A timing diagram of the CLICTD readout is presented in Figure 7.14.

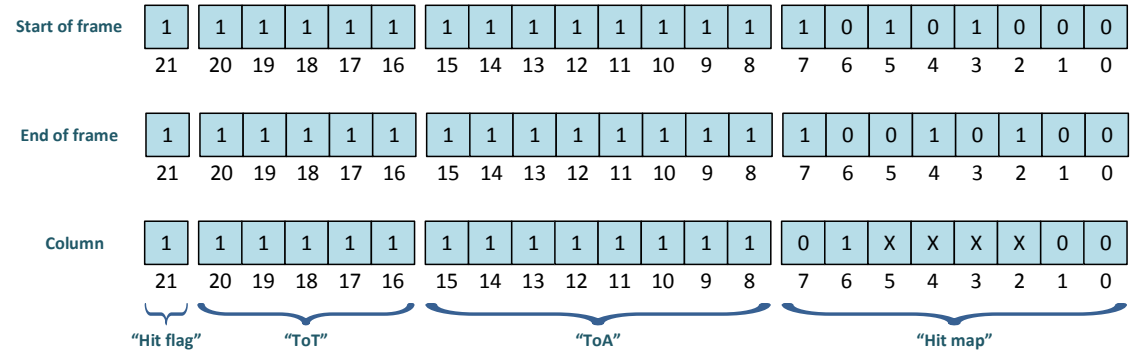


Figure 7.12 CLICTD headers.

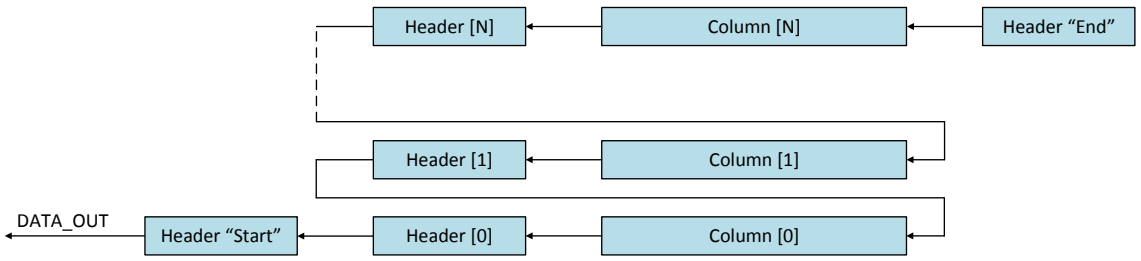


Figure 7.13 CLICTD data stream.

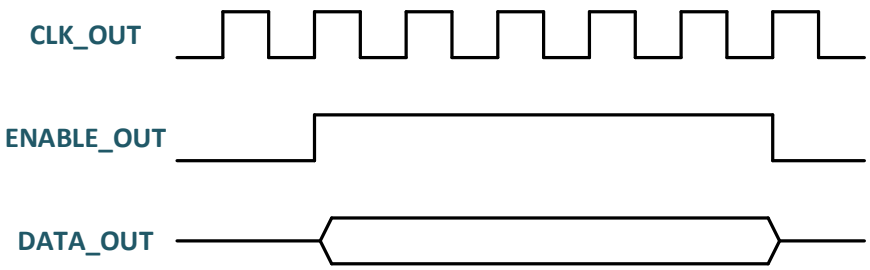


Figure 7.14 Timing diagram of the CLICTD readout.

7.3.5 Compression algorithm

The expected maximum occupancy in the CLIC silicon tracker, for the cell dimensions of CLICTD, is $\sim 1\%$. In order to reduce the amount of data that are shifted out of the chip, a data compression scheme, based on a zero suppression algorithm, is implemented. When data compression is enabled, the total of 22 bits stored in the cell is shifted out only if the cell detected a hit (i.e. if the hit flag was set to "high"). For cells that were not hit, only one bit, corresponding to the hit flag, will be shifted out. The option to disable the compression algorithm and force all data to be shifted out is foreseen for the CLICTD prototype, for debugging purposes.

As presented in Table 7.4, the applied compression algorithm can reduce the readout time by a factor of ~ 15. The numbers refer to the CLICTD matrix size (16×128 pixels) and the amount of data shifted out when the compression is applied is calculated for a detector cell occupancy of 1%.

Table 7.4 Readout time without and with compression.

	Data per frame	**Readout time**
Compression disabled	45 kbits	1.12 ms
Compression enabled	2.9 kbits	72 µs

7.3.6 Power consumption

As introduced in Section 4.2, a power pulsing scheme was implemented in the CLICTD chip in order to set the circuit to a standby mode between acquisitions.

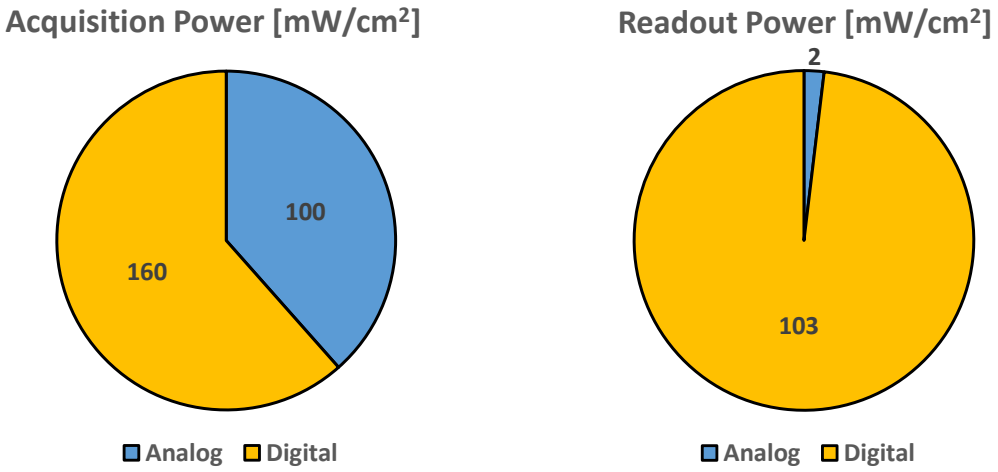
For the analog part of the pixel matrix, the main current driving nodes of the front-end can be set to a low power mode by selecting between power on and standby biasing DACs. The biasing lines are connected to the pixels from the left side of the matrix, where multiplexers are used to switch between power on and standby biasing. In the front-end, power pulsing is applied to the level shifter and preamplifier current sources, the NMOS and PMOS current sources in the discriminator and to the threshold equalisation DAC. By applying the power pulsing scheme, the average power consumption of the analog part of the matrix can be reduced by a factor of ~ 50; from 100 $\mathrm{mW/cm^2}$ during operation with continuous power, to ~ 2 $\mathrm{mW/cm^2}$.

The analog periphery consists of 21 biasing DACs, buffers to drive the biasing signals and a bandgap circuit. The total power consumption of the analog periphery is simulated to be about 8 mW, while no power pulsing is applied to these blocks.

In the digital logic of the CLICTD pixel, the power consumption is minimised by means of clock gating. During acquisition, the clock is enabled in the counters only if a hit is detected. The clock gating in the pixel is handled by asynchronous state machines. When a readout is issued, the clock is gated in the End-of-Column, and enabled only for the column that is being read out. The buffers for distributing the clock signal along the column are therefore running only as long as a clock is enabled in the column.

During acquisition, the average digital power consumption of a channel that detects a hit is 455 µW (calculated as a worst case scenario, with the maximum switching activity). Based on the pixel occupancy in the experiment, only $\sim 1\%$ of the pixels are expected to detect a hit. According to simulations, when data are being read out, the chip consumes about 103 $\mathrm{mW/cm^2}$. This was calculated based on the switching activity in the matrix, for a worst case scenario. Distributing the clock requires an additional 110 $\mathrm{mW/cm^2}$ (during acquisition, when a 100 MHz clock is distributed), while a static leakage power of 0.6 $\mathrm{mW/cm^2}$ has been simulated.

The contributions of the analog and digital power consumption of the CLICTD matrix during acquisition and during readout are presented in Figures 7.15a and 7.15b respectively. The digital power consumption is calculated as the average power consumption for a worst case scenario and for an occupancy of 1%.



(a) (b)

Figure 7.15 Contributions of the analog and digital power consumption of the CLICTD matrix (a) during acquisition and (b) during readout (simulated values).

Averaging the three different components that contribute to the digital power consumption in the CLICTD matrix (power for data acquisition, readout and clock distribution), and taking

into account the leakage current, results in an average power consumption below 3 $\mathrm{mW/cm^2}$ over the 20 ms cycle of the CLIC beam (for the expected pixel occupancy of 1%).

The two clock signals arriving to the chip are gated in the digital periphery. The 100 MHz, acquisition, clock is gated with the power pulsing signal and distributed to the matrix only when the chip is in power-on mode. The 40 MHz readout clock is gated at the input of the readout logic. The logic is therefore clocked only after a readout command reaches the chip. An average power consumption over the CLIC cycle below 3 mW has been simulated for the CLICTD digital periphery (worst case scenario simulated, with the maximum switching activity).

Further power is consumed by the differential receivers and drivers in the periphery. The CLICTD chip features two differential receivers for the 100 and 40 MHz clock inputs and three differential drivers for the clock, data and enable output signals. The power consumption of these blocks is 7.2 mW per driver (biased with a constant current of 4 mA at 1.8 V power supply, in order to provide a voltage difference of 400 mV across a 100 Ω termination resistor) and 2.5 mW per receiver (at their maximum bias current). Similar to the analog periphery, no power pulsing is foreseen for the differential drivers and receivers in the CLICTD prototype. The simulated total power of the CLICTD periphery (for the maximum bias current for the LVDS drivers) is therefore $\sim$ 38 mW (22 mW LVDS drivers + 5 mW LVDS receivers + 8 mW analog periphery + 3 mW average power consumption for digital periphery).

7.4 Integration and verification of the CLICTD chip

Similar to the C3PD chip, the CLICTD design was integrated using the digital-on-top approach. The functional verification of the chip was performed using the Universal Verification Methodology (UVM) [98].

The chip was thoroughly verified before being submitted. A list of tests was defined once the slow control and readout architectures have been decided, and all tests were run in two phases. The first phase of the verification was performed using the behavioural models of the different blocks (RTL netlist). After debugging the functionality in the RTL netlist, the design was synthesized, placed and routed and a post-layout netlist, including the delays introduced to the signals from the gates and routing lines was generated. The post-layout netlist was verified in three different process-voltage-temperature corners (minimum, typical and maximum in Table 7.5) in order to detect any timing violations that could have possibly resulted from the clock tree synthesis, routing etc. The procedure was repeated until all tests, in all three corners, were running without any timing violations.

Table 7.5 Simulation corners for the CLICTD verification.

Corner	Process	Voltage [V]	Temperature [C]
Minimum	Fast	1.98	-40
Typical	Typical	1.80	25
Maximum	Slow	1.62	125

The final layout of the CLICTD chip is presented in Figure 7.16. All I/O pins are placed on the bottom side of the chip, with the pad to pad pitch at 100 µm. Additional pads are placed on the sides for connecting the reverse bias voltages. Table 7.6 presents a list of the pins in the CLICTD prototype.

The design of the CLICTD prototype was done in view of a future chip with a full reticle sized matrix (possibly measuring $\sim 2.5 \times 3.2$ cm^2) that can be used in the experiment. The design is therefore scalable and different blocks can be re-used with only minor (or no) modifications. If desired, the blocks in the pixel matrix (front-end and digital logic), as well as the analog periphery and readout logic can be directly imported to a new design. The slow control interface, although suitable for a prototype, could be replaced by a faster standard protocol (such as SPI) for future, larger chips that require a higher amount of data to be shifted in the chip for programming the pixel matrix. Encoding algorithms (e.g. 8b/10b or 64b/66b encoding) can be possibly implemented in next versions to allow clock recovery from the readout data. A future system-on-chip could also feature a PLL, such that only one clock (e.g. the 40 MHz readout clock) is input to the chip and the other clock (e.g. the 100 MHz acquisition clock) is generated internally. The advantage from the system point of view would be that only one, relatively low frequency, clock would need to be distributed to all modules.

The CLICTD prototype is developed in a process with six metal layers available. Since the routing in the pixel matrix required the five lower metals to be complete, the power is connected to the matrix using only the top, low resistivity, metal layer. This ensures an acceptable voltage drop along the pixel columns for the matrix size of the CLICTD chip (below 5 mV/column for the analog power), where the power is connected to power pads at the bottom side of the periphery and routed to the top. However, the power drop would be limiting for a large-scale matrix, meaning that the power distribution would need to be revised for the design of a future chip. For example, power could be connected from both the bottom and top side of the chip, or additional power pads could be placed on top of the pixel matrix.

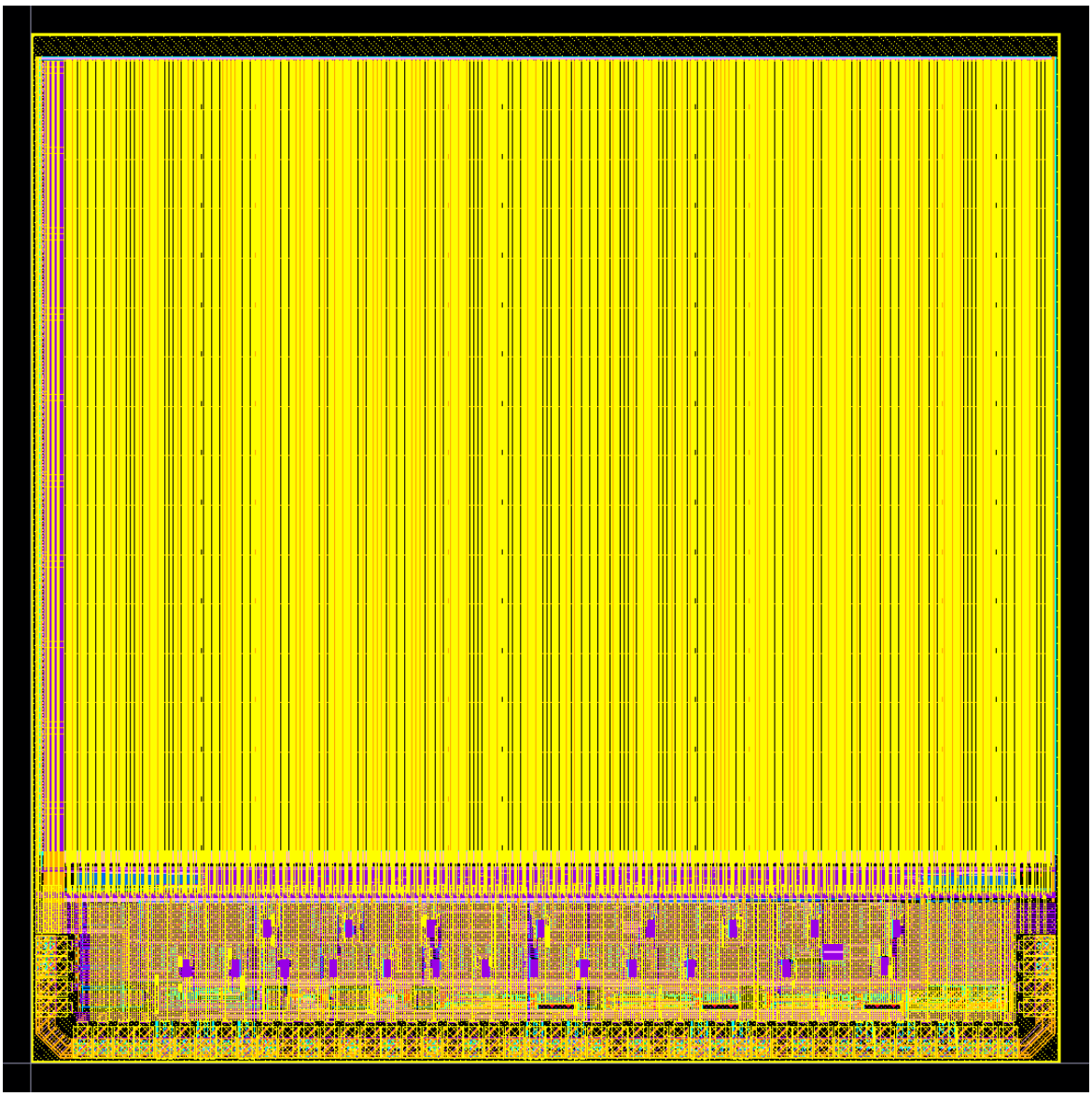


Figure 7.16 Layout of the CLICTD chip.

Table 7.6 List of I/O pins in the CLICTD prototype.

Pin	Dir.	Description
SDA	CMOS I/O	I^2C data line
SCL	CMOS In	I^2C clock line
PWREN	CMOS In	Power pulsing signal
TPULSE	CMOS In	External test pulse signal
READOUT	CMOS In	External pin to issue readout
SHUTTER	CMOS In	Shutter signal
RSTN	CMOS In	Reset signal (active low)
CLK_100_p	LVDS In	100 MHz acquisition clock
CLK_100_n	LVDS In	100 MHz acquisition clock
CLK_40_p	LVDS In	40 MHz readout clock
CLK_40_n	LVDS In	40 MHz readout clock
DATA_OUT_p	LVDS Out	Serial data output
DATA_OUT_n	LVDS Out	Serial data output
CLK_OUT_p	LVDS Out	Clock output
CLK_OUT_n	LVDS Out	Clock output
ENABLE_OUT_p	LVDS Out	Enable data output
ENABLE_OUT_n	LVDS Out	Enable data output
ANALOG_IN	Analog In	Analog input
REF	Analog In	Reference voltage
ANALOG_OUT	Analog Out	Analog output
VDDA	Power	Analog power supply (1.8 V, 7 pins)
VSSA	Ground	Analog ground (7 pins)
VDDD	Power	Digital power supply (1.8 V, 8 pins)
VSSD	Ground	Digital ground (8 pins)
PWELL	Reverse bias	P-well bias (2 pins)
SUB	Reverse bias	Substrate bias (2 pins)

7.5 Summary

The CLIC Tracker Detector (CLICTD) is a monolithic chip designed in a 180 nm High Resistivity (HR-) CMOS process. The chip was submitted using a process split, and wafers will be produced with two different geometries for the additional N-layer: one with continuous N-layer under the sensitive area and one with segmented N-layer along the long direction in order to reduce the signal collection time.

The key design parameters of the CLICTD chip are summarised in Table 7.7. The first measurement results, obtained once the chip was produced, are presented in Chapter 8.

Table 7.7 Main parameters of the CLICTD design.

Parameter	**Value**
Process technology	180 nm HR-CMOS
ASIC size	5.0×5.0 mm^2
Sensitive area	4.8×3.84 mm^2
Matrix size	16×128 pixels
Pixel size	300×30 µm^2
Collection diode pitch	37.5×30 µm^2
Gain[1]	550 mV/ke$^-$
Noise RMS[1]	14 e$^-$
Minimum threshold[1]	93 e$^-$
Nominal measurement mode	8-bit ToA + 5-bit ToT
Other measurement modes	13-bit ToA / 13-bit photon counting
ToA bin size	10 ns
ToT range	$0.6 - 4.8$ µs
Data compression	Zero-suppression per pixel
Readout scheme	Shutter based
Data output clock	40 MHz
Power pulsing scheme	Analog low-power mode and clock gating
Power consumption (no power pulsing)[1]	210 mW/cm^2 + 38 mW periphery
Power consumption (after power pulsing)[1]	5 mW/cm^2 + 38 mW periphery

[1] Simulated values.

Chapter 8

Measurements with the CLICTD chip

In this Chapter, the first measurements that were performed once the CLICTD chip was fabricated are presented. The first, preliminary, results with the CLICTD chip presented in the next sections, will be followed by further extensive characterisation in laboratory and beam tests.

8.1 Measurement setup

The CaRIBOu readout system, same as the one used for characterising capacitively coupled assemblies with the C3PD sensor and CLICpix2 readout chip (described in Chapter 6), was used for characterising the CLICTD chip. The same evaluation kit and the CaR interface board were used, while a new custom PCB was designed and produced for wire-bonding and connecting the CLICTD chip. Further details on the custom PCB design for the CLICTD chip may be found in Appendix A.3. A photo of the CLICTD chip, wire bonded on the PCB, is shown in Figure 8.1. The measurement setup is presented in Figure 8.2.

Similar to the case of the capacitively coupled assemblies, all signals and communication protocols, as well as the regulation of power supplies, are handled by the CaRIBOu readout system. Four power supplies are connected to the CLICTD chip. Two for powering the analog and digital circuitry of the chip, and two more for controlling each of the two reverse bias voltages required for the sensor operation, as will be described in Section 8.2.

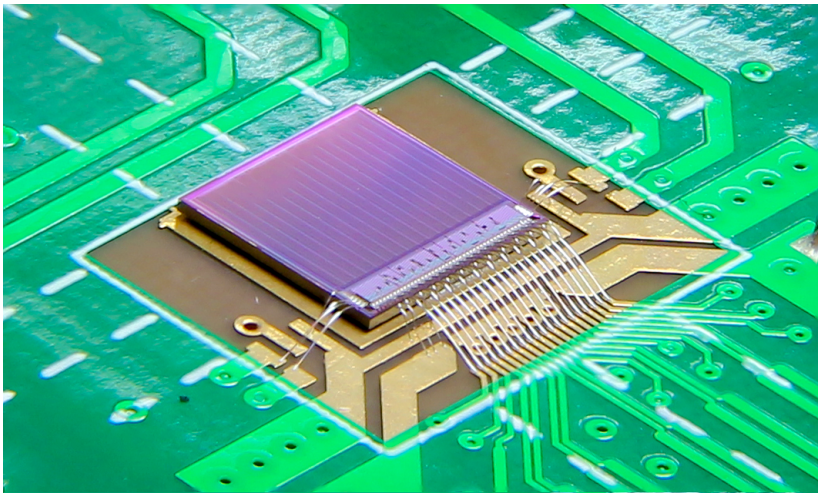


Figure 8.1 Photo of the CLICTD chip, wire bonded on the PCB.

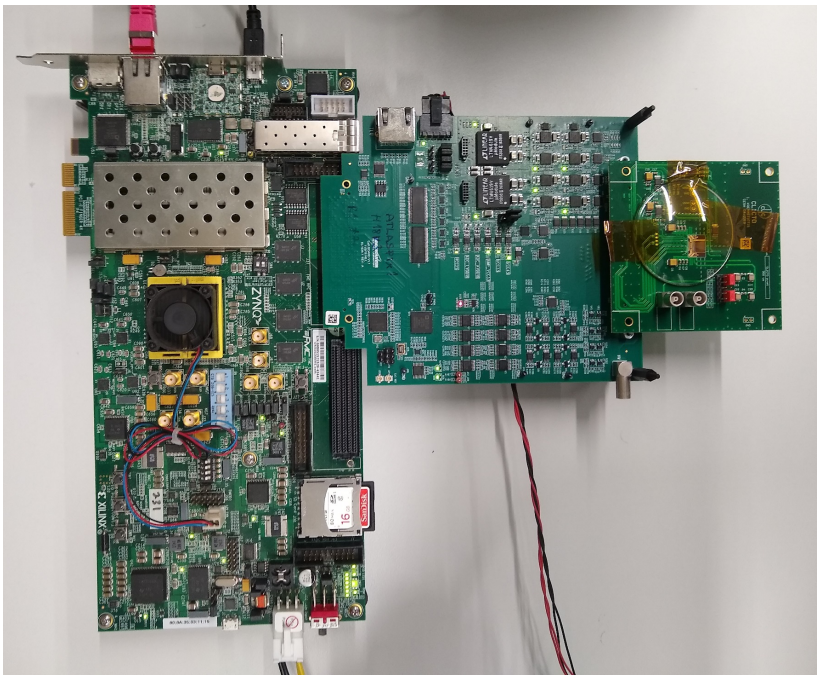


Figure 8.2 Photo of the CaRIBOu readout system for testing the CLICTD chip. From left to right: evaluation kit, CaR board, chip board with a CLICTD sample mounted on it.

8.2 I-V characteristic

Following the production of the CLICTD chips, the first samples were wire-bonded on the PCBs and the sensor characteristics were measured. In order to deplete the sensor volume, two nodes need to be reverse biased: the P-wells where the on-pixel electronics are placed (PWELL in Figure 8.3), and the substrate of the chip (SUB in Figure 8.3).

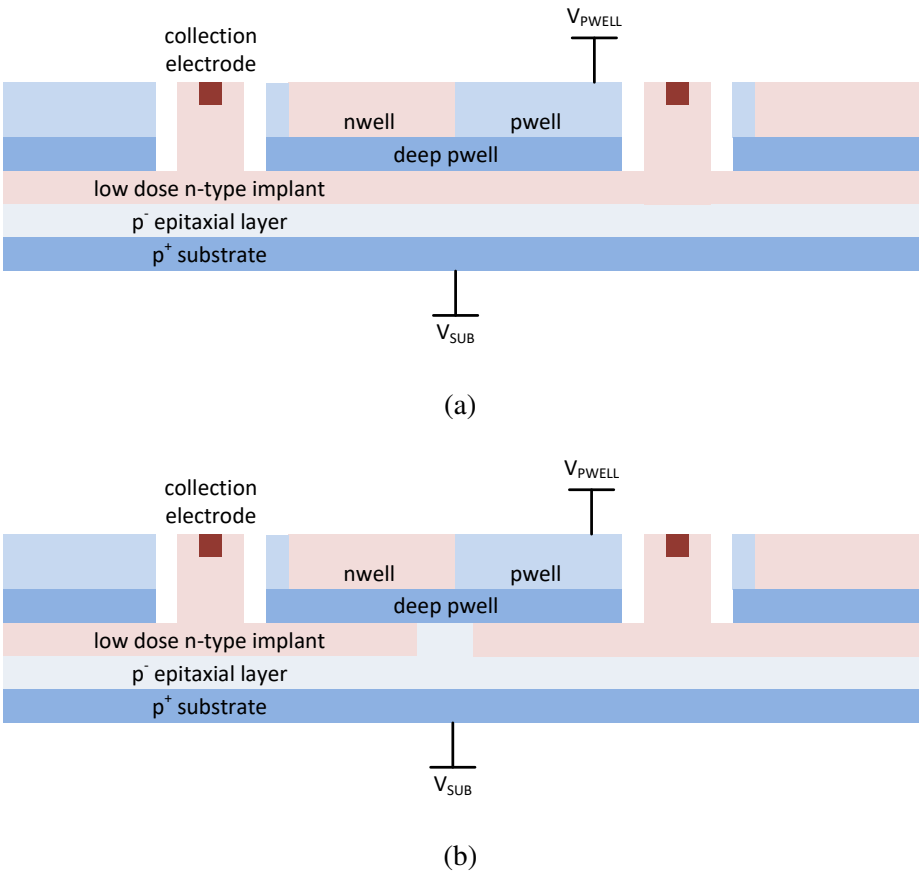


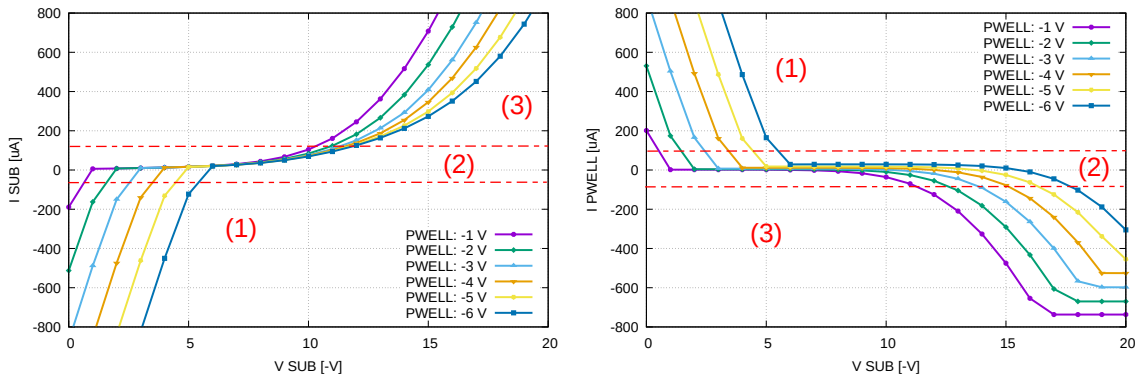
Figure 8.3 The two CLICTD process splits: (a) the first CLICTD process split, with continuous N-implant, and (b) the second CLICTD process split, with gap in N-implant (not to scale).

A schematic cross-section of the first process split is presented in Figure 8.3a. This process split offers an improved isolation of the P-wells from the chip substrate, thanks to the continuous N-implant. Due to this isolation, the possibility to apply a higher (in absolute value) reverse bias to the substrate compared to the P-wells is expected. The reverse bias at the P-wells can be as low as -6 V, limited by the on-pixel circuits [113].

In the second process split, introduced in Section 7.1, the deep N-implant is segmented at the pixel borders, as illustrated in Figure 8.3b. For this process split, a different I-V characteristic is expected, as the isolation between the deep P-well in the matrix and substrate is now reduced.

In order to investigate the different sensor behaviour for the two process splits, the sensor I-V characteristics were measured. Two power supplies were used to reverse bias the two nodes. The deep P-well bias was set to a fixed voltage ranging from -1 to -6 V. For each deep P-well bias, the substrate voltage was scanned and the leakage current was measured both at the deep P-well and the substrate. All measurements presented in this section were performed at room temperature, and with the CLICTD chip powered on.

Starting from the first process split, the leakage current in the substrate was measured while scanning the reverse bias applied to the substrate. Figure 8.4a presents the measured values of the substrate leakage current as a function of the substrate bias for different values of the deep P-well bias, for one measured CLICTD sample. Then, the leakage current in the PWELL node was measured, again as a function of the substrate bias for different values of the deep P-well bias. The resulting curves are plotted in Figure 8.4b. The saturation for higher absolute values of the reverse bias voltage is an artefact of the substrate leakage current reaching the current compliance of the instrument used for this measurement. A second sample from the same split was also measured and similar results were obtained.



(a) (b)

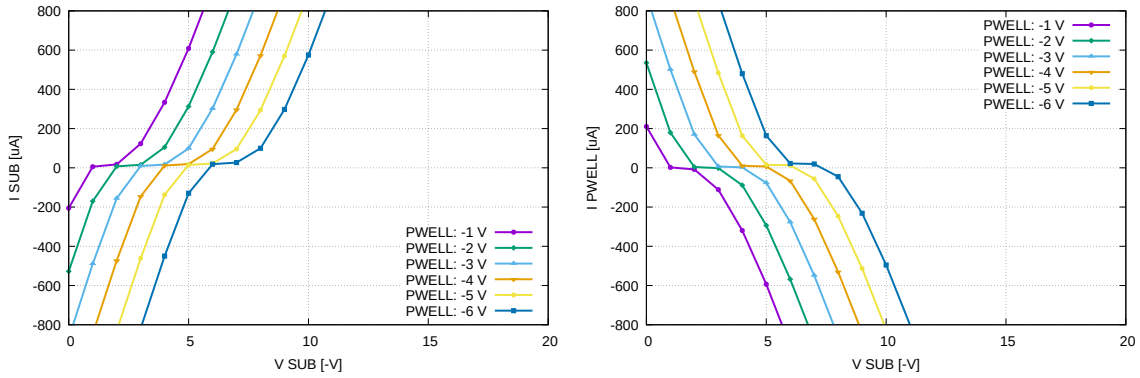
Figure 8.4 Leakage current measured at (a) the substrate and (b) the P-wells in the CLICTD matrix as a function of the applied substrate bias. Each curve is measured for a different value of the P-well bias. Results shown for the CLICTD sample from the first process split - continuous N-implant.

As shown in the plots in Figure 8.4, the I-V characteristic is divided into three different regions. In the first region (region "1" in Figure 8.4), the P-well voltage is more negative than the substrate voltage. In this case, the holes move to the P-well, resulting in a positive current measured at the P-well and negative at the substrate. This current flow is due to the punch-through behaviour resulting from the voltage difference between the two terminals. The current path in punch-through is from a P-type terminal to another P-type terminal, in contrast with the junction breakdown (such as in Section 6.1.2) where the current flows from an N-type terminal to the P-type substrate. Increasing the absolute value of the substrate voltage results in entering a second region, with stable low leakage current, marked with "2" in Figure 8.4. This is the region where the sensor can be operated. A further increase in the absolute value of the substrate voltage will lead to a punch-though with inverted current flow compared to the first region, as holes will move to the substrate (region "3" in Figure 8.4).

The curve for the PWELL leakage current (Figure 8.4b) is in good agreement with the TCAD simulations [110]. The leakage current measured in the P-wells is stable, and limited to $< 20\,\mu A$ within a range of about 10 V of the substrate bias. Outside this range, a high leakage current is measured due to the punch-through between the deep P-well and the substrate. The bias voltage where the punch-through between the deep P-well and the substrate is lower (in absolute value) than the simulated in [110] due to the different doping for the deep N-implant. Moreover, the value of the punch-through voltage may vary depending on the temperature. For the substrate leakage current (Figure 8.4a), a similar curve with inverted leakage current direction would be expected. The stable region (marked with "2" in Figure 8.4a) has a reduced width compared to the same range for the P-well leakage current. In addition, the measured leakage current in this region is constantly increasing instead of remaining stable. The substrate leakage current in this region is not dominated by punch-through, indicating that possibly other effects at the edge of the matrix or at the chip periphery are also affecting this measurement. Nevertheless, the sensor can be biased at its nominal operation point (-6 V at both nodes), with a leakage current below $20\,\mu A$ for the full chip area.

The plots for the leakage current in the substrate and the deep P-well as a function of the reverse bias voltages, for the measured CLICTD sample from the second process split, are presented in Figures 8.5a and 8.5b respectively. The resulting curves are in good agreement with the simulations and the slope is, as expected, dominated by the punch-through behaviour. The gap in the N-implant results in an electrical connection between the deep P-well and the substrate through the high resistivity P-type epitaxial layer. Consequently, the reverse bias voltage range where the detector has low leakage current is reduced, indicating that the two nodes should be biased at similar voltage levels during the operation of the chip. For a

voltage bias of -6 V both at the deep P-well and the substrate, a leakage current of 20 µA was measured, for the full chip area.



(a) (b)

Figure 8.5 Leakage current measured at (a) the substrate and (b) the P-wells in the CLICTD matrix as a function of the applied substrate bias. Each curve is measured for a different value of the P-well bias. Results shown for the CLICTD sample from the second process split - gap in N-implant.

Concluding, the sensor I-V characteristics were measured for samples from both process splits, confirming that the sensor can be operated at its nominal bias, with low leakage current. The performance of each process split in terms of spatial resolution, charge collection time and efficiency will be evaluated over beam tests.

8.3 Slow control

After powering up the chip, a test on the slow control interface was performed, in order to verify that all internal registers have their expected values after resetting the chip, and that a successful read / write operation can be performed using the slow control interface.

The operation of the CLICTD slow control interface has been verified successfully for the tested samples. The reset values of the CLICTD slow control registers, as expected by design and verified after resetting the chip, are presented in Table 8.1.

Table 8.1 Reset values of the CLICTD slow control registers.

Register	**I^2C Address**	**Length**	**Reset value**
globalConfig	0x00	8	0x01
internalStrobes	0x01	8	0x00
externalDACSel	0x02	8	0x00
monitorDACSel	0x03	8	0x00
matrixConfig	0x04	8	0x08
configCtrl	0x05	8	0x00
configData	0x06	16	0x0000
readoutCtrl	0x08	8	0x00
tpulseCtrl	0x0A	16	0xFFFF
VBIASResetTransistor	0x10	8	0x03
VRESET	0x11	8	0x68
VBIASLevelShift	0x12	6	0x09
VANALOG1	0x13	9	0x000
VANALOG2	0x15	8	0x00
VBIASPREAMPN	0x16	6	0x05
VNCASC	0x17	8	0x5B
VPCASC	0x18	8	0x82
VFBK	0x19	8	0x47
VBIASIKRUM	0x1A	6	0x04
VBIASDISCN	0x1B	6	0x08
VBIASDISCP	0x1C	6	0x09
VBIASDAC	0x1D	6	0x07
VTHRESHOLD	0x1E	9	0x09A
VNCASCCOMP	0x20	8	0x76
VBIASLevelShiftstby	0x21	6	0x01
VBIASPREAMPNstby	0x22	6	0x01
VBIASDISCNstby	0x23	6	0x01
VBIASDISCPstby	0x24	6	0x01
VBIASDACstby	0x25	6	0x01
VBIASSlowBuffer	0x26	8	0x0F
AdjustDACRange	0x27	8	0x03
VLVDSD	0x28	4	0x0F

8.4 DAC scans

As introduced in Section 7.3, the voltages generated in the CLICTD analog periphery DACs can be monitored in order to verify that they match the simulated ones. DAC scans were performed for each of the periphery DACs, confirming that they respond as expected and in good agreement with the simulations. An example plot of the monitored voltage level at the output of one current DAC (bias for the preamplifier current) as a function of the applied DAC code is presented in Figure 8.6.

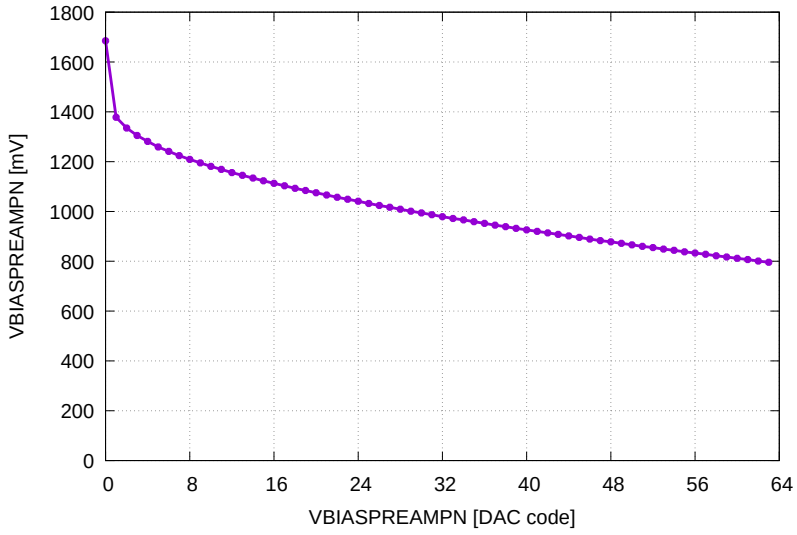


Figure 8.6 Measured voltage level at the output of the preamplifier bias current DAC.

A dedicated slow control register, described in Section 7.3.1, is used to control a set of current mirrors in order to adjust the range of the DACs. Figure 8.7 presents the measured voltage level at the output of the threshold voltage DAC, for different values of this range tuning. As expected, adjusting the DAC range has an effect on the linearity of the DAC in higher codes.

8.5 Matrix equalisation

As introduced in Chapter 7, each analog front-end in the CLICTD matrix comprises a 3-bit DAC for local threshold tuning. This DAC is used to tune the discriminator current in order to compensate for pixel-to-pixel baseline variations. The baseline is extracted by scanning the threshold DAC while measuring the number of detected noise hits and then finding the

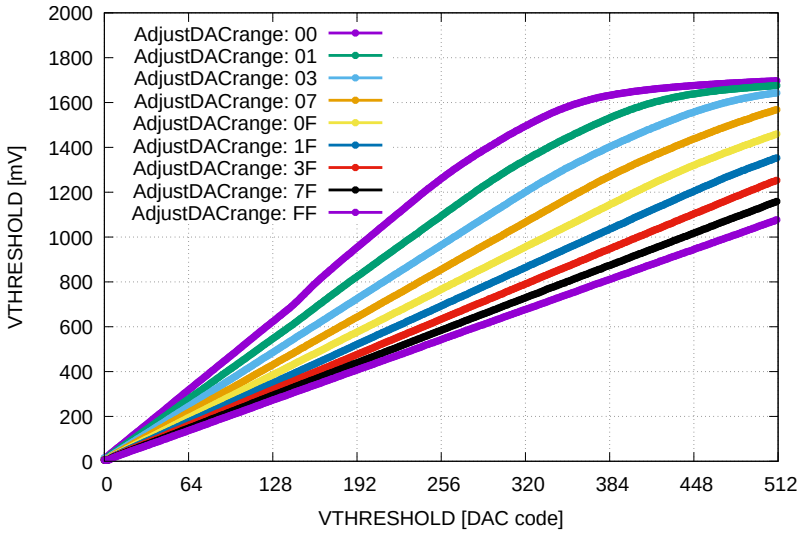


Figure 8.7 Measured voltage level at the output of the threshold voltage DAC, for different values of the adjustable DAC range.

threshold DAC code which corresponds to the mean of the measured Gaussian. The threshold scan was performed for minimum and maximum values of the local threshold tuning DAC for all pixels. Following a linear interpolation of the measured threshold for each pixel, the local threshold tuning DAC code was selected for each front-end such that the threshold dispersion over the matrix is minimised. In addition, in order to equalise the CLICTD matrix at a sub-pixel basis, the above steps were repeated eight times, each time masking all but one of the eight front-ends in the CLICTD detecting channel.

Figure 8.8 presents the obtained threshold scan for minimum ("0") and maximum ("7") tuning DAC code for all pixels before equalisation (blue and red curves respectively). The threshold scan after selecting the tuning DAC code for which the matrix is equalised is plotted in green in the same figure. The threshold dispersion before equalisation is between ~ 6 (minimum tuning DAC code) and ~ 7 (maximum tuning DAC code) threshold DAC codes, while after matrix equalisation the threshold dispersion is reduced to 1.6 threshold DAC codes. As will be described in Section 8.6, each threshold DAC code has been extracted to correspond to ~ 16 e^-. Therefore, the threshold dispersion for the equalised matrix is about 25 e^-.

During the threshold scans, the noise RMS for each pixel in the CLICTD matrix was extracted. The histogram of the per pixel noise RMS, in threshold DAC codes, is presented in Figure 8.9. The mean value of the pixel noise RMS over the CLICTD matrix is 0.8 threshold DAC codes or about 13 e^-.

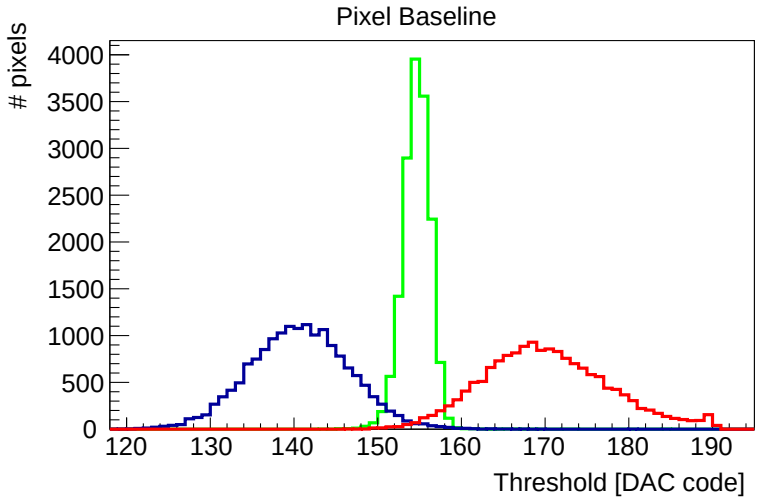


Figure 8.8 CLICTD threshold scan for minimum (blue), maximum (red) and equalised (green) local threshold tuning DAC code.

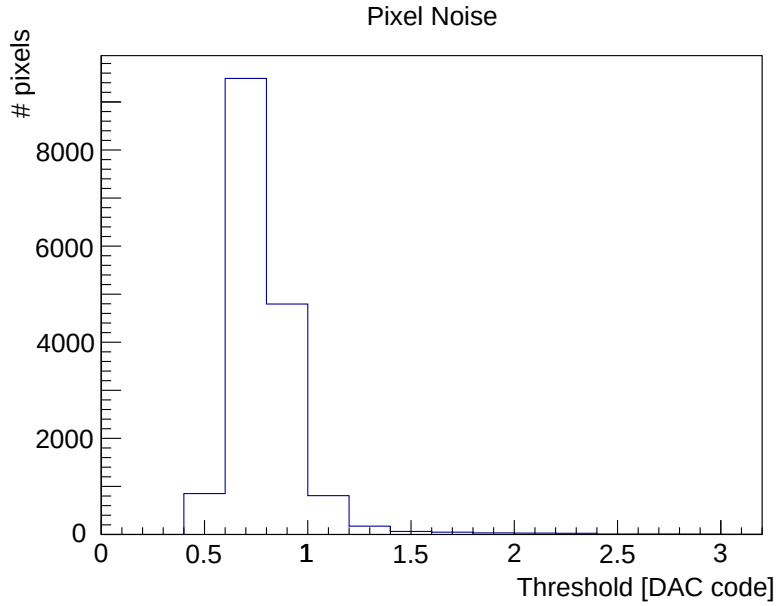


Figure 8.9 Histogram of noise RMS per pixel for the CLICTD chip, measured in threshold DAC codes.

8.6 Measurements with radiation sources

The CLICTD measurement setup was placed inside an X-ray machine in order to measure the fluorescence from iron and copper targets with the CLICTD chip. For this measurement, the CLICTD chip was operated in photon counting mode, the threshold was scanned while the X-rays were on and the value of the on-pixel counters was read out for each threshold. The fluorescence spectra for the iron and copper targets were then obtained from the derivative of the resulting occupancy curve. As illustrated in Figure 8.10, the K_α peak for iron (6.4 keV) is observed at a threshold DAC code of 260 (red curve) and the K_α peak for copper (8.04 keV) at a threshold DAC code of 287 (blue curve). Based on this measurement, the conversion factor from threshold DAC codes to electrons is $\sim 16\ e^-$ per threshold DAC step.

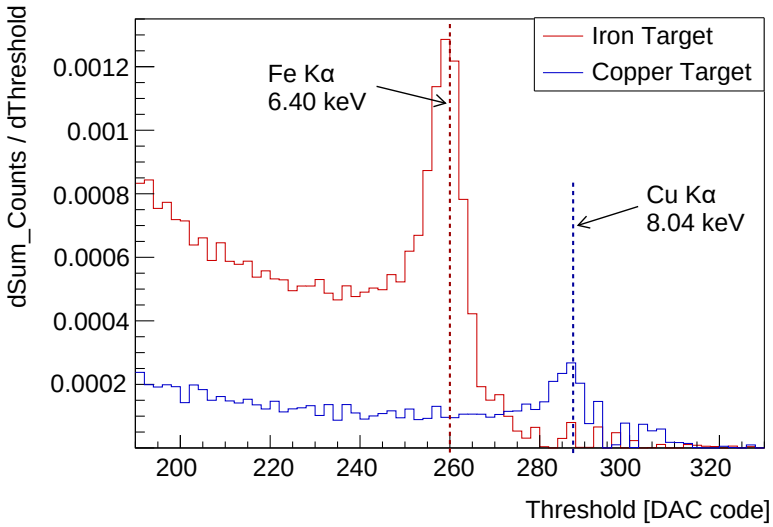


Figure 8.10 Fluorescence spectra using iron (red) and copper (blue) targets, measured with the CLICTD chip.

Taking advantage of the segmented detecting channel architecture in the CLICTD chip and the binary hit information per segment, an image of a small item placed between the X-ray tube and the CLICTD chip was recorded. The image of a screw, presented in Figure 8.11, was recorded after acquiring 1000 shutter frames, each lasting 4 ms. The number of frames when each front-end detected at least one particle is accumulated from each front-end resulting in an image with a granularity of $37.5 \times 30\ \mu m^2$.

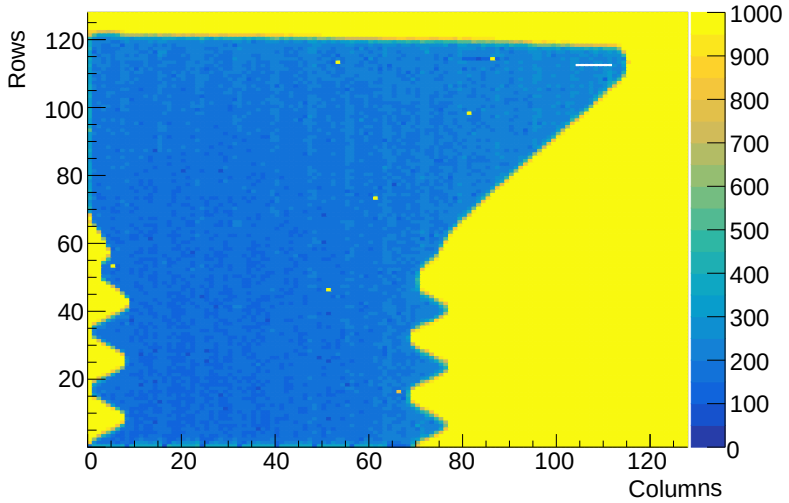


Figure 8.11 X-ray image of a screw, recorded with the CLICTD chip.

8.7 Power consumption

The power consumption of the CLICTD was measured using current monitoring devices on the interface board. After resetting the chip, all biasing DACs are set to their default values and the measured analog power consumption for the pixel matrix is $\sim$170 mW/cm^2. The analog power consumption depends on the operating point of the front-end and can be further optimised after studying the pixel performance. In the digital domain, the power consumption for the pixel matrix is 240 mW/cm^2, dominated by the power required for distributing the clock in the pixel matrix. Therefore, a total of $\sim$410 mW/cm^2 are consumed by the CLICTD matrix. An additional 43 mW are consumed by the analog and digital periphery electronics.

Preliminary estimates for the average power consumption over the cycle of the CLIC accelerator give an average power consumption of $\sim$5 mW/cm^2 for the CLICTD pixel matrix, after the power pulsing scheme is applied. This estimate is extrapolated based on simulations and static measurements for the standby power of the circuit. A duty cycle of 30 µs / 20 ms is assumed for this calculation, in order to give sufficient time for the front-end to be ready to detect particles. As the (analog or digital) periphery electronics are not power pulsed, the 43 mW contribution of the periphery circuitry will be constant, independent of the applied power pulsing.

8.8 Summary and next steps

As presented in the above sections, the CLICTD chip has been produced in two process variants with different geometry for the high resistivity deep N-implant. The first samples from both process variants were wire-bonded on custom designed PCBs and preliminary measurements have been performed, including I-V measurements, DAC scans, and measurements with radiation sources.

The work on characterising the CLICTD chip is on-going. Further, comprehensive, measurements will follow, including characterisation of the front-end performance and beam tests. Results from the chip characterisation will be extensively covered in a future publication.

Chapter 9

Conclusions

In this thesis, the design, implementation and characterisation of two ASICs targeted at the vertex and tracking layers of the CLIC detector was presented.

The first ASIC, presented in Chapters 5 and 6, is the CLICpix Capacitively Coupled Pixel Detector (C3PD). The C3PD chip is designed in the context of the CLIC vertex detector R&D. Based on the monolithic High-Voltage (HV) CMOS technologies, this chip comprises a preamplifier implemented on top of the collection electrode. The charge generated in the sensor is transformed into a voltage pulse. Instead of using the bump-bonding technique, which is widely used in hybrid pixel detectors, a different mechanism is employed to transfer the signal to the readout chip. A thin layer of dielectric glue is applied between the two chips in order to glue them together. The voltage pulse at the output of the C3PD HV-CMOS sensor chip is injected to the capacitance formed by the glue. Thus, the signal is capacitively coupled to the input of the front-end in the readout chip. This capacitive coupling technique offers the advantage of eliminating the cost and complexities of the bump-bonding process.

The C3PD chip contains a matrix of 128×128 square pixels with 25 µm pitch in order to match the dimensions of the pixel matrix in the CLICpix2 readout chip. The ASIC, produced on wafers with different values for the substrate resistivity (20, 80, 200 and 1000 Ωcm), has been successfully operated in laboratory tests with electrical test pulse injection and radiation sources, as well as in beam tests. A summary of the main design parameters and measured values of the C3PD chip is presented in Table 9.1. Analysis of the test beam results from capacitively coupled assemblies with higher substrate resistivity C3PD chips is on-going in order to confirm the expected benefits of the higher substrate resistivity on the sensor performance.

Through the tests performed using assemblies with the C3PD HV-CMOS sensor and the CLICpix2 readout chip, the concept of capacitive coupling was found to suitable for building a low-mass, low-power detector with fast signal collection. In terms of the future perspectives,

different options (such as smaller pixel size) should be investigated in view of the required 3 µm single point resolution, and the glueing process as well as the signal transfer chain can be optimised in order to maximise the efficiency of the capacitively coupled assemblies.

Table 9.1 Summary of the C3PD prototype.

Pixel size	25×25 µm^2
Number of pixels	128×128
Sensitive area	3.2×3.2 mm^2
Total chip size	3.33×4.03 mm^2
Process	180 nm HV-CMOS
Sensor thickness	50 and 250 µm
Substrate resistivity	20, 80, 200 and 1000 Ωcm
Slow control interface	I^{2}C
Charge gain[1]	190 mV/ke$^-$
Noise RMS[1]	40 e$^-$
Rise time[1]	20.8 ns
Leakage current at -60 V (full chip)[1]	40 nA
Breakdown voltage[1]	-69 V
Power consumption (continuous power)	770 mW/cm^2
Power consumption (average over CLIC cycle)	16 mW/cm^2

[1] Averaged over 6 samples with the standard substrate resistivity, measured in standalone mode.

The second ASIC designed in the context of this thesis is a monolithic pixel sensor chip, the CLIC Tracker Detector (CLICTD). The CLICTD chip was implemented in the framework of the CLIC silicon tracker study. A HR-CMOS process with charge collection on a small electrode was selected for this design, as it offers a very small input capacitance and the possibility to integrate on-pixel CMOS logic without coupling to the sensor.

A total of 16×128 elongated pixels is included in the CLICTD matrix, each measuring 300×30 µm^2. To ensure prompt charge collection, each of the pixels is segmented in the long direction into eight collection diodes, each including its own analog front-end (level shifter, voltage amplifier, discriminator and 3-bit DAC for local threshold tuning). The eight discriminated outputs are combined in the on-pixel digital logic, where a simultaneous timing (with 8 bits resolution and 10 ns time binning) and energy (with 5 bits resolution) measurement is performed. A serial readout at 40 MHz is implemented, while the slow control is based on the I^{2}C protocol. Using a process split, two versions of the chip were produced: one with a continuous N-implant on top of the P-type high resistivity epitaxial layer, and one with a gap in the N-implant in the long dimension between neighbouring

collection diodes. Based on simulations, this latter modification is expected to enhance the lateral field and result in a faster collection time for the hits that occur in the region between the collection diodes.

The first, preliminary, results from laboratory measurements with the CLICTD chip were presented. Detailed characterisation of the CLICTD chip is currently on-going. Further laboratory measurements will follow these first functional tests, as well as beam tests to characterise the timing and the efficiency of the chip. These studies will help to evaluate the suitability of this process for the environment of the CLIC silicon tracker, as well as for different particle detection applications.

Table 9.2 Summary of the CLICTD prototype.

Pixel size	300×30 µm^2
Collection diode pitch	37.5×30 µm^2
Number of pixels	16×128
Sensitive area	4.8×3.84 mm^2
Total chip size	5.0×5.0 mm^2
Process	180 nm HR-CMOS
Sensor thickness	300 µm
Slow control interface	I^{2}C
Readout scheme	Shutter based
Data output clock	40 MHz
Data compression	Zero-suppression per pixel
Nominal measurement mode	8-bit ToA + 5-bit ToT
ToA bin size	10 ns
ToT range	$0.6 - 4.8$ µs
Other measurement modes	13-bit ToA / 13-bit photon counting
Gain[1]	550 mV/ke$^-$
Noise RMS[1]	14 e$^-$
Minimum threshold[1]	93 e$^-$
Power consumption (no power pulsing)[2]	410 mW/cm^2 + 43 mW periphery
Power consumption (after power pulsing)[3]	5 mW/cm^2 + 43 mW periphery

[1] Simulated values.
[2] Front-end operating point not optimised.
[3] Value extrapolated from static measurements and simulations.

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Appendix A

PCB Designs

Custom-designed Printed Circuit Boards (PCBs) have been developed in order to perform measurements with the ASICs presented in this thesis once they have been fabricated. The design details of each of the produced PCBs are presented below.

A.1 Board for testing the C3PD chip in standalone tests

Once the C3PD HV-CMOS sensor chip (presented in Chapters 5 and 6) was submitted for fabrication, the design of the PCB started in order to prepare the measurement setup for the chip. The board where the ASIC is mounted on, was designed to be compatible with the uASIC readout system [100]. All signals are therefore routed to a PCI Express connector that fits the one on the uASIC interface board.

A visualisation of the C3PD board, exported from the PCB design software, is presented in Figure A.1. The chip is mounted and wire-bonded on the PCB. A pad-to-pad pitch of 100 µm is used in the C3PD chip, while the pad arrangement enables the use of 100 µm wide tracks with 100 µm separation on the PCB.

Apart from the chip, the board includes the circuits for sampling the amplifier outputs from the monitored cluster of pixels in the C3PD pixel matrix. The amplifier outputs are routed to rail-to-rail operational amplifiers on the PCB and then to connectors where they are sampled with an oscilloscope. The length of the lines routed to the connectors is matched among the different amplifier outputs. A power connector was included on the board to have the option to connect an external power supply in case the amplifiers didn't perform well enough with the supply provided by the uASIC.

Test points are placed on the board, where the power supplies and different digital signals can be probed. All signals required for the operation of the chip are provided by the uASIC readout system.

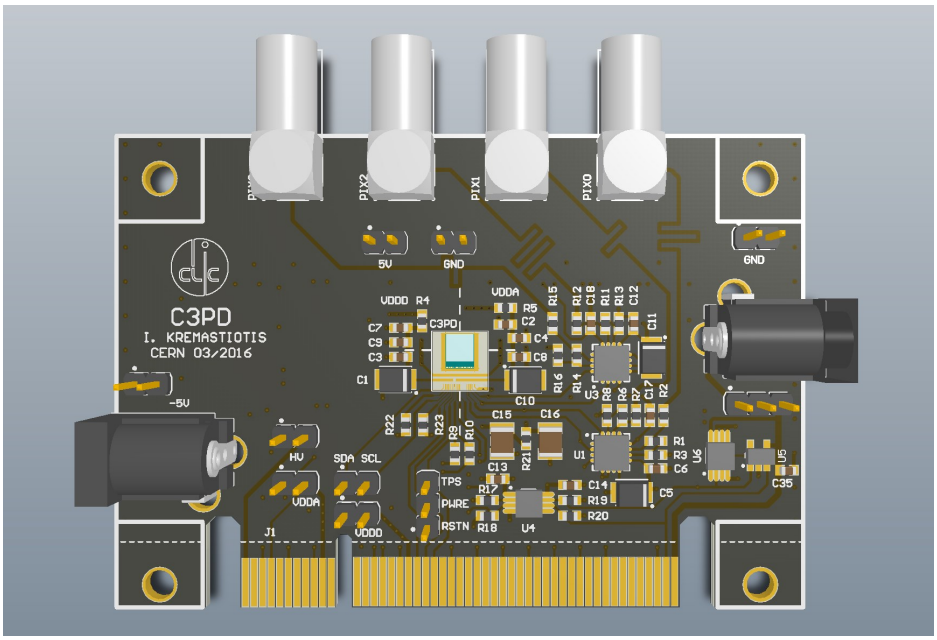

Figure A.1 Visualisation of the PCB designed for testing the C3PD chip in standalone mode.

A photo of the board, with a C3PD sensor chip mounted and wire-bonded on it is presented in Figure A.2.

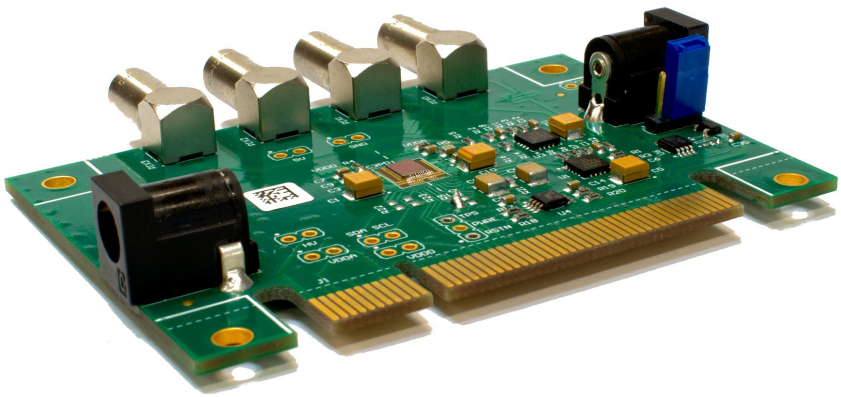

Figure A.2 Photo of the C3PD PCB.

A.2 Board for testing the CLICpix2 and C3PD chips in capacitively coupled assemblies

The capacitively coupled assemblies with the C3PD sensor chip and the CLICpix2 readout chip were tested using the CaRIBOu readout system, as described in Chapter 6. Due to the need for simultaneous operation of the two ASICs, a more complex PCB had to be designed. The PCB for this test is based on two separate boards that are connected together. A visualisation of the design is presented in Figure A.3.

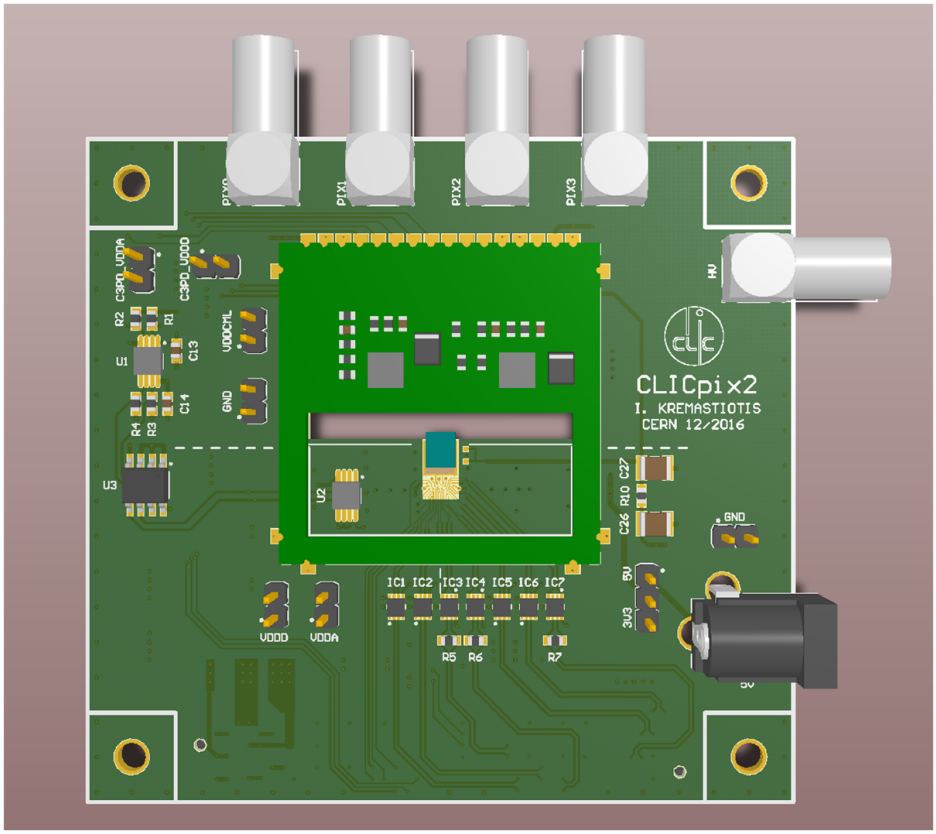

Figure A.3 Visualisation of the PCB designed for testing capacitively coupled assemblies with the CLICpix2 and C3PD chips.

First, the CLICpix2 readout chip is mounted and wire bonded on a custom designed PCB. This PCB is based on a SEAM high-speed, high-density connector in order to match the one on the CaR interface board. Signals such as CMOS lines, differential lines, analog inputs and outputs, as well as power supplies are handled by the interface board. A temperature sensor is placed close to the chip, and dedicated ICs are used to translate the CML outputs of the chip to LVDS pairs such that they are compatible with the readout system (and, accordingly, the LVDS lines from the interface board to CML inputs for the chip). The track width

and separation of the differential lines with selected such that an impedance of 100 Ω is maintained. Further, a level translator for the I^2C bus and connectors for monitoring the C3PD pixel outputs with an oscilloscope are included on this board.

The C3PD sensor chip is glued on top of the readout ASIC and wire bonded on a second, smaller, board which is mounted on the CLICpix2 board. This second board includes the operational amplifiers that drive the monitored pixel outputs to the connectors. All signals are routed to the CLICpix2 board and then to the CaR interface board. This PCB assembly allows a double-sided wire-bonding scheme, making the operation and testing of the two chips at the same time possible. The design was based on the PCB used for capacitively coupled assemblies with the first generation of the CLICpix readout chip [71, 100]. Apart from the measurements with capacitively coupled assemblies, the same PCB was used for testing the CLICpix2 readout chip with planar sensors. Figure A.4 presents a photo of the two PCBs with a capacitively coupled assembly mounted and wire-bonded on them.

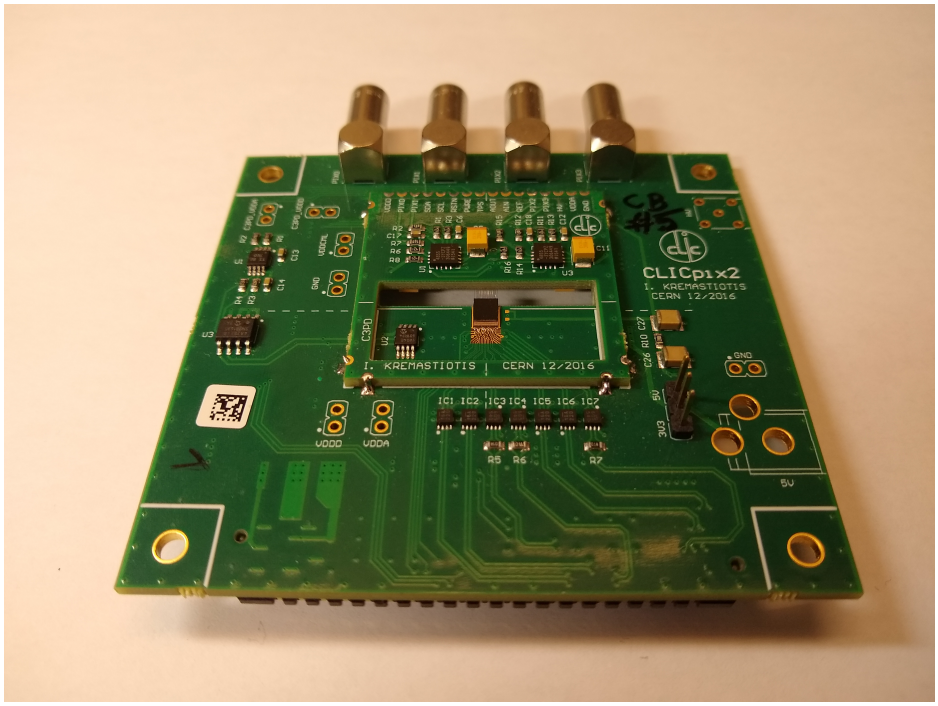

Figure A.4 Photo of the CLICpix2/C3PD PCB.

A.3 Board for testing the CLICTD chip

Similar to the PCB for the CLICpix2 and C3PD assemblies, the custom board for testing the CLICTD chip is designed to be compatible with the CaRIBOu readout system. Same as before, all signals from or to the chip are connected through a SEAM connector. The standard 100 µm track width and separation is kept on the PCB close to the area where the wire-bonds are connected. As the CLICTD chip employs the LVDS standard, no translation is needed and the differential lines can connect directly to the readout system. Figure A.5 presents a visualisation of the board exported from the PCB design software. The board was designed such that it is compatible with the mechanical supports designed for the CLICpix2/C3PD PCB, in order to use the same supports during beam tests.

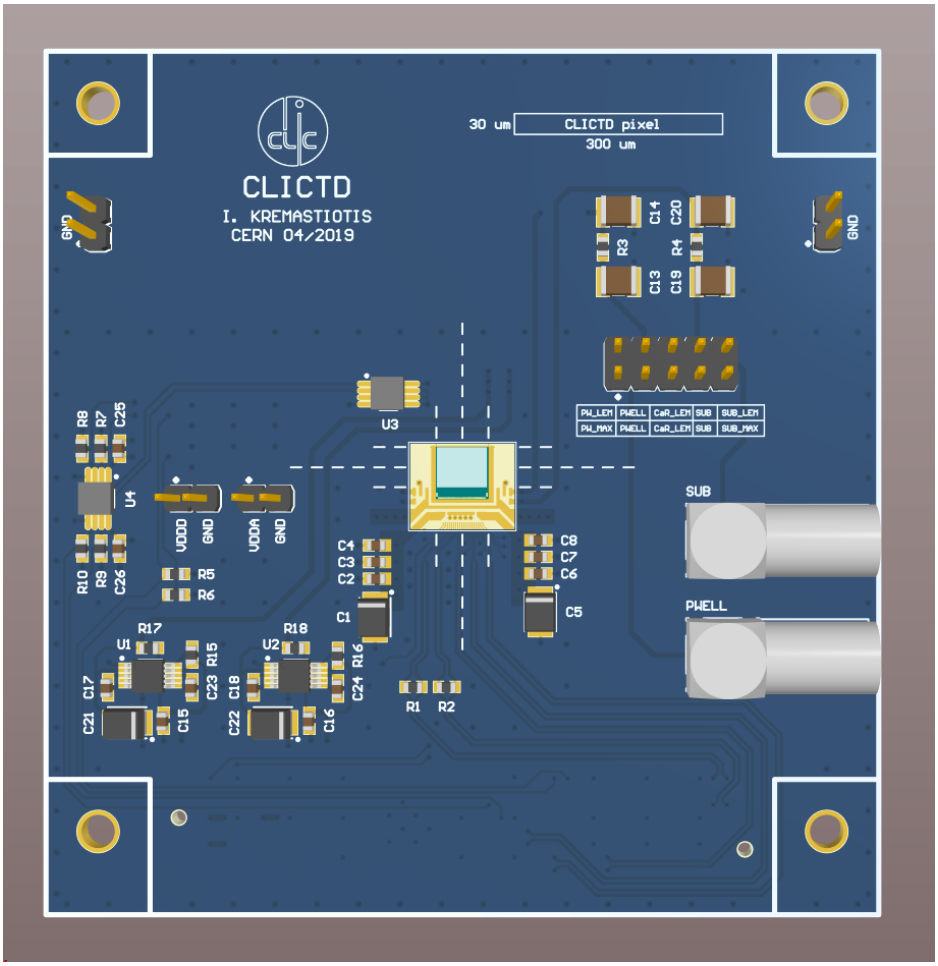

Figure A.5 Visualisation of the PCB designed for testing the CLICTD chip.

The power supplies for the CLICTD chip are provided by the CaR interface board. Two additional power supplies from the interface board are used to generate the two required

reverse bias voltages (the first for the P-well in the CLICTD active area, and the second for the substrate of the chip). For this scope, commercial inverting charge pump circuits are placed on the board in order to generate a negative voltage from the positive voltage supplied by the readout system [114]. The option to connect the reverse bias from external power supplies is also included in order to have the possibility to precisely measure the sensor leakage current and to apply a higher reverse bias voltage. Similar to the other boards, an I^2C level translator and a temperature sensor are included in this design. A photo of the PCB, with a CLICTD sample wire-bonded on it, is presented in Figure A.6.

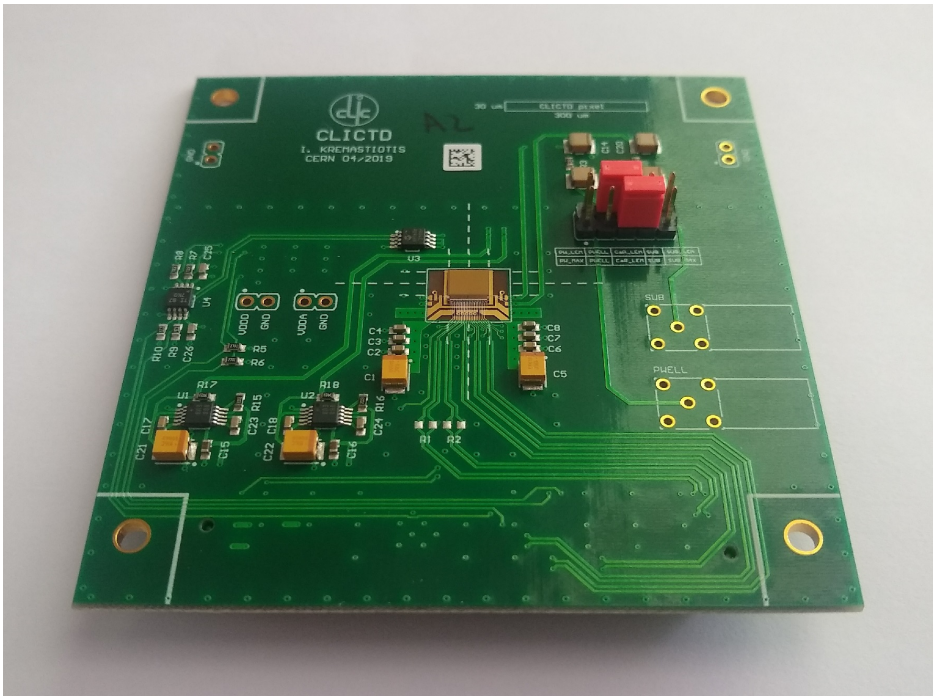

Figure A.6 Photo of the CLICTD PCB.