

Front and Back-Junction Carbon Nanotube-Silicon Solar Cells with an Industrial Architecture

Jianhui Chen,* Daniel D. Tune, Kunpeng Ge, Han Li, and Benjamin S. Flavel*

In the past, the application of carbon nanotube-silicon solar cell technology to industry has been limited by the use of a metallic frame to define an active area in the middle of a silicon wafer. Here, industry standard device geometries are fabricated with a front and back-junction design which allow for the entire wafer to be used as the active area. These are enabled by the use of an intermixed Nafion layer which simultaneously acts as a passivation, antireflective, and physical blocking layer as well as a nanotube dopant. This leads to the formation of a hybrid nanotube/Nafion passivated charge selective contact, and solar cells with active areas of 1–16 cm² are fabricated. Record maximum power conversion efficiencies of 15.2% and 18.9% are reported for front and back-junction devices for 1 and 3 cm² active areas, respectively. By placing the nanotube film on the rear of the device in a back-junction architecture, many of the design-related challenges for carbon nanotube silicon solar cells are addressed and their future applications to industrialized processes are discussed.

1. Introduction

Carbon nanotube-silicon solar cells are a niche field of photovoltaics and consist of a thin carbon nanotube (CNT) film interfaced with a silicon substrate.^[1] Incident light mostly passes through the CNT film and is absorbed by the silicon base to create excited electron–hole pairs. These diffuse to the CNT:Si junction and are separated by an electric field in this region that is established due to the built-in potential between the two materials. For a solar cell constructed with p-type nanotubes/

n-type silicon (or n-type nanotubes/p-type silicon), the holes (electrons) are collected by the nanotubes and the electrons (holes) by the silicon. In the past, CNT:Si solar cells have been fabricated with the use of a metallic frame with an active area in its middle. This has been achieved via etching of an insulating layer such as SiO₂ on silicon followed by coating of the SiO₂ with metal (Cr/Au, Ti/Pt, Ag) and finally the placement of a CNT film on top. In this way, the CNT film is contacted by the metal top contact at its edges.^[2–6] With this architecture device power conversion efficiency (PCE) has steadily increased over the past decade from the preliminary work of Wei et al.,^[7] who reported 1.4% for a 0.49 cm² active area, to works from Jia et al.,^[2] Shi et al.,^[8] and the team around Maruyama,^[9] reporting 13.8%, 15.1%, and 14.1%, respectively, for ≈0.01 cm²

active areas. Notably, in 2014 Wang et al.^[10] reported a power conversion efficiency of 17% but over an area of 0.008 cm², and in 2019 Wu et al.^[11] achieved 16.2% for 0.81 cm². In our most recent work, we communicated the attainment of 17.2% and 15.5% for 1 and 5 cm² active areas, respectively.^[12] This advance was possible due to the use of a textured antireflective silicon surface and a Nafion layer which acted as an antireflective coating and nanotube dopant. Nafion is proving to be a promising dopant for carbon systems and was originally demonstrated for graphene and carbon nanotubes by Kwon et al.^[13] and Jeon et al.,^[14] respectively, and recently, Maruyama and co-workers also demonstrated the use of Nafion in CNT:Si solar cells and reported a PCE of 14.4% for an area of 0.09 cm².^[15]

The device performance of CNT:Si solar cells made with a metallic frame on the front of the device is strongly coupled to a tradeoff between optical transparency and electrical conductivity of the nanotube film and this is described by the σ_{DC}/σ_{OP} figure of merit of Hu et al.^[16] The CNT film should be as thin as possible to maximize light absorption by the silicon and avoid parasitic current losses while providing a low resistance pathway for the excited carriers to reach the nearest metallic contact. Toward this goal, both structural and chemical strategies have been employed in the literature. Chemical dopants such as SOCl₂,^[17] AuCl₃,^[6,18] HNO₃,^[19] metallocenes,^[20] and chlorosulfonic acid (CSA)^[21] have all been shown to dramatically reduce the sheet resistance of the film and simultaneously bleach the optical transitions of the CNTs to improve transmittance. Alternatively, Cui et al.^[4] prepared a CNT film consisting

Dr. J. Chen, Dr. D. D. Tune, Dr. H. Li, Dr. B. S. Flavel
Institute of Nanotechnology
Karlsruhe Institute of Technology
Karlsruhe 76131, Germany
E-mail: benjamin.flavel@kit.edu

Dr. J. Chen, K. Ge
Hebei Key Lab of Optic-Electronic Information and Materials
College of Physics Science and Technology
Hebei University
Baoding 071002, China
E-mail: chenjianhui@hbu.edu.cn

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of microscale hexagons comprising highly densified nanotube forests surrounding regions of much thinner surface coverage and Xu et al.^[22] produced cells with contact fingers made from thin strips of CNTs overlaid onto much thinner CNT films. The latter two examples have the advantage of being long-term stable, but the use of CNTs contact fingers, which have a higher inherent resistivity compared to commonly used noble metals, or indeed the use of a metallic frame as a top contact will always lead to problems during active area scale-up. In these designs, the distance a carrier has to travel between generation and collection at a metal contact is unavoidably increased as the active area increases. Recently, Harris et al.^[6] and Yu et al.^[23] used a metallic grid to realize active areas of 0.1 and 0.49 cm². Likewise, a metallic grid was used in our most recent work to obtain active areas up to 5 cm².^[12] For such a solar cell design, despite the overall active area being large (5 cm²) the reported area was the sum of many smaller subcells within a lithographically patterned insulating frame (SiO₂) coated by a metallic overlayer.

To date, the approach of using a lithographically defined active area, either singularly or in a grid array, has been exclusively used by the CNT:Si solar cell field, but it is in stark contrast to industry standards for silicon photovoltaics. The development of CNT:Si solar cells is limited by this design for several reasons: 1) The requirement of a central active area implies a large ineffective area from which no light is harvested, where the SiO₂ frame and fingers increase the nonjunction region and reduces the effective junction area; 2) Technological complexities and lithography are required in the fabrication process to define the insulating SiO₂ frame; 3) A wet chemical process (HF etching) is a basic prerequisite for high-efficiency crystalline Si (c-Si) solar cells,^[24] but this cannot be performed without removing the SiO₂ frame. In industrial designs, metallic contact fingers are directly deposited onto the emitter layer (which would be the CNTs in this case), and the pitch, thickness, and length of the fingers can readily be adjusted for increased active area. In industry, the entire wafer normally defines the active area, whereas for research grade CNT:Si designs, a large substrate is required to define the active area but this is only a small region in the middle. Using an industrial design, Si-wafer-based solar cells are approaching PCEs of 26.7%^[25] and these benefit from phosphorus/boron-doped Si bulk, doped thin film carrier-selective contact materials, back-contact architectures, and high-quality surface passivation schemes.^[26] For n-type solar cells, near-surface p⁺ emitter regions are commonly formed by boron diffusion at high temperature (≈900 °C),^[27] followed by passivation with SiO₂ or Al₂O₃ and SiN_x. Additionally, plasma enhanced chemical vapor deposition (PECVD) techniques have been developed to produce ultrathin hydrogenated amorphous Si (a-Si:H) films with dual function as a carrier-selective contact and interface passivation layer.^[28] However, these approaches are technologically complex and contribute significantly to the final solar cell price. It is for this reason that researchers have begun to develop “dopant-free carrier-selective heterocontacts.”^[29]

Recently, dopant-free hole-selective contacts, such as transition metal oxides^[30] and conductive polymers such as poly(3,4-ethylenedioxythiophene) (PEDOT)^[31] have been used in high-efficiency industrial architectures and represent a burgeoning field of silicon photovoltaics. Alternatively, researchers have looked toward new nanomaterials for silicon-based solar

cells. Here, the situation is similar to the CNT:Si field, in which initial proof-of-principle devices are shown with metallic frame like architectures, but the PCE does not scale well with increasing active area. In recent examples, MoS₂ and graphene have been used as a top contact and PCE values of 5.6% (1 cm²) and 14.6% (0.07 cm²), respectively, were reported.^[32] In the case of the graphene device, the PCE fell to 8.6% when the active area was scaled to 1 cm². On the other hand, Zheng et al.^[33] built a tandem solar cell using a perovskite and demonstrated a PCE of 20.5% (4 cm²), which reduced to 17.1% (16 cm²) upon scale-up. A similar situation has been found for single-junction perovskite solar cells in the work by Abuhelaiqa et al.,^[34] who reported a PCE of 21.4% for 0.16 cm² and 16.7% for 15 cm². Indeed, the scale-up of photovoltaic technologies is a general challenge and applies broadly to silicon, perovskite,^[35] organic^[36] and dye-sensitized^[37] solar cells.

In principle, CNT films form a “carrier-selective” interface with c-Si, and have the advantage of having tunable (chirality dependent) band structures, excellent photoelectrical properties, and are solution processable.^[38] The inability to apply industry approaches to CNT:Si solar cells is related to the porous nature of a thin CNT film such that direct deposition of contact fingers onto the film would result in metal reaching the underlying silicon surface. In this work, we show that a conductive CNT network incorporated by an insulating Nafion polymer matrix not only does not affect the sheet resistance of the CNT film, but also can form an effective physical blocking layer to prevent the direct contact of metal to the silicon at the CNT:Si interface. In this way, industrial architectures, including front and back-contact geometries, on silicon wafers typically used in the Si PV industry, with a passivated back- (BSF) and front- (FSF) surface field and a textured front surface, are applied to CNT:Si solar cells. Additionally, the back-junction design for CNT:Si solar cells introduces a new way to utilize CNTs which is not limited by the sheet resistance or transmittance of the nanotube film, and this results in record high efficiency across large areas. We demonstrate that the CNT:Si solar cell concept can be applied in an industrially compatible way and prepare front and back-junction solar cells with scalable active areas ranging from 1 to 16 cm² and PCEs of 18.9–15.2%. These are the largest CNT:Si solar cells with largest active area reported to date.

2. Results and Discussion

Figure 1a depicts the design of both front and back-junction solar cells on n-type silicon. The front-junction cell is most familiar to the CNT:Si solar cell community and consists of a silver backing electrode followed by a n⁺ BSF region that was passivated by a 80 nm silicon nitride layer. Through firing of a finger array formed by a screen-printed silver paste, local silver contacts were made between the n⁺ BSF region and the silver backing. The front side is textured with random pyramids (RPs), coated with a CNT film and infiltrated with a thin layer of Nafion before evaporating the top silver contact fingers. In relation to previous front-junction CNT:Si solar cells, the defining difference here is that there is no insulating frame and the top contact is deposited directly onto the CNT/Nafion layer. This is an important difference separating research grade solar cells

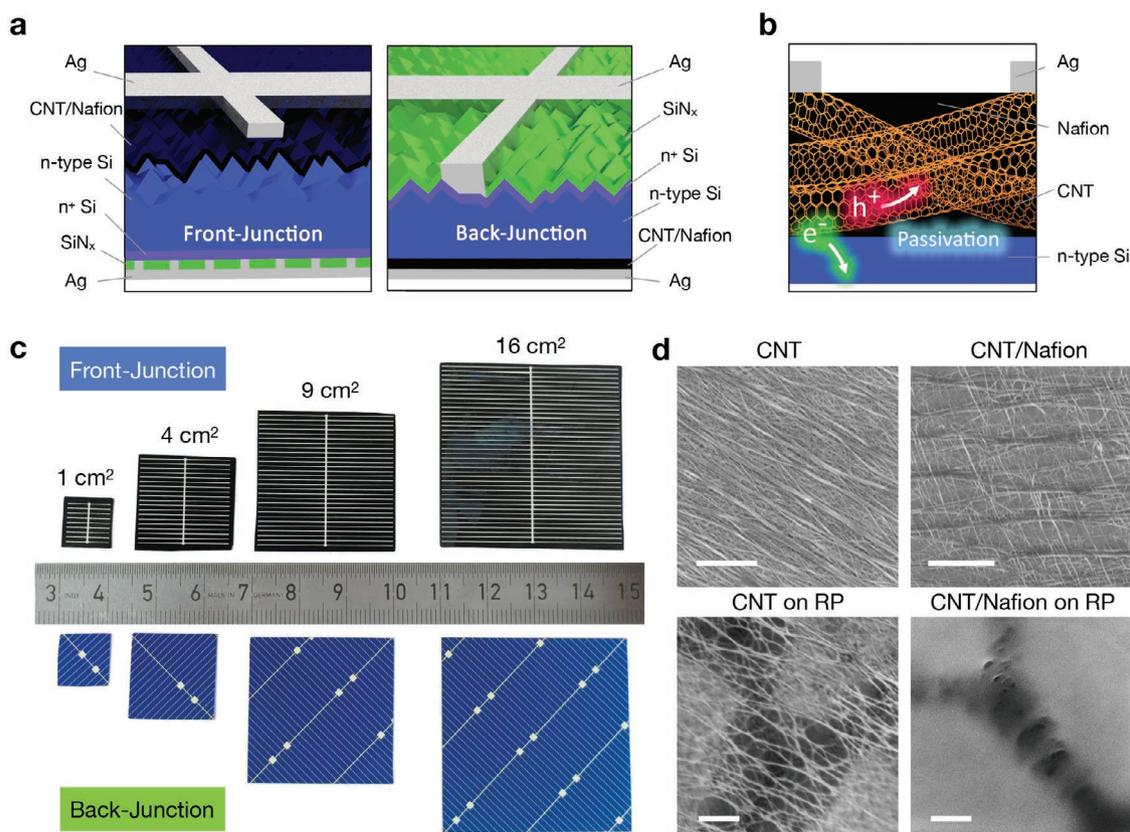


Figure 1. a) Cross-sectional schematic of the front and back-junction carbon nanotube-silicon solar cell design. b) Schematic of hybrid PCSC operation: Electrons are collected by the silicon and holes by the nanotubes, the holes then traverse the nanotubes to a silver contact, which for a front-junction cell is a finger array (as depicted) and for a back-junction cell is a full contact electrode. The nanoscale exposed regions of silicon are passivated by Nafion. c) Solar cells with an active area of 1–16 cm² showing the top contact design for the front and back-junction architectures. d) Scanning electron microscopy images of carbon nanotube films on polished silicon and random pyramid (RP) textured silicon with and without Nafion.

from an industrially relevant architecture for which the active area can easily be scaled up. Figure S1 (Supporting Information) provides a further schematic comparison of the CNT:Si silicon solar cell architecture used in the past to those used in industry and in this current work. For a back-junction solar cell, the layer stack is essentially reversed and the CNT/Nafion layer is deposited directly onto the back of the n-type silicon wafer before evaporating a full contact rear silver electrode. In this design, instead of the CNT film, a n⁺ FSF is diffused into the random pyramids and passivated by 80 nm silicon nitride. The top electrode is formed by screen-printed silver paste placed directly on the silicon nitride with through-fired silver contacts. As shown in Figure 1c, the design of both architectures is highly scalable, only requiring an increase in the number of top contact fingers, and solar cells with active areas of 1–16 cm² were fabricated. Figure 1b shows a schematic of the passivated charge selective contact (PCSC) principle for both front and back-junction solar cells. It consists of two interfacial regions: a) a region in which carbon nanotubes contact silicon and are responsible for exciton dissociation and transport; b) nanoscale silicon areas passivated by Nafion. This concept provides a carrier-selective contact with defect state passivation on the nanoscale level required for low-dimensional material based Si solar cells such as CNT:Si.

Nafion forms a physical blocking layer to prevent the direct contact of silver to the silicon at the CNT:Si interface. Nafion

infiltrates the porous nanotube film and covers any bare areas of silicon that would otherwise have been exposed to air and coated in metal during electrode deposition. Figure 1d provides scanning electron microscopy (SEM) images of this process for CNT films deposited on a flat silicon and an RP textured surface. Further SEM images can be found in Figure S2 (Supporting Information). The CNTs have a general alignment corresponding to the direction of shear used in their manufacture.^[39] Further information pertaining to the optimization of the nanotube film thickness and its composition can be found in previous work by Tune et al.^[12] After Nafion it can be seen that the films become uniform, closed, and coated in an organic layer. However, the CNTs in the upper most portion of the film remain visible and it is these which are later contacted by the silver electrode. Despite Nafion being an insulator, the sheet resistance of the CNT film is essentially unchanged (Figure 2a and Figure S3, Supporting Information). Notably, the transmittance of the CNT film is improved after Nafion coating due to its wide bandgap, low refractive index ($n = 1.35\text{--}1.38$), and low extinction coefficient ($k < 0.004$) between 245 and 826 nm (Figure S4, Supporting Information). Typically, mean sheet resistances of 376 ± 113 and $360 \pm 104 \Omega \text{ sq}^{-1}$ are measured for the CNT and CNT/Nafion films, respectively. As shown in Figure S2 (Supporting Information), this resulted in a $\sigma_{\text{DC}}/\sigma_{\text{OP}}$ value of 4.3 for the CNT/Nafion film. This suggests that good electrical contact is made to the uppermost

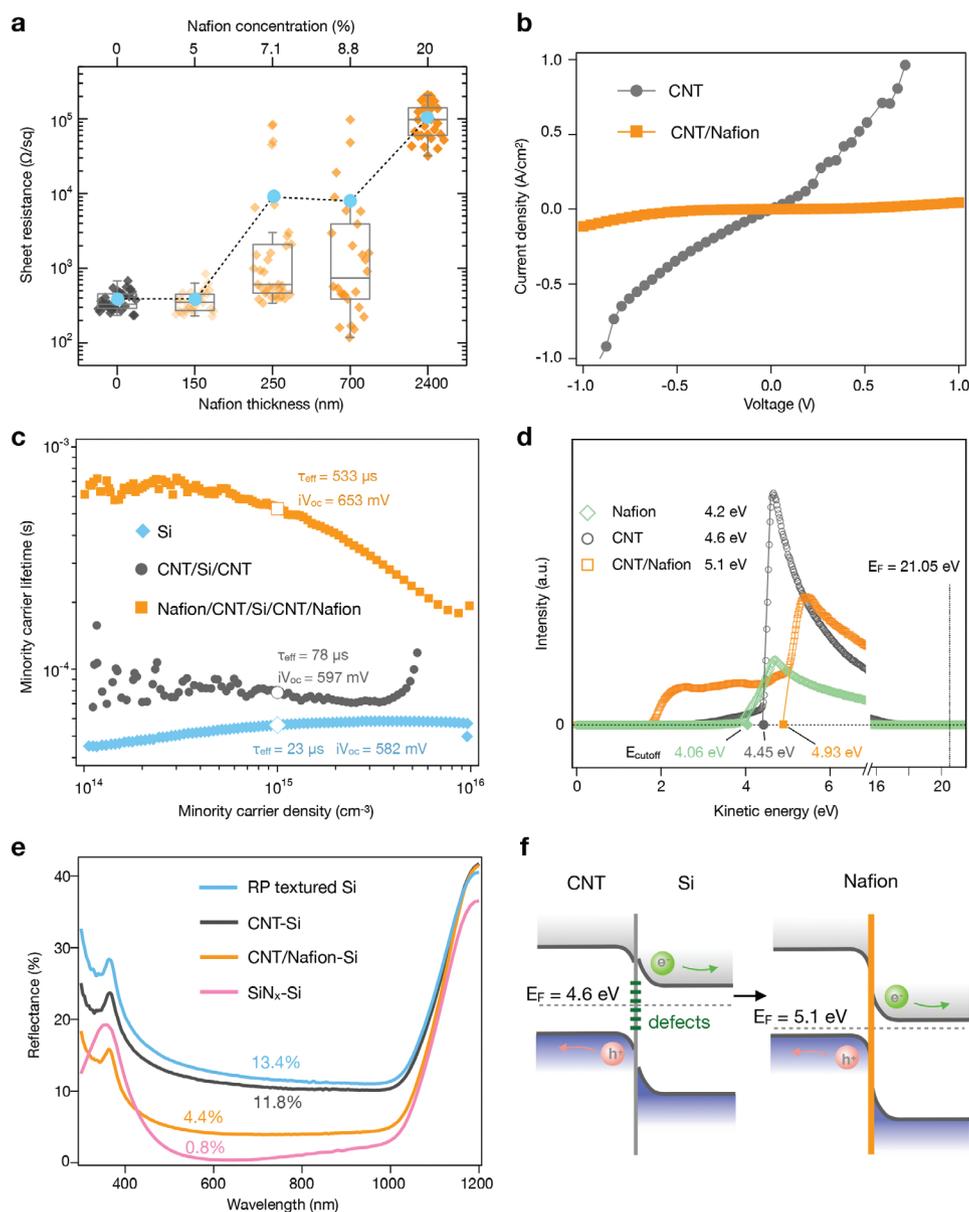


Figure 2. a) Sheet resistance of a CNT/Nafion film with increasing Nafion thickness, the mean values are indicated by a blue circle. b) J - V curves from two top contacted silver pads; one on the silicon surface and the other on a region containing only CNTs or a CNT/Nafion film. c) Transient photoconductance decay measurements of CNT films on silicon with and without Nafion. d) Ultraviolet photoelectron spectroscopy of a Nafion, CNT and CNT/Nafion film. The calculated Fermi level (E_F) is shown in the legend. e) Reflectance spectra of the various light side coatings used for the front and back-junction devices. f) Predicted band alignment at the CNT:Si interface after coating with Nafion. In the interests of simplicity, only the frontier orbitals of the largest diameter semiconducting CNTs in the mixture are shown.

CNTs and that sheet resistance is primarily determined by the nanotube:nanotube junctions within the film. It also implies that there is a maximum Nafion thickness after which all CNTs are coated. In Figure 2a, the concentration of Nafion used in spin-coating and thereby the thickness of the layer was varied. For thicknesses larger than 150 nm, it can be seen that the mean sheet resistance (blue circle) increases relative to the uncoated CNT film and that there is a larger spread of the data (8.8 ± 21.8 to $105 \pm 54 \text{ k}\Omega \text{ sq}^{-1}$). This is due to inhomogeneities in the number of exposed CNTs as the Nafion layer approaches full coverage. In all proceeding measurements, a 150 nm Nafion coating

was used and the thickness of the CNTs film was the same for both front and back-junction devices. Figure 2b highlights the ability of Nafion to prevent silver deposition onto the silicon surface by comparing current density–voltage (J - V) curves made with two top contacted silver pads, one on the silicon surface and the other on a region containing a CNT only or CNT/Nafion film. An almost linear increase in current with voltage for the CNT film alone is a clear indication of silver penetration through the film and onto the silicon. In the past, this has restricted CNT:Si solar cells with a metallic frame and a central active area, but is resolved with the use of Nafion.

In addition to filling the void space within the nanotube film, Nafion was also found to have a surface passivation effect. Using the technique of the quasi steady-state and transient photoconductance decay (PCD), the minority carrier lifetimes for silicon wafers coated symmetrically with a CNT film or a CNT/Nafion film were measured and are shown in Figure 2c. Relative to the silicon alone, the CNTs were found to slightly increase the effective carrier lifetime (τ_{eff}) from 23 to 78 μs , but after the deposition of Nafion this increased to 533 μs . For comparison, τ_{eff} for Nafion alone is 1975 μs . This suggests that the nanotubes remain in close contact with the silicon after Nafion coating and that only the nanoscale, uncoated, silicon regions are passivated. As discussed by Chen et al.,^[40] an electrochemical mechanism involving the oxygen in the sulfonic functional group of Nafion is responsible for passivation. Oxygen grafts to the dangling bonds on the Si surface to fill defects states. Additionally, PCD measurements allow for the implied V_{oc} (iV_{oc}), which is the energetic distance between the electron and hole quasi-Fermi levels, to be calculated by Equation (1)^[41]

$$iV_{\text{oc}} = \frac{kT}{q} \ln \left(\frac{\Delta n (\Delta n + N_{\text{D}})}{n_i^2} \right) \quad (1)$$

where Δn is the excess carrier density, n_i is the intrinsic carrier concentration, and N_{D} is the effective bulk donor concentration. Upon the deposition of a CNT film, the iV_{oc} rose slightly from 582 to 597 mV, but after Nafion coating this increased to 653 mV. As shown in Figure S5 (Supporting Information), the surface passivation afforded by Nafion when exposed to ambient conditions was found to be stable for the period of hours required for device fabrication and measurement, but began to slowly degrade over a period of several days. Ultraviolet photoelectron spectroscopy measurements in Figure 2d show that Nafion additionally acts to dope the CNT film. By taking the inelastic electron cutoff energy (E_{cutoff}) and the Fermi level (E_{F}) of the corresponding Au calibration, the E_{F} of a CNT/Nafion film was determined to be 5.1 eV using Equation (2)^[42]

$$\phi = h\nu - (E_{\text{F}} - E_{\text{cutoff}}) \quad (2)$$

For comparison, the CNT film prior to Nafion coating had an E_{F} of 4.6 eV. As shown previously,^[5,43] the use of CSA dispersed CNT inks for film manufacture also has a doping effect on the nanotubes and this is confirmed by absorption spectroscopy in Figure S6 (Supporting Information). Interestingly, the combination of CNTs with Nafion results in the emergence of an additional peak with an E_{cutoff} of 1.72 eV and corresponding E_{F} of 1.9 eV. At this stage, the origin of this effect is unclear, but it is only present for the CNT/Nafion hybrid system and we speculate that it may be due to nonuniform doping of the inner and outer walls of the double-walled CNTs used in the film. Finally, as shown by other researchers,^[44] Nafion acts as an antireflective coating to improve light absorption by the silicon base. Figure 2e shows reflectance (R) spectra of a RP textured silicon substrate before and after CNT film deposition and finally after subsequent Nafion coating. These had $(1-R)_{550}$ values of 86.6%, 88.2%, and 95.6%, respectively. In combination, the results of Figure 2c–e lead us to draw the band structure diagram of the CNT:Si interface shown in Figure 2f. Nafion not only passivates

any surface defect states and dangling bonds on silicon, but it also further enhances the band bending at the interface and the overall number of excitons generated in the silicon.

J - V , external (EQE) and internal (IQE) quantum efficiency curves for front and back-junction solar cells are shown in Figure 3a,b, respectively. Notably, the measured V_{oc} of 624–638 mV closely match the measured iV_{oc} of 653 mV, indicating effective surface passivation afforded by the CNT/Nafion PCSC. This is comparable to previous literature devices with V_{oc} of <600 mV.^[9,10,22,45,46] Additional performance data for 60 front and 70 back-junction devices can be found in Figure S7 (Supporting Information), where a high level of reproducibility for the proposed system can be seen. Devices consisting of Nafion alone can be found in Figure S8 (Supporting Information). For a 1 cm^2 area front junction, the PCE was 15.2% and for a 3 cm^2 back junction the PCE was 18.9%. When the active area was scaled to 16 cm^2 the PCE was found to drop to 8.8% (front) and 17% (back). The large decrease in PCE for the front junction is predominately due to a reduced fill factor (43.1% for 16 cm^2 compared to 65.2% for 1 cm^2) and is related to the necessity of holes, once dissociated, to laterally traverse the carbon nanotube network before reaching a silver contact. This is a process that is highly susceptible to the sheet resistance of the CNT film, scattering sites within it, and the distance to a metallic contact. On the other hand, the back junction is far less susceptible to these variations. In a back-junction design, the holes at the CNT:Si interface are immediately transferred to the back electrode and FF is not reliant upon the initial lateral diffusion of holes. A back-junction design also has the additional advantage of having a highly transparent silicon nitride layer on the front. In a front-junction design, a portion of the incident light will always be absorbed by the CNT film and one is forced to balance decreases in sheet resistance with increased absorbance. As shown in Figure 2e, silicon nitride has a $(1-R)_{550}$ of 99.2%, such that more incident photons reach the silicon base.

The EQE curves for front and back-junction devices were found to be highly flat across most of the wavelength range. In particular, EQE for the front junction remained above 85% between 470 and 1000 nm. This surpasses all previous work reporting an EQE value of <70% at 1000 nm.^[10,45,47] The high QE is a result of complete coverage of the textured Si wafer with CNTs and the excellent antireflection properties of Nafion. Using EQE and $1-R$ data, IQE was calculated and it can be seen that EQE and IQE for the front junction are slightly separated. This indicates that there are J_{sc} losses, presumably because the antireflection properties of the CNT/Nafion layer are less than perfect. For back-junction devices, the near-perfect antireflection properties of SiN_x thin film result in a higher EQE of >90% at 490–920 nm. In this case, EQE and IQE are almost overlaid on top of each other suggesting that all light absorbed is converted into current. In both the front and back-junction cells, the EQE and $1-R$ curves are offset from each other, indicative of parasitic absorption and recombination losses, which mainly come from the CNT films and highly doped n^+ FSF.

Insights into the role of Nafion at the CNT:Si interface can be gained by further analysis of the completed solar cells. Here, it is irrelevant if a front or back junction is measured and Figure 4 provides an example for a front-junction device with and without Nafion. Firstly, in Figure 4a it can be seen that

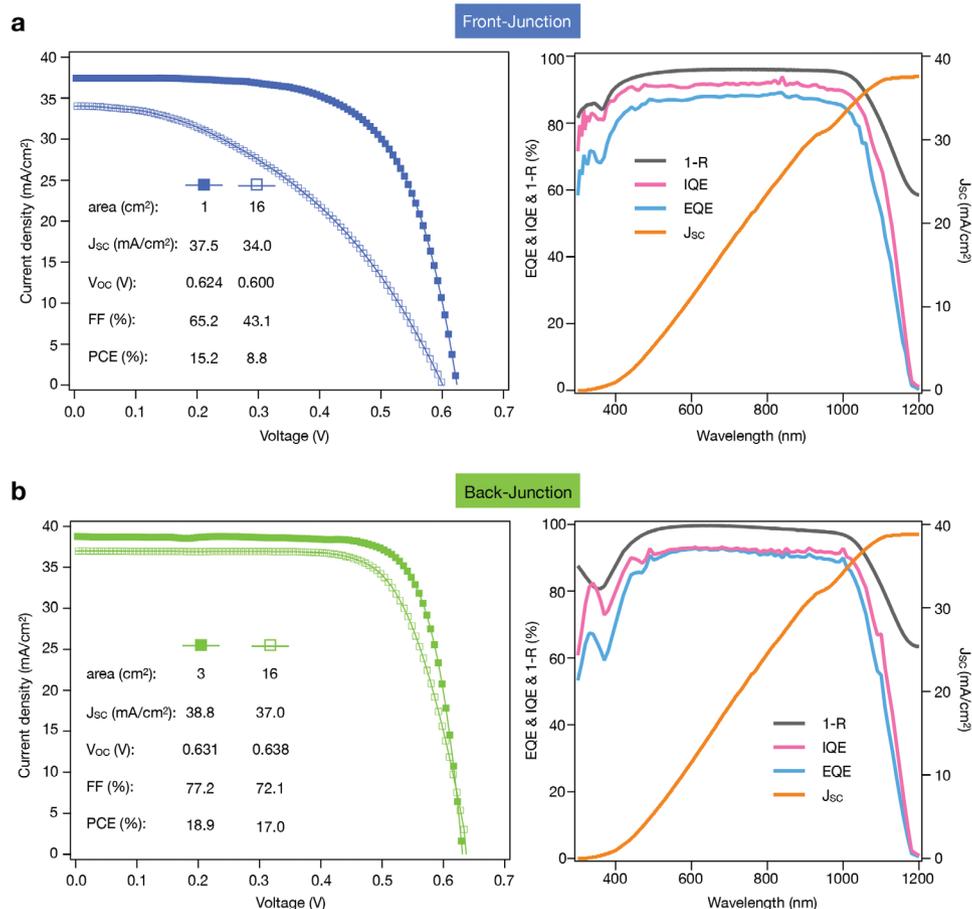


Figure 3. a,b) J - V , EQE, IQE, and integrated J_{sc} data for champion front and back-junction solar cells with device parameters provided as an inset.

the photovoltaic performance of the cell without Nafion (J_{sc} : 16.0 mA cm⁻², V_{oc} : 0.327 V, FF: 31%, PCE: 1.6%) was considerably worse than with Nafion (J_{sc} : 37.9 mA cm⁻², V_{oc} : 0.610 V, FF: 63.2%, PCE: 14.6%). In agreement with Figure 2b, this is due to ineffective separation of the top metal contact from the CNT:Si interface. Nanoscale silicon regions are contacted with metal and a metal-semiconductor junction is formed within CNT:Si heterojunction. This leads to a pinning of defect states within the bandgap and current leakage. Log J - V curves in the dark in Figure 4b show that current leakage is suppressed significantly after the introduction of Nafion. As discussed by others in the field, the physics surrounding the CNT:Si heterojunction is complex and has not been found to fit conventional models.^[5,6] Nevertheless, we tentatively use thermionic emission theory to calculate the ideality factor and Equation (3) to calculate the Schottky barrier height (ϕ_B)^[48]

$$\phi_B = \frac{kT}{q} \exp\left(\frac{A^* T^2}{J_0}\right) \quad (3)$$

where q is the electronic charge, k is the Boltzmann's constant, T is the absolute temperature in Kelvin, J_0 is the saturation current density, and A^* is the Richardson constant. In agreement with Hobbie and co-workers,^[5,6] the ideality factor was found to be outside of the reasonable range of 1–2 and was

3.5 and 8.6 for devices with and without Nafion. The Schottky barrier heights were determined to be 0.88 eV (CNT/Nafion) and 0.78 eV (CNT). According to the Schottky theory, the barrier height of a heterojunction formed between two materials can also be determined by their work function difference as measured by ultraviolet photoelectron spectroscopy (UPS) in Figure 2d. ϕ_B (CNT: Si) = $W_{CNT} - W_{Si}$ and ϕ_B (CNT/Nafion: Si) = $W_{CNT/Nafion} - W_{Si}$. This calculation provides a theoretical ϕ_B of 1.1 and 0.6 eV for the devices with and without Nafion, respectively. A large difference between theoretical and measured ϕ_B values and in particular a larger experimental value for the CNT/Nafion:Si heterojunction indicate the poor suitability of this model. For the device without Nafion, interfacial defects pin the Fermi level and, in this case, in addition to the work function difference, ϕ_B is dependent on the interface density of states and interface charge, as described by the Bardeen model in Equations (4) and (5). Further details pertaining to this calculation are provided in the Supporting Information

$$\phi_B = \gamma(W_{CNT} - \chi_{Si}) + (1 - \gamma)(E_g - \phi_0) - \Delta\phi_n \quad (4)$$

$$\gamma = \varepsilon / (\varepsilon + \delta q D_{it}) \quad (5)$$

where ϕ_0 is defined as the energy below which the surface states must be filled for charge neutrality at the Si surface, χ_{Si}

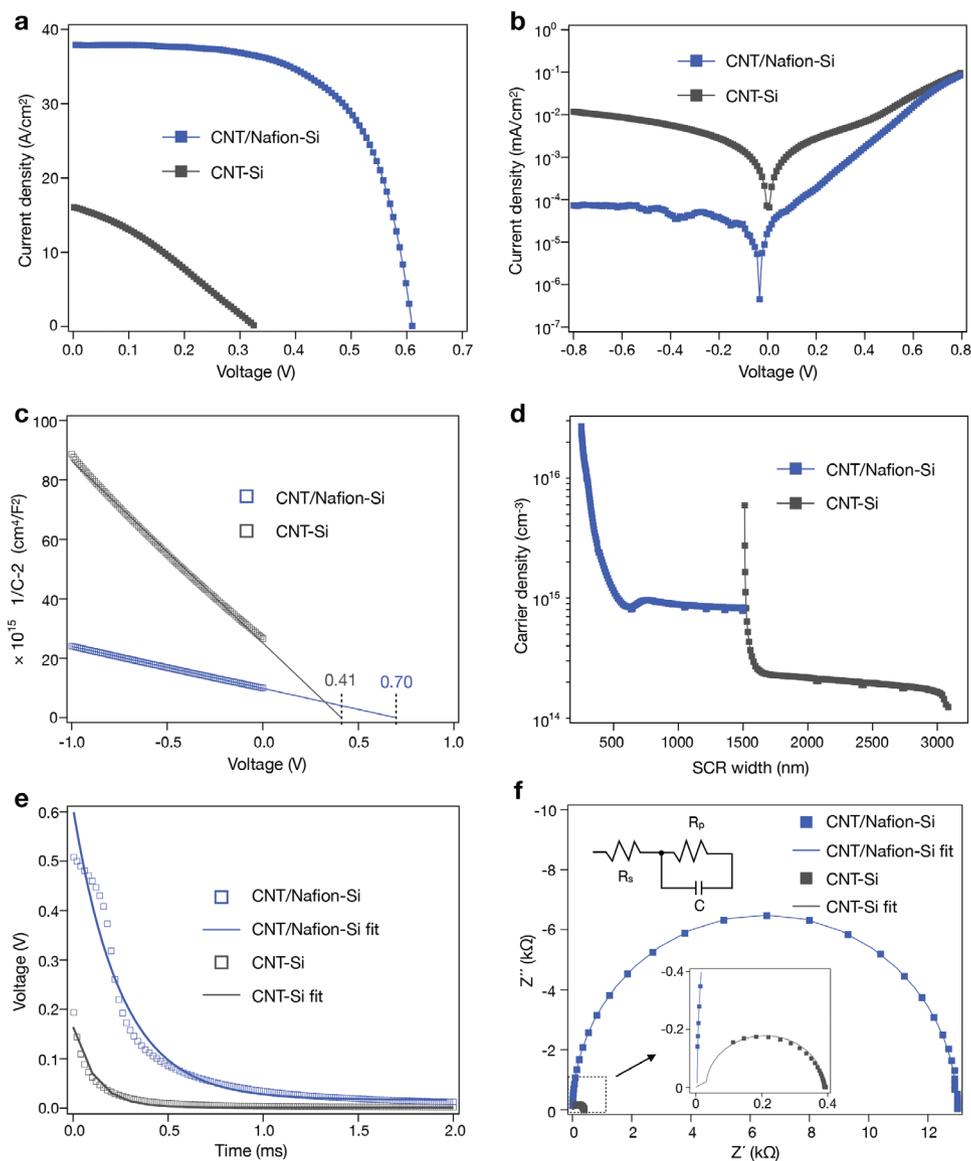


Figure 4. Comparison of solar cells with and without Nafion. a) J - V curves in the light and b) $\log J$ - V curves in the dark. Capacitance voltage measurements to determine c) the built-in potential and d) the doping level and the interface. e) Photovoltage transients and f) electrochemical impedance spectroscopy.

is the electron affinity of silicon, D_{it} is the interface density of states, ϵ is the dielectric constant of the interfacial layer, δ is its thickness, E_g is the bandgap of silicon, and $\Delta\phi_n$ is the barrier reduction attributed to the image force, which is related to the charge density in the interfacial passivation layer. Using a value of 0.22 for $\Delta\phi_n$, the Bardeen model determined ϕ_b to be 0.81 eV (CNT/Nafion:Si) and 0.39 eV (CNT:Si).^[49]

Capacitance voltage (CV) profiling techniques are employed to study the built-in potential (V_{bi}) and doping level (N_D) at the heterojunction interface. V_{bi} can be calculated using Equation (6) and N_D from Equation (7)^[50]

$$\frac{1}{C^2} = \frac{2(V_{bi} - V)}{A^2 \epsilon q N_D} \quad (6)$$

$$W (V) = \sqrt{\frac{2eV_{bi}}{qN_D}} \quad (7)$$

where A is the area of the device, ϵ is the permittivity, q is the fundamental charge, and W is width of the space charge region (SCR). Figure 4c,d indicates that Nafion doping of the CNTs increases the carrier concentration as well as the built-in potential (V_{bi}) at the CNT:Si junction. The x -intercept of a C^{-2} - V plot corresponds to V_{bi} and was found to be 0.41 and 0.70 V for devices with and without Nafion, respectively. For the CNT:Si device, this is close to the ϕ_b value from the Bardeen model and experimentally measured V_{oc} . Transient photovoltage decay (TPV) curves are shown for the two devices in Figure 4e. In a TPV measurement, the devices are maintained

Table 1. Simulated R_s , R_p , and C values for front-junction solar cells with and without Nafion.

	R_s [Ω]	R_p [$k\Omega$]	C [nF]	τ_{eff} [μs]
CNTs	30.7	0.36	8.23	2.96
CNT/Nafion	4.0	13.0	11.36	147.68

at open-circuit conditions under a simulated 1 sun condition, the light is switched off and V_{oc} decreases due to carrier recombination. The decay rate of V_{oc} is therefore an indication of the carrier lifetime. For CNTs alone, V_{oc} was observed to decay to 0 V within 0.5 ms, whereas for CNT/Nafion devices it persisted for 2 ms. Using an exponential fit the carrier lifetime in a device was calculated to be 270 and 118 μs with and without Nafion, respectively. A more than twofold increase suggests that Nafion acts to reduce the surface recombination rate. Electrochemical impedance spectroscopy (EIS) was performed and Nyquist plots are shown in Figure 4f. Using the ZView2 software, the impedance was calculated using an equivalent circuit model consisting of a series resistance (R_s), a parallel resistance (R_p), and a capacitance (C). Simulated R_s , R_p , and C values for solar cells with and without Nafion are listed in Table 1. For both devices, the curves are near semicircles, suggesting that only a single junction exists in the device. R_s is determined by the resistance of the external circuit and it can be seen that a

lower R_s is obtained for the device with Nafion. This contributes to the enhanced FF shown in Figure 4a. The increase of R_p suggests a suppression of recombination and leakage in device with Nafion. Additionally, the minority carrier lifetime (τ) can be obtained using $\tau = R_p C$.^[51] In agreement with the TPV measurements, τ was found to be higher with Nafion (147.7 μs) compared to without (3.0 μs).

Toward industrial application it is well known that p-type silicon solar cells have dominated the market for many years. This is due to the existence of simple and well-established fabrication lines. On the other hand, and despite offering several advantages including higher efficiency, low light induced degradation of the dopant, and double-side electrical generation, n-type silicon solar cells are much less widespread. This is due to the increased process complexity and therefore cost associated with their fabrication. Primarily this is related to the high temperatures required for boron diffusion to form the p⁺ emitter layer, but additional wet chemical cleaning steps and the use of AgAl pastes to improve the contact between the electrode and p⁺ layer lead to longer production lines and higher cost for n-type silicon solar cells. Figure S9 (Supporting Information) shows the fabrication steps used by industry to prepare n- and p-type silicon solar cells along with a predicted n-type CNT:Si solar cell line. The use of carbon nanotubes as a low temperature p⁺ emitter already dramatically reduces the complexity of fabrication, but if in the future strategies can be

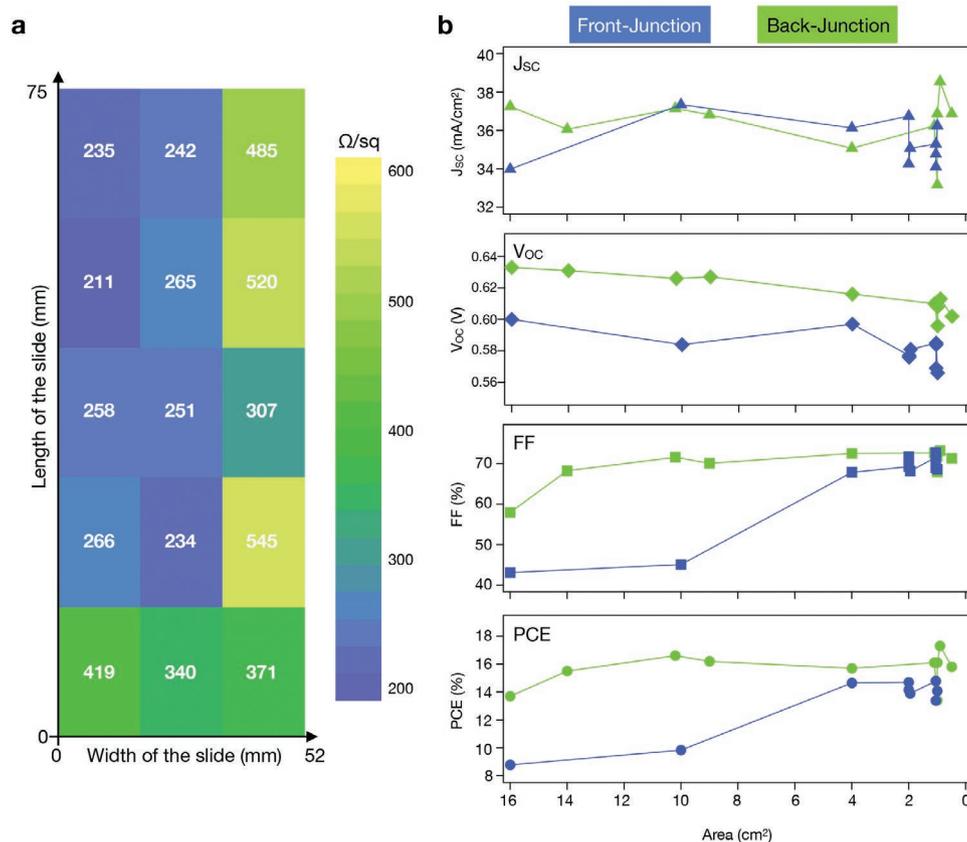


Figure 5. a) Sheet resistance measurements across a CNT film used for the fabrication of 16 cm² front or back-junction. b) Increase in performance as an active area of 16 cm² is diced into sequentially smaller active areas.

developed to combine Nafion and CNTs into a single ink, all of the benefits of n-type solar cells will be achievable with a close to p-type process. Using existing production lines, it is envisaged that p-type CNT/Nafion inks can be screen-printed onto the back junction of n-type solar cells. Of course, this does not immediately remove all high-temperature processes, but a host of dopant-free electron-selective contacts, such as LiF_x , TiO_2 , and MgO may offer a solution in the future. Moreover, as dopant strategies for CNTs become more developed, it will be possible to consider CNT(p)/n-Si/CNT(n^+) architecture.

At this stage, the ability to prepare homogenous CNT films over large areas remains a challenge for the uptake of both front and back-junction designs in industry. Additionally, the current requirement of super acid use and a two-step process involving CNT film transfer followed by Nafion coating introduce undesirable complexities in an industrial setting. **Figure 5a** shows common variations in sheet resistance across a typical CNT film used in the manufacture of devices with a device area of 16 cm^2 . Intuitively, a solar cell made from a film with a lower sheet resistance will perform better than one with a higher value, but on a large area one is forced to incorporate both. **Figure 5b** demonstrates this effect by taking the two 16 cm^2 cells and dicing them into sequentially smaller areas. Here, it is important to highlight that it is not standard to be able to dice a solar cell into smaller pieces and remeasure. Certainly, this would not be possible with all of the previous CNT:Si solar cells which have a metallic frame architecture. The only reason this can be achieved in this work is because of the highly scalable and industrially applicable design, which is relatively insensitive (at least in a back-junction design) to the active area. A clear increase in FF and PCE along with an increase in the variability among devices can be seen with decreasing active area. In agreement with what was discussed earlier, the effect on FF and PCE for front-junction cells is much greater than for the back-junction. As shown in **Figure S10** (Supporting Information), the performance of the back-junction cells approaches the best in the field for industry standard large area nanomaterial based silicon photovoltaics.

3. Conclusion

Proof-of-concept front and back-junction carbon nanotube/silicon solar cells with power conversion efficiencies approaching 19% were presented and their highly scalable device design allowed for device areas of up to 16 cm^2 to be reached. The high porosity of the carbon nanotube film in combination with Nafion enabled the formation of a hybrid PCSC to which metal fingers or a full contact could be directly deposited. This allowed for the use of an industrial design and it is predicted that the approach can be extended to other 1D and 2D materials, such as flakes of graphene, black phosphorous, or MoS_2 , which have also been shown to form an extended porous network and act as carrier selective contacts. In the future, strategies to combine carbon nanotubes and polymer passivation materials into a single ink will dramatically simplify the process and allow for a one-step deposition of a PCSC and is the focus of our ongoing work. These potential developments are expected to promote the PCSC cell approach into the realm of competitive c-Si cell technology.

4. Experimental Section

CNT films were prepared on glass substrates ($76 \times 52 \text{ mm}$) by the super acid sliding method.^[46] Before use, the glass slides were ultrasonically rinsed in deionized water, 2-propanol, and finally dried with N_2 . A precursor CNT solution was prepared from a 1:1 mix of single wall and double wall carbon nanotubes. 1 mg of CoMoCAT (CHASM, Batch No. SG65i-L56) and 2.5 mg of double wall carbon nanotubes (TORAY, Japan) were dispersed in 1 mL of chlorosulfonic acid (Merck KGaA) by continuous stirring for 4 d or until a homogenous solution was obtained. Several drops ($20\text{--}30 \mu\text{L}$) of this solution were placed between two glass slides and a compressive force applied to evenly distribute it. The glass slides were then rapidly withdrawn in opposing directions, resulting in lateral shear of the CNT solution and the formation of a thin film on the face of both slides. CNT solutions and films were prepared in a glove box filled with nitrogen. CNT films were allowed to dry in the glove box for 16 h before being taken into ambient conditions and transferred to devices by floating on water and picking them up with a silicon wafer.

(100)-oriented n-type CZ wafers with a thickness of $180 \mu\text{m}$ and resistivity of $\approx 2 \Omega \text{ cm}$ (bulk doping concentration is $\approx 2.4 \times 10^{15} \text{ cm}^{-3}$) were acquired from Yingli Green Energy Holding Co. Ltd. Wafer processing to obtain completed front and back-heterojunction CNT:Si solar cells consisted of several steps: 1) Single-side texturing of the surface by a chemical polish in a KOH ($2\text{--}3 \text{ wt}\%$, $82 \text{ }^\circ\text{C}$, 16 min) texturing bath to yield pyramids with an average size of $5 \mu\text{m}$; 2) The formation of an n^+ BSF by single-side POCl_3 diffusion performed on the polished surface for front-junction devices and on the textured surface for back-junction devices and subsequent removal of the phosphorus silicon glass (PSG) with HF; 3) Passivation of the n^+ surface by an $\approx 80 \text{ nm}$ SiN_x dielectric layer deposited by PECVD and subsequent metallization of back surface (for front-junction devices) or front surface (for back-junction devices) by screen-printing an Ag paste followed by a standard firing process; 4) Placement of the CNT films on the textured surface for front-junction devices or on the polished surface for back-junction devices. The films were either used as deposited or a low-temperature thermal treatment of $250 \text{ }^\circ\text{C}$ for 30 min in a nitrogen atmosphere was applied; 5) Spin coating of an $\approx 150 \text{ nm}$ -thick Nafion layer onto CNT:Si interface using a precursor solution (Sigma-Aldrich, 5 wt% in a mixture of lower aliphatic alcohols and $15\text{--}20\%$ water) at 3500 rpm for 40 s and RT under ambient atmosphere after a ramp time of 6 s; 6) Thermal evaporation of a 300 nm full contact Ag electrode for back-junction devices and patterned fingers for front-junction devices using a shadow mask onto the Nafion/CNT:Si interface. The active area of the solar cells ranged from 1 to 16 cm^2 . 60 front and 70 back-junction devices were made and solar cell parameters of V_{oc} , J_{sc} , FF, and PCE were measured to investigate the reproducibility of the proposed system.

Solar cells were characterized by $J\text{--}V$ curves using a source meter (Keithley 2601B) and a LOT-QD-133 solar simulator (RERA) under standard test conditions of AM1.5, 100 mW cm^{-2} and $25 \text{ }^\circ\text{C}$. EQE measurements were performed with a SpeQuest QE 1226 (RERA) using monochromated light from a Xenon arc-discharge lamp. A Zeiss Ultra Plus with 2.00 kV EHT and 2.9 mm working distance was used for SEM imaging. The reported Nafion thicknesses were determined by a step profiler on a flat silicon surface. The effective minority carrier lifetime was measured using the transient photoconductance decay technique on a WCT-120 system (Sinton, Boulder, CO), in which n-type (100)-oriented FZ Si wafers with DSP surfaces, a resistivity of $1\text{--}5 \Omega \text{ cm}$, and a thickness of $280 \mu\text{m}$ (Topsil) was symmetrically (both sides) covered by CNT thin films and/or passivated with Nafion films. UPS measurements were made with a Thermo Scientific ESCALab 250Xi system (He I, 21.22 eV) and were performed on the same nn^+ Si substrate as used for devices. Transmittance and reflectance spectra were collected using a UV-vis-NIR spectrophotometer (Hitachi U4100) equipped with an integration sphere. Absorption spectra were taken on a Cary50 (Varian) spectrophotometer. The sheet resistance was measured using the four-point probe technique (KeithLink) in a linear geometry and a multimeter (GDM-8261, GW Instek). The capacitance versus voltage ($C\text{--}V$)

measurements were carried out with a semiconductor device analyzer (Agilent, B1500A). The TPV measurement of the device was obtained from the Dyanamo Toolbox (DN-AE01). EIS of the solar cell was tested in a frequency range of 10 Hz to 1 MHz at room temperature by Zahner Ennium electrochemical analyzer (PP211).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

energy, Nafion, photovoltaic, SWCNT, thin-film

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