Circuit Design and Compact Modeling in Printed Electronics Based on Inorganic Materials

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To my parents, for their continuous encouragement.

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Abstract

The field of printed electronics (PE) is a young research area, relative to conventional silicon technology. The idea behind PE is to print electronic components, including microelectronic circuits, through out of solution processable materials which are fabricated in an additive process. The additive printing process brings some benefits with it, like avoiding any expensive mask and on demand fabrication. Currently, organic materials are state of the art for realizing printed devices. Semiconductors, conductors and dielectrics are available as organic based materials. These organic materials are used to print solar cells, diodes, resistors, capacitors as well as field-effect transistors (FETs) on rigid (glass, silicon) or flexible substrates (paper, plastic).

However, organic electronics mostly uses p-type devices and field-effect mobility values are lower than in silicon based devices, where threshold voltages are much lower. Also, all printed circuits based on organics are rare. For future applications, eg. Internet of Things (ITO), soft electronics for robotics or smart sensors, it is essentially to develop a fully printed technology together with suitable circuit designs.

An interesting alternative to organic semiconductors are oxide semiconductors. For example, indium oxide provides intrinsic mobility values of approximate 100 $cm^2\,V^{-1}\,s^{-1}$. Higher mobility values lead to higher current densities and enhance the overall speed of the devices. Oxide semiconductors are inkjet printable, integrateable into a non-toxic fabrication process, and optically transparent. In oxide electronics, n-type oxide semiconductors are common, while p-type oxide semiconductors are rather rare. The exhibited intrinsic mobility of p-type metal oxides is three orders of magnitude lower than the values shown by n-type metal oxide semiconductors. Unfortunately, metal oxides, typically, require high annealing temperatures ($\sim$ 400 °C), to form the desired transition phase. This is a disadvantage compared to organic semiconductors where room temperature processes are frequent.

The goal of this thesis is therefore to develop an inorganic printed electronics technology with corresponding modeling methodologies to capture device behavior for industry standard circuit simulators as well as circuit designs as building blocks for future applications. To reduce the high supply voltage requirements ($\geq$ 5 V) in PE, alternative gating approaches for FETs are considered. One approach is to replace the dielectric with an electrolyte. Due to the formation of a Helmholtz double layer (HDL), a FET with a high gate-capacitance ($\sim$ 5 $\mu F\,cm^{-2}$) is expected, reducing the voltage requirements to $\sim$ 1 V. By combining the indium oxide channel with the electrolyte-gating approach, high performance devices with low voltage requirements are available in PE.

The structure of this thesis is to firstly characterize electrolyte-gated field-effect transistors (EGFETs) with indium oxide channels, and secondly create a predictive model which is able to be integrated into a circuit simulator. Following, reliable design topologies for the presented transistor technology are shown. The evaluation of the design topologies will take place on basic microelectronic digital logic cells and ring

oscillator structures.

To model EGFETs, different modeling approaches for the different transistor regions are needed. The above threshold region is modeled accurately through the Curtice model. Furthermore, the Curtice model only requires a few parameters and depict the linear and saturation regions with only one equation. For the subthreshold region, the conventional silicon subthreshold model predicts the electrical characteristic of the EGFET very well. Smoothness and continuity between the simulated below and above threshold regions are ensured with an interpolation scheme that models the near threshold region. This modeling approach provides a good match between the measured and simulated data.

The developed model is integrated into a simulation program with integrated circuit emphasis (SPICE) and into a process design kit (PDK) to support the development of new applications. Therefore, the behavior of microelectronic circuits based on EGFETs are predictable through simulation. In addition, simulations are used to evaluate the performance of circuits under different environmental conditions, i.e. effects of humidity on EGFETs based applications.

Since p-type oxide semiconductors, which have equal performance than n-type semiconductors are not available, complementary circuit designs are not feasible in oxide electronics. For this reason, the pull-up network, which is based on p-type FETs in conventional microelectronics, is replaced through either a resistor or an n-type EGFET. The pull-down network is based on one or more n-type EGFETs in both cases.

The first approach to replace the p-type EGFET is demonstrated on an inverter designed within the transistor-resistor logic (TRL) topology. As result, the inverter has a gain of around -5 and a propagation delay time of ~ 0.9 ms, measured at a supply voltage of 1 V. At the same voltage level, the sequentially built three stage ring oscillator, oscillates at a frequency of 296 Hz. Standard logic gates (NAND, NOR and XOR) are likewise feasible with EGFETs in TRL.

It is also possible to design microelectronic circuits within the transistor-transistor logic (TTL) topology. In TTL, the resistor in the pull-up network is supplanted by a depletion mode EGFET. All logic gates, show similar performance to the TRL based cells, but the ring oscillator operates in the sub-kHz regime. Furthermore, in a NAND gate, the power consumption is shown to be reduced by a factor of 6.

Zusammenfassung der Arbeit

Die gedruckte Elektronik ist ein im Vergleich zur konventionellen Siliziumtechnologie junges Forschungsgebiet. Die Idee hinter der gedruckten Elektronik ist es elektronische Bauteile wie Widerstände, Kapazitäten, Solarzellen, Dioden und Transistoren mit gängigen Druckmethoden herzustellen. Dabei ist es möglich die elektronischen Bauteile auf unbiegsamen Substrate, wie Glas oder Silizium, als auch auf biegsamen Substrate, wie Papier und Folie, zu drucken. Aufgrund des Druckprozesses, sind die Herstellungskosten gering, da drucken ein additiver Prozess ist und somit teure Masken obsolet sind.

In einem Feldeffekttransistor, wird der Halbleiter zwischen zwei Elektroden (Drain- und Source) gedruckt. Die Drain- und Source-Elektroden werden dabei durch einen Vakuum- oder Druckprozess abgeschieden und strukturiert. Der halbleitende Kanal wird durch einen Dielektrikum von der Gate-Elektrode isoliert. Auch für das Dielektrikum und die Gate-Elektrode sind ein Vakuum- oder Druckprozess denkbar. Standardmäßig finden organische Materialien Einsatz in der gedruckten Elektronik. Leider weisen organische Halbleiter, in einem Feldeffekttransistor, nur eine geringe Ladungsträgerbeweglichkeit ($\leq 1\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$) auf. Die niedrige Ladungsträgerbeweglichkeit führt zu einer geringen Ladungsträgerdichte im Halbleiter und als Resultat zu geringen Stromdichten. Auch sind größtenteils nur p-leitende Halbleiter für den Einsatz in Schaltungen vorhanden, weswegen die meisten Schaltungen nur p-leitende Feldeffekttransistoren besitzen. Ein weiterer Nachteil der organischen Elektronik ist, dass die eingesetzten Dielektrika mit dem Halbleiter eine mangelhafte Grenzfläche bildet. Deshalb sind Versorgungsspannungen in Bereich von 5 V keine Seltenheit.

Eine interessante Alternative zu organischen Halbleitern sind Materialien die der Kategorie der Oxide zugeordnet sind. Zum Beispiel in Indiumoxid (In_2O_3) ist eine Ladungsträerbeweglichkeit um die 100 $\mathrm{cm^2\,V^{-1}\,s^{-1}}$ messbar. Leider sind durch Oxide realisierte p-leitende Feldeffekttransistoren sehr selten, weshalb die meisten Schaltungen auf n-leitenden Feldeffekttransistoren basieren. Ein weiterer Nachteil von Metalloxidhalbleitern is das hohe Glühtemperaturen ($\sim 400\ ^\circ\mathrm{C}$) benötigt werden um die richtige Kristallstruktur zu erzielen.

Durch den Einsatz eines Elektrolyten, anstatt eines Dielektrikum, werden die benötigten hohen Versorgungsspannungen auf 1 V reduziert. Der Grund für die Reduzierung der Versorgungsspannung liegt in der hohen Kapazität ($\sim 5\ \mu\mathrm{F\,cm^{-2}}$), die sich zwischen der Gate-Elektrode und dem Kanal ausbildet. Die optimale Grenzfläche zwischen der Gate-Elektrode und dem Elektrolyten sowie als auch zwischen dem Elektrolyten und dem Kanal, wo sich eine Helmholtz-Doppelschicht ausbildet, ist der Grund für die hohe Kapazität.

In dieser Arbeit, werden die Vorteile der hohen Ladungsträgerbeweglichkeit, resultierend von einem Indiumoxid-Kanal, und der niedrigen Versorgungsspannungen, durch den Einsatz eines Elektrolyten als Isolator, in einem gedruckten Transistor kombiniert. Daher ist das Ziel zunächst Transistoren basierend auf einem Elektrolyten und

Indiumoxid-Kanal zu charakterisieren und zu modellieren. Auch werden Möglichkeiten zum Schaltungsentwurf mit der hier vorgestellten Transistortechnologie ausgearbeitet. Der Schaltungsentwurf wird anhand mikroelektronischen Zellen und Ringoszillator-Strukturen verifiziert.

Wichtig für den Schaltungsentwurf sind Modelle die fähig sind die elektrischen Eigenschaften eines Transistors abzubilden. Dabei muss die simulierte Kurve Stetigkeit und Kontinuität aufweisen um Konvergenzprobleme während der Simulation zu verhindern. Zur Modellierung der elektrischen Eigenschaften und Ströme der Transistoren wird ein Modell basierend auf den Curtice-Modell entwickelt. Der Bereich über der Schwellwertspannung wird daher durch das Curtice-Modell abgebildet und der Bereich unter der Schwellspannung durch ein aus Siliziumtransistoren bekanntes Standard-Modell beschrieben. Kontinuität und Stetigkeit wird durch eine Interpolation zwischen den beiden Transistormodellen gewährleistet. Ein Verglich zwischen gemessenen und simulierten Daten zeigt das das Modell die hier vorgestellte Transistortechnologie sehr gut abbilden kann.

Das entwickelte Transistormodel wird zur unterstützung des Schaltungsentwurf in einem Prozesskit (PDK) integriert. Dadurch ist das Verhalten einer Schaltung durch Simulation vorhersehbar. In der Simulation können auch der Einfluss der Umwelt, z.B. Luftfeuchtigkeit, auf die Transistoren analysiert werden.

In der digitalen Schaltungstechnik wird ein p-leitender Feldeffekttransistor verwendet um ein Eingangssignal hochzusetzen, während um ein Signal runterzusetzen, ein n-leitender Feldeffekttransistor von Vorteil ist. Da p-leitende Oxide selten und unzuverlässig sind, wird der p-leitende Feldeffekttransistor durch einen Widerstand (Transistor-Widerstand-Logik (TRL)) oder einen n-leitenden Feldeffekttransistor (Transistor-Transistor-Logik (TTL)) ersetzt. Ein Inverter in TRL weist bei einer Versorgungsspannung von 1 V einen Verstärkungsfaktor von ungefähr -5 auf und eine Signalverzögerung von 0.9 ms. Die Oszillatorfrequenz im entsprechend Ringoszillator beträgt 296 Hz. Weitere Logikgatter (NAND, NOR und XOR) sind ebenfalls realisierbar mit TRL-Entwürfe.

In TTL wird der p-leitende Feldeffekttransistor durch einen n-leitenden Verarmungstyps Feldeffekttransistor ersetzt. Die in der TTL entworfene Logikgatter verhalten sich identisch zu den TTR-Zellen aber die Frequenz vom Ringoszillator steigt bis in den unteren kHz-Bereich an. In TTL ist es ebenfalls möglich die Verlustleistung um einen Faktor von 6 zu reduzieren.

List of publications

Journals

- **G. C. Marques**, A. M. Sukuramsyah, A. Arnal, S. Bolat, A. Aribia, X. Feng, S. A. Singaraju, E. Ramon, Y. Romanyuk, M. Tahoori and J. Aghassi-Hagmann, "Fabrication and Modeling of pn-Diodes Based on Inkjet Printed Oxide Semiconductors", *IEEE Electron Devices Letters*, vol. 41, no. 1, pp. 187-190, 2020.

- X. Feng, **G. C. Marques**, F. Rasheed, M. B. Tahoori and J. Aghassi-Hagmann, "Nonquasi-Static Capacitance Modeling and Characterization for Printed Inorganic Electrolyte-Gated Transistors in Logic Gates", *IEEE Transactions on Electron Devices*, vol. 66, no. 12, pp. 5272-5277, 2019.

- J. Jeong, **G. C. Marques**, X. Feng, D. Boll, S. A. Singaraju, J. Aghassi-Hagmann, H. Hahn and B. Breitung, "Ink-Jet Printable, Self-Assembled, and Chemically Crosslinked Ion-Gel as Electrolyte for Thin Film, Printable Transistors", *Advanced Materials Interfaces*, vol. 6, no. 21, pp. 1901074, 2019.

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- **G. C. Marques**, F. von Seggern, S. Dehm, B. Breitung, H. Hahn, S. Dasgupta, M. B. Tahoori and J. Aghassi-Hagmann, "Influence of humidity on the performance of composite polymer electrolyte-gated field-effect transistors and circuits", *IEEE Transactions on Electron Devices*, vol. 66, no. 5, pp. 2202 - 2207, 2019.

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- F. Rasheed, M. S. Golanbari, **G. C. Marques**, M. Tahoori and J. Aghassi-Hagmann, "A smooth EKV-based DC model for accurate simulation of printed transistors and their process variations", *IEEE Transactions on Electron Devices*, vol. 65, no. 2, pp. 667 - 673, 2018.
- **G. C. Marques**, S. K. Garlapati, S. Dehm, S. Dasgupta, H. Hahn, M. Tahoori, and J. Aghassi-Hagmann, "Digital power and performance analysis of inkjet printed ring oscillators based on electrolyte-gated oxide electronics", *Applied Physics Letters*, vol. 111, no. 10, pp. 102103, 2017.
- **G. C. Marques**, S. K. Garlapati, D. Chatterjee, S. Dehm, S. Dasgupta, J. Aghassi, and M. B. Tahoori, "Electrolyte-gated FETs based on oxide semiconductors: fabrication and modeling", *IEEE Transactions on Electron Devices*, vol. 64, no. 1, pp. 279 - 285, 2017.

Conferences

- **G. C. Marques**, F. Rasheed, B. Breitung, H. Hahn, M. Tahoori and J. Aghassi-Hagmann, "Modeling and characterization of low voltage, inkjet printed devices and circuits", *in Proceedings of the Large-area, Organic & Printed Electronics Convention*, 2018, München.

Workshops

- X. Feng, **G. C. Marques**, F. Rasheed, M. B. Tahoori and J. Aghassi, "Analog properties of printed electrolyte-gated FETs based on metal oxide semiconductors", *in 59. MPC Workshop, IEEE German Section Solid-State Circuit Society*, pp. 67 - 71, 2018. (Best Paper Award)
- **G. C. Marques**, S. K. Garlapati, S. Dehm, S. Dasgupta, J. Aghassi and M. B. Tahoori, "Compact modeling of inkjet printed, high mobility, electrolyte-gated transistors", *in 55. MPC Workshop, IEEE German Section Solid-State Circuit Society*, pp. 29 - 32, 2016. (Best Paper Award)

Invited Papers

- **G. C. Marques**, F. Rasheed, J. Aghassi-Hagmann and M. B. Tahoori, "From silicon to printed electronics: A coherent modeling and design flow approach based on printed electrolyte gated FETs", *in Proceedings of the Asia and South Pacific Design Automation Conference*, pp. 658 - 663, 2018.

Contents

Part I.

Introduction

1. Printed electronics technology

In this modern age, our lives are highly governed by microelectronics. In most of the everyday electronic devices, data is processed, even without the user's notice. For instance, in cars or refrigerators, physical quantities are measured by sensors and processed through a microcontroller to make our lives safer and more convenient. Recently, the internet of things (IOT) domain, where a variety of sensors and actuators communicate with each other and without any human interference, is gaining in popularity all over the world. For eg., a smartwatch and a heartbeat monitor can communicate with a smartphone during a workout in a way which allows the user to monitor and improve his performance with greater ease.

One of the most basic electronic components in modern microelectronic circuits are silicon (Si) based field-effect transistors (FETs), which are the basis of logic gates. Logic gates, in turn, are the most essential building blocks of integrated circuit based applications. In 1965, Gordon E. Moore predicted that the component count is doubled every year in an integrated circuit. [1, 2] Later, in 1975, the Moore's Law was slightly revised to double components every two years. [3, 4] In fact, this prediction turned out to become true, as seen from Figure 1.1. [5]

The continuous increase of transistor density is achieved mainly by scaling down the feature size of the transistors. The first microprocessor (Intel© 4004 4-bit microprocessor) came into the market in 1971 and is designed with 2300 transistors, of which the minimal feature size is 10 µm. Obeying Moore's Law, a processor presented by Intel© in 2010, designed within the 32 nm technology node, is based on 560 million transistors. [6] Besides increasing the component density on a chip, scaling down the transistor size improves the performance and reduces the power dissipation of microelectronic devices. Naturally, reducing the transistor size is limited due to atomic and quantum mechanical effects, leading to increases in leakage current and power consumption. [7, 8] Therefore, to satisfy the demand for higher integration density, new device architectures or even materials must be developed. [9, 10]

While the Si industry is attempting to shrink the feature size of their devices for aforementioned reasons, printed electronics (PE) is fine with large area applications. The thoughts behind PE is to have versatile electric components or applications directly printed on demand and at low fabrication costs. Ideally, the substrate on which the devices are printed should not play a role and rigid substrates, like glass, or flexible substrates, like plastic foils, are feasible. [11] However, the minimum feature size of a FET is bound to the printing resolution. For eg., the resolution of an inkjet printer is between 2 - 50 µm. [12, 13] Besides that, the performance of printable FETs, in terms of field-effect mobility (μ_{fet}), are close to two orders of magnitude lower than in the state of the art Si technology. For that reason, the aim of PE is to complement, rather than to replace the Si based FETs. In an application, when manufacturing costs take precedence over the performance of the individual devices; PE can become an interesting alternative

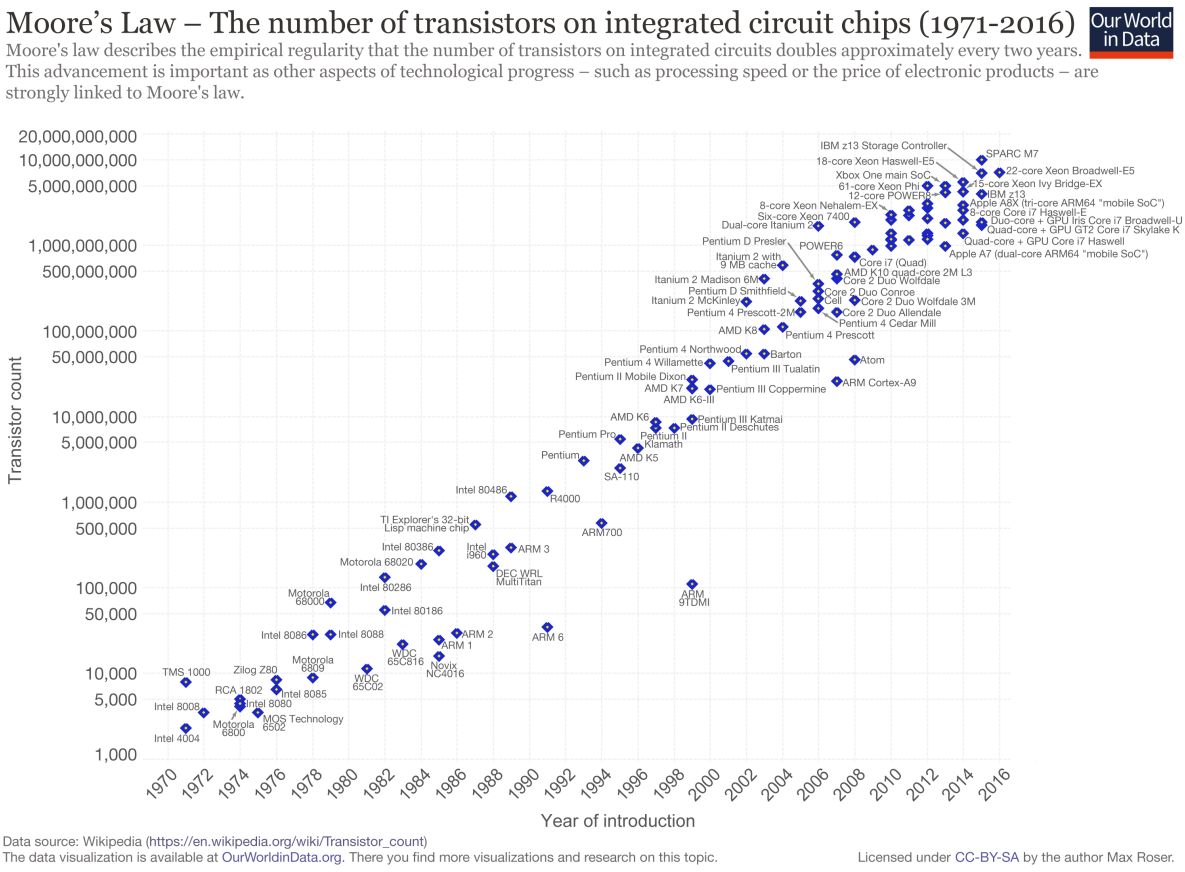


Figure 1.1.: Evolution of transistor counts on integrated chips from 1971 to 2016. Reprint from [5] under license CC-BB-BY-SA.

to conventional Si technology. The low fabrication costs in PE result from the fact that the devices are fabricated in an additive process, by which the functional materials are deposited on top of each other with inexpensive printing methods and without requiring any expensive mask. [11]

People have been printing, and improving the printing technology since early 3500 BCE. Today, we are used going into shops and to buy books or newspapers. Furthermore, households have one or more printers available where various kinds of documents are printed. It is obvious to use this well known and cheap technology to fabricate microelectronic circuits. For printing microelectronic circuits, different printing technologies are available and are categorized in the following types. In jetting based technologies, like inkjet printing, aerosol-jet printing, and electrohydrodynamic printing, the ink is pushed through a nozzle. If high throughput and scaleability is required, replecation type printing, like gravure printing, flexography, screen printing or reverse offset printing is favorable. However, replication type printing typically require masks which can become very expansive. Some key parameters of the presented printing technologies are summarized in Table 1.1. [14]

The jetting type printing technique is a digital and non-contact method, which allows for high flexibility in selecting the printing patterns and reducing contact contamination, hence, suitable for PE. [14] For that reason, the focus of this thesis is on inkjet printed

Table 1.1.: Comparison of different printing techniques suitable for PE. [14]

Printing technique	Resolution (µm)	Film thickness (nm)	Line width (µm)
Inkjet	2 [12]	100-500 [12, 15]	2-8 [16]
Aerosol jet	10 [17]	30-150 [18, 19]	10 [17]
Electrohydrodynamic	2 [20]	20-180 [20, 21]	2 [20, 21]
Gravure	2 [22, 23]	10-400 [24, 25]	35 [24]
Flexography	1 [26]	5-50 [26, 27]	3 [26]
Screen printing	100 [28]	14000-25000 [29, 30]	40 [30]
Reverse offset printing	1 [31]	90-400 [31, 32]	2 [33]

devices. In addition, inkjet printing combines feasible resolution with inexpensive fabrication routines. In an inkjet printer, a pulse is applied to the piezoelectric actuator which changes the volume of the piezo crystal. This causes a pressure wave moving in direction of the nozzle, leading the ink to be jetted, if the transferred kinetic energy is higher than the surface energy. [34] Figure 1.2 depicts the schematic of one nozzle.

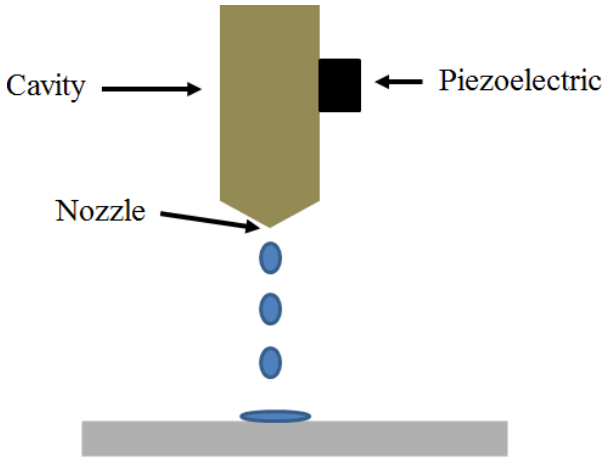


Figure 1.2.: Schematic of a nozzle in an inkjet printer

With regards to FETs, organic-based materials are common in PE. Although much optimization has been done since the publication of the first organic field-effect transistor (OFET) in 1986, organic semiconductors show relatively low carrier mobility values, thereby harming the performance of applications. [35] Furthermore, OFETs and applications based on these OFETs typically require high supply voltages ($\geq$ 5 V). The reason for the high voltage requirements lies in the fact that conventional dielectrics are inefficient gating materials in printed transistors. [11, 36, 37] Depositing of the high- or low-k dielectric results in the formation of a solid dielectric, independent of the deposition method. Consequently, the interface quality between the rough channel surfaces, as it is expected for a printed film, and the dielectric decreases. [38] Nevertheless, a few examples of low voltage applications ($\leq$ 5 V), by sacrificing performance, are found in literature. [39] A seven-stage ring oscillator with only p-type OFETs is able to oscillate at 106 kHz, with a stage delay of 0.68 µs and require a supply voltage of -80 V. [40] Already by reducing the supply voltage to 10 V, the oscillating frequency drops to 1 kHz in a five stage ring oscillator, translating to a stage delay of 100 µs. [41, 42] The frequency drops

further to 1.7 Hz by reducing the supply voltage to 3 V, corresponding to a stage delay of 42 ms in a seven stage ring oscillator. [39, 43]

Circuit designs with p-type only OFETs are not limited to ring oscillators. Radio frequency identification (RFID) transponders realized with p-type OFETs have been highly investigated. The operating frequency of 13.56 MHz seems not to be an obstacle. [44] Also in Active Matrix Organic Light Emitting Diode (AMOLED) displays, OFETs are used for designing the backplane. [45] Marien et al. show that analog designs, based on OFETs, have potential for future applications. [46]

The low performance of devices in PE is not exclusive due to the low field-effect mobility of organic semiconductors or the inefficient gating approach. Also, the lack of reliable n-type semiconductors reduces the performance of applications in PE, causing the circuit designs to be in p-type logic only. [39, 47] The reason for the lack of n-type semiconductors is due to the fact that electrons got trapped at the semiconductor/dielectric-interface by hydroxyl groups in organic semiconductors. [48] A complementary metal oxide semiconductor (CMOS) and organic based seven stage ring oscillator is shown to oscillate at a frequency of ~ 285 Hz, which is equal to a stage delay of 250 µs, and at a supply voltage of 15 V. [49] A storage element with complementary OFETs is also reported; Takeda et al. show that flip flops are achievable with OFETs by printing D-flip flops on a one micron thick plastic substrate (Figure 1.3). [50]

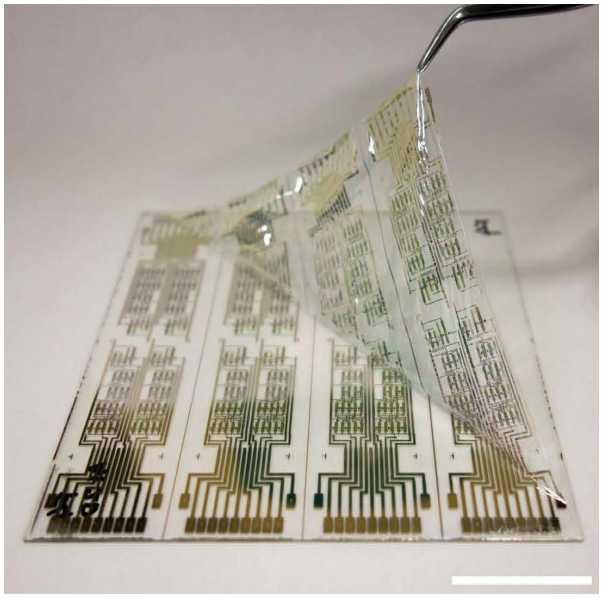


Figure 1.3.: A circuit based on organic FETs printed on a flexible substrate. Reprinted from [50] under license CC-BY-4.0.

To overcome the limitations of the organic semiconductor, inorganic oxides are introduced in PE. [51] In comparison to organic semiconductors, inorganic oxide semiconductors typically show orders of magnitude higher mobility values, making them ideal for increasing the performance of devices in PE. Higher mobility values are desired to increase the switching speed of FETs. Unfortunately, unlike organic semiconductors, which can be processed at room temperature (RT), oxide semiconductors mostly require a post-annealing step with temperatures around $300 - 400$ °C, limiting the choice of

the substrate. [52] Also, high performance p-type oxide semiconductors, comparable to n-type oxides, are not available. For that reason, most of the circuit designs are made only with n-type FETs. [53] In a seven stage ring oscillator with n-type only FETs, based on indium gallium zinc oxide, as semiconductor, and silicon dioxide as gate-dielectric, the frequency is measured to be 33 kHz, corresponding to a stage delay of 2.2 µs, at a supply voltage of 10 V, over-performing organic semiconductors. [54]

On the other hand, the high supply voltage requirements of printed FETs are overcome by using an electrolyte as gate-dielectric. Electrolytes are liquids containing mobile ions, able to form a Helmotz double layer (HDL) together with the charge carriers located at the gate-electrode and the channel. The formation of a HDL results in a high gate-capacitance, drastically lowering the supply voltages to values $\sim$ 2.0 V. [55, 56] However, the general opinion regarding electrolyte-gating is that parasitic effects decrease the speed of the targeted applications. Nevertheless, theoretical calculations have shown that electrolyte-gated FETs are able to operate in the sub-MHz region, which is more than sufficient for PE. [57] On the experimental side, Xia et al. show a five stage ring oscillator, based on organic FETs, oscillating at a frequency of 150 Hz, which is a stage delay of 0.7 ms, and reducing the supply voltage to $\sim$ 2 V.

In this thesis, the benefits of high carrier mobility, resulting from the oxide semiconductor, and low voltage requirements, resulting from the electrolyte-gating, are combined in transistor structures. [58, 59] Indium oxide is used as the channel material because it demonstrates high intrinsic mobility values ($\geq$ 100 $cm^2\,V^{-1}\,s^{-1}$). [14] With this approach, it is possible to have high performance applications with low voltage requirements in the field of PE. [60, 61] Literature also indicates that this transistor technology is feasible for analog applications. [62] Moreover, a direct current (DC) model, is presented, which is able to predict the behavior of such electrolyte-gated field-effect transistor (EGFET), with indium oxide (In_2O_3) channel. [63] Developing predictive models is essential for building a process design kit (PDK). A PDK includes all the design rules and models that a circuit designer needs for designing and simulating circuits. The development of a PDK for the following presented transistor technology is ongoing work. [64] Besides fabricating and modeling EGFETs, the aim of this work is to study design typologies suitable for digital applications based on these EGFETs. Since p-type metal oxides are not able to be combined with n-type metal oxides, typologies with a resistor or a n-type EGFET, replacing the p-type EGFET, are evaluated. The circuit design is evaluated on microelectronic cells as well as ring oscillator structures. This transistor technology, in combination with reliable modeling as well as design methodologies, may forge the way for high performance and low voltage applications in the field of PE.

The organization of the presented thesis is as follows: After this introduction, the background of this thesis is discussed in Chapter 2 and Chapter 3. Thereby, Chapter 2 focuses on the architecture as well as working principles of thin film, printed FETs. As discussed, metal oxides turned out to be very interesting for applications in PE. Therefore, some metal oxides suitable for PE are also reviewed and compared in this chapter. Next, the concept of electrolyte-gating is explained by studying the characteristics of the Helmholtz double layer in more detail. A large number of models are available to model printed FETs and suitable for circuit simulation; therefore, the most important modeling approaches suitable for PE are reviewed in Chapter 3. Chapter 4 introduces the studied EGFET transistor technology and initiates the result part of this thesis. Besides

demonstrating the electrical characteristics of such EGFETs, this chapter purposes a modeling methodology for describing the DC behavior of EGFETs. In Chapter 5, logic gates and ring oscillator structures based on EGFETs are designed. As design topology the so called transistor-resistor logic, where a resistor is used in the pull-up network and an EGFET in the pull-down network, is compared with the transistor-transistor logic, where the pull-up and pull-down networks are based on EGFETs. A correlation between the measured and simulated ring oscillator data is made in Chapter 6. Furthermore, measurements show that the EGFETs and circuits based on EGFETs are influenced by moisture. This dependency on the moisture is understood with the help of simulations. Finally, the work is concluded and an outlook into future tasks is given in Chapters 7 and Chapter 8, respectively.

Part II.

Theory

2. Thin film technology

Before introducing the EGFET technology, an overview on thin film transistors (TFTs) is given. In addition, interesting materials suitable for thin film based devices are discussed. TFTs are very popular in liquid crystal display (LCD) or other display technologies because of a straight forward and well established manufacturing process. For instance, in a LCD matrix, the individual pixels are selected through a TFT. [65] Amorphous or polycrystalline silicon are state of the art materials used in TFTs. On the other hand, metal oxides are getting more attention because of their high intrinsic mobility values and easy manufactureability.

The concept of a TFT is adopted in PE, where the functional materials are printed on top of each other. In general, it is possible to integrate metal oxides into a solution process and deposited these materials through a printer. [53] Unfortunately, because of the used materials, high supply voltages and low performance are expected in PE. As shown in the following, metal oxides in combination with electrolytes reduce the expected supply voltage range, while enhancing the performance of applications.

2.1. Printed transistors

Organic-based compounds are widely used to fabricate TFTs/FETs in PE. In this regard, organic based semiconductors, conductors and insulators are found in literature. [11, 13, 66] To fabricate a printed TFT, the organic materials are either stacked in the top gate (TG) (Figure 2.1a) or the bottom gate (BG) (Figure 2.1b) configurations. The semiconductor, which forms the channel, is always placed between the source- and the drain-electrodes. The vertical distance between the drain- and the source-electrode is known as the channel length (L) and the height of the semiconductor layer in the horizontal direction as the channel width (W) (Figure 2.1c). However, in the TG configuration, the dielectric and the gate-electrode are placed on top of the semiconductor. Conversely, in the BG configuration, the gate-electrode and the dielectric are placed below the semiconductor. [11]

There is a typical distinction between semi and fully printed devices. Semi printed devices, where the transistor terminals and interconnects, preferable based on gold or silver, deposited through a vacuum process, are more common. Printing conductive lines is, however, still a demanding task. Also, in most of the cases, the printed conductive lines require a post annealing step at higher temperatures ($\sim$ 200 °C) than most of the flexible substrates can sustain. [11, 67] Nevertheless, in recent days, researchers are moving towards fully printed devices where everything is printed. [68, 69]

The domain of printed TFTs grows with the progress made in the organic semiconductor research. However, pentacene ($C_{22}H_{14}$) is still one of the most popular semiconductors in this field. The field-effect mobility is a very important parameter in a FET/TFT and

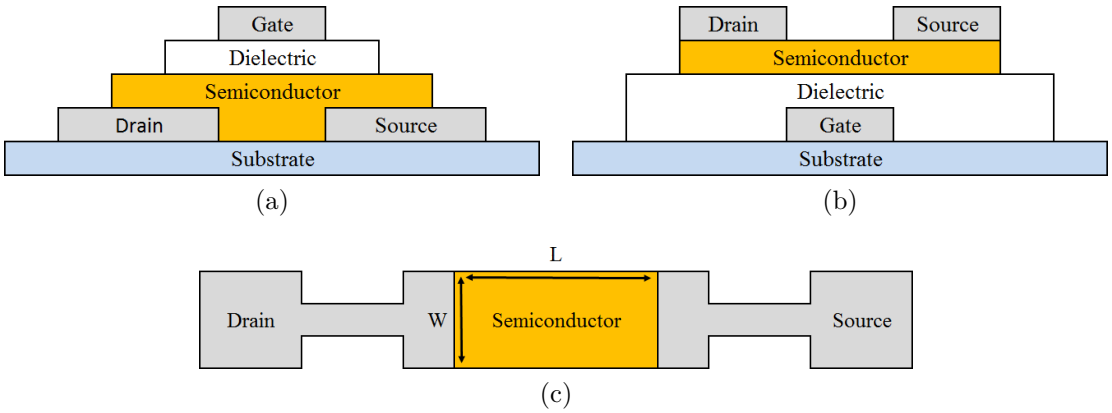


Figure 2.1.: Graphical representation of a TFT in (a) TG and (b) BG configuration. (c) Top view of the channel printed between the source- and drain-electrodes without dielectric and gate-electrode.

describes how fast the charge carriers can travel from the drain- to the source-electrode, under the influence of an electric field. The field-effect mobility of a printed p-type pentacene based OFET can be up to 0.68 $cm^2\,V^{-1}\,s^{-1}$. [70]. Another important organic semiconductor is poly(3-hexylthiophene-2,5-diyl) (P3HT) which has a field-effect mobility value of 0.12 $cm^2\,V^{-1}\,s^{-1}$ in a p-type OFET. [71] Nevertheless, field-effect mobility values around 10 $cm^2\,V^{-1}\,s^{-1}$ are feasible with other organic p-type semiconductors. [72] Bisthienoisatin derivatives are interesting candidates for n-type OFETs. In this regard, a n-type OFET with dicyanomethylene 2-ethylhexyl (BTICN-EH) has a field-effect mobility of around 0.2 $cm^2\,V^{-1}\,s^{-1}$. [73] Unlike in conventional electronics, there are an endless number of semiconductors suitable for PE, therefore, only the most important organic semiconductors are mentioned here. Nevertheless, in Section 2.2.3, oxide semiconductors are introduced where field-effect mobility values ~ 100 $cm^2\,V^{-1}\,s^{-1}$ are measured. It is desirable to maximize the field-effect mobility to increase the driver capability of a TFT, as well as the cut-off frequency (f_t): [57]

$$f_t = \frac{\mu_{fet}\,V}{2\,\pi\,L^2}, \tag{2.1}$$

where V is the driving voltage.

The choice of the dielectric material turned out to be very crucial. Conventional high or low-k dielectric, like silicon dioxide (SiO_2) and zirconium dioxide (ZrO_2), respectively, are well known in PE. [11, 74] Due to the bad interface properties between the semiconductor and the dielectric, high supply voltages is a characteristic of applications based on printed TFTs. By introducing an electrolyte as gate-dielectric, not only does the supply voltage goes down, but also the field-effect mobility value increases, due to the improved surface interface between the gate-dielectric material and the semiconductor. The field-effect mobility value of the P3HT based OFET increases to ~ 18 $cm^2\,V^{-1}\,s^{-1}$ and the pentacene based OFET to ~ 5.6 $cm^2\,V^{-1}\,s^{-1}$ with an electrolyte as insulator. [75]

The working principle of printed/organic TFTs is identical to conventional silicon based TFTs. By increasing the potential between the gate- and the source-electrode (gate-source voltage (V_{gs})), charges accumulate at the surface of the semiconductor,

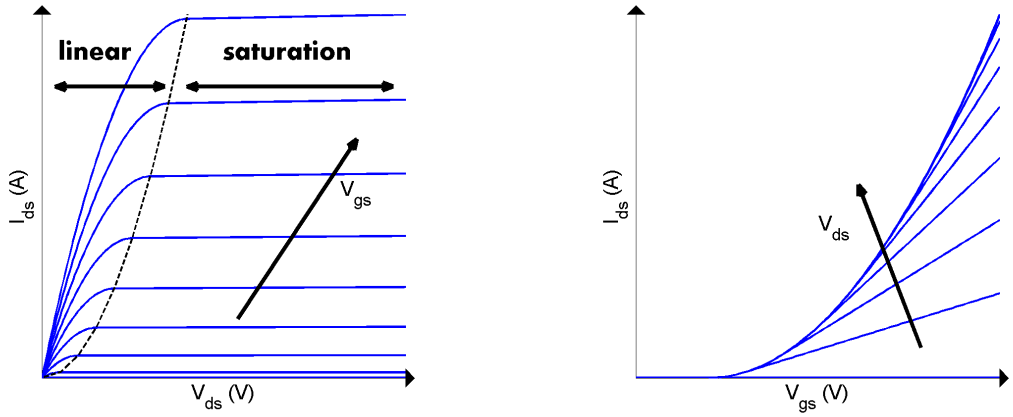
forming a conductive channel between the source- and drain-electrode. The reason for the accumulation of charges lies in the fact that the dielectric builds a plate-capacitor-like-structure together with the gate-electrode and the channel. Therefore, by polarizing the dielectric, the charge carrier density on the surface of the semiconductor is tuned by an electric field. A TFT is, in general, either operating in the cut off, the linear or the saturation region. In the cut off region, where the gate-source voltage is lower than the threshold voltage (V_t), a leakage off-current (I_{off}) flows from the drain-electrode to the source-electrode. As soon as the gate-source voltage becomes equal to, or larger than the threshold voltage, charge carriers begin to accumulate at the surface of the semiconductor, forming a conductive channel between the source- and the drain-electrode. A current, the drain-source current (I_{ds}), is able to flow through the formed channel and rises with the gate-source voltage. In addition, as long as the voltage drop between the drain- and source-electrode (drain-source voltage (V_{ds})) is smaller than or equal to the saturation voltage ($V_{ds,sat} = V_{gs}$ - V_t), the TFT behaves like a resistor and the drain-source current rises linearly with the drain-source voltage. If the drain-source voltage is further increased to values larger than the saturation voltage, the drain-source current saturates, since the channel is pinching off. At this pinch off point, the region on the drain side becomes depleted; however, electrons can still drift from the source-electrode to the drain-electrode because of the presented high electrical fields, as well as high carrier velocity at the drain-electrode. [76]

The output curve (Figure 2.2a) of a transistor shows the different operating regions. To obtain the output curve, the gate-source voltage is fixed at a certain value and the drain-source current is plotted against the drain-source voltage. The saturation current of a transistor is ideally dependent on the gate-source voltage, rather than on the drain-source voltage. In the case of the transfer curve (Figure 2.2b), the drain-source voltage is kept constant while the drain-source current is plotted against the gate-source voltage. Thereby, the drain-source current is described by the following equation, well known from literature and implemented in the Shichman-Hodges transistor model (Level 1 model): [76, 77]

$$I_{ds} = \begin{cases} I_{off}\, \exp\left(-\dfrac{\ln 10}{SS}\,(V_{gs} - V_0)\right) & V_{gs} < V_t, \\ \dfrac{W}{L}\,\mu_{fet}\,C_g\left(V_{gs} - V_t - \dfrac{V_{ds}}{2}\right) V_{ds}\,(1 + \lambda\, V_{ds}), & V_{gs} \geq V_t \text{ and } V_{ds} \leq V_{ds,sat}, \\ \dfrac{1}{2}\,\dfrac{W}{L}\mu_{fet}C_g\,(V_{gs} - V_t)^2\,(1 + \lambda\, V_{ds}) & V_{gs} \geq V_t \text{ and } V_{ds} > V_{ds,sat}, \end{cases} \tag{2.2}$$

where SS is the subthreshold slope and the onset voltage (V_0) determines at which gate-source voltage level the drain-source current of the transistor starts to rise. In some cases, an increase in the drain-source current with drain-source voltage is observed in saturation. This is where, due to the pinch off effect, the effective channel length of the transistor reduces with increasing the drain-source voltage and described through the channel length modulation parameter (λ).

However, by using Equation 2.2, the extracted values for the field-effect mobility are only valid in either the linear, or the saturation region. In the saturation region, the



(a) (b)

Figure 2.2.: Exemplary (a) output and (b) transfer curves of a TFT.

field-effect mobility is discribed by:

$$\mu_{fet} = \left(\frac{d\sqrt{I_{ds}}}{dV_{gs}}\right)^2 \frac{2\,L}{W\,C_g}. \tag{2.3}$$

Nevertheless, it is more suitable to calculate the field-effect mobility value in the linear region. The value of the field-effect mobility might be underestimated in the saturation region because of parasitic effects. Therefore, it is suggested to estimate the field-effect mobility value in the linear region: [11]

$$\mu_{fet} = \frac{dI_{ds}}{dV_{gs}} \frac{L}{WC_gV_{ds}}. \tag{2.4}$$

To extract the threshold voltage, the square root of the drain-current is plotted against the gate-source voltage, at the highest drain-source voltage. At the maximum slope, the linear part of the $\sqrt{I_{ds}}$-plot is extrapolated until intercepting with the x-axis, which is the value of the threshold voltage (Figure 2.3a). By plotting the drain-source current in logarithmic scale (Figure 2.3b), at the highest drain-source voltage, the subthreshold slope, the off-current, as well as the on-current, are extracted. The off-current and the on-current (I_{on}) are the minimum and maximum current values, respectively. However, an important parameter is the I_{on}/I_{off}-ratio which shows over how many orders of magnitude the current changes in a TFT. The steepest slope over one decade of the logarithmic I_{ds}-curve is known as the subthreshold slope, which is an indicator of how quickly the TFT switches from the off-state to the on-state.

The parameter λ is extracted from the output curve at the maximum gate-source voltage, where the saturation region is extrapolated until crossing with the x-axis. At the intercept with the x-axis, the voltage value V_a is obtained (Figure 2.4) and used to estimate the parameter λ: [11, 76]

$$\lambda = \frac{1}{V_a}. \tag{2.5}$$

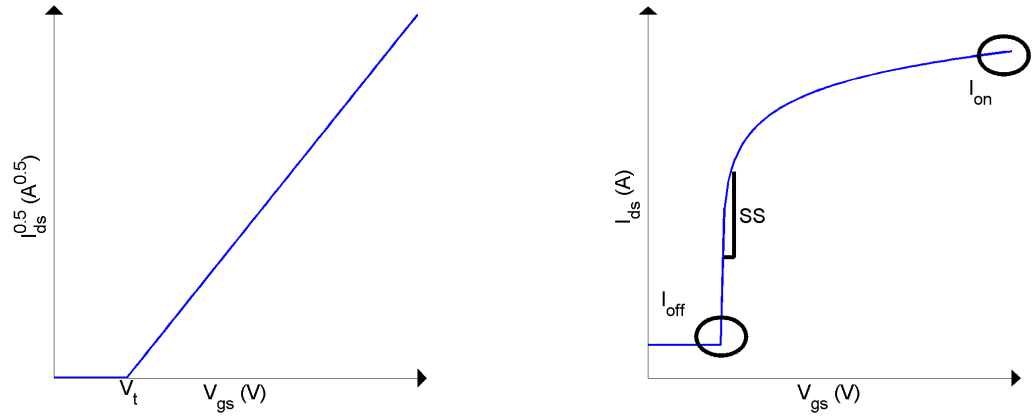


Figure 2.3.: (a) Extracting the threshold voltage of a TFT by plotting $\sqrt{I_{ds}}$ versus the gate-source voltage. (b) Transfer curve in logarithmic scale, at highest potential, to estimate key parameters in TFTs

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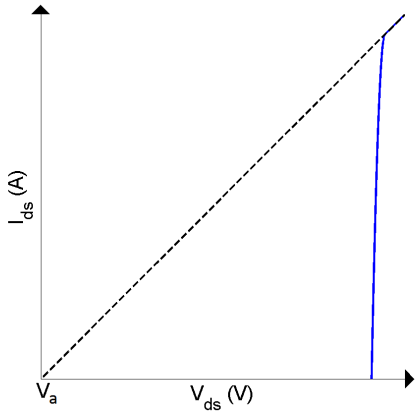


Figure 2.4.: Output curve of a FET at maximum gate-source voltage with extrapolated saturation region.

A further important parameter of a TFT is the transconductance (g_m) (Equation 2.6). The transconductance demonstrates how a small change in the gate-source voltage affects the drain-source current and is useful in a small signal replacement circuit of a TFT, where the TFT is considered to be a current source:

$$g_m = \left.\frac{dI_{ds}}{dV_{gs}}\right|_{V_{ds}>V_{ds,sat}} . \tag{2.6}$$

2.2. Metal oxide electronics

Recently, transparent conducting oxides (TCOs), and transparent semiconducting oxides (TSOs) have proven to be an interesting alternative to organic materials in PE. The reason for the popularity of these oxides lies in the fact that these materials show better electrical characteristics than organic based materials. Although, high performance oxides are found for vacuum processed oxides in literature [53], the focus will remain on oxides that are incorporated into a solution process, since the devices presented in this thesis are fabricated with an inkjet printer. As seen in the following subsections, dielectrics, conductors, as well as semiconductors are available as oxides, which enables the possibility of oxide only circuit designs.

2.2.1. Conductors

In an all oxide TFT, the drain- and source-electrodes are based on a TCO. Also, in microelectronic circuits, TCOs are used as contact pads and conductive interconnects. [53] In a different application, a window coated with a TCO is easily defrosted by driving a high current through the TCO film. [78]

The conduction type of TCOs are chosen in accordance to the application. In a pn-junction, the p-type TSO is in contact with a p-type TCO, while the n-type TSO is contacted through an n-type TCO, in order to avoid offsets in the band structure, or recombination centers. However, achieving either p-type TCOs or TSOs is still challenging because of the strongly localized oxygen orbitals in oxides, as will be discussed in more detail in Section 2.2.3. [53, 79] Unfortunately, solution processed TCOs are lacking in conductivity, which is the reason that TCO based structures are mainly fabricated with a vacuum process. [80, 81]

Although a wide variety of n-type TCOs are found in literature [53, 82], the focus will stay on indium tin oxide (ITO). ITO is essentially indium doped tin oxide ($Sn:In_2O_3$) and exhibit conductivity values as high as 5900 $S\,cm^{-1}$. [80] However, Jeong et al. reports a conductivity of $\sim$ 65 $S\,cm^{-1}$ for an inkjet printed ITO film. [83] The conductivity of p-type TCO is lower compared to their n-type counterparts. One of the highest conductivity values for p-type TCO is achieved with nickel (II) oxide (NiO) based films ($\sim$ 7 $S\,cm^{-1}$). [80, 84]

2.2.2. Dielectrics

In TFTs or, in a more general point of view, FET structures, the charge carrier density inside the semiconductor channel is controlled by an electrical field. As discussed before, a capacitor is formed between the gate and the channel of the TFT. [76] The dielectric is polarized by the electrical field separating the charges, where the positive charge carriers align in the direction of the electrical field and the negative charge carriers in the opposite direction. [85] The dielectric of choice, in TFTs, has been SiO_2 because of its favorable insulating characteristics, e.g. the band gap (E_g) is $\sim$ 9 eV and breakdown occurs at values $>$ 10 $MV\,cm^{-1}$. Nevertheless, SiO_2 has a low dielectric constant of 3.9. [53]

In all kind of TFTs, the driver capability is directly proportional to the gate-capacitance (C_g). The equation for estimating the capacitance value (C) of a parallel capacitor

clearly suggests that, to increase the capacitance, either the thickness of a dielectric is reduced, or the value of the dielectric constant is increased:

$$C = \frac{\kappa\, e_0}{d}, \tag{2.7}$$

where ϵ_0 is the electronic constant and κ is the dielectric constant. However, reducing the thickness of the dielectric is demanding because defects in the film leads to shorts. For that reason, high-κ dielectrics are introduced to increase the gate-capacitance of TFTs while maintaining thick dielectric films, which in addition relaxes the fabrication. Unfortunately, high-κ dielectrics typically have a lower band gap, since the dielectric constant is inversely proportional to the band gap. The low band gap can give rise to the leakage gate-current (I_g) of a TFT. Additionally, the offset between the valence band maximum (VBM), in p-type TFTs, or conduction band minimum (CBM), in n-type TFTs, of the dielectric and the semiconductor is $\geq$ 1 eV, to reduce leakage due to Schottky emission. [53, 85]

Table 2.1 summarizes important high-κ dielectrics, beneficial in increasing the gate-capacitance of TFTs fabricated through a solution process. With a band gap of 8.8 eV, aluminum oxide (Al_2O_3) is a high-κ dielectric feasible for TFTs. [53] The group of Prof. Park is able to fabricate solution-based Al_2O_3 films with dielectric constant values of 8.37, at annealing temperatures of only 60 °C. [86] Since the process temperature of these Al_2O_3 films is relatively low, paper or plastic foils are conceivable substrate choices. The band gap of yttrium oxide (Y_2O_x) is slightly lower ($\sim$ 6.5 eV), but the dielectric constant is nearly doubled compared to Al_2O_3 dielectric; however, the process temperature is within 300 - 500 °C, which is considerably high. [87] By further decreasing the band gap to values around 6 eV, spin coated hafnium oxide (HfO_2) films, annealed at 200 °C, with a dielectric constant of 10.2, are found to be suitable for TFTs. [53, 88] Titanium (IV) oxide (TiO_2) has the lowest band gap value ($\sim$ 3.5 eV). In addition, a dielectric constant value of 27 is found in literature for TiO_2 spin coated films annealed at 250 °C. [53, 88]

Table 2.1.: Popular dielectrics used in solution processed TFTs.

Material	Temperature (°C)	E_g (eV)	Breakdown ($V\,cm^{-1}$)	κ	Reference
SiO_2	200-300	9	$> 10 \times 10^6$	3.9	[53]
Al_2O_3	60	8.8	$> 6 \times 10^6$	8.37	[53, 86]
Y_2O_x	300-500	$\sim$ 6.5	-	$\sim$ 16	[53, 87]
HfO_2	200	6	$\sim 6 \times 10^6$	10.2	[53, 88]
TiO_2	250	$\sim$ 3.5	-	27	[53, 89]

2.2.3. Semiconductors

Besides a conductor and a dielectric, TFTs are also based on a semiconductor. It is well known that a TFT with an oxide semiconductor channel exhibits a higher field-effect mobility value than with amorphous silicon or an organic semiconductor. [53, 90, 91] Furthermore, oxide semiconductors are printable, show high optical transparency, and are stable under ambient conditions. [53] In the following, a few n- and p-type oxide semiconductors, suitable as channel material in TFTs, are presented. In general, n-type

TFTs are used for high performance applications, while p-type TFTs lack in performance. As consequence, n-type only circuit designs are very common in oxide electronics. [80]

The purpose of the following subsections is to give an overview on the most popular oxide semiconductors used in TFTs, rather than to compare the performance of these TFTs. For a more complete overview on oxide semiconductors, literature is referred to [53, 92, 93]. Nevertheless, the complete material stack must be taken into account when TFTs are evaluated, since all materials, especially their interfaces with each other, defines the electrical characteristics of such TFTs. [94] Although electrolyte-gating is a more efficient gating method (Section 2.3), just dielectric-gating is considered here, since the focus is on the oxide semiconductor itself.

n-type oxide semiconductors

The unique band structure of metal oxides provides n-type oxide semiconductors with good conductivity, large mobility and high optical transparency. In general, the valence band of metal oxides is formed by the bonding, as well as by the non-bonding occupied oxygen 2p orbital and the conduction band by the anti-bonding metal ns orbital (n denotes the quantum number) interaction with the oxygen 2p orbital. Herein, the metal ns orbitals are spatially wide-spread, while the oxygen 2p orbitals are strongly localized. Neighboring metal ns orbitals can easily overlap with each other and raise the electronic properties of such metal oxides. Due to strongly localized oxygen 2p orbitals, p-type conduction is difficult in metal oxides and, for the same reason, TFTs based on metal oxides do not operate in inversion mode. [53, 79, 95–98]

Binary compounds like zinc oxide (ZnO) or indium oxide have excellent electrical properties, making them beneficial as channel material in TFTs. [53] As an example, a TFT fabricated at RT with sputtered ZnO channel and silicon oxynitride (SiO_xN_y) gate-insulator shows a field-effect mobility of around 70 $cm^2\,V^{-1}\,s^{-1}$. The threshold voltage and the subthreshold slope are 1.8 V and 0.68 $V\,dec^{-1}$, respectively. Also the on-current ($\sim 10^{-3}$ A) and the off-current ($\sim 10^{-9}$ A) are reasonable. It is also possible to integrate the ZnO into a solution process. Neverthless, the field-effect mobility of the TFT drops to 1.02×10^{-3} $cm^2\,V^{-1}\,s^{-1}$ when the ZnO is solution-processed and thermally annealed at 180 °C. A reduction of the field-effect mobility is expected for solution-processed TFTs, since these thin films have a less beneficial microstructure, e.g. grain size, porosity and crystallization, compared to vacuum processed thin films. In addition, SiO_2 is used as gate-insulator, which further reduces the field-effect mobility, since the interface between the insulator and the channel plays a crucial role in defining the field-effect mobility of a TFT. [94] On the other hand, Han et al. proves that indium oxide is a very interesting material as an active layer (semiconductor) for solution-processed TFTs. A solution-processed TFT with an In_2O_3 channel annealed at 500 °C achieves field-effect mobility values around 55 $cm^2\,V^{-1}\,s^{-1}$. [91]

Also, tertiary and quaternary compounds like zinc tin oxide (ZnSnO) or indium gallium zinc oxide (InGaZnO), respectively, are used in solution-processed and/or printed TFTs. Sykora et al. shows in a TFT with printed ZnSnO channel a field-effect mobility value of 7.8 $cm^2\,V^{-1}\,s^{-1}$, annealed at a high temperature of 500 °C. [99] On the other hand, indium gallium oxide (InGaO) films cured at 350 °C are utilized in TFT structures in combination with scandium zirconium oxide ($S_{c1}Z_{r1}O_x$) dielectric. Measurements on

these printed InGaO based TFTs show excellent electrical properties, e.g. the field-effect mobility is reported to be 12 $cm^2\,V^{-1}\,s^{-1}$. [100] It has been proven that indium zinc oxide (InZnO) films are very interesting for low temperature processes (250 °C), exhibiting field-effect mobility values around 11 $cm^2\,V^{-1}\,s^{-1}$. [101] Less beneficial is that the InZnO TFTs operate in depletion mode (negative threshold voltage), probably because of the large charge carrier density inside the channel. The quaternary compound InGaZnO, heated at 300 °C and implemented in a TFT, has a field-effect mobility as low as 1.41 $cm^2\,V^{-1}\,s^{-1}$. The electrical performance of the InGaZnO based TFT is further improved by confining a layer of indium tin zinc oxide (InSnZnO) between the channel and the dielectric. With this confining layer, the field-effect mobility is improved to 12 $cm^2\,V^{-1}\,s^{-1}$, at an annealing temperature of 350 °C. The reason for the improvement is that the band structure of the InSnZnO and InGaZnO align very well, since a barrier controlling the electron flow is formed at the InSnZnO/InGaZnO interface. [102]

All electrical parameters of the before-presented TFTs are summarized in Table 2.2. Besides that, also the required annealing temperatures are considered in order to be compatible to the assigned substrates. If flexible substrates like plastic or paper are desired, then annealing temperatures of $\sim$ 150 °C are acceptable. [103] Nevertheless, flexible polyimide substrates can also sustain temperatures up to 350 °C. Higher temperatures up to 600 °C are only allowed for rigid substrates. [104]

Table 2.2.: Material stack and key electrical properties of different n-type oxide based TFTs.

Channel	Insulator	Stack	μ_{fet} ($cm^2\,V^{-1}\,s^{-1}$)	V_t (V)	I_{on}/I_{off}	SS ($V\,dec^{-1}$)	Year
ZnO	SiO_xN_y	BG	70	1.8	2×10^5	0.68	2004 [105]
ZnO	SiO_2	BG	0.001	18	-	-	2008 [94]
In_2O_3	SiO_2	BG	55.26	-	$\sim 10^7$	-	2011 [91]
ZnSnO	SiO_2	BG	7.8	7.0	3.2×10^8	0.35	2016 [99]
InGaO	$S_{c1}Z_{r1}O_x$	TG	12	~ 0.0	5.8×10^6	0.12	2018 [100]
InZnO	SiO_2	BG	~ 11	~ -1.0	$\sim 10^6$	~ 0.42	2010 [101]
InGaZnO	SiO_2	BG	1.41	1.0	4.3×10^7	0.37	2011 [106]
InSnZnO/ InGaZnO	SiO_2	BG	22.16	~ 5.29	$\sim 10^7$	0.51	2014 [102]

p-type oxide semiconductors

At the same time at which the band structure is beneficial to n-type oxide semiconductors, it is disadvantageous to the electronic properties of p-type metal oxides. The reason for that lies in the fact that the valance band is formed by strongly localized oxygen 2p orbitals. Oxygen, in general, has a high electronegativity, causing a large effective hole mass and low carrier mobility. [53, 79, 95–98]

To overcome the limitations of p-type metal oxides, the band structure of the oxides needs to be changed. One popular approach is to introduce a metal with a fully filled 3d shell, which has a similar energy level as the oxygen 2p orbital. In this regard, copper is a promising candidate. The valence band of copper (II) oxide (CuO) is formed by the

copper 3d orbital and the oxygen 2p orbital, while the conduction band is formed by the copper 4s orbital. [53, 79, 95, 96]

Therefore, the main focus in p-type metal oxides lies in copper compounds. [79, 107] For example, Sung et al. reports on a TFT with a sputtered, 200 °C annealed CuO thin film channel and a field-effect mobility of 0.40 $cm^2 V^{-1} s^{-1}$. [108] A TFT with sputtered copper (I) oxide (CuO_2) film, annealed at 200 °C, with a field-effect mobility as high as 3.6 $cm^2 V^{-1} s^{-1}$, but a low I_{on}/I_{off}-ratio of only $\sim 2 \times 10^{-2}$, is also found in literature. [109] The I_{on}/I_{off}-ratio is reduced, since the CuO_2 films show high intrinsic conductivity, resulting in a higher off-current. [108] In CuO_2 based TFTs, it is demonstrated that it is possible to integrate copper oxide based TFTs in a solution process. However, due to the solution process, the field-effect mobility drops to 0.16 $cm^2 V^{-1} s^{-1}$, although the film is annealed at 400 °C. [110] Also, copper chromate ($CuCrO_4$), cuprous thiocyanate (CuSCN), and/or copper (I) iodide (CuI) are considered to be channel materials, but do not add any significant progress in improving the field-effect mobility of copper oxide based p-type TFTs; the field-effect mobility is, in all presented cases, below 1 $cm^2 V^{-1} s^{-1}$. [95, 111, 112]

Next, tin (I) oxide (SnO) based devices have proven to be an interesting p-type semiconductors for TFT applications. The reason for the increasing popularity of SnO is that this material shows reasonable hole mobility, as well as high charge carrier density because of the spherically spread 5s orbitals. [97] As one example, an ambipolar TFT with pulsed laser deposited SnO channel and SiO_2 dielectric is reported in literature. The field-effect mobility in this TFT is 0.78 $cm^2 V^{-1} s^{-1}$, slightly higher compared to similar stacked CuO based TFTs. [97] Nevertheless, by optimizing the crystalline structure, it is even possible to achieve field-effect mobility values upwards to 6 $cm^2 V^{-1} s^{-1}$ in SnO based TFTs. [113] Although tin (IV) oxide (SnO_2) phase is thought to be n-type in nature, p-type conduction is achieved by tuning the annealing temperature. The SnO_2 phase is already achieved by annealing the films at 100 °C, but the field-effect mobility is only 0.011 $cm^2 V^{-1} s^{-1}$, in comparison to SnO-based TFTs. In addition, the TFT based on SnO_2 operates in depletion mode, which is attributed to the high carrier density inside the material. [114] However, a solution-processed SnO based TFT shows a field-effect mobility of 0.13 $cm^2 V^{-1} s^{-1}$, which is too low for the use in printed oxide based CMOS-like designs. [115] Also here, the threshold voltage is large (≤ -10 V) but tunable by the choice of the dielectric. In this regard, the threshold voltage of SnO based TFTs is lowered by changing the gate-dielectric, e.g. the threshold voltage is reduced to -0.3 V with a Al_2O_3-based dielectric. [116]

Recently, Kim et al. made a huge step in optimizing the performance of p-type oxide semiconductors. The compound of copper (I) iodide and tin (I) oxide (a-CuSnI) shows p-type behavior with a hall mobility (μ_{hall}) around 9 $cm^2 V^{-1} s^{-1}$. The obtained high hall mobility value is the result of the spatially spread large p-orbitals in a-CuSnI. [117] Therefore, a-CuSnI is an interesting candidate for p-type TFTs; however, this material is not employed in a TFT yet.

Table 2.3 summarizes the electrical properties of all discussed oxide p-type TFTs. One can see that some of the TFTs have a very low threshold voltage compared to the others. Over the last 10 years, many efforts have been made to improve the performance of p-type oxide TFTs but by comparing Table 2.2 and 2.3, it is obvious that it is difficult to design complementary circuits (e.g. CMOS like structures) in oxide electronics, since the p-type

Table 2.3.: Material stack and key electrical properties of different p-type oxide TFTs.

Channel	Insulator	Stack	μ_{fet} ($cm^2\,V^{-1}\,s^{-1}$)	V_t (V)	I_{on}/I_{off}	SS ($V\,dec^{-1}$)	Year
CuO	SiO_2	BG	0.40	-	1×10^4	-	2010 [108]
Cu_2O	Al_2O_3	BG	3.60	-12.0	2×10^2	-	2010 [109]
Cu_2O	SiO_2	BG	0.16	-	1×10^2	-	2013 [110]
CuI	SiO_2	BG	0.44	35	5×10^2	-	2018 [111]
$CuCrO_2$	SiO_2	BG	0.59	- 32.81	1×10^5	5.66	2018 [95]
CuSCN	PVDF	TG	0.18	- 1.7	-	1.6	2018 [112]
SnO	SiO_2	BG	0.78	-3.8	-	1.19	2011 [97]
SnO_2	SiO_2	BG	0.011	30.4	$\sim 10^3$	$\sim$ 2.0	2008 [114]
SnO	HfO_2	BG	5.87	-1.0	$\sim 10^3$	7.63	2013 [113]
SnO_x	Al_2O_3	BG	1.6	-0.3	$\sim 10^4$	-	2018 [116]
SnO	SiO_2	BG	0.13	-1.9	85	-	2012 [115]

TFTs are lacking in performance compared to their n-type counterparts. Furthermore, TFTs with indium oxide as channel material shows the best electrical characteristics among the oxide semiconductors and is therefore preferably used to fabricate devices in this thesis.

2.3. Electrolyte-gating

As previously mentioned, electrolytes are an interesting alternative to the dielectrics introduced in Section 2.2.2. These electrolytes can easily take into account the surface roughness of the printed semiconductor, improving the interface properties. TFTs with an electrolyte as the gating approach show high gate-capacitance values (1-10 μFcm^{-2}), reducing the supply voltage requirements to $\sim$ 1 V. An electrolyte is a salt dissolved in a polar solvent, and is in liquid phase. Inside the solvent, the negatively charged ions (anions) got disassociate form the positively charged ions (cations), due to a force ($F = q \cdot E$) applied to the ions, and caused by an electrical field. By adding a polymer to the electrolyte, it is possible to solidify the electrolyte such that it is used as the gating material in TFT structures. However, by mixing a polymer into the electrolyte it must be ensured that the ion mobility stays sufficiently high. [38] Various kind of electrolytes are found in literature, where the main difference lies in the size of the ions or the level of solidification of the electrolyte. [57, 79, 110, 118]

In a TFT, the electrolyte forms together with the gate and the channel, a capacitor-like structure. When a negative potential is applied to the gate, cations are attracted to the gate/electrolyte interface and the anions to the electrolyte/semiconductor interface, due to an internal electrical field (Figure 2.5a). In the case of an n-type semiconductor, as will be used in this thesis, the anions push away the electrons from the surface of the semiconductor leaving behind spatially fixed positive donor atoms. Therefore, it is not possible to drive a current from the drain- to the source-electrode. Ideally, if no voltage is applied to the gate-electrode, the electrolyte is in neutral state and no accumulation of charge carriers occurs inside the semiconductor, thereby preventing a

current from flowing inside the channel (Figure 2.5b). Finally, if a positive voltage is applied to gate electrode, anions get attracted to the gate/electrolyte interface, and at the same time cations gather at the electrolyte/semiconductor interface, because of the internal electrical field. The cations at the electrolyte/semiconductor interface lead to the accumulation of electrons on the surface of the channel, forming a channel between the drain- and source electrodes (Figure 2.5c). The formed channel, allows a current to flow between the drain- and the source-electrode, which magnitude depends on the voltage drop between these electrodes (drain-source voltage). [38, 110]

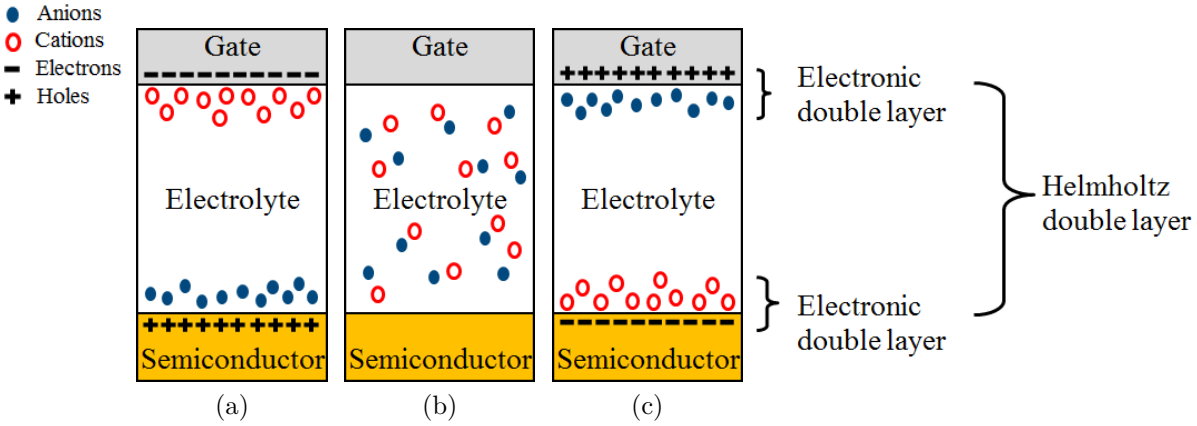


Figure 2.5.: Distribution of charge carriers in an electrolytic system when (a) negative biased, (b) unbiased and (c) positive biased.

As it is seen from Figure 2.5, at the gate/electrolyte as well as at the electrolyte/semiconductor interfaces, charge carriers form an electronic double layer (EDL) with ions of opposite signs. Each of the EDLs are understood as an individual plate capacitor where the distance of the plates is the thickness of the EDL layer. The thickness of the EDL layer is in the range of the solvation shell of the ions ($\sim$ 1 nm), and a dielectric constant value of $\sim$ 10 is realistic. [110] The electrical field inside the electrolyte can reach values up to 10 MVcm^{-2}. [38] Both EDLs are known as the Helmotz double layer (HDL) and the area between the EDLs is ideally in neutral state and non-conducing. Nevertheless, due to impurities inside the electrolyte, a negligible leakage current flows from the gate towards the semiconductor. [110] It is also observed that the density of ions decrease exponentially from the respective interface forming a diffusion layer called the Gouy-Chapman layer, increasing the leakage current. Otto Stern adopted both approaches in his model for describing the behavior of electrolytes in 1924. [119]

In general, the electrolyte system is described through the equivalent circuit in Figure 2.6. The equivalent circuit consists of the electrolyte resistance (R_{el}), the EDL capacitance at the gate/electrolyte interface ($C_{g/el}$), and the EDL capacitance at the electrolyte/semiconductor interface ($C_{el/sc}$). By increasing the gate-electrode area to a size bigger then the semiconductor area, the EDL capacitance at the gate/electrolyte interface becomes much bigger compared to the EDL capacitance at the electrolyte/semiconductor interface. Consequently the EDL capacitance at the gate/electrolyte interface is negligible. For this reason, the voltage drop between the gate-electrode and the semiconductor happens mostly at the electrolyte/semiconductor interface, pushing more charge carriers

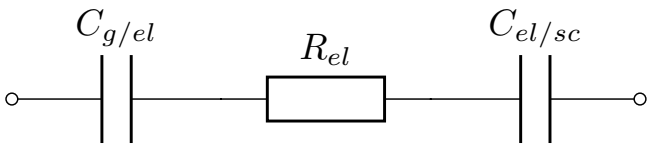


Figure 2.6.: Equivalent circuit of the electrolyte used as gate dielectric.

into the formed channel because of a higher electrical field. The electrolyte resistance is estimated with the help of the specific conductivity of the electrolyte (σ_{el}):

$$\sigma_{el} = q\,(n_{cation}\,\mu_{cation} - n_{anion}\,\mu_{anion}), \tag{2.8}$$

where q is the elementary charge, n_{cation} is the density of the cations, n_{anion} is the density of anions, μ_{cation} and μ_{anion} the mobility of the cations and anions, respectively. Finally, to estimate the value for the electrolyte resistance, the area (A) as well as the length (L_{el}) of the electrolyte structure needs to be known: [38]

$$R_{el} = \frac{L_{el}}{\sigma_{el}\,A} \tag{2.9}$$

For reliable circuit design, the equivalent circuit shown in Figure 2.6 is adjusted because of the frequency dispersion behavior of the electrolyte. [120] At low frequencies, a considerable number of ions do not drift in response of the electrical field, forming the Gouy-Chapman layer and lowering the ion conductivity. [38, 121] To consider the frequency dispersion behavior of the electrolyte, the two EDL capacitances are summarized in one constant phase element (Z): [120, 122]

$$Z = \frac{1}{(j\omega)^{\delta} Q_{dl}}, \qquad 0 < \delta \geq 1, \tag{2.10}$$

where δ is the non-ideal factor of the EDL. In addition, the gate resistance (R_g) is added to the equivalent circuit (Figure 2.7).

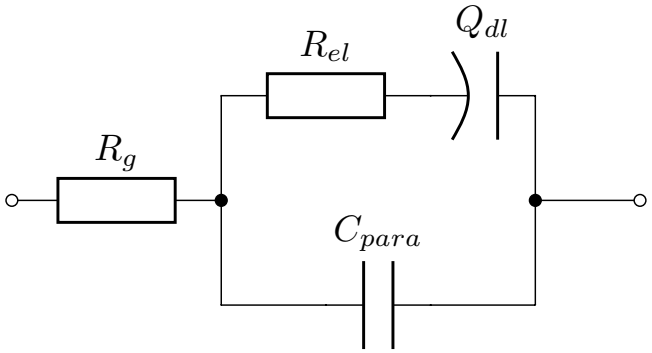


Figure 2.7.: Adjusted equivalent circuit of the electrolyte used in an EGFET.

With the help of Figure 2.7 and Equation 2.10, the overall impedance of the electrolytic system (Z_{tot}) is estimated to:

$$Z_{tot} = R_g + \frac{R_{el} \cdot (j\omega)^{\delta} Q_{dl} + 1}{(R_{el} \cdot (j\omega)^{\delta} Q_{dl} + 1)\, j\omega C_{para} + (j\omega)^{\delta} Q_{dl}} \tag{2.11}$$

For transient analysis, the electrolyte is seen as a RC-network and the charging time of the electrolyte is described through the Maxwell relaxation time (τ_{el}):

$$\tau_{el} = \frac{\kappa\,\epsilon_0}{\sigma_{el}} = R_{el}\,C_{tot} \tag{2.12}$$

where C_{tot} ($\approx \frac{1}{C_{g/el}} + \frac{1}{C_{el/sc}}$) is the overall capacitance of the electrolyte. It is worth mentioning, here, that Equation 2.12 can only be applied for TFTs, if the formation of the channel is much faster then charging of the electrolyte, otherwise the time constant for forming the channel would dominate the switching speed of the TFT. [38]

3. Modeling in printed electronics

As previously discussed, there are many different materials available to fabricate a TFT in PE. Besides that, different fabrication processes yield different device characteristics. However, for designing applications it is very important to have reliable and predictive transistor models. These transistor models are integrated into a design tool kit and support circuit designers in developing new applications. [64] As numerous the materials and processes are, as many transistor models exist in PE. Therefore, there is no universal model available and the choice of the model is always in accordance with the transistor technology.

In the following, the most accepted transistor models are presented. The Level-1 model (Equation 2.2) is very popular to describe printed TFTs but it lacks in accuracy since the dependency of the field-effect mobility from the gate-source voltage is not captured. To improve the fit of the field-effect mobility behavior, polycrystalline and amorphous TFT models are used, since polycrystalline and amorphous structures are dominant in PE. Polycrystalline and amorphous TFT models are more suitable to mimic the behavior of printed TFTs, because charge trapping is taken into account. [123] Another popular approach to model printed transistor is to use empirical models which do not consider physical effects, nor device structures.

3.1. Unified model and parameter extraction

The unified model and parameter extraction method (UMEM) is very popular in PE because it has the ability to accurately fit the DC characteristics of printed TFTs, and provides a straight forward parameter extraction scheme. The unified model is originally developed for polycrystalline and amorphous TFTs and describes the drain-source current through the following set of equations: [124, 125]

$$I_{ds} = \begin{cases} \dfrac{W}{L}\,\mu_0\,n_0\,\eta\,V_{th}\,e^{\frac{V_{gs}-V_t}{\eta\,V_{th}}}\left(1-e^{-\frac{V_{ds}}{\eta\,V_{th}}}\right) & V_{gs} < V_t \text{ (cut off)}, \\ \dfrac{W}{L\,f_r}\,\mu_{fet}\,C_g\left((V_{gs}-V_t)\,V_{ds}-\dfrac{V_{ds}^2}{2\,\alpha_{sat}}\right) & V_{ds} < \alpha_{sat}\,(V_{gs}-V_t) \text{ (linear)}, \\ \dfrac{W}{L\,f_r}\,\mu_{fet}\,C_g\,(V_{gs}-V_t)^2\,\alpha_{sat} & V_{ds} \geq \alpha_{sat}\,(V_{gs}-V_t) \text{ (saturation)}, \end{cases} \tag{3.1}$$

where n_0 is the surface minority carrier inside the semiconductor, μ_0 is the field-effect mobility value in the subthreshold region, η is a constant, V_{th} is the thermal voltage and α_{sat} is the saturation modulation parameter. The function f_r is required to model the

series resistance of the source- and drain-electrodes: [124]

$$f_r = 1 + R_{total}\,\frac{W}{L}\,\mu_{fet}\,\mu_0\,C_g\left(\frac{V_{gs}-V_t}{V_{aa}}\right)^{\gamma}\,(V_{gs}-0.5\,V_{ds}), \tag{3.2}$$

where V_{aa} and γ are empirical parameters, while R_{total} is the combined source and drain series resistances. However, the equations for the linear and saturation regions is simplified to only one equation: [124]:

$$I_{ds} = \frac{W}{L\,f_r}\,\mu_{fet}\,C_g\,\frac{(V_{gs}-V_t)\,V_{ds}(1+\lambda V_{ds})}{\left(1+\left(\frac{V_{ds}}{0.5\,\alpha_{sat}\,(V_{gs}-V_t)}\right)^{m}\right)^{\frac{1}{m}}}, \tag{3.3}$$

where m is a constant to ensure continuity, and λ is the channel length modulation parameter.

In a polycrystalline TFT the field-effect mobility gets affected by the grain boundaries, since trap states cause charge carrier to deplete at the grain boundaries. [123] The field-effect mobility is described in a polycrystalline TFT by:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{00}} + \frac{1}{\mu_1}\left(\frac{n_0}{n_s}\right)^{m_\lambda}, \tag{3.4}$$

where μ_{00} is the maximum field-effect mobility value in a TFT, n_s is the sheet carrier density inside the semiconductor, μ_1 and m_λ are fitting parameters. [124]

On the other hand, in amporphous TFTs, the field-effect mobility is highly dependent on the applied gate-source voltage because most of the charge carriers get trapped. The reason for the trapping mechanisms in amorphous TFTs is that the atoms are randomly distributed, causing many energy states, even in the band gap. [123] The field-effect mobility for polycrystalline TFTs is described by:

$$\mu_{fet} = \mu_0\left(\frac{V_{gs}-V_t}{V_{aa}}\right)^{\gamma}, \tag{3.5}$$

where μ_0 is a fitting parameter. [126] Nevertheless, it is found that if the parameter γ is positive, the field-effect mobility rises with the gate-source voltage corresponding to amorphous conduction mechanism. On the other hand, if the parameter γ is negative, the field-effect mobility decreases with the applied gate-source voltage, typically found in pollycrystalline TFTs, since charge carrier scattering becomes important. Equation 3.5 turned out to be universal and also applicable to printed OFETs.[125]

The UMEM provide a straightforward extraction routine for the parameters required by the model. Firstly, to extract the parameters γ and V_t, the H-function is evaluated:

$$H = \frac{\int_0^{V_{gs}} I_{ds}(x)\,dx}{I_{ds}(V_{gs})}. \tag{3.6}$$

By approximating the linear part of the H-function with

$$H(V_{gs}) = \frac{V_{gs}-V_t}{1+\gamma}, \tag{3.7}$$

the parameter V_t is estimated by extrapolating Equation 3.7 until intercepting with the x-axis. The parameter γ is calculated through the slope of Equation 3.7 $\left(\approx \frac{1}{1+\gamma}\right)$. [124, 125, 127]

Next, $I_{ds}^{\frac{1}{1+\gamma}}$ is plotted against (V_{gs} - V_t) and with the help of its slope (Sl_1), V_{aa} is calculated: [124, 125, 127]

$$V_{aa} = \left(\frac{\frac{W}{L}\,\mu_0\,C_g\,V_{ds}}{Sl_1^{1+\gamma}} \right)^{\frac{1}{\gamma}}. \tag{3.8}$$

In a similar manner, the parameter α_{sat} is estimated. In the saturation region, $I_{ds}^{\frac{1}{2+\gamma}}$ is plotted against (V_{gs} - V_t) and α_{sat} is obtained through its slope (Sl_2): [124, 125, 127]

$$\alpha_{sat} = \frac{Sl_2^{2+\gamma}\,V_{aa}^{\gamma}\,\sqrt{2}}{\frac{W}{L}\,\mu_0\,C_g}. \tag{3.9}$$

The parameter m is attained by the following expression:

$$m = \frac{\log 2}{\log \frac{\frac{W}{L}\,\mu_0\,C_g}{V_{aa}^{\gamma}}\,\frac{\alpha_{sat}\,(V_{gs}-V_t)^{1+\gamma}}{I_{sat}}}, \tag{3.10}$$

where I_{sat} is the saturation current evaluated at $V_{ds} = \alpha_{sat}$ (V_{gs} - V_t). [124, 125, 127] In a last step, the channel length modulation parameter λ is directly calculated either by using Equation 3.1 in saturation, or by evaluating the slope of the output curve in saturation. [125]

One benefit of the UMEM is that the model is already implemented as Automatic Integrated Circuit Modeling SPICE (AIM-SPICE) Level 16 transistor model. Unfortunately, the high number of parameters makes the model complex and in many cases a simpler model is desired.

3.2. AIM-SPICE Level 15 transistor model

The AIM-SPICE Level 15 transistor model is likewise a popular model to simulate the DC behaviour of TFTs in PE. The model is developed for amorphous TFTs and relates the drain-source current to different sources of contributions, like the leakage current (I_{leak}) and the accumulation current (I_{ab}), by:

$$I_{ds} = I_{leak} + I_{ab}. \tag{3.11}$$

The leakage current is the current flow related to the intrinsic conductivity of the semiconductor and the accumulation current to the accumulation of charge carriers. Typically, in PE the TFTs operate only in accumulation mode, therefore no contribution from inversion is expected. [128]

The leakage current is described as:

$$I_{leak} = I_{\sigma,0}\,V_{ds}, \tag{3.12}$$

where $I_{\sigma,0}$ is the minimum leakage current. With the help of the channel conductance in the linear regime (g_{ch}), the accumulation current is calculated as follows: [128]

$$I_{ab} = g_{ch,0} \frac{V_{ds}}{\left(1 + \left(\frac{V_{ds}}{\alpha_{sat}\,(V_{gs}-V_t)}\right)^m\right)^{\frac{1}{m}}} (1 + \lambda\, V_{ds}), \tag{3.13}$$

To estimate the effective conductivity of the channel, the source series resistance (R_s), the drain series resistance (R_d) and the intrinsic conductivity of the channel ($g_{ch,i}$) are required: [128]

$$g_{ch,0} = \frac{g_{ch,i}}{1 + g_{ch,i}\,(R_s + R_d)}. \tag{3.14}$$

The intrinsic conductivity of the channel is described by: [128]

$$g_{ch,i} = q\, n_s \frac{W}{L} \mu_{fet}. \tag{3.15}$$

The parameters required for this model are extracted with the methods described previously. However, this model also requires a large number of parameters, and is therefore disadvantageous.

3.3. Variable range hopping model

In printed OFETs, the variable range hopping (VRH) model is able to describe the transport mechanism in organic semiconductors. Charge carriers in organic semiconductors are thermally activated and hop between localized states, which is modeled through the VRH. [123] One possibility to describe the drain-source current with the VRH model is by the following equation: [129]

$$I_{ds} = \frac{W}{L} \frac{a_1\, C_g}{b_1 + 2} \left(r^{b_1+2}(V_{gs} - V_t) - r^{b_1+2}(V_{gd} - V_t)\right), \tag{3.16}$$

where the parameters a_1 and b_1 are fitting parameters related to the field-effect mobility: [123, 129]

$$\mu_{fet} = a_1\, (V_{g,x} - V_t)^{b_1}, \tag{3.17}$$

where $V_{g,x}$ is the gate-voltage at the position x of the channel. The step function $r(x)$ is described as:

$$r(x) = \begin{cases} x, & x \geq 0 \\ 0, & x < 0. \end{cases} \tag{3.18}$$

This model is very interesting since the model complexity is reduced and, therefore, just a few number of parameters need to be extracted.

3.4. Charge drift model for electrolyte-gated field-effect transistors

Transistor models are also available to simulate EGFETs. A transistor model, developed for describing EGFETs based on an organic semiconductor, is assuming that the charge carrier transport takes place as drift under an electrical field. The nonlinear and voltage dependent double-layer capacitance, which is related to the gate-capacitance, is described as: [130]

$$C(V) = C_0 + C_v(V_{gt} - V(x))^{\chi}. \tag{3.19}$$

The double layer capacitance is based on a voltage independent capacitance (C_0), a voltage dependent capacitance (C_v) and an empirical parameter (χ). Since the potential inside channel is dependent on the location x, the parameter $V(x)$ captures this voltage dependency.

The charge drift transport model, describes the drain-source current at a location x inside the channel:

$$\frac{I_{ds}}{W} = \mu(x)\, Q(x)\, |E(x)|, \tag{3.20}$$

where all quantities, including the field-effect mobility, the charge carrier density (Q), and the electrical field (E) are dependent on the location at the channel. However, the field-effect mobility is simplified by Equation 3.5. [130]

With the help of Equation 3.19, the charge carrier density is estimated as,

$$Q(x) = C(V)(V_{gt} - V(x)) = C_0(V_{gt} - V(x)) + C_v(V_{gt} - V(x))^{\chi+1}, \tag{3.21}$$

and included in Equation 3.20 with $|E(x)| = \partial V(x)/\partial x$. The drain-source current is: [130]

$$\frac{I_{ds}}{W} = \mu_0 \left(C_0 \left(V_{gt} - V(x)\right)^{\gamma+1} + C_v(V_{gt} - V(x))^{\gamma+\chi+1} \right) \frac{\partial V(x)}{\partial x}. \tag{3.22}$$

By integrating Equation 3.22 along the channel, the drain-source current in the linear regime is estimated to be: [130]

$$I_{ds} = \frac{W\,\mu_0}{L} \left(C_0 \frac{V_{gt}^{\gamma+2} - (V_{gt} - V_d)^{\gamma+2}}{\gamma+2} + C_v \frac{V_{gt}^{\gamma+\chi+2} - (V_{gt} - V_d)^{\gamma+\chi+2}}{\gamma+\chi+2} \right). \tag{3.23}$$

In saturation regime, the expression $(V_{gt} - V_d)$ is negligible and the drain-source current is: [130]

$$I_{ds} = \frac{W\,\mu_0}{L} \left(C_0 \frac{V_{gt}^{\gamma+2}}{\gamma+2} + C_v \frac{V_{gt}^{\gamma+\chi+2}}{\gamma+\chi+2} \right) (1 + \lambda(V_d - V_{gt})). \tag{3.24}$$

Unfortunately, the charge drift model is not able to model the subthreshold behavior of an EGFET because most of the charge carriers are trapped in the subthreshold regime.

Therefore, the subthreshold model is a slightly adjusted version of the traditional silicon based model for the subthreshold region: [130]

$$I_{ds} = \frac{W\,\mu_0\,C_0\,V_{ss}^2}{L}\exp\left(\frac{V_{gt}}{V_{ss}}\right)\left(1-\exp\left(\frac{-V_d}{V_{ss}}\right)\right) \tag{3.25}$$

Nevertheless, also for this model a smaller number of parameters is desirable.

3.5. Drift-diffusion modeling approach

Within Technology computer aided design (TCAD) simulations, it is possible to model the electrical behavior of a transistor with emphasis on the device physics. For an EGFET with an organic semiconductor channel, the behavior of the transistor is described through a set of physically motivated equations, e.g. drift-diffusion equations, continuity equation, as well as the Poisson equation: [131]

$$J_n = -q\,\mu_n\,\triangle\phi + q\,D_n\,\triangle n, \tag{3.26}$$

$$J_p = -q\,\mu_p\,\triangle\phi - q\,D_p\,\triangle p, \tag{3.27}$$

$$\triangle \cdot J_n = q(R-G), \tag{3.28}$$

$$\triangle \cdot J_p = -q(R-G), \tag{3.29}$$

$$\triangle \cdot (\epsilon_0\kappa\,\triangle\phi) = q(n-p+N_D^+-N_A^-+p_{At}), \tag{3.30}$$

where the electron current density (J_n), the hole current density (J_p), the elementary charge (1.602×10^{19} C) (q), the electron mobility (μ_n), the hole mobility (μ_p), the Laplace operator ($\triangle$), the electrostatic potential (ϕ), the electron diffusion coefficient (D_n), the hole diffusion coefficient (D_p), the recombination rate (R), the generation rate (G), the electronic constant (8.854×10^{12} F m^{-1}) (ϵ_0), the donor impurity concentration (N_D^+), the acceptor impurity concentration (N_A^-) and the density of trapped holes (p_{At}) are physical motivated parameters. To account for organic semiconductors, a Pool-Frenkel field-effect mobility is used: [131]

$$\mu = \mu_0(T)\,\exp\left(\sqrt{\frac{E}{E_0}}\right), \tag{3.31}$$

where E_0 is the effective parameter with a constant value of 3×10^5 V cm^{-1}. Besides adjusting the expression for the field-effect mobility, the band structure is modified in a way that holes are easily injected, to account for the p-type semiconductor. Furthermore, an interface trap model is used to describe the hopping transport mechanism. Also the Poisson-Boltzman equation is adopted in a form to match the gate-capacitance which arises from the electrolyte-gating: [131]

$$\triangle(\epsilon_o\,\kappa\,\triangle\phi) = -\sum_{i=1}^{N} z_i\,q\,c_{i,0}\exp\left(-\frac{z_i\,q\,(\phi-V_t)}{k_B\,T}\right), \tag{3.32}$$

where the parameters are the valency ion concentration (z), the bulk ion concentration ($c_{b,0}$), the Boltzmann constant (k_B), and the temperature (T).

This model is meant for a physical description, and is therefore not feasible for simulation program with integrated circuit emphasis (SPICE) simulations.

3.6. Table model

A table model is a purely empirical model and implemented in most SPICE simulators. In table modeling, the output and transfer characteristics of a TFT are stored in a table and accessed based on the voltages applied to the transistor terminals. Since the current values are directly stored, high accuracy between the measured and simulated data is expected. The huge advantage of such a modeling approach is that a circuit designer can design applications despite a physical or SPICE compatible model is not available, due to missing understanding of the underlying physics or the development of the model is ongoing work. Furthermore, no parameter extraction routines are required, since the measured current values are directly stored. A disadvantage of the table model is that it is less compact compared to other transistor models and no scaling is possible because the model is not accessible by parameters. [123]

3.7. Modeling the transition region

It is desirable to model the drain-source current with only one single equation to avoid discontinuities in the simulated transistor curves. Discontinuities lead to convergence issues during simulation. Unfortunately, most transistor models have different expressions between the sub- and above threshold regions. Therefore, strategies to model the transition region between the sub- and above threshold regions are important for reliable simulation. Typically, the subthreshold current (I_{sub}) and the above threshold current (I_{above}) is combined in the total current (I_{total}) as follows: [110, 132]

$$I_{total} = \frac{1}{\frac{1}{I_{sub}} + \frac{1}{I_{above}}}. \tag{3.33}$$

This approach is, however, not applicable for printed TFTs because the transition region spreads over a wide voltage range. [110] To overcome the issue of modeling a wide spread transition region, a transition function (f_t) is introduced: [133]

$$f_t(V_g, V) = V_{sub} \ln\left(1 + \exp\left(\frac{V_g - V - V_t}{V_{sub}}\right)\right). \tag{3.34}$$

The subthreshold voltage (V_{sub}) is obtained by: [133]

$$V_{sub} = \frac{dV_g}{d\ln(I_d)} \approx 0.43\,(\gamma + 2)\,SS. \tag{3.35}$$

It is possible to directly integrate the transition function into the drain-source current

equation by:

$$I_{total} = \frac{W}{L}\,\mu_0\,C_g\,\frac{f_t^{\gamma+2}(V_g, V_s - V_t) - f_t^{\gamma+2}(V_g, V_d - V_t)}{\gamma + 2}, \tag{3.36}$$

where the drain voltage (V_d) and the source voltage (V_s) serves as input for the transition function. [133]

However, the use of the transition function limits the choice of the subthreshold current equation to a subthreshold model which does not match with most of the printed TFTs. Therefore, a tangent hyperbolic transition function, may model the transition region accurately. A further benefit of the tangent hyperbolic transition function is that it is mathematically continuous. By using the tangent hyperbolic transition function, the total current is desecribed as: [110]

$$I_{total} = I_{above}\,\frac{1}{2}\,(1 - \tanh\,(B\,(V_{gs} - V_b))) + I_{sub}\,\frac{1}{2}\,(1 + \tanh\,(B\,(V_{gs} - V_b))). \tag{3.37}$$

Through the transition voltage (V_b) and transition parameter (B), the position and the degree of transition is tuned. [110]

Also for the transition models, it is the case that there is no universal model available. The choice of the model must always be in accordance with the simulated and measured data. Nevertheless, the most accurate model with least complexity should always be chosen to describe a TFT in circuit simulation.

Part III.

Results

4. Electrolyte gated field-effect transistors based on indium oxide channel

As discussed in Section 2.3 and in Section 2.2.3, electrolytes, as the gating-approach, and indium oxide, as the channel material, respectively, are promising candidates for printed TFTs. Therefore, in an EGFET with In_2O_3 channel, the advantages of having high field-effect mobility values, and hence high performance, with low voltage requirements are combined. A composite solide polymer electrolyte (CSPE) is used as electrolyte. The CSPE has the benefit that a solid phase is achieved with a polymer, dissolved in a solvent, yielding high ionic mobility values. The ion mobility is high because the solvent stays trapped in the polymer matrix, forming conducive pathways where the ions can move more easily. [134] Therefore, such an EGFET can become very attractive for applications in the field of PE. Garlapati et al. show inkjet printed EGFETs with field-effect mobility values up to 126 $cm^2\,V^{-1}\,s^{-1}$, at only one volt applied to the gate- and drain-electrode. [135]

The low voltage requirement of the EGFET is the result of the high gate-capacitance (C_g) ($\sim$ 5 µF cm^{-2}), that is introduced to the transistor, due to the electrolyte-gating. [135] As already discussed, the small distance between the charge carriers, forming the HDL at the respective interfaces, and the high dielectric constant of the CSPE are responsible for the high gate-capacitance value. Also, the electrolyte can follow the surface roughness of the In_2O_3 film, gating the channel of the TFT in a more efficient way. [38] Although establishing a HDL reduces the operating frequency of TFTs, since the ion mobility is slower than the electron mobility, the EGFET can theoretically operate in the sub-MHz regime. Interestingly, once the HDL is established, the cut-off frequency of the EGFET depends only on the field-effect mobility, the channel length and the driving voltage (V): [57]

$$f_T = \frac{\mu_{FET} V}{2\pi L^2}. \tag{4.1}$$

In terms of stability, on a similar TFT structure, the lifetime of the CSPE is proven to be at least 20 days. [136] More recently, a lifetime of three months is achieved for a one bit memory (latch) designed with the aforementioned EGFETs. [137]

In the following subsections the fabrication process of In_2O_3 based EGFETs is introduced, and typical electrical device characteristics are discussed. Furthermore, the effect of the process variation on the device performance will be studied on several EGFETs with different channel geometries. As known from state of the art silicon technology, computer aided design kits are powerful tools that support circuit designers in developing new applications. One important component of such a design kit is a transistor model

which can mimic the electrical characteristics of the used TFTs. Therefore, this chapter will conclude with a modeling methodology for EGFETs with a In_2O_3 channel.

4.1. Fabrication routine

The fabrication steps for inkjet printed EGFETs are visualized in Figure 4.1. First, a glass substrate, sputtered with 150 nm ITO, is structured through an e-beam process. After structuring, the drain-, gate- and source-electrodes, resistors as well as all interconnects, based on ITO, remain on the substrate. Next, the substrate is cleaned with acetone (C_3H_6O) and 2-propanol (C_3H_8O) with a ratio of 1:1 in a ultrasonic cleaner, before printing the functional materials.

The In_2O_3 precursor is printed with a industry ink jet printer, namely Fujifilm Dimatix Materials Printer (DMP-280) (Figure 4.2a), between the drain- and the source-electrode. While printing the In_2O_3 precursor, the stage of the printer, where the substrate is placed, is heated to 60 °C. The indium oxide precursor is made with 0.05 M of indium nitrate hydrate ($In(NO_3)_3 \times H_2O$), dissolved in double de-ionized water and glycerol (4:1). The solution is stirred until it is homogeneous and filtered with a 0.2 µm polyvinylidene difluoride (PVDF) syringe filter before printing. Afterwards, the substrate is annealed at 400 °C for two hours in a furnace. At annealing temperatures below 400 °C, the metal halide precursor is incomplete decomposed, forming a secondary indium phase, and lowering the field-effect mobility. [34, 135] Thesefore, the temperature of the furnace is slowly raised, in over two hours to prevent the formation of cracks within the In_2O_3 film, from RT to 400 °C. The substrate is also kept inside the furnace after annealing, while cooling down to RT. This reduces the thermal stress which might be introduced to the In_2O_3 film. However, the high temperature requirement limits the choice of the substrate

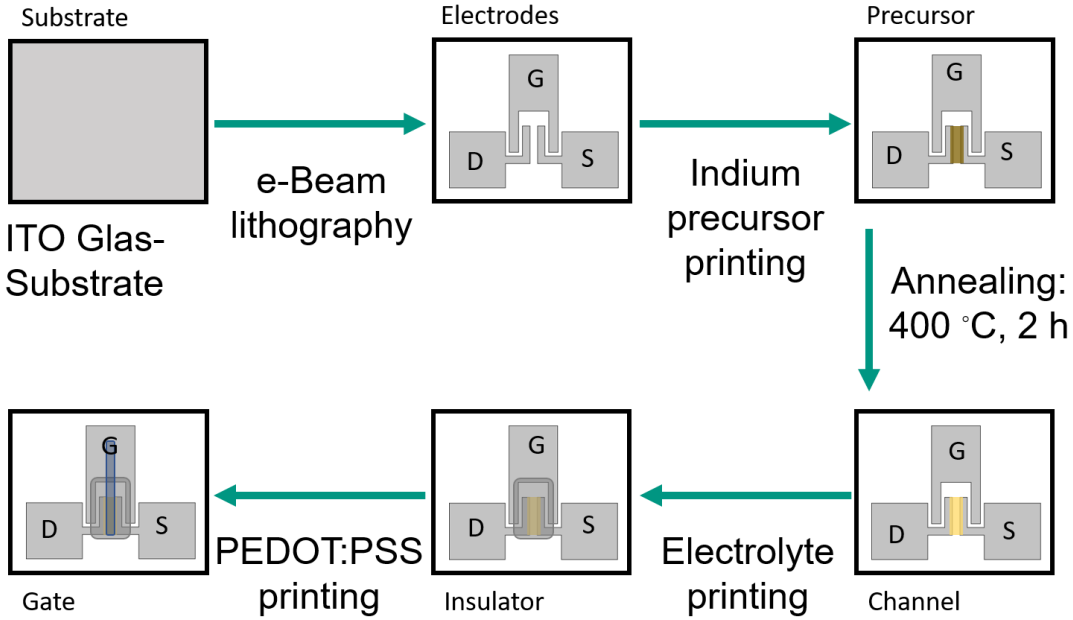
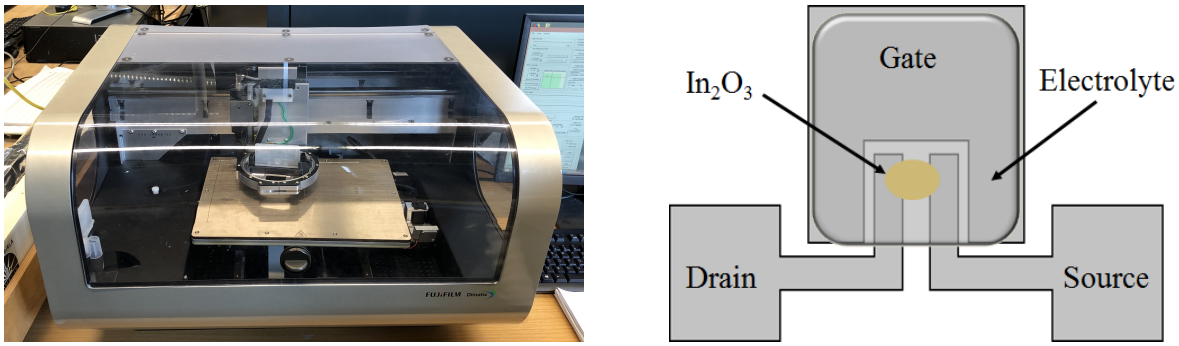


Figure 4.1.: Fabrication methodolgoy for printed EGFETs with In_2O_3 channel.

to glass, silicon or kapton substrates. Nevertheless, in literature, chemical or photonic curing methods are presented to prepare a In_2O_3 film at ambient conditions. [138–140] Since changing the curing method from thermal annealing to chemical or photonic curing reduces the field-effect mobility value by a factor of ~ 10, a trade off between device performance and the choice of substrate needs to be made before designing the application.

Subsequent, the CSPE ink is printed on top of the channel while the stage of the ink jet printer is heated to 40 °C. To prepare the CSPE, 4.29 wt% poly(vinyl alcohol) (PVA) is dissolved in 85.71 wt% dimethyl sulfoxide (DMSO) and stirred for two hours at 90 °C. Parallely, 1 wt% lithium perchlorate ($LiClO_4$) is dissolved in 9 wt% propylene carbonate (PC) and stirred for two hours at RT. Both solvents are mixed together and likewise stirred at RT, until a homogeneous solution is obtained. The CSPE ink is filtered through a 0.2 µm polytetrafluoroethylene (PTFE) membrane before printing. In an EGFET, the gate-electrode can be displaced from the channel and does not need to be on top of the channel (in-plane gate) (Figure 4.2b). However, in an in-plane structure, the area of the gate-electrode covered with the CSPE must be much bigger than the channel area. This is in order to push the maximum amount of electrons into the channel, therefore, to improve the gating mechanism. [38]



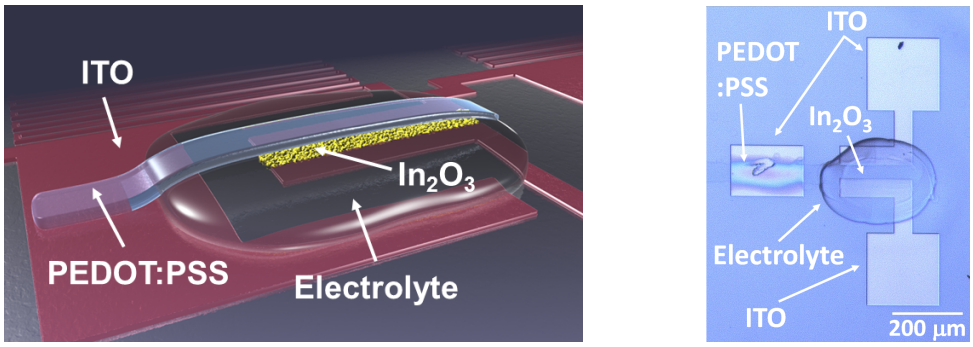
(a) (b)

Figure 4.2.: (a) Picture of the Fujifilm Dimatix Materials Printer (DMP-2850) used to print the devices. (b) Top-view of an in-plane EGFET.

The efficiency of the gating-mechanism is maximized if a top-gate is printed on top of the CSPE. The top-gate material is based on a conductive polymer, poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfonate (PEDOT:PSS), and it does not require any post annealing step nor further post treatment which could harm the CSPE. [59] However, the top-gate ink is a mixture of 70 wt% PEDOT:PSS and 30 wt% Ethylene glycol ($(CH_2OH)_2$), stirred for two hours, and then filtered through a 0.45 µm PVDF membrane.

4.2. Electrical characteristics

An n-type In_2O_3 based EGFET (Figure 4.3) with a W/L-ratio of 600 µm / 70 µm is characterized in the following. For the rest of this thesis and if not mentioned differently,



(a) (b)

Figure 4.3.: (a) Graphical representation of a top-gated EGFET with indium oxide channel. (b) Microscopic image of the EGFET. Reprint with permission from [134] © 2019 IEEE.

EGFETs will always be referred to TFTs with In_2O_3 channel and the CSPE as gate-insulator, likewise it is introduced in the previous subsection. From the output curve (Figure 4.4a), one can see that the EGFET behaves like an ordinary transistor with visible linear and saturation regions. The off-current is extracted from the transfer curve (Figure 4.4b) at minimum drain-source current and a drain-source voltage of 1.0 V. Therefore, the off-current current is $\sim$ 370 pA. To extract the on-current, the drain-source current is evaluated at a drain-source voltage and gate-source voltage of 1.0 V. Under these conditions, the on-current is $\sim$ 630 µA and the I_{on}/I_{off}-ratio is subsequently 1.7×10^6, which is large enough to provide a feasible signal to noise margin (SNM) required for designing circuits. The values for the threshold voltage and the subthreshold slope are 0.21 V and 74.8 mV dec^{-1}, respectively. Interestingly, the subthreshold slope is close to the theoretical limit of 60 mV dec^{-1}, demonstrating the excellent switching behavior of the EGFET.

The gate-capacitance (Figure 4.4c) is measured by shortening and grounding the drain- and source-electrodes, while sweeping the potential at the gate-electrode. As seen, the gate-capacitance rises with increasing gate potential, but it is relatively flat for negative gate voltages. The reason for that lies in the fact that In_2O_3 is an accumulation based semiconductor and for negative gate-potentials an inversion layer needs to be formed, which is not possible with In_2O_3. In the accumulation region, the gate-capacitance rises with the gate-potential, since electrons accumulate at the electrolyte/semiconductor interface. However, the gate-capacitance is usually normalized to the channel area which is not possible, here, because the surface roughness of the semiconductor significantly increases the effective area of the channel. The determination of the exact channel area is still challenging. Nevertheless, in a plate capacitor structure, where the CSPE is sandwiched between two ITO electrodes, the gate-capacitance per unit area is measured to be 4.7 µF cm^{-2}. [135] Assuming that the capacitance value of the plate capacitor is close to the value of the gate-capacitance, and by using Equation 2.4, the field-effect mobility value of the EGFET becomes $\sim$ 52 cm^2 V^{-1} s^{-1}. Furthermore, the g_m-plot is shown in Figure 4.4d.

The threshold voltage of the EGFETs is tuned by the channel geometry (Figure 4.5).

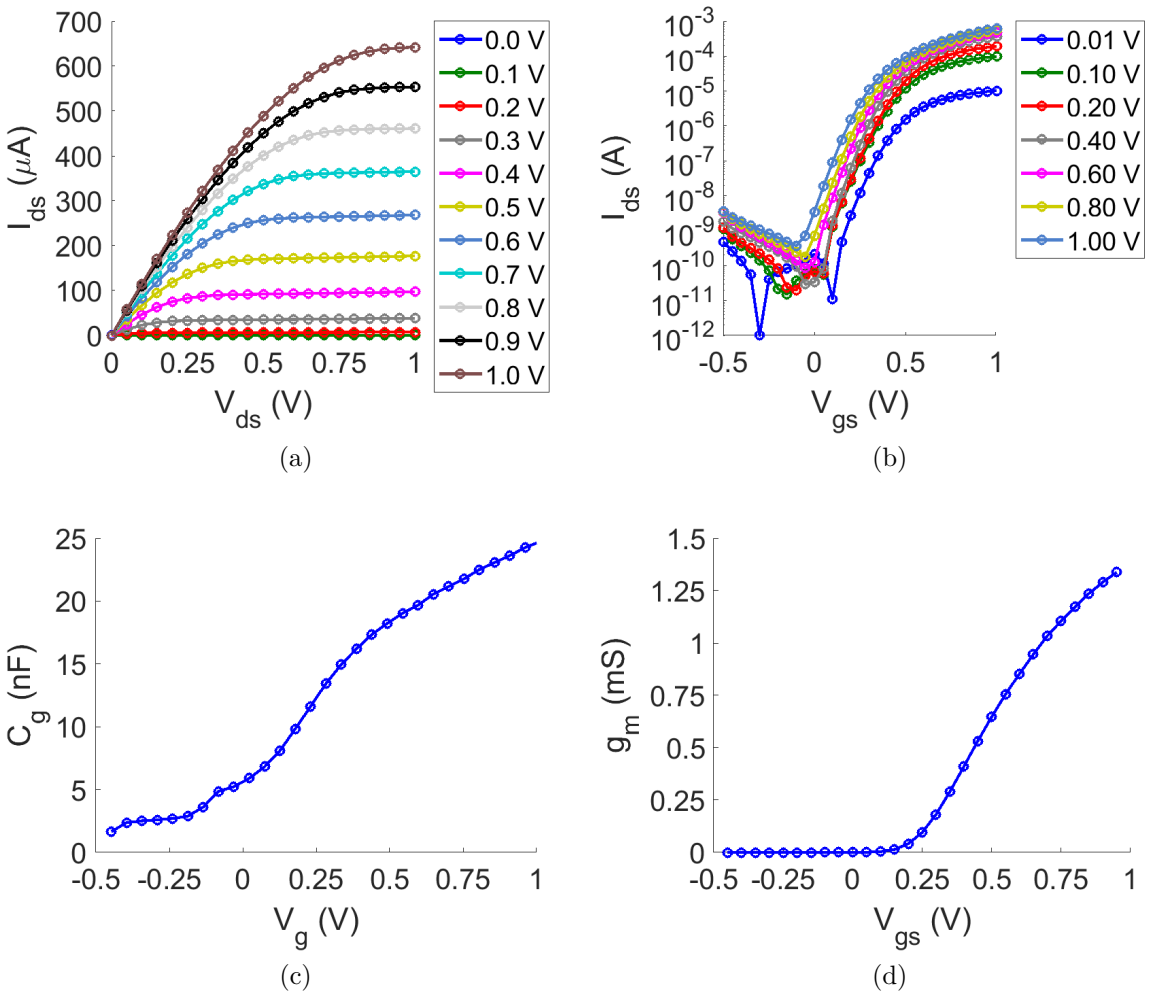


Figure 4.4.: (a) Output and (b) transfer curves of an EGFET. The voltage values placed on the top right side of each graph denote the respective gate-source voltage and drain-source voltage levels. (c) The gate-capacitance of the EGFET plotted against the gate-voltage. (d) Transconductance of the EGFET measured at a drain-source voltage of 1.0 V.

As depicted in Figure 4.5a, the threshold voltage significantly drops with decreasing the channel length. On the other hand, the threshold voltage deceases moderately with increasing the channel width. In addition, for a channel length of 10 µm the threshold voltage is always negative. In case that the channel length is 40 µm, depending on the process variation, the threshold voltage is either positive or negative. For a channel length of 80 µm, the trend of the threshold voltage is towards positive values. In conclusion, it is possible to adjust the threshold voltage fine grained by changing the channel width and by several factors through the channel length. This result is also confirmed by Figure 4.5b, where the threshold voltage is plotted against the channel width for different channel length values. Independently of the channel width, the threshold voltage is negative for channel lengths smaller than 60 µm and positive for larger sizes. Unfortunately, the data is incomplete for EGFETs with a channel width of 400 µm because, in this

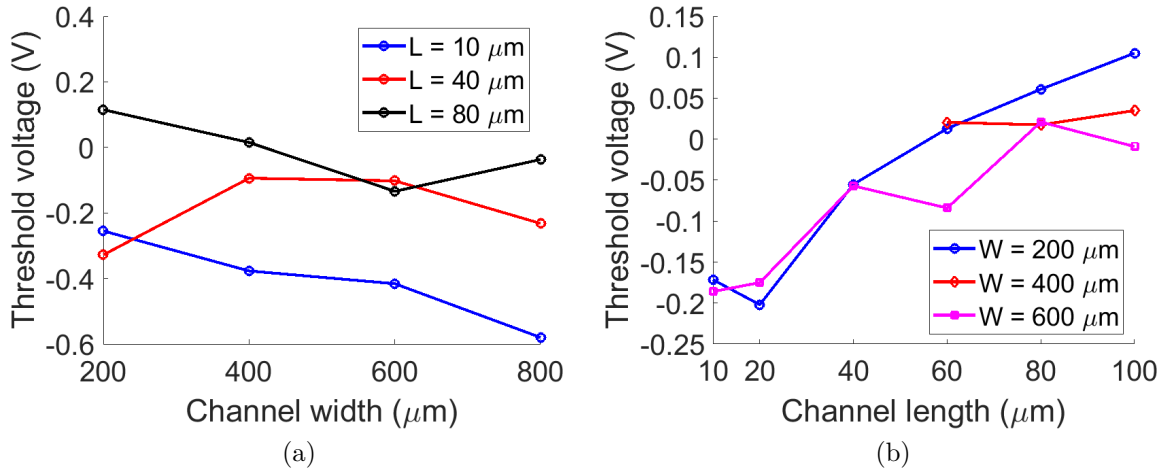


Figure 4.5.: Dependency of the threshold voltage from (a) the channel width and (b) the channel length.

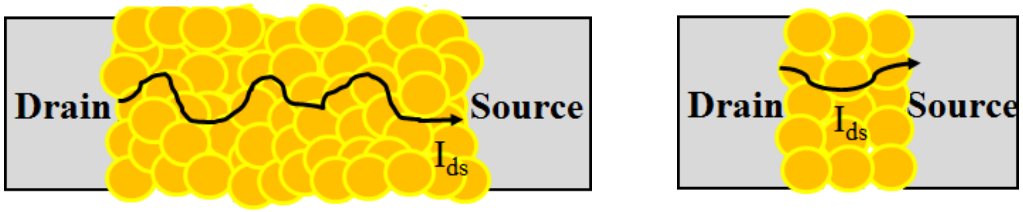
particular case, internal shorts are observed and, thusly, affected devices excluded from the evaluation.

Tuning the threshold voltage through the channel geometry is an interesting future task because the EGFET is able to operate either in enhancement ($V_t \geq 0$) or depletion ($V_t < 0$) mode. There is the potential to replace p-type EGFETs with depletion mode EGFETs. In modern microelectronic circuits, CMOS designs where a p-type FET pulls up and a n-type FET pulls down the input signal are well established to reduce the power consumption. Unfortunately, CMOS-like designs are not feasible with metal oxide semiconductors as discussed in the previous chapter. Therefore, for designing circuits based on EGFETs, a W/L-ratio of 600 µm / 10 µm, for the depletion mode EGFET, and for the enhancement mode EGFET, a W/L-ratio of 200 µm / 80 µm, is suggested in accordance to Figure 4.5.

The reason why the threshold voltage is changed with the channel geometry is explained by the grain boundaries inside the In_2O_3 film. If the distance between the drain- and source-electrodes is increasing, the percolation path that the drain-source current needs to drive increases overproportionally because of the increased number of grain boundaries (Figure 4.6a). In consequence, a higher driving voltage, which is translated into the threshold voltage, is required to turn on the EGFET. In a short channel EGFET (L $\leq$ 10 µm), even negative threshold voltage values are observed because of the high carrier density inside the In_2O_3 film, and thus high conductivity. Additionally, the electrons have to pass a lower number of grain boundaries, reducing deflection of electrons (Figure 4.6).

4.3. Variability

The printing process itself is a huge source of variability that influences the reliability of EGFETs. Variations in layer thicknesses and printed area cannot be avoided. Also the indium particle concentration in an ink may vary, changing the surface roughness of the



(a) (b)

Figure 4.6.: Graphical representation of the cross section view of the In_2O_3 channel in a EGFET, describing the percolation path of the drain-source current current in (a) a long and (b) short channel device.

printed film. All the described effects contribute that similar fabricated EGFETs have different electrical characteristics, decreases the chances for commercial applications. [141]

Figure 4.7 shows the transfer curves of several EGFETs with a channel width fixed at 200 µm and different channel lengths. For a channel length of 10 µm, 10 EGFETs; for 20 µm, 8 EGFETs; for 40 µm, 9 EGFETs; for 60 µm, 7 EGFETs; for 80 µm, 10 EGFETs and for 100 µm, 9 EGFETs are evaluated. The maximum number for all EGFETs is 10, but due to the process variation some of the printed EGFETs have an internal short circuit between the gate-electrode and the channel. These EGFETs are excluded from the evaluation. An internal short circuit can happen if the top-gate electrode (PEDOT:PSS) comes in contact with the drain- and/or source-electrodes because the area of the printed electrolyte is too small. Another reason for an internal short circuit may caused by a too thin electrolyte film, where the PEDOT:PSS layer penetrates the electrolyte, electrically contacting the channel. Nevertheless, the variability introduced by the printing process is in an acceptable range, here (Figure 4.7).

To visualize the variability of the EGFET, the key parameters (the on-current, the off-current, the threshold voltage, the subthreshold slope and the field-effect mobility) of the EGFETs are plotted in a boxplot. Unfortunately, it is not possible to do further statistical analysis, at this point, because of the limited number of EGFETs that can be characterized at once. In a boxplot (Figure 4.8), 50 % of the measured data is summarized in the blue box. The lower limit of the blue box defines that all values equal to, or lower than, this value represents 25 % of the data. On the other hand, the upper limit defines that all values below than, or equal to, this limit represents 75 % of the data. Inside the box, the median is defined by a red vertical bar. Some of the measured data may lie outside the blue box. Thereby, a value is considered to be minimum, if it is lower than the lower limit of the blue box and at least equal to the value of the lower limit - 1.5 × the interquartile range (IQR). Similarly, a value is considered to be maximum, if it is bigger than the upper limit of the blue box and it is maximal equal to the upper limit + 1.5 × IQR. The minimum and maximum values are denoted by a black vertical bar. By subtracting the value of the upper limit with the value of the lower limit, the IQR is estimated. All other data points are considered to be outliers and marked with a red cross.

As expected, the on-current decreases with increasing channel length (Figure 4.8a). For channel length values between 10 µm and 60 µm, it is feasible to describe the

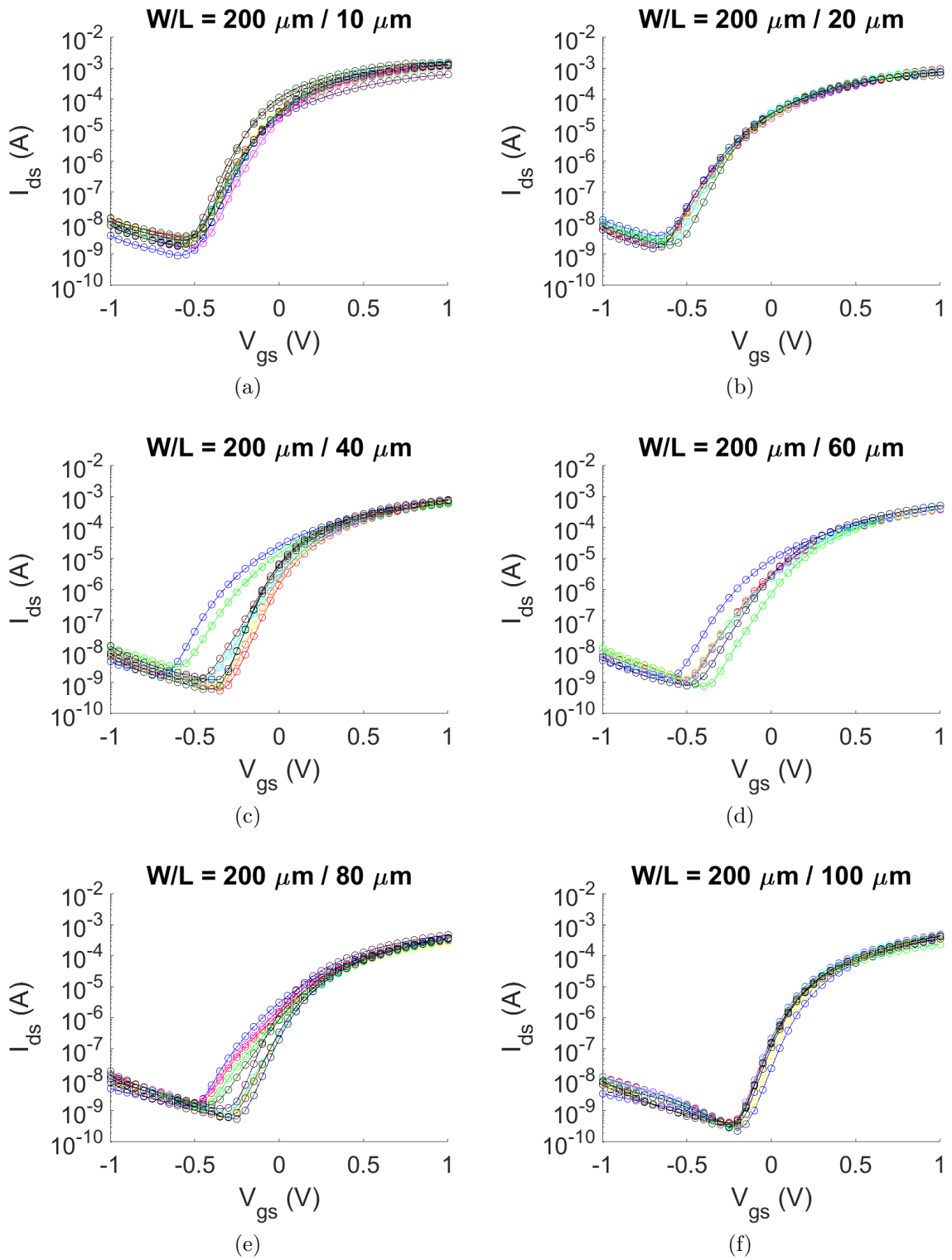
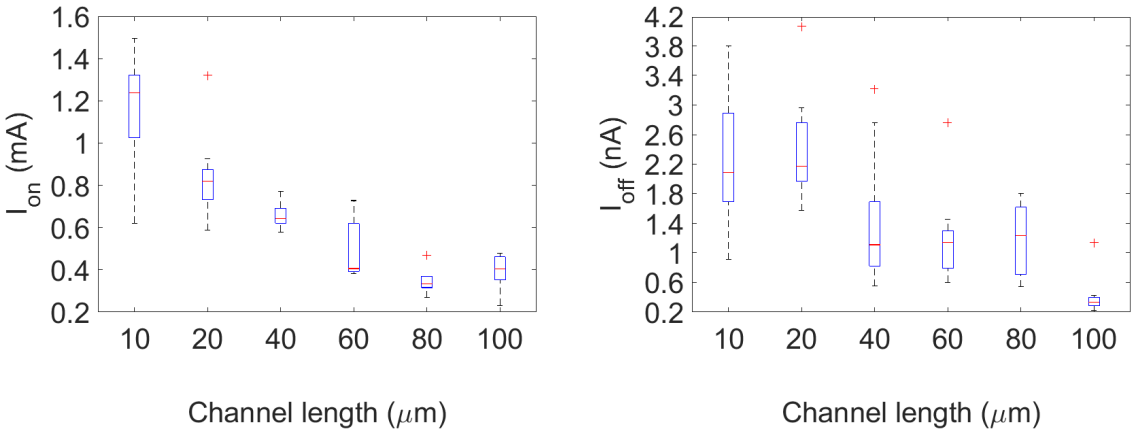
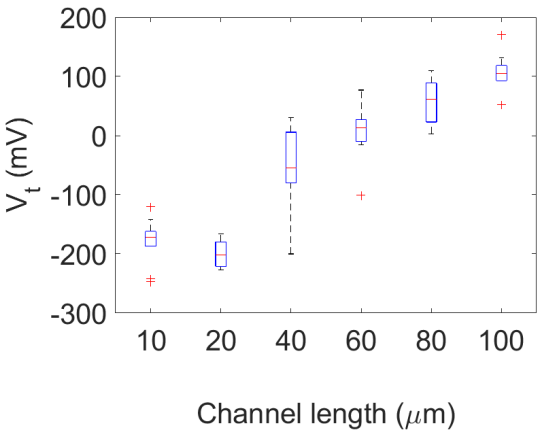


Figure 4.7.: Transfer curves of several EGFETs with fixed channel width (200 µm) and different channel length. All EGFETs plotted in one window have the same geometry and are recorded at a drain-source voltage of 1.0 V.

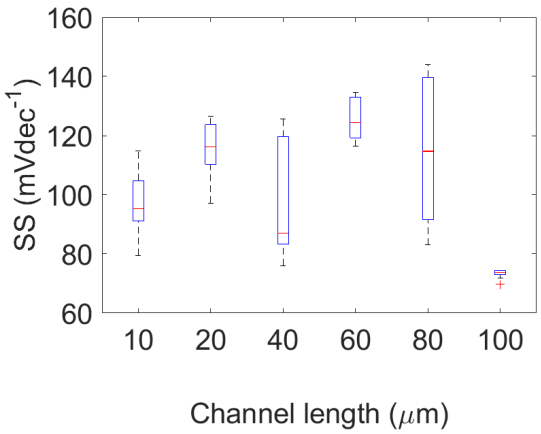


(a)

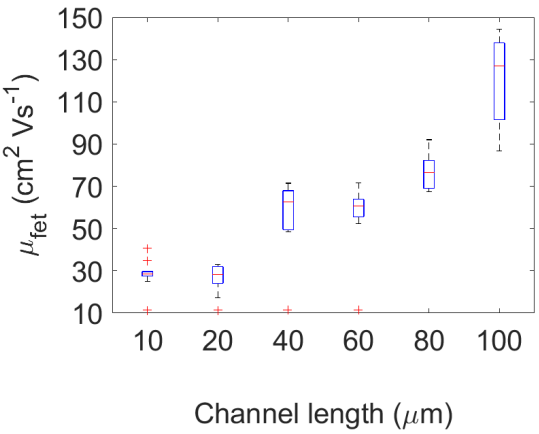
(b)



(c)



(d)



(e)

Figure 4.8.: Dependency of (a) the on-current, (b) the off-current, (c) the threshold voltage, (d) the subthreshold slope and (e) the field-effect mobility from the channel length summerized in different boxplots.

on-current through a linear dependency. At channel length values ≥ 80 µm the influence of the channel length on the on-current is less pronounced because the percolation paths inside the channel starts limiting the drain-source current. The off-current decreases slightly with the channel length, since the off-current is governed more by leakage effects, than by geometry effects (Figure 4.8b). As discussed previously, the threshold voltage is highly dependent on the channel length (Figure 4.8c) because of the current percolation path inside the channel. For channel length values smaller than 60 µm, the EGFET operates in depletion mode and for channel length values bigger than, or equal to 80 µm in normally off mode. This scaling behavior of the threshold voltage is also observed, here. For the subthreshold slope there is no noticeable dependency on the channel length (Figure 4.8d). The field-effect mobility is evaluated in the linear region, and a gate-capacitance value of 4.77 µFcm^{-2} is assumed. Figure 4.8e shows that the field-effect mobility value rises with the channel length. This behavior of the field-effect mobility is unexpected since smaller channel length reduces centers of charge carrier scattering. However, the double-layer effect is a surface effect and is, therefore, influenced by the surface area, which is different than assumed in the constant gate-capacitance value, used for calculating the field-effect mobility. In the future, it is important to estimate the right value for the gate-capacitance.

4.4. Modeling

For designing circuits based on the EGFETs, it is important to have a reliable model which describes the electrical characteristics of the EGFET in circuit simulations. Thereby, the simulated curves provided by the model must be smooth and continuous to avoid convergence issues during simulation.

Most of the models, like the Level 1 FET model (Equation 2.2), used for state of the art silicon based TFTs, expect a quadratic growth of the drain-source current with the gate overdrive voltage ($V_{ov} = V_{gs} - V_t$). However, observations show that the drain-source current does not follow the quadratic law in a EGFET. One reason is that trap states and charge carrier scattering effects reduce the field-effect mobility value like in amorphous or polycrystalline semiconductors. [142] The other models described in Chapter 3 require too many input parameters and are not able to model the linear region of the EGFET accurately. In addition, the drift-diffusion model is too complex to be integrated into a SPICE simulator.

Since the aforementioned transistor models are not reliable to mimic the DC characteristics of the EGFETs, a new modeling methodology is presented in the following. The model is based on the Curtice model, developed for gallium arsenide (GaAs) metal-semiconductor FETs (MESFETs), where only one equation is sufficient to describe all transistor regions. Different equations for the various transistor regions add complexity to the modeling approach, since discontinuities between the different transistor regions are common. [143] The Curtice model, and therefore, the developed model is based on a tangent hyperbolic function, which is very similar to the output curve of a TFT and captures all transistor regions. [144] In addition, as discussed in Section 3.1, Equation 3.5 models the field-effect mobility of amorphous and polycrystalline semiconductors accurately. Since printed indium oxide films are polycrystalline, the mobility model

(Equation 3.5) is integrated into the Curtice model as follows in the above threshold regime ($V_{gs} \geq V_t$): [59]

$$I_{ds} = \frac{W}{L} \cdot C_g \cdot \mu_0 \cdot (V_{gs} - V_t)^{\gamma} \cdot \tanh(\alpha \cdot V_{ds}), \tag{4.2}$$

where α is the parameter to describe the knee region of a TFT.

For the below threshold regime ($V_{gs} < V_t$), the well known subthreshold current model is adjusted, by adding the tangent hyperbolic function. Continuous simulated transistor curves are ensured by adding the $\tanh(\alpha \cdot V_{ds})$ expression to the equation: [59]

$$I_{ds} = I_{off} \cdot e^{\frac{\ln(10)}{SS}(V_{gs} - V_0)} \cdot \tanh(\alpha \cdot V_{ds}), \tag{4.3}$$

where V_0 is the the onset voltage.

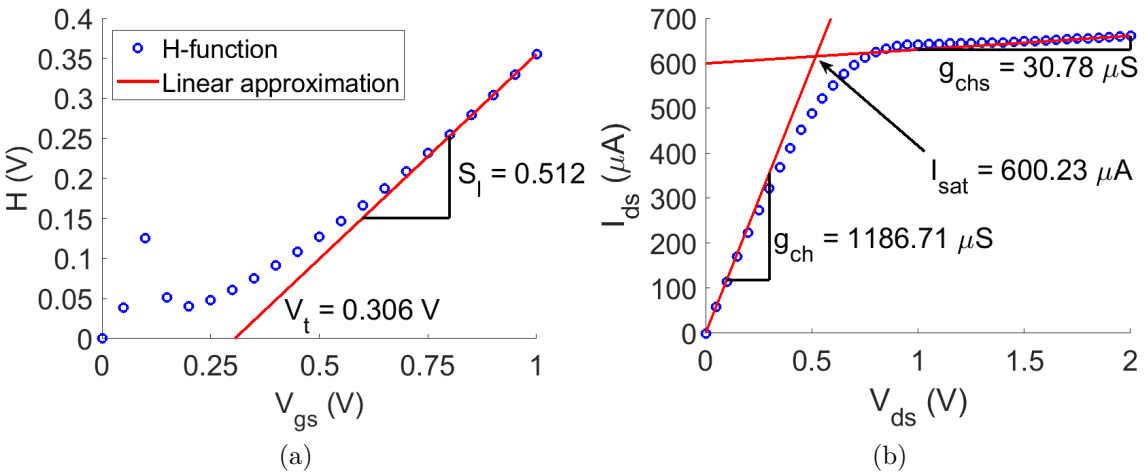
The modeling approach developed for EGFETs is demonstrated on a transistor with a W/L-ratio of 600 µm / 70 µm:

Firstly, to extract the parameters V_t and the power law parameter (γ), the integral H-function (Equation 3.6) is evaluated at a drain-source voltage of one volt and the linear part of the H-function is approximated through Equation 3.7. The intercept of the linear approximation with the x-axis is defined as the parameter V_t and the slope of the H-function (S_l) is used to calculate the parameter γ. [59, 125, 127, 145, 146] Figure 4.9a shows that the V_t is 0.306 V and S_l is 0.512, which yields a value of 0.954 for the parameter γ with the help of Equation 3.6.

Secondly, the parameter α is estimated through the channel conductance in the linear regime and the saturation current (I_{sat}) of the output curve at a gate-source voltage of one volt:

$$\alpha = \frac{g_{ch}}{I_{sat}}. \tag{4.4}$$

With Equation 4.4 and Figure 4.9b, the parameter α is calculated to be 1.977.



(a) (b)

Figure 4.9.: (a) Integral H-function to extract the parameters V_t and γ. (b) Extraction of the parameter α from the output curve.

Thirdly, the slope of the drain-source current is evaluated over one decade, in the linear part of the transfer curve and at the steepest slope, to extract the subthreshold slope. The remaining parameters for the subthreshold current (Equation 4.3) are fitted in a way that the measurement data fits with the calculated curve (Figure 4.10).

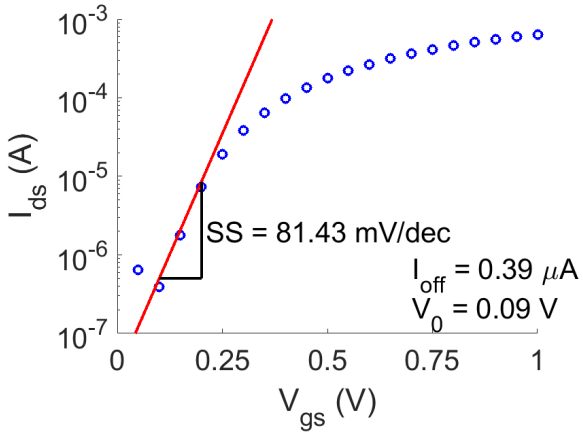


Figure 4.10.: Extraction of the parameters relevant for the below threshold regimes.

As is seen from Figure 4.11a, the model accurately predicts the output curves of the EGFET. However, Figure 4.11b clearly shows that the modeled provides discontinuous transfer curves at gate-source voltage values around the threshold voltage because of switching from the below, to the above threshold model.

To achieve a continuous transition from the below to the above threshold regime, a transition function is used. Due to the huge discrepancy between the calculated transfer curves, provided by the below and above threshold regime models, none of the methods introduced in Section 3.7 fit with the measured data and a cubic interpolation method is

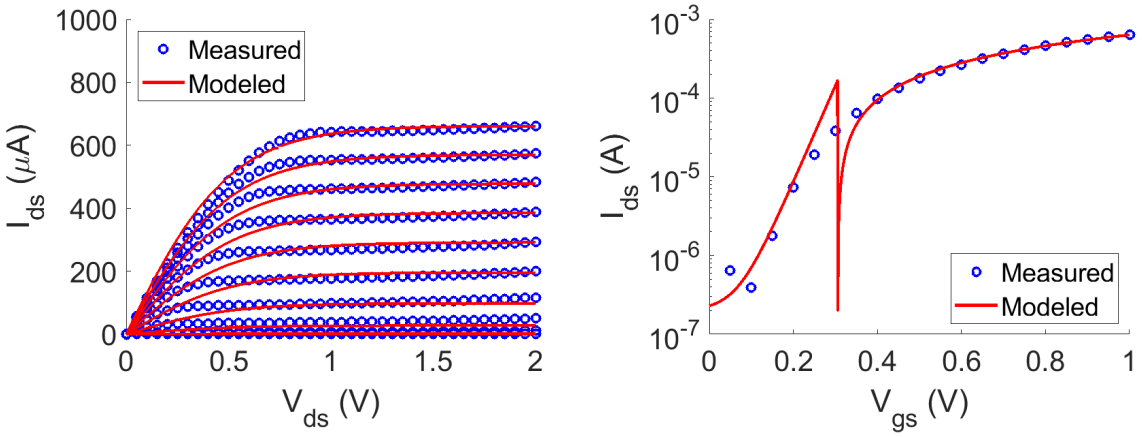


Figure 4.11.: (a) Comparison between measured and modeled output curves. (b) Measured and modeled transfer curves at drain-source voltage equal to 1.0 V.

used for the transition region: [59]

$$I_{ds} = \left(a\,V_{gs}^3 + b\,V_{gs}^2 + c\,V_{gs} + d\right) \cdot \tanh\left(\alpha \cdot V_{ds}\right) \tag{4.5}$$

where the parameters a, b, c, d are constants and fitted to the measured data. As input for the fitting algorithm, two current values provided by Equation 4.2 and 4.3, respectively, are required. The selected current values are divided by a factor of $\tanh\left(\alpha \cdot V_{ds}\right)$ before proceeding with the fit. For an accurate fit, it is suggested to take the drain-source current value close to the threshold voltage, having a minimum distance to the measured curve. The parameters of the model are summarized in Table 4.1, and Figure 4.12 shows that the presented modeling approach is accurate to describe the EGFET.

Table 4.1.: Extracted parameters used for the EGFET model.

a (V^{-3})	b (mV^{-2})	c (mV^{-1})	d ($\times 10^{-3}$)	I_{off} (μA)	V_0 (mV)	V_t (V)	SS ($mVdec^{-1}$)	α (V^{-1})	γ
-0.11	2.23	-56.62	382.5	0.39	90	0.3	81.43	1.98	0.95

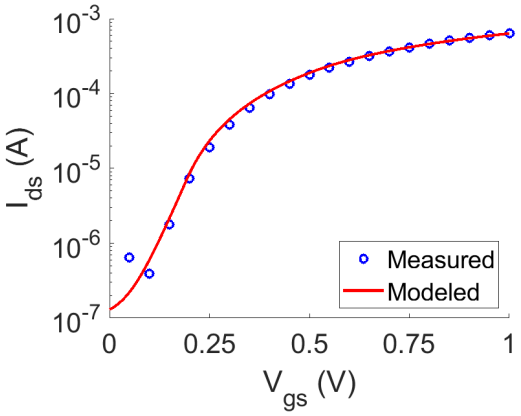


Figure 4.12.: Improved modeling of the region between the below and above threshold regimes.

Nevertheless, a disadvantage of this modeling approach is that the below and above threshold are modeled with different equations and a transition function is required to link both models together. That is why this model is very sensitive to process variation, affecting parameters like the threshold voltage and finally leading to discontinuities. In an ongoing work the EGFET is modeled through an adopted version of the Enz-Krummenacher-Vittoz (EKV) model, which is well known in the silicon community and requires only one equation to model all transistor regimes. [63, 147] Interestingly, it is also possible to extend the adopted EKV model in a way that the process variation is taken into account. [148]

5. Digital Circuits

Digital circuits based on the aforementioned EGFETs are presented in the following. However, in modern CMOS-like designs, p- and n-type TFTs reduce the power consumption, since the formation of a conductive path from the supply voltage (V_{dd}) to the source supply (V_{ss}) is only possible during a signal transition. In theory, only one TFT is in on-state at a time. In addition, the output gain of a digital cell is maximized with CMOS-like designs.

In CMOS, the p-type TFT is responsible for pulling up, and the n-type FET, for pulling down the signal. In oxide electronics, as discussed in Section 2.2.3, due to the inequality between p-type and n-type metal oxide semiconductors, designs are exclusively in n-type only logic. The n-type logic is preferred over the p-type logic because the performance and reliability is higher in n-type metal oxides. In this regard, transistor-resistor logic (TRL) designs, where the p-type EGFET is replaced with a resistor, and transistor-transistor logic (TTL) designs, where the p-type EGFET is replaced by a pull-up n-type EGFET, are investigated. As circuit topology, basic logic gates (inverters, NAND, NOR and XOR gates) and ring oscillator structures are studied.

5.1. Standard cells in transistor-resistor logic

In terms of complexity an inverter is the most simple logic gate. The inverter requires only two elements (transistor/transistor or transistor/resistor). The output voltage (V_{out}) of the inverter alternates between two voltage levels, the supply voltage (logic 1) and the source supply (logic 0) levels, depending on the input voltage (V_{in}). It is worth mentioning that the source supply is grounded in most of the cases. However, if the input of the inverter is at logic 1, then the output of the inverter is pulled-down to logic 0 and vice versa. For an inverter designed in TRL, the pull-up network consists of a resistance with a value of ~ 45 kΩ and the pull-down network of an EGFET with a channel geometry of 600 µm/80 µm (Figure 5.1a). While the EGFET is inkjet printed, as discussed before, the resistor is based on ITO and structured by e-beam lithography (Figure 5.1b). The resistivity of the ITO is ~ 0.67 kΩ/□. The resistance value of the ITO resistor is tuned through the size of the meander structure. Figure 5.1c and 5.1d show the electrical characteristics of the resistance and the EGFET, respectively. Unfortunately, the EGFET slightly operates in normally on mode ($V_t = -0.09\ V$), but Figure 5.2 suggests that the threshold voltage is sufficient high for an inverter.

The output signal of the inverter can almost be pulled-up to the level of the supply voltage and pulled-down to a level of around 0.05 V. Furthermore, the inverter starts to operate at a supply voltage level ~ 0.3 V (Figure 5.2a), which is very low for a printed system. The EGFET is not able to pull-up and down the signal completely, because the resistor in the pull-up network always provides a conductive path from supply voltage

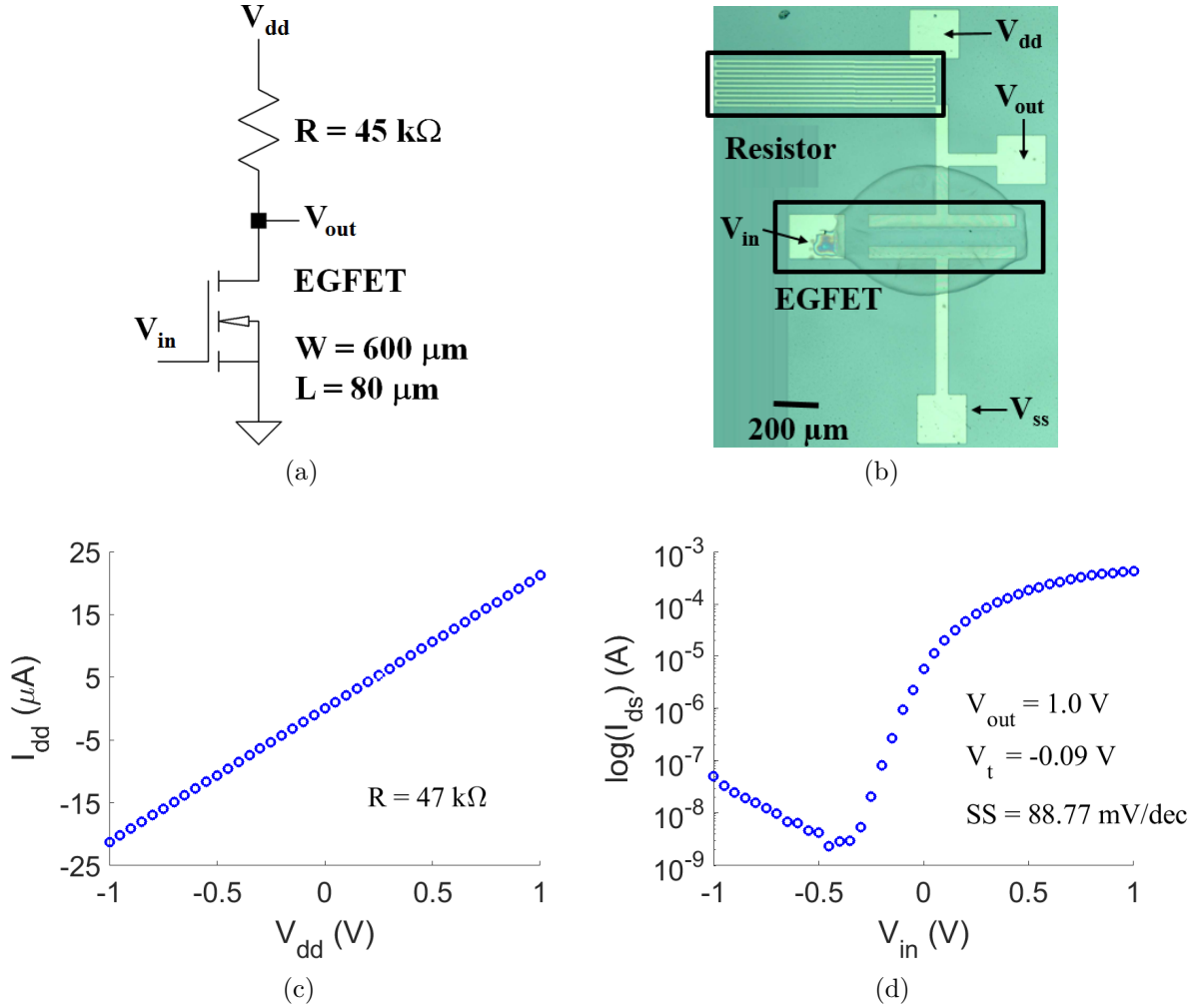


Figure 5.1.: (a) Schematic and (b) microscope image of an inverter designed in TRL. Electrical measurements of (c) the pull-up resistance and (d) the pull-down EGFET at a drain-source voltage of 1.0 V.

node to the output node. Another reason for the incomplete signal swing is that the EGFET is slightly operating in normally-on mode. In this case, the EGFET is not able to completely open, and the output signal is only partially pulled up. However, the resistor and the channel of the EGFET must be sized in a way such that the driver capability of the EGFET is much larger than the conductivity of the resistor; otherwise, the signal cannot be pulled down. Nevertheless, in TRL it is not possible to achieve rail-to-rail output signals.

The signal gain is defined between the slope of two adjacent points in the voltage transfer curve (VTC) (Figure 5.2b). As seen, the signal gain raises with the supply voltage, ranging from 0 V to ~ 0.2 V, and decreases afterwards. Therefore, for a supply voltage of 1 V the absolute signal gain is maximum at an input voltage of ~ 0.2 V and its value is close to -5. The signal gain should always be ≤ -1, apart from that it is not possible to propagate a signal from one inverter stage to another, because each inverter stage would reduce the signal swing.

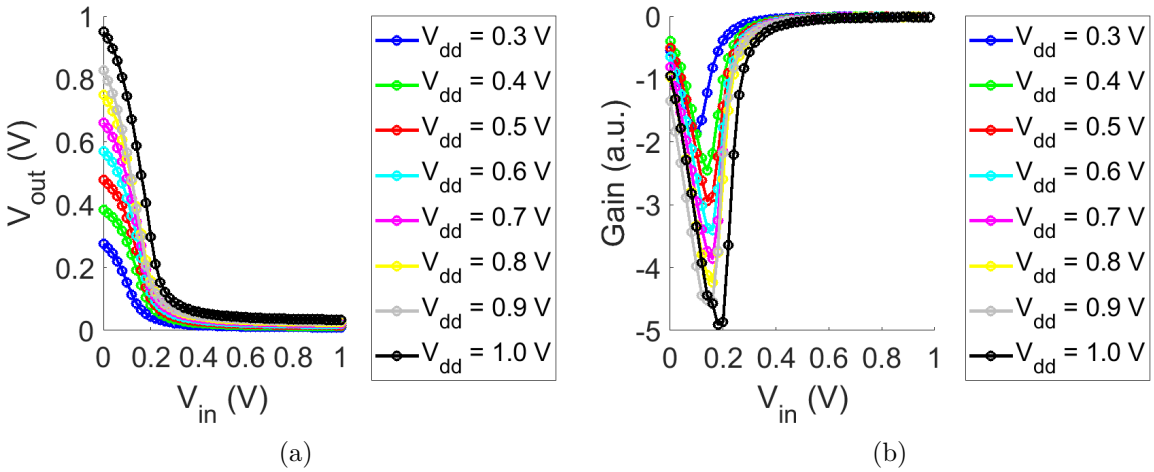


Figure 5.2.: (a) Voltage transfer curve, and (b) output gain of the inverter designed in TRL, measured at various supply voltage levels.

A signal transition at the input causes a delayed reaction at the output, rather than a simultaneous reaction. This delay is known as the propagation delay time (τ_p):

$$\tau_p = \frac{\tau_{p10} + \tau_{p01}}{2}. \tag{5.1}$$

Both response times, the high to low signal transition (τ_{p10}) and the low to high signal transition (τ_{p01}), are measured as the time difference between input voltage and output voltage at a 50 % signal swing. [149] Furthermore, the rise time (τ_r) and the fall time (τ_f) are important timing parameters to determine the speed of the inverter. Usually, the τ_r is the time it takes for the output signal to rise from 10 % to 90 % of its maximum voltage level, and the τ_f is the time constant for a 90 % to 10 % transition (Figure 5.3).

The transient analysis shows that the signal reliably switches between the logic 0 and

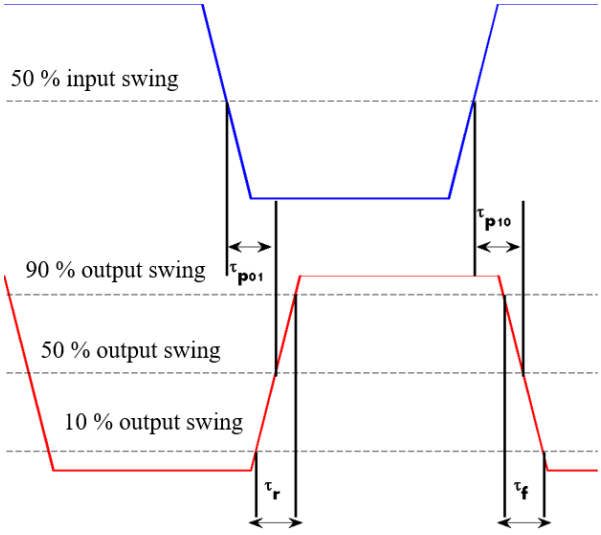
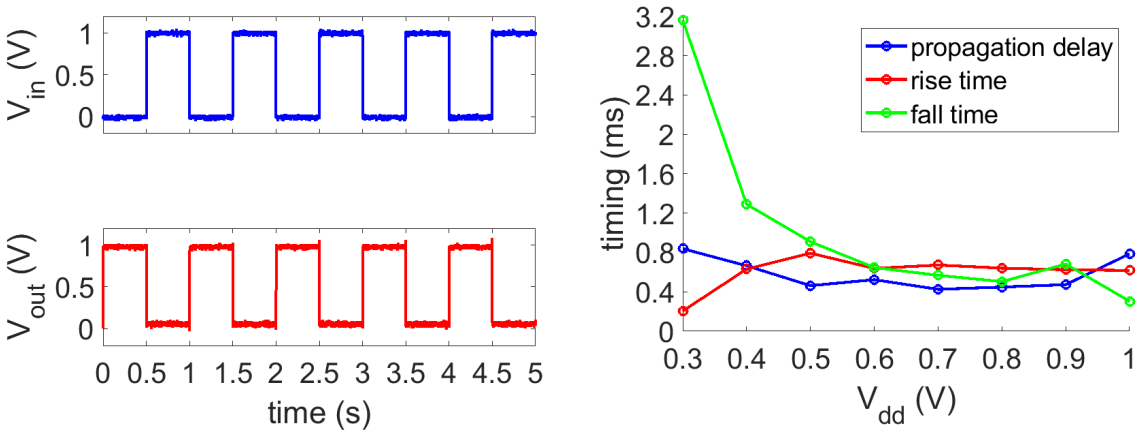


Figure 5.3.: Extraction of the key timing parameters of an inverter.

logic 1 levels (Figure 5.4a). Since the pull-up network consists of a resistor with a fixed resistance value, the rise time is nearly constant ($\sim$ 0.7 ms). The propagation delay time slightly increases from $\sim$ 0.8 ms to $\sim$ 0.9 ms within the evaluated supply voltage window, because the parasitic capacitance of the pull-down EGFET rises with the supply voltage. In contrast, the fall time decreases with the supply voltage due to the increased driver capability of the EGFET with increasing the supply voltage; starting to saturate at a supply voltage of $\sim$ 0.6 V (Figure 5.4b). All the timing constants saturate for higher supply voltages because the ion inside the electrolyte need to drift for building up and demolishing the HDL, which is not compensated by higher supply voltages, hence, higher driver capability.



(a) (b)

Figure 5.4.: (a) Transient analysis of the inverter at a supply voltage of 1 V. (b) Propagation delay, rise and fall times measured at difference supply voltage levels.

The static power consumption (P_{stat}) is estimated by measuring the current flow through the inverter while $V_{in} = 0$ V is applied to it, and is known as the quiescence current ($I_{dd,q}$). In contrast, the active current ($I_{dd,a}$) is measured by applying a 1 Hz rectangular signal to the input of the inverter. The active current is used in turn to calculate the dynamic power consumption (P_{dyn}). With the help of the active and quiescence currents, the power dissipation of the inverter is calculated as follows:

$$P_{stat} = I_{dd,q} \cdot V_{dd}, \tag{5.2}$$

$$P_{dyn} = I_{dd,a} \cdot V_{dd}, \tag{5.3}$$

$$P_{tot} = P_{stat} + P_{dyn}, \tag{5.4}$$

where P_{tot} is the overall power consumption.

For the characterized inverter, the static power consumption varies between 0.1 nW and 3.1 nW, in a supply voltage range from 0.3 V to 1.0 V. In the same voltage range, the dynamic power consumption and the total power consumption rise from 0.1 µW to 20.6 µW (Figure 5.5). It is obvious that the static power consumption is essentially non existent, because in the quiescence case, the pull-down EGFET is in off-state and as

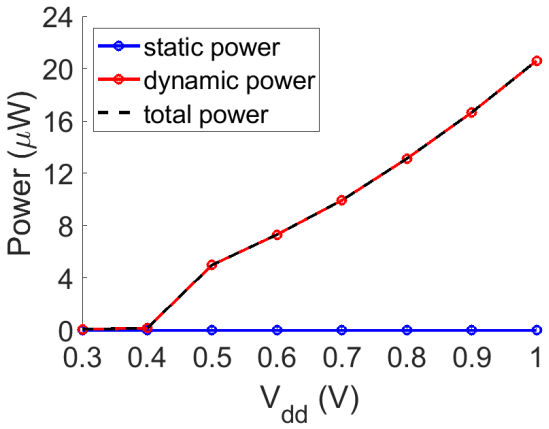


Figure 5.5.: Power consumption of the inverter designed in TRL, measured at different supply voltage levels.

consequence only a leakage current can flow from the supply voltage node to the source supply node. In the active state, the EGFET is partially in on-state and a significant current is able to flow from the supply voltage to the ground, dissipating a lot of power. This behavior is considerably different from state of the art complementary technology, where a current is just flowing from the supply voltage node to the source supply node in the transition region where both TFTs are in the on-state.

5.1.1. NAND gate

By connecting an additional EGFET in series to the pull-down network of an inverter, a NAND-gate is formed. The resistor has a resistance value of 45 kΩ and the W/L-ratio of both EGFETs is 600 µm / 80 µm. The Schematic and microscope image of the NAND-gate are shown in Figure 5.6.

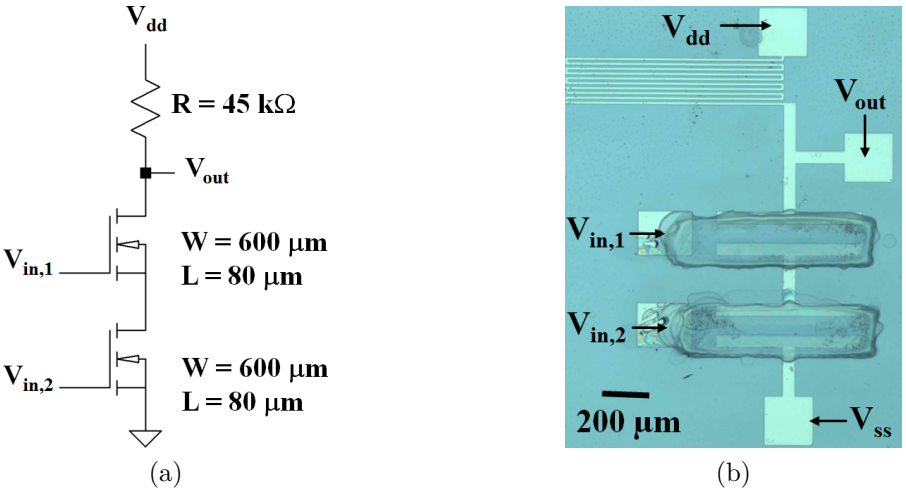
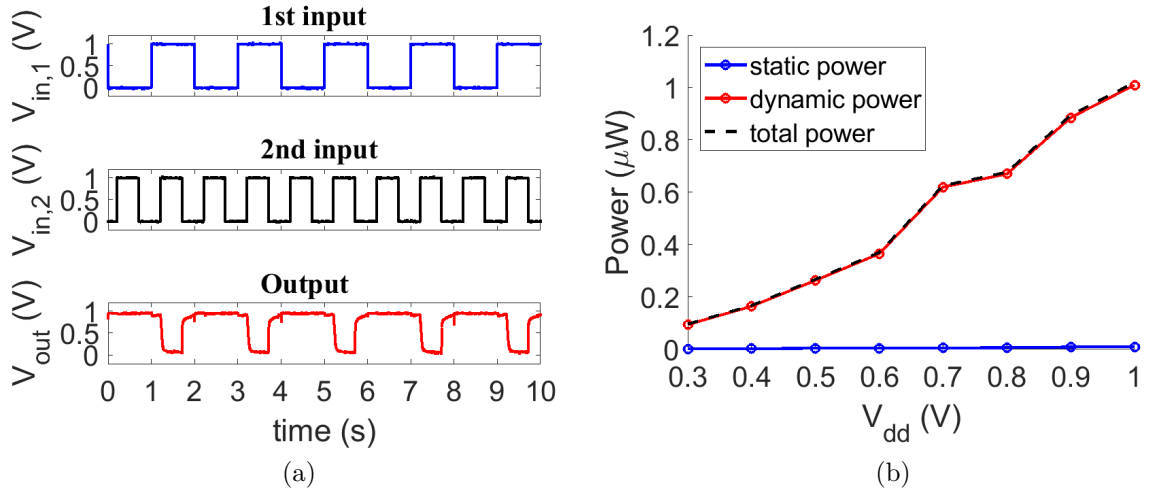


Figure 5.6.: (a) Schematic and (b) microscope image of a NAND gate designed in TRL.

The transient analysis shows that the NAND gate operates as expected (Figure 5.7a).

If one of the input signals ($V_{in,1}$ or $V_{in,2}$) is logic 0, the output voltage is pulled up to the level of the supply voltage. On the other hand, the output voltage is at logic 0, if both input signals are logic 1. The static power consumption is negligible, if both inputs are logic 0, where only a small leakage current flows from the supply voltage node to the source supply node. The power consumption rises significantly in active state, where the inputs of the NAND gate are pulsed by the input signals shown in Figure 5.7a. For that reason, the total power consumption is governed by the active power consumption. Furthermore, the dynamic and total power consumption are similar, since the static power consumption is negligible, and rise from $\sim$ 0.1 µW to $\sim$ 1.0 µW at a supply voltage level between 0.3 V and 1.0 V (Figure5.7b). The power consumption of the NAND gate is lower than for the inverter because the two EGFETs, connected in series, limiting the time period where a direct connection from the supply voltage node to the source supply node is available.



(a) (b)

Figure 5.7.: (a) Transient analysis of a NAND gate designed in TRL at a V_{dd} of 1 V. (b) Power consumption of the NAND gate in dependency of the applied supply voltage.

5.1.2. NOR gate

In a NOR gate, the two EGFETs in the pull-down network are connected in parallel instead of in series. Also for the NOR gate the pull-up resistance has a value of 45 kΩ and both pull-down EGFETs have a W/L-ratio of 600 µm / 80 µm (Figure 5.8).

As soon as one of the input signals is set to logic 1, the output signal is pulled down to the level of the source supply, otherwise the output signal is pulled up to the level of the supply voltage. Figure 5.8c shows that the NOR gate is operating normally with a resistor and two EGFETs. Also for the NOR gate a negligible static power consumption is observed, since applying logic 0 to both inputs causes both EGFETs to open, removing the conductive path from the supply voltage node to the source supply node. Alternatively, if the input signals are like in Figure 5.8c, a significant current may flow from the supply voltage node to the source supply node. Therefore, the total power consumption is defined by the dynamic power dissipation (Figure 5.8d), and rises from 0.1 µW to 15.6 µW in a supply voltage window between 0.3 V and 1.0 V. By comparing

the total power consumption of the NOR gate and the NAND gate, one can see that the the power consumption of the NOR gate is around a factor of 16 higher. This difference in the power consumption lies in the fact that for the NOR gate the EGFETs are in parallel, and in this case the time period where a conductive path from the supply voltage to the source supply is higher than for the NAND gate. The power consumption is, however, in a similar range as for the inverter.

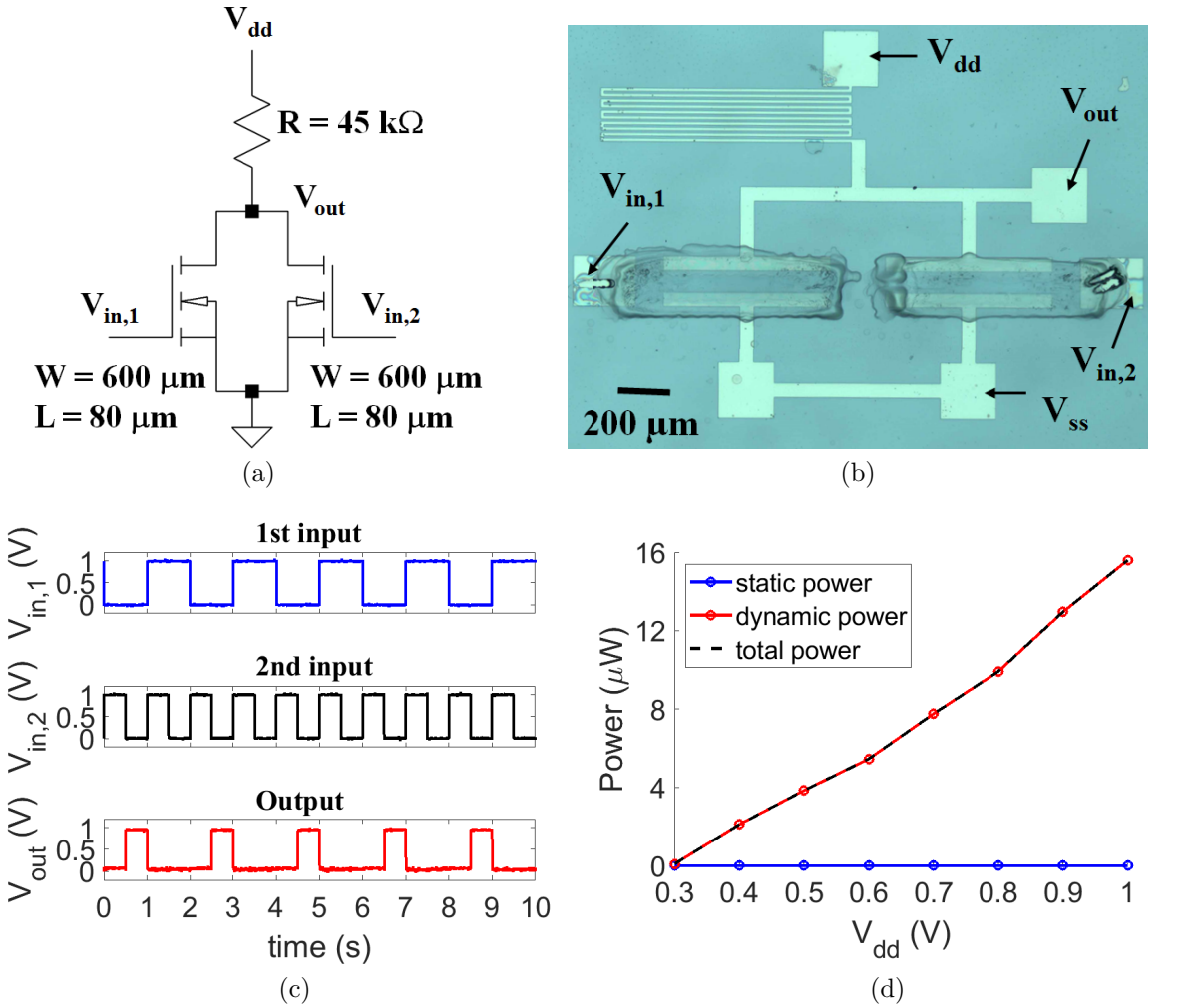


Figure 5.8.: (a) Schematic, (b) microscope image, (c) transient characteristics, measured at a supply voltage of 1 V, and (d) power consumption of a NOR gate designed in TRL.

5.1.3. XOR gate

In a XOR gate, the output voltage is only pulled up, if the input voltages are at different levels. As shown in Figure 5.9, the XOR gate is designed with NAND gates only, although other implementations are possible. The reason for the choice of the NAND gate logic design is to demonstrate that complex circuits are also feasible within the presented transistor technology. Another reason for the implementation with NAND gates is, that this design is more efficient in terms of power consumption, because the power dissipation for NAND gates is very low compared to other logic gates, as discussed before.

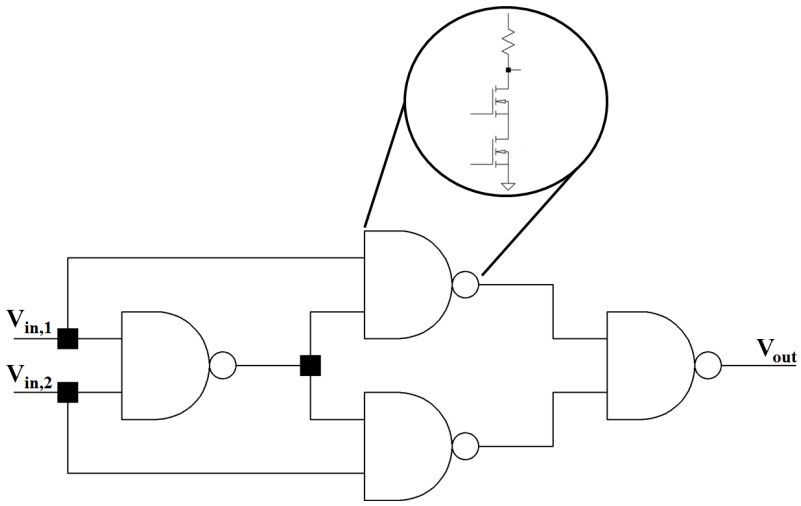
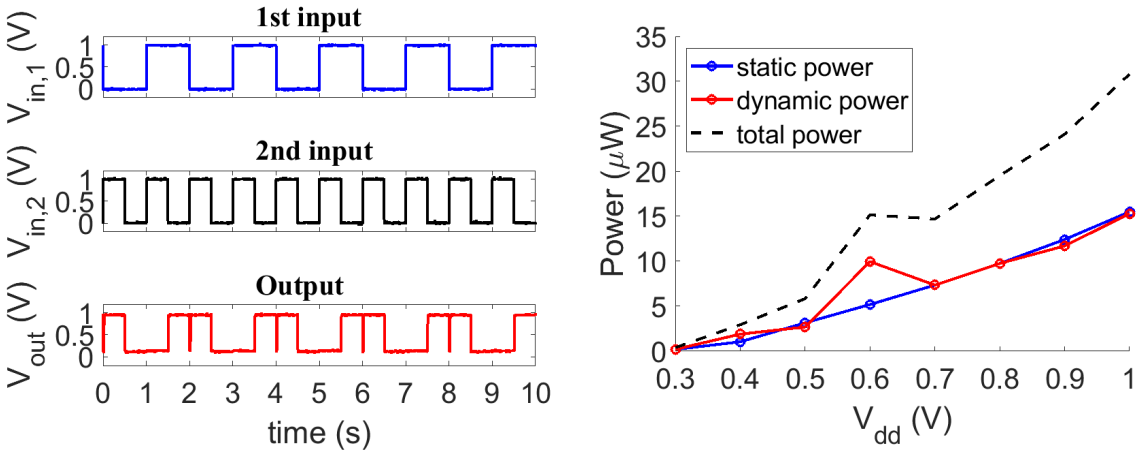


Figure 5.9.: Schematic of a XOR gate designed in TRL.

As seen in Figure 5.10a, the XOR gate is working as expected. More interesting is the evaluation of the power consumption (Figure 5.10b). The static and dynamic power dissipation are on the same level, and each increase from 0.4 µW to 15.3 µW, while changing the supply voltage from 0.3 V to 1.0 V. The static and dynamic dissipation are equal because the XOR gate is based on four NAND gate stages, and for that reason there is always a conductive path from the supply voltage node to the source supply node available, regardless of the voltage level applied to the inputs. Consequently, the total power dissipation is double the static or dynamic power consumption and rises from ~ 1 µW to ~ 35 µW in a voltage window from 0.3 V to 1.0 V, respectively.



(a) (b)

Figure 5.10.: (a) Transient characteristics of a XOR gate designed in TRL at a supply voltage of 1 V. (b) Power consumption of the XOR gate in dependency of the applied supply voltage.

5.1.4. Ring oscillator

Ring oscillator structures are important for characterizing transistor technologies since these structures give insight into the expected minimal supply voltage, the power consumption, and the reliability of applications. For ring oscillator structures, an odd number greater than one of inverters are connected in parallel. In addition, the output of the last inverter stage is connected to the input of the first inverter stage. As soon as the the supply voltage is applied to the ring oscillator, each inverter inside the ring oscillator structure starts to invert their respective input signal, and since the output of the last inverter is connected to the input of the first inverter, the output of the ring oscillator starts to oscillate.

For characterization purposes, the active current and the quiescence current are recorded while the ring oscillator is oscillating and idling, respectively. Whenever a signal transition is observed at an inverter inside the ring oscillator, a current starts to flow through this particular inverter. On average, the switching current (I_{sw}) is driven by the ring oscillator:

$$I_{sw} = I_{dd,a} - I_{dd,q} \frac{2\,\alpha_{sw}}{2\,\alpha_{sw} + 1}, \tag{5.5}$$

where $2\,\alpha_{sw} + 1$ is the number of stages, and α_{sw} is a constant. The propagation delay time of the ring oscillator is defined as:

$$\tau_p = \frac{1}{2\,(2\,\alpha_{sw} + 1)\,f_r} = R_{sw}\,C_{sw}, \tag{5.6}$$

where f_r is the oscillation frequency of the ring oscillator, R_{sw} is the switching resistance and C_{sw} is the switching capacitance. In accordance to Equation 5.6, the frequency of the ring oscillator is modeled through the switching resistance and the switching capacitance. The switching capacitance is calculated with the help of the switching current and the propagation delay time of the ring oscillator:

$$C_{sw} = \frac{I_{sw}}{V_{dd}}\,2\,\tau_p. \tag{5.7}$$

By evaluating Equation 5.6 and 5.7, the switching resistance yields:

$$R_{sw} = \frac{\tau_p}{C_{sw}}. \tag{5.8}$$

The static power consumption of the ring oscillator is

$$P_{stat} = I_{dd,q}\,V_{dd}, \tag{5.9}$$

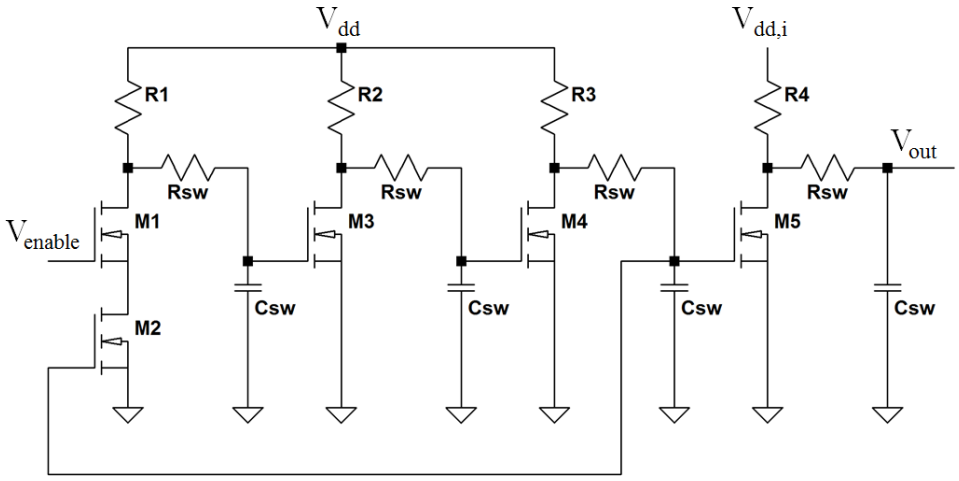
while the dynamic power consumption is calculated by: [149–151]

$$P_{dyn} = C_{sw}\,V_{dd}^2\,(2\,\alpha_{sw} + 1)\,f_r = I_{sw}\,V_{dd}. \tag{5.10}$$

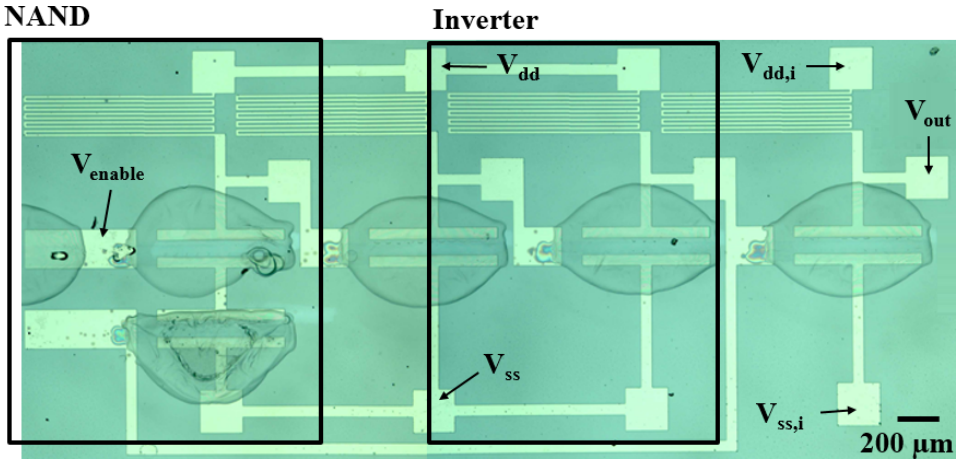
The overall power consumption is the sum of the static and dynamic power consumption.

To measure the active current and the quiescence current, it is required to measure the current flowing through the ring oscillator while it is in quiescence and active states. In order to turn the oscillation on and off, a NAND-gate replaces the inverter at the first

stage of the ring oscillator. With an enable signal (V_{enable}) the oscillation is turned on and off. If the V_{enable} is at the logic 0 level, the ring oscillator is in quiescence mode, otherwise the NAND-gate acts like an inverter, and the ring oscillator is in active mode. To avoid that the measurement equipment influences the oscillation of the ring oscillator, an inverter is connected to the output of the ring oscillator and the output signal of the ring oscillator is measured at the output of this buffer stage. The schematic and a microscopic image of the three stage ring oscillator is shown in Figure 5.11. The elements C_{sw} and R_{sw} in the schematic are not printed but included in the schematic to model the delay introduced by each stage during circuit simulation.



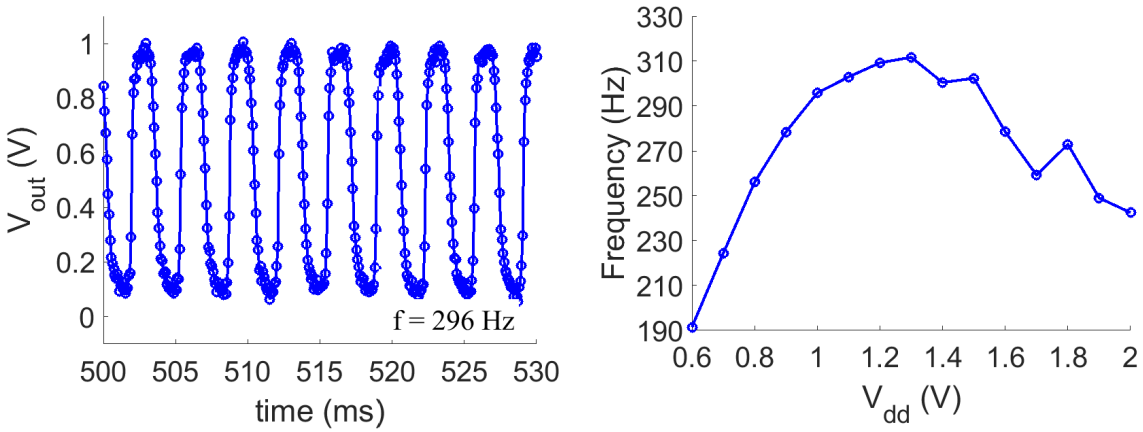
(a)



(b)

Figure 5.11.: (a) Schematic with parasitic elements and (b) microscopic image of a three stage ring oscillator designed in TRL.

The performance of the ring oscillator is shown on a structure where all EGFETs have a W/L-ratio of 600 µm/80 µm, and the resistors a resistance value of 47 kΩ. At a supply voltage of 1 V, the ring oscillator oscillates between values of 0.1 V and 1.0 V, with a frequency of 296 Hz (Figure 5.12a). The output signal is not completely pulled down because the resistance value chosen for the resistors is too low. Figure 5.12b shows that the minimum supply voltage at which an oscillation is observed at 0.6 V ($\sim$ 190 Hz)

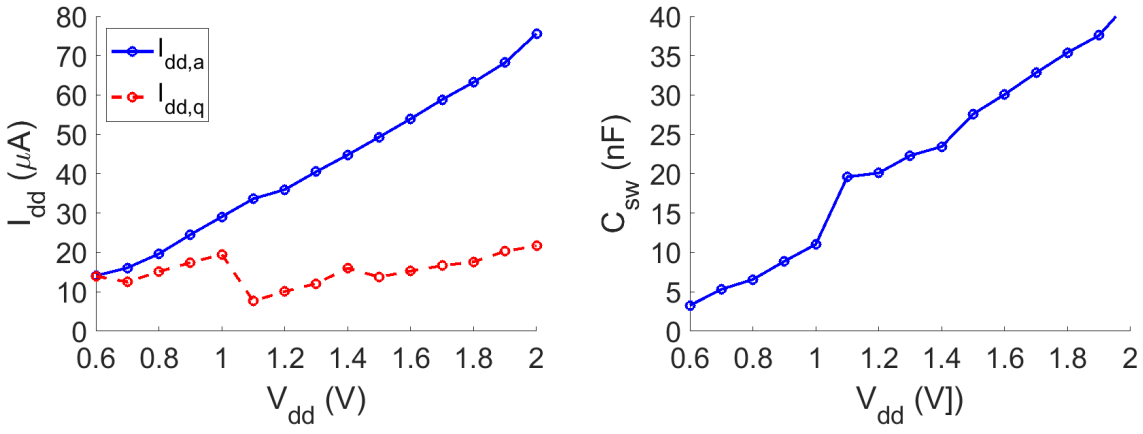


(a) (b)

Figure 5.12.: (a) Output signal of a three stage ring oscillator designed in TRL and measured at a supply voltage of 2.0 V. (b) Frequency dependency of the ring oscillator from the supply voltage.

and the frequency rises with the supply voltage up to ∼ 310 Hz at a supply voltage level of 1.3 V. However, the minimum supply voltage of 0.6 V is also confirmed in other circuits [137, 149, 152]. The frequency of the ring oscillator drops beyond a supply voltage level of 1.3 V because the parasitic capacitance rises with the supply voltage. While printing, the electrolyte spreads unavoidable on the drain- and source-electrodes, forming a parasitic capacitance between the gate-electrode and the respective electrodes. Notability, in electrolytes, the capacitance value is depended on the applied bias.

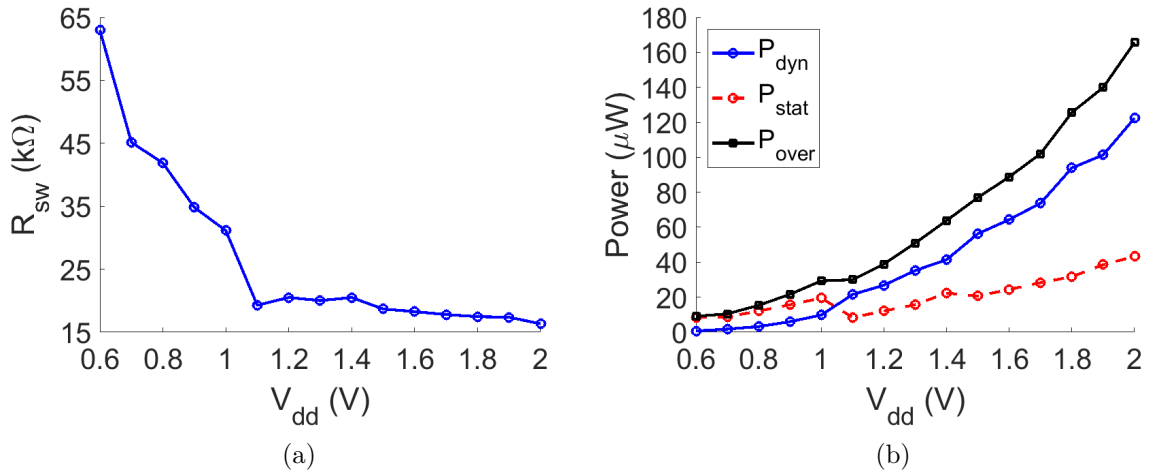
The active current rises linearly with the supply voltage from ∼ 14 µA to ∼ 80 µA and the quiescence current rises from ∼ 14 µA to ∼ 22 µA in a supply voltage range between 0.6 V and 2.0 V (Figure 5.13a). In the same supply voltage range, the switching



(a) (b)

Figure 5.13.: (a) Current flow through the ring oscillator, and (b) switching capacitance of the ring oscillator designed in TRL at different voltage levels.

capacitance increases from 3 nF to ∼ 43 nF (Figure 5.13b). At the same time, the switching resistance decreases from ∼ 63 kΩ to ∼ 16 kΩ (Figure 5.14a) because each EGFET starts to form its individual channel, reducing the overall resistance. Since the falling switching resistance compensates the rising switching capacitance, for lower supply voltage levels (≤ 1.3 V), the frequency of the ring oscillator rises. After a supply voltage level of 1.3 V, the switching capacitance becomes huge and the frequency simultaneously decreases, since the switching resistance flattens. The static power consumption rises from 8.4 µW to 43 µW, in the analyzed voltage window. In the same voltage range, the dynamic consumption increases from 0.6 µW to 122.4 µW. Hence, the total power dissipation increases from 9.6 µW to 165.7 µW (Figure 5.14b). Since the pull-up network is based on a resistor, a high power consumption is expected. However, by replacing the resistor with a n-type EGFET the power consumption eventually reduces as shown in the upcoming sections.



(a) (b)

Figure 5.14.: Evaluation of (a) the switching Resistance, and (b) the power consumption of the ring oscillator designed in TRL at different voltage levels.

5.2. Standard cells in transistor-transistor logic

TRL designs are distinctive through their huge power consumption, which is the result of the usage of a resistor in the pull-up network. To minimize the power consumption, p-type TFTs are preferable to implement pull-up networks in microelectronic structures, in general, but not feasible in oxide electronics. Besides replacing the p-type EGFET with a resistor, n-type EGFETs based pull-up networks are also possible. Circuit designs with exclusively n-type EGFETs, in the pull-up and pull-down networks, are known as TTL designs.

For using an n-type EGFET in the pull-up network, two options are available. The first option is to use the pull-up EGFET, with a positive threshold voltage, as an enhancement load by connecting the gate-electrode of the pull-up EGFET to the supply voltage node. Another option is to connect the gate-electrode of the pull-up EGFET, with negative threshold voltage, to the output voltage node of the logic gate (depletion

load configuration). However, these design approaches are shown to have a high static power consumption and poor noise margins because once the logic 1 level is applied to the input of the logic gate, a large current drives through the structure. [153]

To overcome the drawbacks of TTL designs, two Pseudo-CMOS designs are purposed. The main benefits of these designs are that the TFTs only require one threshold voltage. Also, the designs can be applied for either depletion or enhancement mode TFTs and are feasible for low voltage operation. [153, 154] The Pseudo E-load configuration (Figure 5.15a) is favorable for structures including enhancement mode TFTs and the Pseudo D-load configuration (Figure 5.15b) for structures with depletion mode TFTs.

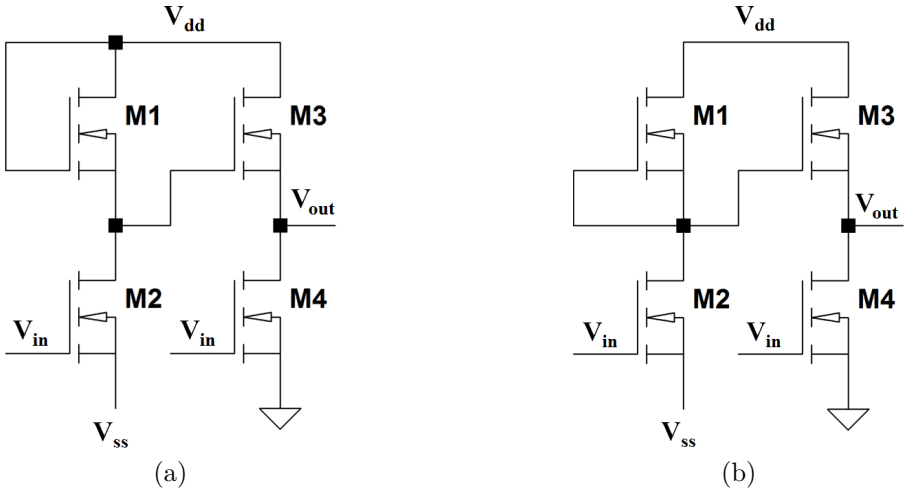


Figure 5.15.: Schematic of the inverters designed in (a) Pseudo E-load and (b) Pseudo D-load.

Unfortunately, the Pseudo-CMOS designs require the double amount of EGFETs, which will drastically reduce the speed of the inverter, since each EGFET introduces a delay to the design because of the intrinsic parasitic capacitance. A further disadvantage of the Pseudo-CMOS design is that two different supply voltage levels (V_{dd} and V_{ss}) are required to completely pull-down the output signal. For that reason the evaluation of TTL designs will be limited to the enhancement and the depletion load configurations, although disadvantageous as discussed above.

5.2.1. Enhancement load configuration

In the TTL with enhancement load configuration, all EGFETs operate in enhancement mode, by choosing a W/L-ratio of 200 µm/90 µm for the pull-up EGFET and a W/L-ratio of 400 µm/90 µm for the pull-down EGFET (Figure 5.16a).

Unfortunately, the threshold voltage from the pull-up EGFET can not be estimated, since the gate-electrode is shortened with the drain-electrode. Figure 5.16b suggests that the pull-up EGFET is operating in enhancement mode because the current starts to rise at voltage levels higher than 0.3 V. The pull-down EGFET has a low threshold voltage (0.05 V) but is still operating in enhancement mode (Figure 5.16c).

If the input voltage of the inverter is logic 0, then the pull-down EGFET is in off-state and the output node is pulled-up towards the supply voltage. The output node can not be completely pulled-up to the supply voltage level because the pull-up EGFET opens in

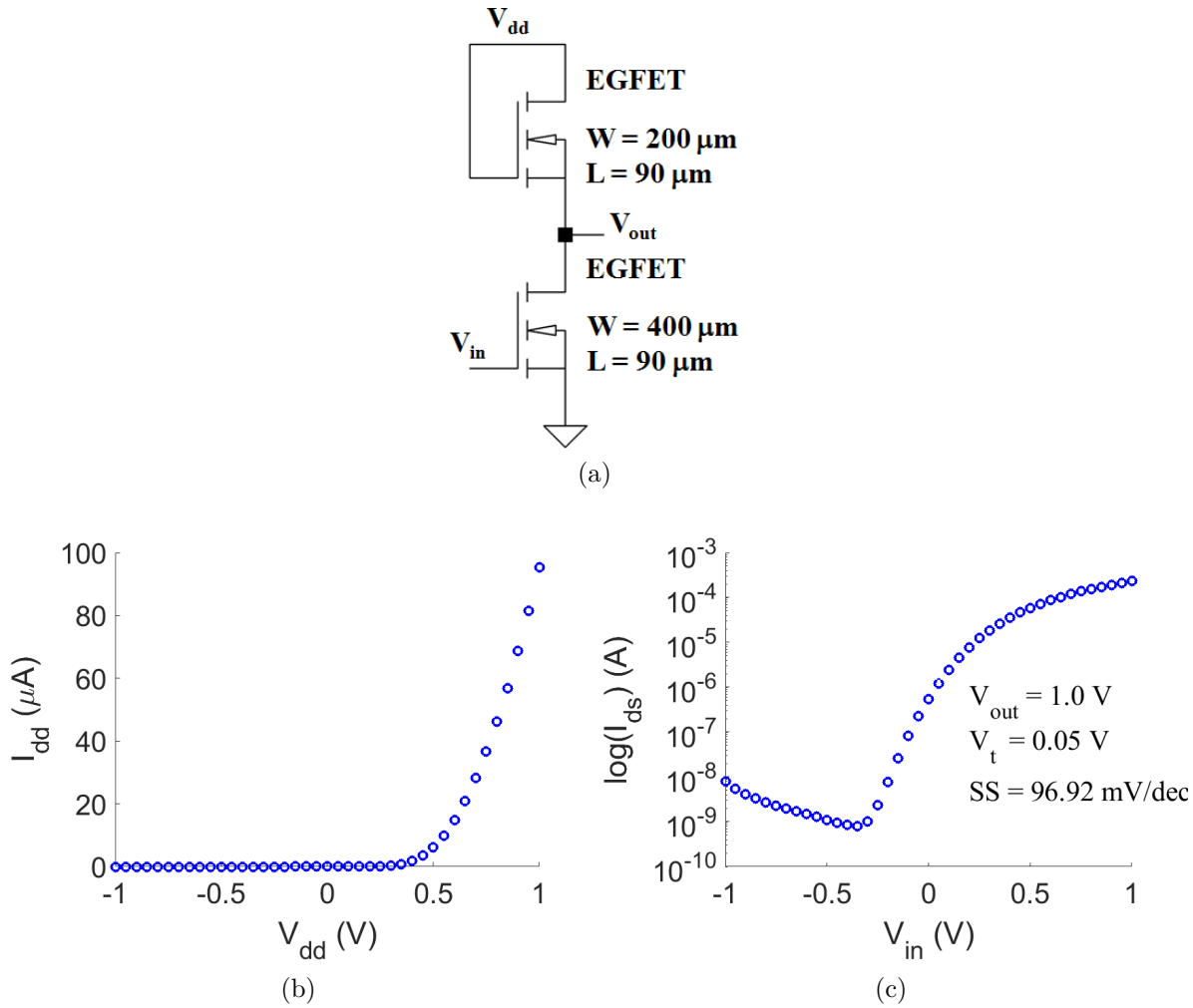


Figure 5.16.: (a) Schematic of an inverter designed TRL with an enhancement load. DC measurements of the (b) pull-up, and (c) the pull-down EGFET at a supply voltage of 1.0 V.

accordance to the applied voltage levels. In this case, the two EGFETs can be simplified through two resistors, forming a voltage divider. Both EGFETs are shut while logic 1 is applied to the input of the inverter. Due to the conductive pull-up EGFET, the minimal value for the output signal is around 0.2 V. Therefore, the output characteristics of the inverter recorded at a supply voltage of 1 V show that the output signal swings between $\sim$ 0.2 V and $\sim$ 0.75 V, and the maximum gain is slightly lower than -1 (Figure 5.17). The low signal swing leads to a low signal-to-noise ratio, which can trigger an unwanted signal transition. Since the gain is very close to -1, it is not possible for a signal to propagate through an inverter chain, because each stage reduces the signal swing until the signal is completely lost.

The infeasibility of the resistor load configuration is further confirmed with the transient analysis (Figure 5.18). Also in the transient analysis, measured at a supply voltage of 1 V, the signal swing is only $\sim$ 0.45 V, making further timing analysis impossible. However, all efforts to build a ring oscillator within the enhancement load configuration failed because of the low gain. Instead of an oscillation, a constant value is

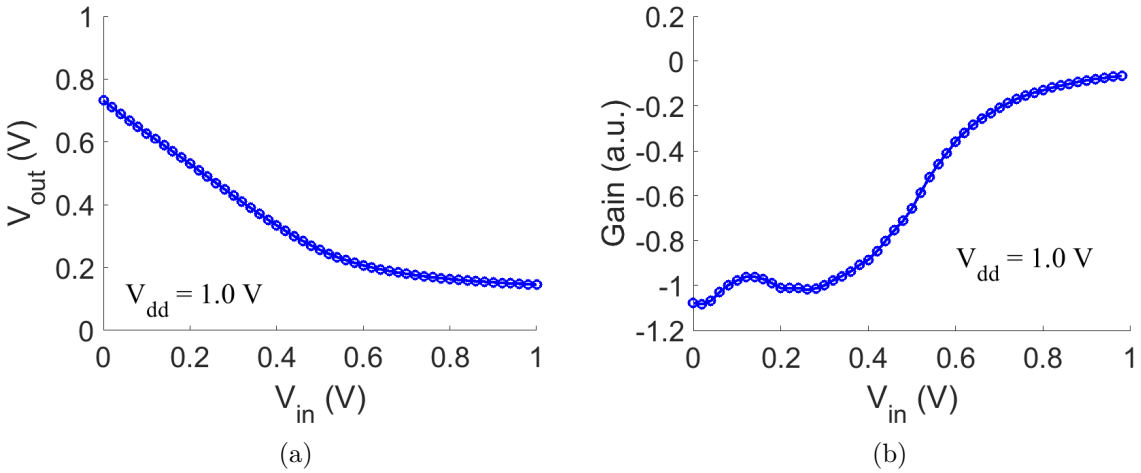


Figure 5.17.: (a) Output characteristics and (b) gain of the inverter designed in the resistor load configuration, measured at a supply voltage of 1.0 V.

observed at the output of the ring oscillator.

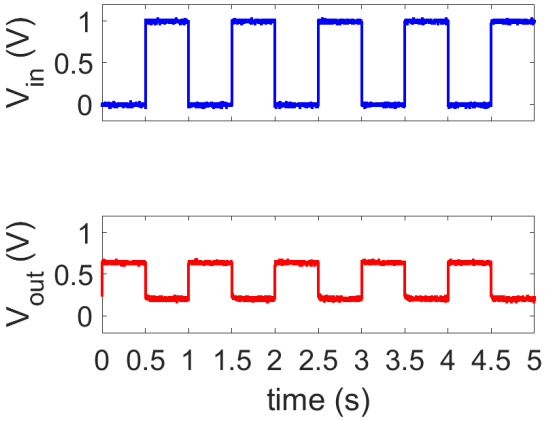


Figure 5.18.: Transient analysis of the inverter in resistor load configuration, measured at a supply voltage of 1.0 V.

The overall performance can be improved by sizing the pull-down EGFET in a way that the current density increases. The most straight forward way to achieve a higher current density in the transistor is to make the channel length smaller and/or by increasing the channel width. This is not an option for the presented transistor technology because changing the channel geometry leads to a shift of the threshold voltage towards negative values, as previously discussed in Section 4.2. As reminder, in the resistor load configuration both EGFETs must operate in enhancement mode. Nevertheless, one workaround to increase the current density in the pull-up network is to use more EGFETs in parallel which increases the required area on the other side.

5.2.2. Depletion load configuration

On option to increase the signal gain of the logic gates, designed in TTL, is through the depletion load configuration. The depletion load configuration requires a pull-up network based on a n-type EGFET. The difference to the enhancement load configuration is that the pull-up EGFET must operate in depletion mode, and the pull-down EGFET in enhancement mode. In the depletion mode configuration, the pull-up EGFET is connected in a way that the gate-electrode of the pull-up EGFET is shorten with the output node of the logic gate. A reliable negative threshold voltage (depletion mode) is achieved by reducing the channel length of the EGFET to 10 µm (Figure 4.5).

Inverter

For an inverter designed in the depletion load configuration, the pull-up EGFET is sized as W/L = 200 µm/10 µm and the pull-down EGFET as 100 µm/90 µm (Figure 5.19a). Also, here the pull-up EGFET can not be measured individually because the gate-electrode is shortened with the source-electrode (Figure 5.19b).

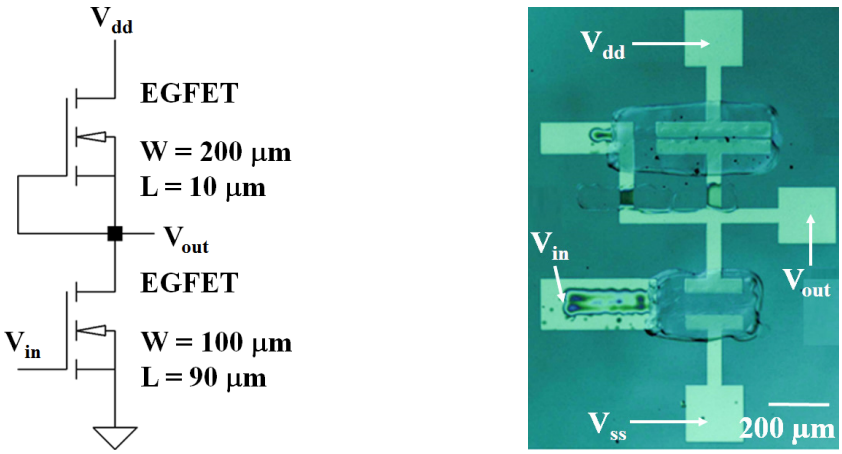
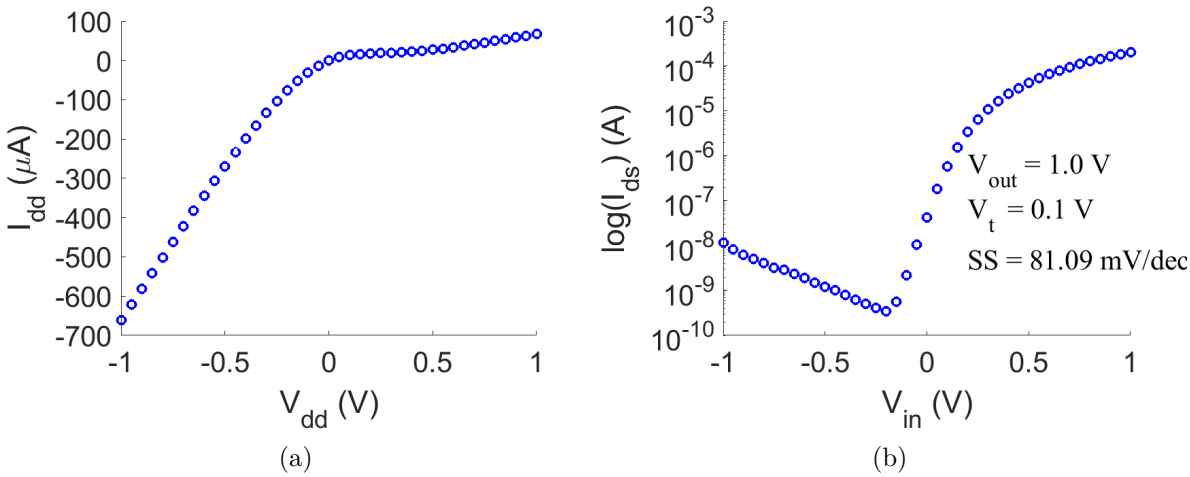


Figure 5.19.: (a) Schematic and (b) microscopic image of the inverter designed in depletion load configuration.

The DC measurement of the pull-up EGFET proves that the EGFET is operating in depletion mode because the current is significantly negative for a negative voltage drop between the drain- and source-electrodes. For a positive voltage drop across the drain- and source electrodes, the absolute value of the current is considerable less (Figure 5.20a). The pull-down EGFET clearly has a positive threshold voltage (0.1 V) and hence is operating in enhancement mode (Figure 5.20b). If Logic 1 is applied to the input of the inverter, the pull-down as well as the pull-up EGFETs shut, and the output signal is pulled down. In the case that logic 0 is applied to the input of the inverter, the pull-down EGFET opens, and the pull-up EGFET stays shut, pulling up the input signal.

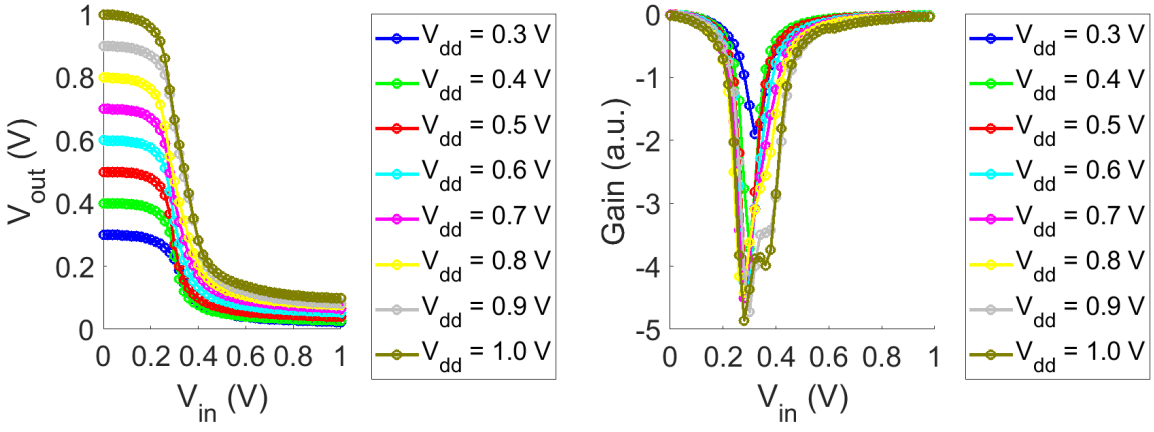
At an input voltage of 0 V, the output voltage is 1.0 V and at an input voltage of 1.0 V, the output voltage is 0.05 V, yielding a signal swing of 0.95 V (Figure 5.21a). The signal swing is in the same range as the voltage swing for the inverter designed in



(a) (b)

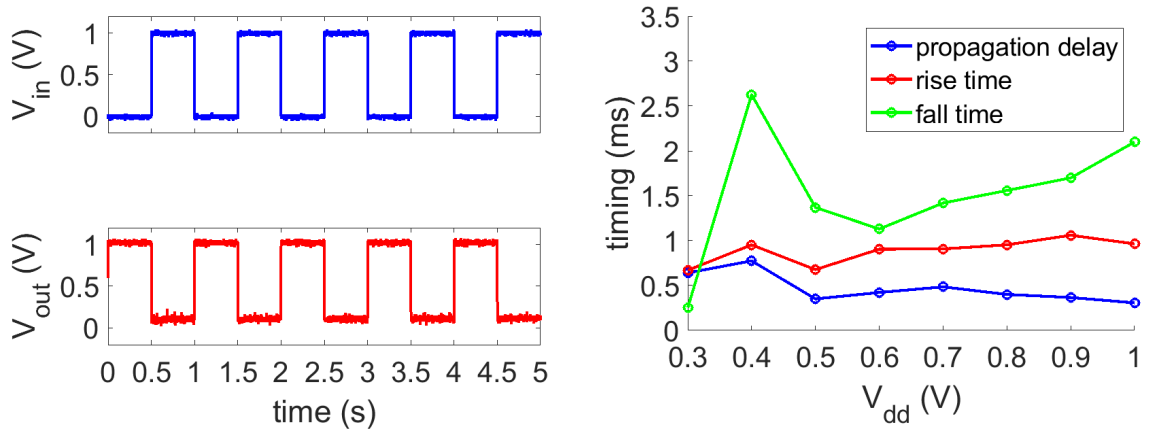
Figure 5.20.: Measurement of (a) the pull-up and (b) the pull-down EGFET, inside an inverter in depletion mode configuration, at a supply voltage of 1.0 V.

TRL (0.9 V), and much higher than the inverter in the enhancement load configuration (0.55 V). Therefore, the inverters designed in the depletion mode configuration are more robust against noise compared to the inverters designed in the enhancement load configuration. In addition, the maximum signal gain is reached at an input voltage of 0.26 V, with a value of -5 (Figure 5.21b), which is higher than values obtained in the enhancement load configuration (~ -1), and in the same range as the inverter designed in TRL. Interestingly, for the depletion load configuration the absolute maximum gain is obtained at higher input voltages because the pull-down EGFET needs a higher input voltage to compensate the high driver capability of the pull-up EGFET. However, the maximum gain should be as close as possible to an input voltage level of half the supply voltage, to make the inverter robust against noise.



(a) (b)

Figure 5.21.: (a) Output characteristics and (b) gain of the inverter designed in depletion mode configuration, measured at a supply voltage of 1.0 V.



(a) (b)

Figure 5.22.: (a) Transient analysis, measured at supply voltage of 1 V, and (b) Timing constants of the inverter designed in depletion load configuration.

The transient analysis confirms that the depletion load configuration is feasible for designing logic gates (Figure 5.22a). The propagation delay time is 0.3 ms, the rise time is 1.0 ms, and the fall time is 2.0 ms (Figure 5.22b), similar to the TRL inverter.

As it is observed for TRL designs, the static power consumption is negligible. Unfortunately, the dynamic power dissipation, and hence, the total power consumption is doubled in comparison with the TRL design (Figure 5.23). The higher power dissipation is due to the pull-up EGFET, which has a higher driver capability compared to the resistor.

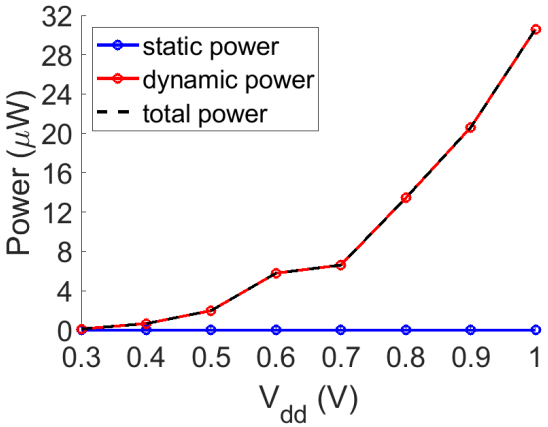


Figure 5.23.: Power consumption of the inverter designed in depletion load configuration at different supply voltage levels.

Table 5.1 compares the inverter structures designed in TRL and TTL. The DC characteristics of both inverter structures, recorded at a supply voltage of 1 V, are similar but the transient characteristics are slightly different. The rise time and the fall time are by 1.8 ms and 0.4 ms, respectively, faster in the TRL case. On the other hand, the propagation delay time is by 0.5 ms faster in the TTL design. Therefore, the timing

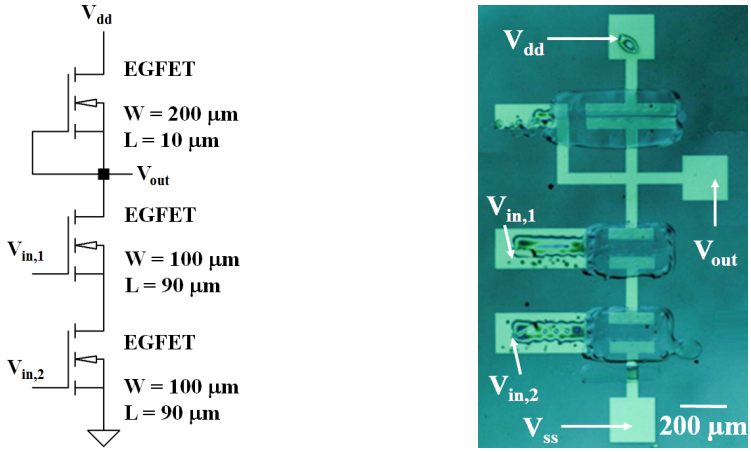
Table 5.1.: Comparison between the inverters designed in TRL and TTL. The timing information are based on measurements performed at a supply voltage of 1.0 V.

Parameter	Transistor resistor logic	Transistor transistor logic
gain (a.u.)	-4.9	-4.9
V_{out} min (V)	1.0	1.0
V_{out} max (V)	0.04	0.07
t_r (ms)	0.6	1.0
t_f (ms)	0.3	2.1
t_{pd} (ms)	0.8	0.3
P_{stat} (nW)	0.5	0.2
P_{dyn} (µW)	20.6	30.6
P_{tot} (µW)	20.6	30.6

analysis suggests that in TRL, the high and low levels are reached faster, but the TTL yields a quicker signal response. The reason behind this timing behavior is that the pull-up EGFET drives a high current, which needs to be compensated by the pull-down EGFET, adding an asymmetry between the pull-up and pull-down network to the design. The high driver capability of the pull-up network is also the reason for the faster signal transition, since parasitic capacitances are charged in a lesser time compared to the TRL design. The higher driver capability of the pull-up network lead to an increase of the dynamic and total power consumption, both from 20.6 µW to 30.6 µW. The difference in the static power dissipation is negligible (0.5 nW (TRL) and 0.2 nW (TTL)).

NAND gate

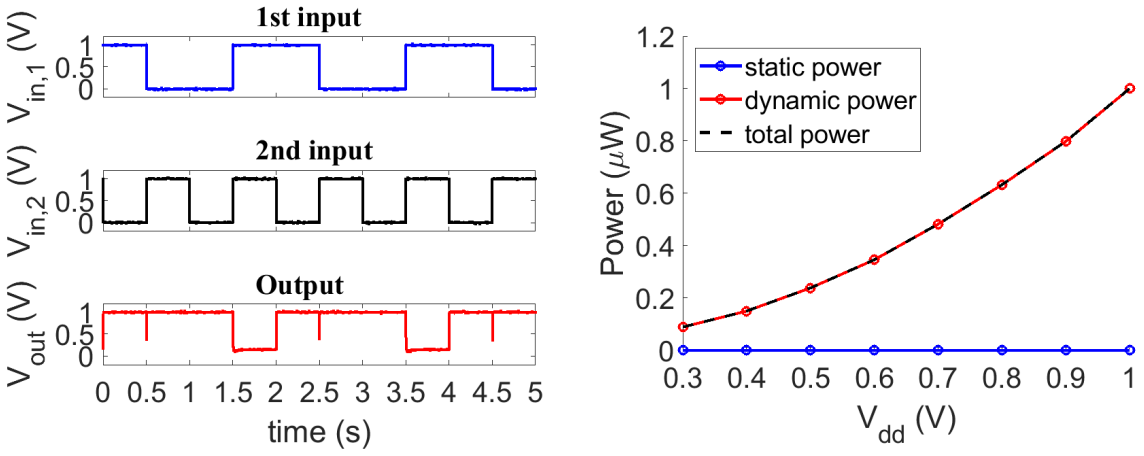
The NAND gate, within the depletion load configuration, is based on a normally-on pull-up EGFET, with a W/L-ratio of 200 µm / 10 µm, and two in series connected normally-off pull-down EGFETs, with a W/L-ratio of 100 µm / 90 µm (Figure 5.24).



(a) (b)

Figure 5.24.: (a) Schematic and (b) microscope image of a NAND gate designed in depletion load configuration.

The transient analysis of the NAND gate measured at a supply voltage of 1.0 V shows the proper functionality of the NAND gate (Figure 5.25a). Also for TTL, the static power consumption is negligible. In contrast, the dynamic power consumption rises from ~ 0.1 µW to ~ 1.1 µW in a supply voltage range between 0.3 V and 1.0 V, respectively. Since the static power consumption is negligible, the total power dissipation is in the same range as the dynamic power consumption (Figure 5.25b). The TTL design reduces the static power consumption from 10 nW to 0.2 nW (Table 5.2), because the leakage currents are lower. Interestingly, the dynamic and total power consumption are in all cases 1 µW. Therefore, the choice of the design has a negligible influence on the power consumption of the NAND gate. As discussed for the TRL design, the power consumption is for the NAND gate much lower compared to the inverter because the two EGFETs connected in series in the pull-down network limit the time where a direct connection from the supply voltage node to the ground is available. By comparing the output voltage levels and the power consumption of the NAND gates, designed in TRL and the depletion load configuration, one can see that both NAND gates perform equally.



(a) (b)

Figure 5.25.: (a) Transient analysis of a NAND gate in TTL, at supply voltage of 1.0 V. (b) Power consumption of the NAND gate in dependency of the applied supply voltage.

Table 5.2.: Electrical comparison of a NAND gate designed in TRL and TTL at a supply voltage of 1 V.

Parameter	Transistor resistor logic	Transistor transistor logic
V_{out} min (V)	0.09	0.13
V_{out} max (V)	0.98	1.0
P_{stat} (nW)	10.0	0.2
P_{dyn} (µW)	1.0	1.0
P_{tot} (µW)	1.0	1.0

NOR gate

Figure 5.26 shows the schematic and microscope image of a NOR gate designed in TTL with the depletion load configuration. The transient characteristic of the NOR gate is

as expected (Figure 5.26c). As for the NAND gate, the static power consumption is negligible, while the dynamic power rises from ∼ 0.2 µW to ∼ 11.4 µW at supply voltage levels between 0.3 V and 1.0 V. Since the static power is negligible, the total power consumption is defined by the dynamic power (Figure 5.26d). Table 5.3 compares the NOR gate designed in TRL with the depletion load configuration. Both logic designs perform equally, and in terms of performance neither is preferable over the other. Also for the TTL design the power consumption is higher compared to the NAND gate because the two pull-down EGFETs are connected in parallel as disused in Section 5.1.1.

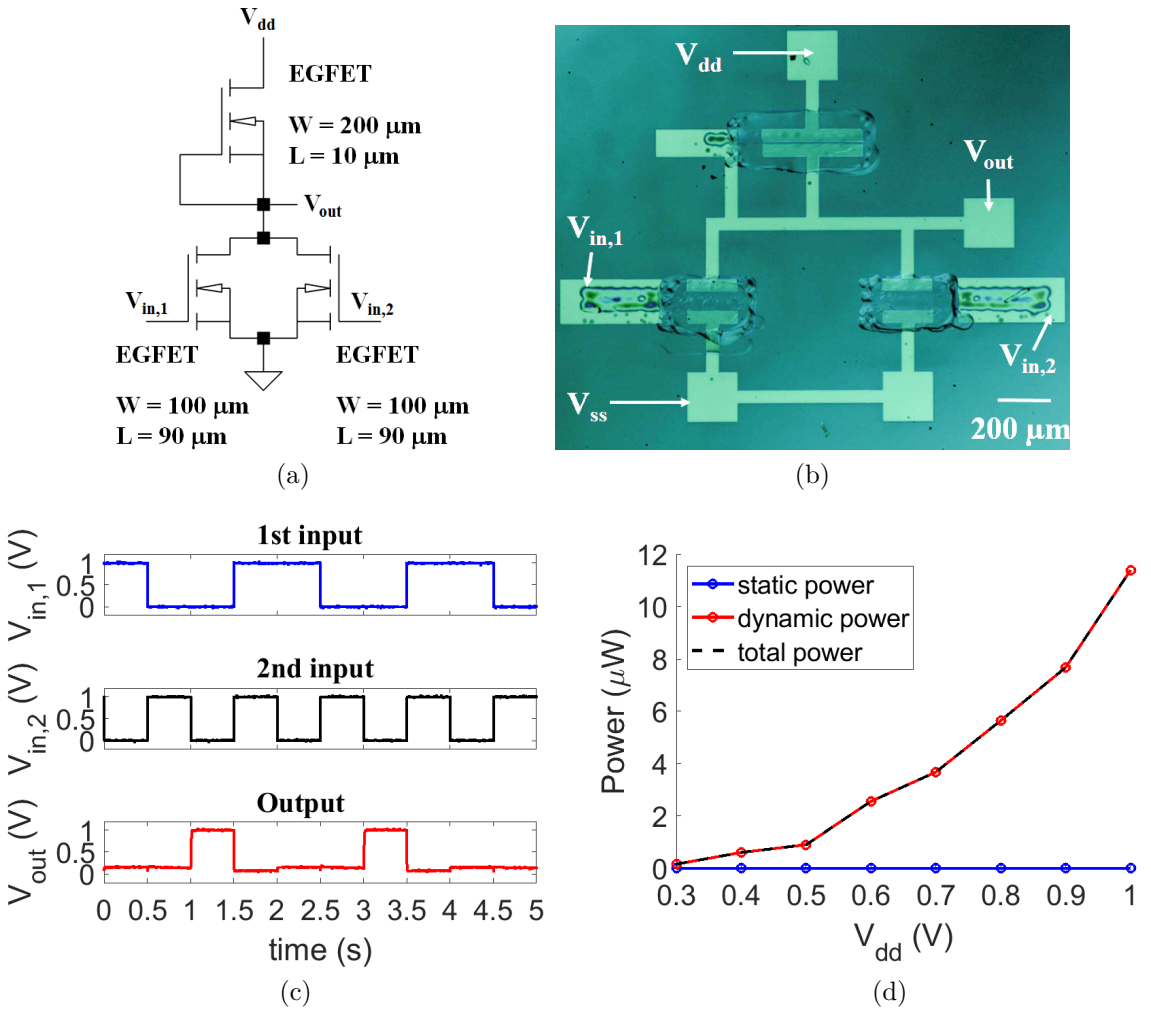


Figure 5.26.: (a) Schematic, (b) microscope image, (c) Transient characteristics, at a supply voltage of 1 V, and (d) power consumption of a NOR gate with depletion load.

Table 5.3.: Comparison between the NOR gate designed in TRL and TTL measured at V_{dd} =1 V.

Parameter	Transistor resistor logic	Transistor transistor logic
V_{out} min (V)	0.04	0.04
V_{out} max (V)	0.93	1.0
P_{stat} (nW)	1.7	0.6
P_{dyn} (µW)	15.6	11.4
P_{tot} (µW)	15.6	11.4

XOR

Similar to the TRL, by characterizing a XOR gate, a more complex circuit is designed, within the depletion load configuration. The XOR gate is based on four NAND gates (Figure 5.27).

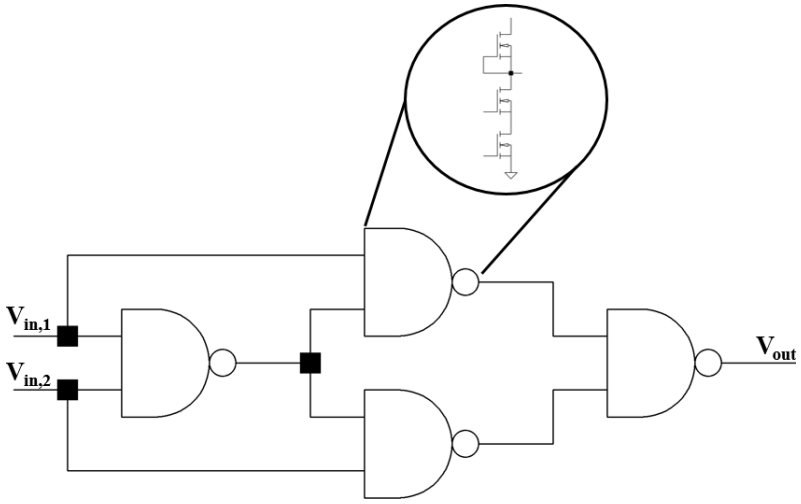
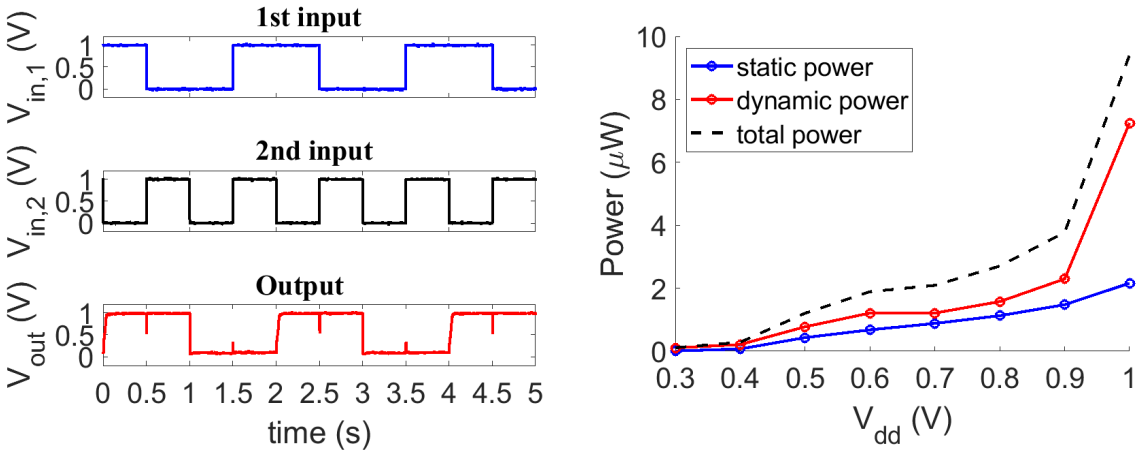


Figure 5.27.: Schematic of a XOR gate designed in TTL.

The correct functionality of the XOR gate is seen in the transient analysis (Figure 5.28a). The static power consumption rises from $\sim$ 0.1 µW to $\sim$ 2.1 µW, at a supply voltage between 0.3 V and 0.9 V. In the same voltage range, the dynamic power consumption rises from $\sim$ 0.1 µW to $\sim$ 2.3 µW. However, at a supply voltage of 1 V, the dynamic power consumption jumps to a value of $\sim$ 8 µW (Figure 5.28b). Since a sudden increase of the power consumption is not expected, the measured dynamic power value at a supply voltage of 1 V is considered to be artificial. Therefore, the maximum power consumption is extrapolated to be $\sim$ 5 µW.



(a) (b)

Figure 5.28.: (a) Transient characteristics, measured at a supply voltage of 1 V, and (b) Power consumption of the XOR gate with a depletion load.

Comparing the XOR gates designed in TRL and the depletion load configuration (Table 5.4), shows that the achieved output voltage levels are feasible, as for the other logic gates. In TTL, the static power consumption is reduced from 15.5 µW to 2.2 µW. Also a huge reduction in the dynamic and total power consumption is observable by using the TTL design. The dynamic power consumption decreases from 15.3 µW to 7.3 µW, while the total power consumption reduces from 30.8 µW to 9.4 µW. The reduction in power dissipation is so pronounced because, in TRL, regardless of the voltage level of the input signals, always at least one NAND gate is turned on. This is why always a conductive path from the supply voltage to ground is present in TRL. On the other hand, in TTL only at a signal signal transition, a conductive path from the supply voltage node to the ground is available.

Table 5.4.: Comparison of the output voltage levels and power consumption between a XOR gate designed in TRL and TTL at a supply voltage of 1 V.

Parameter	Transistor resistor logic	Transistor transistor logic
V_{out} min (V)	0.12	0.08
V_{out} max (V)	0.98	1.0
P_{stat} (µW)	15.5	2.2
P_{dyn} (µW)	15.3	7.3
P_{tot} (µW)	30.8	9.4

Ring oscillator

Finally, the depletion load configuration will be tested on a three-stage ring oscillator structure. Similar to TRL, the first stage is a NAND gate and the output signal is measured through an output inverter stage, which is isolated from the ring oscillator structure. As for the other logic gates, all EGFETs in the pull-up network have a W/L-ratio of 200 µm/10 µm, and for the EGFETs in the pull-down network the W/L-ratio is 100 µm/90 µm. The schematic and the microscopic image of the ring oscillator are shown in Figure 5.29; as a reminder, the switching resistance (R_{sw}) and switching capacitance (C_{sw}) elements are not printed and included in the schematic to model the delay of each stage in simulation. All parasitic effects resulting from the EGFETs and the interconnects are summarized in the elements R_{sw} and C_{sw}.

The output signal of the ring oscillator is shown in Figure 5.30a, at a supply voltage of 1.0 V, where an oscillation frequency of 364 Hz is observed. In the depletion load configuration, the minimal supply voltage is $\sim$ 0.7 V. The frequency increases from $\sim$ 250 Hz to $\sim$ 1750 Hz, in a supply voltage range between 0.7 V and 2.0 V. This result clearly shows that it is possible to operate applications in the sub-kHz region within the EGFET transistor technology.

As discussed in Section 5.1.4, when measuring the active and quiescence currents (Figure 5.31a), the values of the switching resistance, the switching capacitance, as well as the power consumption of the ring oscillator is estimated. Something noticeable is that the quiescence current is higher than the active current, which is obvious since the pull-up EGFET is able to drive a high current. The switching capacitance falls from 9.7 nF to 2.8 nF within a supply voltage range from 0.7 V to 2.0 V (Figure 5.31b). The

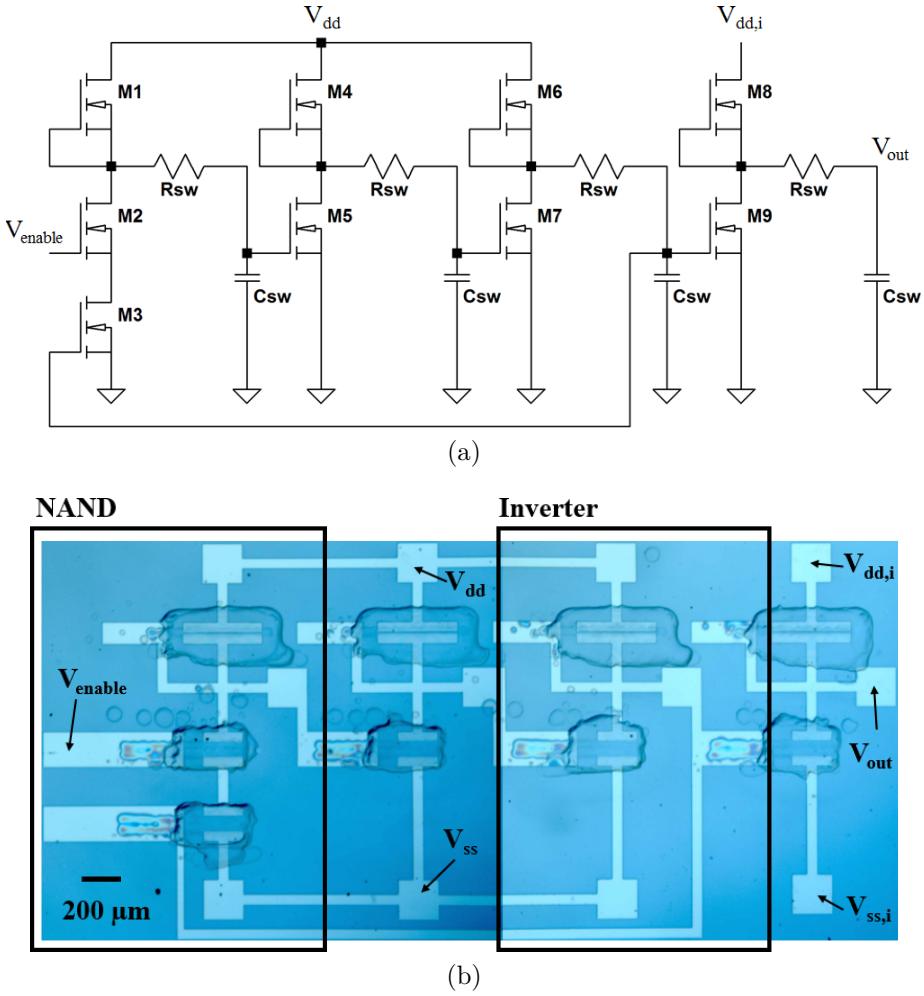


Figure 5.29.: (a) Schematic and (b) microscopic image of a ring oscillator designed in TTL.

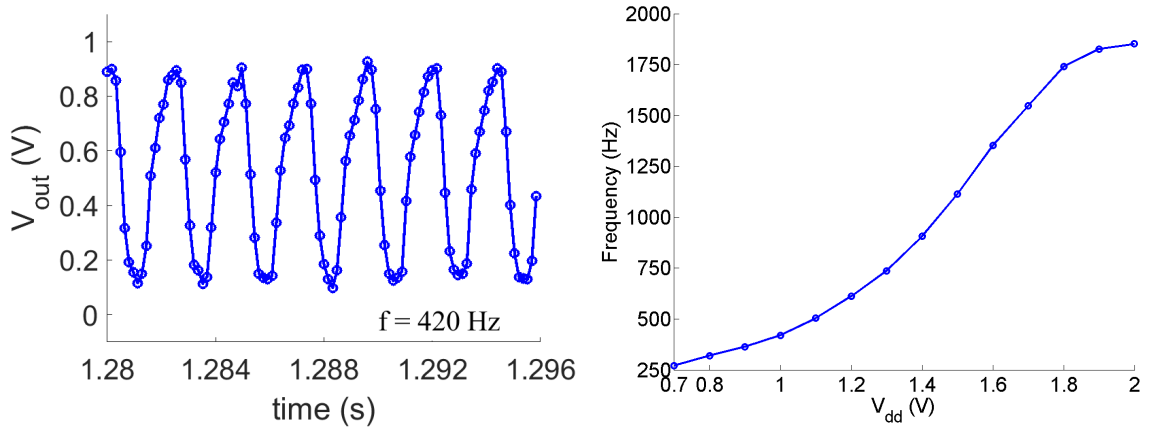


Figure 5.30.: (a) Output signal measured at a supply voltage of 1 V, and (b) dependency of the frequency from the supply voltage of a three-stage ring oscillator designed in TTL.

decreasing behavior of the switching capacitance is counter intuitive, but can be explained with the parasitic capacitance introduced by the pull-up EGFET, which is connected in series with the parasitic capacitance of the pull-down EGFET. Because the area of the electrolyte is smaller in the pull-up EGFET, the pull-up EGFET contributes with a smaller parasitic capacitance, thus dominates the switching capacitance. Therefore, both parasitic capacitances rise with the applied voltage, and since they are connected in series, the switching capacitance drops for lower supply voltage levels (0.9 V). Due of the interdependence of the parasitic capacitances, the switching capacitance has the trend to saturate for supply voltage levels higher than 0.9 V. At the same time the switching capacitance shrinks, the switching resistance decreases from 63.3 kΩ to 31.5 kΩ (Figure5.31c) because the channel conductance of each EGFET rises with the supply voltage, both, being the reason for the high frequency achieved within TTL designs. However, in the same voltage range, the overall power consumption rises from 21.7 µW to 591.1 µW (Figure 5.31d). The high power consumption is due to the static power dissipation resulting from the high conductivity of the pull-up EGFETs.

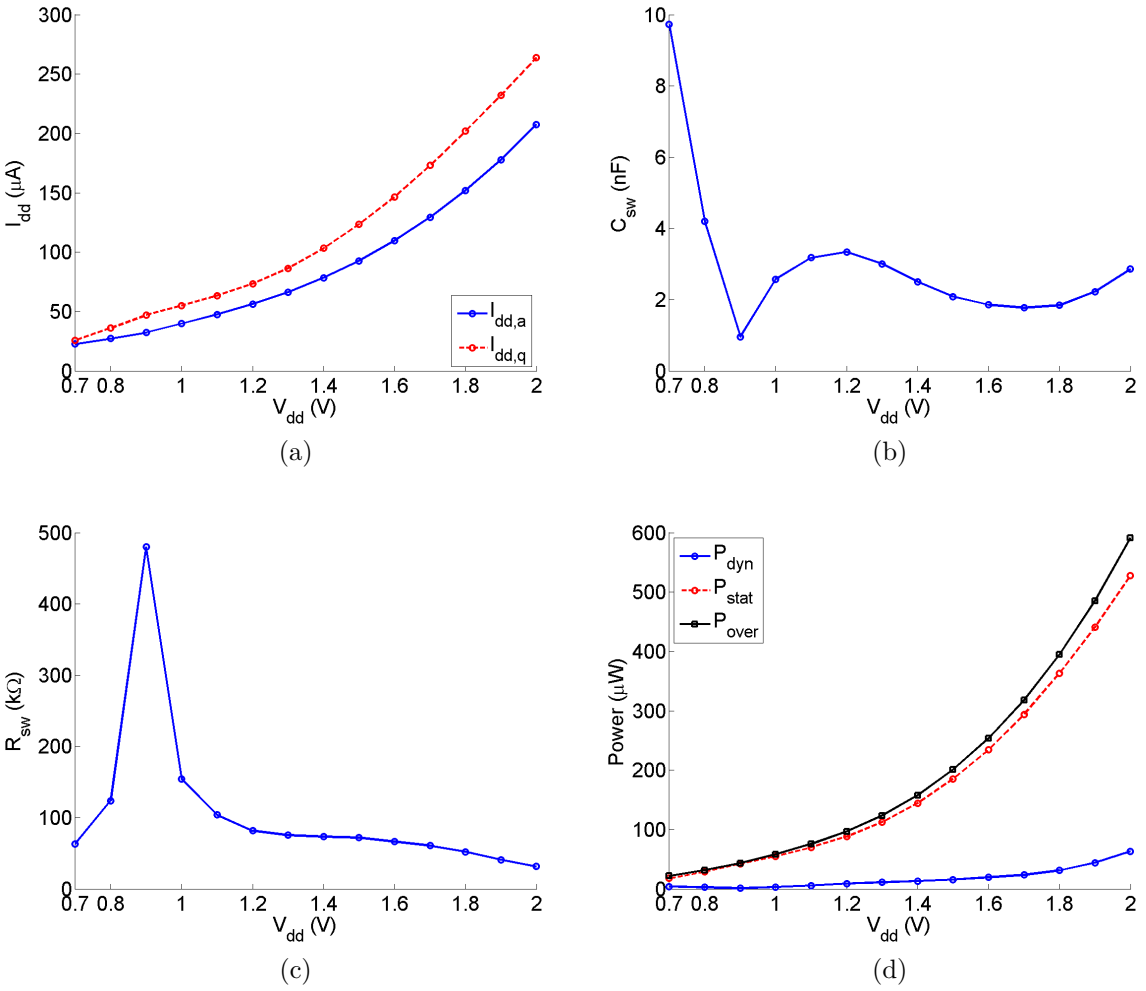


Figure 5.31.: (a) Measured current, (b) switching capacitance, (c) switching resistance, and (d) power consumption of the ring oscillator, designed in TTL, at different voltage levels.

In Table 5.5 a comparison is made, between the ring oscillator designed in TRL, and TTL at a supply voltage of 1.0 V. At this voltage level, the frequencies of both designs are comparable. However, at higher supply voltage levels ($> 1\ V$), in TTL, the frequency of the ring oscillator rises up to the sub kHz-regime, outperforming the TRL design. This is due to the fact that in TTL the switching resistance reduces with the supply voltage, because of the increased conductivity of the EGFETs with the applied potential, while the switching capacitance is low compared to the TRL design. The static power consumption is in the TRL case 19.5 µW and 54.8 µW in the TTL based ring oscillator. The static power consumption is expected to be higher in the TTL design due to the higher driver capability of the EGFETs in the pull-up network. However, the dynamic power consumption reduces from 9.8 µW to 3.2 µW by changing from TRL to TTL, since the pull-up network is in TTL only active during a signal switch. Nevertheless, the total power consumption is in TRL 29.3 µW, and in TTL 58.1 µW, showing that TTL consumes more power.

Table 5.5.: Comparison between the ring oscillator in TRL and TTL, at a supply voltage of 1.0 V.

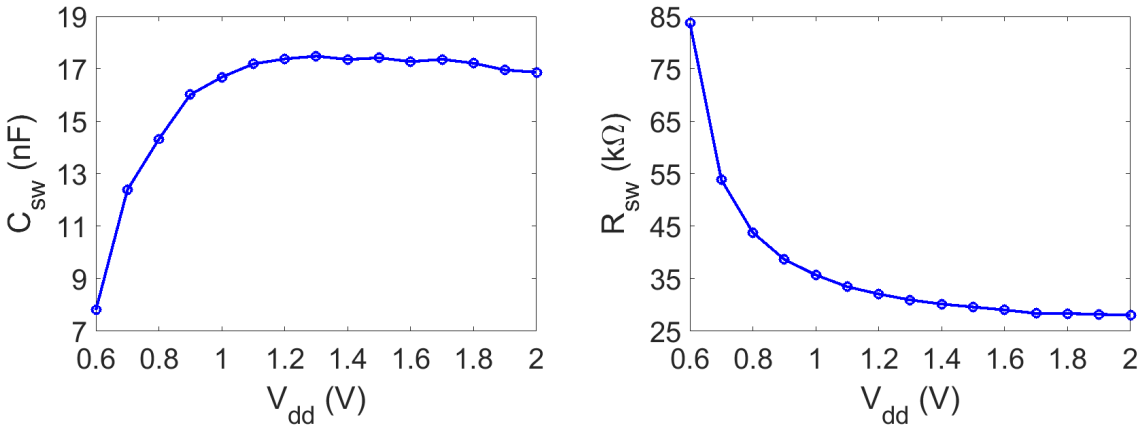
Parameter	Transistor resistor logic	Transistor transistor logic
f (Hz)	296	364
C_{sw} (nF)	11.0	2.6
R_{sw} (kΩ)	31.1	154.1
P_{stat} (µW)	19.5	54.8
P_{dyn} (µW)	9.8	3.2
P_{tot} (µW)	29.3	58.1

The measurements of the logic gates and ring oscillator structures clearly shows that TTL designs might be beneficial to increase the operation frequencies but are not always the best choice in terms of power consumption. However, the TTL designs are very efficient in reducing the power dissipation in NAND gates because the pull-down network consists of to in series connected EGFETs, as discussed previously. Therefore, instead of designing circuits with inverters, like it is the case for ring oscillator structures, NAND gates are an attractive alternative to reduce the power consumption.

6. Model-hardware correlation

SPICE simulations are very popular to optimize or to study the behavior of a circuit. As an example, the channel geometry, of the EGFET, and resistance values, used in the previous Sections, are chosen in accordance to prior performed simulations. The EGFET channel geometry and the resistance values, are varied, in simulation, until the signal gain is maximized. In a robust circuit design, impervious to noise, the maximum gain is obtained at an input voltage close to $V_{dd}/2$. In general, the optimization of logic gates are done on inverter structures, since inverters have the least complexity and are similar to other logic gates (based on a pull-up and a pull-down network). However, it is important that the simulation correlates with the measurement. Once it is ensured that the simulation can predict the behavior of a circuit, the circuit designer develops and optimizes a circuit on simulation level before it is fabricated.

To demonstrate the accuracy of the simulation by using the EGFET technology and the modeling approach presented in Chapter 4, a three stage ring oscillator is designed in TRL (Figure 5.11a). The resistors, in the pull-up network, have a resistance value of 60 kΩ, and the W/L-ratio of all EGFETs, in the pull-down network, is 400 µm/40 µm. The values for the switching capacitance and resistance are chosen in accordance to Figure 6.1. [64]



(a) (b)

Figure 6.1.: Measured (a) switching capacitance and (b) switching resistance in dependence of the supply voltage of a three-stage ring oscillator.

Comparing the measured frequency of the ring oscillator with the simulated data (Figure 6.2) proves that a good agreement between simulation and measurement is achievable. The error of the simulations is only around 4 %. Nevertheless, the error is negligible at a supply voltage of 1 V, which is the targeted supply voltage.

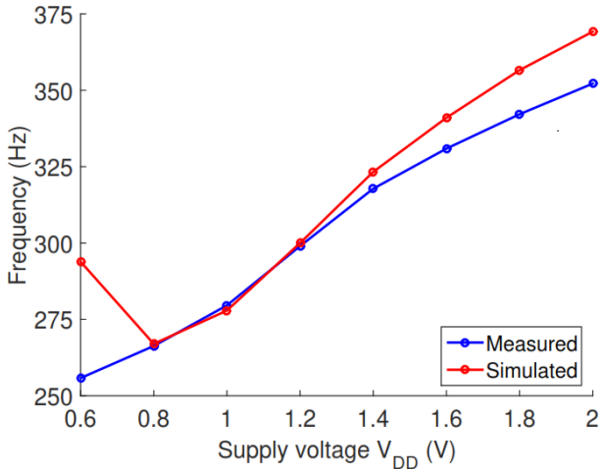


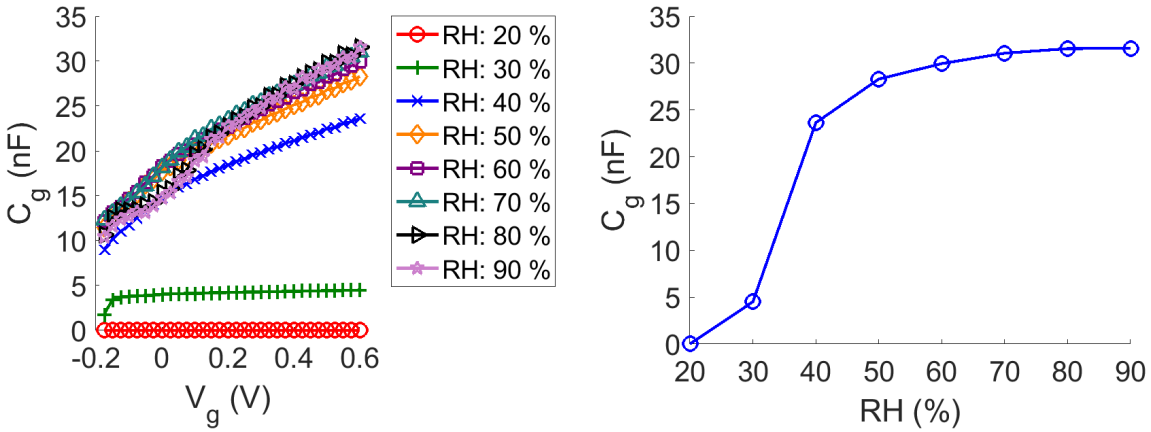
Figure 6.2.: Simulated and measured frequency dependency from the supply voltage in a three-stage ring oscillator designed in TRL. Reprint with permission from [64] © 2018 IEEE.

In the following, the influence of the humidity on the performance of a ring oscillator is studied through measurements and simulation. A disadvantage of the modeling approach presented in Section 4.4 is that the model is only a DC model. Therefore, for transient analysis, the switching resistance and the switching capacitance are added as delay elements to the output of logic gates. Consequently, as replacement for the switching resistance and the switching capacitance, in simulation, a model for the EGFET terminal capacitances is presented and discussed on a ring oscillator structure.

6.1. Humidity effects

Before simulating the ring oscillator based on EGFETs, the influence of the humidity on EGFETs is studied. It is well known that electrolytes are sensitive to moisture, and therefore predestined for humidity capacitive sensor applications. [155–157] This sensitivity to humidity is especially pronounced in dry polymer electrolytes where the ion drift takes place along a polymer matrix. The same situation is found in the CSPE because the PC stays trapped in the PVA based polymer backbone. Furthermore, residuals of DMSO are used by the ions as conductive side channels. [158, 159] In consequence, a certain humidity level is required to establish the HDL in an EGFET, since absorbed water (H_2O) molecules/hydroxyl ions help to establish conducting pathways, which is proven by measuring the gate-capacitance at different relative humidity (RH) levels. The measurement of the gate-capacitance of a EGFET with a W/L-ratio of 400 µm / 40 µm at different relative humidity levels suggest that a minimum relative humidity level of 30 % is required, to establish the HDL. With increasing the RH, the gate-capacitance value rises until saturating at a relative humidity level of $\sim$ 50 % (Figure 6.3). [134]

Table 6.1 summarizes the values obtained for the on-current, the off-current and the threshold voltage at different relative humidity levels. Interesting are the relative humidity values where the HDL is fully established (RH $\geq$ 50 %). In this regard, for relative humidity levels between 50 % and 90 %, the on-current slightly rises by a factor



(a) (b)

Figure 6.3.: (a) Gate-capacitance plotted against the gate-voltage at different humidity levels. (b) gate-capacitance versus the relative humidity at a gate-source voltage of 0.6 V. Reprint with permission from [134] © 2019 IEEE.

Table 6.1.: Electrical parameters of the EGFET under different humidity conditions. [134]

RH (%)	I_{on} (µA)	I_{off} (µA)	I_{on}/I_{off} (10^5)	V_t (V)
20	4.731	3.328	-	-
30	224.764	0.001	3.35	0.01
40	249.554	0.001	2.10	-0.07
50	266.172	0.002	1.29	-0.12
60	278.459	0.004	0.79	-0.17
70	279.990	0.006	0.44	-0.20
80	279.556	0.010	0.27	-0.21
90	282.463	0.017	0.16	-0.27

of 1.06. A more pronounced effect is observed for the off-current and the threshold voltage where in the same relative humidity range their values rise by a factor of 8.5 and 2.25, respectively. The absorbed H_2O/hydroxyl ions may define the carrier concentration at the surface of the semiconductor, but scattering effects or carrier density saturation may flatten the on-current. The fact that the off-current rises with the relative humidity may prove that the H_2O/hydroxyl ions control the carrier density at the surface of the In_2O_3. Furthermore, the increasing carrier density at the electrolyte/semiconductor interface leads to a threshold voltage shifting towards negative voltage levels. This is because lower voltages are required to establish a channel, due to the increased carrier density at the surface of the semiconductor. [134]

The output curves of the discussed EGFET, measured at different relative humidity levels (Figure 6.4), confirms that a minimum relative humidity level of 30 % is needed to operate the EGFET. Furthermore, the drain-source current increases with the relative humidity, because of the higher charge carrier density at the surface of the semiconductor. For RH $\geq$ 80 %, the drain-source current decreases due to charge carrier scattering.

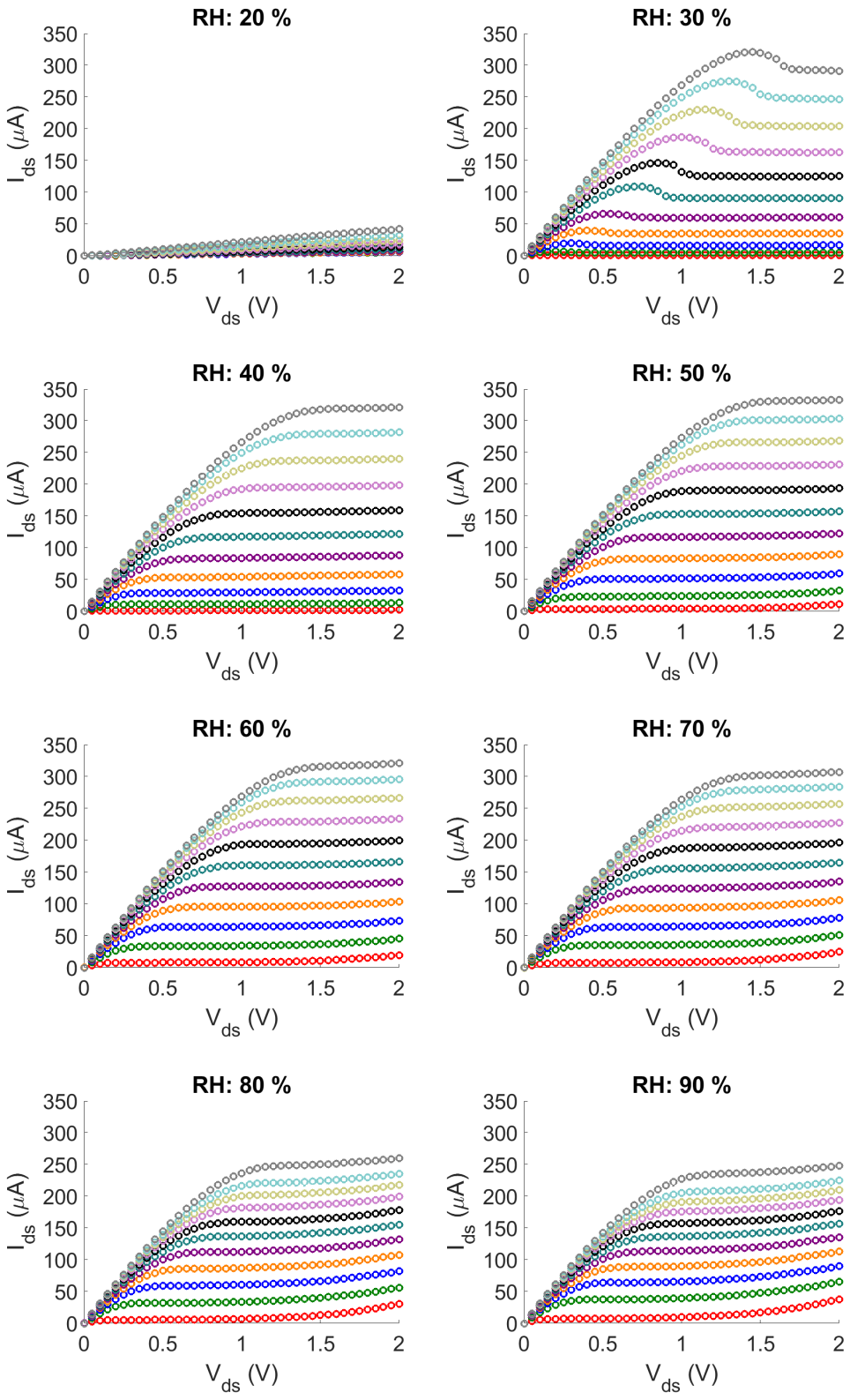


Figure 6.4.: Output characteristics of an EGFET measured at different relative humidity conditions. In each output curve, the gate-source voltage is varied from 0.0 V to 1.0 V in 0.1 V steps.

By plotting the transfer curves at various humidity levels, and eliminating the factor of the threshold voltage from the curves, it is possible to observe that the main parameters influenced by the humidity are in fact the off-current, as well as the threshold voltage. All transfer curves, measured from 30 % to 90 %, overlap by excluding the threshold voltage from the transfer curves (Figure 6.5). The overlapping of the transfer curves clearly shows that the semiconductor is not influenced by the humidity, otherwise the drain-source current current would change with the humidity in the plot shown in Figure 6.5. However, for relative humidity levels $\leq$ 20 %, the EGFET does neither switch on nor off, because the conductivity of the CSPE is too low to establish a HDL, and the drain-source current current is mainly defined by the channel resistance and is not tuned by electrostatic coupling like it is usual for TFTs. [134] Since the transfer curve, measured at a RH of 20 % overlaps with the other transfer curves, measured at an overdrive voltage (V_{gs} - V_t) around 0 V, confirms that the curve measured at a RH of 20 % is the semiconductor conductivity.

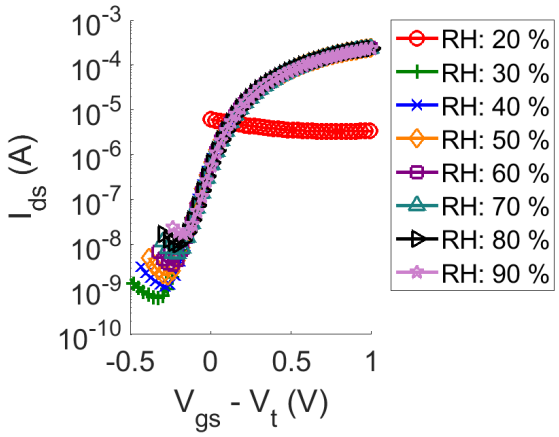


Figure 6.5.: Transfer curve of an EGFET at various relative humidity levels.

To analyze the influence of the humidity on a circuit level, a three stage ring oscillator is characterized under different humidity conditions. The pull-up resistors have a resistance value of 40 kΩ and the pull-down EGFETs a W/L-ratio of 400 µm/ 40 µm. [134] As design topology the TRL is chosen to avoid any side effects which might be introduce by a pull-up EGFET.

By increasing the relative humidity from 20 % to 60 %, the frequency of the output signal rises with the relative humidity. If the relative humidity is further increased, the signal frequency drops with increasing the relative humidity (Figure 6.6a). The reason behind this frequency behavior lies in how the transistor capacitances, summarized in the switching capacitance, are affected by the moisture. Until a relative humidity of 40 %, low mobile ions cause a huge capacitance. For higher relative humidity values, absorbed H_2O/hydroxyl ions may decrease the resistance of the electrolyte, reducing the capacitance value. At relative humidity levels $\geq$ 60 %, the absorbed ions will additionally accumulate between the electrolyte/semiconductor and the electrolyte/interconnects interfaces, further increasing the switching capacitance (Figure 6.6b). On the other hand, the switching resistance decreases with increasing the relative humidity level, which is to be expected, since more charge carriers are accumulated at the surface of the channel,

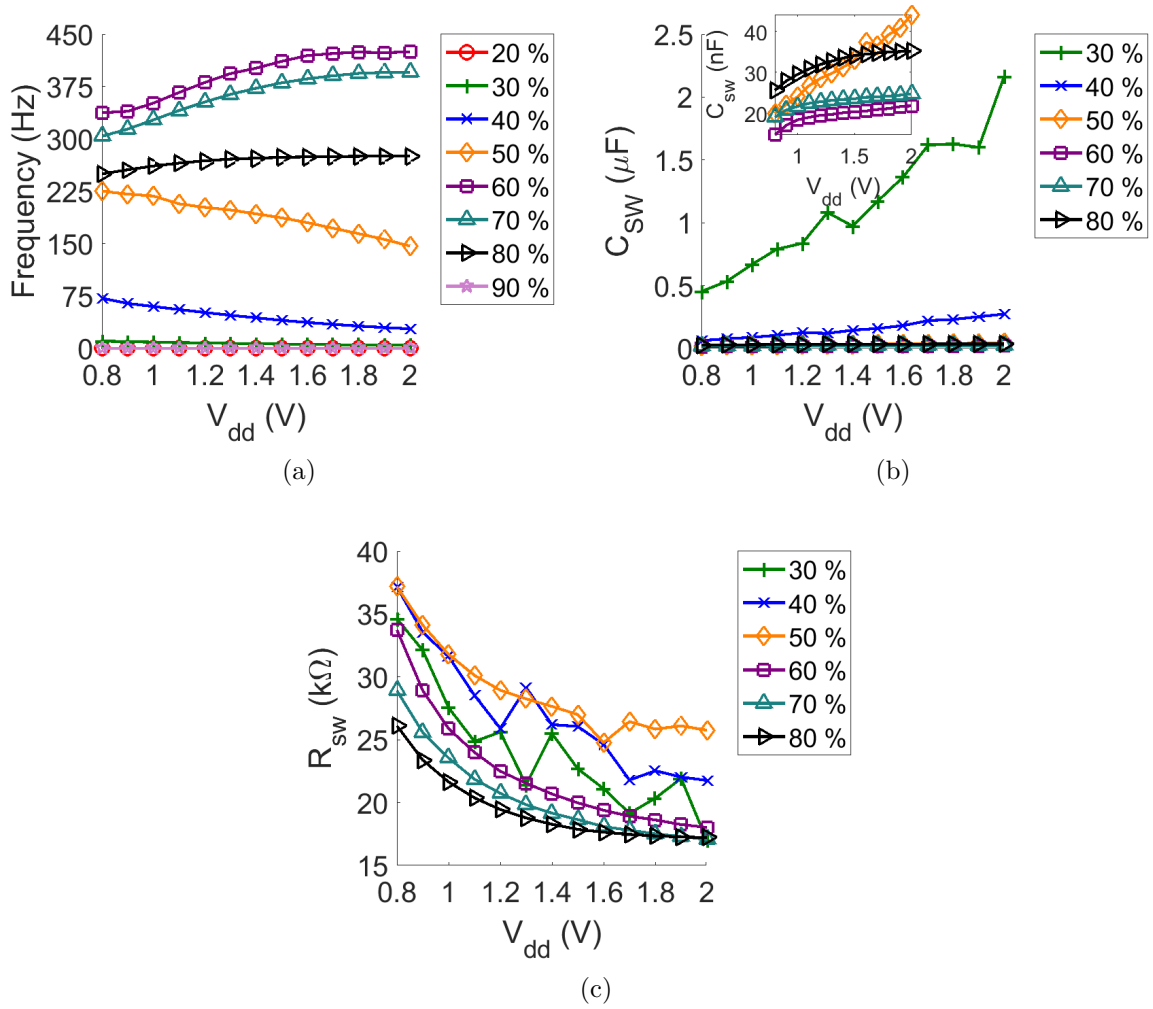


Figure 6.6.: Dependency of (a) the frequency, (b) the switching capacitance, and (c) the switching resistance from the relative humidity of an three stage ring oscillator. Reprint with permission from [134] © 2019 IEEE

increasing the conductivity of the EGFET. [134]

Plotting the output signal of the ring oscillator at a supply voltage of 2 V, and at different RH levels, shows that the frequency increases with the RH level, in a range from 20 % to 60 %, however, decreasing for higher RH levels. In addition, the signal swing reduces constantly with increasing RH level (Figure 6.7). This effect is explained with the shift in the threshold voltage. As discussed, the threshold voltage of an individual EGFET shifts towards negative values with increasing RH, changing the ratio between the pull-up resistance and the channel resistance. If the channel becomes conductive at low gate-voltage levels, then the output signal is no longer able to be pulled up because the EGFET is not switching into the off-state. This is observed at RH of 90 % where the oscillation stops because the threshold voltage is too negative, and the EGFETs cannot be turned off anymore. [134]

The simulation result confirms that the ring oscillator stops to operate, due to the negative threshold voltage of the individual EGFETs (Figure 6.8). For simulation

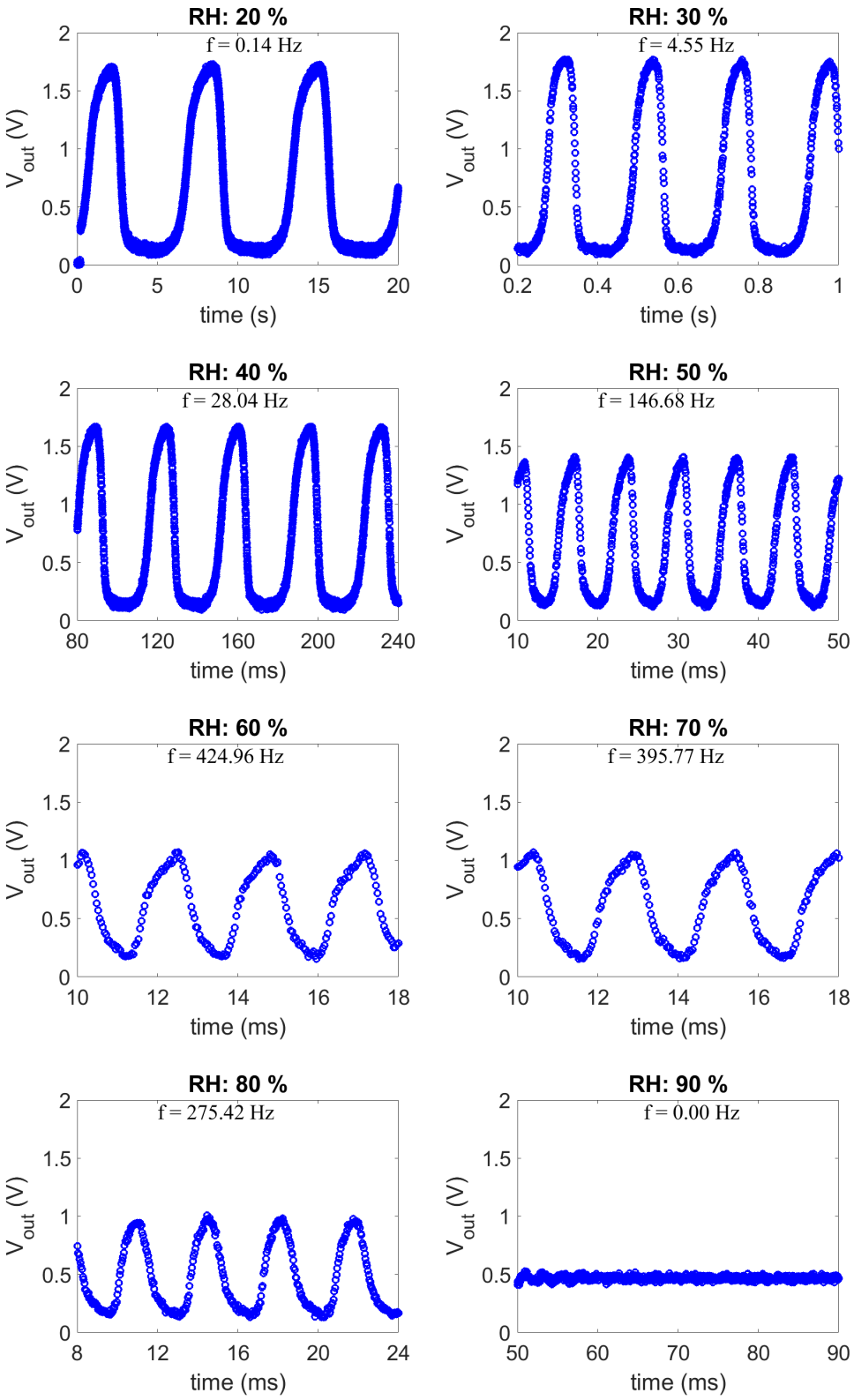


Figure 6.7.: Output curves of the ring oscillator at different relative humidity levels and a supply voltage of 2.0 V.

purpose, the ring oscillator schematic shown in Figure 5.11a is used and the values for the switching capacitance and switching resistance are chosen in accordance to Figure 6.1. Since the switching capacitance and switching resistance are dependent on the supply voltage, the respective capacitance and resistance values are changed manually in the simulation. In general, the TFTs in a circuit are designed within a threshold voltage margin and leaving this margin leads to failures.

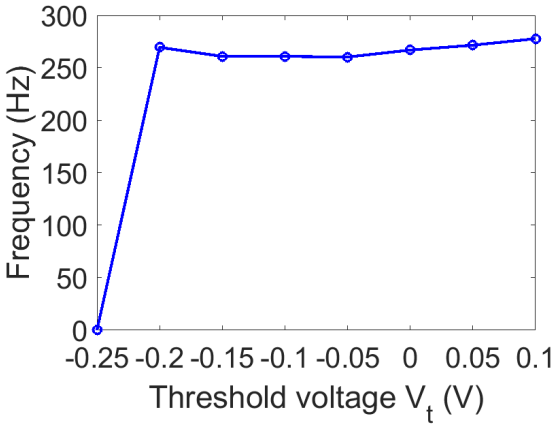


Figure 6.8.: Dependency of the threshold voltage on the oscillation frequency of a three-stage ring oscillator. Reprint with permission from [134] © 2019 IEEE

The influence of the humidity is an issue for the EGFET technology. In security applications, a circuit design within this EGFET technology is unreliable because of the humidity sensitivity. To overcome the issue of humidity sensitivity, encapsulation of the devices at a certain relative humidity (50 % - 60 %) is essential for preventing the absorption of H_2O molecules from the environment, and keeping the EGFETs at a well defined relative humidity level. Another approach is to change the components of the CSPE and develop an electrolyte that is not sensitive to humidity.

6.2. Performance assessment

As seen previously, the switching capacitance and the switching resistance need to be included to the output of a logic gate to enable transient simulations. This two elements provide the delay information to the circuit simulator. However, including the switching capacitance and the switching resistance to the simulation is misleading, because they are not physically present in the fabricated circuit. A further disadvantage is that a ring oscillator, must be characterized prior to the simulation. The simulation is meant as a tool for supporting circuit designers in developing new applications, and should always be performed before manufacturing the application.

Another approach to provide the delay information to the circuit simulator, is to include the terminal capacitances (gate-drain capacitance (C_{gd}) and gate-source capacitance (C_{gs})) to the DC transistor model. By adding the terminal capacitances, only the transistor is characterized to create a compact transistor model, compatible with transient

simulations. In addition, only physical present electrical elements are required in the schematic, used for the simulation.

In conventional silicon technology, the Meyer capacitance model is popular for describing the terminal capacitances. The Meyer capacitance model is based on the assumption that all charges in a metal-oxide semiconductor FET (MOSFET) are conserved. Thereby, the charges are attributed to the terminal capcitances: [160, 161]

$$\begin{aligned} C_{gd} &= \frac{\delta Q_g}{V_{gd}}, \\ C_{gs} &= \frac{\delta Q_g}{V_{gs}}, \end{aligned} \tag{6.1}$$

where V_{gd} is the potential between the gate-electrode and the drain-electrode. The total charge located at the gate-electrode (Q_g) is described, in the linear region, by: [161]

$$Q_g(V_{gs}, V_{gd}) = \frac{2}{3} C_g \frac{(V_{gd} - V_t)^3 - (V_{gs} - V_t)^3}{(V_{gd} - V_t)^2 - (V_{gs} - V_t)^2}. \tag{6.2}$$

In the saturation region, the total charge located at the gate-electrode is:

$$Q_g = \frac{2}{3} C_g (V_{gs} - V_t). \tag{6.3}$$

Therefore, in the linear regime, the terminal capacitancs are: [161]

$$\begin{aligned} C_{gd} &= \frac{2}{3} C_g \left(1 - \frac{(V_{gd} - V_t)^2}{((V_{gd} - V_t) + (V_{gs} - V_t))^2}\right), \\ C_{gs} &= \frac{2}{3} C_g \left(1 - \frac{(V_{gs} - V_t)^2}{((V_{gd} - V_t) + (V_{gs} - V_t))^2}\right). \end{aligned} \tag{6.4}$$

Whereas, in the saturation regime, the terminal capacitances change to: [161]

$$\begin{aligned} C_{gd} &= 0, \\ C_{gs} &= \frac{2}{3} C_g. \end{aligned} \tag{6.5}$$

By modifying the Meyer capacitance model, it is also applicable to EGFETs. Due to the ionic nature of the electrolyte, the overall EGFET capacitances are splited into intrinsic and extrinsic components. The extrinsic transistor capacitances are mostly formed by the overlap of the electrolyte with the metallic drain- and source-electrodes, and considered to be the source of the parasitics. On the other hand, the intrinsic transistor capacitances are formed due to the interaction of the electrolyte with the semiconductor. The extrinsic and intrinsic capacitances are in parallel to each other. For that reason, the extrinsic capacitance dominates the behavior of the total capacitance, since its value is larger compared to the intrinsic capacitance. [162]

To measure the extrinsic transistor capacitances, a de-embedding EGFET structure is used without printing the semiconductor between the drain- and source electrodes,

where only the overlap of the electrolyte with the ITO based drain- and source electrodes is considered (Figure 6.9). Following, an EGFET with the same W/L-ratio, as the de-embedding structure, and printed semiconductor is characterized (Figure 6.10). More important is that the width of the ITO metal lines must remain equal as for the de-embedding structure. The measurement of the ordinary EGFET contains the superposition of the extrinsic and intrinsic transistor capacitances. However, both structures are characterized in a similar way. The terminal capacitances are characterized by connecting the gate-electrode to the low input terminal of the LCR meter and the drain- or source-electrode to the high input terminal of the LCR meter. If the gate-drain capacitance is measured, then a AC signal with an amplitude of 10 mV and a frequency of 40 Hz is applied to the drain-electrode, while the source electrode is biased with a constant value. To obtain the gate-source capacitance, the AC signal is applied to the source-electrode and the constant voltage level to the drain-electrode. For a complete description of the transistor capacitances, also the gate-capacitance must be examined. Therefore, the gate-capacitance is measured by connecting the gate-electrode to the low input terminal of the LCR meter and the shorten drain- and source electrodes to the high terminal of the LCR meter. [162]

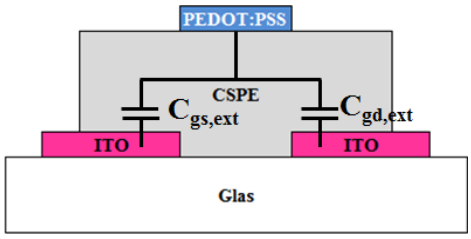


Figure 6.9.: Terminal capacitances of a EGFET.

In any case, the impedance value connected between the low and high terminals of the LCR meter is measured by the instrument. The imaginary part of the measured impedance ($Im(Z)$) is evaluated to estimate the capacitance value (C): [162]

$$C = \frac{1}{2\,\pi\,f\,Im(Z)}. \tag{6.6}$$

As discussed previously, for developing a Meyer capacitance like model, suitable for EGFETs, the capacitances of the de-embedding structure are characterized first. In this context, the extrinsic gate-capacitance is modeled through a linear function: [162]

$$C_{g,ext} = c_{g0} + c_{g1}\,V_{gs}, \tag{6.7}$$

where c_{g0} and c_{g1} are constants. Also, the extrinsic gate-drain capacitance ($C_{gd,ext}$) as well as the extrinsic gate-source capacitance ($C_{gs,ext}$) are measured on the same de-embedding structure and follow a linear relationship: [162]

$$\begin{aligned} C_{gd,ext} &= c_{gd0} + c_{gd1}\,(V_{gs} - V_{ds}), \\ C_{gs,ext} &= c_{gs0} + c_{gs1}\,V_{gs}, \end{aligned} \tag{6.8}$$

where c_{gd0}, c_{gd1}, c_{gs0} and c_{gs1} are empirical parameters.

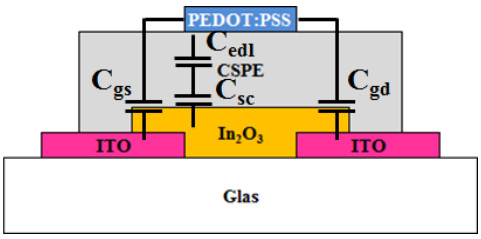


Figure 6.10.: Capacitances in a EGFET.

Next, the overall EGFET capacitances (including extrinsic and intrinsic sources) are measured on a EGFET structure with the same W/L-ratio as used for modeling the extrinsic capacitances (Figure 6.10). Hence, the overall gate-capacitance is the parallel connection between the extrinsic and intrinsic gate-capacitance, described by the following expression: [162]

$$C_g = C_{g,ext} + C_{g,int}, \tag{6.9}$$

The intrinsic gate-capacitance ($C_{g,int}$) is the series connection between the EDL capacitance (C_{edl}), resulting from establishing the double layer at the gate/electrolyte interface, and the space-charge capacitance, introduced by the interface between the electrolyte and the semiconductor (Figure 6.10): [162]

$$C_{g,int} = \frac{C_{sc}\, C_{edl}}{C_{sc} + C_{edl}}. \tag{6.10}$$

As soon as the potential at the gate-electrode reaches a certain onset voltage, the space-charge capacitance rises linearly with the gate-source voltage: [162]

$$C_{sc} = \begin{cases} 0 & V_g < V_0 \\ c_{sc0}\,(V_g - V_0) & V_g \geq V_0. \end{cases} \tag{6.11}$$

where c_{sc0} is an empirical parameter.

After obtaining the intrinsic gate-capacitance through Equation 6.9, the intrinsic gate-drain capacitance ($C_{gd,int}$) and the intrinsic gate-source capacitance ($C_{gs,int}$) are modeled in a similar manner as suggested by the Meyer capacitance model: [162]

$$\begin{aligned} C_{gd,int} &= \frac{2}{3}\, C_{g,int}\, K_d \left[1 - \left(\frac{V_{gte}}{2\,V_{gte} - V_{dse}}\right)^2\right], \\ C_{gs,int} &= \frac{2}{3}\, C_{g,int}\, K_s \left[1 - \left(\frac{V_{gte} - V_{dse}}{2\,V_{gte} - V_{dse}}\right)^2\right], \end{aligned} \tag{6.12}$$

where K_s is a fitting function, K_d is a constant, V_{gte} and V_{dse} are transition functions. The quadratic function K_s is defined as: [162]

$$K_s = q_{ks0} + q_{ks1}\, V_{gs} + q_{ks2}\, V_{gs}^2. \tag{6.13}$$

where q_{ks0}, q_{ks1} and q_{ks2} are empirical parameters. Different to the original Meyer capacitance model, the presented capacitance model requires only one equation to

describe the linear and saturation regions, which is achieved by using the transition functions in Equation 6.12: [162]

$$\begin{aligned} V_{gte} &= \frac{1}{2}\left(V_{ds} + (V_{gs} - V_t) - \sqrt{V_\delta + (V_{ds} - V_{gs} - V_t)^2}\right), \\ V_{dse} &= \delta_1 V_{ds}, \end{aligned} \tag{6.14}$$

where V_δ and δ_1 are constants. Also, the parameters K_d and K_s are not original from the Meyer capacitance model and need to be included because of the voltage dependency of the EDL.

The resulting schematic of the EGFET model is shown in Figure 6.12. As seen from Figure 6.12, the gate resistance (R_g) is included to the model, to describe the ion movement inside the electrolyte, as well as the resistance of the PEDOT:PSS. The gate resistance is an important parameter because it does not allow the terminal capacitances to charge instantaneous, as it is the case in a real capacitive system. However, the DC EGFET model, presented in Section 4.4, and described by the transistor symbol in Figure 6.11, is compatible with the capacitance model presented in this section. [162]

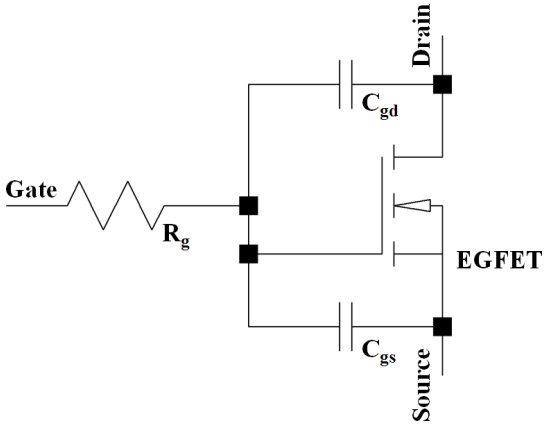


Figure 6.11.: Schematic of the EGFET capacitance model.

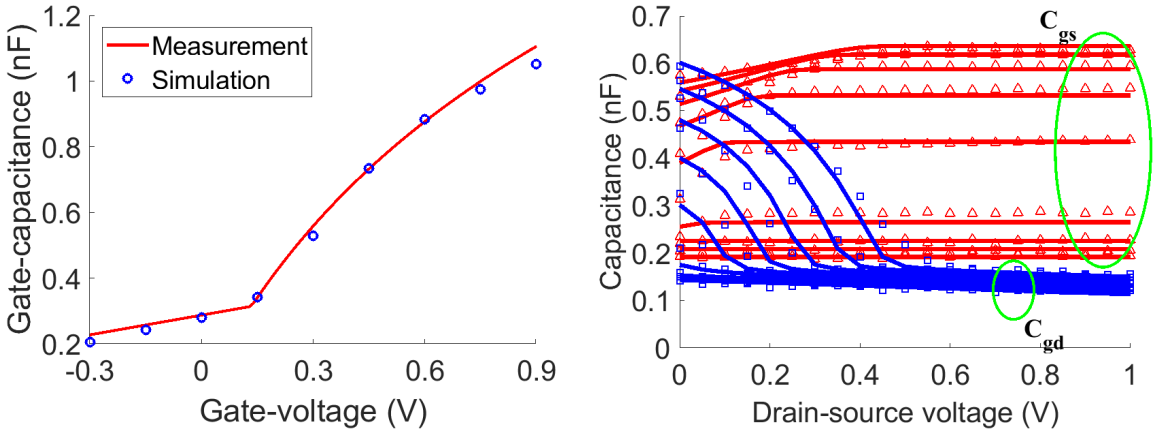
To demonstrate the accuracy of the capacitance model, the required model parameters are extracted from a EGFET with a W/L-ratio of 100 µm /60 µm, and summarized in Table 6.2. [162] However, the extraction of the gate resistance is demonstrated in the following paragraphs. Using the extracted parameters in combination with the above described capacitance model, an acceptable fit between measured and calculated data (Figure 6.12) is achieved for the gate-capacitance as well as the terminal capacitances.

The feasibility of the EGFET capacitance model for circuit simulation is elaborated on a three-stage ring oscillator, as shown in the schematic (Figure 6.13). By comparing Figure 6.13 with Figure 5.11a, it is notable that due the capacitance model, the switching capacitance and switching resistance are obsolete for performing simulations. The W/L-ratio of the EGFETs is 400 µm/40 µm and the resistance value for all resistors is 60 kΩ.

The value of the gate resistance is chosen in accordance to the measurement of the ring oscillator. Therefore, the supply voltage, of the ring oscillator, is varied and the

Table 6.2.: Extracted parameters used in the EGFET capacitance model.

Parameter	Value	Parameter	Value	Parameter	Value
c_{g0} (nF)	0.28	c_{gs1} (nFV^{-1})	0.15	c_{gd0} (nF)	0.16
c_{gd1} (nFV^{-1})	0.04	c_{gs0} (nF)	0.23	c_{gs1} (nFV^{-1})	0.08
c_{sc0} (nFV^{-1})	3.0	c_{edl} (nF)	3.2	V_0 (V)	0.118
K_d	0.92	q_{ks0}	2	q_{ksq1}	2.5
q_{ksq2}	-1.79	V_δ (V)	0.027	δ_1	0.62



(a) (b)

Figure 6.12.: (a) Gate-capacitance of an EGFET in dependence of the gate-source voltage. (b) Terminal capacitances (gate-source and gate-drain capacitance) of the EGFET in dependence of the drain-source voltage at different gate-source voltage levels (from -0.3 V to 0.9 V in 0.15 V steps). All solid curves are measurements and the dotted lines denote simulation results. [162]

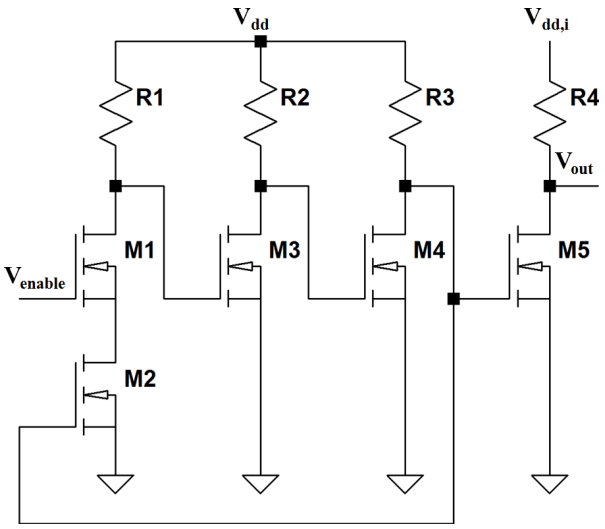


Figure 6.13.: Schematic of the three-stage ring oscillator used in the simulation. The EGFET terminal capacitances are combined with the DC EGFET model in the transistor symbol.

value of the gate resistance is changed until the measurement data matches with the simulation data. A cubic fit yields the expression for the gate resistance:

$$\frac{1}{R_g} = 7.71\ \mu\text{S} \cdot (-1.4 \cdot V_{dd}^3 + 5.1 \cdot V_{dd}^2 - 2.9 \cdot V_{dd} + 4.7), \tag{6.15}$$

where all parameters are found empirically. However, this approach, to describe the gate resistance, is not optimal because the circuit needs to be measured before the simulation is performed. In future, it is desirable to find a method to extract the value of the gate resistance directly from the EGFET characterization.

In the following, the measurement data of the three-stage ring oscillator is compared with the corresponding simulated data. Figure 6.14a shows that the oscillation frequency of the ring oscillator is predictable by simulation. Also, the quiescence current is captured very well by the simulation. However, the active current is around 20 µA higher in simulation than in the measurement (Figure 6.14b). The reason for the lower current

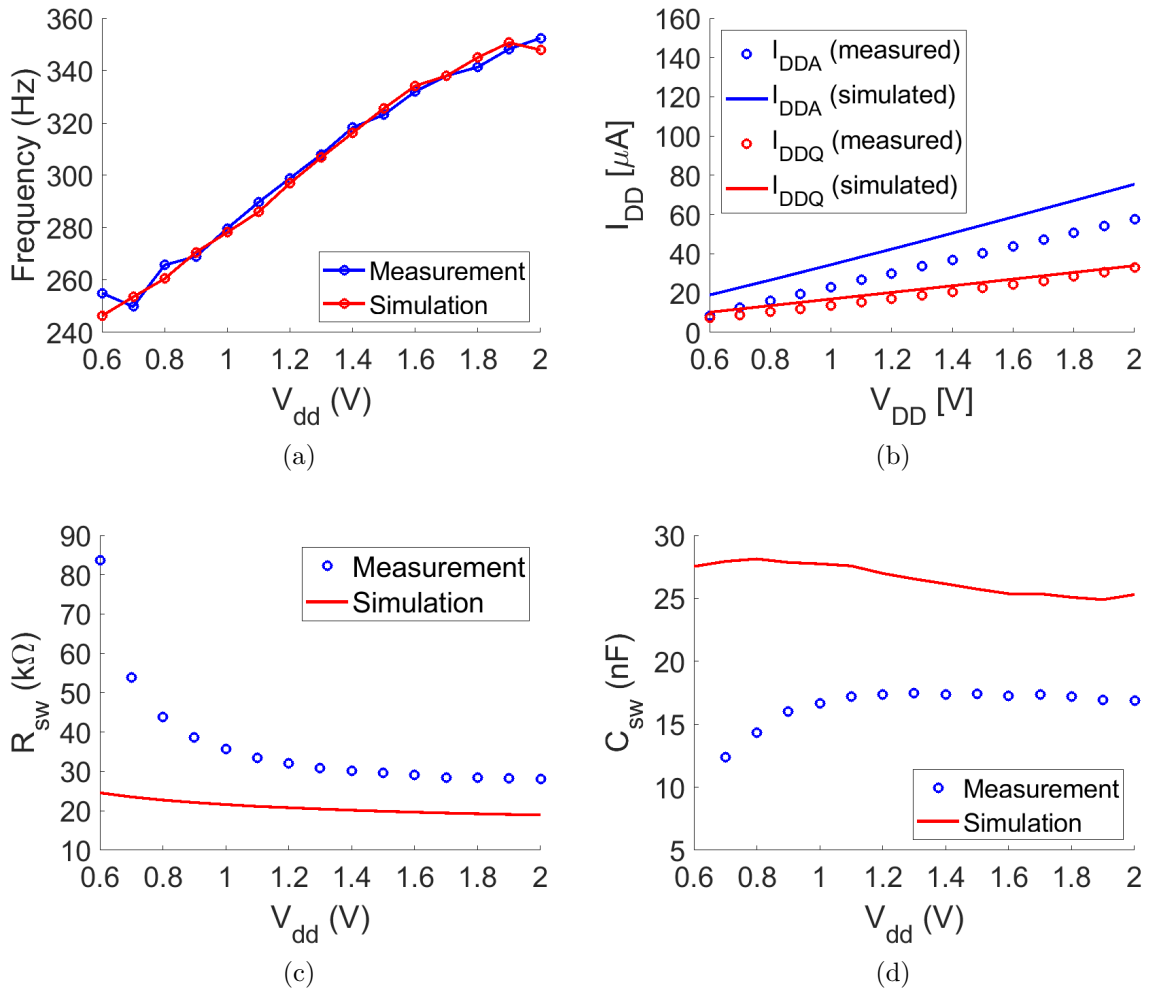


Figure 6.14.: Comparison of (a) the frequency, (b) the active and quiescence currents, (c) the switching resistance, as well as (d) the switching capacitance of a three-stage ring oscillator in measurement and simulation.

observed in the measurement lies in the fact that the conductivity of each EGFET is due to process variation different. The process variation affects also the pull-up resistance, leading to different resistance values in the measurement compared to the resistance value in the simulation. Consequently, in the simulation, the switching resistance (Figure 6.14c) is underestimated and the switching capacitance (Figure 6.14d) overestimated. However, the fact that the switching resistance and the switching capacitance are wrongly simulated can be ignored because this two parasitic elements are only required for simulation purpose and insignificant while using the capacitance model. More important is that the error in the simulation of the total power consumption is acceptable (Figure 6.15).

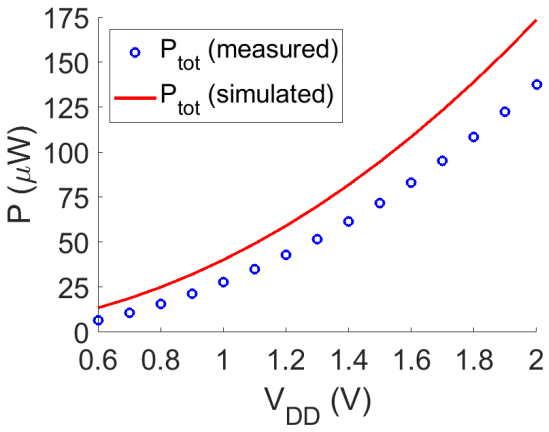


Figure 6.15.: Simulated and measured power consumption of a three-stage ring oscillator in dependency of the supply voltage.

The comparison between the measured and simulated ring oscillator frequency as well as the results for the power consumption clearly demonstrates that the proposed capacitance model is feasible for circuit simulation. Within the EGFET transistor technology, the capacitance model together with the expression for the gate resistance (Equation 6.15) are directly integrateable and without any change to simulate other structures than ring oscillators. Nevertheless, a routine to extract the gate resistance from a EGFET structure is highly desirable, to perform simulations without requiring the measurement data of the ring oscillator structure.

Part IV.

Summary, conclusions and outlook

7. Summary and conclusions

Printed electronics is a young research field compared to conventional microelectronics. A variety of interesting new applications are developed where printing approaches are more feasible, since the applications are directly printed on demand and at the required place. However, the aim of printed electronics is not to replace the well established silicon industry, but to complement existing technologies. Whenever a solution realized with silicon based approaches is too expensive, and high performance is not required, additive and maskless processing, as used in printed electronics, is an interesting alternative.

Up to now, a large number of materials, namely conductors, insulators, and semiconductors, have been developed to be used in a printing process for fabricating resistors, capacitors, solar cells, diodes and field-effect transistors. To overcome the low field-effect mobility of organic semiconductors, inorganic semiconductors are introduced in printed electronics. In particular, indium oxide can exceed field-mobility values of 100 $cm^2\,V^{-1}\,s^{-1}$ when inkjet printed. Unfortunately, p-type oxide semiconductors with comparable performance to their n-type counterparts are not available and applications are designed with only n-type field-effect transistors. On the other hand, a composite solid electrolyte (CSPE), used as the gate-insulator, is able to reduce the voltage requirements to values ~ 1.0 V. The reason for the low voltage requirements in the electrolyte-gating approach is that high gate-capacitance values of $\sim 5\ \mu F\,cm^{-2}$ are achievable.

In this thesis the electrolyte-gating approach is combined with the indium oxide channel in a top-gate transistor structure. This approach yields relatively high performance applications with low voltage requirements in the field of printed electronics. The electrolyte-gated field-effect transistors (EGFET) show excellent electrical characteristics, when printed through an inkjet printer. Interestingly, depending on the channel length, such EGFET can operate in enhancement and depletion mode. With a channel length of 10 µm a threshold voltage of -0.13 V and for a channel length of 60 µm a threshold voltage of around 0.10 V is achievable. In any case, the subthreshold slope is $\sim 80\ mV\,dec^{-1}$ and very close to the theoretical limit of $60\ mV\,dec^{-1}$.

The presented electrolyte-gated field effect transistor with indium oxide channel is used to design basic microelectronic logic circuits and standard cells. Due to the lack of high performance p-type oxide semiconductors, an inverter is designed within the transistor-resistor logic (TRL), where a resistor is used as the pull-up network and an electrolyte-gated field-effect transistor, operating in the enhancement mode, as the pull-down network. This inverter operates at a supply voltage of only 1.0 V, showing a signal gain of -5. The propagation delay time of the inverter is ~ 0.9 µs and consumes around 22 µW. A subsequently built three stage ring oscillator shows a frequency of 296 Hz at a supply voltage of 1.0 V and the frequency increases up to 311 Hz at a supply voltage of 1.3 V. However, the ring oscillator shows that within this transistor technology and design methodology, a minimum supply voltage of 0.6 V is achievable, outperforming organic based technologies.

In transistor-transistor logic (TTL), the pull-up transistor is replaced by an n-type transistor. Thereby, one option is to use an enhancement load EGFET in the pull-up network. In the transistor technology presented here, it is not possible to use designs with the enhancement load configuration, because the pull-up transistor needs to be sized in a way that it becomes very conductive, which would shift the threshold voltage to negative values. Another option is to configure the pull-up transistor as a depletion load, by using a depletion mode n-type EGFET. In terms of DC characteristics, the logic gates designed in TTL, with a depletion mode n-type EGFET, perform similar to the TRL designs. On the other hand, ring oscillator structures show that the TTL design is able to increase the operation frequency of circuits up to the kHz-regime.

Due to the pull-up EGFET, most of the TTL based designs dissipate a huge amount of power. The reason for the high power consumption lies in the fact that the driver capability of the EGFET is higher than for the resistor. Nevertheless, in designs were two EGFETs are connected in series, like NAND gates, the TTL design is able to reduce the power consumption by a factor of ~ 6. Therefore, in future, NAND gate designs, or circuit architectures that connect two EGFETs in series to the pull-down EGFET, might be a feasible approach to enhance the performance, and at the same time to reduce the power consumption of applications based on the presented transistor technology.

A disadvantage of EGFETs is that most of the electrolytes are sensitive to moisture. By increasing the relative humidity level, H_2O molecules get absorbed by the electrolyte, forming conductive pathways inside the electrolyte, allowing a faster establishment of the Helmholtz double layer. Mainly, the threshold voltage is reduced due to faster ion movement inside the CSPE. In a certain relative humidity level range (≤ 60 %) the performance of the ring oscillator gets improved because of the higher ion mobility. At higher relative humidity ranges (> 60 %), the additional introduced ions cause the frequency to drop because of an increased overall parasitic capacitance as well as charge carrier scattering due to the excessive amount of charge carriers at the surface of the semiconductor. At relative humidity around 90 %, the ring oscillator stops to oscillate because the shift of the EGFETs threshold voltage becomes too large.

The simulation confirms that the threshold voltage shift, caused by varying the humidity level, leads to a stop of the oscillation. For simulation purpose, a RC-network, namely the switching resistance and the switching capacitance, are included at the output of each logic gate, in the schematic used for the simulation. This RC-network provides the delay information to the simulator in transient analysis. Modeling the delay of the circuit by the switching resistance and the switching capacitance is an empirical approach that can be much improved by the inclusion of a verified capacitance model.

Therefore, the terminal capacitances (gate-source capacitance and gate-drain capacitance) are characterized and modeled. It turns out, that, with small modifications, the Meyer capacitance-model, which is also used for silicon devices, is able to predict the terminal capacitances of an EGFET. In a three-stage ring oscillator structure, where the terminal capacitance model replaces the RC-network approach, the simulation is able to predict the frequency behavior and the power consumption accurately.

In conclusion, EGFETs with indium oxide semiconductors, like indium oxide, open the door for interesting applications with low power and low to medium performance requirements in the field of printed electronics. For circuit design, TRL and TTL with depletion load configuration are feasible approaches. However, a trade off between

performance and power consumption needs to be made. For applications which require a high performance, the TTL with depletion load configuration is suggested. Conversely, the TRL is preferable for applications where the power consumption is a major design constraint.

The transistor technology presented here, in combination with the modeling approach, has the potential to pave the way for new, high performance and low voltage applications in the field of printed electronics.

8. Outlook

In the future, it is interesting to fabricate fully printed devices. In a fully printed device everything is printed, including the passive structures, which has the benefit of avoiding a vacuum process during fabrication. As fabrication strategy, the indium oxide film is printed and cured first. Following, the transistor electrodes are printed, where the drain- and source-electrodes are printed on top of the indium oxide film with a defined distance (channel length) to each other. The CSPE and the PEDOT:PSS top-gate are printed in sequential steps. Figure 8.1 depicts an all printed EGFET.

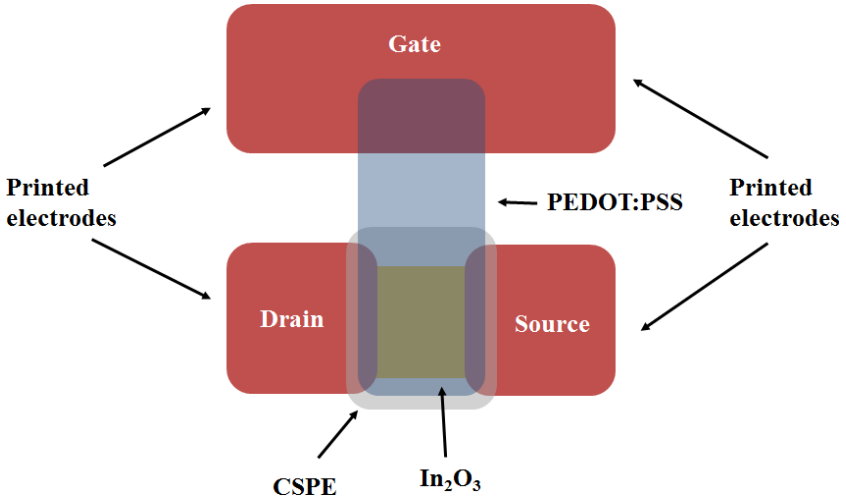


Figure 8.1.: Graphical representation of an all printed EGFET.

However, the choice of the material used for the passive structures is crucial because some metals like copper and silver react with the electrolyte, excluding themselves to be used as electrode materials in EGFETs. An alternative is graphene which is compatible with the CSPE. Measurements have already confirmed that all printed EGFET with graphene based passive structures are feasible. Unfortunately, the conductivity of graphene is several orders of magnitude lower than that of printed metal structures. [68] The low conductivity will significantly reduce the frequency of the printed applications. Therefore, graphene and the silver ink can be combined in a circuit in a way that all the drain-, source- and gate-electrodes are printed with graphene and the interconnects with silver. With this approach, the electrolyte is no longer in contact with the electrolyte, and the low conductivity of the graphene is compensated by the silver.

Also, the line width of the drain- and source-electrodes needs to be optimized. The CSPE provides a high gate-capacitance, but unfortunately when in contact with the drain- and source-electrodes, a large parasitic capacitance slows down the applications. Since the formation of a Helmholtz double layer is a surface effect, the parasitic capacitance is reduced by making the line width smaller. However, with decreasing the line width,

the overall series resistance increases, reducing the driver capability of the EGFET. Therefore, decreasing the speed of the applications. The optimal line width, and, as a result, an optimized ratio between series resistance and parasitic capacitance is essential.

As elaborated, the CSPE is sensitive to moisture since it absorbs H_2O molecules. This humidity dependency is problematic, especially for security applications, where the humidity changes the output of a circuit. One possible way to reduce the sensitivity of the CSPE is to encapsulate the devices at a certain humidity level. With encapsulating the device at a defined humidity level, it is possible to maintain a certain humidity level around the device, independent of the environment. Another approach is to change the components of the CSPE to make it insensitive to humidity. By replacing the CSPE with a so called ion gel, it is demonstrated that the devices are less sensitive to humidity. [163] Nevertheless, for reliable printing, the ion gel process requires to be improved.

In addition, the annealing temperatures of the indium oxide film is 400 °C, too high for conventional flexible substrates like plastic foils or paper. Some interesting techniques, like photonic curing or chemical curing approaches, are introduced to reduce the curing temperatures, even down to room temperature. The mentioned curing methods, unfortunately, drastically reduce the field-effect mobility value of the EGFET. It is suggested to further improve the choice of the parameters used in the room temperature process, to enter the very interesting field of all printed and flexible electronics without requiring expensive and special flexible substrates like kapton.

In standard microelectronic logic cells, designed in TTL with the depletion load configuration, the power consumption is very high compared to designs in TRL. The power consumption can likely be reduced by optimizing the W/L-ratios of the pull-up and pull-down EGFET, due to the high driver capability of the pull-up EGFET. By adjusting the channel geometry of the pull-up EGFET, the driver current is reduced. However, by using CMOS-like designs, the power consumption is reduced to a minimum and the performance of the circuits will most likely increase. Unfortunately, p-type EGFETs are not feasible within oxide electronics. In this regard, hybrid circuits with indium oxide EGFETs, in the pull-down network, and organic based EGFETs, in the pull-up network are interesting. This approach requires a lot of tuning and compensation because the organic EGFET needs to be able to drive a similar current as the indium oxide EGFET, at the same voltage level.

On the simulation side, by modeling the behavior of the terminal capacitances, circuits are fairly predictable without introducing any other elements, which are not physically presented in the real circuit, to the schematic. Unfortunately, the capacitance model is very sensitive to the gate-resistance. The gate-resistance is obtained by measuring a ring oscillator structure and fitting the resistance value to the measured frequency. Therefore, in future it is interesting to find a method to extract the gate-resistance directly from the measurement of an EGFET.

Achieving a hybrid design is an interesting challenge for future material scientists as well as engineers, and in combination with a feasible and reliable modeling approach it has the potential to bring the field of printed electronics to the next level.

Part V.

Index and references

Glossary

List of Abbreviations

AIM-SPICE Automatic Integrated Circuit Modeling SPICE.

AMOLED Active Matrix Organic Light Emitting Diode.

BG bottom gate.

CBM conduction band minimum.

CMOS complementary metal oxide semiconductor.

CSPE composite solide polymer electrolyte.

DC direct current.

EDL electronic double layer.

EGFET electrolyte-gated field-effect transistor.

EKV Enz-Krummenacher-Vittoz.

FET field-effect transistor.

HDL Helmotz double layer.

IOT internet of things.

IQR interquartile range.

LCD liquid crystal display.

MESFET metal-semiconductor FET.

MOSFET metal-oxide semiconductor FET.

OFET organic field-effect transistor.

PDK process design kit.

PE printed electronics.

RFID radio frequency identification.

RH relative humidity.

RT room temperature.

SNM signal to noise margin.

SPICE simulation program with integrated circuit emphasis.

TCAD technology computer aided design.

TCO transparent conducting oxide.

TFT thin film transistor.

TG top gate.

TRL transistor-resistor logic.

TSO transparent semiconducting oxide.

TTL transistor-transistor logic.

UMEM unified model and parameter extraction method.

VBM valence band maximum.

VRH variable range hopping.

VTC voltage transfer curve.

Chemical Compounds and Elements

$(CH_2OH)_2$ Ethylene glycol.

a-CuSnI compound of copper (I) iodide and tin (I) oxide.

Al_2O_3 aluminum oxide.

BTICN-EH dicyanomethylene 2-ethylhexyl.

$C_{22}H_{14}$ pentacene.

C_3H_6O acetone.

C_3H_8O 2-propanol.

$CuCrO_4$ copper chromate.

CuI copper (I) iodide.

CuO copper (II) oxide.

CuO_2 copper (I) oxide.

CuSCN cuprous thiocyanate.

DMSO dimethyl sulfoxide.

GaAs gallium arsenide.

H_2O water.

HfO_2 hafnium oxide.

In_2O_3 indium oxide.

$In(NO_3)_3 \times H_2O$ indium nitrate hydrate.

InGaO indium gallium oxide.

InGaZnO indium gallium zinc oxide.

InSnZnO indium tin zinc oxide.

InZnO indium zinc oxide.

ITO indium tin oxide.

$LiClO_4$ lithium perchlorate.

NiO nickel (II) oxide.

P3HT poly(3-hexylthiophene-2,5-diyl).

PC propylene carbonate.

PEDOT:PSS poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfonate.

PTFE polytetrafluoroethylene.

PVA poly(vinyl alcohol).

PVDF polyvinylidene difluoride.

$S_{c1}Z_{r1}O_x$ scandium zirconium oxide.

Si silicon.

SiO_2 silicon dioxide.

SiO_xN_y silicon oxynitride.

Sn:In_2O_3 indium doped tin oxide.

SnO tin (I) oxide.

SnO_2 tin (IV) oxide.

TiO_2 Titanium (IV) oxide.

Y_2O_x yttrium oxide.

ZnO zinc oxide.

ZnSnO zinc tin oxide.

ZrO_2 zirconium dioxide.

Physical Symbols

$\triangle$ Laplace operator.

λ channel length modulation parameter.

κ dielectric constant.

δ non-ideal factor of an EDL capacitor.

χ empirical parameter.

ϕ electrostatic potential.

γ power law parameter.

ϵ_0 electronic constant (8.854×10^{12} $\mathrm{F\,m^{-1}}$).

μ_{anion} mobility of the anions.

μ_{cation} mobility of the cations.

σ_{el} specific conductivity of the electrolyte.

τ_{el} Maxwell relaxation time.

τ_f fall time.

μ_{fet} field-effect mobility.

μ_{hall} hall mobility.

μ_n electron mobility.

μ_p hole mobility.

τ_p propagation delay time.

τ_{p01} low to high signal transition.

τ_{p10} high to low signal transition.

τ_r rise time.

A area.

B transition parameter.

C capacitance value.

C_0 voltage independent capacitance.

C_{edl} EDL capacitance.

$C_{el/sc}$ EDL capacitance at the electrolyte/semiconductor interface.

C_g gate-capacitance.

$C_{g,int}$ intrinsic gate-capacitance.

$C_{g/el}$ EDL capacitance at the gate/electrolyte interface.

C_{gd} gate-drain capacitance.

$C_{gd,ext}$ extrinsic gate-drain capacitance.

$C_{gd,int}$ intrinsic gate-drain capacitance.

C_{gs} gate-source capacitance.

$C_{gs,ext}$ extrinsic gate-source capacitance.

$C_{gs,int}$ intrinsic gate-source capacitance.

C_{sw} switching capacitance.

C_{tot} Area.

C_v voltage dependent capacitance.

D_n electron diffusion coefficient.

D_p hole diffusion coefficient.

E electrical field.

E_g band gap.

F force.

G generation rate.

I_{ab} accumulation current.

I_{above} above threshold current.

$I_{dd,a}$ active current.

$I_{dd,q}$ quiescence current.

I_{ds} drain-source current.

I_g gate-current.

I_{leak} leakage current.

I_{off} off-current.

I_{on} on-current.

I_{sat} saturation current.

I_{sub} subthreshold current.

I_{sw} switching current.

I_{total} total current.

J_n electron current density.

J_p hole current density.

L channel length.

N_A^- acceptor impurity concentration.

N_D^+ donor impurity concentration.

P_{dyn} dynamic power consumption.

P_{stat} static power consumption.

Q charge carrier density.

Q_g total charge located at the gate-electrode.

R recombination rate.

R_d drain series resistance.

R_{el} electrolyte resistance.

R_g gate resistance.

R_s source series resistance.

R_{sw} switching resistance.

S_l slope of the H-function.

T temperature.

V driving voltage.

V_0 onset voltage.

V_b transition voltage.

V_d drain voltage.

V_{dd} supply voltage.

V_{ds} drain-source voltage.

$V_{ds,sat}$ saturation voltage.

V_{enable} enable signal.

V_{gs} gate-source voltage.

V_{in} input voltage.

V_{out} output voltage.

V_s source voltage.

V_{ss} source supply.

V_{sub} subthreshold voltage.

V_t threshold voltage.

W channel width.

Z constant phase element.

Z_{tot} overall impedance of the electrolytic system.

$c_{b,0}$ bulk ion concentration.

f_t cut-off frequency.

g_{ch} channel conductance in the linear regime.

$g_{ch,i}$ intrinsic conductivity of the channel.

g_m transconductance.

k_B Boltzmann constant.

n_{anion} density of the anions.

n_{cation} density of the cations.

p_{At} density of trapped holes.

q elementary charge (1.602×10^{19} C).

z valency ion concentration.

List of Figures

List of Tables

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