Compact Modeling and Physical Design Automation of Inkjet-Printed Electronics Technology

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To my family

Work, work and work and we are bound to success

Muhammad Ali Jinnah
(Founder of Pakistan)

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Hiermit erkläre ich an Eides statt, dass ich die von mir vorgelegte Arbeit selbstständig verfasst habe, dass ich die verwendeten Quellen, Internet-Quellen und Hilfsmittel vollständig angegeben haben und dass ich die Stellen der Arbeit - einschlielich Tabellen, Karten und Abbildungen - die anderen Werken oder dem Internet im Wortlaut oder dem Sinn nach entnommen sind, auf jeden Fall unter Angabe der Quelle als Entlehnung kenntlich gemacht habe.

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Farhan Rasheed

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ABSTRACT

Trends like ubiquitous electronics require new forms of emerging electronics, many of them being flexible, wearable, transparent and customizable. Printed electronics (PE) holds many of these attributes and hence, is suitable for sensors, Internet of things, smart homes and soft robotics. There are a variety of PE technologies available which include gravure , flexographic, offset (lithographic), screen and inkjet printing. Some of these printing methodologies are based on additive manufacturing and some employ subtractive processes. The subtractive process include series of additive (deposition) and subtractive (etching) steps. It resembles the present-day silicon based processing but with larger feature sizes (several micrometers). In an additive process, only the depositions steps are involved. Printed layers are deposited layer-upon-layer to realize active devices, passive components, interconnects and crossovers. One such additive technology is the electrolyte-gated transistor (EGT) technology based on inorganic material. EGTs are developed by replacing the conventional dielectric with an electrolyte which enable them to operate at very low-voltages ($< 1V$) and making them a promising candidate for battery and energy harvester powered applications.

As most of the research and development focus of PE has been on materials, processes, and devices, hence, the standard design flow and electronic design automation (EDA) tools for inkjet-printed electronics technology are missing at large. Additionally, the EDA tools for very-large-scale integration (VLSI) technology need to be updated with printed electronics design and manufacturing constraints to support these technologies. Moreover, due to the lack of printed technologies specific design tools, a wide gap exists between circuit design and technology development making it further difficult for the wide adoption of the technology.

Besides the progress on improving the technology and fabrication process of the EGTs, having an accurate and versatile transistor models and design flow are the crucial initial steps to enable the design automation for this technology. The objective of this work is to develop models and a complete design automation flow for EGT technology. This work has multiple contributions in terms of compact models, placement and routing flow, standard cell library and Process Design Kit (PDK). The contributions of this thesis are:

Compact Modeling: The accurate description of transistor behavior in electronic design is not only crucial for modern VLSI technologies but even more relevant for emerging technologies such as printed electronics. Compact models are vital to optimize functionality and manufacturing yield, especially along the design chain from the single device to circuit simulations. A good model should be able to explain the characteristics of transistor in different operating regions of output and transfer curves by accurately capturing the 3-D behavior of drain–source current with respect to drain–source and gate–source voltages (V_{DS}–V_{GS}–I_{DS}). Additionally, as the process variation in printed electronics technologies is considerably high, a single segment and continuous model is vital for that purpose.

We propose an EGT model valid for all operating regions. This model is an extension of the Enz Krummenacher Vittoz (EKV) model, which is a well-known model for metal-oxide-semiconductor (MOS) transistors. The proposed single-segmented EGT model is more accurate compared with the state of the art, at the same time, it has less complexity. As a result, the

model has fewer parameters and it is much easier to incorporate the model into circuit simulation. Additionally, the EGT's DC model is extended to model the variabilities in the printed devices and circuits. The parameters of the DC model are extracted from the measurement data of the printed transistors. The distribution of model parameters are then estimated using a Gaussian Mixture Model (GMM). The model parameters from GMM are defined as statistical parameters to simulate and evaluate the effect of process variations on printed devices and circuits.

Placement and Routing Optimization: Unlike conventional silicon based technologies, inkjet-printed electronics technology is an additive manufacturing process where multiple layers are printed on top of each other to realize functional devices such as transistors and their interconnections. Due to the additive manufacturing process, the technology has limited routing layers. For routing of complex circuits, insulating crossovers are printed at the intersection of routing paths to isolate them. The crossover can alter the electrical properties of a circuit based on specific location on a routing path which leads to failure of the circuit.

We propose a crossover-aware placement and routing (COPnR) methodology for inkjet-printed circuits by integrating the crossover constraints in our design framework. Our proposed placement methodology is based on state-of-the-art evolutionary algorithm while the routing optimization is done using a genetic algorithm. The proposed methodology is compared with the industrial standard placement and routing (PnR) tools. On average, the proposed methodology has 38% fewer crossovers and 94% fewer number of failing paths compared to the industrial PnR tools applied to printed circuit designs.

Design Flows and Methodologies: With the development of technology and shorter design cycles time, printed circuits face various challenges related to the reliability and automation of design verification. Process Design Kit (PDK) plays an important role to overcome such challenges by providing a bridge between circuit designers and process technology.

We propose and develop a complete design flow for EGT technology. The PDK contains comprehensive set of data files including physical layers definition, parametrized cells (pcells), SPICE models, a standard cell library, platform for statistical circuit analysis, and rule deck for design rule check (DRC), layout-versus-schematic (LVS) and parasitic extraction (PEX). This flow is compatible with industrial standard Computer-Aided Design (CAD) and Electronic Design Automation (EDA) tools. This PDK can be used to design, simulate, verify and extract the layout of inkjet-printed circuits.

ZUSAMMENFASSUNG

Allgegenwärtiges Rechnen im Rahmen er „Internet der Dinge“ (IdD) erfordert neuartige Hardware-Ansätze, um elektronische Systeme zu realisieren die flexibel, tragbar, transparent und kunden-spezifisch sind. Diese Anforderungen könnten durch Printed Electronics (PE) (druckbare Elektronik) erfüllt werden, weshalb sie als neuartige Technologie im Bereich des IdD, Smart Homes, Soft Robotics und Sensoranwendungen potentiell eingesetzt werden kann. Es gibt verschiedene Herstellungsprozesse, um gedruckte Schaltungen zu realisieren, wie zum Beispiel Flexo- und Gravur Druck, Offsetdruck (lithographisch), Siebdruck und Tintenstrahldruck. Einige dieser Druckprozesse basieren auf additiven Herstellungsprozessen, andere hingegen auf subtraktiven Prozessen. Die subtraktiven Prozesse bestehen aus einer Serie von additiven (Deposition) und subtraktiven (Ätzen) Verfahren. Sie ähneln den heutigen Silizium-basierten Verfahren, jedoch mit viel geringeren Auflösungen (mehrere Mikrometer). In einem additiven Druckprozess, werden hauptsächlich Depositionen durchgeführt. Gedruckte Schichten werden Schicht für Schicht deponiert, um aktive und passive Komponenten als auch leitfähige Verbindungen oder Crossover zu realisieren. Elektrolyt-basierte Transistor-Technologie (EGT-Technologie) ist ein solcher Prozess, welcher auf anorganischen Materialien basiert. EGTs werden hergestellt durch Substitution von konventionellem Dielektrikum durch einen gedruckten Elektrolyten, welches sehr geringe Betriebsspannungen ermöglicht. Dadurch werden EGT-basierte Schaltungen in Batterie- und Energy-Harvester-betriebenen elektronischen Systemen bevorzugt eingesetzt.

Im Fokus der Entwicklung standen bisher eher Materialeigenschaften, Prozessoptimierungen und Realisierung von einzelnen druckbaren Komponenten, wohingegen die Erschließung von Standard Design Flows und elektronischen Design Automation (EDA) Tools für Tintenstrahldruckprozesse in PE vernachlässigt wurden. Zusätzlich müssen existierende EDA Tools für „Very Large Scale Integration“-Technologien (VLSI) um druckbare Designs und technologisch bedingten Herstellungseinschränkungen erweitert werden. Des Weiteren, durch den Mangel an PE-spezifischen Design Tools, besteht eine große Lücke zwischen Schaltungsentwurf und Technologieentwicklung, welche eine Adoption von PE erschweren.

Neben den Fortschritten bezüglich Technologie und Herstellungsprozessen von EGTs, sind jedoch auch genaue und vielseitig einsetzbare Transistor-Modelle und Design Flows unerlässlich, um Design-Automation in PE zu ermöglichen. Das Ziel dieser Arbeit ist die Entwicklung von Modellen und vollständigen Design-Automation Abläufen in der PE-Technologie. Diese Arbeit hat mehrere Beiträge bezüglich Compact Modelling, Placement and Routing Abläufen, Standardzellen-Bibliotheken und Process Design Kit (PDK).

Compact Modeling: Die genaue Beschreibung von Transistorverhalten in elektronischen Entwürfen ist nicht nur entscheidend für moderne VLSI-Technologien, sondern auch relevant für neu aufkommende Technologien wie druckbare Elektronik. Compact Models spielen eine bedeutende Rolle bei der Optimierung von Funktionalität und Produktionsausbeute, beginnend mit dem Entwurf von individuellen Komponenten bis zur Schaltungssimulation. Ein gutes Modell ist dadurch gekennzeichnet, dass es die Transistor-Charakteristiken in verschiedenen Betriebsmodi von Transfer- und Ausgangskennlinien durch 3-D-Verhalten von Drain-Source-Strömen in Abhängigkeit von Drain-Source und Gate-SourceSpannungen (VDS-VGS-IDS) akkurat beschreibt. Zusätzlich, da Prozessvariationen in PE-Technologien beträchtlich hoch sind, ist ein zusammenhängendes und kontinuierliches Modell für diesen Zweck vorteilhaft.

Wir schlagen ein EGT-Modell vor, welches in allen Betriebsmodi des Transistors gültig ist. Dieses Modell ist eine Erweiterung des Enz Krummenacher Vittoz (EKV)-Modell, bekannt für die Beschreibung von Metal-Oxide-Semiconductor (MOS) Transistoren. Das vorgeschlagene zusammenhängende (singlesegment) EGT-Modell ist genauer bezüglich existierender Ansätze des Stands der Dinge, und hat zur selben Zeit auch geringere Komplexität. Als Ergebnis benötigt das Modell weniger Parameter und lässt sich dadurch leichter in Schaltungs-Simulationen einbetten. Zusätzlich wurde das Gleichstrommodell des EGTs erweitert, um Variationen der gedruckten Komponenten und Schaltungen mit einzubinden. Die Parameter des Gleichstrommodells wurden aus Messdaten der gedruckten Transistoren extrahiert. Die Verteilung der Modell-Parameter wurde dann durch ein Gaussian-Mixture Model (GMM) geschätzt. Die Modell Parameter des GMM wurden als statistische Parameter definiert, um den Einfluss von ProzessVariationen auf gedruckte Komponenten und Schaltungen zu simulieren.

Placement and Routing Optimierung: Im Gegensatz zu konventionellen Silizium-basierten Technologien, basieren Tintenstrahl-gedruckte Technologien auf additiven Prozessen, in denen mehrere Schichten übereinander gedruckt werden, um funktionale Komponenten wie Transistoren und deren Verbindungen untereinander zu realisieren. Wegen des additiven Herstellungsprozesses hat diese Technologie jedoch Einschränkungen bezüglich der Routing-Schichten. Um Routing von komplexen Schaltungen zu ermöglichen, werden vereinzelte Crossovers gedruckt an Verbindungsknoten von Routing-Pfaden um solche elektrisch zu isolieren. Die Crossover haben jedoch Einfluss auf die elektrischen Eigenschaften einer Schaltung, abhängig von der Platzierung auf einem Routing-Pfad, welches zu Ausfällen der Schaltung führen kann.

Wir schlagen deshalb eine Place and Routing-Technik für Tintenstrahl-gedruckte Schaltungen vor, welche Crossover mit einbeziehen durch Integration solcher in unserem Design Framework. Unsere Placement-Technik basiert auf Stand-der-Dinge evolutionären Algorithmen, während die Optimierung durch einen genetischen Algorithmus realisiert wird. Die vorgeschlagene Technik wird mit industriellen Standard-Placement-And-Routing-Tools verglichen. Im Durchschnitt hat der vorgeschlagene Ansatz 38

Entwurfsabläufe und Methoden:: Durch die Weiterentwicklung von PE-Technologien, und den damit verbundenen geringeren Entwurfszeiten, entstehen neue Herausforderungen bezüglich der Zuverlässigkeit und Automatisierung der Entwurfsverifizierung. Process Design Kits (PDKs) sind hier von großer Bedeutung, da sie eine Brücke zwischen Designern und Prozess-Technologien herstellen.

Wir schlugen und entwickelten ein solches PDK für die EGT-Technologie vor. Das PDK enthält eine ausschöpfende Menge an Daten, welche Physical Layer Definition, Parameterized Cells (pcells), SPICE-Modelle, Standardzell-Bibliotheken, Plattformen für statistische Schaltungsanalyse, Design Rule Check (DRC), Layout-versus-schematic (LVS) und Parasitic Extraction (PEX) enthalten. Dieser Ansatz ist kompatibel zu industriellen Standard Computer-Aided-Design- (CAD) und Electronic Design Automation- (EDA) Tools. Das entwickelte PDK kann genutzt werden für Entwurf, Simulation, Verifikation und Layout-Extrahierung von Tintenstrahl-gedruckten Schaltungen.

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List of All Publications

1. **F. Rasheed**, M. S. Golanbari, G. C. Marques, M. Tahoori and J. Aghassi-Hagmann, (2018). "A smooth EKV-based DC model for accurate simulation of printed transistors and their process variations", IEEE Transactions on Electron Devices, 65(2), 667-673.

2. G. C. Marques, **F. Rasheed**, J. Aghassi-Hagmann and M.B. Tahoori, (2018, January). "From silicon to printed electronics: A coherent modeling and design flow approach based on printed electrolyte gated FETs", In 2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC) (pp. 658-663). IEEE.

3. X. Feng, G. C. Marques, **F. Rasheed**, M. B. Tahoori and J. Aghassi, "Analog Properties of Printed Electrolyte-Gated FETs based on Metal Oxide Semiconductors", in 59. MPC Workshop, IEEE German Section Solid-State Circuit Society, 2018 Germany. (Best Paper Award).

4. **F. Rasheed**, M. Hefenbrock, M. Beigl, M. Tahoori and J. Aghassi-Hagmann, (2018). "Variability modeling for printed inorganic electrolyte-gated transistors and circuits", IEEE Transactions on Electron Devices, 66(1), 146-152.

5. **F. Rasheed**, M. Hefenbrock, R. Bishnoi, M. Beigl, J. Aghassi-Hagmann and M.B. Tahoori, (2019, March). "Predictive Modeling and Design Automation of Inorganic Printed Electronics", In 2019 Design, Automation & Test in Europe Conference & Exhibition (DATE) (pp. 30-35). IEEE.

6. X. Feng, G. C. Marques, **F. Rasheed**, M. B. Tahoori, and J. Aghassi-Hagmann, (2019). "Nonquasi-Static Capacitance Modeling and Characterization for Printed Inorganic Electrolyte-Gated Transistors in Logic Gates", IEEE Transactions on Electron Devices, 66(12), 5272-5277.

7. **F. Rasheed**, M. Hefenbrock, R. Bishnoi, M. Beigl, J. Aghassi-Hagmann, and M. B Tahoori, (2020). "Crossover-aware Placement and Routing for Inkjet Printed Circuits", ACM Journal on Emerging Technologies in Computing Systems (JETC), 16(2), 1-22.

8. N. Bleier, M. H. Mubarik, **F. Rasheed**, J. Aghassi-Hagmann, M. B. Tahoori, and R. Kumar, "Printed microprocessors", In Proceedings of the 47th Annual International Symposium on Computer Architecture (ISCA). ACM, 2020.

9. A. T. Erozan, D. D. Weller, **F. Rasheed**, R. Bishnoi, J. Aghassi-Hagmann, M. B. Tahoori, (2020). "A Novel Printed Look-Up Table-Based Programmable Printed Digital Circuit", IEEE Transactions on Very Large Scale Integration (VLSI) Systems.

Glossary

AIC Akaike Information Criterion.

ASIC Application-Specific Integrated Circuit.

BIC Bayesian Information Criterion.

C-V Capacitance-Voltage Characteristics.

CMA-ES Covariance Matrix Adaptation Evolution Strategy.

CMOS Complementary Metal-Oxide-Semiconductor.

CNT Carbon Nanotube.

COPnR Crossover-Aware Placement and Routing.

DIBL Drain-Induced Barrier Lowering.

DRC Design Rule Check.

DRF Display Resource File.

EDA Electronic Design Automation.

EGT Electrolyte-Gated Transistor.

EKV Enz-Krummenacher-Vittoz.

EM Expectation Maximization.

GA Genetic Algorithm.

GMM Gaussian Mixture Model.

HCI Hot Carrier Injection.

HDL Hardware Description Language.

I-V Current-Voltage Characteristics.

IC Integrated Circuit.

IoT Internet of Things.

ITO Indium Tin Oxide.

LASSO Least Absolute Shrinkage and Selection Operator.

LMA Levenberg-Marquardt Algorithm.

LVS Layout Versus Schematic.

MC Monte Carlo.

MOS Metal-Oxide-Semiconductor.

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

OPC Optical Proximity Correction.

OTFT Organic Thin-Film Transistor.

PCB Printed Circuit Board.

pcell Parameterized Cell.

PDK Process Design Kit.

PE Printed Electronics.

PEX Parasitic Extraction.

PnR Placement and Routing.

PUF Physical Unclonable Function.

RFID Radio-Frequency Identification.

RRMSE Relative Root Mean-Squared Error.

RTL Register-Transfer Level.

SCL Standard Cell Library.

SOC System on a Chip.

SPICE Simulation Program with Integrated Circuit Emphasis.

TFT Thin-Film Transistor.

TR Transistor-Resistor.

TRNG True Random Number Generator.

VLSI Very-Large-Scale Integration.

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1 Introduction

The history of electronics is dated back to 19th century when J.A. Fleming invented vacuum diode in 1897 [10]. Later in 1906, vacuum triode was also implemented by Lee De Forest to amplify electrical signals [11]. Subsequently, the junction transistor was demonstrated in 1948 [12]. This was the starting point of advent of electronics. Everything started becoming digital and electronics industry saw a boom in research and invention [13, 14, 15]. Moreover, thanks to Moore's law that predicted well in advance the trend of the density of transistors per silicon chip which eventually improves the computing speed [16]. Overtime, whether it was personalized devices (like cell phones) or commercial devices (like computers/servers), every electronic products started getting better (in terms of functionality), compact and faster [17, 18]. On the other hand, with the advancement of technology, many new challenges are faced by the technology developers [19, 20, 21]. To overcome such challenges researchers focus on

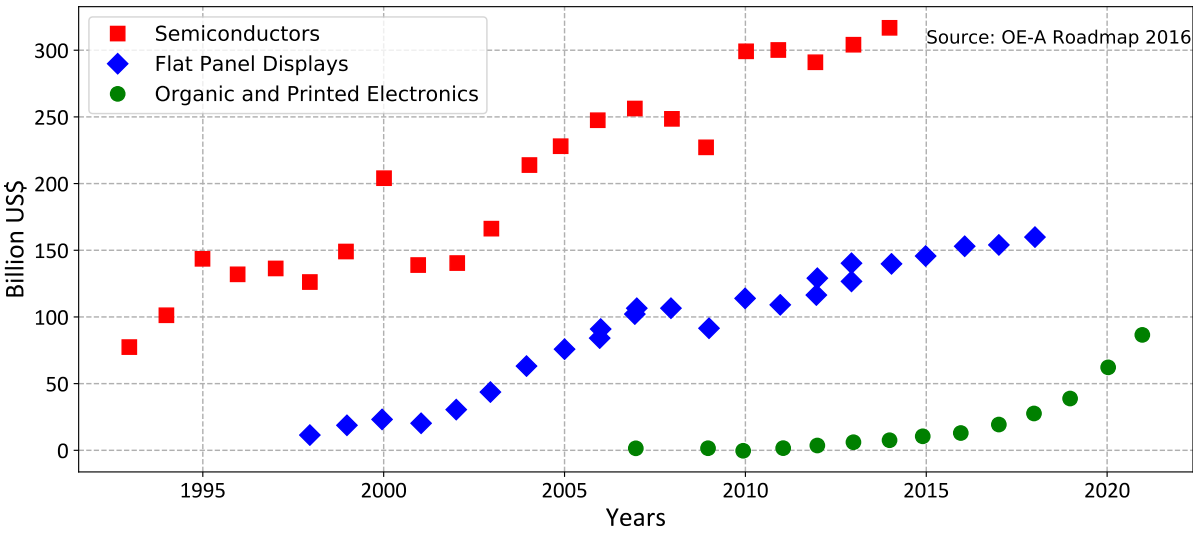


Figure 1.1: Multi-Billion US$ Market Enabled by New Technologies.

creative ideas to develop new form of electronics technologies (Nanosheet/FinFET transistor [22, 23], Spintronics [24], Printable/Flexible Electronics [25]) and architectural optimization (such as Neuromorphic [26] and Quantum computing [27]) to keep the semiconductor industry alive. All these solutions are necessary for technology advancement, device optimization, cost reduction and performance improvement.

In the recent years, consumer electronics market has reached to around 1800 billion US$ [28]. However, the semiconductor industry has not seen much improvement in the performance but the cost of operating the Integrated Circuits (IC) fabrication plants have reached to billion dollars [29]. Moreover, trends like ubiquitous electronics require new forms of emerging electronics, many of them being mechanically flexible, wearable, transparent, user-customizable and at the same time cost-effective. Unfortunately, for silicon based processes, where the fabrication cost is already in billion US dollars, adding further process to the design flow would surpass multi-billion US dollars to design such products which will eventually increase the end-product price [30, 31, 32]. So, for low cost processing and large-area applications, new technologies are re-

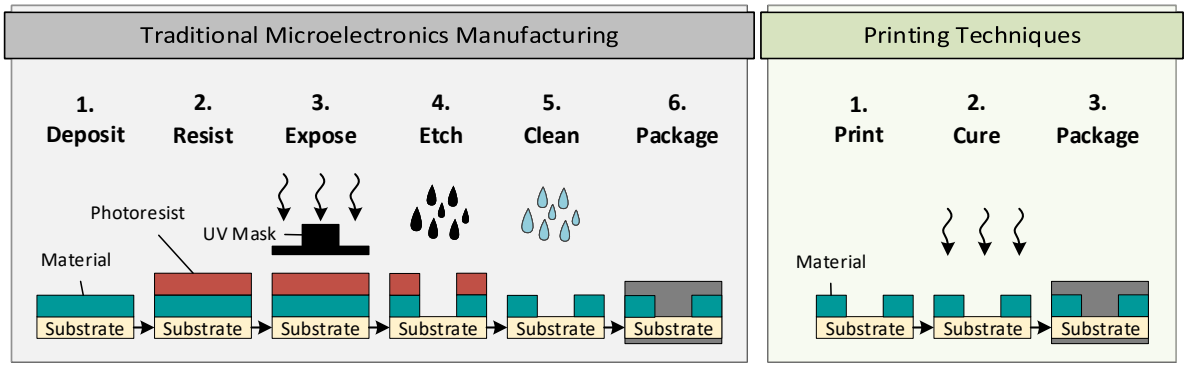


Figure 1.2: Comparison of traditional microelectronics and printing techniques process steps.

quired to cover the technological gaps associated with conventional silicon based processing techniques. Printed and Flexible electronics are becoming the prominent candidate for the next electronic revolution with a variety of technological benefits and low-cost processing with the market value crossed over 50 billion US$ in the last decade as shown in Figure 1.1.

Printed electronics (PE) is an all-encompassing term used to denote a set of emerging printing technologies which enable flexible, on demand, and low-cost fabrication process for electronic devices on various substrates. Which make these technologies suitable and very attractive for wearables, implantables, sensors, Radio-frequency identification (RFID), Internet of Things (IoT), smart homes and soft robotics [5, 33, 34, 35, 36]. Printing technologies are broadly divided into two categories. Some printing technologies are based on purely additive manufacturing process, while others employ subtractive process as well. Printable devices and circuits are realized by depositing multiple thin-films materials on substrates but the processing steps are much less compared to the silicon counterpart (see Figure 1.2). Printed electronics do not compete with silicon-based electronics in terms of integration density, area and performance. Typical frequencies achieved by printed circuits are in the range of few Hz to a few kHz [37, 38, 39]. Similarly, the feature size tends to be several microns. However, they meet the area and performance requirements for variety of applications [40, 41, 42, 43].

Though all printing techniques have similarities, inkjet-printed electronics is considered as more promising compared to others. It is a maskless, digital, low-cost, non-contact deposition method. Due to the additive nature of the technology, material can be deposited on the specified areas which, on one hand, reduces the material waste and on the other hand makes it more environment friendly technique compared to the subtractive process based technologies.

1.1 Motivation and objective

Despite all advantages of the printing technologies, they has some shortcomings which make it difficult in realization of reliable circuits and systems. For example, during material deposition in inkjet printing technologies, print head, ink and substrate interaction plays an important role to correctly print the thin-films. Several imperfections may appear including satellite drops, dispersion of ink on substrate and non-ejecting nozzles. Additionally, structure defects in amorphous organic polymers, interconnects corner rounding and printing inaccuracies also contribute to the process variability [44]. All such imperfections lead to variations in the electrical characteristics of the printed devices and circuits. Nevertheless, printed electronics technologies are constantly evolving with better materials, improved performance and modern printers [45, 46, 47, 48].

As most of the research and development focus of PE has been on materials, processes, and

devices [49, 50, 51], and much less work was related to printable circuits and systems [52]. Hence, the standard design flow and electronic design automation (EDA) tools for printed electronics technologies are missing at large. Additionally, the EDA tools for very-large-scale integration (VLSI) technologies need to be updated with printed electronics design and manufacturing constraints to support these technologies. Moreover, due to the lack of printed technologies specific design tools, a wide gap exists between circuit design and technology development making it further difficult for the wide adoption of the technology. Research on this area, with the help of heavily-researched silicon-based microelectronics knowledge, would help to bridge the gap between technology development and circuit design. Thus enabling the circuit designers to design circuits/systems without in-depth knowledge of the process technology.

To develop the design flow for any technology, Process Design Kit (PDK) with accurate and versatile models are the initial steps to enable the design automation. PDK contains the necessary information of the process technology to abstract the design from the manufacturing. The objective of this thesis is to develop a complete design kit for inkjet-printed electronics technology. This includes compact models of the printed devices, placement and routing optimization, standard cell library (SCL) and technology files for the PDK.

1.2 Contributions of this thesis

This work is part of the MERAGEM (Modellierung, Entwurf, Realisierung und Automatisierung von gedruckter Elektronik und ihren Materialien) Doctoral Program funded by the Ministry of Science, Research and Arts of the state of Baden-Württemberg, Germany [53]. The main objective of this research project is the optimization of printing materials, designing of printed circuits and their applications in sensory systems. In this project, the focus of this thesis is on the compact modeling and design automation of inkjet-printed electronics technology. The methodologies and tools in this thesis are proposed for the inkjet-printed electrolyte-gated transistor (EGT) technology with inorganic channel material. However, these methodologies are applicable to any similar additive printing technology. We address challenges in the design flow of printed electronics and improve it through the proposed design automation techniques. Our contributions for different steps of the design flow are shown in Figure 1.3. The main contributions are divided in to three categories: i) Compact modeling, ii) Placement and routing optimization, and iii) Design flows and methodologies.

1.2.1 Compact Modeling

The accurate description of transistor behavior in electronic design is not only crucial for modern VLSI technologies but even more relevant for emerging technologies such as printed electronics. Compact models are vital to optimize functionality and manufacturing yield, especially along the design chain from the single device to circuit simulations. A good model should be able to explain the characteristics of transistor in different operating regions of output and transfer characteristics by accurately capturing the 3D-behavior of drain–source current with respect to drain–source and gate–source voltages (V_{DS}–V_{GS}–I_{DS}). Additionally, as the process variation in printed electronics technologies is considerably high, a single segment and continuous model is vital for that purpose. Moreover, it is always challenging to simulate effects of process variations and closely reflect it in design automation tools. Unlike silicon-based process, in inkjet-printed electronics all devices are printed individually by multiple additive process steps, where each step can vary on its own. These process and systematic variations originating from the ink, substrate and manufacturing tools are random and cannot easily be explained.

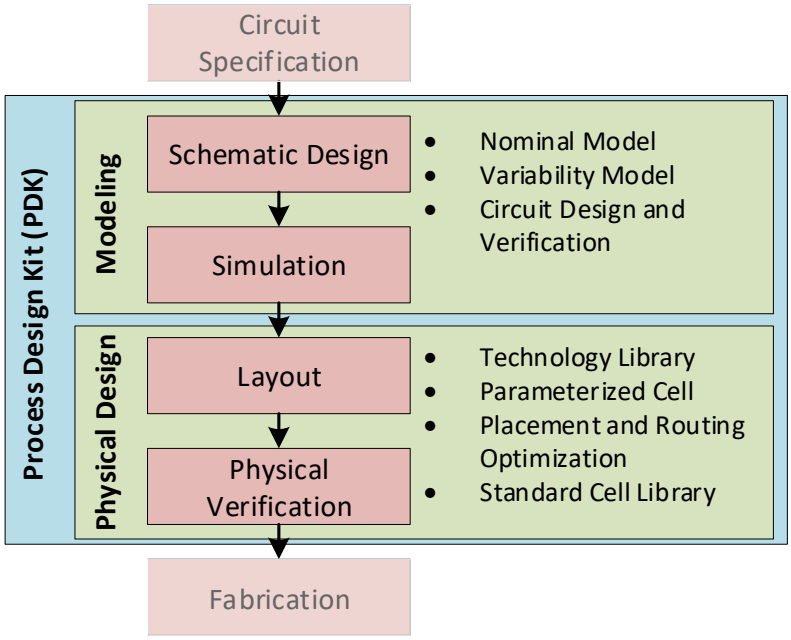


Figure 1.3: Contributions of this thesis for different steps of the design flow.

We propose a compact model valid for all operating regions of EGTs [54]. This model is an extension of the Enz Krummenacher Vittoz (EKV) model, which is a well-known model for metal-oxide-semiconductor (MOS) transistors. The proposed single-segmented EGT model is more accurate compared with the state of the art, at the same time, it has less complexity. As a result, the model has fewer parameters and it is much easier to incorporate the model into circuit simulation. Additionally, the EGT's DC model is extended to model the variabilities in the printed devices and circuits [55]. The parameters of the DC model are extracted from the measurement data of the printed transistors. The distribution of model parameters are then estimated using a Gaussian Mixture Model (GMM). The model parameters from GMM are defined as statistical parameters to simulate and evaluate the effect of process variations on printed devices and circuits.

1.2.2 Placement and Routing Optimization

Unlike conventional silicon based technologies, inkjet-printed electronics technology is an additive manufacturing process where multiple layers are printed on top of each other to realize functional devices such as transistors and their interconnections. Due to the additive manufacturing process, the technology has limited number of (e.g., two) metal layers for routing. One metal layer is typically used for routing and the other metal layer is used for making crossovers at the intersection of routing paths of different nets. For routing of complex circuits, insulating crossovers are printed at the intersection of routing paths to isolate them. The crossover can alter the electrical properties of a circuit based on specific location on a routing path which leads to failure of the circuit. Moreover, the number of crossovers scales with the complexity of the circuit which makes the crossover printing process very time consuming and error prone.

We propose a crossover-aware placement and routing (COPnR) methodology for inkjet-printed circuits by integrating the crossover constraints in our design framework [3, 56]. Our proposed placement methodology is based on state-of-the-art evolutionary algorithm while the routing optimization is done using a genetic algorithm. The proposed methodology is compared with the industrial standard placement and routing (PnR) tools. On average, the proposed

methodology has 38% fewer crossovers and 94% fewer number of failing paths compared to the industrial PnR tools applied to printed circuit designs.

1.2.3 Design Flows and Methodologies

With the development of technology and shorter design cycles time, printed circuits face various challenges related to the reliability and automation of design verification. Moreover, due to the technology-specific design constraints (manufacturing tools, additive/subtractive process), a common design flow cannot be followed for all printed electronics technologies. Process Design Kit (PDK) plays an important role to overcome such challenges by providing a bridge between circuit designers and process technology.

We propose and develop a complete PDK to enable the design flow for EGT technology. The PDK contains comprehensive set of data files including physical layers definition, parametrized cells (pcell), SPICE models [54, 55, 57], a standard cell library (SCL) [58], platform for statistical circuit analysis, and rule-deck for design rule check (DRC), layout-versus-schematic (LVS) and parasitic extraction (PEX). This flow is compatible with industrial standard Computer-Aided Design (CAD) and Electronic Design Automation (EDA) tools. The PDK is verified for variety of printed devices and circuits [37, 59, 60, 61, 62, 63]. This PDK and SCL can be used to design, synthesize, simulate, verify and extract the layout of EGT based inkjet-printed circuits.

1.3 Structure of this Thesis

The rest of the thesis is organized in five chapters:

- Chapter 2 provides an overview of printed electronics technologies. Especially, the technology and printing process of inkjet-printed electrolyte-gated transistor technology is discussed in detailed. The key variability sources in inkjet printing technologies are discussed in this chapter. Preliminaries on modeling and design automation as well as state-of-the-art in such domains are also discussed.

- Chapter 3 discusses the modeling methodologies for electrolyte-gated inkjet-printed transistors. There, the parameters extraction and compact model development is explained for printed transistors. Additionally, the process variability source and modeling approach for printed transistors is also discussed.

- Chapter 4 discusses the layout automation for printed electronics. We showed that the existing VLSI tools can be used for the placement and routing flow in additive printing technologies with sub-optimal results. We apply optimization methodologies in the placement and routing flow by integrating the technology specific constraints in the EDA tools.

- In Chapter 5, we discuss the key components required to enable the design flow for any emerging technology. Several components of the design kit, developed for the EGT technology, are discussed. The standard cell library characteristics, developed with the help of the measured EGT-based logic gates, are also discussed.

- Finally, Chapter 6 concludes the thesis and provides an outlook for future research direction in printed technologies and its application.

2 Background

Printed Electronics (PE) technologies attract a lot of attention due to their promising features including low-cost manufacturing, mask-less and on-demand printing on flexible substrates. This chapter presents an overall introduction about printed electronics technologies. Moreover, the inkjet-printed electronics and variability challenges in this technology are discussed. The electrolyte-gated transistor (EGT) technology is introduced and the device printing and characterization processes are discussed. Additionally, the background and the critical steps in design flow and EDA tools are also discussed. Finally, the state-of-the-art approaches in overcoming the challenges in inkjet printing technology are reviewed.

2.1 Printed Electronics: Overview

Printed Electronics (PE) is a term associated with printing technologies used to deposit thin-films of functional inks on a variety of substrates to realize electrical circuits through printed electrical components and interconnects. These technologies are also referred as Plastic Electronics, Organic Electronics or Bendable/Flexible Electronics. They have a variety of attributes of emerging electronics as it provides mechanical flexibility, low-cost process and on-demand fabrication [64]. These attributes make these technologies suitable for sensors, Internet of Things (IoT), Radio-frequency identification (RFID), smart homes and soft robotics [5, 33, 34, 35, 36]. There are multiple PE technologies available which include gravure , flexo-

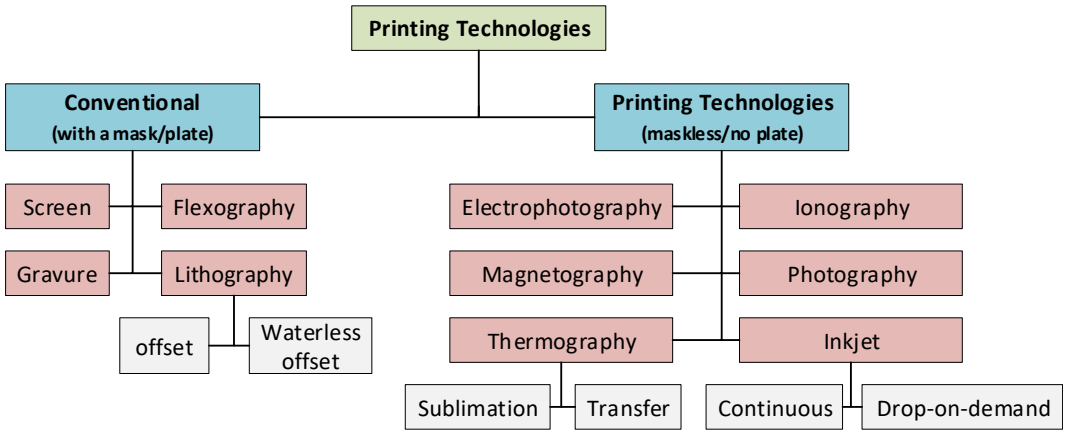


Figure 2.1: Printing Technologies Classification[4]

graphic, offset (lithographic), screen and inkjet printing (see Figure 2.1). Some of these printing methodologies are based on additive manufacturing and some employ subtractive processes [52]. The subtractive process (including laser ablation and photolithography) include series of additive (deposition) and subtracting (etching) steps. It resembles the present-day silicon-based processing but with larger feature sizes (several micrometers compared to nanometers in silicon). The subtractive process involves highly specialized processing and require expensive equipments and infrastructure. Additionally, due to the use of corrosive chemicals for etching, subtractive process is not on demand, has high costs due to the wastage of material and is

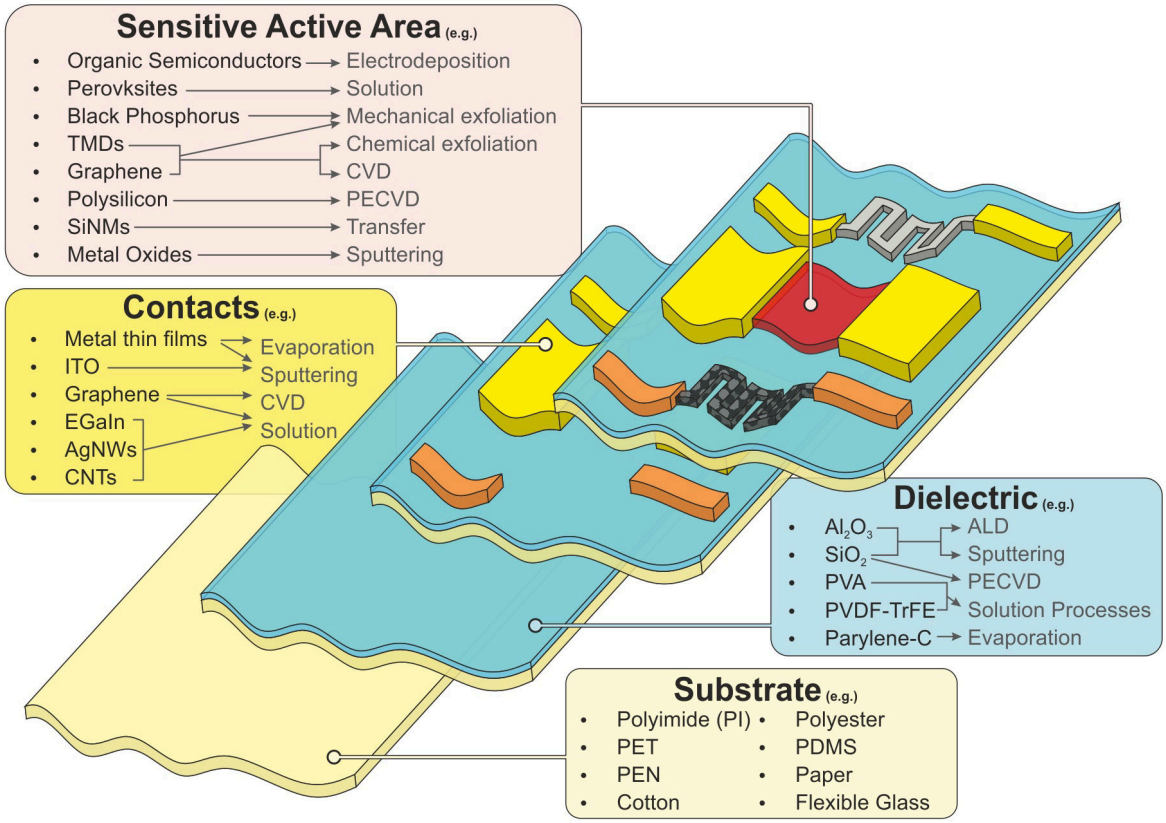


Figure 2.2: Common materials and printing/fabrication methods used for manufacturing flexible sensors [5].

not an environmental friendly technology. Contrary, in an additive process, only the depositions steps are involved. Printed layers are deposited layer-upon-layer to realize active devices [65, 66, 67, 68], passive components [69], interconnects [70, 71] and crossovers [72, 56]. In comparison with the subtractive-based printed electronics, fully-additive printed electronics have low carrier mobility and are limited to applications that require low-to-medium speed operation [73].

Nevertheless, the interest in printed technologies has been increased as they can be used for the deposition of functional materials for a variety of devices. Conductive structures have been printed on flexible, rigid and stretchable materials and can be used for wiring, resistors, capacitors, antennas and electrodes [74, 75]. RFID antennas and other contact-less communication applications have been realized [76, 77]. Several complex and fully-printed components including solar cells, diodes and field-effect transistors are also reported in the literature [75, 78]. Batteries and energy harvesters based on printed technologies are also reported [79, 80, 81]. A variety of sensors can be found in the literature and on the market already [82, 83]. All such components can be used to realize complex intelligent systems such as smart cards [78], wearable devices [84], smart textiles [85], environmental sensors [41] and displays [86]. Figure 2.2 shows an example of common materials and fabrication methods used to realize flexible sensors.

The common characteristics of different printing technologies are compared in Table 2.1. The printing resolution refers to the minimum feature size that can be realized with the technology. Printing thickness is the thickness of the materials deposited on the substrate. The printing speed defines the material deposition time on a particular substrate, which is in the range

Table 2.1: Comparison of Printing Techniques. The table is adapted from [1].

Parameter	Gravure	Offset	Flexographic	Screen	Inkjet	Microcontact & Nanoimprint	Transfer
Print Resolution [µm]	50-200	20-50	30-80	30-100	15-100	1-20	4-50
Print Thickness [µm]	0.02-12	0.6-2	0.17-8	3-30	0.01-0.5	0.18-0.7	0.23-2.5
Print Speed [m/min]	8-100	0.6-15	5-180	0.6-100	0.01-5	0.006-0.6	N/A
Solution Viscosity [Pa. S]	0.01-1.1	5-2	0.01-0.5	0.5-5	0.001-0.1	0.1	N/A
Material Wastage	Yes	Yes	Yes	Yes	No	Yes	No
Technique	Contact	Contact	Contact	Contact	Contactless	Contact	Contact
Printing area	Large	Large	Large	Medium	Large	Medium	Medium

of minutes. All printing techniques have material wastage during the printing process except inkjet and transfer printing methodologies. Solution viscosity is the viscosity of the ink and pastes that are compatible with the printing techniques. The technique and printing area refers to the material deposition method (contact/contactless) and substrate requirement for the applications, respectively.

Even though all printed technologies provide a variety of advantages still inkjet-printed electronics is of special interest due to its unique features such as mask-less, low-cost and non-contact deposition methods. The focus of this thesis is on inkjet-printed electronics technology, but the developed tools and concepts can also be applied to other additive technologies for PE. The detailed introduction of the inkjet-printed electronics technology is given in the next section.

2.2 Inkjet-Printed Electronics

Inkjet printing technology has gained a lot of interest and attention due to its unique feature of depositing functional inks through digital printing. The inkjet printable functional inks have enabled manufacturing of RFID tags, displays, thin-film transistors and variety of sensors [87]. Based on their electrical properties, these inks can be divided into three categories: dielectrical, semiconductive and conductive inks.

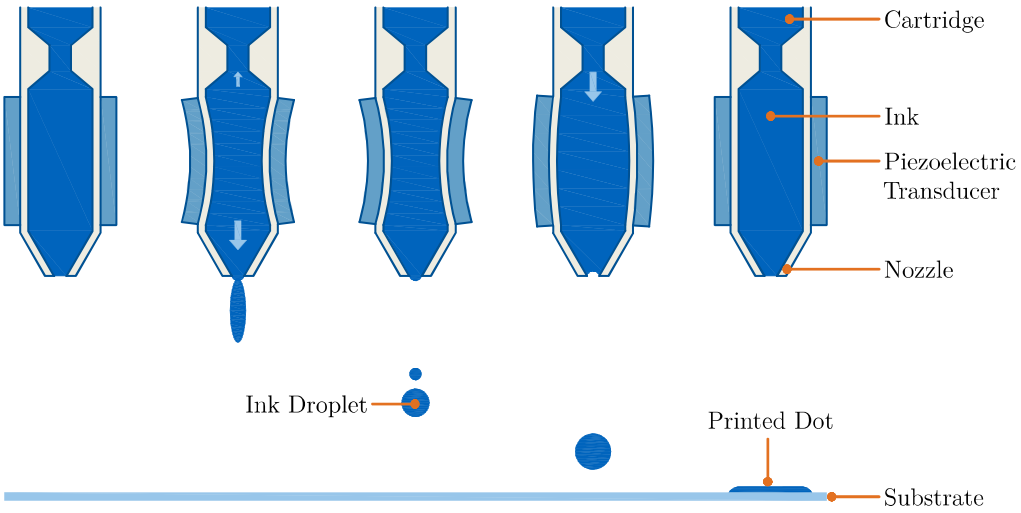


Figure 2.3: Drop-on-demand print head during printing process [6]

Inkjet printing technology is a digital printing technology as it does not require patterning of plates and masks. The inks are loaded in the print head and an electronic controller is used to eject a certain amount of ink on the substrate. Depending on the type of print head it can have one to several ten thousand nozzles. The print head may move once or multiple times over the same pattern to increase its thickness. A print head consist of an ink cartridge, filtering unit, nozzles and the actuation unit. During printing, the actuation unit is enabled to shrink the cartridge which ejects the ink out of the nozzle. If no droplets are required then the actuation unit is disabled and the print head remains inactive. This unique feature in inkjet printing technology is called drop-on-demand printing. The schematic of the piezo-electric drop-on-demand print head during printing process is shown in Figure 2.3. The ink formation on the surface of the substrate is determined by the volume and speed of the droplet, as well as the viscosity of the ink and its surface energies with respect to the substrate.

The key feature of inkjet printing is the on-demand printing that allows to control printed pattern and each pattern can be different from the previous one while providing an overall control over the process. This makes inkjet printing technology a low-cost process. This technique can significantly reduce the design cycles time required from the idea to proof-of-concept demonstration at the laboratory stage. For this reason this technology has gained a lot of interest and increasing research in developing processes, devices and applications using all inkjet-printed and hybrid approaches [88]. Especially in the academic field, inkjet printing technique has been used to realize antennas, organic light-emitting diodes (OLED), photovoltaics, thin film transistors (TFT), and sensors [87, 89, 90]. However, there are some challenges associated with this technology. The intrinsic characteristics of the functional material inks lead to different constraints and challenges while printing them on the substrate. Inkjet in comparison to flexography, spin coated and gravure printing generally results in rougher and far less uniform morphology which increases variability in printed devices and also deteriorate their performance. Additionally, proper ejection of droplets on the desired substrate area and with an acceptable quality of printed structures is challenging due to the influence of the evaporation rates of the solvents as well as spreading of the solution on the substrate. Misfiring, clogging, bulging of lines are the other key challenges associated with this technology. All these effects are the key sources of variation of printed devices and circuits. These effects are crucial for the production yield of printed circuits and should be accounted in the design flow. The typical variability sources in inkjet-printed technology are discussed in the next section.

2.2.1 Variability Sources

Variations in any technology can be broadly classified into spatial and temporal variations. Spatial variations are permanent variations and are responsible for the process variations. Unlike silicon based technologies, where the fabrication process is much better controlled through photolithography based process, printing technologies process involves multiple mechanical processes leading to mechanical vibrations. These vibrations cause printing inaccuracies including variations in film-thickness and dimensions. Additionally, the interfaces between the deposited layers (e.g., semiconductor and dielectric interface) also contribute to the process variations. On the other hand, temporal variations are mostly caused by the bias stress effects and hot carrier injection (HCI). Bias stress effect occurs when a transistor current is degraded when it is used for a longer time period. The continuous bias causes the structural defects in the semiconductor layer which reduces the field-effect mobility. In HCI phenomenon, the charge carriers get enough energy to inject into the gate dielectric leading to permanent shift in the threshold voltage of the transistor.

In inkjet-printed electronics (or any similar additive) technology, the performance of the printed components and interconnects is dependent on the quality of the printed thin-films.

However, the film quality is dependent on variety of features ranging from the ink composition to the substrate type. The fluid dynamics parameters of the functional inks such as viscosity and surface tension should be in a suitable limit for the effective printing process. The printing system works well when the ink, print head and substrate are compatible and ink-substrate interaction is optimized. The key characteristics and the associated challenges of the functional inks are discussed in this section.

Coffee Ring Effect

When the ink is deposited on the substrate, the ink drop starts drying, moving most of the ink particles at the periphery of the drop, forming a ring-like structure called coffee ring effect. This happens due to higher evaporation at the outer edges of the drop which causes an outward convectional flow towards the edges and accumulating solute at the periphery (Figure 2.4a). This effect changes the thickness of the printed materials causing thin layer from the center and thick layers at the periphery. It is more sever for a printed component as the thin layer can be punctured resulting in a non-functional device. Figure 2.4c shows an example of a coffee ring effect on a transistor's dielectric layer resulting in a high gate-leakage current.

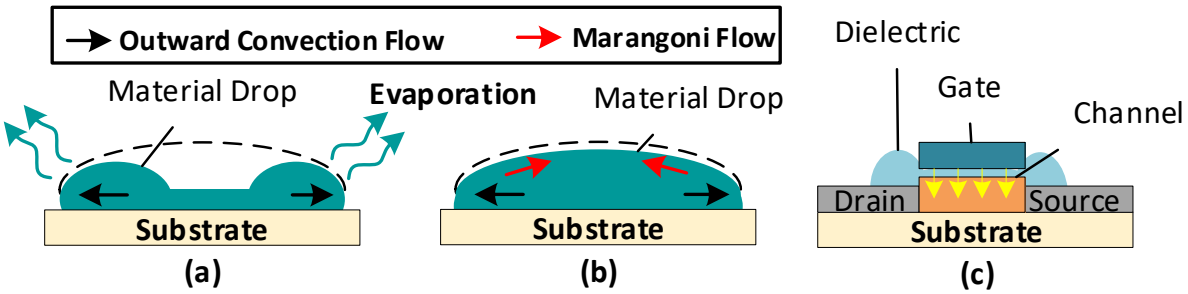


Figure 2.4: Drop drying process after deposited from inkjet printer. (a) formation of coffee ring (b) coffee ring suppressed by Marangoni flow [7] (c) cross-section view of a transistor showing coffee ring effect on dielectric layer. Thinning of the dielectric increases gate leakage current represented by the yellow arrows (↓)

For any printing technology, overcoming such nature of the matter is essential. The evaporation of drops is non-linear and complex. Thus, it is challenging to control the capillary flow of the solute particles. Researchers have found multiple ways to mitigate the coffee ring effect by manipulating the capillary flow. One such method suggests controlling the surface tension of the solvents in the ink. As the surface tension is dependent on the temperature and chemical composition of the ink, changing temperature at different parts of the drop (through substrate heating) develops a surface tension gradient. This allows the particles flow from a lower surface tension region to a higher surface tension region within the drop resulting in the appearance of the Marangoni effect [91] (Figure 2.4b). Additionally, the shape of the solute particles can also help to reduce the coffee ring effect [92]. Isotropically shaped particles are susceptible to the coffee ring effect. However, during evaporation for the anisotropic shaped particles, the deformed interfaces produce a strong interparticle capillary interaction. Which results in the uniform dispersion of the particles on the substrate.

Drop Coalescence

Drops are used for printing of lines and 2D patterns where the interaction between drops plays an important role in determining the morphology of deposited functional materials. Deposition morphology of the solution-processed functional ink colloidal drops is crucial for inkjet and

gravure printed electronics applications. With the availability of a variety of organic and inorganic material inks, the challenge is to effectively assemble the nano-particle inks into useful structures mitigating the drop coalescence. The process of drop coalescence takes place in three stages. The initial stage starts when the edges of the two droplets make contact and form a thick liquid bridge. In the second stage, the contact point of the drops begins to move, causing wetting on one side while dewetting on the other side. In the final stage, the combined drop relaxed toward a spherical cap which is the minimum surface energy configuration.

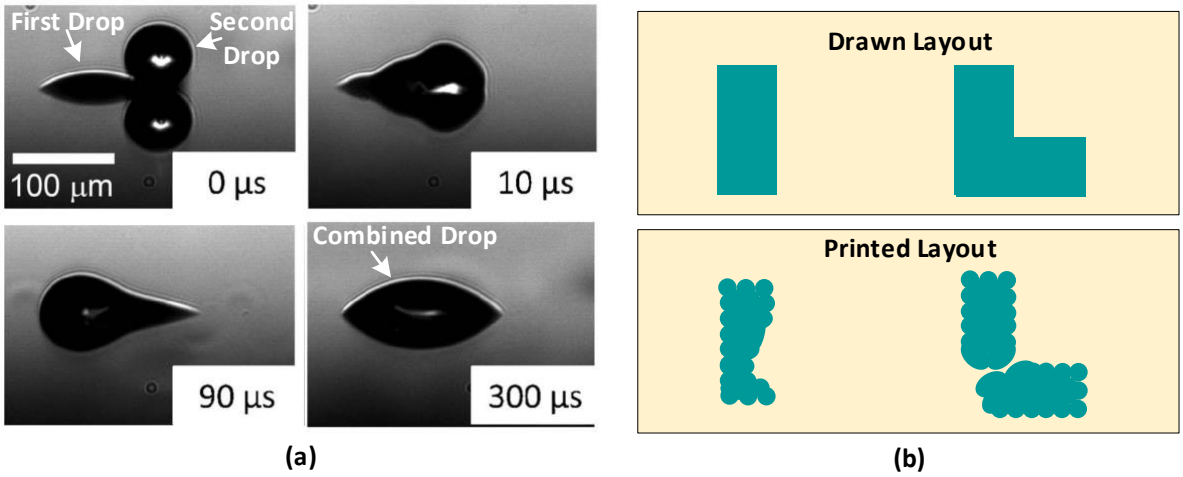


Figure 2.5: (a) Side-view images showing the impact of two consecutively printed drops [8] and (b) drawn layout of "I" and "L" shape structure and effect of drop coalescence on the printed layout

Figure 2.5a shows the side-view images for the coalescence of two consecutively printed drops on a glass substrate. It can be seen that the second drop (right) came into the contact of the first drop (left) within 10 µs. The combined drops spread due to inertia, viscous stress and surface tension. At t= 300 µs surface energies are minimized and the combined drop becomes stable. For printed structures, drop coalescence can alter the shape of the printed design with a reduced shape width or an incomplete structure (see Figure 2.5c). This would result in a reduced electrical performance of the printed components. In case of the conductive structure/path, the former condition results in a reduced conductivity while latter is more severe as it leads to non-conductive path.

Nozzle Issues

The functional materials are deposited by an inkjet printing process, where jetting is controlled by a CAD software, which describes the printed patterns in a digital format. Each pixel in the digital CAD file represents individual drops and slight variability in the drop flight from nozzle to substrate would change the intended structure layout. For example, contamination or air inside the nozzle would force the ink drop to eject at a different angle. This will cause the printed droplet to be slightly off to the intended printing spot. Additionally, the contaminated or clogged nozzles can also block the ejection of drops. Due to these non-jetting nozzles, the layout structure would not be completely printed. Drop ejection velocity is another important parameter that should be adjusted for all nozzles that are used in the printing process. It directly influences the overall printing quality and line fidelity. All mentioned nozzles issues are demonstrated in Figure 2.6.

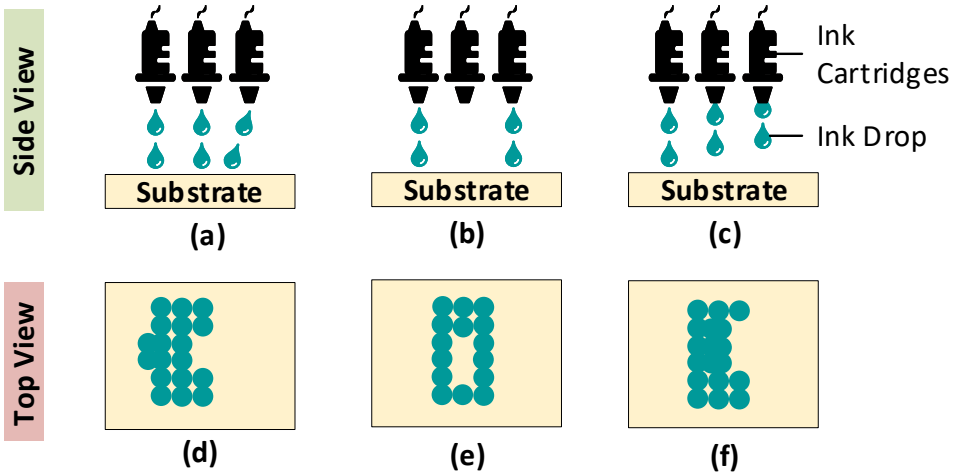


Figure 2.6: Nozzle issues: (a) misdirected drops (b) non-jetting nozzles (c) non-matched velocities. (d), (e) and (f) represent the effect on printing pattern due to misdirected drops, non-jetting nozzles, and non-matched velocities, respectively

2.2.2 Electrolyte-Gated Transistor Technology

State-of-the-art inkjet-printed field effect transistors (FETs) are realized using organic materials [78]. These organic FETs (OFETs) have organic semiconductor materials as a channel printed between the source and drain electrodes [93]. The gate dielectric is printed on top of the channel and then the top gate material. In organic technologies, circuits are based on p-type transistors as n-type OFETs are rare and have much lower performance compared to the p-type [94]. The OFETs have low field-effect mobility [95] and the typical supply voltage is higher than 5 V. The high supply voltage requirements make such technologies less attractive for low-power printed electronics applications.

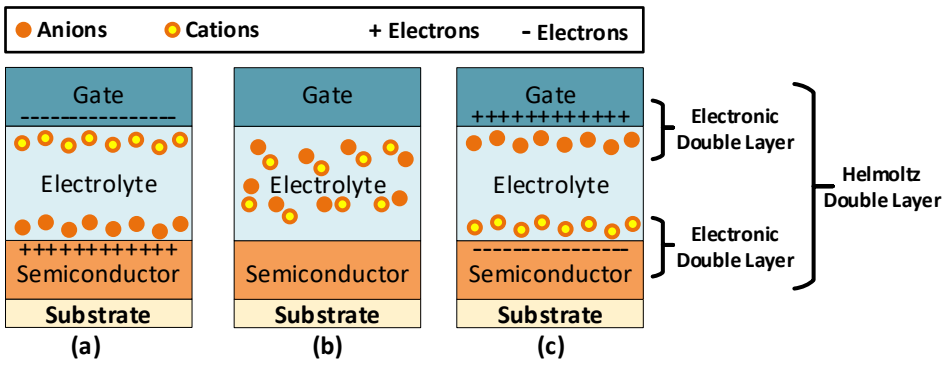


Figure 2.7: Distribution of charge carriers in an electrolyte sandwiched between semiconductor and gate-electrode. Gate is (a) negative biased (b) unbiased (c) positive biased

Contrary to that, inorganic oxide semiconductors are promising alternative to organic semiconductors as they provide high field-effect mobility [96]. One such inkjet printing technology based on the inorganic channel material is the Electrolyte-Gated Transistor (EGT) Technology (also referred as EGFET). The indium oxide (In_2O_3) semiconductor is used as a channel material while the gate dielectric is replaced with a solid polymer electrolyte. When a positive potential is applied at the gate electrode, the negative ions in the electrolyte accumulate at the gate-electrolyte interface. On the other hand, the positive ions accumulate at the electrolyte-

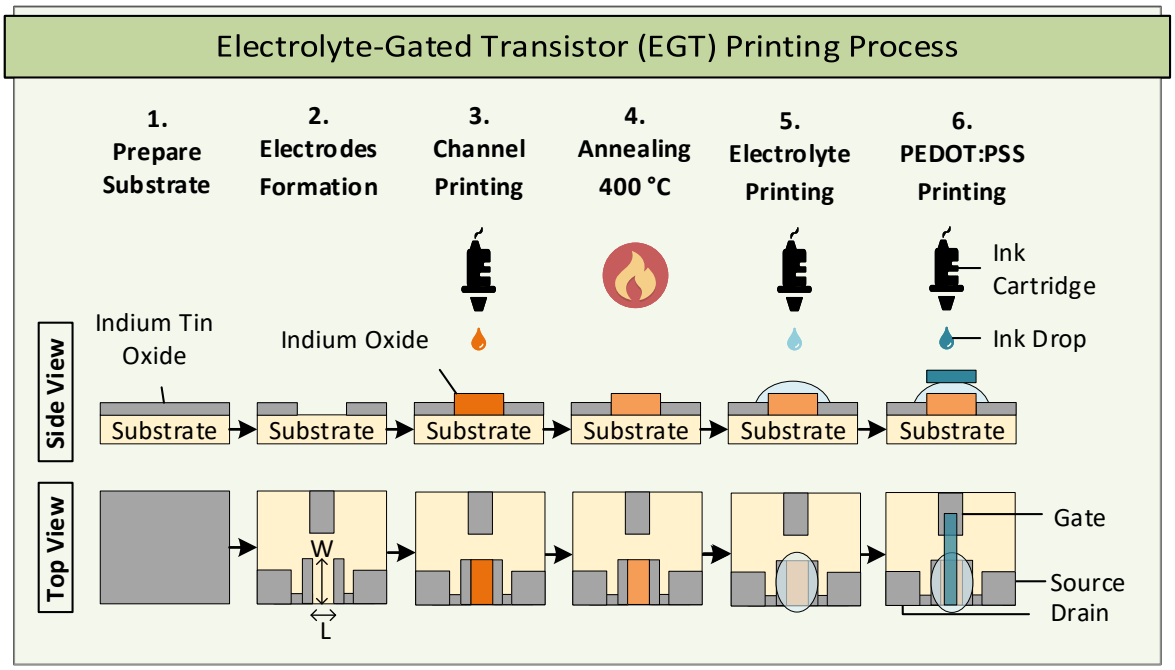


Figure 2.8: Electrolyte-Gated Transistor (EGT) Printing Process (W = Channel Width, L = Channel Length).

semiconductor resulting in the accumulation of negative charges at the channel surface. The electronic layers between gate-electrolyte and electrolyte-semiconductor interface are known as Helmholtz double layers [97] (refer Figure 2.7). These layers provide high-gate capacitance which allow EGTs to operate at very low supply voltage (<1 V) [2, 37, 59, 63] making it a promising candidate for battery and energy harvester powered applications. The PEDOT:PSS is used as the top-gate electrode. The typical threshold voltage (V_{th}) of EGT is around 0.2V.

The fabrication cost in EGT technology can be considerable lower than the cost of silicon-based circuits. As an example, a standard Dimatix Materials Printer DMP-2831 used to print EGT -based circuits costs less than 50 thousand US$. Compare this against the hundreds of millions of dollars needed for even the older silicon foundries [98]. The promise of printing is that these low fabrication costs can be used to target disposable and ultra-low cost margin application domains.

Fabrication Process

EGTs are prepared on 150 nm coated indium tin oxide (ITO) glass substrate. Before printing, the substrate is cleaned with acetone and 2-propanol. After cleaning, drain-, source- and gate-electrodes are structured on the substrate using e-beam process. Next, the channel material (indium precursor) is inkjet-printed between the source- and drain-electrode. The indium precursor is composed of 0.05 M $In(NO_3)_3 \times H_2O$ dissolved in double deionized water and glycerol (4:1). Following the channel printing, the substrate is annealed at 400 °C for two hours to improve the morphology of the printed channel. There is a possibility to cure the channel material at room temperature using photonic curing [99]. However, such devices show less field-effect mobility values compared the annealed devices. In the next step, composite solid polymer electrolyte (CSPE) is printed on top of the channel material. The CSPE is formulated by dissolving 4.29 wt% polyvinyl alcohol (PVA) in 85.71 wt% dimethyl sulfoxide (DMSO) and 1 wt% lithium perchlorate ($LiClO_4$) is dissolved in 9 wt% propylene carbonate

Figure 2.9: (a) Dimatix Material Printer (DMP-2831) and ink solution (b) semiconductor parameter analyzer and characterization stage (Image Source: Fujifilm Dimatix Inc. and Keysight Technologies, Inc.

(PC). Both solvents are mixed together when they are completely dissolved. In the final step, a conductive polymer, Poly-3,4-ethylendioxythiophen:polystyrolsulfonat (PEDOT:PSS), is printed as a top-gate on top of the CSPE connecting the CSPE with the ITO gate-electrode. The EGT printing process is shown in Figure 2.8. All materials are printed with Dimatix Material Printer (DMP-2831). The printer, cartridge and an example of solution processed ink is shown in Figure 2.9a.

Electrical Characterization

After printing the devices, the substrate is taken to the characterization stage (see Figure 2.9b) to measure the electrical characteristics of the devices. All devices are characterized for output and transfer characteristics for different voltage values. During measurement, humidity level is set to 50 % as humidity can alter the device characteristics [100]. All measurements are performed with Keysight 4156C precision semiconductor parameter analyzer. The measured transfer characteristics of EGTs with different channel area are shown in Figure 2.10 [1].

Circuit Design Flow

In EGT technology, circuits are realized with transistor-resistor (TR) logic. This is because until now no reliable p-type EGT has been realized in this technology [102]. Currently, two types of resistors are realized in this technology: printed (PEDOT:PSS based) and structured (ITO based), as shown in Figure 2.11. The ITO-based resistors are realized by structuring meanders (obtained through laser ablation) on ITO-coated glass substrate. The resistance value is controlled through the length and width of the meander structure. On the other hand, PEDOT:PSS printed resistors are realized by printing PEDOT:PSS between two ITO pads. The resistance value is controlled through the length, width and the number of printed layers of the PEDOT:PSS. The layout and printed design of a top-gate EGT and TR-logic based inverter circuit are shown in Figure 2.12. EGT channel width (W) is 200 µm and length (L) is 40 µm. In the inverter circuit, the ITO resistor is used in the pull-up network while EGT is used in the pull-down network. Variety of EGT based circuits are demonstrated in [103].

[1] Part of this data has been published in [101]

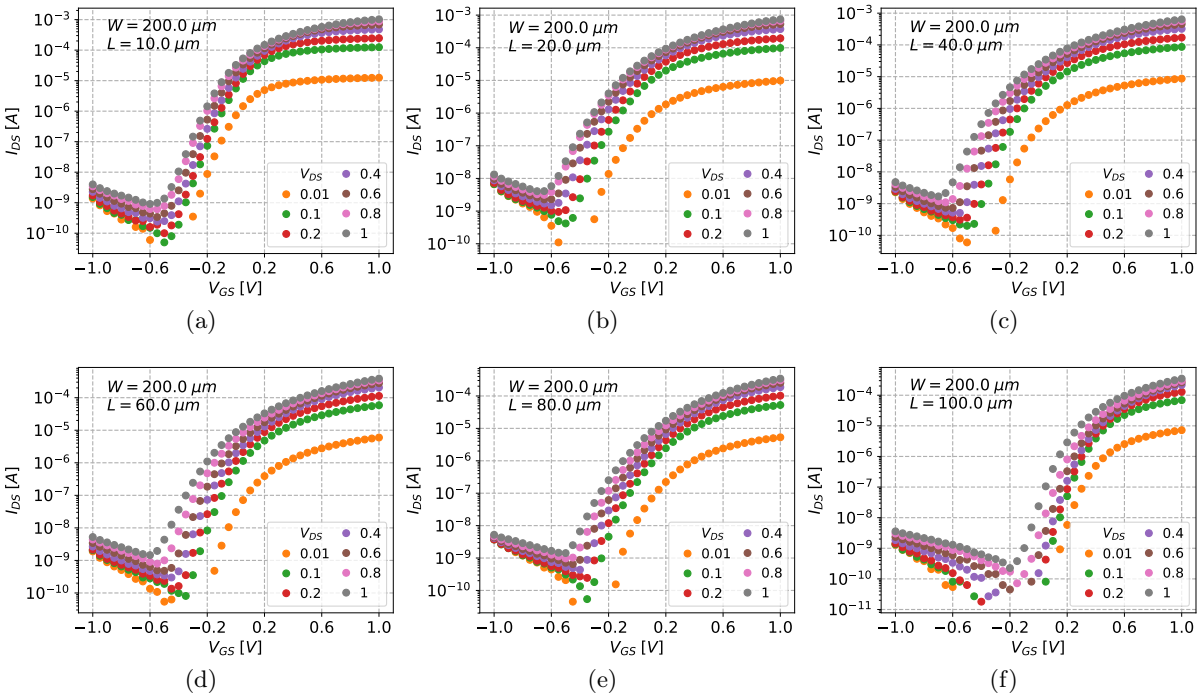


Figure 2.10: The measured transfer characteristics of EGT with channel width (W)= 200 µm and channel length (L)= 10 µm to 100 µm. (V_{GS} = −1 V to 1 V and V_{DS} = 0.01 V to 1 V)

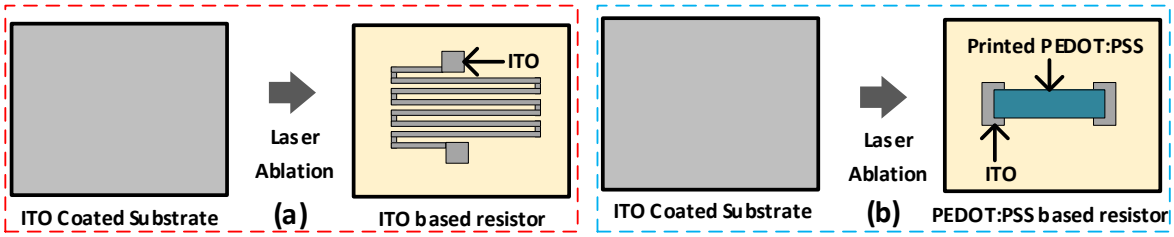


Figure 2.11: (a) Indium Tin Oxide (ITO)-based meander structure resistor (b) PEDOT:PSS-based printed resistor between two ITO pads.

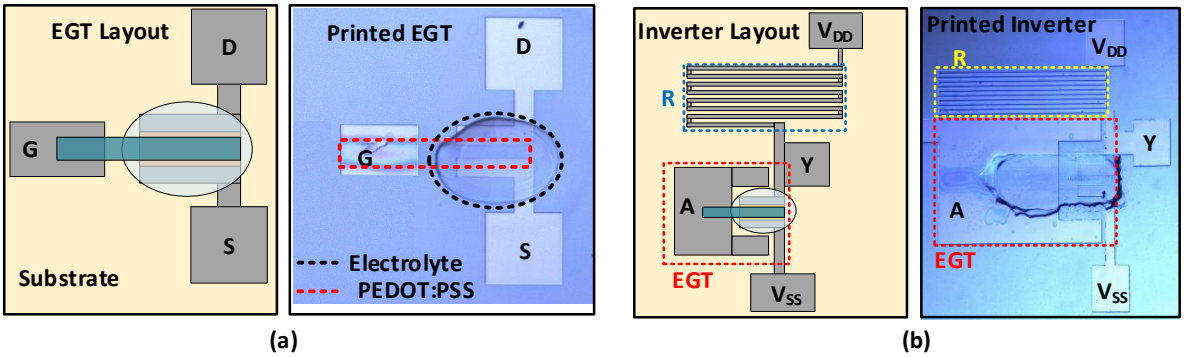


Figure 2.12: (a) The top-gate Electrolyte-Gated Transistor (EGT): layout and printed. The channel width W = 200 µm and length L = 40 µm (b) Transistor-Resistor (TR) logic based inverter circuit: layout and printed design.

2.3 Design Flow Challenges

From the previous section discussion, it can be concluded that inkjet-printed electronics (PE) technology has a variety of features which can enable a wide range of new applications. On the other hand, there are many materials and printing related parameters that the user should be aware of while designing circuits and applications in this technology (see section 2.2.1). It is worth mentioning that the majority of research areas in inkjet-printed electronics revolve around material and printing improvements to enhance the device performance [104, 105]. There are also some work on circuit design as well but very few contributions on printed electronics design flow [106, 107, 108, 109, 110]. In order to scale the printed technologies and

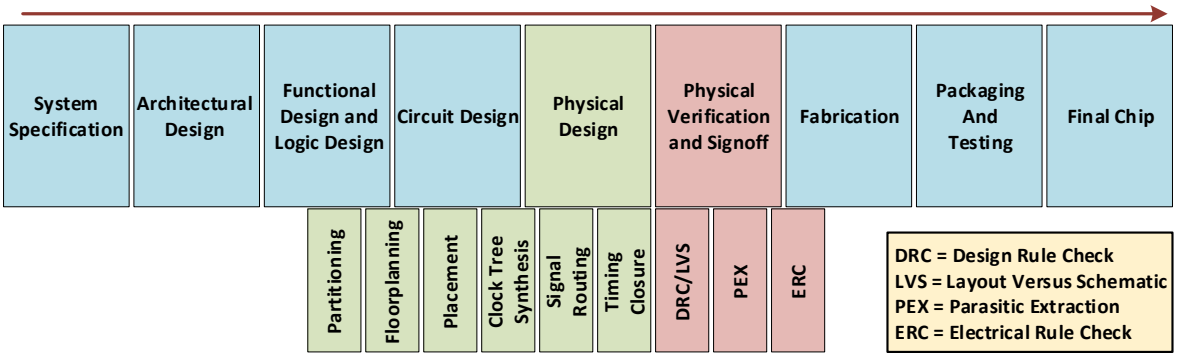


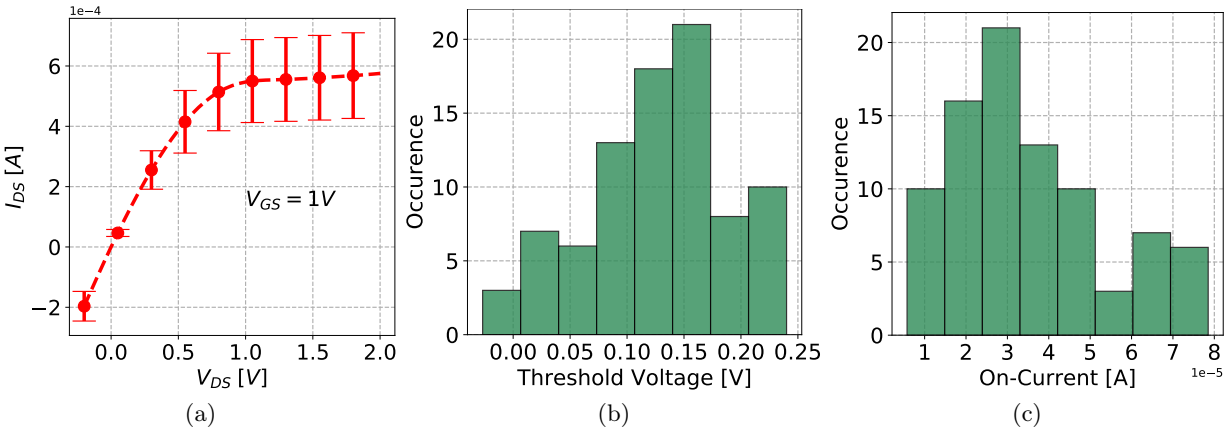
Figure 2.13: VLSI Design Flow.

bridge the gap between technology and design, the research around printed electronics design flow should be explored. This can be achieved by either using the Electronic Design Automation (EDA) tools developed for the microelectronics world and modify them for the PE design constraints or developing a new PE PE technology specific EDA/CAD tools. Additionally, a Process Design Kit (PDK), containing all the necessary information about the technology and printer parameters, should be developed to aid the designers in developing PE circuits and applications. There are a variety of steps involved to develop such circuits/applications and all these steps are part of the design flow for any technology. The typical design flow is shown in Figure 2.13. As PE processes are still on the early stages of technology development, we adapt full-custom design flow. The key components of the design flow, which are also the main contributions of this thesis, are discussed in the next subsections.

2.3.1 Modeling

The term model is used to represent the functionality of the devices and software simulation of a process in a technology. The device models are developed to represent the electrical characteristics of the devices in the simulation tools. Such models are not limited to device level, logic and circuit level models can also be developed from the fundamental device models. The device models have some key parameters that a user can modify to optimize the device performance. Process models are used to simulate any process step in the technology such as OPC (Optical Proximity Correction) in silicon-based methodologies or drop simulation in inkjet PE technology. These models are used to analyze and verify that the relative process step would not alter the design characteristics or introduce electrical faults in the design.

For the accurate printing and functionality of the printed circuits, in-depth knowledge of the printing processes and their modeling is required. Currently, the main research in PE is still on material and device improvements. There are some works related to modeling of deposited lines and films in the printing process [111]. As the EGT technology is still in the development



(a) (b) (c)

Figure 2.14: Parameters variation in EGT technology. Variations in measured (a) output characteristics (b) threshold voltage and (c) on-current of 88 EGTs.

phase, the modeling work in this thesis is focused on the compact models of the printed devices and their electrical characteristics under process variation. To develop proper analysis and design automation tool-sets for EGT technology, having an accurate and versatile transistor and process variation model is a crucial first step. The typical approach in modeling is to characterize the transistors and fit the measurement data to any standard transistor model by extracting some parameters from the measured data. A good model should be able to explain the characteristics of EGTs in different operating regions of output and transfer characteristics. In case of statistical modeling, the characterization approach remains the same. However, multiple devices are characterized to extract the distribution of model parameter. Then, these model parameters are estimated using statistical distributions. Figure 2.14 shows the variations in the output characteristics of EGTs as well as the distribution of the extracted key model parameters (threshold voltage and on-current). Process variation in inkjet PE is high because all devices are printed individually by multiple additive process steps, where each step can vary on its own. Moreover, the sources of variation (see section 2.2.1) in PE are more crucial than conventional silicon-based technologies. Thus it is crucial to model the electrical characteristics of the devices in nominal case as well as under process variation to scale the technology and optimize the design flow.

2.3.2 Physical Design

The physical design is the process of transforming a circuit description into the physical layout, which describes the position of cells and routes for the interconnections between them. This step is further divided into multiple sub-steps including design, verification and validation of the layout. Physical design flow uses technology libraries that contains the substrate information, standard cell constraints and the layout rules. The key steps in design flow include netlist synthesis, floorplanning, placement, clock-tree synthesis, routing, physical verification and GDSII generation. Some of these steps can be directly applied in PE design using microelectronics EDA tools. However, few of them (such as placement, routing and design verification rules) should be modified for the PE design constraints.

As inkjet PE is an additive technology, it has very limited metal layers for routing. For the physical design of complex circuits, crossovers are printed at the intersection of two different routing paths. Such crossovers can alter the performance of the circuits and their placement should be optimized in the placement and routing flow. This problems does not exist in

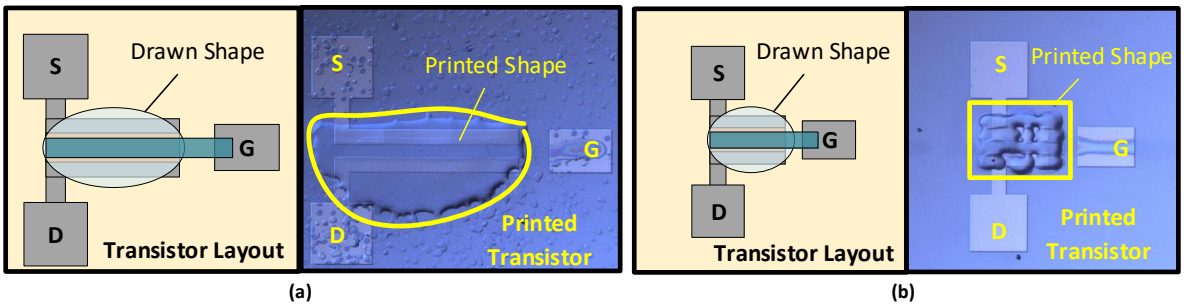


Figure 2.15: Layout and printed EGTs with different layout imperfections: (a) dispersion of printed material and (b) voids in the printed layout due to drop coalescence (D, G, S represent Drain-, Source- and Gate-electrode, respectively).

traditional microelectronics, as *via* is used for the conductive connection between different metal layers. Additionally, the design rules definition in additive PE technologies is complex due to fluid dynamics of inks/pastes. In silicon based technologies, these design rules are defined by the foundry that enable the designer to verify the correctness of the layout for the lithographic photomask. These photomasks are used to fabricate the silicon ICs with negligible variations in the fabricated design. However, additive PE technologies are based on maskless process where the deposited material shows a number of mechanical properties (such as dispersion and coalescence) (see Figure 2.15). Hence, extensive characterization of the printed materials is required to define new set of design rules and new EDA tools are required to model such complex interactions of the printed materials. Only then the verified printed design can be extracted from the layout tools. Moreover, after generating the final layout file (GDSII), the post-layout procedures are different compared to the conventional silicon based-technologies. Such as, in microelectronics, OPC is preformed on the layout while layout compensation techniques are applied for PE technologies [9]. The next step after the post-layout procedures is the manufacturing of the circuit.

2.3.3 Technology and Design Kit

The circuits and applications in a particular technology are realized through a Process Design Kit (PDK). The PDK is comprised of a set of files that contains all the information of the process technology and it is used with Computer Aided Design (CAD) tools to enable the design flow for that technology. The PDK is developed by extensively characterizing and modeling the process and technology parameters. For any emerging technology like PE, the PDK is developed through step-by-step characterizing at different steps of the design flow (from materials to circuits). This allows to develop basic PDK with few technology parameters and then it is evolved with the new set of characterization and modeling data. The basic PDK requires schematic design, electrical simulation and physical design. The schematic design is a technology-independent step and it aids the user to design circuits based on the available devices in the design kit. Every device should have a model to run electrical simulation. Different design parameters can be modified in the schematic to observe the changes in the simulations. The physical design is enabled by defining the necessary technology layers, their connectivity and parameterized cells (pcell). The pcell allows automatic generation of the device layout based on the defined parameters. The schematic then can be converted into layout with the help of this information. The automation of this process can help to generate a variety of benchmark circuits and test structures to improve the PDK through extensive technology characterization. The technology characterization and PDK development steps are shown in Figure 2.16.

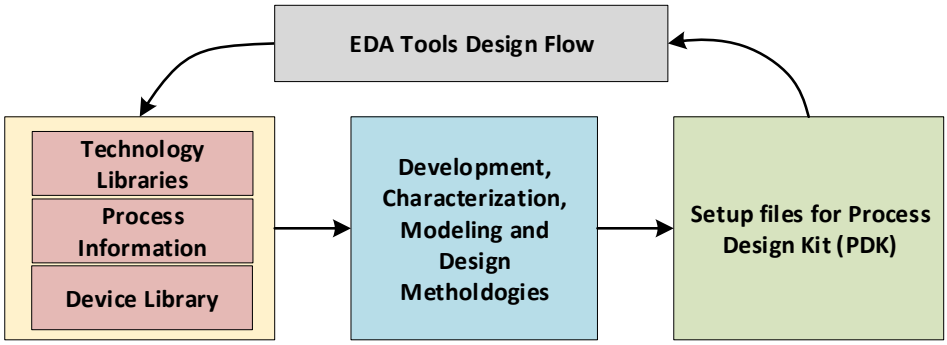


Figure 2.16: Technology, PDK and design flow development through EDA customization [9]

The standard cell library (SCL) is also part of the PDK. However, sometimes it is provided as a separate components as it contains all the process information required to design, simulate and verify the design without PDK. SCL is a library of digital primitive blocks that include set of logic cells called standard cells. The SCL is used to design, synthesis and place and route application-specific integrated circuit (ASIC) designs. Every standard cell contains set of transistors and their interconnects to realize a boolean logic or a storage cell. It is possible to generate any boolean function using only a NAND or a NOR gate. However, mostly, many different types of logic gates are added in the library due to delay, area and power constraints of the design. A library with a variety of logic gates and multiple driving strength cells can be used to efficiently implement complicated digital systems. Based on the requirement, either primitive gates such as buffer, inverter, NAND, NOR, XOR and memory cells or complex cells such as adders are included (together with the primitive cells) in the library. Every cell has a symbol view for the schematic design and a layout view for the physical design. The designed layout is verified (DRC and LVS) to insure that the design rules are not violated. The area, delay and power information is defined inside the timing file which is generated during the SCL characterization. The timing file contains timing models and data to calculate, input/output path delays, timing check values and interconnect delays. The timing models data is stored in a lookup table and each value is the table is calculated based on the input signal slew rate and output load capacitance (Figure 2.17).

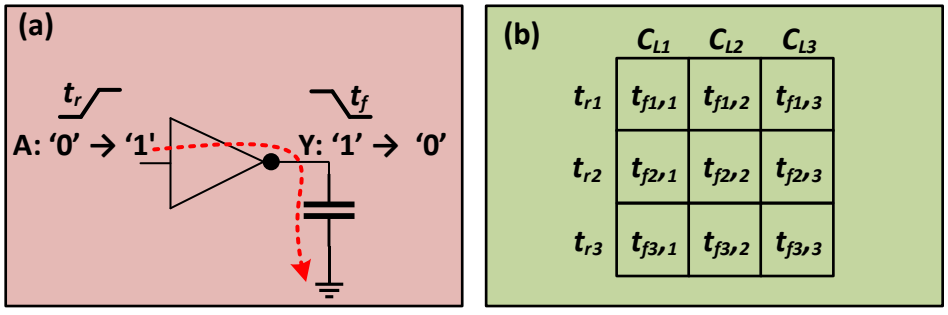


Figure 2.17: (a) NOT gate A → Y arc '1' → '0' output transition (b) Look-up table data containing output fall transition (t_f) based on input rise transition (t_r) and load capacitance (C_L)

The standard cells are first designed at the transistor level and then characterized for different input and output load conditions to extract the delay and power information. Then, a hardware description language (HDL) is used to design the system and then it can be synthesized using the primitive components in the SCL. The final design can be optimized using CAD tools for

different design constraints such as area, delay and power. These constraints are much severe for the EGT technology due to transistor-resistor (TR) based standard cells (refer section 5.4). As the pull-up logic is realized through a resistor, the cell leakage current is high while gain is low. Moreover, the TR logic has asymmetric rise and fall time of a cell and due to the high gate capacitance of EGT the cells have low cut-off frequencies. Due to all such design constrains, architectural optimizations are required for designing digital systems using EGT's SCL (as discussed in [58]).

2.4 State-of-the-art in Inkjet-Printed Electronics Technology

In the last decade, a lot of work has been published to improve the organic inkjet-printed electronics technology. The work was mainly focused on improving the mobility, conductivity, environment stability and other electrical properties [112]. A lot of works have also been published about the physical and chemical properties of the transistor to investigate the organic semiconductor material and device performance [50] including solution-processed n-type semiconductors [94]. Some progress reports and Ph.D. thesis are also published related to the technology development and applications of inkjet-printed electronics technology [105, 38, 103, 113]. There are a number of research articles on passive devices and components including resistor, capacitor, RFID tags, antenna and conductive lines [114, 115, 116, 117]. In the area of inkjet-printed circuits, a variety of work has been published ranging from basic logic gates [118], ring oscillators [37, 119], full-adder [105] to circuits for security applications [61, 59] and neuromorphic computing [120]. Unfortunately no complex circuits have been realized using inkjet-printed process. However, recently we performed the design exploration of printed processors and their applications [58]. For the EDA tools, some groups have reported the design kits [108, 109], layout optimization [9, 121], and technology characterization methodologies [113].

There are many contributions for inkjet-printed technologies ranging from materials to the EDA and design flow. However, this technology is still not mature as other printing technologies where complex digital and analog circuits [38] as well as a microprocessor has been realized [122]. Hence, the objective of this thesis is to improve the compact models, physical design, and process design kit to enable the design flow.

2.5 Conclusion

This chapter provides the preliminary information regarding printed electronics technologies and the technology development. We provided the generic introduction of printed electronics, its features and applications. The inkjet-printed electronics technology is discussed in detail along with key variability sources in this technology. The electrolyte-gated transistor (EGT) technology, for which we developed the design kit, is also introduced. Challenges associated with the design flow of printed electronics technology are also discussed. Additionally, we reported the state-of-the-art work for inkjet-printed electronics technology.

3 Modeling of Printed Electrolyte-Gated Transistors

The accurate description of electrical characteristics and process variability in electronic design is not only crucial for modern very-large-scale integration (VLSI) technologies but even more relevant for emerging technologies such as printed electronics [123, 124, 125, 126]. All such models provide a proper interface between technology and circuit design. These models are developed by characterizing the devices and circuits under different voltage and temperature range. An accurate model should be able to predict the performance of devices and circuits under process, temperature and voltage variations. In this chapter, we propose compact models (nominal and statistical) that can capture the Electrolyte-Gated Transistors (EGT) behavior in typical conditions as well as under process variations [54, 55].

The rest of the chapter is organized as follows. Section 3.2 discusses the printed transistor existing modeling techniques and their draw-backs. In Section 3.3 and 3.4, we present our modeling methods for nominal and statistical model, respectively. The modeling results using the proposed methods as well as comparison of simulation vs measurement is reported in Section 3.5. Finally, Section 3.6 concludes the chapter.

3.1 Introduction and Motivation

Besides the progress on improving the technology and fabrication process of the EGTs, developing proper analysis and design automation tool-sets for EGT technology is equally important. For such purpose, having an accurate and versatile transistor model for EGT is a crucial first step. A good model should be able to explain the characteristics of EGTs in different operating regions of output and transfer curves by accurately capturing the three-dimensional behavior of drain-source current with respect to drain-source and gate-source voltages ($I_{DS} - V_{DS} - V_{GS}$). Additionally, as the process variation in printed electronics is considerably high, a single segment and continuous model is vital for that purpose.

Variability modeling is vital to optimize functionality and manufacturing yield, especially along the design chain from the single device to circuit simulations [127]. It is always challenging to simulate effects of process variations and closely reflect it in design automation tools [128]. In silicon technology, process variations are divided into local and global variations [129]. The variability, whether it is of systematic and/or random origin from lot-to-lot, wafer-to-wafer, or chip-to-chip is applied to all transistors and is referred to as global variations. The remaining with-in chip variations are referred to as local variations [130, 131]. Contrary to that, in inkjet-printed electronics all devices are printed individually by multiple additive process steps, where each step can vary on its own. These process and systematic variations originating from the ink, substrate and manufacturing tools are random and cannot easily be divided into local and global variations.

The major source of variation in this technology involves the dispersion of the ink on the substrate, which is inherent to inkjet printing. Other sources of variations include droplet jetting oddness, satellite drops, wetting and missing droplets [126] (refer section 2.2.1). These effects introduce variations in each printing/process step (channel, dielectric and top-gate) of the EGT and could lead to non-Gaussian distributions of the process and electrical parameters

of the technology. Such distributions may have complex correlations which cannot be captured if they are estimated with a simple Gaussian distribution. The aforementioned variation sources increase the probability of the performance reduction or complete failure of the circuit. From the simulation point of view, the modeling of variability for any new and additive manufacturing technology, such as this, is necessary to reflect the implications of the technology parameters for circuit design.

3.2 Related Work

3.2.1 Nominal Model

A variety of modeling techniques for printed transistors are reported in the literature. There are techniques for organic transistors modeling [132, 133, 134] based on the basic level-1 SPICE model [135]. These models are mainly developed for organic transistors which typically operate at high voltages. The parameter extraction conditions in saturation region, where typically $V_{DS} > 5V$ in organic transistors, are invalid for EGTs. Moreover, these models cannot capture the $I_{DS} - V_{GS}$ behavior of EGT. Modeling of printed transistors based on the amorphous silicon models, such as level-15 AIM SPICE [136] or level-61 SPICE [137], is also proposed in [138, 139]. The main disadvantage of these models is that they require many physical parameters and do not model the below threshold regime for EGTs accurately. To overcome the drawbacks of the previous methods, authors in [2, 140] proposed to divide the transfer curves into three different regions (above-threshold, near-threshold, and below-threshold). The below-threshold region is modeled by sub-threshold swing model [141] and the above-threshold region is typically modeled based on the Curtice model [142, 143]. Finally, a cubic interpolation (in [2]) or a genetic algorithm (in [140]) is used to smoothly connect the below-threshold and above-threshold regions. These methods can effectively model the typical behavior of the printed EGTs. However, they cannot accurately capture the characteristics of various fabricated transistors under process variation, which is intrinsic in the ink-jet printing process, and more severe compared to silicon fabrication process. This is essential for having a predictive model for designing printed electronic circuits. In the multi-region models, it could be very challenging to match the boundaries of the below-threshold, near-threshold, and above-threshold regions for modeling the process variation impact on the transistor behavior. For example, a minor change in the threshold voltage directly impacts the region boundaries. Therefore, it is required to recalculate the boundaries for each instance of the transistors which imposes excessive complexity to these models.

To avoid the problems associated with the aforementioned modeling techniques, we propose to use one model for all the operating regions of the EGTs, similar to the approach in the Enz-Krummenacher-Vittoz (EKV) model [144], which is a well-known model for metal-oxide-semiconductor (MOS) transistors. This ensures model continuity and smoothness across all operating regions for various transistors fabricated subject to printing process variations. Our proposed solution requires fewer parameters resulting in a simpler transistor model which can be easily implemented into any circuit simulator by using languages such as Verilog-A.

3.2.2 Variability Model

Multiple methodologies [145, 44, 146, 147, 148] are proposed in the literature to model and reduce variabilities in organic printed transistors. Some methodologies [145, 44] follow the assumption that the transistor model parameters are normally distributed. Based on a normality test [149], our measurement data shows that this assumption is not valid in EGT technology and might not always be valid for other technologies. Some authors [129, 146] investigated

the variations within-die (WID) by demonstrating parameter variation with respect to channel geometry and some authors proposed different transistor design styles [147] and layout compensation techniques [148], to reduce variabilities in printed transistors. These physical design based methods can reduce the variations but they cannot be utilized in modeling the distribution of individual model parameters for the EGT technology. Thus it is essential to have a predictive model to design and evaluate the behavior of printed circuits under process variations. In this chapter, we propose a generic solution to model variabilities in printed transistors and develop a compact statistical model using Gaussian Mixture Model (GMM) [150]. The methodology was validated for two different measurement datasets of transistors with different channel geometries.

3.3 DC Model for EGTs

In this section, we explain our DC model of the EGTs and the corresponding modeling approach and parameter extraction routines. For this purpose, we modify the EKV model [144], which is a compact model developed for sub-micron MOSFET transistors, to match the characteristics of the EGTs. The EKV model is developed based on physical parameters of the MOS transistors [151] and provides a single model for all operating regions of the MOS transistors. The foundation of the EKV model as well as the full derivation and physical constant assumptions are described in [152, 153]. The final drain current Equation for EKV version 2.6 model is given by [154]:

$$I_{DS} = I_0(\ln(1 + e^{\frac{v_p - v_s}{2}})^2 - \ln(1 + e^{\frac{v_p - v_d}{2}})^2), \tag{3.1}$$

$$I_0 = 2n\mu C_{ox}\frac{W}{L}\phi_t^2, \tag{3.2}$$

where parameters n, μ, and C_{ox} are ideality factor, carrier mobility, and the oxide capacitance per surface unit, respectively. The channel width and length of the transistor are W and L, while v_p, v_d, and v_s present channel, drain, and source potentials, which are normalized by the thermal voltage ϕ_t:

$$\phi_t = \frac{k_B T}{q} = \frac{V_D}{v_d} = \frac{V_S}{v_s} \tag{3.3}$$

$$v_p \approx \frac{V_{GS} - V_{th}}{n\phi_t} \tag{3.4}$$

Here, V_{GS} is the gate-source potential, and V_{th} defines the threshold voltage. Equation (3.1) cannot be used directly to model EGTs, as it poorly fits to the $I-V$) curves of these transistors. We modify this Equation and adjust it according to the physical characteristics of the printed EGTs.

3.3.1 Extension of EKV Model for EGTs

Our objective is to derive a model for all operating regions of the EGTs based on the EKV model. For this purpose, we take the aforementioned Equations and modify them to match the EGT behavior over all regions. Similar to the filed-effect mobility in MOS transistor, the EGTs also have power-law dependence from gate overdrive voltage [2]. So, we adjust Equation (3.1) according to the field-effect mobility of EGTs:

$$I_{DS} = I_0(\ln(1 + e^{\frac{v_p - v_s}{2}})^\gamma - \ln(1 + e^{\frac{v_p - v_d}{2}})^\gamma). \tag{3.5}$$

Equation (3.5), introduce a power-law dependency on the gate overdrive voltage for the above-threshold region. Parameter γ explains the dependency between the gate overdrive voltage and the drain current. We also extended EKV model Equation to match different regions of transistor characteristics curves by introducing fitting parameters in Equations (3.1), (3.2) and (3.4) and modify them to:

$$I_0 = 2nf_1\frac{W}{L}\phi_t^2 \tag{3.6}$$

$$v_p \approx \frac{V_{GS} - (V_{TH} - f_4 V_{DS})}{\frac{n}{f_2}\phi_t} \quad \text{and} \quad n = \frac{1}{SS * \phi_t * ln(10)} \tag{3.7}$$

The fitting parameter f_1 scales the I_0 current, hence, we do not need μ and C_{ox} in the Equation (3.6) anymore. Also, f_2 tunes the knee-region in the output characteristics curves. We observed that in the below-threshold region, the drain current of EGTs increases significantly when the drain-source voltage is increased. This is fairly similar to the Drain-Induced Barrier Lowering effect (DIBL) in the short-channel MOS transistors, which could be attributed to the minor overlapping of drain region and the gate electrolyte. Therefore, parameter f_4 is used to reflect the spreading of transfer curves in the below-threshold regimes.

$$I_{DS} = I_0.(\ln(f_3 + e^{\frac{v_p - v_s}{2}})^\gamma - \ln(f_3 + e^{\frac{v_p - v_d}{2}})^\gamma) \tag{3.8}$$

The final drain current Equation, after all modifications is Equation (3.8). Here, parameter f_3 is introduced to match the transfer curves in below-threshold regime. Our proposed Equation requires few parameters (compared to the previously proposed models) and it is continuous and accurate in all operating regimes.

3.3.2 Parameter Extraction Flow

The proposed model contains fitting and empirical parameters. Fitting parameters are extracted by reducing the sum of mean-squared errors between the measurements and the model generated $I - V$) curves while all other parameters are extracted empirically from the measurement data by extrapolating different regions in the EGT characteristics curves. Before extracting parameters, measurement data should be normalized by dividing to channel geometry of the transistor ($\frac{W}{L}$). Once the model parameters are extracted, drain current Equation is multiplied with $\frac{W}{L}$ as in Equation (3.6) to scale the drain current according to the geometry. The overall flow of the proposed extraction method is shown in Figure 3.1. The flow is divided in two parts:

Empirical Parameters Extraction

The proposed drain current Equation contains 3 empirical parameters V_{th}, γ, and SS. Parameters SS can be extracted directly from the $I - V$) data. The V_{th} and γ are extracted (at $V_{DS} = 1V$) using the H-integral function which is given by Equation 3.9. The intercept of the linear part of $H(V_{GS})$ on x-axis gives the V_{th} and the slope of this linear region is used to estimate the γ.

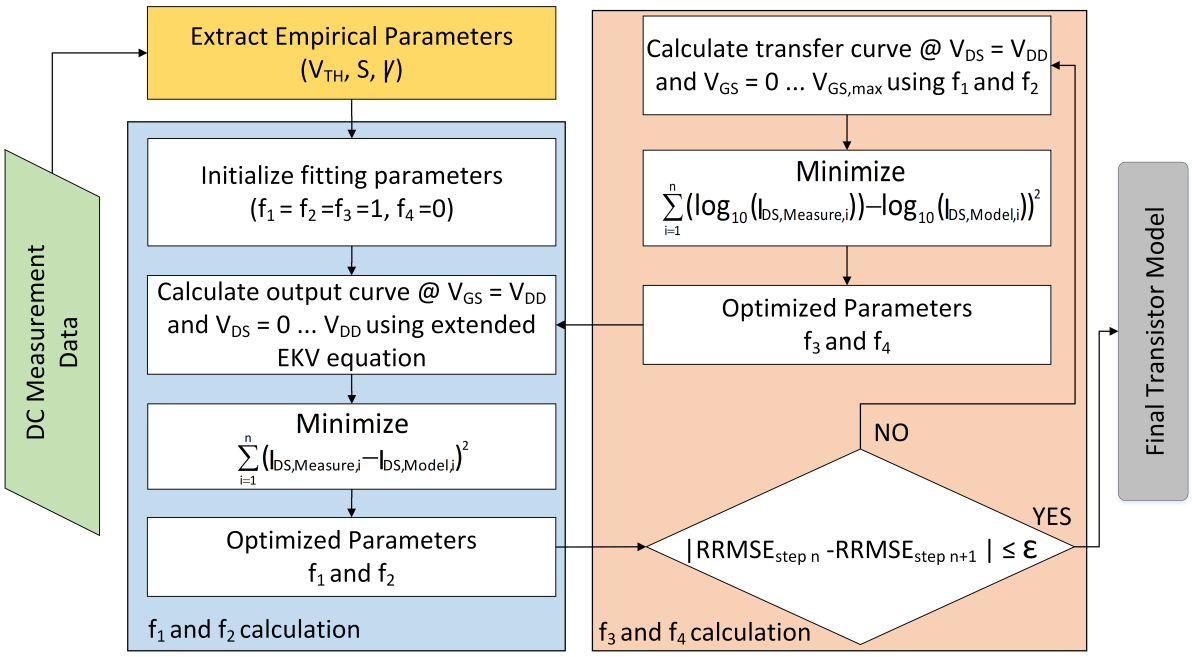


Figure 3.1: Entire modeling flow with explanation of fitting parameters (f_{1-4}) extraction (max. n = 600, $\varepsilon = 1e^{-3}$).

$$H(V_{GS}) = \frac{\int_0^{V_{GS}} I_{DS}(x)}{I_{DS}(V_{GS})} dx \tag{3.9}$$

However, the H-integral function for Equation (3.8) is very complex and cannot be simplified to extract γ. Since the above-threshold behavior of Equation (3.8) is very close to the Curtice model, we use the γ extracted from H-integral function solution for Curtice model instead. All parameters are empirically extracted from transfer and output curves in the same way as explained in [2].

Fitting Parameters Extraction

The model has 4 fitting parameters (f_1, f_2, f_3 and f_4) for matching the measurement data to the model in different regions. Figure 3.2 shows the effect of fitting parameters on output and transfer curves. The extraction of fitting parameters is implemented using Levenberg-Marquardt algorithm (LMA) [155] which is primarily used for non-linear least squares curve fitting (Equation 3.10). This algorithm calculates the fitting parameters (P) of the model curve ($f(x, P)$) by reducing the sum of the squared deviations for a given set of n data pairs (x_i, y_i).

$$\hat{P} = \arg\min_{P} \sum_{i=1}^{n} [y_i - f(x_i, P)]^2 \tag{3.10}$$

After calculating all fitting parameters, an iterative approach is used to find the optimized parameters that produce minimum fitting error in output and transfer curves. The metric we use for the fitting error is Relative Root Mean-Squared Error (RRMSE). It takes the root-mean

squared of the relative error between each measurement and model generated point.

$$RRMSE = \sqrt{\frac{1}{n}\sum_{j=1}^{n}\left(\frac{I_{DS,model,j} - I_{DS,measure,j}}{I_{DS,measure,j}}\right)^2} \times 100\% \tag{3.11}$$

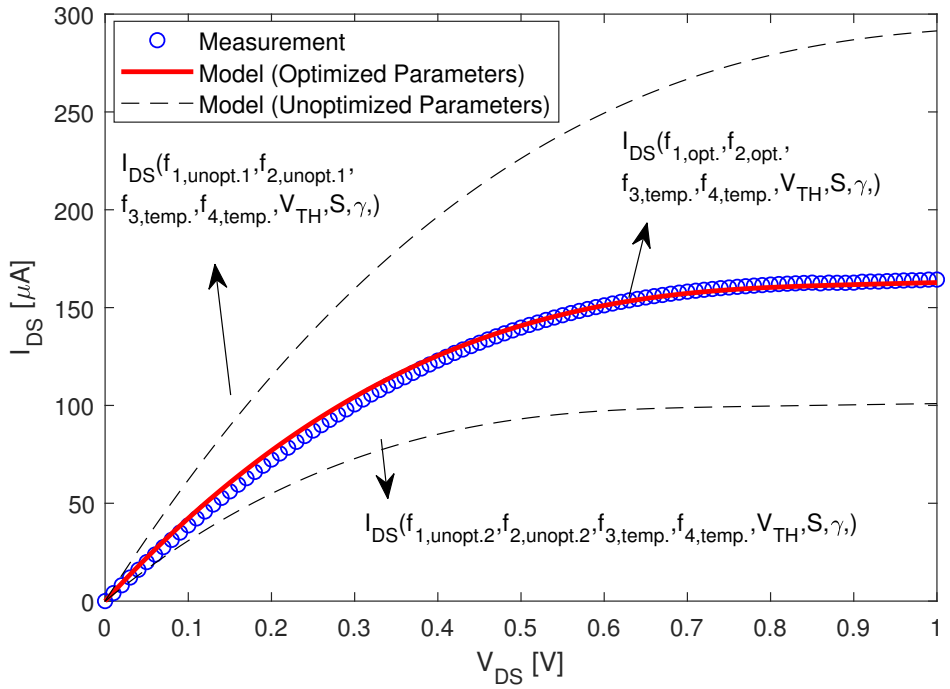
We use RRMSE metric as it considers the same weight for all points in different operating regions of the transistor irrespective of the absolute value of the current at different points. Since it is a three dimensional optimization problem where I_{DS} is captured from V_{DS} and V_{GS}, we divided it into two parts , namely output and transfer curves. Two fitting parameters are calculated in each part. These fitting parameters are calculated in an iterative loop until the RRMSE is saturated. The reason to use an iterative approach is that the best fitting parameters for output curve may not lead to the best fitting for the transfer curve, and hence these fitting parameters need to be adjusted in an iterative manner until the best fitting for both output and transfer curves are achieved, to accurately capture the three-dimensional relationship among I_{DS}, V_{DS} and V_{GS}. This iterative approach will always lead to the fitting parameters which produce best match with measurement data for output and transfer curves, respectively. The procedure to calculate fitting parameters is as follows:

Step 1: First, initial value for fitting parameters ($f_{1,temp.} = f_{2,temp.} = f_{3,temp.} = 1$ and $f_{4,temp.} = 0$) is defined. Empirically extracted parameters from previous section along with initial values of fitting parameters are used in Equations (3.6)-(3.8) to calculate drain current (I_{DS}) for output curve ($I_{DS} - V_{DS}$) for maximum supported V_{GS} and $V_{DS} = 0 \ldots V_{DD}$ with a step-size that produce smooth curve. In our case, $V_{DS} = 0 \ldots 1V$ with $0.01V$ step-size and $V_{GS} = 1V$. The shape of the model-generated $I_{DS} - V_{DS}$ curve would be similar to measurement data. However, the fitting parameters should be tuned to match with the measurement data.

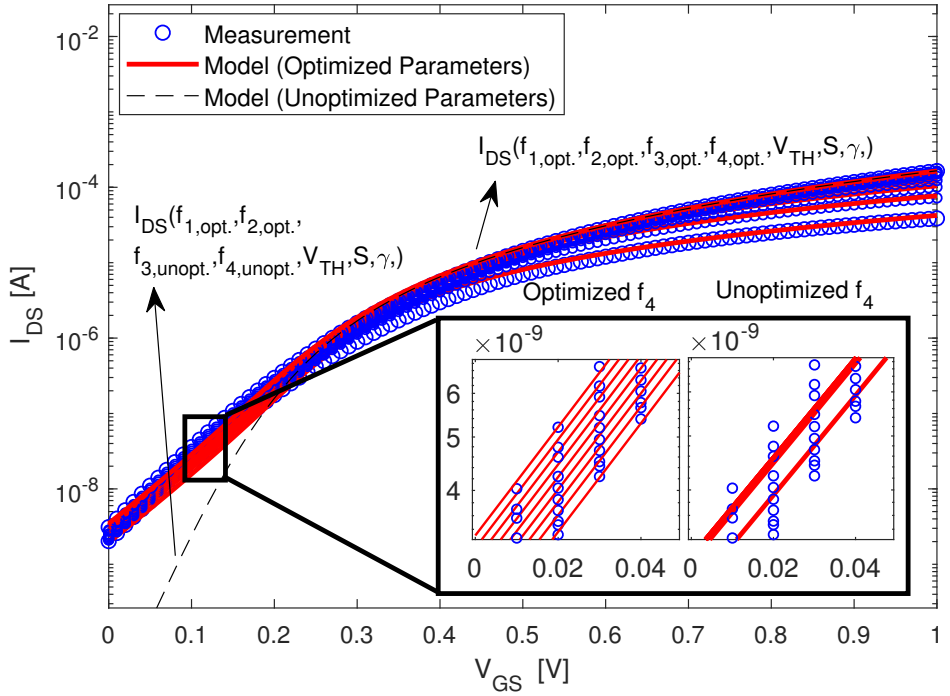
Step 2: Parameters f_1 and f_2 are calculated from $I_{DS} - V_{DS}$ curve at maximum gate voltage i.e. $V_{GS} = 1V$ in our case. A fitting parameter matrix (F) is defined that contains the initial guess of f_1 and f_2 as $F^T = (f_{1,temp}, f_{2,temp})$. LMA calculates the optimized fitting parameters ($f_{1,opt.}$ and $f_{2,opt.}$) by reducing the least-squared deviation (Equation (3.12)) between measured and model-generated curve. These optimized parameters (with initial guess for f_3 and f_4) used in Equations (3.6)-(3.8) to recalculate I_{DS} for output curve. It can be seen in Figure 3.2a that, with $f_{1,opt.}$ and $f_{2,opt.}$, the model-generated curves match accurately with the measurement data. In the same Figure, it can also be seen that how unoptimized parameters would shift the output curve.

$$\hat{F} = \arg\min_{F} \sum_{i=1}^{n} [I_{DS,Measure_i} - I_{DS,EKV}(x_i, F)]^2 \tag{3.12}$$

Step 3: Now, $f_{1,opt.}$ and $f_{2,opt.}$ are used in Equations (3.6)-(3.8) to calculate $f_{3,opt.}$ and $f_{4,opt.}$ from transfer curve ($I_{DS} - V_{GS}$) (as shown in Figure 3.2b). The $I_{DS} - V_{GS}$ at $V_{DS} = V_{DD}$ would match very well with the measurement data in near- and above-threshold regimes. However, below-threshold regime parameters need further optimization. These parameters are extracted by calculating the I_{DS} for $V_{GS} = 0 \ldots 1V$ at maximum V_{DS}. Since, I_{DS} values in below-threshold region are very small and they should be converted into logarithmic scale ($log_{10}(I_{DS})$) to efficiently calculate fitting parameters for this region. Now, $f_{3,temp.}$ and $f_{4,temp.}$ are defined as parameter matrix i.e. $F^T = (f_{3,temp}, f_{4,temp})$ to solve for $f_{3,opt.}$ and $f_{4,opt.}$. The extraction of f_3 and f_4 would introduce a mismatch in $I_{DS} - V_{DS}$ curve. So, f_1 and f_2 should be recalculated by iteratively repeating step 2. For each iteration (n), new fitting parameters will be calculated that produce less fitting error. The iteration runs until the optimization saturates and $|RRMSE_n - RRMSE_{n+1}| \leq \varepsilon$.



(a)



(b)

Figure 3.2: Calculation of fitting parameters: (a) f_1 and f_2 from output curve ($V_{GS} = V_{DD}$) (b) f_3 and f_4 from transfer curve ($V_{DS} = 0 \ldots V_{DD}$ *with* $0.1V$ *step-size*).

The value for ε could be very small, we chose it as $\varepsilon = 1e^{-3}$. All fitting parameters are extracted within 100 iterations. Fitting parameters in combination with empirical parameters can be used to develop the Verilog-A model for EGT using Equations (3.6)-(3.8).

3.4 Variability Model for EGTs

The typical approach to develop a compact statistical model is as follows: First, a set of model parameters that are sensitive to the process variations are determined [156]. The distributions of such model parameters are obtained from the DC characteristics of transistors from multiple wafers/samples. These parameters control the variations in the device's electrical performance which can be simulated using Monte Carlo (MC) simulations. MC simulations generate random samples with different sets of values of model parameters from their probability distributions [127].

In the silicon technology, where the process parameters are much better controlled by lithography and variations are minimal, few physical parameters (such as threshold voltage and oxide thickness) constitute the key variation parameters [156]. There is a direct correspondence between the key variation parameters and other model parameters. Such parameters are defined from the key variation parameters to capture physical correlations in variations [157, 156, 158, 125]. However, this approach cannot be adopted for the semi-physical EGT model since the dependencies and interdependencies of the physical/process parameters (such as channel layer thickness and doping concentration) are not captured [126]. The variation in the key model parameters would hence not capture the variation in other EGT model parameters and could lead to unphysical values. To mitigate this, all EGT model parameters are jointly estimated in order to maintain the correct correlation among them.

In this section, we describe the variability modeling method and the parameters extraction flow based on our EGT DC model which is described in Section 3.3.

3.4.1 Modeling Distribution using the Gaussian Mixture Model

Variability Parameters Selection

The threshold voltage (V_{th}) and the saturation current (I_{sat}) are the key physical properties to analyze the performance of the EGT. The saturation current is extracted from the measured output characteristic (at $V_{GS} = 1V$ and V_{DS} is sweeping from 0 to $1V$). The V_{th} is extracted (at $V_{DS} = 1V$) using the H-integral function as described in Section 3.3. The distribution of the V_{th} is estimated by extracting it from the measurement data of fabricated transistors. However, I_{sat} is dependent on other model parameters (see Equation 3.5). Typically, the model parameters which have no effect on the variable of interest (I_{sat}), or are almost constant like f_3 and f_4 in our case, can be fixed to their mean values and are excluded from the variability analysis. The parameter f_1 is treated as an independent variation parameter because it is the product of mobility (μ) and gate capacitance (C_{gate}). Additionally, the skewed distribution shape of f_1 could lead to negative values being generated from its estimated distribution. To avoid this, we estimate the distribution of $log(f_1)$ instead of f_1 and transform the sampled value back by applying the exponential function to it. We assume that only f_2 is a dependent parameter that can be modeled using the empirical accessible parameters (further described in the sub-section 3.4.1). .

In this work, a set of five model parameters $\{Vth, SS, \gamma, f_1, f_2\}$ are used in the variability modeling of the EGT. It is assumed that if all model parameters are modeled accurately, a statistical distance between the measured and the model generated distributions is minimized. One such distance is the Kolmogorov-Smirnov (KS) Statistic used by the Kolmogorov-Smirnov

(KS) test [159]. The KS statistic (D) for the difference between the measured and model-generated distribution of a given parameter P is given by Equation 3.13.

$$D = \sup_{P} |F_{model}(P) - F_{measured}(P)| \tag{3.13}$$

where $F_{model}(P)$ and $F_{measured}(P)$ are the distributions of the measured and the model-generated P and *sup* denotes the supremum function.

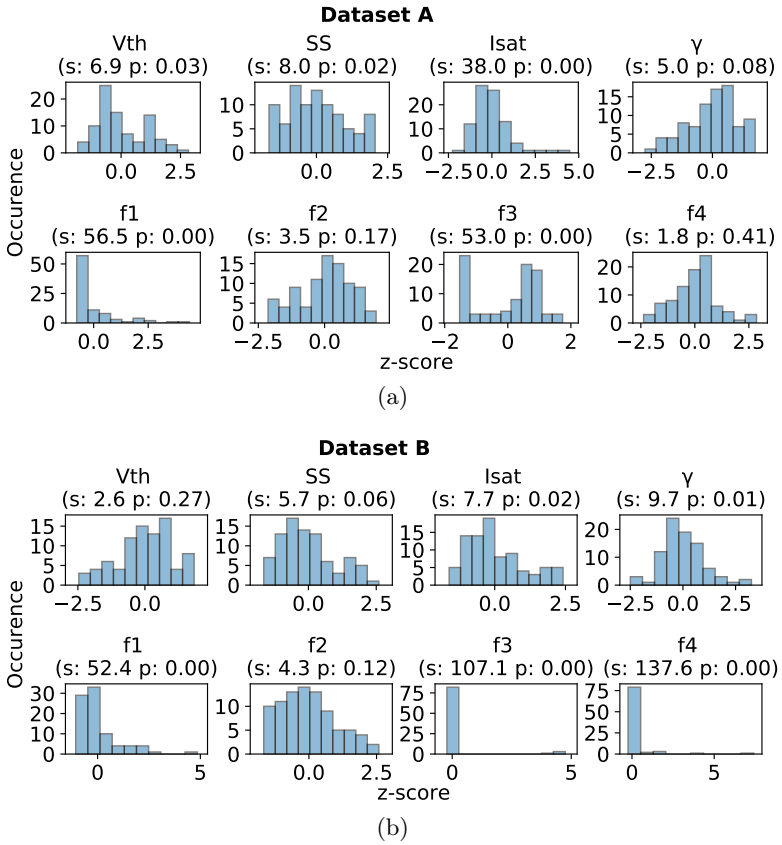


Figure 3.3: The standardized distribution of the parameters. The threshold voltage (V_{th}), sub-threshold slope (SS) and saturation current (I_{sat}) (at $V_{GS} = 1V$) are extracted directly from the characterization data by extrapolating the linear regions of the transistor DC characteristics. Gamma (γ) is an empirically extracted model parameter and f_1, f_2, f_3, f_4 are the fitting parameters of the EGT model. The p and s denote a 2-sided chi squared (χ^2) probability for the hypothesis test and a statistical distance that measures the deviation between the model parameter distribution and a normal distribution, respectively. The z-score is the standard score which is calculated by: $z - score := \frac{x-\mu}{\sigma}$ where x, μ and σ define the observation, sample mean and standard deviation, respectively. The z-score has a $\mu = 0$ and $\sigma = 1$. (a) The Dataset A contain 95 EGTs with channel length (L) and width (W) of $40\mu m$ and of $100\mu m$, respectively (b) The Dataset B contain 88 EGTs with fixed channel length ($L = 40\mu m$) and multiple channel widths ($W = 200, 400, 600$ and $800\mu m$).

Gaussian Mixture Model (GMM)

In this work, the EGT model parameters are extracted from the measurement data of two different datasets of printed transistors. The distribution of the model parameters is dependent on the technology itself and can be changed significantly while the technology evolves. Each model parameter, for both datasets, is tested for normal distribution using the D'Agostino's and Pearson's test [149]. This test measures whether or not the given sample comes from the normal distribution. It returns the probability (p) of the two-sided chi squared (χ^2) hypothesis test and its test statistic (s). Typically, the null-hypothesis is rejected based on the significance level of $\alpha = 0.05$. This means, that in case of $p < 0.05$, the hypothesis of the sample belonging to a normal distribution is rejected.

It can be seen in Figure 3.3 that for the dataset A, some model parameters are not normally distributed, as $p < 0.05$. However, for dataset B, the hypothesis that the data is coming from a normal distribution could not be rejected (since $p > 0.05$). Thus trying to fit the distribution of dataset A with a normal distribution will result in a poor approximation. To account for such cases, we propose to use universal probability density approximation function. One such function is the Gaussian mixture model (GMM) [150]. It can be used to model the parameter distribution regardless of its shape. A GMM utilizes a convex combination of K normal distributions ($\mathcal{N}$) and has three sets of parameters $\boldsymbol{\mu}$, $\boldsymbol{\Sigma}$ and $\boldsymbol{\alpha}$, which correspond to expected values, covariances and component weights, respectively. The parameter vectors μ_k and the matrices Σ_k denote the expected value and the covariance matrix of a respective normal distribution. The number of components K can be decided by indirect test error estimation using the Akaike Information Criterion (AIC) or the Bayesian Information Criterion (BIC) [160]. A mathematical formulation of the probability distribution function p of a GMM is given by Equation 3.14, where $x \in \mathbb{R}^4$ is a four dimensional data vector of the simulation parameters (V_{th}, SS, γ and f_1) which are estimated jointly to capture their dependencies.

$$p(x; \boldsymbol{\mu}, \boldsymbol{\Sigma}, \boldsymbol{\alpha}) = \sum_k \alpha_k \cdot \mathcal{N}(x; \mu_k, \Sigma_k) \tag{3.14}$$

$$\sum_k \alpha_k = 1, \quad \alpha_k \geq 0$$

To estimate the parameters of the GMM, the Expectation Maximization (EM) algorithm is used [161]. EM is a numerical method for maximum likelihood estimation. In addition to the initialization step, it consist of two iteratively repeated steps. In the initialization step, K is defined and the model parameters (i.e. μ_k, Σ_k and α_k) are initialized, for each component k, with reasonable random values based on some heuristic method. After the initialization step, the following steps of the EM algorithm, namely E-step and M-step, are applied iteratively:

- **First step (E):** The E-step, consists of calculating the expectation of the component assignments $\hat{c_{ik}}$ for each data point x_i to each component k given the model parameters μ_k, Σ_k and α_k (Equation 3.15).

$$\hat{c_{ik}} = \frac{\hat{\alpha}_k \mathcal{N}(x_i \mid \hat{\mu}_k, \hat{\Sigma}_k)}{\sum_k \hat{\alpha}_k \mathcal{N}(x_i \mid \hat{\mu}_k, \hat{\Sigma}_k)} \tag{3.15}$$

- **Second step (M):** In the M-step, the values of μ_k, Σ_k and α_k are updated based on the component assignments $\hat{c}_{ik}$ (Equation 3.16 and 3.17). Where n is the total number of

observations and $(x_i - \hat{\mu}_k)^T$ denotes the transpose of the vector $(x_i - \hat{\mu}_k)$.

$$\hat{\alpha}_k = \sum_i \hat{c}_{ik}/n; \quad \hat{\mu}_k = \sum_i \hat{c}_{ik} x_i / \sum_i \hat{c}_{ik} \tag{3.16}$$

$$\hat{\Sigma}_k = \sum_i \hat{c}_{ik}(x_i - \hat{\mu}_k)(x_i - \hat{\mu}_k)^T / \sum_i \hat{c}_{ik} \tag{3.17}$$

This iterative process repeats until the GMM parameter values do not change anymore or a maximum number of iterations is reached.

Reduction of Model Parameters

Since we want to estimate the empirical distribution of our performance parameter I_{sat} based on the uncertainties in the model parameters, comprehensive sampling is required. As the number of samples required to reach a comparable approximation scales with the number of dimensions of the distribution, having a lower dimensional distribution is beneficial and one should try to decrease the number of dimensions (free parameters) if possible. One method which can be used to reduce the model parameters is Linear Regression. To obtain a lower number of Parameters, we fit a Linear Regression model for each Fitting Parameter using the empirical Parameters e.g. Vth, SS and γ of the EGT model as Inputs. Even though this will introduce some error since it is not the complete set of EGT model parameters, the distribution of the key model parameters can then be expressed only in terms of the empirically extracted EGT model parameters, while the fitting parameters are calculated as a deterministic function of them. For the sake of simplicity and due to the need of the model being expressible in a common simulation languages (Verilog-A or SPICE), we try to reconstruct the fitting parameters as a weighted linear combination of basis functions of the empirical parameters.

In the following we denote the vectors of the empirical parameters V_{th}, SS and γ as vectors x_j of length n (e.g. $n = 95$ for dataset A) where $j = 1, 2, 3$, the matrix $X \in \mathbb{R}^{n \times 3}$ as the matrix containing the vectors x_j as columns and the vector Z as the vector of a fitting parameter that we seek to approximate by the empirical parameters. To increase the expressive power of the model, we generate monomial combinations up to the power of $p \in \mathbb{N}$ of the columns of X to construct a new matrix $\Phi_p(X)$ containing the set of all vectors of monomial combinations of the column vectors of X up to degree p.

As increasing p increases the number of basis functions, and would thus almost always guarantee a better fit of the model $f_{w,p}(X) = \Phi_p(X)w$, we use a Test-Train Split to evaluate the overall quality of the Regression model later on. Additionally, since using polynomial basis functions for $p = 2$ already requires 10 coefficients, we regularize the coefficient vector w by including its weighted L1-norm in the optimization problem. Given a suitable regularization weight λ, this should yield a sparse coefficient vector w. The resulting minimization problem is given by Equation 3.18. This procedure is also known as L1-penalized Linear Regression or LASSO (Least Absolute Shrinkage and Selection Operator) [162] solved using [163].

$$\min_w \quad ||f_{w,p}(X) - Z||_2^2 + \lambda ||w||_1 \tag{3.18}$$

Since the values of p (highest polynomial degree) and λ (strength of the regularization factor) can be freely chosen but have a high impact on the resulting model, we solve the problem for a range of p and λ values and evaluate the results in a 10-fold Cross-Validation. The final model is chosen by selecting the model with the lowest average fitting error (i.e. $||f_{w,p}(X) - Z||_2^2$) on all folds. This procedure is commonly referred to as Grid-Search and is often used to find appropriate values for parameters which are not part of the main optimization procedure like p and λ. For measurements of a fitting parameter i.e. Z equals to the vector containing the

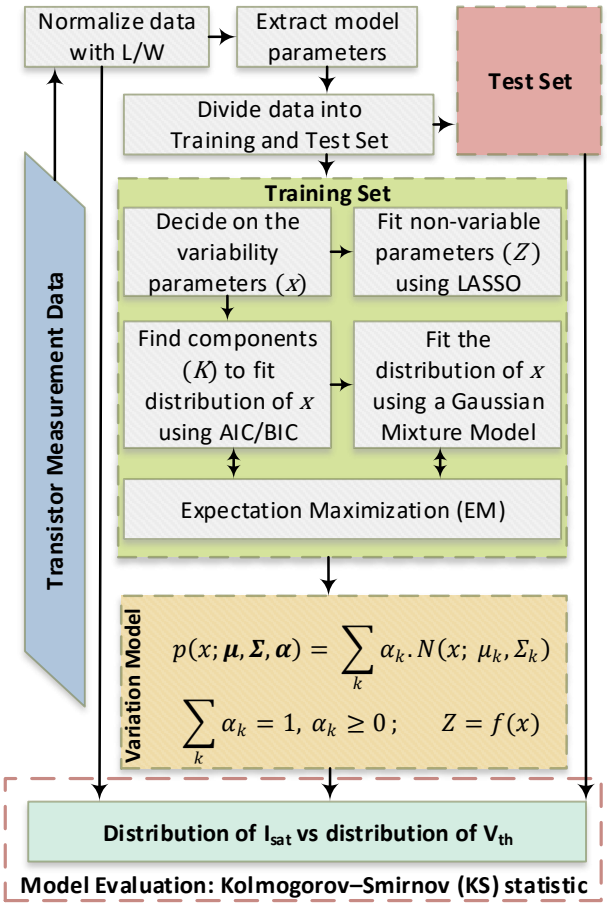


Figure 3.4: The complete modeling flow to model process variations in printed transistors.

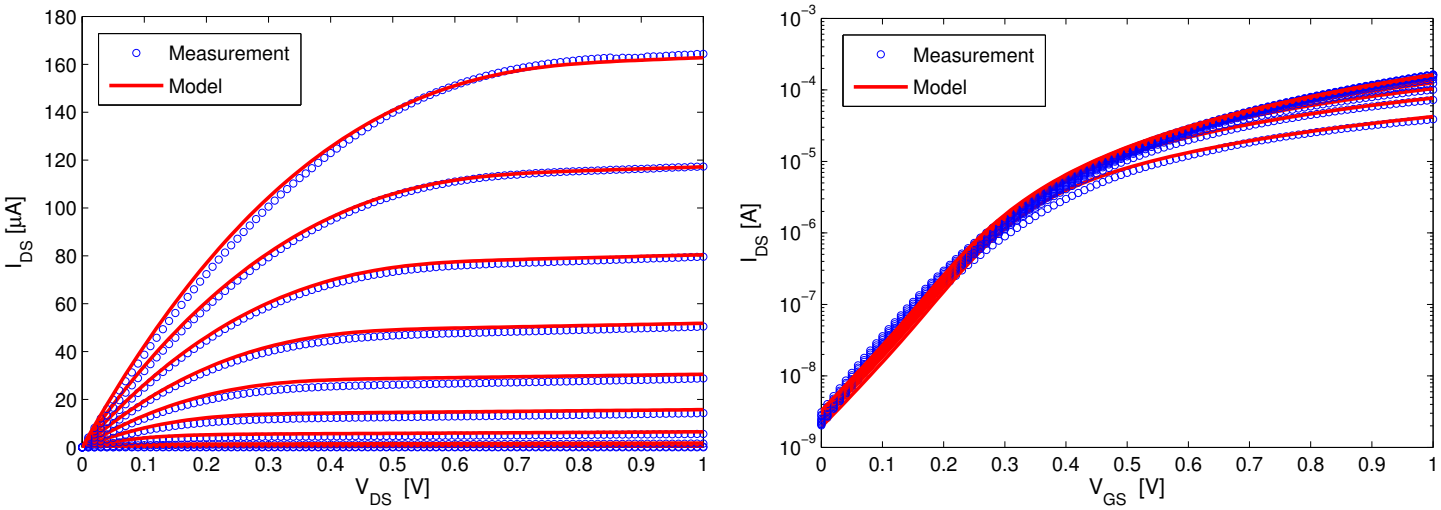
measurements of f_2, the aforementioned procedure suggested $p = 2, \lambda = 0.01$ and 5 coefficients (w).

Variability Modeling Procedure

The complete modeling flow of the proposed methodology is shown in Figure 3.4. The variability modeling data is prepared by extracting all EGT model parameters as defined in Section 3.3. Before extracting the parameters, the measurement data should be normalized by scaling with the channel geometry of the transistor $(\frac{W}{L})$. The extraction of the variability model parameters are defined in the following steps:

Step 1: First, the model parameters are divided into a set $\boldsymbol{X}$ of variation parameters (x_j) and a set $\boldsymbol{Z}$ of dependent parameters. Both sets contain vectors of length n, where n is the number of measurements. In our case, set $\boldsymbol{X}$ contains V_{th}, SS, γ and f_1 as column vectors x_j, while $\boldsymbol{Z}$ contains only f_2. All EGT model parameters are divided into the train (70%) and test (30%) dataset to avoid any over-fitting.

Step 2: The vectors $x_i \in \mathbb{R}^4$ denoting the row vectors of matrix X, which contains the elements of $\boldsymbol{X}$ as columns, are measurements of the empirical parameters of one transistor. Their distribution is approximated using GMM with a suitable number of components. The number of components is selected by sweeping k within a certain range and fitting the distribution of



(a) (b)

Figure 3.5: Measurement and model generated (a) Output and (b) Transfer curves using proposed method.

x_i for each value of k. The best model is selected based on indirect test error estimation using AIC or BIC.

Step 3: Next, the values for the elements of $\boldsymbol{Z}$ are approximated using LASSO regression. The values of p and λ are selected using Grid-Search. The LASSO regression returns the polynomial equations for the elements of $\boldsymbol{Z}$ as functions of x_j.

The extracted GMM parameters are then used to run the Monte Carlo simulation for the EGT. Although the modeling flow is explained for the EGT model it is not limited to any specific technology. The proposed general modeling flow can be used to model the variability in any new technology which is under development containing empirical and fitting parameters.

3.5 Results and Discussions

3.5.1 Experimental Setup

Nominal Model

We prepared an n-channel top-gate EGT on a glass substrate with channel width (W) and length (L) of 100 μm and 40 μm, respectively. First, indium tin oxide (ITO) is sputtered on a glass substrate and then structured using e-beam lithography. A Precursor-derived indium oxide semiconductor (In_2O_3) is then printed between source and drain electrodes and annealed at 400 °C. On top of that, a composite solid polymer electrolyte (CSPE) was printed and dried under ambient conditions. Finally, a conductive polymer (PEDOT:PSS) is printed over the CSPE covering the complete channel region. All materials are printed using a Dimatix DMP-2831 ink-jet printer. Finally the EGT is electrically characterized by measuring the output and transfer characteristics for different voltage ranges. Detailed information on device structure, fabrication and characterization of devices is given in sub-section 2.2.2. All model parameters are extracted from measurement data by implementing the proposed method as a python script. The transistor model is then written in a Verilog-A language to run device and circuit level simulations. Moreover, we use 95 printed transistors measurement data to develop models and see how accurately this method can model transistor behavior under process variation. The

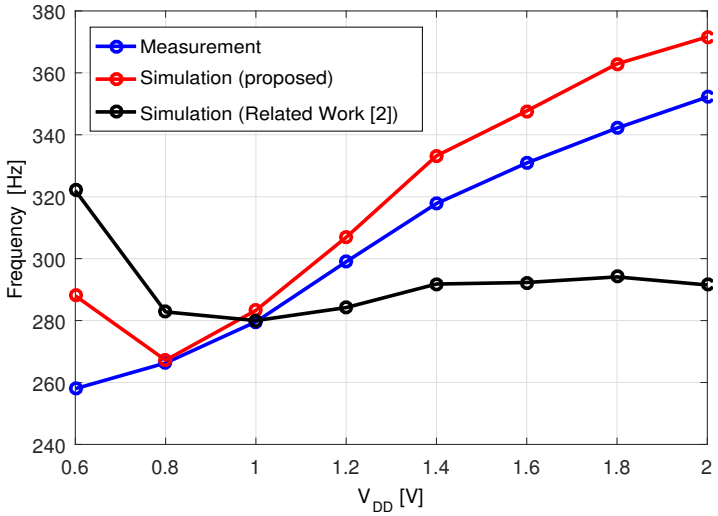


Figure 3.6: Comparison of measured and simulated 3-stage ring-oscillator frequency.

cadence virtuoso design environment, with in-house built design kit [164], is used for the circuit design and simulation.

Variability Model

We printed two-sets of EGTs, with different channel geometries, to capture performance variations on top of the process variations. The first set has 95 top-gate EGTs with $\frac{W}{L} = \frac{100\mu m}{40\mu m}$ and the second set has 88 EGTs with fixed channel length ($L = 40\mu m$) and multiple channel widths ($W = 200, 400, 600$ and $800\mu m$). The devices are characterized at room temperature (23 °C) and fixed humidity level (50%) to minimize the environmental effects. The variability model parameters are written as a statistical block which is used by the EGT DC model for the Monte Carlo simulation.

3.5.2 DC Model Results

Device Simulation Results

Our proposed modeling method leads to very accurate modeling of EGT (shown in Figure 3.5). To compare the fitting quality, we calculate the RRMSE for the proposed and the state-of-the-art methodology [2]. The RRMSE for the transfer and output curves, for different V_{GS}

Table 3.1: RRMSE for proposed and the state-of-the-art model [2]

Output Curves			Transfer Curves		
V_{GS} [V]	Proposed Method	Related Work [2]	V_{DS} [V]	Proposed Method	Related Work [2]
0.0	11.0%	37.9%	0.0	92.5%	92.5%
0.1	19.4%	49.6%	0.1	12.3%	33.8%
0.2	16.2%	45.6%	0.2	10.8%	28.2%
0.3	9.69%	24.3%	0.3	10.7%	26.1%
0.4	19.2%	19.7%	0.4	10.7%	23.3%
0.5	13.7%	11.8%	0.5	10.4%	20.6%
0.6	8.70%	7.00%	0.6	10.2%	17.8%
0.7	4.20%	3.50%	0.7	9.97%	15.0%
0.8	2.15%	2.50%	0.8	9.50%	12.1%
0.9	1.27%	1.90%	0.9	9.18%	10.0%
1.0	2.12%	1.30%	1.0	8.72%	8.30%
Overall	9.82%	18.6%	Overall	17.7%	26.2%

and V_{DS} values, is shown in Table 3.1. Even-though the RRMSE for the previous modeling approach is slightly better for the higher voltage ranges but the overall error for our proposed method is lower.

To verify modeling accuracy of proposed method, we automated the modeling flow to extract parameters for 95 printed transistor measurements. An RRMSE threshold for characteristics curves is defined for accuracy. A model is considered acceptable if the RRMSE for output curve is below 50% and 10% for $V_{GS} \leq V_{th}$ and $V_{GS} > V_{th}$, respectively. Also, RRMSE for transfer curve is below 100% and 50% for $V_{GS} \leq V_{TH}$ and $V_{GS} > V_{TH}$, respectively. Since RRMSE for lower voltage values is high because of very small current values, we divided output and transfer curves in two different regions and defined their thresholds separately. Our proposed method can efficiently model at least 83% transistors. However, the state-of-the-art method can model only 52% transistors.

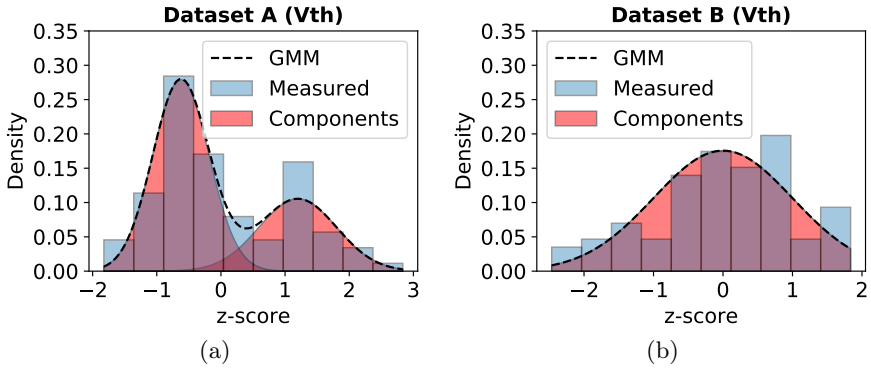
Circuit Simulation Results

For analysis of circuit level simulation, we compare the oscillation frequency of a printed 3-stage ring oscillator obtained using simulation based on the proposed model with the actual measurement results. In the simulation model, an RC network is added to each stage of ring-oscillator circuit design to account for the switching resistance (R_{SW}) and the capacitance (C_{SW}). The R_{SW} and C_{SW} are extracted based on the measurements as described in [37]. The simulation results for different supply voltages are shown in Figure 3.6. We observe maximum of 11% error for very low supply voltage and for $V_{DD} > 0.6V$, the maximum error is around 6%. The results shows that proposed model can be used for the accurate circuit level simulation of printed circuits for different supply voltages.

3.5.3 Variability Model Results

Device Simulation Results

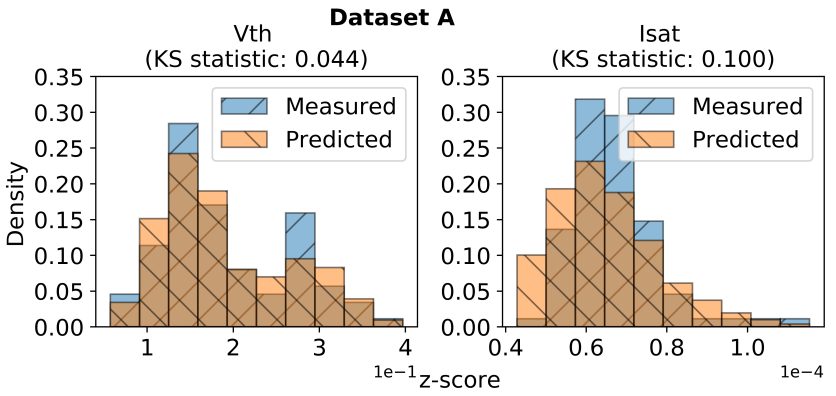
The distribution of the parameters was modeled for both datasets using the proposed approach. Our methodology suggested two components for dataset A and one component for dataset B (based on AIC/BIC). The flexibility of our approach can be seen in Figure 3.7, where the distribution of V_{th} is modeled using a different number of components for each dataset. Next, we run 5000 Monte Carlo device level simulations and evaluated the model performance



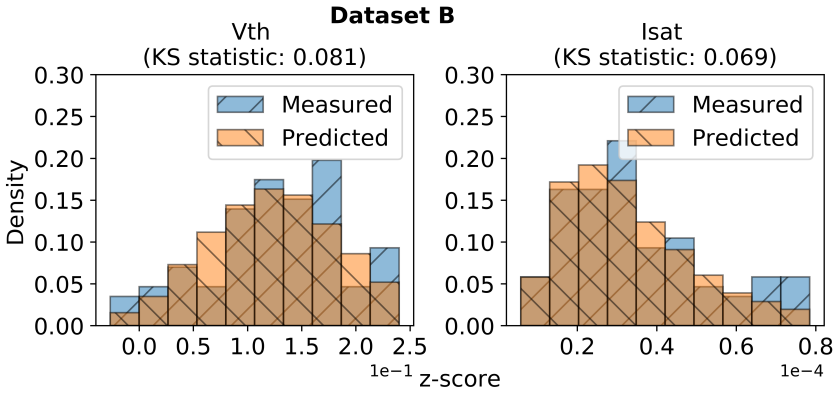
(a) (b)

Figure 3.7: The threshold voltage (V_{th}) z-score distribution modeled using the proposed method (a) Dataset A (95 samples) approximated with two components and (b) Dataset B (88 samples) with one component.

by comparing the estimation of EGT performance parameters (i.e. I_{sat} and V_{th}) from the



(a)

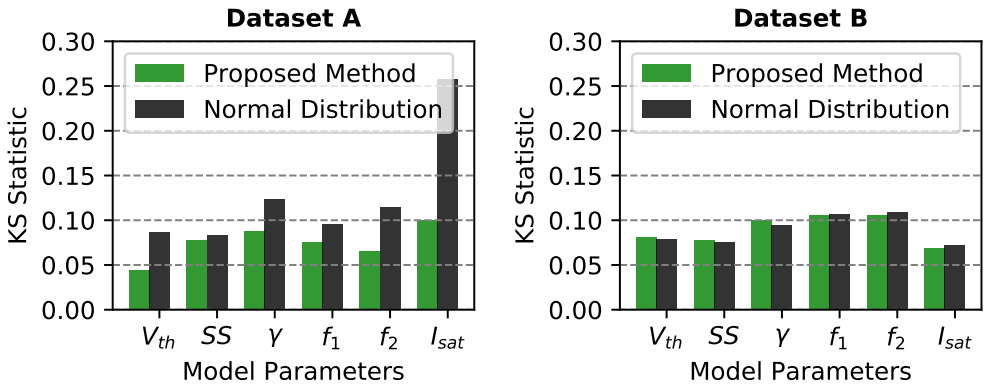


(b)

Figure 3.8: The measured and model-generated prediction of V_{th} and I_{sat} (extracted at $V_{GS} = 1V$) for both datasets. The x-axis shows the z-score and the y-axis displays the relative densities of the respective values. The KS statistic value represent the statistical distance between the measured and model generated predictions (5000 samples). The KS statistic range is between 0 to 1. In our case the highest value is 0.1 (for dataset A I_{sat}), which means that the distribution of the measured and the model generated data have an estimated maximum distance of just 0.1.

measurements and the model (shown in Figure 3.8). It can be seen that the model-generated densities for both parameters matches well with the measurement data which is also reflected in the low values for the KS statistic of the fit.

For further evaluation, the EGT model parameters are jointly estimated using a Gaussian distribution and compared with the proposed method. The KS statistic for the individual model parameters, including I_{sat}, is calculated. The KS statistic between the measured and the modeled distribution (for both datasets) is shown in Figure 3.9. The results show that the proposed method can efficiently model the individual parameter for both datasets. Additionally, for the dataset A, where the proposed method suggested two components, the estimated distributions show a lower statistical distance than the Gaussian distribution for all parameters, while for the dataset B, the performance for both methods is similar. So in cases where just a single component is sufficient, our approach behaves like fitting a Gaussian distribution, while for more complex distributions, the proposed approach can automatically select multiple components to approximate them.

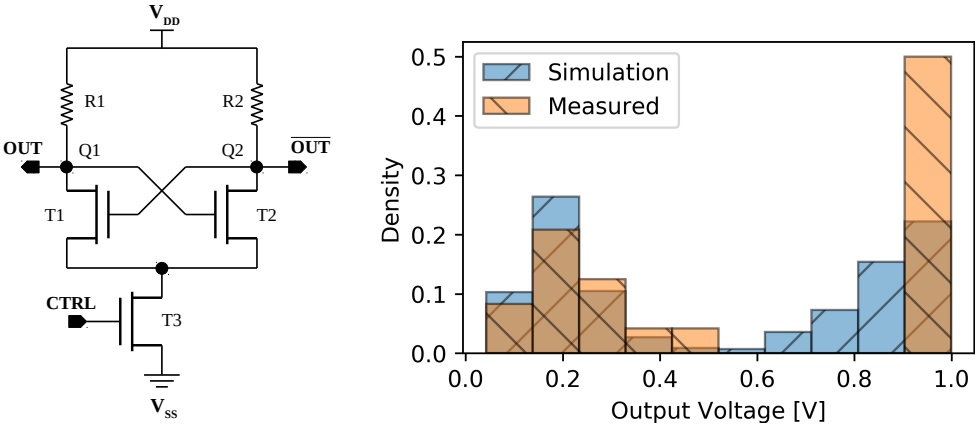


(a) (b)

Figure 3.9: The comparison of the KS statistic for the EGT model parameters with the proposed method and the normal distribution for both datasets.

Circuit Simulation Results

To evaluate the model performance on circuit level, we applied the proposed variability model to predict the behavior of a printed circuit, specifically a Physical Unclonable Function (PUF) [59] as shown in Figure 3.10a. The gate-capacitance setup (as reported in [37, 63]) was incorporated



(a) (b)

Figure 3.10: (a) The schematic of the Physical Unclonable Function (PUF) and (b) The comparison between the Monte Carlo simulation and measured output responses of the printed PUF circuits. The y-axis displays the relative densities of the respective values.

in the EGT model and a Monte Carlo simulation was run 1000 times. The Monte Carlo simulation samples the EGT model parameters from their distributions and runs a simulation with the sampled values. The simulation results are then compared with the measurement data of 12 samples of a printed PUF. The circuit has two output nodes (Out and $\overline{Out}$) which are subject to variations. To increase the sample size from the measurements, the responses of both output nodes are considered for comparison with the simulation results (i.e. 24 measurement samples, 12 for Out, 12 for $\overline{Out}$). It can be seen that the simulation results are similar to the measured output responses of the printed PUF circuits (Figure 3.10b). These results also validate that the variation model can efficiently capture the variations in EGT based circuits.

3.6 Conclusion

Printed electronics opens new doors for the low-cost circuit and system fabrication. At the same time, inkjet-printed devices and circuits are subjected to high variations due to the inherent properties of the printing process, such as dispersion of the liquid on the substrate, droplet jetting oddness, satellite drops and missing droplets. In this chapter, we describe the modeling methodologies for printed devices and circuits. An empirical DC model for the printed electrolyte-gated inorganic transistors is developed by extending and tuning the EKV model to make a good matching in different region of the output and transfer curves. The method is simple, requires few parameters, and is continuous as well as accurate over complete voltage range for this technology. Due to single-segmented model, process variations can be modeled easily. This was not possible with state-of-the-art model because of fixed boundaries for near-threshold region. Furthermore, fitting parameters are extracted using LMA with iterative approach and it can extract all parameters within 100 iterations. The DC model is also validated for circuit level simulation by running simulation for 3-stage ring oscillator. The oscillation frequency is calculated by adding switching capacitance and resistance in the simulation setup and compared to real measurement. The measured and simulated results differ by 4.7% on average, which is 2x more accurate than the state-of-the-art models.

An effective variability modeling approach to model process variations in printed transistors is also presented. Using the proposed method, the variability in two different datasets of printed transistors is efficiently estimated. It is also shown that if model parameters are non-Gaussian distributed, the proposed method can still estimate it with reasonable approximation error. The proposed model uses Gaussian Mixture Model (GMM) to approximate the distribution. It is also shown how the number of required simulations can be reduced by calculating the fitting parameters from empirical model parameters such as V_{th}, SS and γ which are extracted from the DC characteristics of the printed devices. The proposed model was used to run Monte Carlo simulations of printed circuits and the results of the modeled and measured distributions of parameters are in good agreement. These results confirm the accuracy of the EGT models and therefore the proposed methods can be used for design and simulation of EGT based circuits.

4 Placement and Routing Methodology for Additive Manufacturing Circuits

The inkjet-printed electronics technology is a maskless additive manufacturing process. Due to the additive nature of the technology, it is mostly used with a very limited number of (e.g., two) metal layers for routing. One metal layer is typically used for routing and the other metal layer is used for making crossovers at the intersection of routing paths of different nets. The crossover is realized by printing an insulator on the bottom metal layer and then printing conductive material as a crossover forming a stack of metal-insulator-metal. Since the resistance of the crossover-material is higher than the resistance of the normal metal line and introduces parasitic capacitances (due to the metal-insulater-metal stack), it introduces a signal delay on the path. Moreover, the number of crossovers scales with the complexity of the circuit which makes the crossover printing process very time consuming and error prone. In this chapter, we present a crossover-aware placement [56] and routing [3] methodology (COPnR) for additive manufacturing technologies used in printed electronics, such as inkjet printing.

The rest of the chapter is organized as follows. In Section 4.1, the constraints related to crossovers are introduced. Our contribution in placement and routing solution is discussed in detail in Section 4.2. The environmental setup, results and discussion are given in Section 4.3. Finally, the chapter is concluded in Section 4.4.

4.1 Introduction and Motivation

In inkjet-printed electronics, and other additive manufacturing technologies, printed metal layers are limited. Unlike standard silicon-based technologies, *vias* cannot be realized in the inkjet process technology due to the nature of additive manufacturing. Circuits based on such technologies, having few printed components, can be routed with a single metal layer (ITO in our case) without any metal layer crossing (of different nets). However, complex circuits routing have multiple crossing of nets. To isolate the metal layers at the crossing, crossovers are printed (as shown in Figure 4.1e and Figure 4.1f).

Crossovers are printed at the intersection of two different routing nets to isolate them. They are realized by first printing an insulator, such as DMSO (dimethyl sulfoxide) on the bottom metal, e.g., ITO layer, which will electrically isolate it from the top metal-layer. Then, a solution-based conductor such as PEDOT:PSS is printed as a top metal-layer which acts as a crossover at the intersection of two routing nets. The crossover layout and a printed crossover are shown in Figure 4.2a and Figure 4.2b, respectively.

The crossover printing process involves multiple printing steps for each layer. It can lead to non-functional circuits or change in the circuit's electrical characteristics. For example: the typical resistance of the ITO is lower than the PEDOT:PSS [165, 166] and the printing of crossovers increases the parasitic capacitance between the top and bottom metal-layer (due to the metal-insulator-metal stack). Thus every crossover introduces delay in the signal propagation. We printed multiple crossovers and in the worst case a crossover can have a resistance up to $200k\Omega$. Further crossover characterization results are shown in Table 4.1. It has been observed in our crossovers printing experiment that 10 layers of insulator (DMSO) and 16 layers

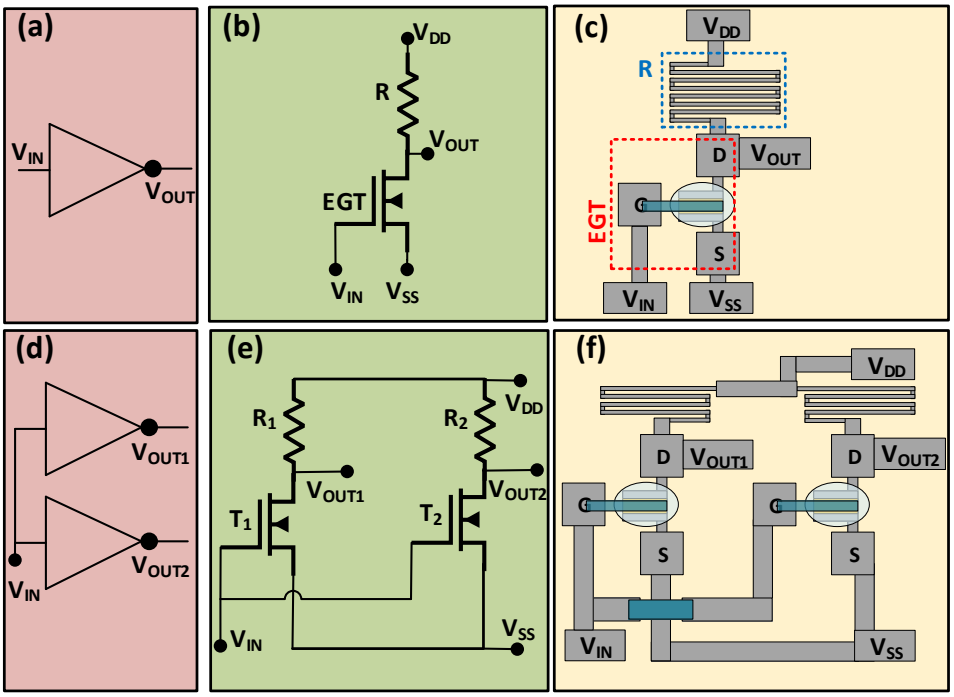


Figure 4.1: (a) Symbolic view of an inverter (b) schematic and (c) layout view of an inverter standard cell based on transistor-resistor logic (d) gate-level, (e) schematic and (f) layout view of two inverters with input tied together. The crossovers on net V_{IN} can be seen in the layout view (f)

of crossover (PEDOT:PSS) gives the best result in terms of isolation and crossover resistance, respectively.

The placement of crossovers is a crucial step in placement and routing flow. There are three different conditions under which the crossover can influence the behavior of a circuit. Consider a simple example with two inverters as shown in Figure 4.1d. The layout (Figure 4.1f) of the circuit require one crossover to completely route the design. Based on the placement of crossover in the routing path, the electrical characteristics of a circuit are effected. Examples of such placements are shown in Figure 4.3. In the first case (schematic: Figure 4.3a, layout: Figure 4.3b) it is shown that if a crossover is between the source terminal of the EGT and the ground (V_{SS}) net, it behaves as an additional passive component between the source terminal of EGT and V_{SS} connection of the logic cell. The voltage drop on a crossover would shift the V_{GS} of the transistor (T_1) and hence, the output (V_{OUT1}) cannot be completely pulled-down

Table 4.1: Characterization results of crossovers with a length = 530μm, Width = 100μm. Printed layers indicate the number of printed layers of insulator and conductor

Testcase	Printed Layers of Insulator	Printed Layers of PEDOT:PSS	Resistance [kΩ] (worst case)
1	3	1	200
2	8	10	14
3	12	10	9
4	20	20	4
5	12	16	1.3

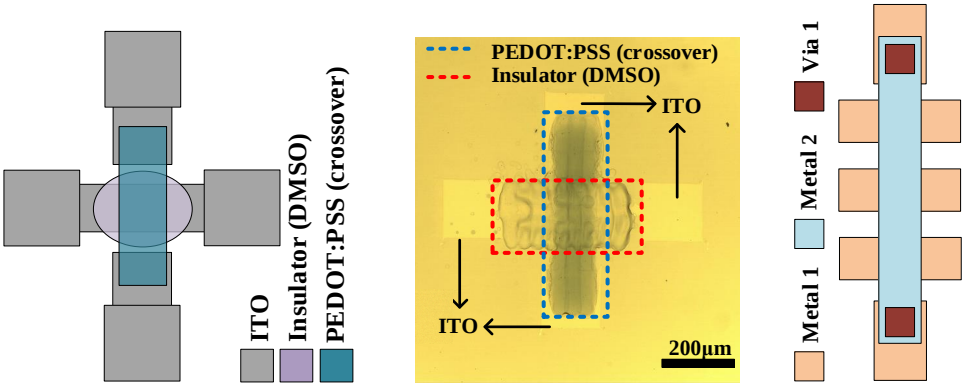


Figure 4.2: (a) The layout of a typical crossover (b) An inkjet-printed crossover connecting the vertical ITO tracks (Length = $530\mu m$, Width = $100\mu m$) (c) Metal-2 utilization in routing in VLSI technology by placing a via between Metal-1 and Metal-2.

(as shown in Figure 4.3c). Thus, any subsequent logic stage would turn on, as logic low for V_{OUT1} is greater than the typical V_{th} of the EGT, and lead to functional failure. This is the most critical situation for the crossover placement.

In the second case (schematic: Figure 4.3d, layout: Figure 4.3e), if the crossover is on the path where gate pins are connected (net V_{IN} in the example), it would introduce delay in the signal propagation. The transient simulation for this configuration is shown in Figure 4.3f where it can be seen that the V_{OUT2} has higher delay compared to V_{OUT1} due to a crossover between the V_{IN} pin and the gate terminal of the T_2. However, for the condition like Figure 4.3g, a crossover on a path where resistor pins are connected is not a critical condition as the crossover resistance can be compensated by subtracting the crossover resistance from a pull-up resistor. The layout for this condition is illustrated in Figure 4.3h and it is shown that when the crossover is placed then pull-up resistor R_1 is smaller, compared to the previous cases Figure 4.3b and Figure 4.3e, by subtracting the crossover resistance from it.

This example has clearly shown that the placement of crossover has a significant impact on the circuit performance and functionality. Due to all these physical design constraints, we proposed a crossover-aware placement and routing methodology. The methodology is validated on multiple benchmark circuits and compared with industrial standard tools. On average, the proposed methodology has 38% and 94% less crossovers and number of failing paths, compared to the industrial placement and routing (PnR) tools, respectively. The proposed flow is suitable for the printed electronics applications where the density of components is far less compared to the VLSI process technology.

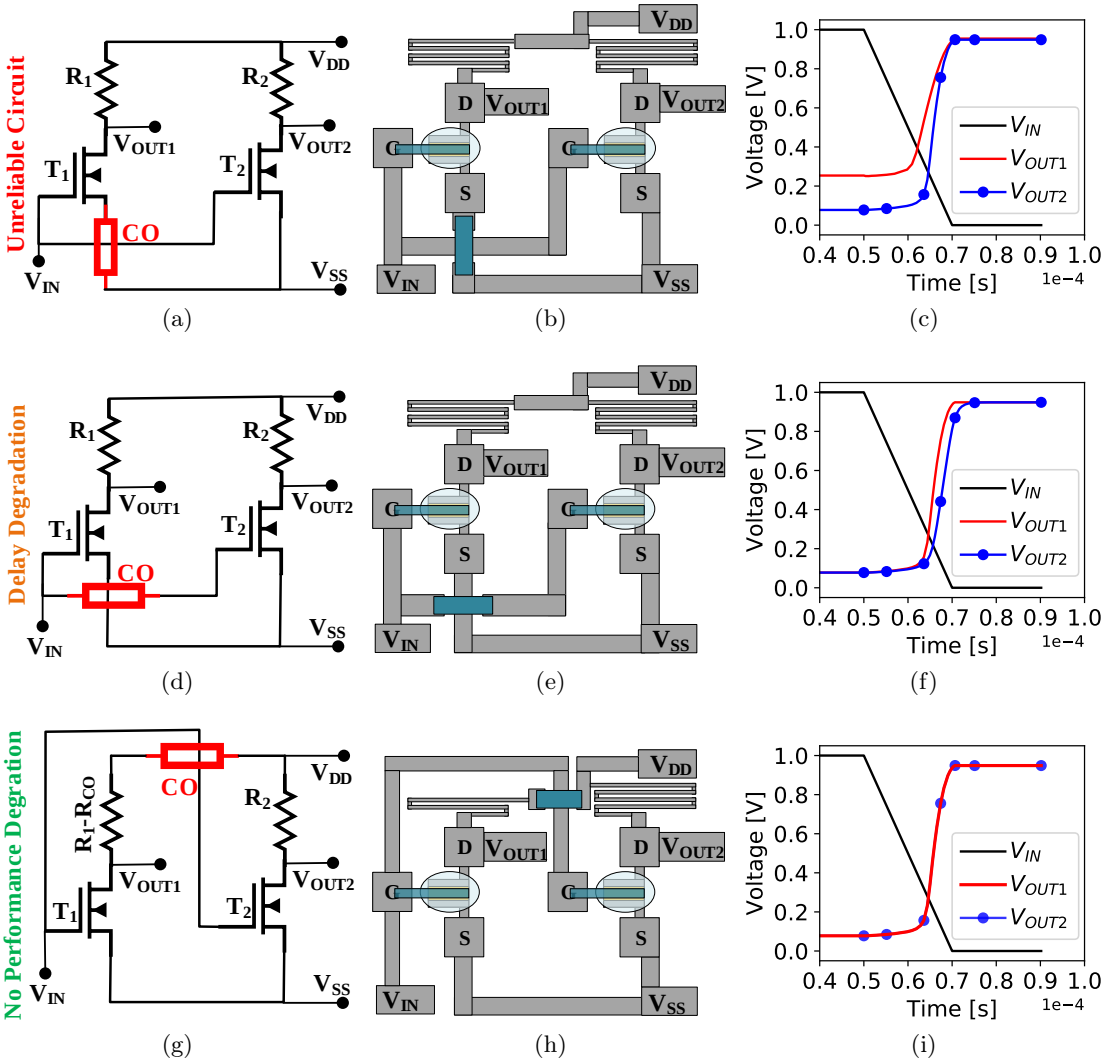


Figure 4.3: The schematic layout and the simulation for the conditions when the crossover is placed on a path that is connected to a source [(a), (b), (c)], gate [(d), (e), (f)] and resistor [(g), (h), (i)] terminal in a standard cell (CO = Crossover).

4.2 Proposed Placement and Routing Solution

Placement and Routing (PnR) plays an important role in any physical design automation flow. A variety of PnR methodologies, including simulated annealing [167, 168], partitioning [169, 170, 171] and analytical [172, 173], were proposed in the past for the standard System on Chip (SOC) physical design flow. Typical objectives for the PnR algorithms include wire length, wire congestion and signal delay [174]. All objectives are encoded in the cost function (objective) for PnR optimization algorithms. For emerging technologies, such as inkjet-printed electronics, the technology specific design constraints are not defined in the design automation tool-set. The existing placement and routing tools can be utilized for inkjet-printed electronics technology based circuits by integrating the physical design constraints of the technology in the design automation tools setup. For example, two metal layers and a *via* is required to fully route a design. Typically, $Metal_1$ (ITO) layer is used for routing until all paths for $Metal_1$ are blocked due to other paths. In that case, a *via* (as crossover) is used to jump

to $Metal_2$ (PEDOT:PSS) to continue routing. All $Metal_2$ paths crossing over $Metal_1$ are actually crossovers for this technology (as depicted in Figure 4.2c). Based on the number of crossings (of $Metal_2$ over $Metal_1$), the number of crossovers will be added to the path which will eventually increase the path delay (as described in Section 4.1). However, these placement [175] and routing [176] tools do not optimize such constraints of crossover and only optimize the general physical design constraints (wire length, delay and area). Hence, the final placement and routing solution from these tools is sub-optimal for inkjet-printed electronics technology in terms of number of crossovers and path delays. We therefore propose a crossover-aware placement and routing methodology by accounting such physical design constraints of crossovers and further optimizing the placement and routing solution.

In the following, we describe our framework for crossover-aware placement and routing of circuit components. To achieve this, a standard-cell placement methodology is developed that is aware of possible crossovers in placement and routing solution of additive manufacturing based circuits. Possible crossovers here refers to an estimation of crossovers if the circuit is modeled as a planar graph. Then, an optimization problem is formulated expressing favourable placement solution given this model. In the next step, a routing scheme based on standard-cell pin-to-pin routing sequences is employed to find a routing solution that minimizes the number of crossovers as well as failing paths (in terms of timing) in a circuit.

4.2.1 Crossover-Aware Placement Solution

Circuit Representation as a Graph

The evaluation of placement quality is only judged by running the detailed-routing methodology (see section 4.2.2). Unfortunately, in the placement optimization process, the detailed-routing would render the computation infeasible since the routing itself is a costly procedure. We therefore implemented the typical method of estimating the placement quality on a graph representation of the problem [177]. The circuit is represented as a graph (G) with transistor-resistor (TR) logic based standard-cells as vertices (V) and wire connection as edges (E). The pins of the standard cells are represented by the sub-vertices (V_p). Every vertex (standard-cell) has three degrees of freedom, i.e. horizontal and vertical position as well as their rotation. A placement solution is therefore encoded as a vector $x \in \mathbb{R}^{3 \cdot n}$ where n is the number of components/cells in the circuit, and the entries of the vector x encode the position and the rotation of the cells in the following way:

$$x = \begin{pmatrix} \text{Vertical position component 1} \\ \text{Horizontal position component 1} \\ \text{Rotation angle component 1} \\ \text{Vertical position component 2} \\ \text{Horizontal position component 2} \\ \text{Rotation angle component 2} \\ \cdots \end{pmatrix} \in \mathbb{R}^{3 \cdot n}$$

The horizontal and vertical positions of a cell represent the mid-point of cell, while the rotation angle is used to encode orientation and pin-positions. The lower and upper bounds for vertical/horizontal placement and rotation angles are set to define the substrate area and valid rotation angles, respectively. The connections between standard-cell pins are represented as linear edges which are used to estimate the wire length for the placement optimization problem. An example of the graph representation of the circuit is shown in Figure 4.4. The placement quality characteristics are extracted from this graph representation which is then used in the placement optimization.

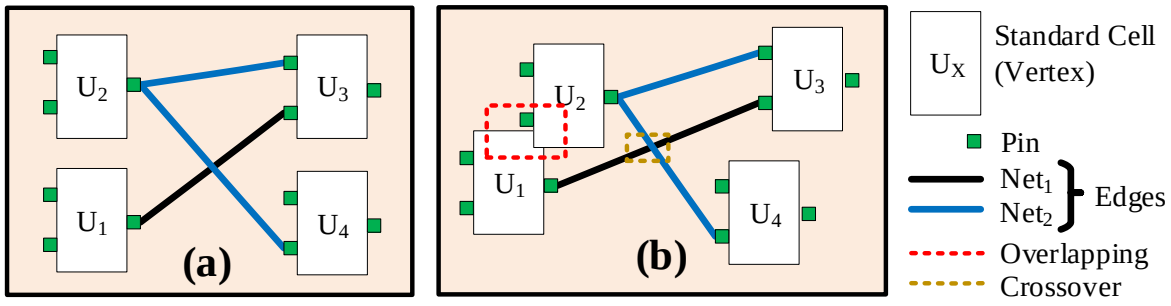


Figure 4.4: (a) The graph representation of a circuit with four standard cells. (b) An example of placement showing overlapping of cells and crossover of nets

Placement Characteristics and Cost Function

To evaluate a possible placement solution of the circuit, we express the favorability of a possible solution. For this, we assign costs to certain unfavourable solution characteristics. In this work, the placement quality is judged based on the following characteristics:

- *Overlapping of standard cells:* This is the most critical problem as it will result in an invalid placement.
- *Number of failing paths:* The failing paths represent the paths in the design that do not meet the timing constraints due to the additional delay introduced by the crossovers on such paths.
- *Crossovers:* The placement of crossovers (as described in section 4.1) as well as the number of crossovers in a placement solution. It reflects one of the contributions of this work.
- *Wire length:* The length of the wires is a standard cost considered in any placement methodology.

The cell-overlapping and crossover conditions are shown in Figure 4.4. To account for these conditions and their criticality, we express them as costs. These costs are defined as cost functions in our framework and they are realized in the following way:

Cell overlapping cost (C_{ol}) is modeled as the exponential distance between the overlapping standard-cells i.e. $exp(-|V_i - V_j|)$. Where V_i and V_j represent placement of two cells. The lower the distance the higher would be the overlapping cost (C_{ol}). This continuous modeling of overlap through coordinate distance should help to guide the later employed optimization procedure.

Failing path cost (C_{fp}) is realized by running a global-route, for the given placement solution, and checking the delay budget. The delay budget represent the delay that a path can have before it violates the timing constraints. It is based on the target clock frequency. Before running the placement flow, the delay budget is extracted for all input to output paths in a circuit with the help of timing information that is reported by Synopsys Design Compiler [178] tool. The crossover delay is modeled based on the measurement data (see section 4.1). During global-route, whenever a crossover is added to any path, crossover delay is subtracted from the delay budget of that path. In the end, the number of failing paths are extracted by checking the delay budget. Paths having negative delay budget (due to many crossovers on that path) are considered as failing paths.

Path cost (C_p) is composed of wire length and crossover characteristics. These characteristics are realized by running global-route, for a given placement, and estimating the routing path between the cell pins (pin-pairs). The wire length is estimated by calculating the euclidean distance between the pin-pairs. In our framework, these paths are modeled as edges and when edges (paths) of different nets cross each other then a crossover cost is added to the path. Additionally, the crossover cost is scaled based on the criticality of the pins connected to the path. For example, comparing the situations like Figure 4.3a and Figure 4.3d the latter is always preferred due to less criticality compared to the former. For the most favorable situation (Figure 4.3g) the scaling factor (α_s) is set to $\alpha_s = 1$ i.e. the penalty of one crossover for every crossover in a path for this situation. While for the most unfavorable situation the α_s is set to very high (in our case, penalty of 10 crossovers for every crossover in a path). The wire length and crossover costs are expressed in terms of each other due to their effect as resistance in the circuit, i.e. a crossover is as bad as a wire with a length that produces a comparable resistance value. For example: the wire (fixed width = $50\mu m$) with a length of approximately $6mm$ produce the same resistance as the typical resistance of a crossover. Typically the wire resistance is $80\Omega/\square$ and based on the wire length the wire resistance (or the wire cost) is calculated. Similarly, based on the number of crossovers in a path, their equivalent resistance is calculated. The path cost is the estimated resistance of the path which is calculated using the wire and crossover cost (Equation 4.1). Where $wire_{res}$ and CO_{res} represent the wire resistance (based on wire length) and crossover resistance, respectively. For a single path (pin-to-pin connection), the path cost is the sum of the wire and crossover resistance. These characteristics are then accumulated in a weighted sum as:

$$C_p = wire_{res} + \alpha_s CO_{res} \tag{4.1}$$

$$C(x) = \alpha_{ol} C_{ol}(x) + \alpha_{fp} C_{fp}(x) + C_p(x) \tag{4.2}$$

The objective is to minimize the cost function $C(x)$ of a placement solution representation $x \in \mathbb{R}^{3.n}$. The individual costs $C_{ol}(x)$, $C_{fp}(x)$ and $C_p(x)$ are thereby calculated as the sum of the costs for x, i.e. $C_{ol}(x)$ considers overlaps for all components/cells, $C_{fp}(x)$ considers all failing paths and $C_p(x)$ evaluates the total path cost given the placement x. where the coefficients α_{ol} and α_{fp} denote the weights encoding their criticality. The more critical the characteristic is, the higher the weight should be compared to the other weights. In this work, the α_{ol} is chosen to be highest since the overlapping of cells is the most critical characteristics as it leads to an infeasible solution (and non-functional circuit). The second critical situation is when the circuit cannot operate at the desired frequency and there are failing paths (timing failure). Thus α_{fp} is chosen as the second-highest weight. The $C_p(x)$ is the least critical cost for the placement characteristics.

All placement characteristics are related to different physical characteristics with individual metrics/units/values and cannot be defined in-terms of each others cost. Also, the choice of separate α for each characteristic may lead to a situation where the most critical cost (overlapping) is smaller than the least critical cost (path cost). We therefore define each α relatively, which also allows the ratio of the costs to scale with circuit complexity. The α_{fp} is chosen as the worst case for path cost i.e. crossover resistance multiply with combination of pin-to-pin paths in the design. The α_{fp} calculation is illustrated in Equation 4.3. The CO_{res} is the crossover resistance and N_{P2P} is the number of pin-to-pin paths in a design. This will ensure that even if there is one failing path and maximum possible path cost, the overall cost for the failing paths is higher than the path cost.

$$\alpha_{fp} = \frac{N_{P2P}(N_{P2P} - 1)}{2} CO_{res} \tag{4.3}$$

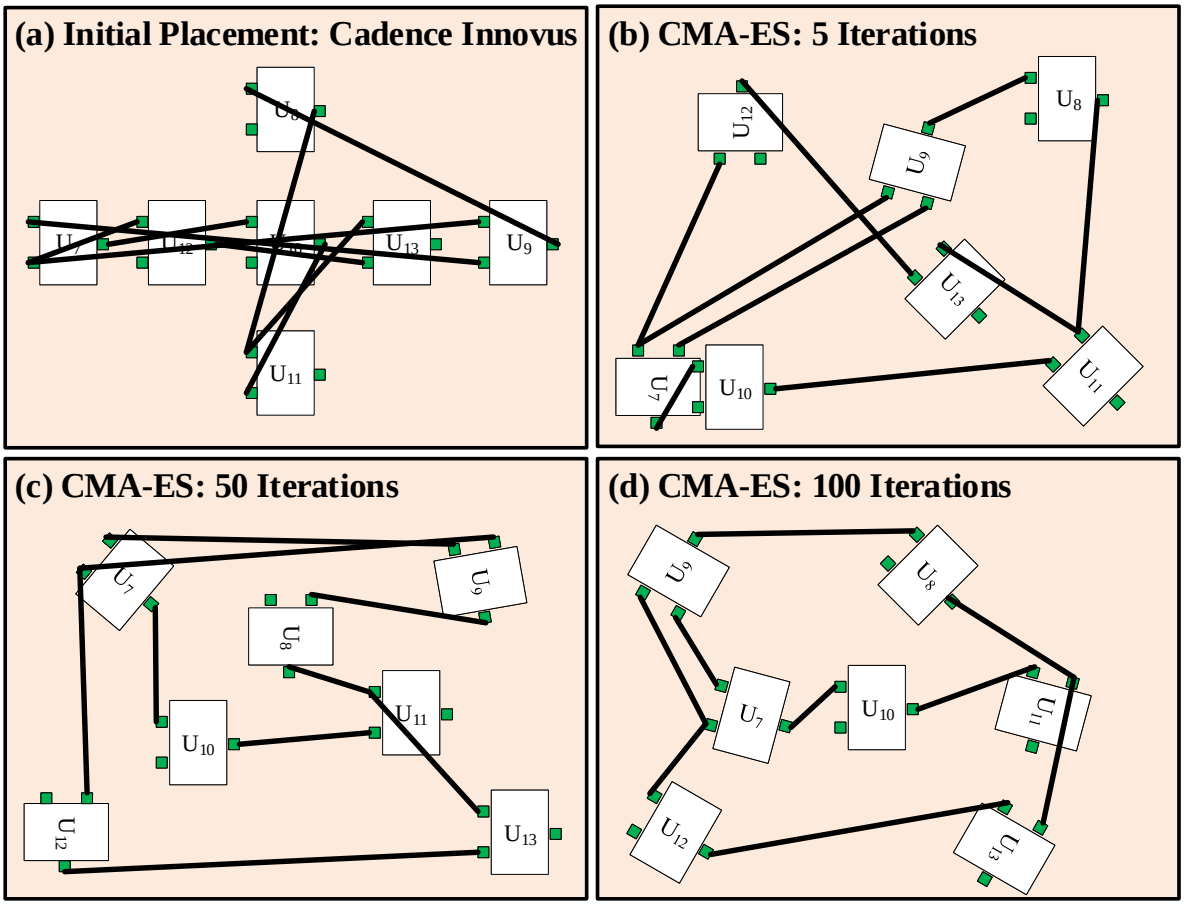


Figure 4.5: Covariance Matrix Adaptation Evolution Strategy (CMA-ES) placement optimization for c17 circuit from ISCAS85 benchmark. (a) The initial placement is read from the cadence innovus tool. Placement optimization using CMA-ES (b) after 5 iterations, (c) after 50 iterations and (d) final solution after 100 iterations with no crossover

Similarly, α_{ol} is chosen as the worst case cost for the failing paths i.e. $\alpha_{ol} = T_p \alpha_{fp} C_{fp}(x)$ where T_p represent the total number of input to output paths in the circuit.

Minimizing the cost function using CMA-ES

Due the non-convex nature of the problem as well as the non-differentiability of the objective produced by the crossover costs, we resort to evolutionary approaches to solve the placement problem. One state-of-the-art evolutionary algorithm to solve optimization problems is Covariance Matrix Adaptation Evolution Strategy (CMA-ES) [179]. CMA-ES works in two main steps which are repeated until either a set budget of function evaluations or a termination criteria is met.

In the first step, a population $\{x_i \in \mathbb{R}^{3n} \mid i = 1, \cdots, \lambda\}_0$ of candidate placement solutions is sampled from a normal distribution $\mathcal{N}(m_0, S_0)$. A placement solution x_i encodes the positions and orientations of all cells in a design with n components as a vector of real numbers, and the parameters $m_0 \in \mathbb{R}^{3n}$ and $S_0 \in \mathbb{R}^{3n \times 3n}$ denote the initial mean vector and the covariance matrix of a normal distribution respectively. The mean vector m_j indicates a possible placement

solution around which similar placement solutions $x_i \in \mathbb{R}^{3n}$ are sampled, while the covariance matrix S_j determines the expected squared deviation from the mean placement solution m_j in iteration j. Through sampling solutions around an initial provided m_0 we obtain a set of perturbed placement solutions with different positions and orientations of their components.

In the next step, the placement costs $C(x_i)$ of the sampled candidate solutions $x_i, i = 1, \cdots, \lambda$ are evaluated. Based on the respective placement costs, the candidates x_i are weighted (selection) and combined to update the mean placement vector m_j and the covariance matrix S_j for the next iteration as well as some parameters guiding the optimization process[1]. The concept of the algorithm can thus be summarized as follows:

- Sample and evaluate a population $\{x_i \in \mathbb{R}^{3n} \mid i = 1, \cdots, \lambda\}_j$ of candidate solutions from a normal distribution $\mathcal{N}(m_j, S_j)$.
- Update the parameters m_j and S_j to m_{j+1} and S_{j+1} based on the sampled candidates x_i and their respective placement costs.

Since there is a justified choice for most of the algorithms parameters (including the population size λ) [180], the only parameters of choice that are left to the user are setting the initial mean $m_0 \in \mathbb{R}^{3n}$ and the initial covariance matrix S_0 as $\sigma_0^2 \cdot I$ (with $\sigma_0 \in \mathbb{R}^+$ and I indicates the $3n \times 3n$ identity matrix). The parameter σ_0 can thereby be thought of as the radius in which initial points are sampled around m_0 in the first iteration of the algorithm.

For the initial covariance matrix $S_0 = \sigma_0^2 \cdot I$, we choose σ_0 such that the boundaries of our search space are in range of $3 \cdot \sigma_0$, similar values are also suggested in [180]. The initial mean m_0 will be set as the solution provided by a commercial placement tool such as Cadence Innovus [175] which allows us to utilize the prior knowledge of a possibly already decent solution i.e. no overlapping cells and a reasonable wire length (e.g. see Figure 4.5). To run $CMA-ES$, we use a python implementation provided by the author [181].

4.2.2 Crossover-Aware Routing Solution

The detailed-routing of a circuit is used to generate the final layout of the design. It typically involves three steps [177]. First, the nets are routed one by one based on their criticality. In the second step, rip-up and re-route methodology is applied to the nets that are failed to route (due to routing constraints or violations). This process is repeated until all nets are routed successfully. Finally, inefficiencies from the second step are removed by ripping-up and re-routing all nets in the sequence that lead to the successful routing of all nets. This sequence of nets is defined as the optimum net routing sequence.

In printed electronics technologies, finding the routing sequence of nets is a crucial step. Additionally, there are other technology constraints that make the routing process further complex. For example: the metal layers, in inkjet-printed electronics technology, are only isolated at crossover position and all crossings of metal $i+1$ over metal i are translated as crossovers, as shown in Figure 4.2c. Hence, utilizing any VLSI router would result in sub-optimal results or even non-functional circuits as it is unaware of the crossovers and their placement in the design.

Crossover-Aware Router

The routing methodology can be adjusted for printed electronics technology by integrating the

[1] While these parameters are part of the algorithm, the user is usually not concerned with choosing them when applying the algorithm as justified heuristic choices exist. For details see Figure 6 and Table 1 in [180].

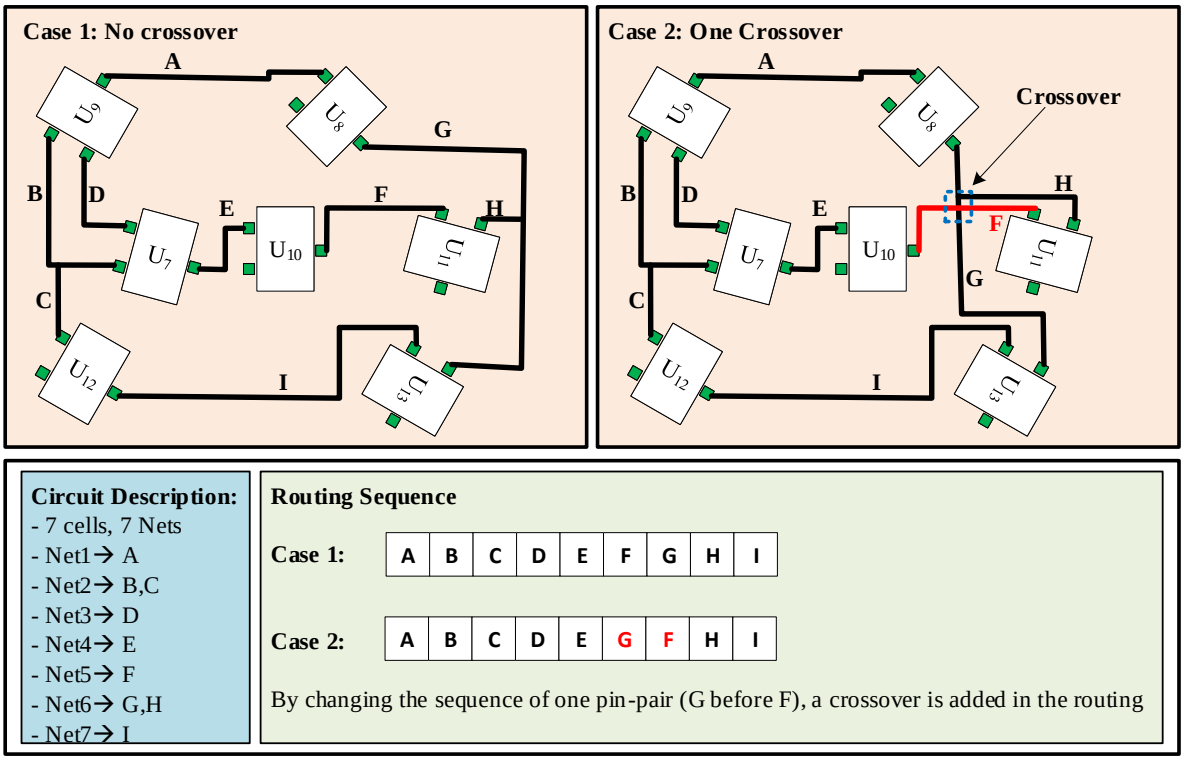


Figure 4.6: An example of detailed routing showing two different routing solutions based on the routing sequence

crossovers cost and technology-specific design constraints in the routing tool. Based on the routing cost, the optimum sequence of routing is extracted. For example: consider the final optimized placement shown in Figure 4.5. Based on the routing sequence there are two solutions. One solution has one crossover and other solution has none (as shown in Figure 4.6). Finding the optimum routing sequence is an NP-complete problem. In our proposed methodology, we utilize the genetic algorithm to find the optimized routing sequence. The genetic algorithm based routing solutions, for limited metal layers, were also proposed in the past [182, 183] but such methodologies have ignored the crossovers placement and their reduction.

Our router is based on the Lee's algorithm [184] with Dijisktra algorithm [185] for the shortest routing path. The routing is preformed in a pin-to-pin routing fashion by dividing nets into pin pairs. This is because the number of paths (from input to output) in a circuit are composed of pin-to-pin paths. Thus delay budget attributes can be easily assigned to each pin-to-pin path. Additionally, based on the criticality of the pins connected to the path, the crossover is placed on a less critical path. The proposed methodology can be utilized for net sequence (instead of pin pairs sequence) without any modification. The genetics algorithm is used to propose the route sequence of pin-pairs. The sequence is labeled as a good or bad sequence based on the routing cost. At the end of the generations, the sequence having the lowest total routing cost would be selected as the optimal routing sequence.

Routing Characteristics and Cost Function

Similar to the placement characteristics, the detailed-routing has three characteristics, i.e. the number of failing paths, the number of crossovers and wire length. These characteristics are

defined in Section 4.2.1. For the detailed routing these characteristics are also encoded as cost functions. The routing cost functions is defined similar to the placement cost function (Equation 4.2) except that there is no overlapping cost. The objective is to minimize the routing cost by trying different routing sequences of pin-pair route. The routing cost guides the genetic algorithm to converge to a valid and optimum routing solution for the given input pin-pairs.

Routing Optimization using Genetic Algorithm

Genetic Algorithms (GA) [186] are evolutionary inspired, heuristic approaches, which can be used to solve general optimization problems. GAs are therefore a suitable choice for finding the optimal pin-to-pin (P2P) routing sequence.

To apply a GA for finding the optimal sequences of pin-to-pin-routing-sequences (P2PS), we map these sequences to *individuals* and formulate *recombination* and *mutation* rules for creating new valid routing sequences out of given ones. We utilize similar rules to [182] for this:

- *Individual* - Is a P2PS $S^i = [s_1^i, s_2^i, \cdots, s_t^i, \cdots, s_n^i]$ of length n, where the elements of $s_t^i \in S^i$ are tuples of pins (u, v) that should be routed at time step t, e.g. $S^1 = [(1,2),(2,3),\cdots]$, $S^2 = [(2,3),(1,2),\cdots]$.
- *Population* - Set of P2PS $\mathbb{P} = \{S^1, \cdots, S^p\} \subset \mathbb{S}$, where p is the population size and $\mathbb{S}$ is the set of all valid sequences.
- *Generation* - Population $\mathbb{P}$ at a specific iteration of the GA.
- *Fitness* - Routing costs $C_R(S^i)$ for a P2PS S^i.
- *(Tournament) Selection* - Selects a P2PS for *recombination* or *mutation* as $\text{argmin}_{S \in \{S^i, S^j\}}\{C_R(S)\}$ where $S^i, S^j \in \mathbb{P}$ are drawn at random from the population.
- *Recombination* - A function $R : \mathbb{S} \times \mathbb{S} \to \mathbb{S}$, where a new sequence $S^k \in \mathbb{S}$ is generated as $S^k = R(S^i, S^j) = [s_1^i, \cdots, s_t^i, s_{t+1}^j, \cdots, s_n^j, s_{t+1}^i, \cdots, s_n^i]$, for $t = \lfloor \frac{n}{2} \rfloor$.
- *Mutation* - A function $M : \mathbb{S} \to \mathbb{S}$, where a new sequence S^k is generated from a sequence $S^i \in \mathbb{P}$ by swapping two random indices s_a^i and s_b^i or reversing the entire sequence.

First, the *fitness* of an *individual* is determined by routing the respective pin-to-pin tuples in the order specified by the *individual* using Dijkstra's algorithm [185], and evaluating the total cost of the resulting routing.

Following this, is the *selection* step, in which *individuals* are chosen for *recombination* and *mutation*. For this, a mechanism called *Tournament Selection* is utilized. In *Tournament Selection*, two random *individuals* of the current *population* are chosen and their *fitness* values are compared. The *individual* with the better *fitness* value is marked for *recombination*. Through this selection mechanism, a good trade-off between exploration and exploitation i.e. evaluating solutions closer to previously found good solutions and investigating rather unexplored parts of the solution space is achieved.

In the recombination step, two *individuals* selected for recombination through *Tournament Selection* are combined to create a new *individual* i.e. candidate solutions by splitting them in the middle and combining the four resulting parts as illustrated in the GA section of Figure 4.7. Since the combined sequence contains every pin-to-pin pair twice, all occurrences but the first

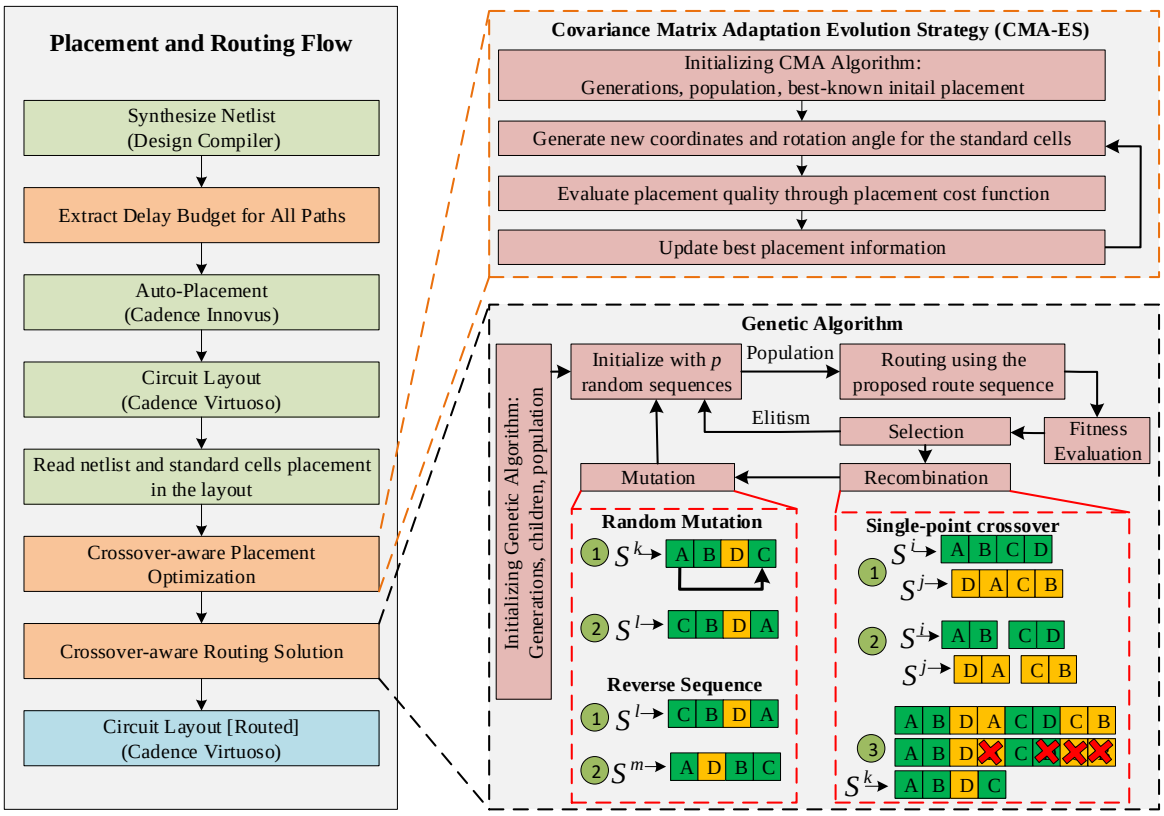


Figure 4.7: The complete placement and routing flow with the detailed explanation of placement and routing optimization. The A, B, C, D, in the routing block, represent the pin tuple/pairs as (u, v) where u and v are the start and end pins, respectively.

one are deleted. Note that after the first three parts, i.e. the beginning-part of the first individual, the beginning-part of the second individual and the end-part of the first individual, the sequence contains all given pin-to-pin pairs already and the end-part of the second individual will always be dismissed as excess occurrences. The newly created *individual* is then added to the candidate-set of the next *generation*.

To additionally increase the variety of newly created *individuals*, we also apply *mutation* operations with a certain probability to all *individuals* of the candidate-set for the next *generation*. If the *mutation* operation is applied to an *individual*, either two random pin-to-pin tuples in the routing sequence are exchanged, or the entire sequence is reversed. The *mutation* operation is illustrated in Figure 4.7. Furthermore, we utilize a mechanism called *elitism* which consists of copying the best *individual* i.e. P2PS with the fewest routing costs to the candidate-set unconditionally. After all these steps are completed, a unique operator is applied to the candidate-set to delete possible duplicate *individuals*. Following this, all *individuals* left over in the candidate-set are copied to the next generation. Note that this might lead to a variable population size throughout different *generations*.

To decrease computational costs for the many routing evaluations of the GA, memorization of routing-sequence-prefixes and their costs can be implemented. Through this, only previously unevaluated sequence-suffixes need to be routed while known sequence-prefixes can be reused. For the implementation of the GA, a custom code was written.

Table 4.2: Number of crossovers comparison between Cadence placement and routing (PnR) tools, GA Router [3] and the proposed methodology (COPnR) (I = ISCAS'85 and E = The EPFL combinational logic benchmark circuits)

Benchmark		# of pin-to-pin	# of Crossovers		
Circuits	# of Gates	Connections	Cadence PnR	GA Router [3]	COPnR
c17^I	7	9	4	1	0
$c432^I$	205	241	840	556	494
$c499^I$	644	685	2729	2038	1862
$c880^I$	428	488	1736	1417	1310
$c1908^I$	519	522	1972	1491	1366
ALU^E	141	148	570	438	402
Int2Float^E	243	256	1340	1219	1145
Decoder^E	616	626	2638	1974	1833
XYRouter^E	169	259	373	258	215

4.3 Results and Discussion

4.3.1 Setup

The design constraints for the technology are integrated in our in-house process design-kit (PDK) [164] of EGT technology. It contains the information of printable layers, valid routing layers, design rules and EGT compact models [54, 55]. The design rules and routing layers are the most critical parameters that need to be accounted during placement and routing (PnR) flow. The minimum spacing and geometry rules of the metal routing paths are defined through design rules. Moreover, the valid routing layers (ITO for routing and PEDOT:PSS for crossover) of the technology are defined for the placer and router tools. Both, design rules and routing layers, are defined in the technology parameters file of the PDK. All such rules and design constraints are considered in our framework during the PnR flow. The compact model of EGT [54] is used for characterizing the standard cells. Three basic standard cells (NOT, 2-input NAND and NOR) are characterized to develop the standard cell library for this technology. Each cell has a spacing of $1mm$ (on each side) to allow enough routing space around the standard-cells. To realize a crossover, a buffer standard cell is characterized that produces comparable delay as a crossover. In this work, only signal routing and "delay degradation" condition (refer Figure 4.3d) is considered when optimizing the path delay and number of crossovers in the PnR flow. The power (V_{DD} and V_{SS}) routing and its constraints are out of the scope of this work and will be addressed in our future work. The benchmark circuits from ISCAS'85 [187] and the EPFL benchmark suite [188] are used to evaluate the proposed methodology. The benchmark circuits that are used in this work have enough number of standard cells to realize any printed electronics related application circuit.

4.3.2 Optimization Flow

The placement and routing optimization are the intermediate steps of the standard design flow. In the first step, the circuits are synthesized using Synopsys Design Compiler [178] to obtain the gate-level netlist. The placement and routing solutions from Cadence Innovus and Virtuoso tools [175, 176] are compared with the proposed methodology. For that purpose, the auto-placement was run using Cadence Innovus tool [175] and then the layout is imported in Cadence Virtuoso layout environment [176]. Next, Virtuoso space-based router (with only two

Table 4.3: Number of Failing Paths comparison between cadence placement and routing (PnR) tools, GA Router [3] and the proposed methodology (COPnR) for the tight delay margin (I = ISCAS'85, E = The EPFL combinational logic benchmark circuits, WNS = Worst Negative Slack, TNS = Total Negative Slack, FP = Failiing Paths)

Benchmark	Cadence PnR			GA Router [3]			COPnR		
Circuits	WNS [s]	TNS [s]	# of FP	WNS [s]	TNS [s]	# of FP	WNS [s]	TNS [s]	# of FP
c17^I	0	0	0	0	0	0	0	0	0
$c432^I$	9.15e-5	1.01e-4	2	0	0	0	0	0	0
$c499^I$	4.31e-3	6.57e-3	11	1.25e-3	1.90e-3	3	1.05e-3	1.19e-3	2
$c880^I$	5.17e-4	8.59e-4	5	0	0	0	0	0	0
$c1908^I$	8.12e-4	1.63e-3	8	1.09e-4	1.09e-4	1	0	0	0
ALU^E	5.39e-5	5.39e-5	1	0	0	0	0	0	0
Int2Float^E	1.32e-4	1.55e-4	3	0	0	0	0	0	0
Decoder^E	3.66e-3	5.29e-3	16	1.21e-3	1.94e-3	4	1.02e-3	1.45e-3	3
XYRouter^E	0	0	0	0	0	0	0	0	0

valid routing metal layers) is used to route the layout. Then, the figure of merits (which are discussed in next sub-section) are extracted from this placement and routing solution. The placement and routing from Cadence tools serves as the baseline for the proposed method.

In the proposed flow, the delay budget for all paths is extracted with the help of timing information reported by Synopsys Design Compiler [178] for the design. The delay budget is extracted for a defined clock. Our framework then imports the layout information (including placement, netlist, logic cells and pins) from the Cadence Virtuoso design environment. The auto-placement solution from Cadence tools is defined as the best known solution to our placement optimization flow. After the placement optimization, cell placement is updated and this new placement is used for the detailed routing flow. Finally, the results from the routing flow are used to extract the figure of merits for the proposed method. The proposed methods are integrated in a single framework to generate the crossover-aware placement and routing solution. The framework is implemented in python language (version 3) and is based on open-source python libraries. We implemented the genetic algorithm while pycma library [181] was used for the placement optimization. Python-igraph library [189] is used for the graph and pin-to-pin routing [189]. The detailed placement and routing flow is shown in Figure 4.7.

4.3.3 Failing Paths Analysis and Discussion

The results are generated for the benchmark circuits by setting parameters for the placement and optimization algorithm. For the placement algorithm, the generations and population-size is set to 100 (as recommended by the author in [181]). The cadence auto-placement solution is used as the best known placement which is helpful in finding the better solution faster, if it exists. The genetic algorithm is run for 1000 generations, with 5 children per iteration and the population size of 50. For the results, number of crossovers and number of failing paths are considered as the figure of merits. The proposed methodology is compared with the Cadence placement and routing solution as well as our GA-based only routing solution (GA router) [3]. For the GA route, no placement optimization was run for the placement of standard cells obtained from cadence innovus and only routing is done as defined in Section 4.2.2.

The results for the number of crossovers are reported in Table 4.2 where it can be seen that the proposed solution has the least number of crossovers compared to the Cadence tools and

Table 4.4: Number of Failing Paths comparison between cadence placement and routing tools (PnR), GA Router [3] and the proposed methodology (COPnR) for the relaxed delay margin (I = ISCAS'85, E = The EPFL combinational logic benchmark circuits, WNS = Worst Negative Slack, TNS = Total Negative Slack, FP = Failiing Paths)

Benchmark	Cadence PnR			GA Router [3]			COPnR		
Circuits	WNS [s]	TNS [s]	# of FP	WNS [s]	TNS [s]	# of FP	WNS [s]	TNS [s]	# of FP
c17^I	0	0	0	0	0	0	0	0	0
$c432^I$	0	0	0	0	0	0	0	0	0
$c499^I$	9.84e-5	1.01e-4	5	1.74e-5	1.74e-5	1	0	0	0
$c880^I$	0	0	0	0	0	0	0	0	0
$c1908^I$	4.25e-5	6.41e-5	2	0	0	0	0	0	0
ALU^E	0	0	0	0	0	0	0	0	0
Int2Float^E	0	0	0	0	0	0	0	0	0
Decoder^E	8.62e-5	9.81e-5	7	1.28e-5	1.28e-5	1	0	0	0
XYRouter^E	0	0	0	0	0	0	0	0	0

only GA router. The fewer number of crossovers has multiple advantages including less process steps, shorter manufacturing time and high manufacturing yield. Additionally, the influence of crossovers on a circuit is also decreased. This is also verified while comparing the number of failing paths for all methodologies.

To extract the number of failing paths, first the clock for every benchmark circuit is set for the synthesized netlist without buffers. Then a delay margin is set so that the paths that cannot finish the operation within the specified clock but do not exceed the delay margin are not considered as failing paths. The failing paths are extracted by adding all crossovers, from placement and routing solution, as buffers in the synthesized netlist. Any path delay higher than the circuit clock plus delay margin would result in timing failure and is recorded as failing path. In this work, two different delay margins are set for the analysis. One has a tight delay margin (20% of the clock) while the other analysis has relaxed delay margin (50% of the clock). This is to show that failing paths are reduced if the delay margin is relaxed.

The failing paths for the tight delay margin condition are reported in Table 4.3. The results for the Cadence tools show that only two benchmark circuits have no failing paths. On the other hand, the GA router has three cases with failing paths while our proposed PnR solution has only two circuits with failing paths. It can also be observed that the number of failing paths increase with the increase in number of crossovers in the design. For the relaxed delay margin condition (see Table 4.4), the failing paths are significantly reduced. There are no failing paths for the proposed PnR solution while for the other two cases, there are some failing paths. This also proves that the failing paths are evitable with crossover-aware placement, which is missing in the GA router.

If power routing is also considered in the proposed PnR flow, then parasitic resistance and capacitance will increase on the power/ground routing paths due to crossovers. This will lead to IR-drop on non-optimal power/ground routing paths. To mitigate this, the power/ground routing can be done on a separate substrate that can be attached to the main substrate (that has all standard cells and signal routing paths). This will connect V_{DD} and V_{SS} pads of the logic gates to the power/ground routing paths thus decreasing the IR-drop caused by the crossovers or long power routing pads. The similar concept has been presented in [190] where two substrates were attached for signal routing. Additionally, the parasitic resistance of the power routing path can be compensated though pull-up resistor of the logic gate to which it

Table 4.5: Runtime comparison between Cadence placement and routing (PnR) tools, GA Router [3] and the proposed methodology (COPnR) (I = ISCAS'85 and E = The EPFL combinational logic benchmark circuits)

Benchmark	Runtime [s]		
Circuits	Cadence PnR	GA Router [3]	COPnR
c17^I	16	50	58
$c432^I$	7242	10812	11085
$c499^I$	25262	39641	40915
$c880^I$	17774	26115	26890
$c1908^I$	21289	34308	35223
ALU^E	3535	5103	5304
Int2Float^E	7989	11121	11458
Decoder^E	26209	40308	41537
XYRouter^E	3933	5718	5955

is connected. This can be achieved by first performing power/ground routing followed by the signal routing. During the signal routing, the impact of power routing (i.e. parasitic resistance and IR-drop) is known for each logic gate in the design. Thus, subtracting the parasitic resistance value from the pull-up resistor value and then placing it in the layout (please see Figure 4.3g and Figure 4.3h) would compensate the additional parasitic resistance.

On average, the proposed PnR solution has 38% fewer crossovers and 94% fewer failing paths (for the tight delay margin) compared to the Cadence tools. However, for the run time, the proposed methodology is slower for both placement and routing optimization compared to the Cadence tools (as reported in Table 4.5). The first reason is that the framework is developed in python language which is much slower than C/C++ in which Cadence tools are written. Secondly, the framework is implemented without applying any run time and software optimizations. The run-time for the proposed methodology can be significantly improved by developing the framework in pure C/C++ language and applying software optimization methodologies, which was out of the scope of this work.

4.4 Conclusion

With the on-going progress on printable materials and improvement in the printed electronics technologies, the standard design flow and design automation methodologies are equally important to have printed functional devices and circuits. In this work, we propose a crossover aware placement and routing (COPnR) methodology for inkjet-printed electronics technology. An evolutionary algorithm is used for the optimization of standard cells placement and genetic algorithm is used for routing. The proposed methodology is compared with the industrial standard PnR tools. On average, the proposed method has 38% fewer crossovers and 94% fewer number of failing paths compared to the industrial PnR tools. These results show that the EDA tools and techniques has to be updated for the constraints of additive manufacturing technologies to ensure proper functionality of printed circuits.

5 Process Design Kit (Kit) for Inkjet-Printed Electronics Technology

Nowadays most of the microelectronic applications are based on silicon CMOS technology. In addition, circuit designers are supported by highly available and defined design flows for developing such silicon based microelectronic systems. On the other hand, Printed Electronics (PE) opens new fields of applications, where silicon based devices are not feasible or too expensive. Unfortunately, standardized design flows similar like for CMOS technologies are rare and mostly specialized for devices based on organic materials in printed technologies. In this chapter we discuss the about the Process Design Kit (PDK) (including its major components) and standard cell library developed for the Electrolyte-Gated Transistor (EGT) technology.

The rest of the chapter is organized as follows. Section 5.1 presents a short introduction of the Process Design Kit (PDK) and Standard Cell Library (SCL). Section 5.2 reviews the available PDKs for printed technologies. Section 5.3 and 5.4 are focused on PDK and SCL development for EGT technology. Finally, Section 5.5 concludes the chapter.

5.1 Introduction and Motivation

Printed circuits face various challenges during the technology development and design cycle time [191, 192]. Such challenges are mitigated by using a well-developed design kit. The design kit plays an important role in the design and test cycle by providing a bridge between circuit design and technology in the design flow. The design flow is chosen based on the technology (Printed Circuit Board or Application Specific Integrated Circuit). The Printed Circuit Board (PCB) design flow is based on circuit designing using discrete components and their associated footprint on the layout board. The PCB design flow is typically used for the prototyping and

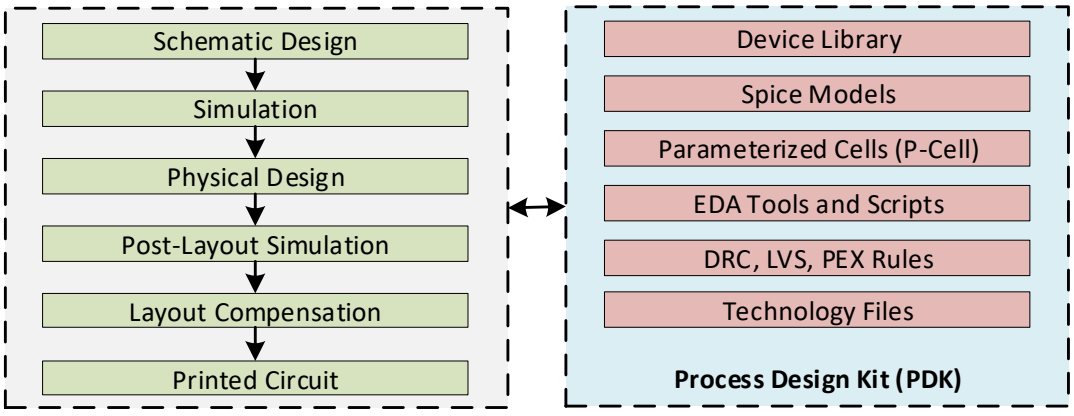


Figure 5.1: Printed electronics design flow including process design kit (PDK) components.

characterization. However, the Application Specific Integrated Circuit (ASIC) design flow is used for circuit design through basic device library and associated compact models. The layout of the device is adjustable based on the parameters of the devices (such as channel geometry area for the transistor or resistance of the resistor). For the inkjet-printed Electrolyte-Gated

Transistor (EGT) technology, we decided to choose full-custom ASIC design flow due to the technology specific design constraints (multiple printed layers, non-discrete components, glass substrate, inkjet printing).

The current microelectronics design flows are chosen as the starting point for EGT design flow. This design flow is enabled by developing a Process Design Kit (PDK). The PDK is used by the designers to design, simulate and very verify the circuit before giving it to the foundry for fabricating chips. That is why an accurate PDK is required to increase the fabrication yield. The PDK divided into multiple components and has variety of data files for the process parameters. Such data files include physical layers definition, parameterized cells (pcells), SPICE models (nominal, corner and statistical), and rule-deck for design rule check (DRC), layout-versus-schematic (LVS) and parasitic extraction (PEX). All of these components are specific for the process technology. They are crucial for the circuit design, verification and test cycle. The design flow for printed electronics is shown in Figure 5.1.

For the digital-design in the ASIC design flow, standard cell libraries (SCL) are used. The input to the design process, in most cases, is the circuit description at the register transfer level (RTL). The final output from the design process is the full chip layout, mostly in the GDSII format. SCL contain primitive cells required for digital design. However, more complex cells that have been specially optimized can also be included. These cells are developed by characterizing the logic functions at the transistor level. A standard cell contains the top-level model for the logic gate with area, delay and power information for different input and output load capacitance. The main purpose of the SCL is to implement the RTL-to-GDS flow using Computer-Aided design (CAD) tools. The SCL is also part of the design kit but sometimes it is provided as a separate module.

We developed a completed design kit (PDK and SCL) for the EGT technology. The PDK is already verified for multiple printed devices and circuits including ring-oscillator [37], physical unclonable function (PUF) [59, 60], true random number generator (TRNG) [61], programmable printed digital circuit [62] and latch [63]. Additionally, the SCL can be used to synthesize any digital circuit design. The developed SCL are also used in the design exploration of printed processors [58]. Further details about the EGT's PDK and SCL are discussed in the next sections.

5.2 Design Kits for Printed Electronics Technologies

In the recent years, printed electronics technology development has gain more and more interest. There are multiple research groups that have developed a variety of EDA tools for printed electronics technologies [38, 193, 194, 139, 110, 39, 9]. All such printed technologies are based

Table 5.1: Design Automation Tools for Printed and Flexible Electronics Technologies

Technology	**Compact Models**	**Statistical Models**	**Process Design Kit (PDK)**	**Standard Cell Library**	**PnR Flow**
EGT [103]	✓	✓	✓	✓	✓
CNT-TFT [38]	✓	×	✓	×	×
OTFT [193]	✓	✓	-	✓	✓
OTFT [194]	✓	-	✓	✓	✓
OTFT [139]	✓	✓	✓	×	×
OTFT [110]	✓	×	×	✓	✓
OTFT [39]	✓	×	✓	×	×
OTFT [9]	✓	×	✓	✓	-

on different materials stack and printed processes. However, most of them are organic channel based printed technologies.

The EGT technology has all components for the analog and digital design flow. The other groups have also contributed to different EDA tools to realize printed and flexible circuits. Notably, authors in [38] have reported the printed devices and circuits based on carbon nanotube (CNT) thin-film transistor (TFT). CNT-TFT is a low voltage technology with a typical supply voltage of $3V$. They developed a PDK which has compact models for their p-type CNT-TFT device as well as process information for the layout tools. Multiple digital and analog circuits based on CNT-TFT are reported in the literature [38]. Additionally, authors in [193] have also worked on models [146], logic gates [195], standard cells and a printed microprocessor [122]. Other researchers have contributed in multiple components of the design flow including model development [194, 139, 110, 39, 9], PDK [194, 139, 39, 9], SCL [194, 110, 9]. The current state of the design automation tools for different printed and flexible electronics technologies are reported in Table 5.1

5.3 Process Design Kit (PDK)

This section discuss about the PDK developed for the inorganic channel based inkjet-printed electrolyte-gated transistor technology. The design kit is compatible with the industrial standard Computer-Aided Design (CAD) and Electronic Design Automation (EDA) tools (such as Cadence Virtuoso, Innovus and Synopsys design compiler). It consist of SPICE compatible models for the inkjet-printed components [54, 55, 57], physical design components including p-cells, layers definition and design verification rules deck [164]. In general, the PDK components are divided into two groups and are discussed in the following subsections.

5.3.1 Front-end components

Front-end components comprise of device symbols, standard cells (discussed in Section 5.4), and models. These components are used to draw schematic and run simulations to assess performance and functionality of the circuit.

Device Symbols

Device symbols are the representation of the components in the schematic design environment. Schematic entry is a technology independent step and require basic devices library for a particular technology node. Each symbol is associated with a particular device model to run simulation. Some of the key parameters (for example geometry of transistor) of electrical model are also accessible through schematic entry. These parameters can be tuned to improve circuit performance.

Compact Models

In order to run electrical simulation, all devices models should be included in the design kit. For realistic performance and power analysis of circuits, three different corner models (fast, typical and slow) for devices are included in design kit. Devices models also contain statistical blocks to run Monte-Carlo simulation, which is essential in printed electronics because of high process variations. Printed devices model are not developed using standard microelectronics devices model sue to slight difference in the electrical characteristics of the devices such as gate-voltage dependent mobility behavior. Hence, electrical simulator should support custom models for the devices. The Verilog-A models for EGT, as presented in the chapter 3, is

```
module EGT_model(d, g, s);

        inout d, g, s;
        electrical d, g, s;
        branch(d, s) vds;
        branch(g, d) vgd;
        branch(g, s) vgs;

        //Channel Geometry
        parameter W=75u, L=40u;

        //Empirical Parameters
        parameter vth = 0.1763;
        parameter S = 12.3591;
        parameter gamma = 2.6983;

        //Fitting Parameters
        parameter f1 = 1.1430e-05;
        parameter f2 = 1.6050;
        parameter f3 = 6.1210;
        parameter f4 = 0.0345;

        //Thermal Voltage = Vt = (K*T)/q
        localparam real Vt = (1.38e-23*300)/1.60e-19;
        //Ideality Factor
        localparam real n = 1/(ln(10)*S*Vt); //ideality factor

        //Other Parameters
        localparam real nf = n/f2;
        localparam real I0 = f1*2*n*pow(Vt,2);
        real Ids, v_s, v_th, v_g, v_d, v_p, i_f, i_r;
    analog begin
                v_s = -(0)/Vt;
                v_th = vth/Vt;
                v_g = V(vgs)/Vt + v_s;
                v_d = V(vds)/Vt + v_s;
                v_p = (v_g - (v_th - f4 * v_d)) / nf;
                i_f = pow(ln(f3+ exp((v_p-v_s)/2)),gamma);
                i_r = pow(ln(f3+ exp((v_p-v_d)/2)),gamma);
                Ids = I0*(i_f - i_r);
                I(vds) <+ W/L * Id;
        end
endmodule
```

Figure 5.2: Verilog-A code for the EGT DC model.

also incorporated in our design environment. Verilog-A code snippet for the EGT DC model is shown in Figure 5.2. Even though we reported DC models in this work, EGT model also contains the capacitance models to enable the transient simulation [57]. The capacitance model was developed by characterizing and modeling the capacitance-voltage (C-V) characteristics of the EGTs. These models are extensively verified with printed devices and circuits.

5.3.2 Back-end components

This group of components contain technology files, rules deck for verification tools and p-cell.

Technology File

Technology files contain the process information for a library, design rules definition, information about layers stack and display resource file that contains the information how the layers should be visible in CAD tools. It also contains foundry specific constraints (such as grid size in layout). The information regarding the routing layers, metal layer resistance and capacitance as well as via definition is also part of the technology files. A snippet of the EGT's technology file with technology layers definition is shown in Figure 5.3. In the same figure, user-defined layers are the name of the technology layers while the abbreviation names are the short names that will be visible in the CAD tools. The color, pattern, and relative position of individual layers are defined through the display resource file (DRF). The DRF tells cadence Virtuoso how layers should be displayed in the layout design environment. It uses a hierarchy of classes to specify display parameters and settings.

Parameterized Cell (pcell)

Parameterized Cells (pcells) are used for the automatic layout generation of devices and circuits to speed-up the design process. They can be coded in programming languages like SKILL

```
;*****************************
; LAYER DEFINITION
;*****************************
layerDefinitions(

techLayers (
; (  LayerName                  Layer#        Abbreviation   )
; (  ---------------            ---------     ----------------  )
; User-Defined Layers;
  (   Indium_Tin_Oxide          0             ITO             )
  (   Indium_Oxide              1             INOX            )
  (   Electrolyte               2             ELEC            )
  (   PEDOT_PSS                 3             PDT_PSS         )
  (   Glass_susbtrate           4             SUB             )
) ;techLayers
```

Figure 5.3: The layers definition block in the technology file for the EGT PDK. The techLayers function defines the user accessible layers for the process technology.

or python and require callback scripts to update the layout in CAD tool. Mostly pcells are developed for the layout view but schematic pcells area also possible. The master pcell has a fix

```
pcellId=pcDefinePCell(
   list(ddGetObj(library) cell "layout")
   ; D= Drain, S=Source, G=Gate
   ;-------------------------------------------------------------
   ; Formal parameters
   ;-------------------------------------------------------------
   (  (W         float   75e-6    ) ;; Channel Width
      (L         float   20e-6    ) ;; Channel Length
   )

   ;-------------------------------------------------------------
   ; Technology parameters
   ;-------------------------------------------------------------
   drainW      = 200   ;; Drain Contact Width
   drainL      = 200   ;; Drain Contact Length
   sourceW     = 200   ;; Source Contact Width
   sourceL     = 200   ;; Source Contact Length
   gateW       = 300   ;; Gate Contact Width
   drainExW    = 50    ;; Drain Extension Width
   sourceExW   = 50    ;; Source Extension Width

   DGSExSep    = 20    ;; G and D/S contacts extension separation
   DGSSep      = 100   ;; G extension and D/S contacts separation
   gateExL     = 100   ;; Gate Extension Length
   ;; G Extension Width
   gateExW     = abs(W + DGSSep - sourceExW - DGSExSep )
   ;; Gate Contact Length
   gateL       = 2*gateExL + 2*DGSSep + 2*drainExW + L
   drainExL    = 2*DGSSep + gateExL  ;; Drain Extension Length
   sourceExL   = drainExL      ;; Source Extension Length
   ;-------------------------------------------------------------
   ; set Layer Names
   ;-------------------------------------------------------------
   ITO         = "ITO"
   Indium_Oxide = "Indium_Oxide"
   Electrolyte = "Electrolyte"
   PEDOT_PSS   = "PEDOT_PSS"
   Substrate   = "SUB"
   TEXT        = "text"

   ;-------------------------------------------------------------
   ; Set design parameters
   ;-------------------------------------------------------------
   sourceLayer = ITO
   drainLayer  = ITO
   gateLayer   = ITO
```

Figure 5.4: The parameterized cell code showing the design and technology parameters.

geometrical shape. The instance of the master pcell is placed and the parameters are modified to update the layout or symbol (for schematic pcell) in the design environment. The EGT technology PDK has pcells for EGT and resistor where channel length/width and resistance can be varied, respectively. The pcell code example with critical design and technology parameters settings is shown in Figure 5.4. When a pcell parameter is changed, the callback script is executed by CAD tool to regenerate layout or schematic symbol based on assigned parameters. Figure 5.5 shows the layout of an EGT and resistor p-cell with different parameter attributes and their respective layouts.

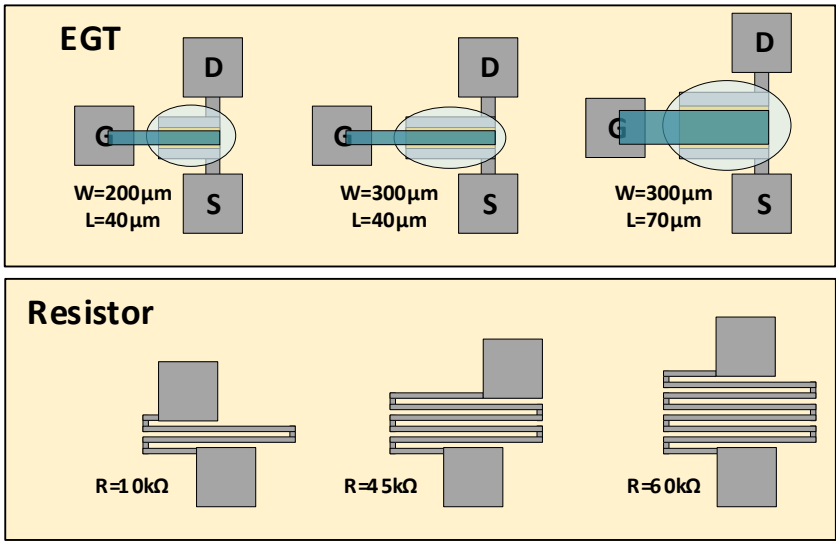


Figure 5.5: Parameterized cell generated layout for EGT and resistor for different geometries (W= channel width, L= channel length, R= resistance).

Verification Rules Deck

The physical verification of the design is based in the rules decks defined for the DRC, LVS and parasitics. These rules play a critical role in eliminating errors from the design as they set the geometric and connectivity restrictions for devices. For example, the critical dimensions and geometries are defined through DRC rules. The user is restricted by these rules to draw layouts according to the process technology and printing/fabrication limit of tools. The layouts are extensively verified through DRC run that all geometries and dimensions comply with the fabrication/printing process limits. Figure 5.6 shows some DRC rules for inorganic

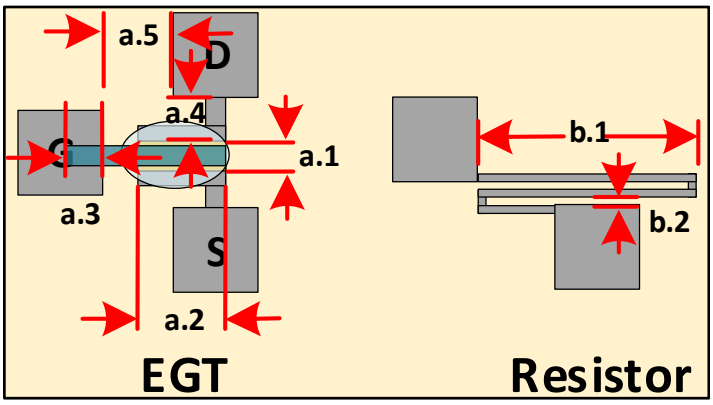


Figure 5.6: Typical design rules for EGT and resistor layout.

channel based inkjet-printed EGT technology and their explanations are given in Table 5.2. For emerging technologies like printed electronics, it is necessary to introduce new set of rules due to nature of the technology and verity of new design constraints.

LVS check is another important verification step. LVS rule deck defines how drawn shapes represent electrical devices and their connections. After drawing the layout of the circuit, LVS is run to verify that the layout is the exact representation of the schematic. If the layout passes the verification process (DRC and LVS check) then it is ready for the further process (parasitic extraction, post-layout simulation).

Table 5.2: Design Rules for Inorganic Printed Electronic Devices

Design Rules	Comments
a.1	Channel length
a.2	Channel width
a.3	Gate electrode width
a.4	Separation between gate-electrode and electrolyte
a.5	Separation between gate-electrode and drain/source-electrode
b.1	Resistance strip length
b.2	Spacing between resistance strip

Another type of rules deck is defined for extraction of parasitics (PEX) from the layout. This step is necessary to estimate the performance of the circuit before fabricating it. Slight change in the electrical characteristics of the circuit, introduced by the parasitic, would lead to low performance or even non-functional circuit. The extracted parasitics are added in the circuit netlist which then represent the layout of the design. After running all verification and extraction flows (and verifying the performance), the design is sent for fabrication/printing. The LVS and PEX steps are shown in Figure 5.7. For the EGT technology, parasitics have not been estimated/extracted from the layout of the printed devices and circuits. For that reason, PEX flow is not integrated in the current version of the PDK.

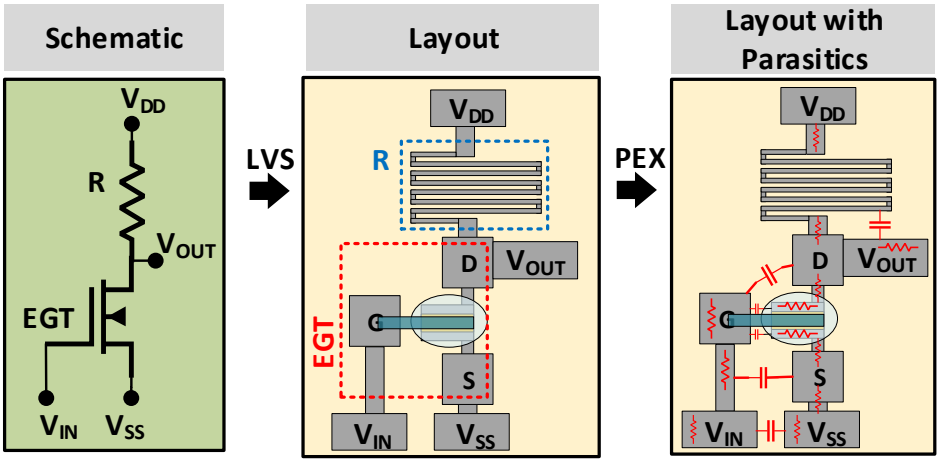


Figure 5.7: The schematic and layout of an inverter verified through LVS check. The layout after the parasitic extraction flow is also shown.

5.4 Standard Cell Library

Standrd cell library is required used to design, synthesis and place and route application-specific integrated circuit (ASIC) designs. In this work, we develop and present standard cell libraries for EGT technology. To the best of our knowledge, this is the first standard cell library for any low voltage printing technology.

In EGT technology, only n-type devices are available as no reliable p-type inkjet-printed EGT has been realized yet [102]. The circuits are hence fabricated in transistor-resistor (TR) logic where the resistor is used for the pull-up logic while EGT is used for the pull-down logic. The schematic of an inverter based on such TR logic is shown in Figure 5.7. We developed a complete EGT standard cell library by characterizing combinational and sequential logic gates

```
//Simulator Settings
simulator lang=spectre
global VSS VDD

//NAND Logic Gate
subckt NAND2X1 A B Y
R0 (Y VDD) res_model R=50k
M0 (Y A int_x) EGT_model W=200u L=40u
M1 (int_x B VSS) EGT_model W=200u L=40u
ends NAND2X1

//NOT Logic Gate
subckt INVX1 A Y
R0 (Y VDD) res_model R=50k
M0 (Y A VSS) EGT_model W=200u L=40u
ends INVX1

//NOR Logic Gate
subckt NOR2X1 A B Y
R0 (Y VDD) res_model R=50k
M0 (Y A VSS) EGT_model W=200u L=40u
M1 (Y B VSS) EGT_model W=200u L=40u
ends NOR2X1
```

Figure 5.8: SPICE sub-circuit netlist used for the characterization of NAND. NOT and NOR standard cells. EGT_model and res_model are the compact models of EGT and ITO-based resistor, respectively.

with different input signal slew rates and for different output load capacitances. The cells are first simulated to ensure proper functionality and timing. The EGT compact models were enhanced by adding measurement proven capacitance values (measured from the printed EGTs) - [196, 57] describe how to extract and accurately model the gate-capacitance using measured data. These models are then used to simulate and characterize standard cells. The SPICE netlist used for the characterization of NAND, NOR and NOT gates is given in Figure 5.8. The delay and power values of the characterized cells are verified with measured delay and power values of the printed logic circuits, whenever applicable. The delay is measured when output signal has crossed 50% V_{DD} value. All rise/fall times are 30% to 70% V_{DD} values. The libraries are developed for the supply voltage range of 0.6 V to 2.0 V. Additionally, the layout of the gates were drawn and added in the PDK. The schematic, layout and inkjet-printed design of NAND, NOR and NOT standard cells are shown in Figure 5.9.

Table 5.3: EGT standard cells characteristics at $V_{DD} = 1\,\text{V}$

Cell Name	**Area** [mm^2]	**Energy** [nJ]	**Rise Delay** [µs]	**Fall Delay** [µs]
INVX1	0.224	9.8	1212	174
NAND2X1	0.247	12.1	1557	986
NOR2X1	0.399	580	1830	904
AND2X1	0.433	584.1	2101	1284
OR2X1	0.563	603.8	2040	1271
XOR2X1	1.042	1460.2	5474	4982
XNOR2X1	1.347	1510.3	6159	3420
TSBUFX1	0.446	597	2553	1004
LATCHX1	0.586	624	2643	942
DFFX1	1.413	2360	6149	3923
DFFNRX1	2.776	3941	5935	4453

The EGT standard-cell library contains NOT (INVX1), 2-input NAND (NAND2X1), 2-input NOR (NOR2X1), 2-input AND (AND2X1), 2-input OR (OR2X1), 2-input XOR (XOR2X1), 2-input XNOR (XNOR2X1), SR-Latch (LATCHX1), D Flip-Flop (DFFX1), D Flip-Flop with asynchronous reset (DFFNRX1) and tri-state buffer (TSBUFX1) cells. Typical characteristics of all logic gates are reported in the Table 5.3.

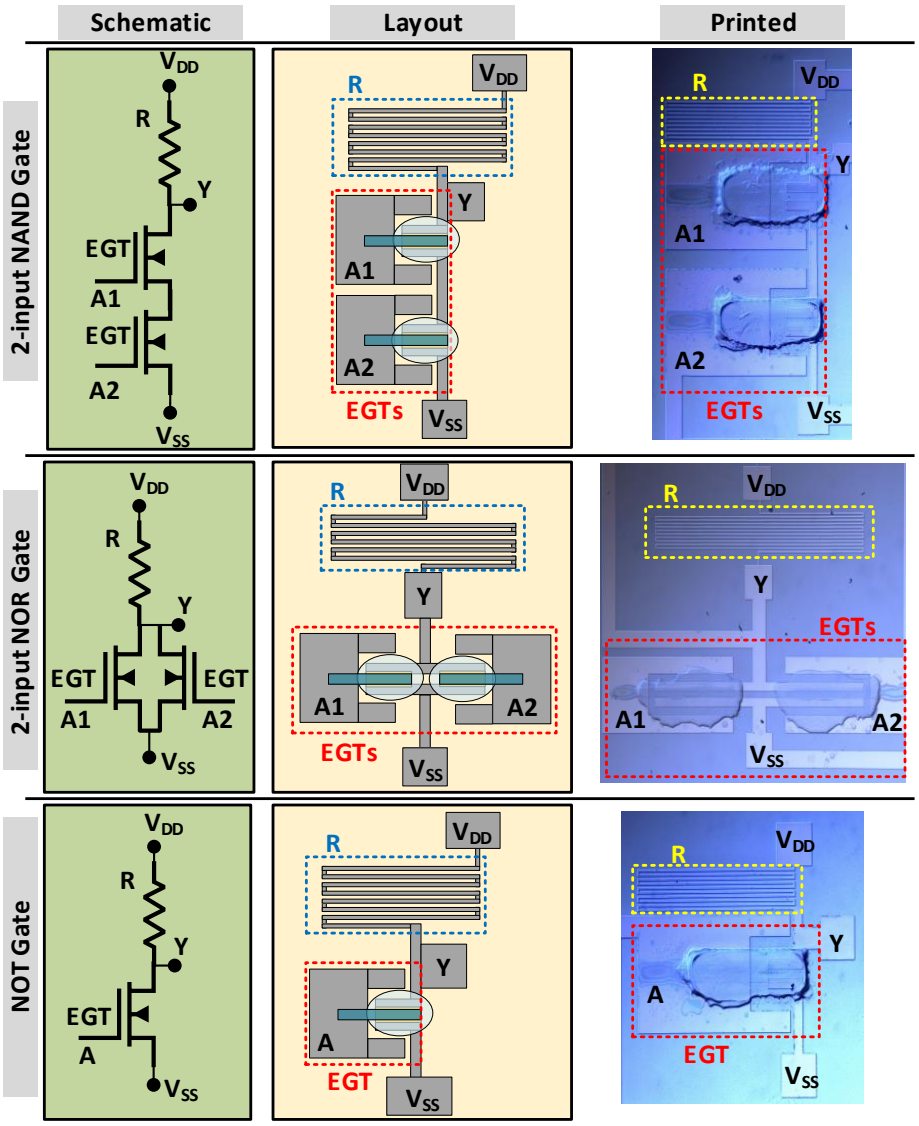


Figure 5.9: EGT based NAND, NOR and NOT logic gates schematic, layout and inkjet-printed design.

5.5 Conclusion

In CMOS technologies, process design kits (PDK) turned out to be a useful and powerful tool to create reliable circuits and systems. In this regard we developed a PDK with accurate compact models to facilitate the design of complex circuits in the inkjet-printed EGT technology. The models are able to mimic the behavior of printed devices. Parameterized cells for EGT and indium tin oxide (ITO) based resistors are included into the PDK. Furthermore, we added the rules deck for the design verification flows. We present standard cell libraries for EGT technology. To the best of our knowledge, these are the first synthesis and physical design ready standard cell libraries for any low voltage printing technology. We believe that our technology in combination with the presented design flow can pave the way for fabricating reliable, low power applications in the fields of printed electronics. In future, more components like diodes and electrolyte-capacitor will be added to the PDK to increase the number of components in the device library. To use flexible substrates, studies will be made on the room temperature for all-printed system.

6 Conclusion and Outlook

Printed Electronics (PE) technologies attract a lot of attention due to their promising features including low-cost manufacturing, maskless and on-demand printing on flexible substrates. PE holds the promise to meet the needs of disposable, conformal, and ultra-low cost applications and hence, is suitable for sensors, radio-frequency identification (RFID) tags, Internet of things (IoT), smart homes and soft robotics. Printable devices and circuits are realized by depositing multiple materials on substrates but the processing steps and productions costs are much less compared to the silicon counterparts. Printed electronics do not compete with silicon-based electronics in terms of integration density, area and performance. Similarly, the feature size tends to be several microns. However, they meet the area and performance requirements for a variety of applications. Recent printing technologies have low enough supply voltage that corresponding electronics can be battery-powered. In the last decade, a variety of printed components, circuits and systems have been demonstrated.

Even though printing technologies have a lot of attractive features, they suffer from new challenges that were not faced by the technology developers in the silicon-based technologies. The major challenges are related the fluid dynamics of the inks/pastes and printing inaccuracies. These challenges lead the process variation in printing technologies resulting in low production yield. These complex properties of the printing process should be modeled and integrated in to the design environment for the scaling and wide adoption of such printing technologies. Therefore, new modeling approaches and design methodologies are required to overcome such challenges.

6.1 Conclusions

In this thesis we address the variability and design flow challenges in inkjet-printed electronic technology. The methodologies in this thesis are proposed for the inkjet-printed electrolyte-gated transistor (EGT) technology with inorganic channel material. However, these methodologies are applicable to any similar additive printing technology. The methodologies and tools in this thesis are proposed for different steps of the design flow ranging from modeling to the physical design. The contributions of thesis are as follow.

- Inkjet-printed devices and circuits are subjected to high variations due to the inherent properties of the printing processes, such as dispersion of the liquid on the substrate, droplet jetting oddness, satellite drops and missing droplets. In Chapter 3, we describe the modeling methodologies for printed devices and circuits. An empirical DC model for the printed electrolyte-gated inorganic transistors is developed by extending and tuning the EKV model to make a good matching in different region of the output and transfer curves. The method is simple, requires few parameters, and is continuous as well as accurate over complete voltage range for this technology. The DC model is also extended to model the variability in printed transistors. The models are verified with the measurements data of the printed devices and circuits. The results confirm the accuracy of the EGT models and therefore the proposed methods can be used for design and simulation of EGT based circuits.

- The inkjet-printed electronics technology is a maskless additive manufacturing process and it has a very limited number of routing layers (e.g., two). One layer is used for routing and the second one is used to print crossovers. Such crossovers can alter the electrical characteristics of the printed circuits. In Chapter 4, we propose a crossover aware placement and routing (COPnR) methodology to optimize the placement and routing of printed circuits. The results show that the existing EDA tools and techniques have to be updated for the constraints of additive manufacturing technologies to ensure proper functionality of printed circuits.
- Process Design Kit (PDK) is a powerful tool for the technology development and design flow enablement. In Chapter 5, we propose the design flow for inkjet-printed electronics technology. The major components of the PDK are discussed in detail. We also present standard cell libraries for EGT technology by extracting the model parameters from the printed logic gates. To the best of our knowledge, these are the first synthesis and physical design ready standard cell libraries for low voltage printing technology.

6.2 Outlook

The work on fully-printed circuits and systems is an on-going field of research. On application level, environmental sensors and artificial skin is getting a lot of attention. In the future, we would like to continue technology development and design flow development through printer optimization. The printing of structures and materials deposition can be modeled through machine and deep learning algorithms by comparing the drawn and printed layouts. A lot of structures can be printed to generate the input (drawn layout) and output (printed design) data for the training of algorithms. Such models would be helpful in printing complex circuits (like printed microprocessors) with high production yield. Another interesting area is the integration of hybrid systems where printed sensors and systems can be integrated with silicon based electronics circuit. This would be extremely helpful in remote sensing and medical applications as the sensor would record the data while complex and fast silicon based readout circuitry would process and send the data to the cloud for further analysis.

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