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A Polymer/Carbon-Nanotube Ink as a Boron-Dopant/Inorganic-Passivation Free Carrier Selective Contact for Silicon Solar Cells with over 21% Efficiency

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Traditional silicon solar cells extract holes and achieve interface passivation with the use of a boron dopant and dielectric thin films such as silicon oxide or hydrogenated amorphous silicon. Without these two key components, few technologies have realized power conversion efficiencies above 20%. Here, a carbon nanotube ink is spin coated directly onto a silicon wafer to serve simultaneously as a hole extraction layer, but also to passivate interfacial defects. This enables a low-cost fabrication process that is absent of vacuum equipment and high-temperatures. Power conversion efficiencies of 21.4% on an device area of 4.8 cm² and 20% on an industrial size (245.71 cm²) wafer are obtained. Additionally, the high quality of this passivated carrier selective contact affords a fill factor of 82%, which is a record for silicon solar cells with dopant-free contacts. The combination of low-dimensional materials with an organic passivation is a new strategy to high performance photovoltaics.

1. Introduction

Silicon solar cells continue to be an important technology and currently occupy ≈90% of the worldwide photovoltaics market.^[1,2–4] This is despite the rapid development and increasingly high power conversion efficiency (PCE) of emerging technologies such as those from perovskites^[5] or organic-electronic materials^[6] and their market dominance is predicted to persist over the coming decades.^[2] Fundamentally, light is absorbed by a silicon wafer that is

bound asymmetrically on either side by carrier selective contacts to provide a built in potential for electron/hole separation. The unrivaled success of silicon photovoltaics can mostly be attributed to the aluminum back surface field (Al-BSF) cell due to its simple and low-cost manufacture through use of an Al paste/ink hole-selective contact. The Al-BSF cell currently accounts for ≈70% of the total crystalline silicon (c-Si) photovoltaic (PV) market,^[2] but recombination losses at the metal-silicon contact limit the design to a PCE of ≈20%.^[2] To further increase efficiency toward a theoretical maximum of 29%,^[4,7] strategies for interface passivation and complicated architectures are required. Current high-efficiency technologies, such as the passivated

emitter and rear cell,^[8] the tunnel-oxide passivating contact,^[9] and the silicon heterojunction (SHJ)^[10] have achieved PCEs over 25% and these are enabled by boron dopant and dielectric passivation layers. For example the SHJ cell employs a thin dielectric passivation interlayer such as intrinsic hydrogenated amorphous silicon (a-Si:H(i)), overlaid with highly doped a-Si:H(n⁺ or p⁺) (phosphorous, n⁺ or boron, p⁺) as a carrier selective contact. Passivation of surface defects is key to high open circuit voltage (V_{oc}), but a large absorption coefficient of a-Si:H means that even a few nanometers have significant parasitic photon absorption and lead to reductions in current (J_{sc}).^[11] There are several geometric variations to the SHJ cell, but the best known is the interdigitated back contact architecture, which avoids the use of a front side doped a-Si:H layer or metallization and currently holds the world record PCE for c-Si cells of 26.3%.^[10]

Despite the high efficiency of these cells, complicated manufacturing steps involving high temperature (≈900 °C) dopant diffusion followed by lithographic patterning and the requirement of capital-intensive processes such as plasma enhanced chemical vapor deposition (PECVD) combined with toxic boron/phosphorous gas precursors do little to address the levelized cost of the architecture.^[12] To this end research has been directed toward the replacement of the a-Si:H(n⁺ or p⁺) layer with dopant free hetero-contacts that can be deposited using simple low temperature (<200 °C) processes such as thermal evaporation, spin and spray coating or sputtering. Materials such as lithium fluoride (LiF_x),^[13–15] magnesium oxide (MgO_x),^[3] cesium carbonate (Cs₂CO₃)^[16] and titanium oxide (TiO_x)^[12,15,17] have been shown to form an electron selective contact, whereas transition metal oxides (MoO_x)^[11,13,14,18]

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NiO_x ,^[19] VO_x ,^[20] and WO_x ^[21] and polymers such as PEDOT^[22] and P3HT^[23] have been shown to be hole selective. In addition to processing simplicity, many of these materials have a high optical transparency compared to doped a-Si:H and thus reduce parasitic light absorption.^[14] In the meantime, the doped silicon layers have been replaced on both sides of the cell in a design known as the dopant free asymmetric hetero-contact (DASH) cell and PCEs over 20% have been reported.^[13,14] Although these cells are dopant free, they are still reliant upon a thin dielectric interlayer such as in the work of Bullock et al.^[13] with a-Si:H(i)/LiF_x/Al and a-Si:H(i)/MoO_x hetero-contacts, and these still remain capital intensive in their deposition. The ultimate advancement of the DASH concept is to combine both passivation and carrier selective transport into a single layer and thereby remove the need for thin dielectric interlayers. In this way high-temperature processes and vacuum equipment can be eliminated entirely from the production line.

In a burgeoning field, organic materials containing the sulfonic functional group have been shown to afford a high quality surface passivation rivaling SiO₂ or Si:H(i), but with the advantage of being processable at low temperatures at ambient pressures.^[24,25] The solution processability of these materials offers the possibility of combination with nanomaterials such as graphene,^[26] MXenes,^[27] carbon nanotubes CNTs,^[28,29] or transition metal dichalcogenides,^[30] which have all been shown to form carrier selective contacts to c-Si. From these nanomaterials many proof-of-principle solar cells, without surface passivation, but with nevertheless promising PCEs have already been demonstrated. For example, CNT:Si solar cells have been developed from 1.4% PCE in first reports to 17.2% and 18.9% for front- and back-junction devices with 1 and 3 cm² device areas, respectively.^[31,32] However, the obtainment of industrial sized cells and PCEs over 20% have been precluded by CNT film inhomogeneities and transfer processes required during fabrication. In the ideal strategy, cues for improvement can be taken from the Al-BSF cell that uses a solution-processable ink to coat a single layer, which achieves both highly-efficient hole-selectivity and interface defect passivation simultaneously. This ink should also be cost effective and have the potential large-scale production.

In this work we now show that CNTs and Nafion can be combined into an ink to form a “passivated charge selective contact” (PCSC) that can be spin coated directly onto c-Si. This process omits the requirement of vacuum equipment, high temperatures and a tunnel dielectric layer. Device performance is shown to be dependent upon the ink composition and record high efficiencies of 21.4% for 4.8 cm² and 20.1% on an industrial sized wafer (245.71 cm²) are shown. This work provides a “low-D + organic passivation” strategy to achieve high-efficiency silicon solar cells, which are dopant and dielectric free and which are made with a simple and cost-effective process. In addition, the polymer has been extensively applied in PV filed due to multiple functions including highly-efficient absorption,^[33] crystallization adjuvant,^[34] carrier transport layer,^[35] electrolytes,^[36] flexible substrates,^[37] protection layer, and so on. Polymers also have advantages in photovoltaics in that they are lightweight, easily disposable and have a low cost for fabrication.^[38] Here it is important to state that the terms “dopant- and “dielectric- free” refer to the absence of a boron/phosphorous dopant and inorganic passivation materials such as silicon

oxide and amorphous silicon, which are energy intensive and are unlike the doping provided by the Nafion to the CNTs.^[39]

2. Results and Discussion

Single walled carbon nanotubes (SWCNTs) with an average diameter of 1.5 nm and Nafion polymer were shear force mixed for 2 h to afford the CNT:Nafion ink used throughout this work, **Figure 1a**. The polar side chain of Nafion allowed for the CNTs to become individualized and well dispersed without the need for surfactants^[40] and the ink was found to remain stable for at least 6 months. Unlike CNT inks made from nanotube solutions previously in our group,^[41] CNT:Nafion solution can be fabricated at the ambient atmosphere without the glove box. The CNT:Nafion ink wet silicon with a small contact angle (11.1°) and was found to be amenable to spin coating. A 150 nm layer, consisting of a random network of CNTs infiltrated by Nafion polymer was cast onto 4.8 and 245.71 cm² wafers in a back-junction solar cell architecture, **Figure 1b**. Further details on the experimental determination of film thickness versus spin speed can be found in **Figure S1a**, Supporting Information. Importantly, the CNT:Nafion film was smooth and closed, **Figure 1c**, and thus formed a physical blocking layer to prevent metal infiltration during deposition of the back electrode (**Figure S1b**, Supporting Information). SEM of the CNT/Nafion layer, **Figure S1b**, Supporting Information, reveal a random network of CNTs intermixed with Nafion.

On the front of the solar cell a state-of-the-art design used by industry was implemented. This consisted of a phosphorous-diffused front surface field (FSF), silicon nitride (SiN_x) antireflection layer and a screen-printed silver grid on the front surface. **Figure 1c** shows a photograph of the front and back of a solar cell made on a pseudo-square (245.71 cm²) industrial-type n-type Czochralski-grown silicon wafer. A typical H-pattern of busbars and fingers is used on the front. Prior to deposition of the back electrode, a homogenous CNT:Nafion coating can be seen and is testament to the processability of the ink. Spin coating of the CNT:Nafion ink enables its direct industrialization. Using this approach device fabrication consisted of only six main steps: silicon surface texturing; front phosphorus diffusion; SiN_x deposition; screening printing of the front fingers; CNT:Nafion coating and Ag metallization on the back. The simplicity of this approach rivals that of the Al-BSF cell as shown in **Figure S2**, where a direct comparison is made.

Figure 2a shows the illuminated *J*-*V* curves of the solar cells with the corresponding solar cell parameters in the insert. The small-area (4.8 cm²) cell achieved a high PCE of 21.4% and yielded an open-circuit voltage (*V*_{oc}) of 654 mV, a short-circuit current density (*J*_{sc}) of 39.9 mA cm⁻² and a fill factor (FF) of 82%. As shown in **Figure S3**, Supporting Information, these PV parameters rival boron doped and dielectric passivated n-type silicon cells. Notably, a FF of 82% is not only a record for CNT-Si heterojunction solar cells, but also for dopant-free contact architectures, including MoO_x and PEDOT based Si solar cells.^[42] Furthermore, a FF of 82% compares well to the best value (82.3%) obtained by traditional Si solar cells.^[43] We speculate that this high FF is related to the CNTs themselves, having a high carrier mobility^[44] and an appropriate band alignment

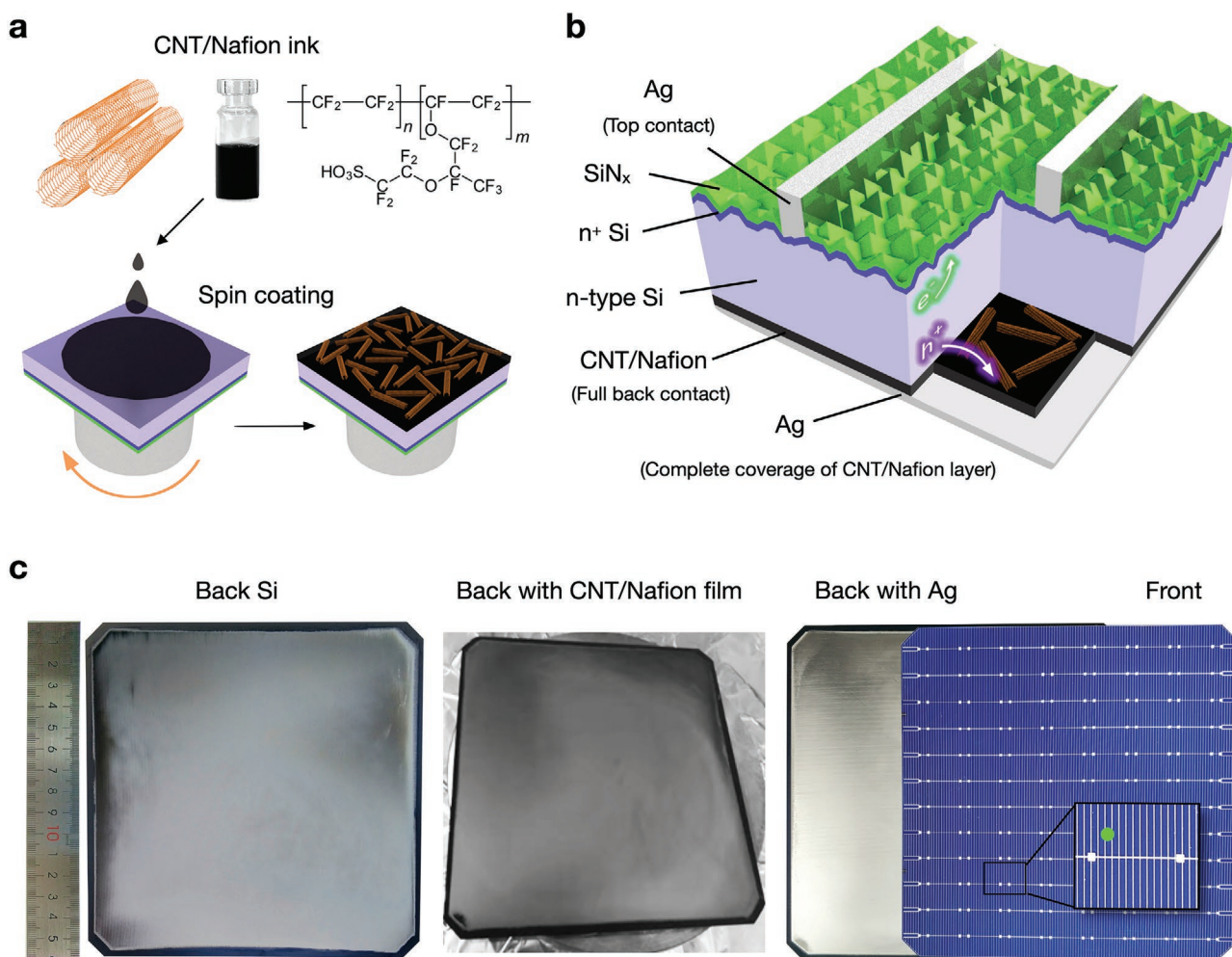


Figure 1. a) Carbon nanotubes and Nafion are shear force mixed to form an ink that can be spin coated onto the back of an b) industrial n-type silicon solar cell. c) Photograph of the back and front of the solar cell. The back is shown before and after CNT:Nafion coating and prior to deposition of the back electrode (Ag). The size of the light spot used for EQE is shown relative to the front Ag fingers.

with silicon. For the large area (245.71 cm²) solar cells a PCE of 20.1% was obtained. Figure 2b shows an EQE measurement for the solar cell with an integrated current density of 39.5 mA cm⁻². The slight reduction of integrated current compared to J_{sc} is an underestimation due to the partial overlap of the light spot on the contact fingers for EQE. The extent of the overlap is shown in Figure 1c. In total 28 solar cells with device areas of 4.8–245.71 cm² were fabricated and their PV parameters are displayed in Figure 2c,d. As can be seen by the small variation in parameters, the use of a CNT:Nafion ink is a robust approach. This reproducibility is enabled by the spin-coating method, stable back surface wet chemistry and the preparation of the ink with the accurate CNT-Nafion ratio.

At the silicon surface, a mixed CNT/Si and Nafion/Si PCSC junction was formed, where the CNTs were used to extract holes and the sulfonic groups of the Nafion were used for interfacial passivation.^[25,32,45] Because of the unsorted raw material containing CNTs with different bandgaps and electronic types, it is difficult to identify its physical nature of the junction simply as a Schottky, metal-insulator-semiconductor or p-n junction^[32,46] but the Barden model including the interface of density fits the

device physics well.^[32] Uniform interfacial contact between the silicon and the CNT:Nafion film is therefore highly important for high performance solar cells. During fabrication the silicon wafer is textured in a KOH bath to afford pyramids on both sides of the wafer as shown in Figure 3a. Spin coating of the CNT:Nafion ink directly onto this highly rough surface led to poor surface coverage of the film and thus poor device performance, Figure 3b. To aid spin coating and increase interfacial contact of the film, a mixed HNO₃/HF solution was used to etch the pyramids and planarize the rear of the solar cell prior to film deposition, Figure 3c. The smoother surface allowed for a better coverage of the CNT/Nafion layer and was essential to high performance, Figure 3d. The PV parameters of V_{oc} , J_{sc} , FF, and PCE with increased etch time for a 4.8 cm² cell are compared in Figure 3e. An etch time of 270 s was found to be optimum and a comparison of illuminated $J-V$ curves with and without etching is shown in Figure 3f. For reference, the unetched solar cell had a V_{oc} of 403 mV, a J_{sc} of 17.3 mA cm⁻², a FF of 43% and a PCE of 3.4%.

Likewise, passivation and electrical contact are dependent on CNT/Nafion ratio used for ink formation. Using the technique

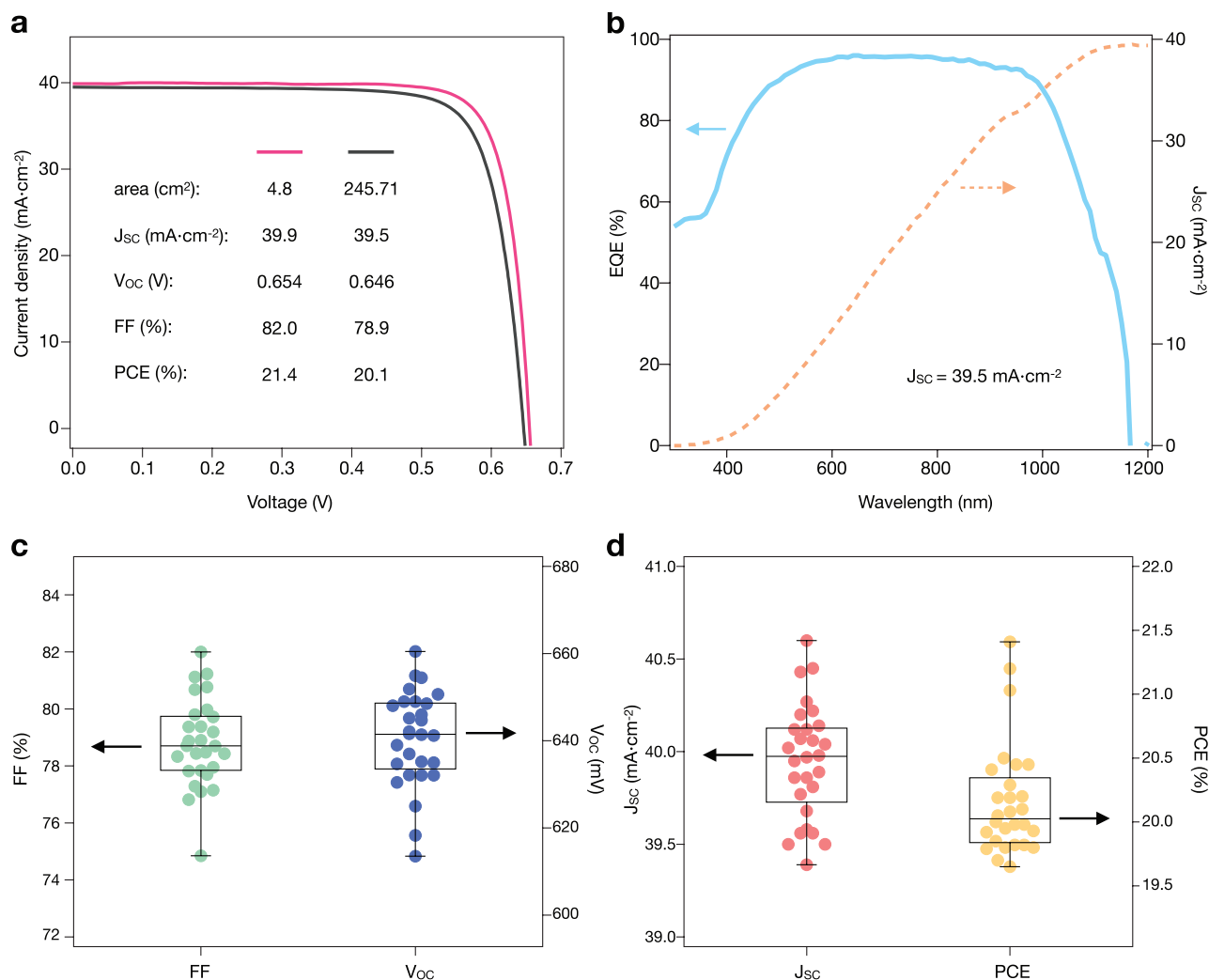


Figure 2. a) J - V data for champion solar cells with device areas of 4.8 and 245.71 cm². Device parameters are provided as an inset. b) EQE and integrated J_{sc} data. c,d) solar cell performance statistics comparing the FF, V_{oc} , J_{sc} and PCE for 28 devices with a device area of 4.8–245.71 cm².

of transient photoconductance decay, the minority carrier lifetime (τ_{eff}) for silicon wafers coated symmetrically with a CNT:Nafion film mixed in ratios 0.4–1.6 mg mL⁻¹ are shown in Figure 4a. Intuitively, due to Nafion being responsible for interfacial passivation, increased Nafion content led to an increase in τ_{eff} from 4.8 ms for a mix of 1.6 mg mL⁻¹ to 9.7 ms for a mix of 0.4 mg mL⁻¹ (m/v). For comparison, τ_{eff} for Nafion and CNTs alone was 25 ms and 78 μ s, respectively. However, as shown in Figure 4b, in electroluminescence (EL) measurements the situation is different and the excess Nafion led to a decrease in intensity. This is because the CNTs are responsible for electrical contact to the silicon and hole extraction. For high performance devices it is necessary to balance the quantity of CNT/Si to Nafion/Si interfacial regions. In this work optimized conditions of 1.3 mg mL⁻¹ CNT/Nafion were employed. PV parameters for a 4.8 cm² cell made with CNT/Nafion mix of 0.4, 0.7, 1, 1.3, 1.6 mg mL⁻¹ (m/v) are plotted in Figure S4, Supporting Information. A highly spatial resolution of photoluminescence (PL) mapping was performed on the 245.71 cm² industrial size solar cell, as shown in Figure 4c, except for some places

of contamination during fabrication, a homogenous contrast throughout all measurements can be regarded as the evidence of minimal variation of the CNT:Nafion film composition.

3. Conclusion

To date the use of low-dimensional semiconductors as dopant-free contacts (without a-Si:H(p⁺) layer) to silicon have failed to enable PCEs above 17%, with most falling below 15%, predominately due to a lack of surface passivation.^[28] Fabrication methods, including lamination, filtration, and film transfer have also limited their development from lab to industry. In this work, the combination of a low dimensional material (CNTs) with a passivation agent (Nafion) into a simple ink removes these barriers to industrialization and an efficiency of 21.4% was obtained. Furthermore, with the exception of the evaporation of silver, the fabrication process is as simple as that of the Al-BSF cell. Here, it is envisaged that a low-temperature rear metallization scheme, such as the use of Ag nanowire inks^[47] or

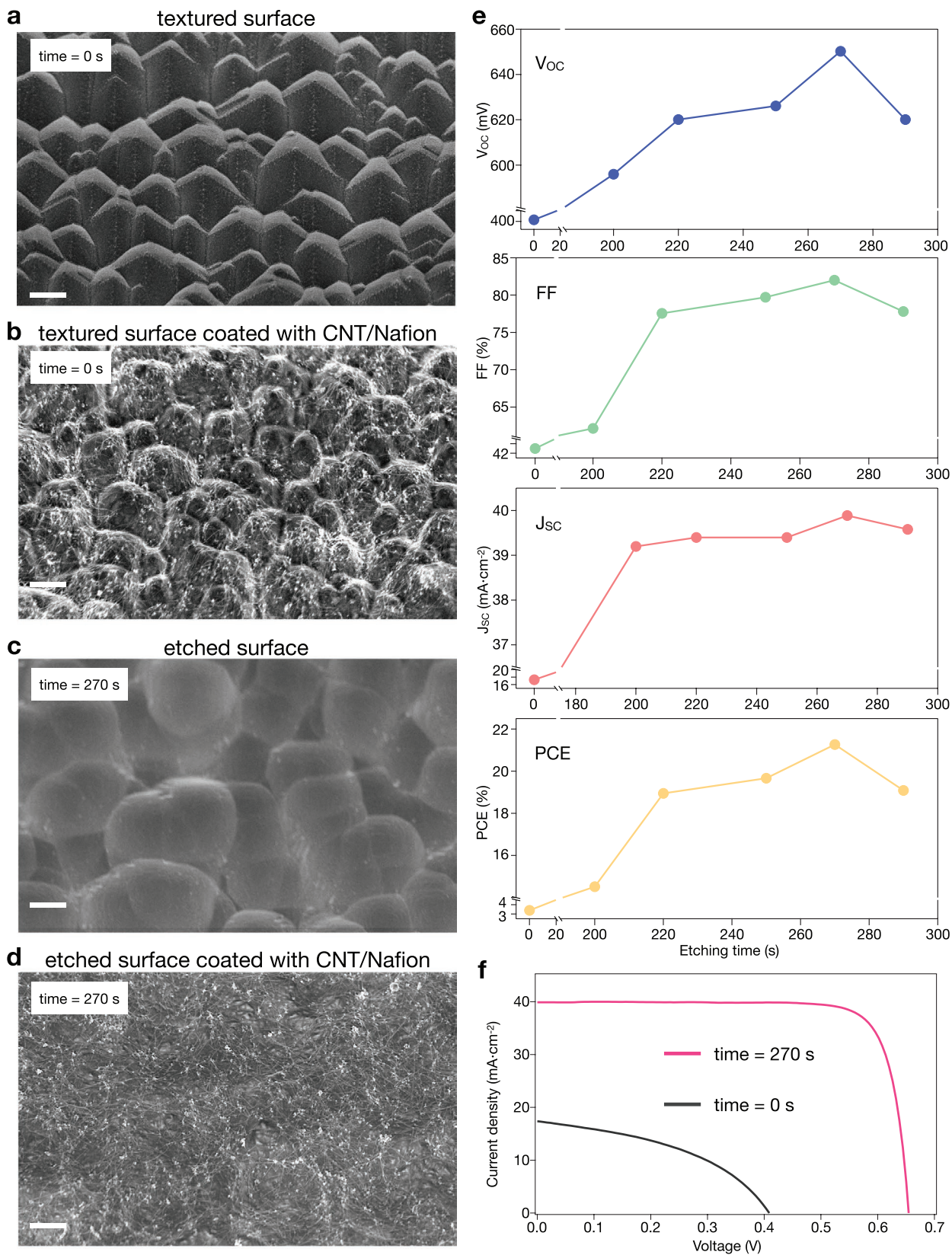


Figure 3. a–d) SEM micrograph of the rear silicon surface before and after etching with HNO_3/HF and the effect this had on the CNT/Nafion coating. Scale bar: $2\ \mu\text{m}$. e) Comparison of the PV parameters V_{oc} , FF, J_{sc} and PCE with increased etching time. f) $J-V$ data for cells with (270 s) and without etching (0 s). Device area: $4.8\ \text{cm}^2$.

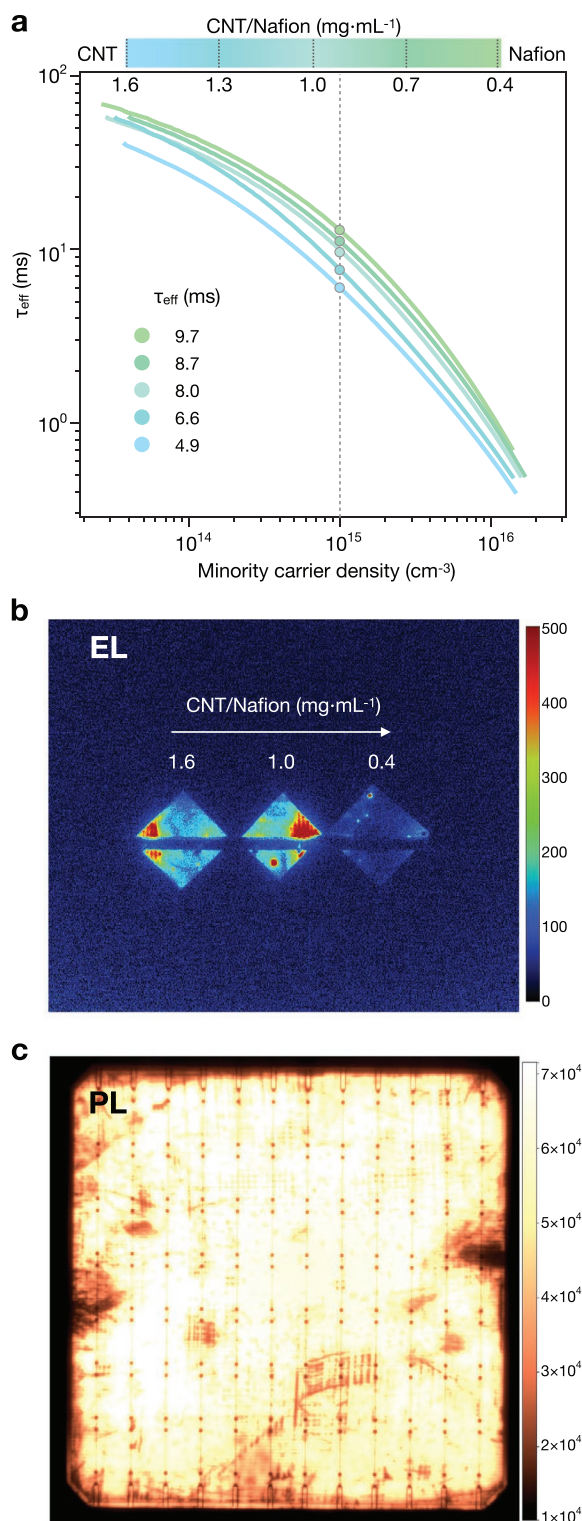


Figure 4. a) Transient photoconductance decay measurements of CNT:Nafion films on lightly doped ($4.5 \times 10^{11} \text{ cm}^{-3}$) double-side polished silicon wafers with different CNT/Nafion ratios. b) Electroluminescence intensity maps of 4.8 cm^2 solar cells made with 0.4, 1, and 1.6 mg mL^{-1} CNT/Nafion. The dark stripe in the middle of each cell is a bus bar probe used for device contact. c) Photoluminescence intensity map of a standard 245.71 cm^2 solar cell.

low temperature metal pastes designed by Schmidt et al.,^[48] will completely omit vacuum equipment and high-temperature processes in the future. A downside of the current approach is the long term stability of the CNT:Nafion composite passivated contacts. CNTs have been shown to have excellent stability toward degradation in ambient, humid, hot, or ultraviolet radiation conditions,^[49] whereas hygroscopic nature of Nafion is known to lead to performance reductions.^[45] In the future the challenge will be to find improvements or alternatives to Nafion, which are long term stable and capable of dispersing CNTs and passivating silicon surface defects.

4. Experimental Section

CNT/Nafion Ink Preparation: Raw electric-arc SWCNT powder (lot AP-A218, Carbon solution) was mixed in a Nafion precursor solution (Sigma-Aldrich, 5 wt% in a mixture of lower aliphatic alcohols and 45% water) in ratios of 0.4– 1.6 mg mL^{-1} . The solution was shear force mixed for 2 h in order to prepare uniform CNT dispersions to ensure the good reproducibility of device performances.

Device Fabrication: (100)-oriented n-type CZ wafers with a thickness of $180 \mu\text{m}$ and resistivity of $\approx 2 \Omega\text{-cm}$ (bulk doping concentration is $\approx 2.4 \times 10^{15} \text{ cm}^{-3}$) were selected for device fabrication involving several steps: 1) texturing of the surface by a chemical polish in a KOH (2–3 wt%, 82°C , 16 min) bath to yield pyramids with an average size of $5 \mu\text{m}$; 2) back surface polishing of the back surface using a $\text{HNO}_3/\text{HF}/\text{H}_2\text{O}$ (4:1:2) mixed solution, which was highly associated with the final CNT:Nafion film morphology and hence very important to get reproducibility of device performances; 3) the formation of a heavy phosphorus doped n^+ FSF by single-side POCl_3 diffusion performed on the textured surface and subsequent removal of the phosphorus silicon glass with HF; 4) passivation of the n^+ surface by a $\approx 80 \text{ nm}$ SiN_x dielectric layer deposited by PECVD and subsequent metallization of front surface by screen-printing a Ag paste followed by a standard firing process; 5) spin coating of a $\approx 150 \text{ nm}$ -thick CNT:Nafion layer onto the planar back surface using a CNT/Nafion ink at 3500 rpm for 40 s and RT under ambient atmosphere with a ramp time of 6 s; 6) thermal evaporation of a 300 nm full contact Ag electrode on CNT:Nafion thin film. Device sizes include a small $\approx 5 \text{ cm}^2$ and an industrial size (M2+) 245.71 cm^2 .

Characterization: The lifetime was measured by spin-coating CNT:Nafion films on both sides of float-zone Si wafers ($370 \mu\text{m}$, n-type, 3–5 $\text{k}\Omega\text{-cm}$) with double-sided mirror-polished surfaces. Solar cells were characterized by current density–voltage (J – V) measurements under standard test conditions (AM1.5, 100 mW cm^{-2} , and 25°C) and the EQE (R3011, Enlitech). A calibration was done for the light source using a reference solar cell (Ser. No. 076–2014, Fraunhofer ISE). A Zeiss Ultra Plus with 2.00 kV EHT and 2.9 mm working distance was used for SEM imaging. PL/EL mapping was performed with a BT imaging LIS-R1 system.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

energy, Na₂SO₄, photovoltaics, single-walled carbon nanotubes, thin films

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