Cascaded H-Bridge based Parallel Hybrid Converter – A new Voltage Source for Power-Hardware-in-the-Loop Emulation Systems

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***Abstract*—This paper presents a new 50 kVA Parallel Hybrid Converter (PHC) for Power-Hardware-in-the-Loop (PHIL) emulation systems. The converter combines the high output voltage quality of a low power 17-level Cascaded H-Bridge (CHB) converter in star configuration with the high efficiency and high power density of a 2-level converter. The requirements a converter topology must fulfill in order to be used for PHIL emulation systems are derived and it is shown, that the PHC topology characteristics ideally meet these requirements.**

***Index Terms*—Parallel Hybrid Converter (PHC), energy and balancing control, predictive current control, Power-Hardware-in-the-Loop, Cascaded H-Bridge Converter (CHB), Modular Multilevel Converter (MMC)**

I. Introduction

In recent years, it has become a common trend to replace expensive and space-consuming rotating machine test benches (Fig. 1) with modern Power-Hardware-in-the-Loop (PHIL) emulation test benches (Fig. 2) for testing of drive inverters. A PHIL emulator allows to analyze a Device under Test (DUT), typically a drive inverter, in an early development phase of electrical drive trains even without an real machine [1,2]. For this purpose, the DUT is connected to the PHIL emulation converter via a linear inductive coupling network (L_{CN}, R_{CN}). The PHIL test bench emulates the electrical terminal behavior of an electrical machine. Therefore, the output voltages of the PHIL converter $u_{\mathrm{PHIL},x}$ ($x \in \{1,2,3\}$) are controlled by a Real-Time Simulation System (RTSS) in such a way that the currents $i_{\mathrm{S},x}$ and the current slopes $\frac{\mathrm{d}i_{\mathrm{S},x}}{\mathrm{d}t}$ through the inductors L_{CN} correspond exactly to the currents and current slopes of the real machine [3].

In Section II of this paper, the operation principle of a PHIL emulation test bench is described. Therein a machine model of a non-linear permanent magnet synchronous machine (PMSM) as well as a model of the PHIL test bench are derived. By means of these models, a computation instruction for the reference values of the PHIL emulation converter output voltages $u^*_{\mathrm{PHIL,x}}$ is determined. Based on these models and their corresponding equations, the requirements, which a PHIL emulation converter topology and the RTSS have to fulfill, are derived in Section III. In Section IV, the operation principle of the proposed novel Parallel Hybrid Converter (PHC) is shown and it is demonstrated, that the characteristics of this converter topology ideally meet the requirements. The PHC topology firstly introduced in [4] is shown in Fig. 6. Finally, in Section V a 50 kVA laboratory prototype of the PHIL test bench is presented. The setup includes a new developed RTSS, which is also used as the Central Control Unit (CCU) of the PHC as well as the power electronic hardware of the PHC.

II. PHIL test bench - Principle of Operation

As shown in Fig. 2, a typical PHIL emulation test bench consists of a RTSS, an emulation converter and an inductive coupling network (L_{CN}, R_{CN}). The DUT inverter is coupled to the emulation converter through this network. To respond

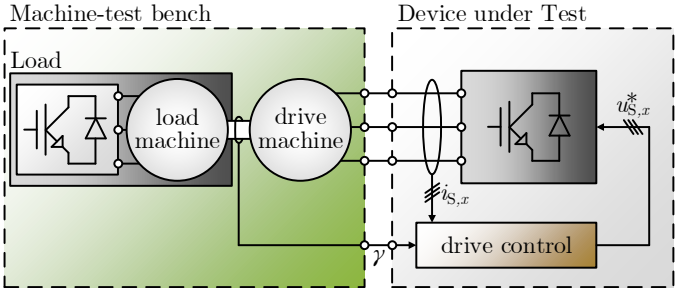


Fig. 1: Rotating machine test bench

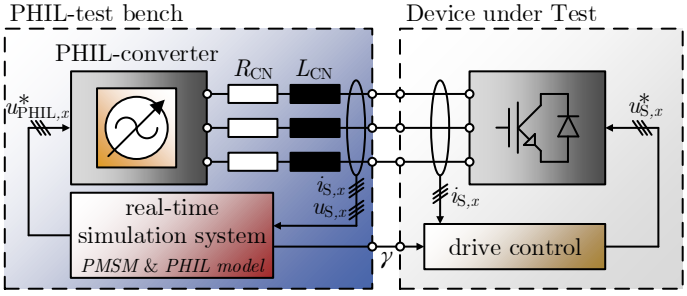


Fig. 2: Power Hardware-in-the-Loop Emulation test bench

rapidly to changes of the DUT's output voltages $u_{\mathrm{S},x}$ and to achieve a precise emulation of a nonlinear electrical machine, the RTSS measures these voltages and the currents $i_{\mathrm{S},x}$ with a high sample frequency ($f_{\mathrm{sample}} > 1\,\mathrm{MHz}$). These values are feed forward to the machine model, which takes the nonlinearity of the emulated machine into account and computes the new values of the machine currents $i^*_{\mathrm{S},x}$. The change of the rotor position angle, the angle γ^* and the angular frequency $\omega^* = \frac{\mathrm{d}\gamma^*}{\mathrm{d}t}$ are computed with the machine model. This computation is based either on a fixed rotor speed, set by the operator, or an superordinate mechanical model, which is not in the scope of this paper. The new values are fed to the PHIL model, which then determines the reference values for the PHIL converter output voltages $u^*_{\mathrm{PHIL},x}$.

A. PMSM model

In the following, the model of a highly utilized, anisotropic PMSM is derived. The model describes the nonlinear reaction of the machine based on the DUT output voltages $u_{\mathrm{S},x}$. The harmonics in the flux linkage are neglected, yielding to a fundamental model. In addition, dielectric displacement currents, iron losses and temperature-dependent effects are also neglected. However, the modeling considers nonlinearities caused by saturation and cross-coupling effects.

Based on the three phase equivalent circuit diagram (ECD) of the emulated PMSM in Fig. 3 a), the voltage equation of a single PMSM phase is derived in (1). $R_{\mathrm{S},x}$ denotes the stator resistance, $i_{\mathrm{S},x}$ the stator currents, $\frac{\mathrm{d}\,\Psi_{\mathrm{S},x}}{\mathrm{d}t}$ the induced voltages, $\Psi_{\mathrm{S},x}$ the stator flux linkages and $u_{\mathrm{S},x}$ are the output voltages of the DUT inverter.

$$u_{\mathrm{S},x} = R_{\mathrm{S},x} \cdot i_{\mathrm{S},x} + \frac{\mathrm{d}\,\Psi_{\mathrm{S},x}}{\mathrm{d}t} \tag{1}$$

The stator voltage equation (1) is transformed into the rotor fixed dq-system (2) and (3) by means of the amplitude-invariant Park Transformation.

$$u_{\mathrm{d}} = R_{\mathrm{S}} \cdot i_{\mathrm{d}} + \frac{\mathrm{d}\,\Psi_{\mathrm{d}}}{\mathrm{d}t} - \omega \cdot \Psi_{\mathrm{q}} \tag{2}$$

$$u_{\mathrm{q}} = R_{\mathrm{S}} \cdot i_{\mathrm{q}} + \frac{\mathrm{d}\,\Psi_{\mathrm{q}}}{\mathrm{d}t} + \omega \cdot \Psi_{\mathrm{d}} \tag{3}$$

Due to the high sample rate required for the model computation, the machine model has to be implemented on the field-programmable gate array (FPGA) of the RTSS. Therefore, the implementation must be causal with time-discrete and value-discrete variables. For the flux based implementation, the flux linkages determine the currents $i_{\mathrm{d}} = i_{\mathrm{d}}(\Psi_{\mathrm{d}}, \Psi_{\mathrm{q}})$ and $i_{\mathrm{q}} = i_{\mathrm{q}}(\Psi_{\mathrm{d}}, \Psi_{\mathrm{q}})$. For the current based implementation, the currents determine the flux linkages $\Psi_{\mathrm{d}} = \Psi_{\mathrm{d}}(i_{\mathrm{d}}, i_{\mathrm{q}})$ and $\Psi_{\mathrm{q}} = \Psi_{\mathrm{q}}(i_{\mathrm{d}}, i_{\mathrm{q}})$. Since the emulated PMSM shows non-linear dependencies between the machine currents i_{d} and i_{q} and the flux linkages Ψ_{d} and Ψ_{q} due to saturation effects, it is not possible to describe these dependencies with simple analytical equations. Therefore, the correlations between the currents and the flux linkages have to be obtained either by measurements of a real machine on a test bench or by the use of finite element method (FEM) and then stored in lookup tables (LUT).

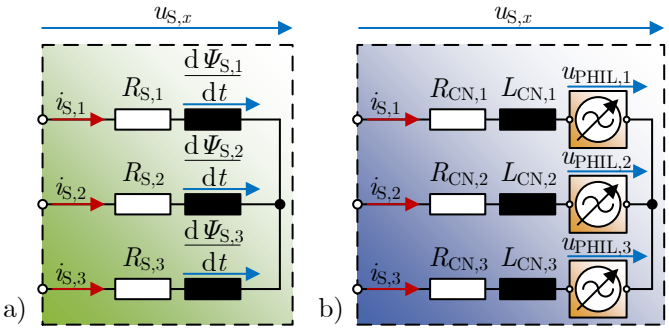


Fig. 3: Equivalent circuit diagram of the PMSM and the PHIL-emulation test bench

In this paper, the flux-based machine model is used as in [1], since this kind of model requires only LUTs for $i_{\mathrm{d}}(\Psi_d, \Psi_{\mathrm{q}})$ and $i_{\mathrm{q}}(\Psi_{\mathrm{d}}, \Psi_{\mathrm{q}})$. The LUTs are depicted in Fig. 4 and were obtained in [5] by inverting the measured flux linkage functions $\Psi_{\mathrm{d}}(i_{\mathrm{d}}, i_{\mathrm{q}})$ and $\Psi_{\mathrm{q}}(i_{\mathrm{d}}, i_{\mathrm{q}})$. The current-based machine model, which was used in [3,6,7], requires six LUTs and thus more memory in the RTSS. Additional to the flux linkages $\Psi_{\mathrm{d}}(i_{\mathrm{d}}, i_{\mathrm{q}})$ and $\Psi_{\mathrm{q}}(i_{\mathrm{d}}, i_{\mathrm{q}})$, four LUTs are needed for the current-based machine model to avoid multiple successive division operations in the FPGA.

To determine the flux linkages of the machine, the voltage equations (2) and (3) are rearranged to the derivatives of the flux linkages and integrated, leading to (4) and (5).

$$\Psi_{\mathrm{d}} = \int u_{\mathrm{d}} - R_{\mathrm{S}} \cdot i_{\mathrm{d}} + \omega \cdot \Psi_{\mathrm{q}} \mathrm{d}t \tag{4}$$

$$\Psi_{\mathrm{q}} = \int u_{\mathrm{q}} - R_{\mathrm{S}} \cdot i_{\mathrm{q}} - \omega \cdot \Psi_{\mathrm{d}} \mathrm{d}t \tag{5}$$

For the implementation on an FPGA, (4) and (5) are discretized using the forward Euler method with the sampling time $t_{\mathrm{S}} = \frac{1}{f_{\mathrm{sample}}}$. This leads to (6) and (7) for the flux linkages at the next sampling time step $k+1$.

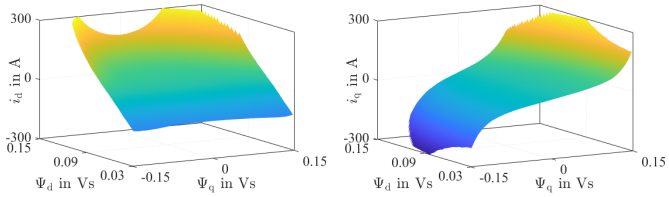
$$\Psi_{\mathrm{d},k+1} = \Psi_{\mathrm{d},k} + t_{\mathrm{S}}(u_{\mathrm{d},k} - R_{\mathrm{S}} \cdot i_{\mathrm{d},k} + \omega_k \cdot \Psi_{\mathrm{q},k}) \tag{6}$$

$$\Psi_{\mathrm{q},k+1} = \Psi_{\mathrm{q},k} + t_{\mathrm{S}}(u_{\mathrm{q},k} - R_{\mathrm{S}} \cdot i_{\mathrm{q},k} - \omega_k \cdot \Psi_{\mathrm{d},k}) \tag{7}$$

The voltages $u_{\mathrm{d},k}$ and $u_{\mathrm{q},k}$ are the measured and dq-transformed output voltages of the DUT. The currents $i_{\mathrm{d},k} = f(\Psi_{\mathrm{d},k}, \Psi_{\mathrm{q},k})$ and $i_{\mathrm{q},k} = f(\Psi_{\mathrm{d},k}, \Psi_{\mathrm{q},k})$ are read out of the LUTs using the previous flux linkages $\Psi_{\mathrm{d},k}$ and $\Psi_{\mathrm{q},k}$. The results of (6) and (7) are used to read the new machine currents $i_{\mathrm{d},k+1}$ and $i_{\mathrm{q},k+1}$ from the LUTs. These values are used for the computation of the new reference values of the PHIL converter output voltages $u^*_{\mathrm{PHIL},x,k+1}$.

B. PHIL model

In order to compute the PHIL converter reference output voltages, a model of the PHIL test bench is needed. This model describes the relation between the calculated PMSM model currents $i^*_{\mathrm{S},x}$, the measured DUT output voltages $u_{\mathrm{S},x}$ and the reference values of the PHIL converter output voltages



(a) $i_\mathrm{d}(\Psi_\mathrm{d}, \Psi_\mathrm{q})$ (b) $i_\mathrm{q}(\Psi_\mathrm{d}, \Psi_\mathrm{q})$

Fig. 4: Stator currents depending on the stator flux linkages Ψ_d and Ψ_q

$u^*_{\mathrm{PHIL},x}$. Fig. 3 b) depicts the ECD of a PHIL emulation test bench with the line resistance $R_{\mathrm{CN},x}$ and coupling inductance $L_{\mathrm{CN},x}$ of the coupling network, the output voltages of the PHIL converter $u_{\mathrm{PHIL},x}$, the DUT output voltages $u_{\mathrm{S},x}$ and output currents $i_{\mathrm{S},x}$. Similar to the derivation of the PMSM model equations, the voltage equation of the ECD, which is given for a single phase in (8), is transformed into the dq-system.

$$u_{\mathrm{S},x} = R_{\mathrm{CN},x} \cdot i_{\mathrm{S},x} + L_{\mathrm{CN},x} \frac{\mathrm{d}i_{\mathrm{S},x}}{\mathrm{d}t} + u^*_{\mathrm{PHIL},x} \tag{8}$$

Then the results are rearranged to the PHIL emulation converter reference voltages $u^*_{\mathrm{PHIL,d}}$ and $u^*_{\mathrm{PHIL,q}}$.

$$u^*_{\mathrm{PHIL,d}} = u_{\mathrm{S,d}} - R_{\mathrm{CN}} \cdot i_\mathrm{d} - L_{\mathrm{CN}}(\frac{\mathrm{d}i_\mathrm{d}}{\mathrm{d}t} - \omega \cdot i_\mathrm{q}) \tag{9}$$

$$u^*_{\mathrm{PHIL,q}} = u_{\mathrm{S,q}} - R_{\mathrm{CN}} \cdot i_\mathrm{q} - L_{\mathrm{CN}}(\frac{\mathrm{d}i_\mathrm{q}}{\mathrm{d}t} + \omega \cdot i_\mathrm{d}) \tag{10}$$

Discretization of (9) and (10) using the forward Euler method with the sampling time $t_\mathrm{S} = \frac{1}{f_\mathrm{sample}}$ leads to (11) and (12).

$$\begin{aligned} u^*_{\mathrm{PHIL,d},k+1} =& u_{\mathrm{S,d},k} - R_{\mathrm{CN}} \cdot i_{\mathrm{d},k+1} \\ & - L_{\mathrm{CN}}(\frac{i_{\mathrm{d},k+1} - i_{\mathrm{d},k}}{t_\mathrm{S}} - \omega_k \cdot i_{\mathrm{q},k+1}) \end{aligned} \tag{11}$$

$$\begin{aligned} u^*_{\mathrm{PHIL,q},k+1} =& u_{\mathrm{S,q},k} - R_{\mathrm{CN}} \cdot i_{\mathrm{q},k+1} \\ & - L_{\mathrm{CN}}(\frac{i_{\mathrm{q},k+1} - i_{\mathrm{q},k}}{t_\mathrm{S}} + \omega_k \cdot i_{\mathrm{d},k+1}) \end{aligned} \tag{12}$$

The PHIL emulation converter reference output voltages $u^*_{\mathrm{PHIL,d},k+1}$ and $u^*_{\mathrm{PHIL,q},k+1}$ are transformed back into the three phase 123-system using the inverse Park Transformation and the new rotor position angle γ^*_{k+1} computed with (13).

$$\gamma^*_{k+1} = \gamma_k + \omega_k \cdot t_\mathrm{S} \tag{13}$$

Finally, the new reference output voltage values $u^*_{\mathrm{PHIL},x,k+1}$ are fed forward to the PHIL emulation converter.

III. PHIL CONVERTER REQUIREMENTS

In order to show the requirements on the PHIL emulation converter's capability to provide given voltage and current reference values ($u^*_{\mathrm{PHIL},x}$, $i^*_{\mathrm{S},x}$) at its output, *Matlab/Simulink* was used to simulate the complete system of a PHIL test bench connected to a 2-level DUT inverter. The PMSM control algorithm used in the simulation to control the 2-level DUT inverter is a predictive current controller for saturated cross-coupled PMSMs with a control frequency of 8 kHz and is presented in detail in [5]. The parameters of the DUT inverter, the parameters of the emulated PMSM as well as parameters of the simulated PHIL test bench are given in Table I. The DUT and machine parameters are the same as in [1,3,5–7].

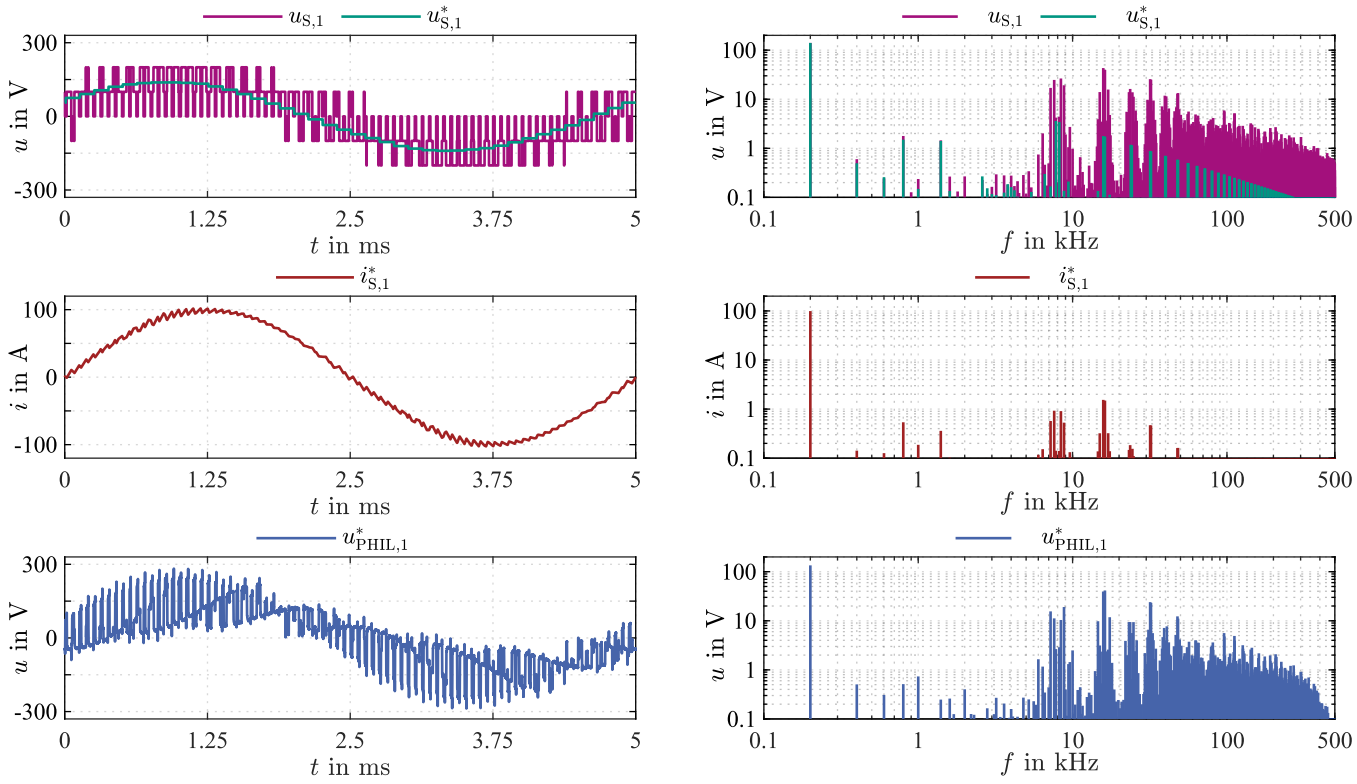
For the simulation, the PMSM rotor speed was set to 4000 rpm or 200 Hz stator current frequency, respectively. The torque reference value of the DUT controller was set to 48.6 Nm leading to a stator phase current amplitude of $\hat{i}_\mathrm{S} \approx 100$ A. The simulation results, depicted in Fig. 5, show the DUT reference values $u^*_{\mathrm{S},1}$, the DUT output voltage $u_{\mathrm{S},1}$, the model based computed resulting machine current $i^*_{\mathrm{S},1}$ and the reference value for the PHIL emulation converter $u^*_{\mathrm{PHIL},1}$. Fig. 5a) and Fig. 5b) show the time domain and the frequency domain of the simulation results for one electrical period. The output voltage required by the controller from the DUT inverter $u^*_{\mathrm{S},1}$ corresponds to the fundamental of the stator frequency. The high frequency components in the reference value are caused by the controller frequency of 8 kHz and the resulting 125 µs wide steps in the reference value $u^*_{\mathrm{S},1}$.

As expected the output voltage $u_{\mathrm{S},1}$ of the 2-level DUT shows apart from the low-frequency large fundamental amplitude at 200 Hz also high-frequency components with significant amplitude values (> 10 V up to 50 kHz and > 1 V up to 500 kHz).

The resulting machine current $i^*_{\mathrm{S},1}$ is shown in the middle of Fig 5. It is computed by the PMSM model equations (6) and (7) from the stored inverse flux linkages $\underline{i}_\mathrm{dq}(\Psi_\mathrm{d}, \Psi_\mathrm{q})$ (Fig. 4) and the DUT output voltage $u_{\mathrm{S},x}$ measured with a sample rate of 2.5 MHz. Typically, for a PMSM the emulated machine current $i^*_{\mathrm{S},x}$ can be separated into a low frequency and a high frequency part as depicted in (14). The low frequency part $i_{\mathrm{S,LF},x}$ includes the high amplitude fundamental current at 200 Hz and the relevant harmonics up to the ν_LF'th harmonic of the machine ($f_\mathrm{LF} < 1$ kHz to 2 kHz), where ν denotes the harmonic number. The high frequency part $i_{\mathrm{S,ripple},x}$ includes all high frequency components above f_LF, which are primarily the frequency components of the machine current ripple in the range of the DUT switching frequency (8 kHz) and its harmonics (16 kHz, 24 kHz, ...). The high frequency components caused by the current ripple are considerably smaller compared to the fundamental component.

$$i^*_{\mathrm{S}x} = i_{\mathrm{S,LF},x} + i_{\mathrm{S,ripple},x} \quad \text{with } i_{\mathrm{S,LF},x} = \sum_{\nu=1}^{\nu_\mathrm{LF}} {}^{\nu} i_{\mathrm{S},x} \tag{14}$$

The computed reference value for the current is fed to the PHIL model, which computes the reference value for the output voltage of the PHIL emulation converter. In the simulation the PHIL converter output voltage is updated with a frequency of 500 kHz. Thus, the reference voltage computed by the PHIL model is averaged over five sampling periods by a moving



(a) Time domain of the simulated results

(b) Frequency domain of the simulation results

Fig. 5: Simulation results for phase 1 of the DUT output voltage $u_{S,1}$, its reference value $u^*_{S,1}$, the machine current $i^*_{S,1}$ computed by the PMSM model and the PHIL converters output voltage reference value $u^*_{PHIL,1}$ computed by the PHIL model

average filter and transferred as $u^*_{PHIL,x}$ to the emulation converter.

At the bottom of Fig. 5a), the reference output voltage $u^*_{PHIL,1}$ of the first phase of the PHIL emulation converter is depicted. As can be seen in the time domain as well as in the frequency domain and as it was derived in Section II, $u^*_{PHIL,x}$ is a discontinuous function with high amplitude and high frequency components, resulting from the switching output voltages $u_{S,x}$ of the DUT inverter and the nonlinear correlations between machine flux linkages and machine currents $i_{dq}(\Psi_d, \Psi_q)$.

The requirements for a PHIL converter to precisely emulate the nonlinear reaction of an electrical machine to the switching output voltage of the DUT inverter can be summarized as follows:

1) The entire PHIL test bench must have a very low overall dead time to respond almost immediately to the switching output voltage of the DUT inverter,in order to minimize deviations of the current slope $\frac{di_{S,x}}{dt}$ from the reference value $\frac{di^*_{S,x}}{dt}$.
2) The PHIL emulation converter must be able to control its output voltage highly dynamic but also highly precise to realize the required voltage-time area [8,9].
3) The requirements for the emulation converter's output current dynamics are much lower than the required output voltage dynamics.

In recent publications, either parallel topologies like the Modular Multiphase Multilevel Converter (MMPMC) [8–11], serial topologies like the Modular Multilevel Converter (MMC) [1,12] or hybrid serial topologies like the Series-Hybrid Cascaded H-Bridge (SH-CHB) Converter [13] are proposed as PHIL converter. Since a PHIL converter for automotive applications must have a high power rating of up to several 100 kW [11], the complexity, volume and weight should be reduced in order to reduce costs. Therefore, this contribution proposes the novel Cascaded H-Bridge (CHB) based Parallel Hybrid Converter for PHIL applications. The PHC was first introduced in [4] and further investigated for the application as grid-connected medium voltage converter in [14,15].

IV. Operation Principle of the Parallel Hybrid Converter (PHC)

The PHC topology shown in Fig. 6 combines the high output voltage quality and dynamics of a Cascaded H-Bridge Converter in star configuration with the high efficiency and high power density of a 2-level converter as Main Power Source (MPS). The MPS is coupled in parallel to the CHB via a coupling network with the line resistance R_m and the coupling inductance L_m and acts as a current source. The general operating principle of the PHC is based on the

TABLE I: Simulation Parameters

DUT Parameter	**Value**
DUT DC link voltage	300 V
DUT switching frequency	8 kHz
PMSM Model Parameter	**Value**
Voltage nom.	214 V
Current nom. / max.	169 A / 300 A
Shaft power nom. / max.	57 kW / 97 kW
Speed nom. / max.	4200 rpm / 11 000 rpm
El. frequency nom. / max.	210 Hz / 550 Hz
Torque nom. / max.	130 Nm / 220 Nm
Number of pole pairs	3
Ohmic stator resistance typ.	10.5 mΩ
PHIL Model Parameter	**Value**
Model sample and computation frequency	2.5 MHz
PHIL output voltage update frequency	500 kHz
Coupling network resistance	8.75 mΩ
Coupling network inductance	500 µH
PHC Parameter	**Value**
CHB carrier frequency	500 kHz
CHB current boundary	20 A
CHB number of cells	8
CHB cell DC link voltage	60 V
MPS DC link voltage	700 V
MPS coupling network resistance	7 mΩ
MPS coupling network inductance	160 µH

following concept: A high dynamic low-power 17-level CHB converter with a high switching frequency, defines the output voltage $u_{\mathrm{o},x}$ and thus controls the output current $i_{\mathrm{o},x}$. The MPS thereby delivers the bulk of the output current $i_{\mathrm{m},x} \approx i_{\mathrm{o},x}$ and is implemented as a high-power 2-level converter with a low switching frequency. As a result, the CHB only has to compensate for the differences between the output currents $i_{\mathrm{o},x}$ and the MPS currents $i_{\mathrm{m},x}$ and therefore only has to deliver distortion reactive power. This reactive power is significantly lower compared to the output power of the PHC, which is completely supplied by the MPS. Thus, the eight CHB cells of each CHB phase do not require an additional power supply. The developed control concept derived in [4] contains an energy controller, which balances the voltages $u_{\mathrm{c,C}x1-8}$ of the CHB cell capacitors as well as a limit controller to keep the CHB current inside a given boundary circle in the αβ-plane. The energy controller utilizes a PI-controller based decoupled control scheme to balance the mean energy of the CHB and the difference energies between the CHB phases separately. A modified Predictive Current Controller (PCC) based on [16] is used as limit controller. The PCC determines the switching states of the MPS and thus limits load independent the root mean square (RMS) value of the CHB current $i_{\mathrm{c,RMS}}$ to $\approx 12\,\%$ of the nominal MPS current RMS value $i_{\mathrm{m,RMS,max}}$.

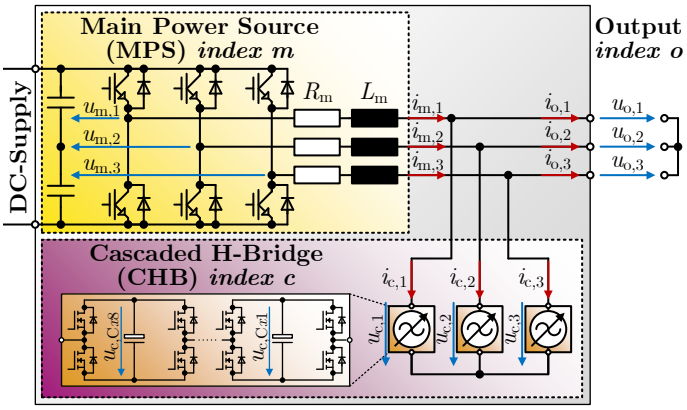


Fig. 6: Equivalent circuit of the novel Parallel Hybrid Converter (PHC)

A. The PHC as a PHIL converter

The bandwidth of the PHC output voltage for small and large amplitudes is only limited by the carrier frequency of the low power CHB, which is set to a frequency of $f_{\mathrm{c,SW}} = 500\,\mathrm{kHz}$. This also applies to the bandwidth of the PHC output current for small amplitude values, which are in the range of the current rating of the CHB. The bandwidth for large output current amplitudes, however, is significantly lower than the PHC output voltage bandwidth and is determined by the

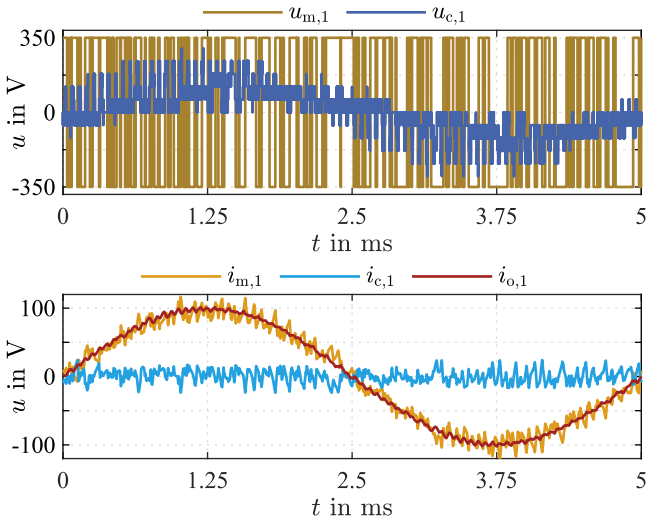


Fig. 7: Simulation results for phase 1 of the PHC used as PHIL emulation converter

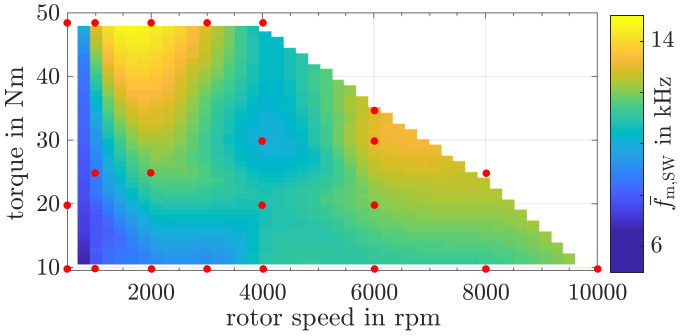


Fig. 8: Operating point depending MPS switching frequency, the red markers represent simulated operating points

high-power 2-level MPS and the coupling inductors $L_{\mathrm{m},x}$. Hence, the PHC offers promising characteristics for the use as a PHIL converter, since, as shown in section III, a PHIL converter requires a very high output voltage bandwidth and thus a very high carrier frequency compared to the DUT ($f_{\mathrm{SW,DUT}} \ll f_{\mathrm{SW,PHIL}} \approx 100\,\mathrm{kHz} - 800\,\mathrm{kHz}$ [1,11]). However, as shown in Fig. 5 and in (14), the required bandwidth of high amplitude output currents is significantly lower than the required output voltage bandwidth.

For the simulation described in Section III, the PHC was already used as PHIL converter with the simulation parameters given in Table I. The resulting output voltages of the CHB $u_{\mathrm{c},1}$ and the MPS $u_{\mathrm{m},1}$ as well as the resulting output currents of the CHB $i_{\mathrm{c},1}$, the MPS $i_{\mathrm{m},1}$ and the PHC $i_{\mathrm{o},1}$ are shown in Fig. 7. The PHIL converter reference voltage $u^*_{\mathrm{PHIL},1}$ is provided by the CHB as $u_{\mathrm{c},1}$ and the resulting PHC output current $i_{\mathrm{o},1}$ corresponds to the emulated PMSM stator current $i_{\mathrm{S},1}$. As can be seen, the CHB output current $i_{\mathrm{c},1}$ is kept within its predefined boundaries very effectively by the limit controller regardless of the CHB output voltage $u_{\mathrm{c},1}$ or the PHC output current $i_{\mathrm{o},1}$. The ratio between the average RMS value of the three CHB currents and the PHC output currents is $\frac{\bar{i}_{\mathrm{c,RMS}}}{\bar{i}_{\mathrm{o,RMS}}} = \frac{9.9\,\mathrm{A}}{70.4\,\mathrm{A}} \approx 0.14$.

The fundamental current of the emulated machine and thus the output current of the PHC is completely provided by the MPS. Thereby, the average switching frequency of the MPS for this simulated operating point of the emulated PMSM is only $\bar{f}_{\mathrm{m,SW}} \approx 10.34\,\mathrm{kHz}$. The MPS switching frequency $\bar{f}_{\mathrm{m,SW}}$ is almost independent of the carrier frequency $f_{\mathrm{c,SW}}$ of the CHB, but varies operating point depending between $5.4\,\mathrm{kHz}$ and $14.5\,\mathrm{kHz}$ as shown in Fig. 8. This is less than twice the switching frequency of the DUT and significantly less than the switching frequency of previously published PHIL converter topologies. Thus, a high performance 2-level converter with $1200\,\mathrm{V}$ Insulated-Gate Bipolar Transistors (IGBT) can be used for the MPS and low power $100\,\mathrm{V}$ silicon Metal Oxide Semiconductor Field Effect Transistors (MOSFET) can be used for the CHB. This could significantly reduce system cost, volume and weight compared to conventional PHIL systems, as these use full-power multi-level converters with high switching frequency.

V. PHIL Converter Concept, Signal Processing System and Power Electronics Hardware

In this section, the concept of the constructed $50\,\mathrm{kVA}$ laboratory prototype of the PHIL test bench is introduced. The new developed Real-Time Simulation System and its use as Central Control Unit of the PHIL is presented. And finally, the new developed power electronics hardware of the PHC is explained as well as first measurement results at an ohmic inductive load are shown.

A. PHIL Converter Concept

Fig. 9 shows a schematic diagram of the PHIL converter system. The system consists of the Cascaded H-bridge based

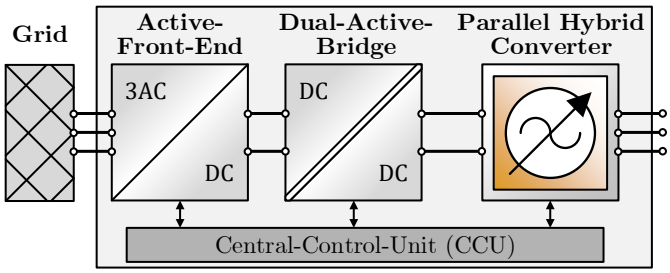


Fig. 9: Schematic diagram of the $50\,\mathrm{kVA}$ laboratory prototype

Parallel Hybrid Converter and an Active-Front-End (AFE) for bidirectional connection to the electrical power grid. A Dual-Active-Bridge (DAB) with a resonant LLC transformer provides galvanic isolation between the AFE and the PHC. The galvanic isolation is necessary since the windings of an electrical machine are also galvanically isolated and, furthermore, to avoid undesired common mode currents between PHIL test bench and DUT. All three power electronic parts of the PHIL converter system are controlled by a single CCU. Both, the closed loop control algorithms of the AFE and the PHC as well as the open loop control algorithm of the DAB are implemented in the FPGA of the CCU. For the implementation of the closed-loop control algorithms, the *HDL coder* of *Matlab/Simulink* was used.

B. Signal Processing System

The *ETI-SoC-System* was developed to be the Central Control Unit for complex converter systems. It is based on the System on Chip (SoC) *ZYNQ7030* from *XILINX* [17]. A sub-rack with two *ETI-SoC-Systems* is depicted in Fig. 10. As shown in Fig. 11, the *ETI-SoC-System* is used as the CCU of the PHIL converter system and as the RTSS for the PMSM and PHIL model computation. The system is highly adaptable due to its eight expansion card slots. To increase the number of expansion cards or to increase the computation power, multiple *ETI-SoC-Systems* can be coupled together via four high-speed $6.25\,\mathrm{Gbit\,s^{-1}}$ GTX transceivers. The analog signals of the

Fig. 10: Sub-rack with power supply PCB on the left side and two *ETI-SoC-Systems* with different expansion cards

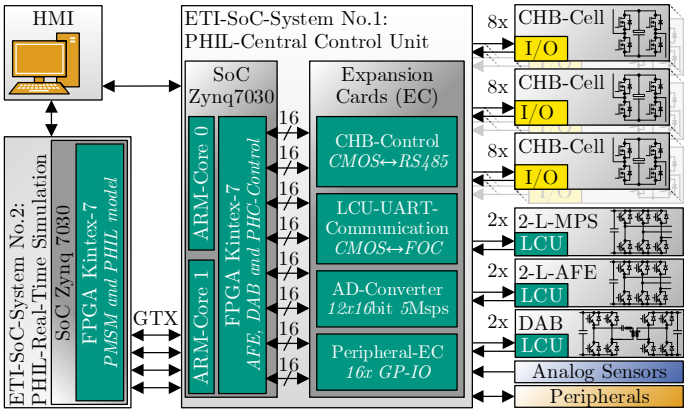
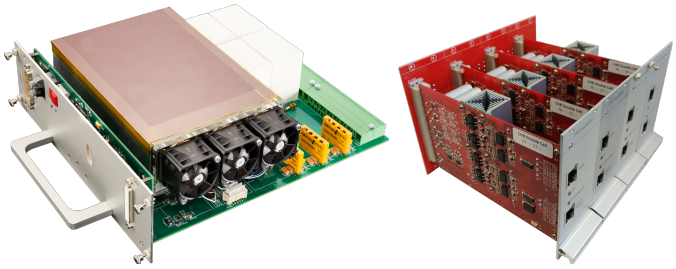


Fig. 11: Detailed control structure of the PHIL laboratory prototype using one ETI-SOC-SYSTEM as CCU and one as PHIL RTSS



(a) Single-board converter equippable with one IGBT- or SiC-B6-bridge (b) Four Double H-Bridge PCBs with backplane PCB

Fig. 12: Power electronics components of the 50 kVA PHIL emulation converter laboratory prototype

various current and voltage sensors are digitized by a 12-channel ADC expansion card with low dead time ($\approx 400\,\mathrm{ns}$), as it is required for high performance PHIL applications.

C. PHC Power Electronics

Fig. 12b) depicts one phase of the CHB. It consists of four developed Double H-Bridge PCBs in single-height *EUROCARD* format ($100\,\mathrm{mm} \times 160\,\mathrm{mm}$) connected in series via a backplane PCB, leading to a $2 \cdot n_{\mathrm{Cell}} + 1 = 17$-level CHB output voltage. Since the aimed application of the PHC prototype is PHIL, a very low dead time ($< 1\,\mu\mathrm{s} - 10\,\mu\mathrm{s}$) of the overall system is crucial [1,8]. Therefore the CHB cell's gate drivers and ADCs are directly controlled by the CCU. The Local Control Units (LCU) on CHB cells typically used for CHB or MMC topologies are omitted. *RS-485* and twisted *Cat6e* cables are used for the signal transmission to the CHB cells. Two of the single PCB 2-level converters in double-height *EUROCARD* format ($233\,\mathrm{mm} \times 280\,\mathrm{mm}$) depcited in Fig. 12a) are used in parallel with their own coupling inductors as MPS. The converter can be equipped with either the *Wolfspeed* Silicon Carbide (SiC) MOSFET module *CCS050M12CM2* or the *Infineon* Si-IGBT module *FS75R12KT4* and has a rated output power of 25 kVA. The dead time of the MPS is less crucial and its *Intel MAX10* FPGA based LCU receives the reference switching states from the *ETI-SoC-System* by a universal asynchronous receiver-transmitter (UART) based serial communication via fiber optic cables (FOC). The LCU of the MPS monitors the three output currents, the DC link voltage and the power module temperature on board and transmits these values back to the CCU via FOCs.

The grid connection is also implemented with two of the 25 kVA single-PCB converters in parallel, each with its own three-phase line inductor. Two 25 kVA medium frequency transformers from *Inductron* are used for the galvanic isolation. Each of these transformers is connected to one DAB. The DABs themselves consist of two 25 kVA single-PCB converters, each operating as H-Bridge, one for the primary side and one for the secondary side.

D. Measurement results

First measurements with an ohmic-inductive load verified that the PHC behaves as in the simulation and that the implementation of the PHCs energy and current controller on the FPGA of the CCU works correctly. The CHB was completely equipped, but for the MPS only one single PCB converter was used. The DC link of the MPS was supplied with 700 V by a bidirectional 15 kW power supply (*EA-PSB 9750-60*). The parameter values of the RL-load as well as all important parameters of the PHC used for the measurements are depicted in Table II.

The measurement results in Fig. 13 show the MPS and CHB output voltages and the MPS, CHB and PHC output currents of the first phase during a 0 kW to 14.7 kW load jump, with a PHC output voltage amplitude of 300 V and frequency of $f_{\mathrm{o}} = 50\,\mathrm{Hz}$. The carrier frequency of the CHB was set to $f_{\mathrm{c,SW}} = 500\,\mathrm{kHz}$ and the measured mean switching frequency of the MPS first phase was $\bar{f}_{\mathrm{m,SW}} = 10.54\,\mathrm{kHz}$.

As expected from the simulation results shown in Fig. 7, the measurement results in Fig. 13 clearly show that the CHB output current is limited to the MPS current ripple. Thus, the

TABLE II: Measurement setup parameters

CHB Parameter	**Value**
Carrier frequency	500 kHz
Energy control frequency	500 kHz
Current limit controller sample frequency	2.5 MHz
Current boundary	20 A
Cell Number	8
Cell DC link reference value	60 V
Output voltage amplitude	300 V
Output voltage frequency	50 Hz
MPS Parameter	**Value**
DC link voltage	700 V
Coupling network resistance	7 mΩ
Coupling network inductance	160 µH
Load Parameter	**Value**
Resistance	9 Ω
Inductance	150 µH

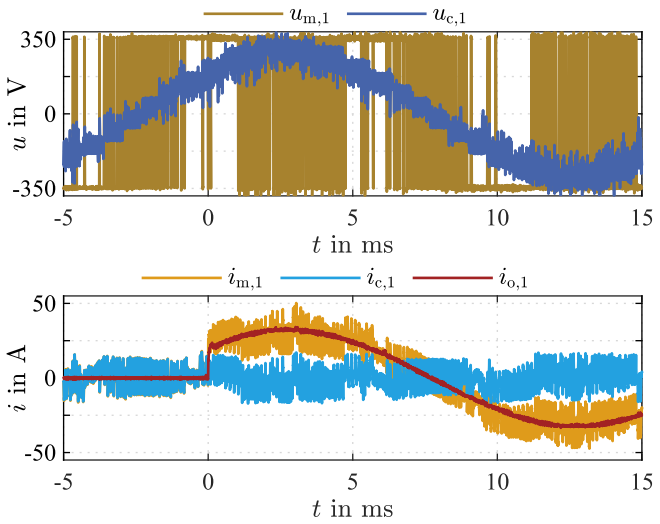


Fig. 13: Measurement results of the first phase of the laboratory PHC prototype during a load step

PHC fundamental output current is supplied completely by the MPS. Additional measurements with output frequencies of $f_o := \{0\,\text{Hz}, 20\,\text{Hz}, 50\,\text{Hz}, 500\,\text{Hz}, 1\,\text{kHz}\}$ were also carried out. In all these operating points the CHB cell voltages were kept stable in their reference value range and the CHB current was limited to the defined boundary value.

VI. Conclusion and Future Work

This paper shows the concept of a PHIL Emulation test bench for the emulation of a highly utilized, anisotropic PMSM and derives its functional principle as well as the arising requirements. It is pointed out that a PHIL converter must be capable of providing high amplitude output voltages very precisely up to 100 kHz and higher, but the required bandwidth of high amplitude output currents is significantly lower and in the range of 1 kHz to 2 kHz.

Based on this, the novel PHC topology is proposed as PHIL emulation converter. It is demonstrated that the PHC perfectly meets the requirements for a PHIL converter. The PHC inherently has a higher power density and lower costs compared to full-power multilevel converters with the same output voltage characteristics. Therefore, the PHC is ideally suited to replace conventional multilevel converter topologies used as PHIL converters, such as the MMC [1,12] or the MMPMC [8–11].

The constructed 50 kVA laboratory prototype of the PHIL test bench, the newly developed signal processing system and the newly developed power electronics hardware are presented in detail. Finally, first measurement results are shown, which verify the simulation results and confirm the correct implementation of the control algorithms on the FPGA of the CCU.

After the grid connection and the glavanic isolation have been put into operation, a second three-phase PHIL system will be integrated into the laboratory prototype in order to emulate six-phase machines.

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