

## Readout Electronics for the First Large HV-MAPS Chip for Mu3e

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Mu3e is an upcoming experiment searching for charged lepton flavour violation in the rare decay  $\mu^+ \rightarrow e^+e^-e^+$ . A silicon pixel tracker based on 50  $\mu\text{m}$  thin High-Voltage Monolithic Active Pixel Sensors in a 1 T magnetic field will deliver precise vertex and momentum information. The MuPix High-Voltage Monolithic Active Pixel Sensor combines pixel sensor cells with integrated analogue electronics and a complete digital readout. For the characterization of the first large MuPix system-on-chip a dedicated readout system was developed. The readout chain and the first results from the characterization of the large scale MuPix8 prototype are presented.

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## 1. Introduction

The Mu3e experiment [1] searches for charged lepton flavour violation in the rare decay  $\mu^+ \rightarrow e^+e^-e^+$ . In order to reject both physics and combinatorial background decay vertex, particle momenta and decay time have to be measured precisely. The Mu3e pixel detector is based on High-Voltage Monolithic Active Pixel Sensors (HV-MAPS) thinned to 50  $\mu\text{m}$ . The HV-MAPS developed for the Mu3e experiment, called MuPix, is a system-on-chip combining sensor diode, analogue and digital electronics. The MuPix chips are controlled and readout via aluminium flex-prints by the front end boards. These on detector front end boards house FPGAs which pre-process the pixel data and send it over multi Gbit/s optical links to the counting house. In the counting house switching FPGA boards of type PCIe40 [2] receive the optical data of multiple front end boards, build sub-detector events and forward the pre-processed data to the online event filter farm [3].

In the last two years, the first prototype with full system-on-chip functionalities was tested successfully [4, 5]. This year the first large MuPix prototype with full pixel column length, the MuPix8, is under investigation. The MuPix8 chip has about  $1 \times 2 \text{ cm}^2$  active area, which is almost the full length and half the width of the final sensor envisioned for the Mu3e experiment. For the sensor characterization of this complex ASIC, a dedicated readout chain was developed which is based on an ASIC test board with ultra clean power distribution and a commercial FPGA board. The FPGA controls the MuPix chip via an SPI protocol and receives a continuous serial data stream from the MuPix at 1.25 Gbit/s. The system has been successfully integrated in laboratory test setups and is used to build test beam telescopes with four MuPix8 planes.

The dedicated readout chain and first results from the characterization of the first large scale MuPix prototype are presented.

## 2. HV-MAPS

HV-MAPS combine a fast readout with a very low material budget. A bias voltage of  $-85 \text{ V}$  is applied and generates a small depletion zone ( $\approx 10 \mu\text{m}$  for  $20 \Omega \text{ cm}$  substrate resistivity) which leads to fast charge collection well within 1 ns when an ionizing particle passes through the chip. Most of the substrate is passive and the HV-MAPS are thinned to 50  $\mu\text{m}$ . The amplification stage is inside the sensitive pixel cell and a good signal-to-noise ratio of  $\geq 20$  is achieved [6]. Each pixel cell is connected to its readout cell placed peripherally to the pixel matrix via a separate transmission line. As the discriminator and the digital readout are physically separated from the pixel diode, digital crosstalk is reduced. The HV-MAPS chips have integrated logic for slow control and data handling as well as fast serial outputs.

### 2.1 MuPix

The Mu3e detector design requires that the MuPix chip has an active area of  $2 \times 2 \text{ cm}^2$ ,  $80 \times 80 \mu\text{m}^2$  pixel size and is thinned to 50  $\mu\text{m}$  [7]. Full analogue and digital readout electronics are integrated in the MuPix, so no additional readout chip is required in the ultra-thin detector layers, see fig. 1. Each hit is converted on-chip into pixel address and time-stamp. Zero suppressed data is sent through one to three serial differential output links at 1.25 Gbit/s. The performance of small MuPix prototypes is described in [4, 5].

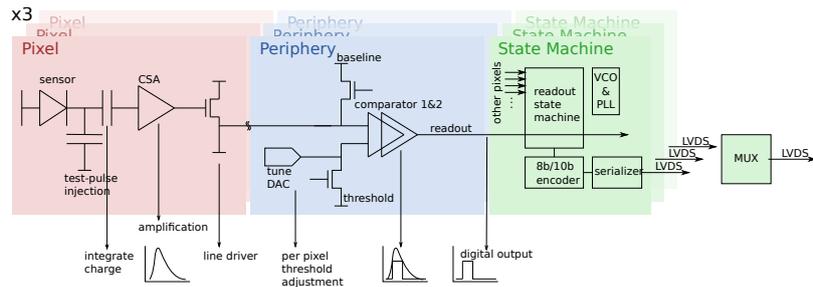
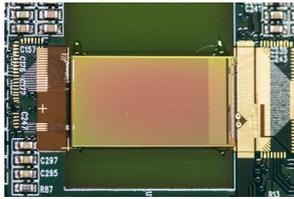


Figure 1: Block diagram of the MuPix detector-system-on-one-chip. Sensitive HV-CMOS diode, pre-amplifier shaper and analogue line driver shown left are in the active pixel cell.

## 2.2 Current MuPix prototypes

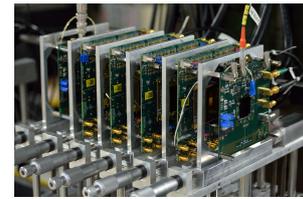
The MuPix8 is the first large MuPix prototype and has  $200 \times 128$  pixels with a size  $80 \times 81 \mu\text{m}^2$  each, see fig. 2a. It has single stage amplification for each pixel and an integrated readout state machine. Recently, the small MuPix9 prototype has been submitted. This small chip has test structures for an I2C inspired slow control and serial powering test structures which are instrumental for the pixel module integration.



(a) The Mupix8 HV-MAPS chip prototype on the insertable PCB.



(b) The Mupix8 HV-MAPS chip prototype in the single sensor test setup.



(c) MuPix8 Telescope at DESY.

Figure 2: Photos of the MuPix8 test environment.

## 3. MuPix readout electronics

In order to characterize the MuPix chips in the laboratory and at test beams a readout chain has been developed. Its main components are the MuPix PCB and an FPGA card inside a computer. The MuPix8 PCB allows to either bond the chip directly on the board or to mount the chip on the Insert PCB which can be pushed into a connector, see fig 2. The use of different Insert PCBs allows to combine the MuPix8 PCB with multiple HV-MAPS prototypes. Clean low voltage with less than  $100 \mu\text{V}$  ripple is generated with commercial power regulators. Temperature is measured by generating an adjustable current and measuring the voltage across the MuPix8 temperature sense diode. A test-pulse circuit allows to inject test pulses of adjustable height with the help of a 14-bit DAC. The four differential links for serial data output at 1.25 Gbit/s can either be probed with the help of SMA connectors or they are boosted by a repeater and transmitted over twisted pair SCSI3 cable to the FPGA card. The slow control and clock signals are also transmitted differentially over the SCSI3 cable from and to the FPGA card. The FPGA card is a commercial Altera Stratix IV

development kit, mounted in a PCIe slot of the computer. FPGA board daughter cards connect to two MuPix PCBs each and to timing reference scintillators. This modular readout system allows for control and readout of four or eight MuPix chips used as beam telescopes [8] in high rate beams.

The FPGA firmware decodes the incoming fast data stream, and separates hits from flow control and status information. Histograms of all received quantities allow to identify stuck bits and study differential non-linearities. Hits are then sorted by timestamp using a large memory block and then sent to the main memory of the readout PC using PCIe direct memory access. The PCIe interface additionally provides registers for control and status information and a memory block for the pixel configuration data.

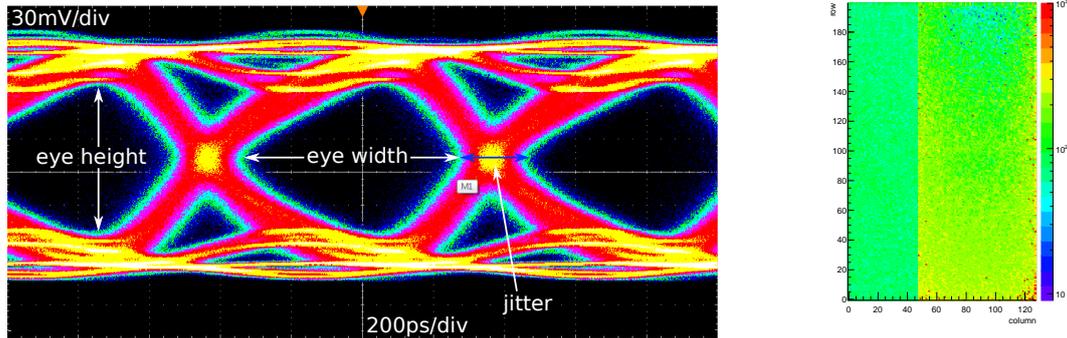
For the development of the MuPix8 FPGA firmware, the MuPix8 chip was emulated. In a first step the MuPix8 was emulated within the readout firmware. In a second step an emulation adapter PCB was plugged into the MuPix8 PCB and connected to a second FPGA. This allowed to emulate the MuPix8 with the help of one FPGA and develop the firmware for the FPGA controlling, clocking and reading out the MuPix8 and to test the full readout chain. In a vertical slice test of the Mu3e readout electronics eight MuPix8 PCBs will be connected via fast LVDS links to one Mu3e front end board which in turn pre-processes the data and sends events over multi Gbit/s optical links to a filter farm PC in the counting house.

#### 4. MuPix8 first results

Measurements with early MuPix8 samples have started. The serial data output works at 1.25 Gbit/s with successful 8b/10b encoding, the bit error rate is below  $10^{-14}$ , an eye diagram is shown in fig. 3a. The eye height for this measurement is  $199 \pm 1$  mV, the eye width  $528 \pm 1$  ps and the jitter  $45.2 \pm 0.3$  ps. After a successful setup of the slow control and the data acquisition chain the MuPix8 has been tested with a radioactive source, see fig. 3b. The MuPix8 has three pixel matrices, the left one uses voltage driven signal lines from the pixel cells to the periphery, the right ones current driven signal lines, which leads to a different response to the  $^{90}\text{Sr}$  source at the same global bias current and threshold settings. All pixel cells are responsive. The characterization of the MuPix8 chip during testbeam campaigns at DESY has started and preliminary results indicate good efficiencies and time resolution.

#### 5. Conclusions

A versatile readout system for the first large HV-MAPS chip for Mu3e has been developed. This readout system ensures the controlled operation of the MuPix8 system-on-chip prototype including very clean low voltage, temperature monitoring, test-pulse injection, clock distribution, slow control and high-speed data acquisition. The readout system can handle up to eight MuPix chips which allows to operate them as a MuPix Telescope in high rate test beams. Measurements with early samples of the first large MuPix prototype - the MuPix8 - have shown that the high speed data outputs work reliably and all pixel cells are fully responsive. Ongoing analysis of test beam measurements indicate high efficiencies and good time resolution. In a next step the MuPix8 chip will be integrated into a vertical slice of the Mu3e readout electronics.



(a) Eye diagram for the MuPix8 serial data output at a data rate of 1.25 Gbit/s, the clock recovery module of the fast sampling oscilloscope leads to 6.6 dB damping.

(b) Hit-map for irradiation with a  $^{90}\text{Sr}$  source.

Figure 3: First tests performed with the Mupix8 chip.

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