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A Novel Receiver Design for Energy Packet-Based Dispatching

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A steadily growing share of renewable energies with fluctuating and decentralized generation as well as rising peak loads require novel solutions to ensure the reliability of electricity supply. More specifically, grid stability is endangered by equally relevant line constraints and battery capacity limits. In this light, energy packet-based dispatching with power signal dual modulation has recently been introduced as an innovative solution. However, this approach assumes a central synchronicity provision unit for energy packet (EP) dispatching. To overcome this assumption, the present article's main contribution is a design of an EP receiver which recovers the required synchronicity information directly from the received signal itself. Key implementation aspects are discussed in detail. By means of a direct current (DC) grid example, simulation results show the performance and applicability of the proposed novel receiver for packet-based energy dispatching.

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1. Introduction

Today's electricity grid is based on the equilibrium principle, i.e., the amount of power generated corresponds to the power consumed at every instant of time. Due to the steadily growing number of renewable energies with fluctuating and decentralized generation as well as increasing peak loads due to the rising use of electric vehicles and heat pumps in the context of the energy transition, it is increasingly challenging to guarantee this instantaneous balance while considering local constraints. Demand Response (DR), Demand Side Management (DSM), and Energy Management Systems (EMS) can be considered as potential solutions to this challenge, at least in the short term.[1–4] Unfortunately, the possibilities for load-shifting in today's power grids are limited due to equally relevant line constraints and battery capacity limits. For a long-term solution, it is therefore necessary to consider completely new concepts, which operate without overall synchronicity between generation and consumption.

A packet-based energy distribution concept, as presented, e.g., in refs. [5,6], can be one of such long-term solutions. Inspired by the Internet Protocol (IP) known from modern communication technologies, an asynchronous energy distribution is a promising option to solve the problem described earlier and to make the entire power-distribution network future-proof. Equivalent to the data packet from the IP, an energy packet (EP) is defined as the key element in this concept. An EP itself is a defined amount of energy that is exchanged within the distribution network between source and sink asynchronously according to demand or availability. In combination with energy storage elements, this approach enables energy transmission based on the store-and-forward principle known from the IP. The two characteristics of this concept, namely the EP definition and the store-and-forward principle, result in two major advantages which contribute significantly to the improvement of the energy supply infrastructure: 1) creating a clear decoupling between demand and generation; 2) always allowing the best use of the infrastructure capacity, i.e., line limits and storage capacity.

Although in ref. [5], the vision and the underlying theoretical considerations are presented in detail, in ref. [6], a possible solution for the realization of EPs and their transmission via a direct current (DC) grid is described. Thereby, for successful transmission of EPs, synchronicity on the data level is assumed.

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The present contribution significantly extends[6] by designing the solution of a practicable receiver for EPs. The synchronization necessary for the detection of the information part of the EP is derived from the received packet itself. This means that the previous central synchronization prerequisite is no longer necessary and the EPs can therefore be exchanged asynchronously over the distribution network, as demonstrated by the simulation results in Section 5.

This article is organized as follows: Section 2 introduces the concept of packet-based energy distribution and outlines the basic idea of power signal dual modulation (PSDM) for packet-based energy distribution. Furthermore, the advantages and disadvantages of related solutions are discussed. In Section 3, the basic idea of a PSDM transmitter is outlined. Section 4 describes in detail which steps have to be taken in the communication part of the PSDM receiver to transmit EPs without global synchronicity and how the required point-to-point synchronization between the participants can be achieved from the received signal. In Section 5, the simulation results are summarized. Finally, the main conclusions and an outlook are provided in Section 6.

2. Packet-Based Energy Distribution

2.1. Concept

Figure 1 visualizes the concept of packet-based energy distribution in a simplified form. Each participant of this simple energy-distribution network is connected to a DC bus either via DC/DC (see G1, L1, and L3) or DC/AC converters (see L2). The generator G1 supplies the DC bus with a constant DC voltage V_{G1}. Communication paths are represented by transceiver blocks Tx/Rx. All loads are in standby at initial time t_0, i.e., the respective input impedance of the converters is very high and no current flows. At time t_1, an EP is transmitted to the load L_3. For this purpose, the load L_3 is informed via a communication path that it should switch to the current consumption mode for the duration T_{L3}. For the duration T_{L3}, a current I_{L3} flows. This process could be interpreted as an EP transmission procedure:
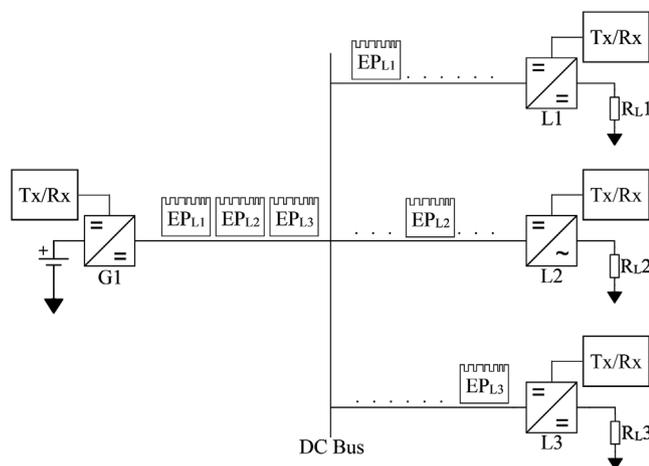

Figure 1. Concept of packet-based energy distribution.

$$EP_{L3} = \int_a^b v(t)_{G1} i(t)_{L3} dt \tag{1}$$

Clearly, the same principles apply to the transmission of EP_{L2} at t_2 and EP_{L1} at t_3. Taking the concept shown in Figure 1 as a basis, it becomes clear that an EP is a combination of the energy flux and the data necessary to transmit an EP to the destination load. The minimum data are the address of the destination and the size and duration of the energy packet. In a more advanced network, where several intermediate transmissions between the source and the destination may be necessary, additional information such as the address of the intermediate destination, number of hops, etc. may also be required. Note that the power part of the energy packet transceiver does not necessarily have to be implemented as a DC system. AC systems with fixed or variable frequency are also conceivable. The only requirement is an inverter suitable for the application needs. The exemplary specification on a DC bus presented in the following is only due to the coherence to the previous publications.

2.2. Related Research

One of the first publications of packet-based energy dispatching was published in 1997 by Saitoh et al.[7] (called "power packets" in the article). Authors proposed an electric power dispatching as a packet of energy tagged with the dispatching information. The study produced a number of promising results, but was not followed up due to technical feasibility of that time. In ref. [8], an architecture based on EP was proposed as possible approach to energy dispatching. The article introduces an elemental circuit for power routing with EPs which relies on resonance initiated by Silicon Controlled Rectifier (SCR) switching. Nevertheless, the proposed strategy is quite limiting because there is no clear specification of the EP and the information exchanged among the elements of the microgrid. Moreover, a lockout circuit ensures that multiple devices can never command an EP at the same time.

A rudimentary outline of the packet-based energy transfer idea is also given in ref. [9]. In the article, it is pointed out that the Digital Grid Consortium wanted to digitize the japanese power grid. The gradual conversion of the existing synchronous grid into asynchronous, autonomous, but interconnected cells of different sizes is presented as a goal. Unfortunately, no discussion of how the idea should be implemented is given. Basically, the article contains very few technical details. It is described that a 2 kW proof-of-concept "digital grid router" (DGR) has been developed and that it consists of a solid-state AC/DC/AC converter using insulated gate bipolar transistor and a Central Processing Unit (CPU), memory, data storage, and network communications. However, how DGR operates or what the overall concept looks like is not discussed.

A more extended vision of a packet-based electrical grid has been presented in ref. [10], where a wide-area power system is considered to be subdivided into cells, called digital grid cells, asynchronously interconnected by means of DGRs. The DGRs are characterized by a multileg AC/DC/AC conversion with a Central Processing Unit that coordinates the power and the information and that controls the terminals. The article

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demonstrates that in the proposed digital grid, the active and reactive power can be controlled independently. The active power can be exchanged among the DGRs in the form of a packet of energy and the reactive power can be used to maintain the voltage to the specific set-point, given that DGR allows the decoupling of the two sides of the converters through the DC conversion stage. The digital grid is managed by the digital grid controller (DGC) that interacts with the DGR and other DGSs by sending information on the status of the grid and the commands to the controllers of generators, loads, and energy storage units. This innovative approach shows a general vision of a possible AC digital grid and how the digital grid can utilize the existing grid components; however, it does not analyze the dispatching of the packet and the coordination of the information among the DGRs.

An original solution for the generation and dispatch of EPs—also called "power packets" in the respective articles—is described in refs. [11-13] and supported by experimental results. The authors presented a new system for energy dispatching based on the definition of mixer and router. The mixer is a power electronic device that collects the sources and dispatches the EP. The router stores the received EP and dispatches it toward the assigned loads. However, this configuration identifies a completely new structure of the electrical grid that is incompatible with the existing one and thus makes it difficult to deploy the concept. In addition, multiple connections of the mixers is prohibited.[11]

Even most recent publications address the concept and the advantages of packet-based energy dispatching.[14,15] In ref. [14], it is pointed out that thanks to the wide bandgap semiconductors (WBG) much higher operating frequencies can be achieved than before. Various advantages and possible future applications are discussed. One of them is Packetized Energy and Peer-to-Peer Energy Exchange. It is emphasized that DERs will only fully realize their benefits if energy can be exchanged between participants in a truly independent manner. Unfortunately, ref. [14] contains no concrete solution for this challenge. As a possible implementation, the concept of refs. [11–13] is suggested. As a consequence, the same problems as described earlier arise and the approach requires a radical redesign of the grid.

The authors of ref. [15] claim that the future power grids should have similar qualities of self-organization and robustness as the Internet. To achieve this, the differences and similarities between data and power dispatching are first discussed. The article shows why the Internet as a set of hierarchically structured subnetworks with its layer principle is future-proof and where the existing distribution grid will have problems in the future and what challenges need to be overcome to make the power supply grid as intelligent as the Internet. Based on the fact that the future grid consists of several micro grids as well as Building Energy Management Systems (BEMS) and Neighbourhood Energy Management Systems (NEMS), it is proposed to integrate them into the global power grid as self-managing networks and thus create a similar structure of "networks of networks"[15] Unfortunately, this publication does not present a systematic solution how to achieve this. The problem of close coupling of networks by tight operating frequency is also left out of consideration.

In contrast to the discussed articles, which mainly concentrate on isolated solutions of single elements and are usually strongly disciplinary oriented, we propose with refs. [5,6] and the present article a systematic, interdisciplinary approach, which focuses on three core objectives: The increase in robustness and stability of the power grid and a close-to-maximum use of line capacities. The concept presented in ref. [5] aims to transform the current closely coupled power grid into a network of subnetworks to increase its robustness and stability in the long term. In addition, electricity is to be transmitted on the basis of EPs to increase flexibility and thus to achieve a close-to-maximum use of line capacities—starting in the distribution grid which will come to its limits when, e.g., all houses have PV on their roofs, heat pump usage, and electromobility connected to them (Then classical dispatching will not work anymore as the prices will be too high to heighten the grid capacities). At the same time, we are not proposing a radical break with the existing power grid. With the implementation solutions presented in ref. [6] and in the present contribution, existing power grids can be extended or gradually replaced by packet-based transmission technology.

2.3. EPs Metadata Providing Strategies

The information path for the control of the EP transmission mentioned earlier can be realized in various ways. The use of industrial or conventional wired communication technologies such as EtherCAT or IEEE 802.3(xx) is conceivable. However, this approach results in significant additional installation and cost effort and is therefore not practical in every section of an energy distribution network.

Wireless low-rate communication technologies such as IEEE 802.15.4, Z-Wave or EnOcean for low-rate wireless personal area networks (LR-WPAN) could be a possible solution for dedicated power-distribution network subsections such as a house, an industrial building or an industrial plant.[16–18] These are known among others from several applications in the field of Smart Homes and Home Automation and are becoming more and more popular. These communication technologies provide sufficient high bandwidths for the applications mentioned, have low production costs, and enable the plug-and-play expansion of the communication network without installing additional cables.

As described in ref. [19], all these low-cost and low-power radio communication standards unfortunately also have some critical disadvantages that make the use of these techniques problematic in the context of EP transmission. Due to the very low transmission power defined by the respective standards and the cost-effective design of the transceivers, the established network is very sensitive to any kind of interference and multipath influences, which are always present in buildings and industrial plants.[20] Therefore, a network created by these communication techniques is called a Lossy Network, i.e., a high number of lost information packets is expected by definition. This is also reflected in the name of the Routing Protocol for Low power and Lossy Networks (RPL).[21] Due to the desired high degree of reliability of the power distribution network, lossy networks are not appropriate in this case. In addition, the coverage of such networks is relatively small.[20,22] Moreover, building topologies such as steel concrete ceilings or electromagnetic shielding are challenging as they can lead to nonaccessibility of net-elements by radio. Especially, many

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large loads or generators are installed in rooms with electromagnetically shielding walls. Even in industrial plants, large loads or generators are often not easily accessible by radio.

However, in most cases, a power outlet is within reach. As all participants of the power distribution network have to be connected to the powerline, Powerline Communication (PLC) is a natural choice for the transmission of the control data at least within certain subsections with a limited extension and a relatively manageable number of participants.

The PLC techniques themselves can be divided in two groups: Broad Band–Powerline Communication (BB–PLC) and Narrow Band–Powerline Communication (NB–PLC). In Europe, BB–PLC communications technology operates in a frequency band between 1.6 and 30 MHz and can provide data rates of several gigabit per second (Gbps).[23] However, as these data rates can only be achieved under optimal conditions and are not n ecessary for the transmission of EPs, and the BB–PLC transceivers are significantly more expensive in production than NB–PLC transceivers, the use of this technology is not considered. In contrast to BB–PLC, NB–PLC technology operates in a frequency band between 3 and 500 kHz and provides data rates of up to 1 Mbps, depending on the communication standard and frequency band. The coverage radius is between 100 m and several kilometers, depending on the standard used.[23,24] Therefore, NB–PLC is definitely a promising technique in the context of grid element control and smart grid applications, as demonstrated in several studies.[25–27] Unfortunately, the European Committee for Electrotechnical Standardization (CENELEC) comparatively limits the permissible frequencies and transmission powers for NB–PLCs in Europe to a very high degree, thus immensely limiting the achievable transmission rates. The European standard (EN) defines the in-band and out-of-band emission limits and states that the CENELEC A band (3–95 kHz) is reserved for energy suppliers and that only the CENELEC B-D bands (95–148.5 kHz) may be used by consumer installations.[28] Due to these restrictions, conventional NB–PLC technology operates in Europe exactly within a frequency band where the power electronics required for generating the EPs have the maximum disturbance emission, and consequently, communication is vulnerable to the switching frequency noise.

In refs. [11-13,29,30], a completely different approach to the unique tagging of EPs is pursued. Central aspect of the proposed solution is that the meta information required for distribution is achieved by binary amplitude shift keying (ASK) of the supply voltage in the baseband as a binary line code. As the information is transmitted in the baseband, this approach does not require carrier recovery and only the bit clock recovery is required to synchronize the participants. This can be done as described in refs. [29,30] using a conventional or a fully digital phase-locked loop with phase-frequency error detector. However, the hard keying of the supply voltage (with a high energetic potential) causes an immense broadband spectral interference, the parts of which are radiated via the power lines. Furthermore, the integration of this approach into conventional power distribution systems (DC and AC)—as the authors in ref. [11] themselves write—is clearly impossible. This is the main challenge to be addressed in a practical system.

2.4. PSDM-Based PLC for EP Distribution

To overcome this problem, PLC based on PSDM was proposed in the articles.[6,31–33] With PSDM, the information signal is embedded into the power signal by manipulating the pulse width modulation (PWM) signal of the power converter. Either the phase or the frequency of the PWM signal can be manipulated to inject the information. In this way, both data modulation and power conversion are implemented in a single electronic circuit and no explicit analog front-ends or coupling units are required as in conventional PLC transmitters. This simplifies the system structure and minimizes implementation costs.

The article,[6] on which the present contribution is based on, describes exactly how EPs can be generated and transmitted using PSDM technology. However, the article does not answer how the synchronization required for processing the information part of an EP can be achieved. Other publications dealing with PSDM also do not give a satisfactory answer to the problem of synchronization in the receiver. For example, the theoretical demodulation process of a Differential Binary Phase-Shift Keying (DBPSK) is described in ref. [34] and it is also pointed out that the symbol clock is crucial for the demodulation of the data, but at the same time it is written: "Still, bit-synchronization is required, which can be easily achieved by program". However, as described in Section 4 bit-synchronization or more precisely symbol-clock recovery is not an easy procedure at all, and is essential for processing and interpreting the received information. In ref. [32], a Phase-Shift Keying/Direct Sequence Spread Spectrum (PSK/DSSS) modulated signal with suppressed carrier is coherently demodulated. The authors noted that accurate information about the frequency and phase of the carrier is necessary to demodulate the data. To obtain this information, they propose to transform the received PSK/DSSS signal simply into the frequency domain without any preoperation. However, a nonlinear operation has to be applied to a suppressed carrier information signal first to obtain a clear spectral line of the carrier, as can be found in refs. [35,36].

Furthermore, another essential component of a receiving unit, the Adaptive Gain Control (AGC), has been completely disregarded in all cited articles, whereby in all of them the interpretation of the data depends on a normalized level.

Hence, the present contribution discusses possible solutions for synchronization and level stabilization in the information path in the context of packet-based energy distribution based on PSDM.

3. PSDM Transmitter for EP Generation

To provide an input signal for the implemented receiver, a PSDM-based generator for EPs as proposed in ref. [6] is realized. **Figure 2** shows the structure of this generator.

As the name implies, the generator performs two tasks: First, it acts as a buck converter, which supplies the DC bus with a constant DC voltage and the energy during the EP transmission phase. Second, it also acts as an analog part of a powerline transmitter by injecting the information signal into the power line without additional circuits such as an analog front-end or
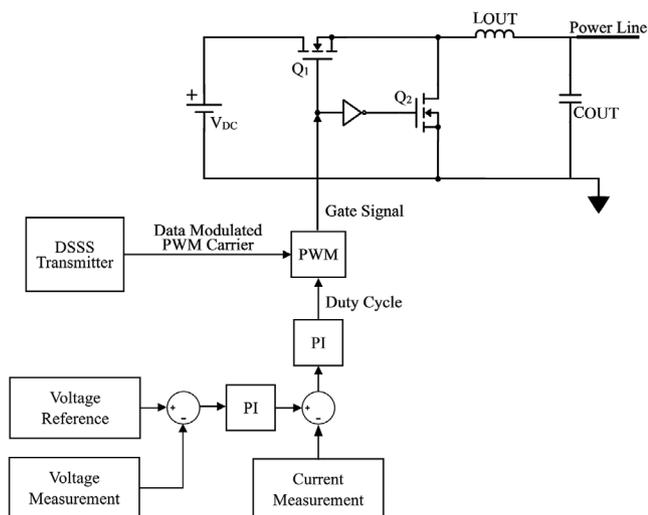
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Figure 2. Block diagram EPs Source.

coupler. A short explanation of the functional principle follows. The theoretical basics are explained in detail in refs. [5,23].

As shown in Figure 2, the information signal is embedded in the power signal by manipulating the phase of the triangular carrier signal for PWM generation used to control the power transistors. More precisely, the phase of the PWM signal is manipulated using DBPSK modulation and DSSS technology. The use of DSSS transmission technology makes it possible to secure the data connection against the pulse interference and multi-path propagation strongly represented within the power line and thus to design the control path reliably.[37,38] It also ensures a certain level of security, as only the load that knows the corresponding despreading sequence can decode the data. For this purpose, the information data to be transmitted are first

DBPSK-coded, then spreaded with an orthogonal pseudo-random sequence based on the Walsh–Hadamard matrix and finally modulated onto the triangular carrier. As a consequence, the output voltage of the power converter is superimposed with the information signal. That is, the existing ripple of the DC voltage of the power converter no longer represents only the unwanted noise: it is used constructively for the information transmission. The transmission signal is available as a broadcast signal to all devices connected to the bus, whereby only if the participants actively listen to it and also have the correct encryption code, they can decrypt and handle the information.

In the following simulation, the output signal of this generator serves as input signal for the realized receiver.

4. Receiver for the Information Part of EPs

Figure 3 shows the implemented PLC receiver. In principle, every receiver and also the implemented PLC receiver is a transmitter backward that contains some additional elements, especially several indispensable synchronization units. These are necessary because the receiver generally has no precise information about the symbol, i.e., chip clock, frequency and phase of the carrier and the start point of the data packet. Furthermore, the receiver has to derive this information from the received signal itself. In addition, the clock elements in both the transmitter and receiver have a certain temperature drift, manufacturing tolerances, aging phenomena, which cause a variable time offset.[39]

The resulting time errors have an influence on the signal level within the digital signal processing and can significantly influence the reception quality or even make data transmission impossible.[36] Therefore, the receiver has to perform at least the following synchronization tasks for a successful data
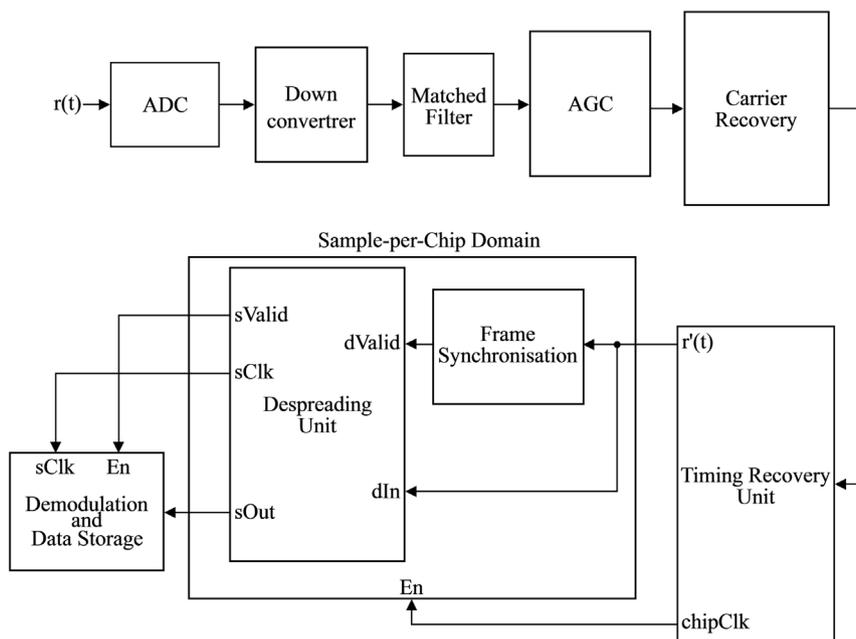

Figure 3. Block diagram PLC receiver.

transfer[35,36,40]: 1) Carrier synchronization; 2) Timing recovery and 3) Frame synchronization.

In general, two additional synchronization stages are required for direct spread spectrum systems: Code acquisition and Code tracking.

However, these are only indispensable if one has to deal with strong frequency-selective interference or if one wants to implement a system with code multiplexing media access. However, as we primarily use spread-spectrum technique to assign the messages to the respective load and our intention is to show that the synchronization approaches presented afterward can also be used for PSDM, we can skip with these two synchronization stages in the first step. This is possible because a DBPSK/DSSS signal can be treated for synchronization purposes as a pure DBPSK signal with a data rate increased by the spreading factor (SF). Furthermore, the synchronization approaches described in the following are so generically implemented that they can be modified to a strict DSSS solution with a manageable effort. Among the required adjustments are the replacement of the timing-error detector (TED) by a code phase error detector, the addition of a code acquisition unit and the calculation of the carrier phase error using the despread symbols and not the baseband signal. Thus, the solutions shown in this article can be considered as the basis for further synchronization steps.

Next, the realized synchronization levels are explained in detail. The corresponding simulation results follow in Section 5. The description of the general elements of the receiver, such as matched filter, demodulation unit, etc., which form the counterpart to the transmitter, is omitted, but reference is made to further literature where these elements are described in detail.[35,36,41]

4.1. Adaptive Gain Control

Phase Locked Loop (PLL)-based synchronization algorithms require a constant average signal energy, as this influences the K_p factor of the Phase Error Detector (PED) or TED.[41] The level of the threshold value for frame synchronization also depends on the average signal energy of the incoming signal.[42] Thus, a constant signal level is a critical parameter for the realization of a digital transmission system. This is ensured by the AGC unit.

As shown in Figure 3, the signal level correction via AGC takes place in the baseband, i.e., after the down-conversion of the input signal, but before any synchronization. At this point the signal can be described by

$$u(k) = A(k) \cdot e^{j\phi_r(k)} \tag{2}$$

where $u(k)$ represents the input signal, $A(k)$ the amplitude of the symbol, and $\phi_r(k)$ the phase of received symbols. Due to the variable distance between the transmitter and receiver, the used transmission power as well as different attenuation influences within the channel, the amplitude $A(k)$ of the signal is variable and even time-variant. To compensate this variance and to adjust the signal level to the reference level, the AGC unit is used. Following difference equations describe the implemented Least Mean Squares (LMS) signal level adaptation algorithm

$$x(k + 1) = x(k) \cdot (1 - \alpha|u(k)|) + \alpha R \tag{3}$$

$$y(k) = x(k) \cdot u(k) \tag{4}$$

where

$u(k)$ represents the complex input signal
R represents the reference signal level
α represents the step size
$x(k)$ represents the divide by factor
$y(k)$ represents the output signal of the AGC

To ensure a constant signal level, the magnitude of the AGC output signal $y(k)$ is compared with a reference signal level R. If the output signal level is too high (low), a negative (positive) signal is fed back, reducing (increasing) the gain. The control parameter α regulates the amplitude of the feedback signal and is used to control the AGCs time constant.

Corresponding to Equation (3), the calculation of the absolute value of the complex input signal $|u(k)|$ for determining the amplitude of the input signal is a nonlinear process, so the resulting equation is also nonlinear. However, based on the assumption that the system is driven by a step $u(k) = c_k$ with $c_k > 0$, the nonlinear equation becomes a linear difference equation

$$x(k + 1) = x(k) \cdot (1 - \alpha c) + \alpha R \tag{5}$$

From this solution follows that in steady state, the gain is $x(k) = \frac{R}{c}$ and the system time constant is $\tau = \frac{1}{\alpha c}$.

4.2. Carrier Synchronization

A phase deviation of the local oscillator of the down-converter from the carrier wave regardless of whether time-variant or not causes an offset (if time-invariant) or rotation (if time-variant) of the received symbols in the symbol domain.[40] **Figure 4** shows
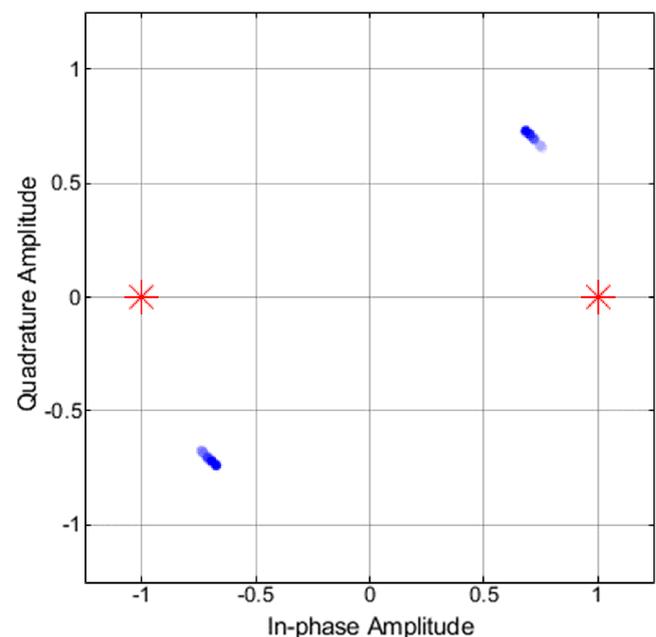
Figure 4. Deviation of the symbols from the nominal value when there is a phase offset between the local oscillator and the carrier wave.

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an example of such a time-variant deviation of the received symbols (blue) from the expected symbols (red). At the shown snapshot, the phase shift of the symbols is $\approx 45°$. If the offset is large enough—in the case of the BPSK more as $+/- 90°$ a wrong symbol will be detected.

The task of carrier synchronization is to keep this phase offset as low as possible. In principle, carrier synchronization is a process of tracking the frequency or phase of the local oscillator to the frequency and phase of the carrier wave. This can be undertaken in different ways.[36,40,41] To avoid the need for additional frequency offset estimation and to keep the complexity of the receiver as low as possible, a PLL-based decision-feedback carrier synchronizer is implemented. This has the advantage that it can correct both phase and frequency offset at least within a limited range. As shown in **Figure 5**, the implemented carrier synchronization unit consists of a carrier PED, a loop filter $F(z)$, a phase error accumulator as well as a phase rotator.

The carrier PED determines the phase error between the carrier wave and the local oscillator. The loop filter removes the unwanted high-frequency signal components and generates the corresponding control signal for the phase error accumulator. The phase error accumulator is responsible for determining an accumulating phase error. The phase rotator eliminates the estimated phase error.

Since the functionality of the used Proportional Integral (PI) loop filter and phase error accumulator is known from discrete PLLs, only the principle of the used carrier synchronization and the functionality of the implemented carrier PED are presented in the following. For the general functionality of the loop filter and phase error accumulator, please refer to the further literature.[41,43]

The received signal can be described by

$$r(t) = G_a \sum_k \{i(k)p(t - kT_s) \cdot \cos(\omega_0 t + \varphi_e)\} + w(t) \qquad (6)$$

where the representations are
  G_a gains and losses of the signal
  $i(k)$ k-th chip
  $p(t)$ unity-energy pulse shape
  φ_e unknown combined phase offset
  T_s sample period
  $\omega_0 t$ angular frequency of carrier wave
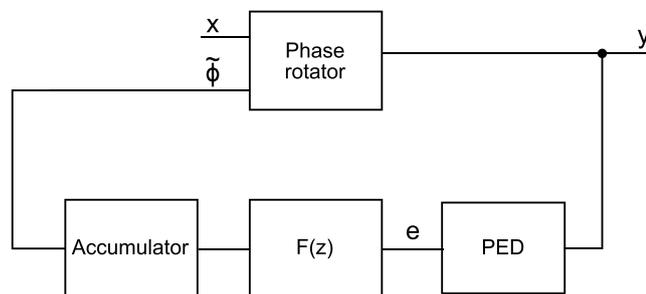 $w(t)$ additive white Gaussian noise

Figure 5. Carrier synchronization unit.

Without loss of generality and for simplicity, only the part of the overall function that is relevant for carrier synchronization is used in the following:

$$r(k) = i(k) \cdot \cos(\Omega_0 k + \phi_e) \qquad (7)$$

The combined phase shift $\phi_e = \Delta\omega t + \Delta\phi$ consists of a possible frequency shift $\Delta\omega$ and a constant phase shift $\Delta\phi$ between the carrier wave and the local oscillator. To eliminate ϕ_e, an asynchronous shift of the passband signal into the baseband is first performed by means of the down-converter using a complex signal $s(k) = 2e^{-j\Omega_0 k}$, cf. Figure 3

$$r_{bb}(k) = r(k) \cdot s(k) = i(k) \cdot \cos(\Omega_0 k + \phi_e) \cdot 2e^{-j\Omega_0 k} \qquad (8)$$

The double-frequency components resulting from the multiplication are then eliminated by the matched filter and the following relation is obtained

$$x(k) = i(k) \cdot e^{-j\phi_r} = |i(k)|e^{(j\phi_d)} \cdot e^{-j\phi_e} \qquad (9)$$

This means that the symbols $x(k)$ of a signal mixed down asynchronously are shifted in the symbol domain by phase offset ϕ_e from the nominal position ϕ_d of the symbols as shown in Figure 4. The phase error increment that occurs during a single chip interval is calculated in the implemented PED as follows

Angle of the received symbol

$$\phi_r = \tan^{-1}\frac{\text{Im}(\gamma(k))}{\text{Re}(\gamma(k))} \qquad (10)$$

Angle of the nearest possible symbol

$$\phi_d = \tan^{-1}\frac{\text{Im}(\gamma_d(k))}{\text{Re}(\gamma_d(k))}$$
$$= \tan^{-1}\frac{0}{\text{Re}(\gamma_d(k))} \qquad (11)$$
$$= \tan^{-1}\frac{0}{|i(k)| \cdot \text{sgn}[\text{Re}(\gamma(k))]}$$

Resulting phase error

$$e(k) = \phi_r - \phi_d = \tan^{-1}\frac{\text{Im}(\gamma(k))}{\text{Re}(\gamma(k))} - \tan^{-1}\frac{0}{|i(k)| \cdot \text{sgn}[\text{Re}(\gamma(k))]} \qquad (12)$$

The resulting correction phase is then formed using the phase error accumulator by integrating the phase error; subsequently the phase rotator eliminates the offset. **Figure 6** shows the S-Curve of the PED. Observe that the S-Curve has two stable locking points at $\phi_e = 0$ and $\phi_e = \pm\pi$. Therefore, a phase ambiguity of π exists. This disadvantage is eliminated by difference coding in the transmitter, as mentioned in Section 3.

4.3. Timing Recovery

The output of the matched filter must be sampled periodically at the corresponding chip (A chip is a single elementary modulation state within the DSSS. The sequence of different chips is determined by both the spreading code and the transmitted
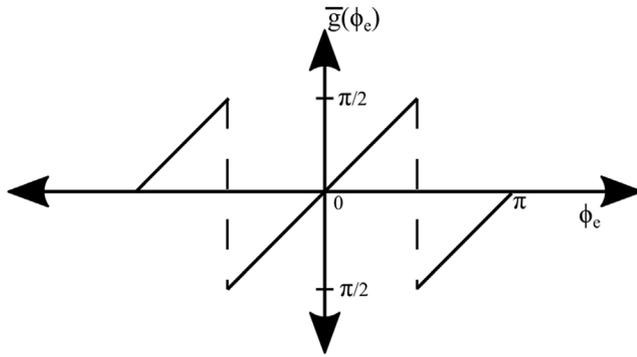
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Figure 6. S-Curve PED.

symbols. The chip rate of the spreading code is typically higher than the symbol rate. The ratio between chip rate and symbol rate is called SF and is defined as: $SF = \frac{R_c}{R_s} \gg 1$.) rate f_c at time $t_k = kT_c + \tau$, where T_c describes the chip period and τ the time delay due to the signal propagation between the transmitter and the receiver. Since τ is generally unknown and T_c in the transmitter and receiver are not completely identical, e.g., due to production tolerances of the clocking elements or thermal variance,[39] the optimum sampling point is generally unknown. Not sampling the output of the matched filter at this optimum sampling point t_k and with the locally generated asynchronous sampling frequency $\widetilde{f_c}$ results in periodic degradation of the signal level, leading either to a wrong symbol decision or to temporary full signal loss,[36,40] cf. Figure 16 in Section 5.

The task of the Clock Recovery Unit (CRU) is to find this optimal sampling point, i.e., to synchronize the receiver with the received signal. Note that as both the installation of a separate clock line between all devices and the reduction of the available signal power (respectively transmission bandwidth) in favor of an explicit clock signal are not viable options, the symbol clock must be derived from the received data. This can be executed both in the time-continuous domain and in the time-discrete domain.[41] In the presented article, a time-discrete solution first introduced by Erup and Gardner is implemented.[44,45] **Figure 7** shows the block diagram of the implemented clock synchronization unit. This consists of a third-order Fractional Delay Filter, a Gardner TED, a loop filter, and a Timing Control Unit (TCU).
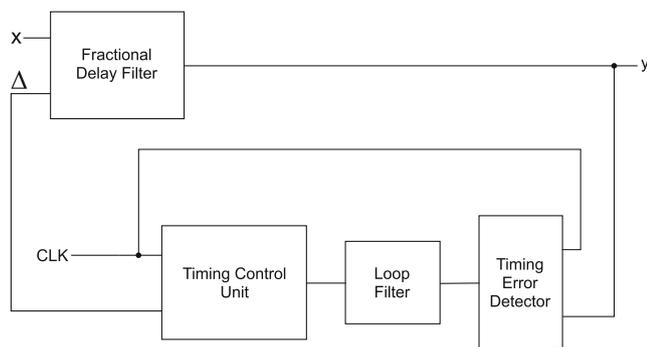

Figure 7. Timing Recovery Unit.

In the first step, the received continuous signal is oversampled discretized with a fixed asynchronous local frequency $f_s = 1/T$. Then, with the aid of the down-converter, it is mixed down into the baseband area and fed to the matched filter. After signal level correction in the AGC and carrier synchronization, the signal can be described as

$$x(kT) = \sum_n i(n) \cdot r_p(kT - nT_c - \tau) \tag{13}$$

Thereby $i(n)$ describes the n-th chip, T the sampling period, T_c the chip duration and $r_p(u)$ is the autocorrelation function of the pulse shape and τ the unknown timing delay. The goal of the Timing Recovery Unit (TRU) is to eliminate τ, i.e., each resulting sample is aligned with the maximum eye opening.

This can be achieved by shifting the asynchronous signal by means of fractional delay interpolation, so that after interpolation the data looks as if it had been sampled at the optimal sampling point. To accomplish this, first the timing error $e(n) = f(\tau)$ is determined in the TED. Then $e(n)$ is fed to the loop filter to determine the corresponding phase and frequency error of local chip clock. Subsequently, the TCU generates a fractional delay Δ from the loop filter output signal. This fractional delay Δ is required to correct the estimated timing offset $\tilde{\tau} = -\tau$ by sample value correction via interpolation in the interpolator. At the same time, the TCU calculates the optimum sampling time in the maximum amplitude of the symbol, i.e., it adjust the local chip clock.

4.3.1. Interpolation Unit

As mentioned earlier, the fraction delay filter is used to compute desired samples of $y(nT_c)$ at the optimum sampling instances from the available sample $x(kT)$. To ensure a linear-phase transmission behavior of the filter, an odd-order polynomial is chosen. However, due to the fact that interpolation with a first degree polynomial leads to large deviations, the next option of a third degree polynomial is used. The resulting algorithm for calculating the desired interpolation value is

$$y(nT_c) = x((k + \Delta)T) = \sum_{l=0}^{p} \Delta^l \sum_{i=-2}^{1} b_l(i) x((\Delta - i)T) \tag{14}$$

where p represents the order of the used interpolation polynomial, Δ the fractional delay of the TCU, and $b_l(i)$ the corresponding filter coefficient, **Table 1**.

These filter coefficients are obtained by determining the polynomial coefficients of the third degree interpolation polynomial

Table 1. Fraction delay filter coefficient.

i	$b_3(i)$	$b_2(i)$	$b_1(i)$	$b_0(i)$
−2	1/6	0	−1/6	0
−1	−1/2	1/2	1	0
0	1/2	−1	−1/2	1
1	−1/6	1/2	−1/3	0

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$$x(k + \Delta) = b_3[(k + \Delta)T]^3 + b_2[(k + \Delta)T]^2 + b_1[(k + \Delta)T] + b_0 \tag{15}$$

as a function of Δ, considering the four given samples, which are arranged in pairs to the left and right of the value to be interpolated, cf. **Figure 8**.

A detailed description of the calculation of the filter coefficient as well as a deeper description of the functionality of the TCU is omitted and reference is made to the corresponding sources.[41,45,44]

4.3.2. Timing Error Detector

Implemented TED use the Gardner algorithm to determine one timing error value $e(n)$ per chip. The algorithm is based on a delay difference between the current sample and another sample of the same symbol delayed by half the symbol period and and requires two samples per chip. To determine the timing error, three consecutive samples are used which are shifted by half a chip to each other. The error signal is finally obtained according to[46]

$$e(n) = \gamma((n - 1/2)T_c) \cdot [\gamma((n - 1)T_c) - \gamma(nT_c)] \tag{16}$$

where $\gamma(nT_c)$ are generally complex values. If the sampling is performed at the optimum time point, two values are located in the chip center and one exactly at the transition between two chips, $e(n) = 0$. If sampling is premature, then $e(n) < 0$, if sampling is delayed, then $e(n) > 0$. The advantage of this algorithm is the insensitivity to a carrier frequency offset, thus no previous carrier synchronization is required.

4.3.3. Timing Control Unit

The TCU provides the interpolator with the fractional interval Δ and the TED with the strobe signal CLK to calculate the correct timing errors once per chip. The interpolation is performed for every sample, and a strobe signal is used to determine if the interpolant is taken as output value. The operation principle of the timing controller is based on the Modulo-1 decrements counter. The counting frequency is determined by the constant $1/N$, where N is the number of samples per chip. The output of the Modulo-1 counter is defined as

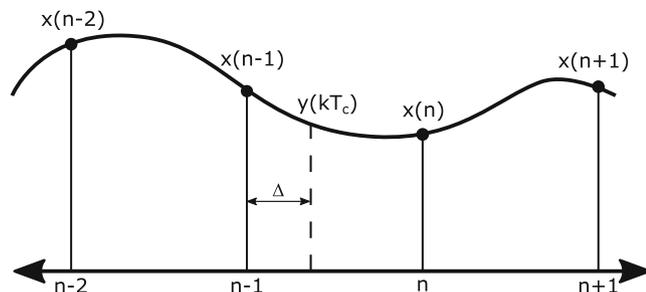$$\Delta(n) = \begin{cases} N \cdot \delta(k) & \text{CLK} = 1 \\ \Delta(n - 1) & \text{else} \end{cases} \tag{17}$$

with

$$\delta(k) = [\delta(k - 1) - M(k - 1)] \bmod 1 \tag{18}$$

and

$$M(k) = 1/N + \nu(n) \tag{19}$$

where $\nu(n)$ corresponds the loop filter output and $\delta(k)$ corresponds each sample calculated Δ. The $\nu(n)$ signal from the loop filter adjusts the amount by which the counter decrements and $\delta(k)$ is only passed to the interpolation filter as Δ if the strobe signal is valid.

4.4. Loop-Filter

For both carrier and clock synchronization, a time discrete PI filter is used to calculate the control variable for the frequency and phase offset. The filter is a first order filter with the following transfer function in the z-domain[47]

$$F(z) = \frac{C_2 + C_1(1 - z^{-1})}{1 - z^{-1}} \tag{20}$$

The gain parameters C_1 and C_2 define the behavior of the closed loop and are calculated as

$$C_0 = \frac{1}{K_0 K_D} \cdot \frac{8\zeta\omega_n T_c}{4 + 4\zeta\omega_n T_c + (\omega_n T_c)^2} \tag{21}$$

$$C_1 = \frac{1}{K_0 K_D} \cdot \frac{4(\omega_n T_c)^2}{4 + 4\zeta\omega_n + (\omega_n T_c)^2} \tag{22}$$

ζ is the loop attenuation coefficient, K_0 the numerically-controlled oscillator (NCO) gain, K_D the error detector gain, T_c the chip interval, and ω_n natural frequency. Values from **Table 2** are used for the carrier synchronization loop respectively timing recovery loop. The NCO Gain K_0 correspond to the gradient of characteristic curve of the respective NCO. The Error Detector Gain K_D can be taken from the respective S-curve of Error Detector.[41]

4.5. Frame Synchronization

After successful carrier synchronization and timing recovery, the next step is to locate a structure in the chip stream within which the valid data is located.

For the reliable detection of a frame start within the chip stream, a 78-chip synchronization word is used, which consists of a 64-chip long code word and a 14-chip long guard interval.

Figure 8. Interpolation principle.

Table 2. Loops parameter.

	Carrier loop	Timing loop
K_0	1	-1
K_D	1	2.55
ζ	0.7071	0.7071
B_n	200 Hz	100 Hz
ω_n	$1.89B_n$	$1.89B_n$
T_c	125 μs	125 μs

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The code words are lines of the Hadamard-Matrix H_8 spread with a SF of 8, which are recursively derived from the formation rule

$$H_{2n} = \begin{pmatrix} H_n & H_n \\ H_n & -H_n \end{pmatrix} \tag{23}$$

with

$$H_1 = 1 \tag{24}$$

The selected codewords $(H_{8,3}, H_{8,5})$ have very good aperiodic autocorrelation properties. This ensures a sufficient distance between the maxima of frame start detection and the side lobes.

The detection of the synchronization pattern is performed by a correlator realized in finite impulse response (FIR) filter structure, which cross-correlates the local version of the synchronization pattern with the incoming baseband symbol stream. The amount of the cross-correlation is then squared. By applying a nonlinear function, the distance between the main maxima and the possible sidelobes is further increased. This enables reliable detection even with a very low signal-to-noise ratio. If the set threshold value is exceeded, a preamble is detected and valid data follows. The data can then be despread and demodulated. The block diagram of the frame synchronization unit is shown in **Figure 9**.
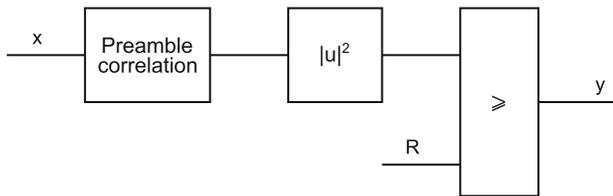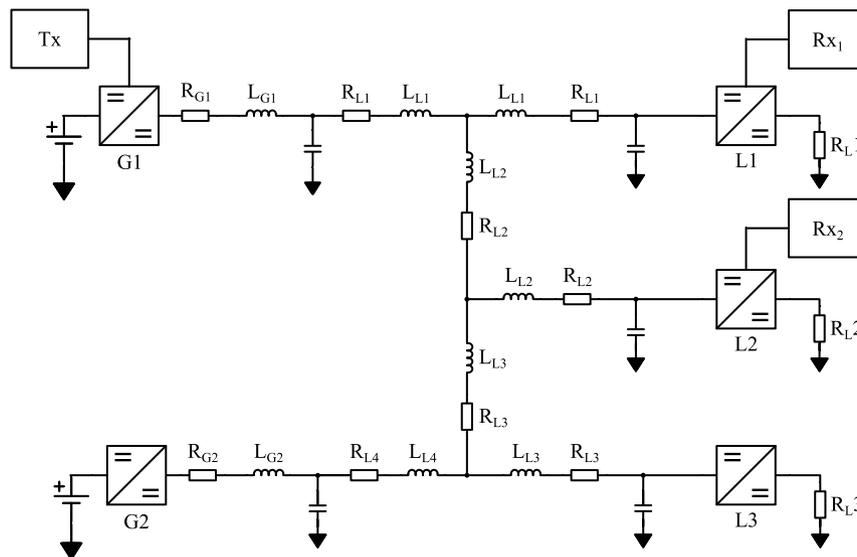

Figure 9. Frame Synchronization Unit.

4.6. Despreading and Demodulation

After synchronizing all three levels, the received data must now be despread and demodulated. After clock synchronization, chip stream to be treated is now available as chip/sample. The code phase position required for successful despreading of the data is also known due to the detection of the start of frames in the frame synchronization. Now the data is fed to a despreading unit in FIR filter structure. This delivers all L (length of code word) chips the despreaded symbol, which is converted into a data bit in the DBPSK demodulation unit. The resulting data bit stream is then stored in a queue register.

5. Simulation Results

Figure 10 shows the structure of the DC grid which was used for the simulative performance analysis of the implemented transmission system. This model is based on the structure for testing the PSDM techniques for packet based energy dispatching from ref. [6]. It is a low voltage DC circuit consisting of two generator converters (G1 and G2) and three consumer converters (L1–L3). The converters on the generator side and on the load side are synchronous DC/DC buck converters.

In contrast to the original model,[6] the DC/DC buck converters are equipped with the transmission system developed in the present article. The example shows that the information exchange between generator and load, which is necessary for the exchange of EPs, does not require a third-party synchronization unit. Furthermore, all parameters required for successful information and energy exchange can be derived from the received signal itself. For this purpose, the relationship between the exchange of information to trigger the energy transport and the subsequent transport of the EPs is first shown in an overview manner. This is followed by a detailed presentation of the results of the implemented synchronization levels, the major contribution of this article. For the sake of readability, the following simplifications are

Figure 10. Simulated DC grid for testing the transmission system.

made: 1) The communication occurs unidi-rectional from source to sink. In general, all loads or generators that utilize converters as interfaces to the bus can be equipped with Tx/Rx-Unit for bidirectional communication. Multiple access to the same communication channel can be realized either by code division multiplexing (CDM) or time division multiplex-ing (TDM); 2) The energy transfer phase is selected extra short in the figures to be able to recognize the activities in the process of information transfer. In reality, the phase of energy transfer would be much longer than in the simulation, if only for reasons of efficiency; 3) To analyze the quality of the transmission, the duration of the information phase is extra long. In fact, it is adjustable to the requirements. It depends on the following factors: Information word length k (i.e., how many symbols should to be transmitted in one frame), the type of modulation used, the desired transmission rate R, and the spreading factor SF; 4) The load L3 is connected to the DC bus via an conventional DC/DC converter. At the beginning, the load is off and is turned on manually at $t = 125$ ms.

Figure 11a shows the output signal of the generator (G1). It supplies the DC bus with 15 V DC voltage. In the information transfer phase, the information signal is modulated by the PSDM to the DC voltage. As a result, the existing residual ripple of the DC voltage no longer represents only the unwanted noise; it is used constructively for information transmission. The messages sent by G1 for testing are coded alternately with the unique sequence S1 for load L1 and S2 for load L2. This signal is available as a broadcast signal to all devices connected to the bus. Only if the participants actively listen to it and also if have the correct encryption code, they can decrypt and handle the information.

At the beginning of this simulation example $t = 0$ s, the loads are operated in listening mode and high input impedance ($I_{L1} = I_{L2} = I_{L3} = 0$ A), cf. Figure 11d,g,h. The two correlation peaks in Figure 11b with an excursion above the threshold of 0.8 show that L1 detects at time $t = 35$ and $t = 185$ ms valid data addressed to him within the receiveddata stream. After the synchronization, decoding and demodulation processes described in Section 4 have been performed, the receiver signals the presence of valid data by setting the signal "Valid data avaible" to high Figure 11c and passes the data to the control unit of load L1 for further processing. After elimination of the metadata by receiver, the data contains the control information regarding the amount of load current required and how long this should be present. This data is interpreted in the control unit and then the current flow enable signal is activated for the required time Figure 11c and the required current level is set for 35 ms. A similar process occurs at time $t = 110$ ms for load L2; see Figure 11e–g. The resulting total current is shown in subplot (i) of Figure 11. In the following, the results of the realized synchronization level are presented. These enable the asynchronous transmission of EPs via PSDM and derivation of metadata from the received data.

To test the AGC of the implemented receiver, the information part (i.e., high-frequency part) of the broadcast signal undergoes time-variable random amplification ($G = 0.5$–1.25). The change period is 175ms. **Figure 12** summarizes the simulation results of the AGC tests. Subplot (a) shows the received signal in the passband, which varies randomly every 175 ms. In subplot (b),
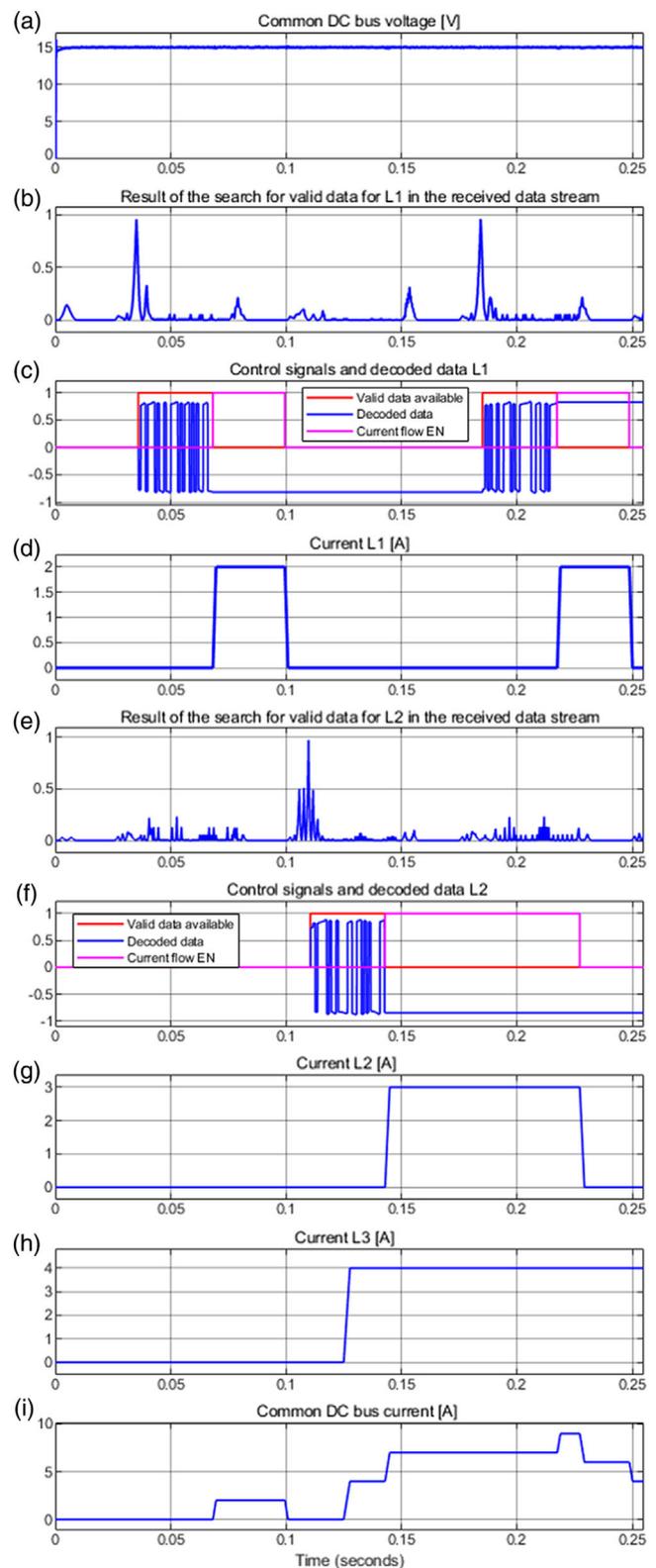

Figure 11. Simulation results. a) Common DC bus voltage [V]. b) Result of the search for valid data for L1 in the received data stream. c) Control signals and decoded data L1. d) Currrent L1 [A]. e) Result of the search for valid data for L2 in the received data stream. f) Control signals and decoded data L2. g) Current L2 [A], h) Current L3 [A]. i) Common DC bus current [A].
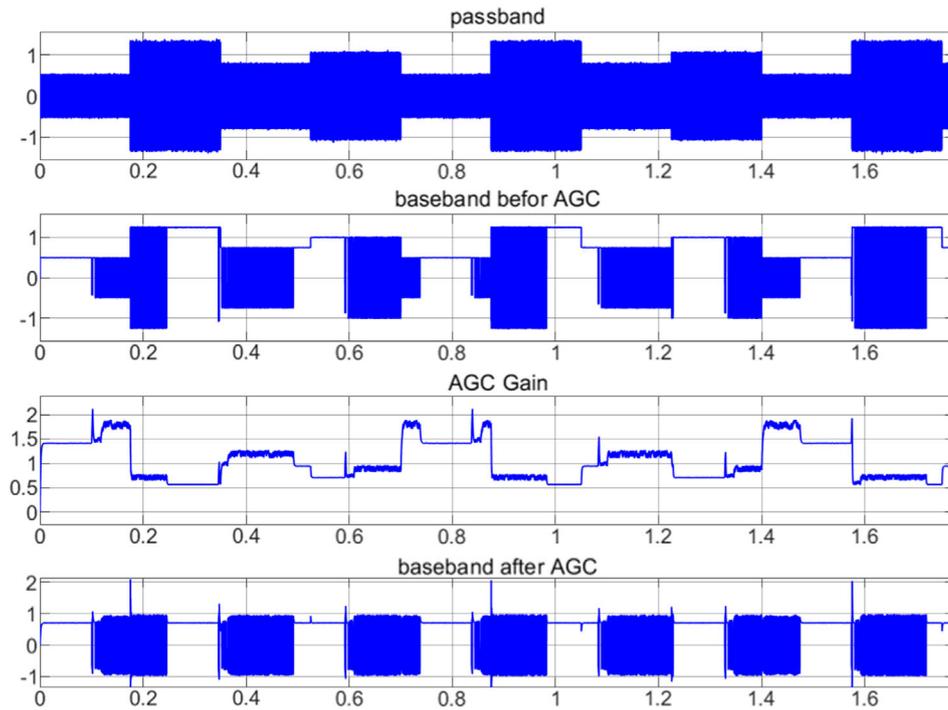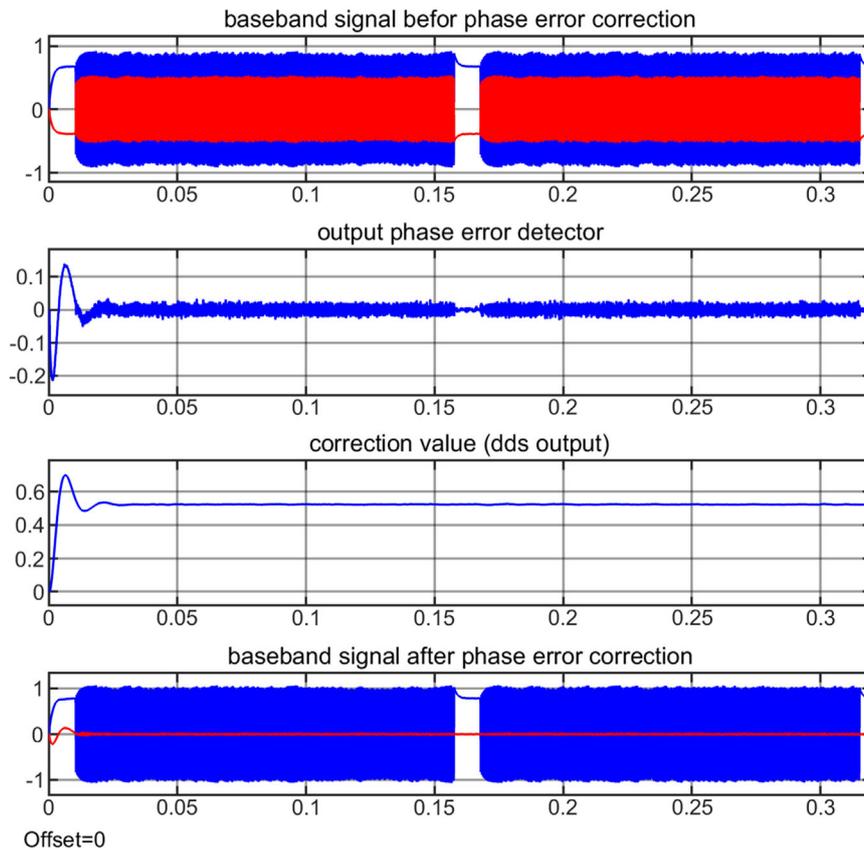
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Figure 12. Results AGC test.

Figure 13. Results carrier synchronization for phase offset.

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the corresponding baseband signal before the AGC is shown, which changes in the same way. In subplot (c), the gain factor is shown which is applied to keep the output signal constant according to the reference. Finally, the subplot (d) shows the nearly constant baseband signal after the AGC.

Next, the results of the phase and frequency offset correction are presented using the carrier synchronization unit. **Figure 13** shows the correction process of a phase offset between the carrier wave and the phase of the local oscillator of $\frac{\pi}{6}$. Subplot (a) shows the asynchronously downconverted baseband signal. Due to the phase shift, part of the signal power is transferred to the imaginary part (red). Subplot (b) shows the output of the PED. Subplot (c) shows the resulting correction value $\tilde{\phi}$ and subplot (d) the baseband signal after phase offset correction.

The carrier synchronization results at a frequency offset are shown in **Figure 14**. The frequency offset that is used is $\Delta f = 5\,\text{Hz}$.

The results of Chip Clock Recovery (CCR) are summarized below. The sampling frequency offset of $\Delta f = 2\,\text{Hz}$ is used to test the TRU. Subplot (a) of **Figure 15** shows the baseband signal of the received signal $r(t)$ sampled without the local clock recovery. As one can see, plot (a) contains samples that should not be present in a DBPSK signal. These result from an asynchronous sampling. In the subplot (b), the same signal is shown but after the CCR. The constellation diagrams, **Figure 16**, further clarify the asynchronicity between the received data and the local clock as well as the result of the synchronization by the CRU. **Figure 17**

shows the corresponding estimated timing error and the resulting fractional delay for timing error correction.

Finally, as described in Section 4, the frame synchronization, the despreading of the chips to the DBPSK symbols, and finally the demodulation of the data is performed. The results of these operations for two received data frames is shown in **Figure 18**. Subplot (a) shows the received chipstream. The result of the cross correlation for the preamble detection is shown in the subplot (b). Subplot (c) shows the valid-frame-detected signal and subplot (d) shows the corresponding DBPSK symbols.

In contrast, **Figure 19** shows the same procedure but for the second load. As this load expects data coded with L2 unique sequence, no valid message is detected, which can be seen from the result of the cross correlation.

A series of ten information frames are sent to check the overall functionality of the implemented receiver. The received binary data are then cross-correlated with the transmitted data. The result of the cross-correlation is shown in **Figure 20**. A complete match of the transmitted and the received data can be recognized by the unique peak at $\tau = 0$.

6. Conclusion and Outlook

The present article extends previous contributions[5,6] regarding packet-based energy transmission by describing a practicable design of an EP receiver which recovers the required
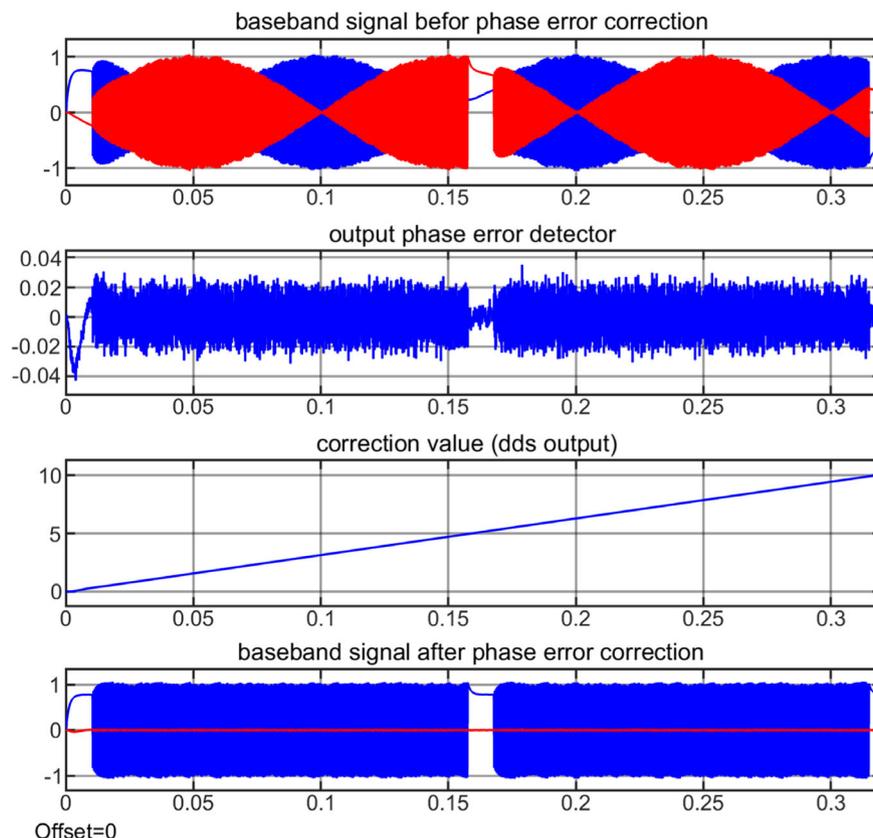

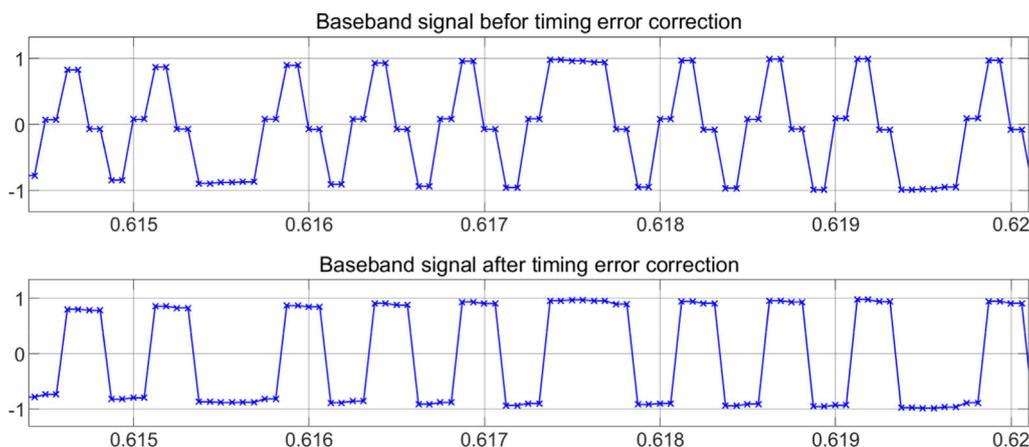**Figure 14.** Results carrier synchronization for frequency offset.

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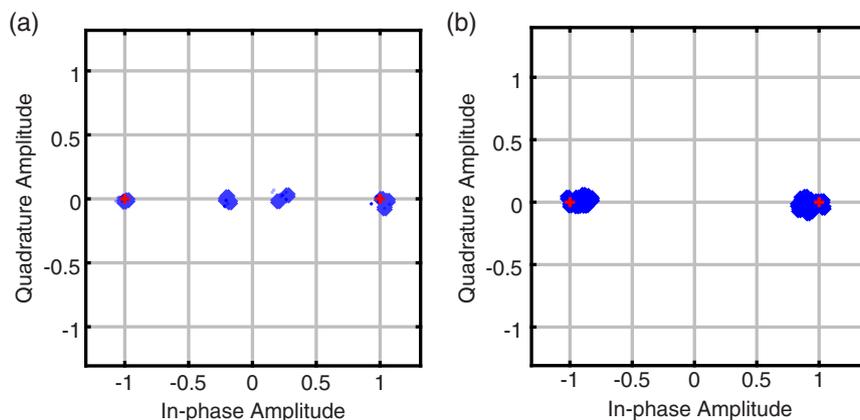**Figure 15.** Baseband signal before and after timming recovery.

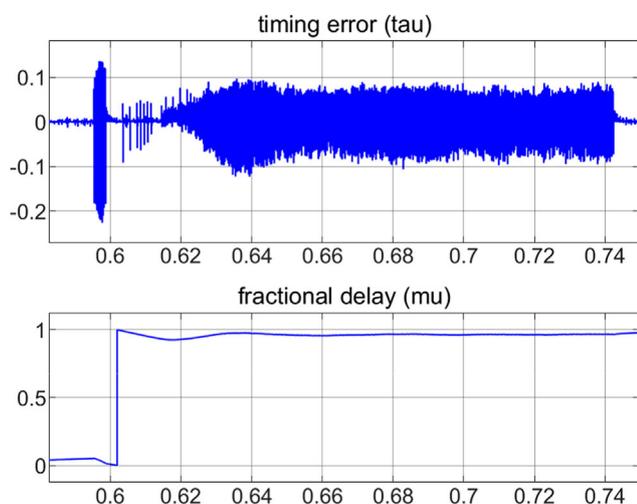**Figure 16.** Received signal constellation diagram. a) Before and b) after clock recovery.

Figure 17. Estimated timing error and the resulting fractional delay.

synchronicity information directly from the received signal itself. The main focus is on the reception and lossless preprocessing and interpretation of the metadata of the information part of the EP. For this purpose, implemented solutions for the respective synchronization levels 1) Carrier Recovery, 2) Clock Recovery, and 3) Frame Recovery are discussed in detail. Drawing upon a DC grid example, simulation results show the performance and applicability of the proposed novel receiver for packet-based energy dispatching. In addition, the simulation results show further beneficial effects of using the PSDM for the unique tagging of EPs. Using PSDM, the information part of the EPs is transmitted in a passband. As a consequence, the output voltage of the power converter looks as regular DC/DC output signal, but it is superimposed with the information signal. The transmission signal is available as a broadcast signal to all devices connected to the bus, whereby only if the participants actively listen to it and also have the correct encryption code, they can decrypt and handle the information.

As shown in the article, the realization of a suitable receiver is more complicated than for the concepts where the meta information required for distribution is achieved by binary ASK of the supply voltage in the baseband as a binary line code. However, the new method introduced in the present article
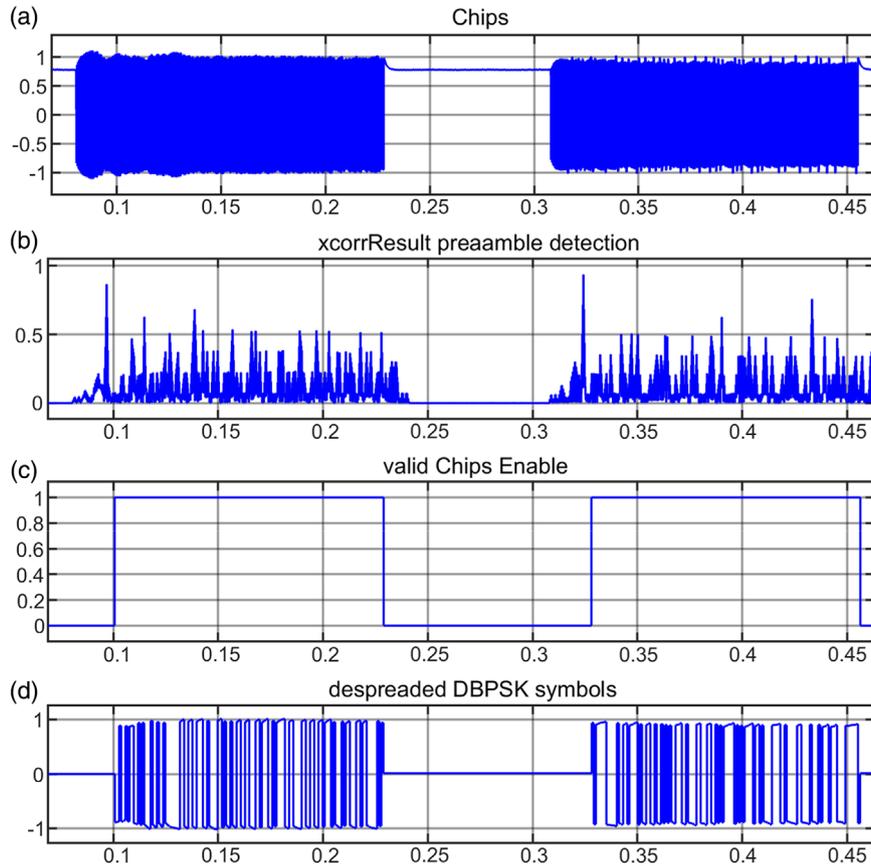
Figure 18. Result frame synchronization load 1. a) Chips. b) xcorrResult preaamble detection. c) Valid chips enable. d) Despreaded DBPSK symbols.
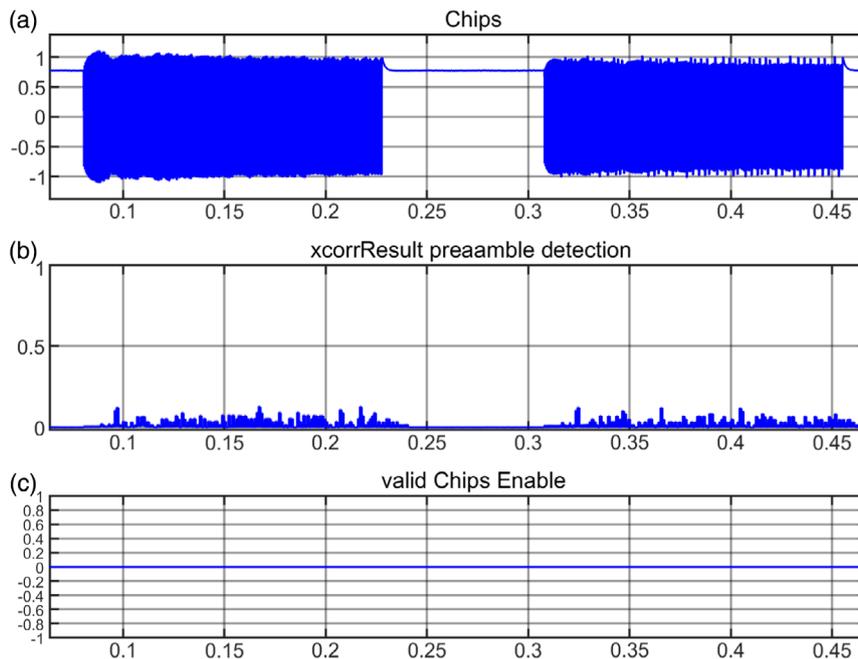

Figure 19. Result frame synchronization load 2. a) Chips. b) xcorrResult preaamble detection. c) Valid chips enable.
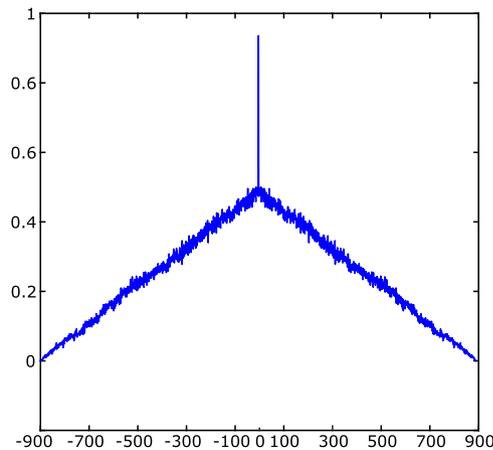
Figure 20. Result of the cross-correlation between sent and received data.

yields several advantages: 1) No additional interference is produced, as the existing ripple of the DC voltage is used constructively for the information transmission; 2) The concept can be used for DC/DC as well as DC/AC or even AC/DC/AC converters; 3) Existing both AC and DC networks can be extended with subscribers with the possibility of packet-based energy transmission.

As future work, the proposed approach of packet-based energy distribution will be implemented and validated within the KIT Energy Lab 2.0 infrastructure.[48]

Conflict of Interest

The authors declare no conflict of interest.

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