# Optimizing Utilization of an MMSPC with Model Predictive Control

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***Abstract*—While the numerous degrees of freedom of a Modular Multilevel Series Parallel Converter (MMSPC) for automotive applications can be used for active balancing of the distributed batteries' energy and to reduce total converter losses, it is a challenge to determine the optimal next states.**

**In this contribution, we present the implementation of a real-time model predictive control (MPC) algorithm for an automotive MMSPC that is able to optimize the switching states in each control cycle ($12.5\,\mu s$). The focus of the presented algorithm is the optimal control of the internal states of the MMSPC itself, without taking the control loops of the motor speed and torque into account. In addition to the capability of balancing all batteries within and between the phases simultaneously, the algorithm uses the common-mode (CM) voltage of the converter to reduce both the battery and the semiconductor losses. The control scheme is implemented on a field-programmable gate array (FPGA) and validated on a machine test bench.**

***Index Terms*—Multilevel Converters, Current Ripple, Automotive, Model Predictive Control, Real-Time, Active Balancing**

## I. Introduction

State-of-the-art two-level converters generate a three phase alternating current (AC) for the motors of electric vehicles (EV) from direct current (DC)-link voltages of $400\,\mathrm{V}$ to $800\,\mathrm{V}$. The energy source, which usually is either a battery or a fuel-cell, provides a DC voltage. To improve the low output voltage quality of two-level converters, multilevel converters have been investigated for automotive applications [1]–[3]. The increased output voltage quality of multilevel converters reduces magnetic losses, dielectric stress and the maximum $\frac{\mathrm{d}V}{\mathrm{d}t}$.

However, a significant drawback of multilevel converters, especially modular multilevel converters, is the increased effort to control the internal converter states [4]. Therefore the converter itself and its internal states have to be taken into account while pursuing the overall goal of the motor control.

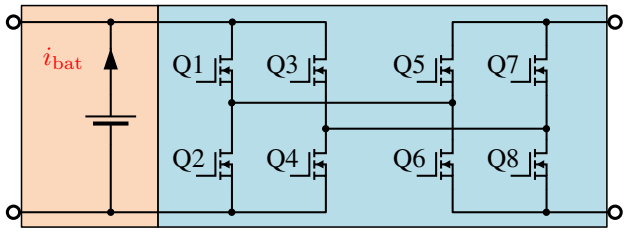
In [5] a new modular multilevel converter topology was introduced. The special characteristic of the modular multilevel series parallel converter (MMSPC) is, that a battery energy storage is integrated into each submodule (SM) directly. Additionally and in contrast to common multilevel converters, each SM can be switched to both a series and a parallel state. This ability leads to an additional degree of freedom to balance the distributed batteries' state of charge (SoC) as well as the opportunity to reduce conduction losses in the converter by reducing the overall resistance.

A main challenge in the operation of the MMSPC is to find the optimal state transitions, because of the large solution space. Some different approaches for controlling an MMSPC [6]–[8] or single converter arms of the same topology [9], [10] are presented in literature already. In [7] the control scheme reduces the batteries' root mean square (rms) currents by injecting a 3rd harmonic of the controller's output voltage in order to switch more modules in parallel while the current is high to reduce ohmic losses. In [6] only the conduction losses in the batteries are taken into account to determine the next state while the conduction and the switching losses of the transistors are neglected. In [9]–[12] different scheduling methods for one arm of an MMSPC are described.

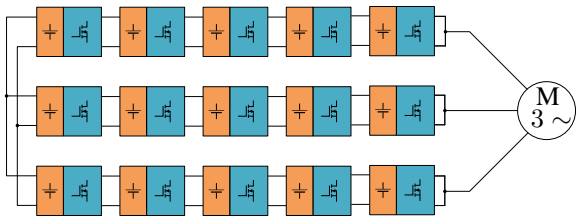
In this paper, a new model predictive control (MPC) algorithm that optimizes the switching state of the entire MMSPC in real-time is described. In dependence of the weighting factors, the objective function of the algorithm balances the SMs' SoCs and increases the efficiency of the converter, taking all significant losses into account. Furthermore, the control scheme can freely use the degree of freedom of the common-mode (CM) voltage to optimize the converter output. In the examined system the motor speed and the motor torque are controlled by PI-controllers which work independently from the MPC of the MMSPC.

## II. Topology

We use the MMSPC with asymmetric SMs, shown in Fig. 1a. Each of the three phases of the MMSPC consists of $n_{\mathrm{ph}}$ SMs, which are linked as shown in Fig. 1b. Due to the usage of the asymmetric SM, the three modules and the batteries at the converter's neutral point (on the left-hand side of Fig. 1b) are connected in parallel. Each SM has six active states: series-positive, series-negative, bypass-top, bypass-bottom and two parallel states. The last module has only two different states, because its output ports are shorted which prohibits the parallel states. The remaining two different active states are series-positive and series-negative. As a result, the total number of different switching states of one phase $N_{\mathrm{pos,ph}}$ is $2 \cdot 6^{n_{\mathrm{ph}}-1}$. If there are five modules per phase the total number of different switching states of the whole MMSPC is $(2 \cdot 6^{5-1})^3 > 10^{10}$. For further reading, a more detailed analysis of the switching states is presented in [5] and [6].




(a) Microtopology




(b) Macrotopology

Fig. 1: MMSPC Topology

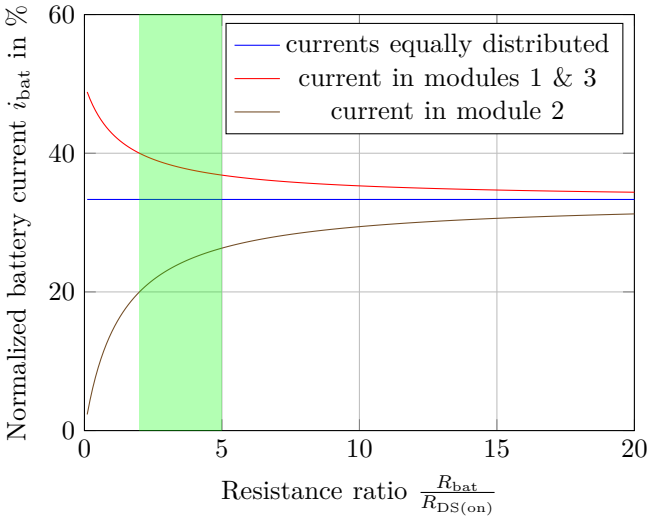



Fig. 2: Current distribution within three parallel SMs

The main advantage of the MMSPC topology is that SMs which are not switched to either series state in order to generate the required output voltage, can be switched parallel to its neighboring module. This leads to two opportunities. First, the total losses of the modules can be reduced, since the phase currents can be distributed between parallel modules and batteries. Second, the possibility of switching parallel can be used to actively balance the batteries' SoCs.

Standard sorting algorithms for a Modular Multilevel Converter (MMC) – as described in [13] – sort the SMs in descending order according to their capacitors' voltages. They switch the semiconductors to discharge capacitors with higher voltages and to charge capacitors with lower voltages. These algorithms do not take the additional degree of freedom of parallelization into account, therefore the utilization of the converter is not at its limit and the MMSPC would not have any advantages. As a consequence, new algorithms to make use of all degrees of freedoms of an MMSPC have to be developed.

## III. Analysis

In this section, we present the circuit analysis of the MMSPC, on which the new control scheme is based. The analysis of the converter is divided into three sections, the calculation of the battery current distribution (Section III-A), the converter's internal resistance (Section III-B) and the estimation of the switching losses of the transistors (Section III-C).

### A. Battery current distribution

In contrast to common approaches (e.g. [6]), the approach presented in this paper does not expect the battery currents to be equally distributed within parallel modules. This is because the metal-oxide-semiconductor field-effect transistors (MOSFET) have a resistance that is not negligible in comparison to the resistance of the batteries. Taking this into account, the currents in the batteries depend not only on the number of parallel modules, but also on the position of the module in the parallel group. Furthermore, if the module is connected to the neutral point the resulting current distribution depends on the switching states of the other phases.

As an example, Fig. 2 shows the current distribution in three parallel modules with equal battery voltages within a phase. The green rectangle shows the area of expected ratios between the battery resistance $R_{\mathrm{bat}}$ and the $R_{\mathrm{DS(on)}}$ of the transistors in the examined system.

For analysis of the MMSPC, each MOSFET is modeled as either an open-circuit, if it is blocking, or as a resistance with $R_{\mathrm{DS(on)}}$, if it is conducting. The battery is modeled as a voltage source with the open circuit voltage $U_{\mathrm{bat},}$ and a series resistance $R_{\mathrm{bat}}$.

The mathematical model of the converter is derived by analyzing the feasible switching states within a phase, and separately, across the phases. This leads to battery current distribution matrices $\boldsymbol{A}_{\mathrm{bat,ph}}$ and $\boldsymbol{A}_{\mathrm{bat,np}}$, shown in (4) and (9), which are calculated and simplified offline. They are used to calculate each battery current in dependence of the battery voltages, the phase currents and each possible next switching state, in real-time.

An example of one possibility, based on the parallel group of three SMs within a phase, is shown in Fig. 3:

In general, if there are $n_{\mathrm{par}}$ modules in a parallel group, $n_{\mathrm{par}} - 1$ different equations according to (1) are needed to describe the battery currents. The variables $U_{\mathrm{bat},k}$ and $i_{\mathrm{bat},k}$ are the voltage and current, respectively, of the battery in module $k$. The last equation, describing sum of all battery currents in the parallel group, is set up according to the state combination of the first and the last module in the parallel group, according to (2). This sum $\sigma_{\mathrm{I}}$ is either the positive phase current $i_{\mathrm{ph}}$, the negative phase current $i_{\mathrm{ph}}$ or it adds up to no current. The four cases of the switching states of the first and the last module which have to be differentiated, are:

(a) The first and the last module are both in series-positive
(b) The first and the last module are both in series-negative

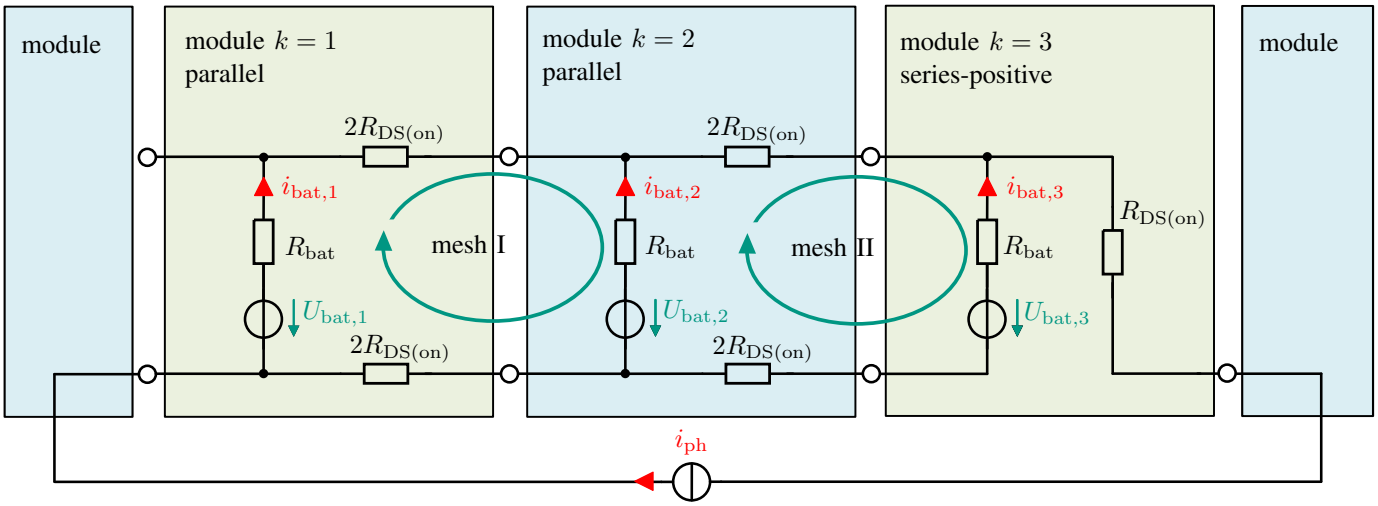



Fig. 3: Parallel group within a phase consisting of three modules with series-positive interconnection

(c) The first module is in series-positive and the last module in series-negative
(d) The first module is in series-negative and the last module in series-positive

Here, in the example of Fig. 3, it is case (a).

$$0 = -U_{\mathrm{bat},k} + R_{\mathrm{bat}} i_{\mathrm{bat},k} + 2R_{\mathrm{DS(on)}} \sum_{c=1}^{k} i_{\mathrm{bat},c} - R_{\mathrm{bat}} i_{\mathrm{bat},k+1} + U_{\mathrm{bat},k+1} - 2R_{\mathrm{DS(on)}} (i_{\mathrm{ph}} - \sum_{c=1}^{k} i_{\mathrm{bat},c}) \tag{1}$$

$$\sigma_{\mathrm{I}} = \sum_{c=1}^{n_{\mathrm{par}}} i_{\mathrm{bat},c} = \begin{cases} i_{\mathrm{ph}}, & \text{case a)} \\ -i_{\mathrm{ph}}, & \text{case b)} \\ 0\,\mathrm{A}, & \text{case c) or d)} \end{cases} \tag{2}$$

Combining (1) and (2) to a linear system of equations and solving it, leads to an equation to estimate the battery currents $i_{\mathrm{bat},k}$ of each module $k$ during operation within a phase. This approach is also used to estimate the battery currents in the neutral point SMs of the MMSPC.

In the following, the general equation to calculate all module currents within a phase is shown.

The vector $\underline{i}_{\mathrm{bat,ph}}$ contains the estimated battery currents within a parallel group in a phase and it has the dimension $(n_{\mathrm{par}} + 1) \times 1$.

$$\underline{i}_{\mathrm{bat,ph}} = \begin{pmatrix} i_{\mathrm{bat},1} & i_{\mathrm{bat},2} & \cdots & i_{\mathrm{bat},n_{\mathrm{par}}} \end{pmatrix}^{\mathsf{T}} \tag{3}$$

Matrix $\boldsymbol{A}_{\mathrm{bat,ph}}$ consists of constants and the values of the resistors of the system. Its dimension is $(n_{\mathrm{par}} + 1) \times (n_{\mathrm{par}} + 1)$ and it is calculated offline.

$$\boldsymbol{A}_{\mathrm{bat,ph}} = \begin{pmatrix} R_{\mathrm{bat}} & -R_{\sum} & -4R_{\mathrm{DS(on)}} & \cdots & -4R_{\mathrm{DS(on)}} \\ 0 & R_{\mathrm{bat}} & -R_{\sum} & \ddots & -4R_{\mathrm{DS(on)}} \\ \vdots & \ddots & \ddots & \ddots & \ddots \\ 0 & \ddots & \ddots & R_{\mathrm{bat}} & -R_{\sum} \\ 1 & \cdots & \cdots & \cdots & 1 \end{pmatrix} \tag{4}$$

where $R_{\sum} = R_{\mathrm{bat}} + 4R_{\mathrm{DS(on)}}$.

In vector $\underline{B}_{\mathrm{bat,ph}}$, the state values of the system during run-time, such as battery voltages and the phase current are contained. Its dimension is $(n_{\mathrm{par}} + 1) \times 1$.

$$\underline{B}_{\mathrm{bat,ph}} = \begin{pmatrix} U_{\mathrm{bat},1} - U_{\mathrm{bat},2} + 2\alpha R_{\mathrm{DS(on)}} i_{\mathrm{ph}} \\ U_{\mathrm{bat},2} - U_{\mathrm{bat},3} + 2\alpha R_{\mathrm{DS(on)}} i_{\mathrm{ph}} \\ \vdots \\ U_{\mathrm{bat},n_{\mathrm{par}}-1} - U_{\mathrm{bat},n_{\mathrm{par}}} + 2\alpha R_{\mathrm{DS(on)}} i_{\mathrm{ph}} \\ \sigma_{\mathrm{I}} \end{pmatrix} \tag{5}$$

$\alpha$ is a factor to define the direction of circulating currents within a parallel group and it is defined in dependence of the state of the last module in the group as follows:

$$\alpha = \begin{cases} +1, & \text{last module is in series-negative} \\ -1, & \text{last module is in series-positive.} \end{cases} \tag{6}$$

Equation (7) shows the calculation performed for each possible parallel group during each switching cycle to estimate the current distribution in the batteries.

$$\underline{i}_{\mathrm{bat,ph}} = \boldsymbol{A}_{\mathrm{bat,ph}}^{-1} \underline{B}_{\mathrm{bat,ph}} \tag{7}$$

The matrices used to calculate the currents in the neutral point are larger, because one has to distinguish between more cases. Vector $\underline{i}_{\mathrm{bat,np}}$ is the result which consists of the estimated battery currents in the neutral point modules according to the predicted switching state. Its dimension is $(n_{\mathrm{par,np,U}} + n_{\mathrm{par,np,V}} + n_{\mathrm{par,np,W}} + 3) \times 1$.

$$\underline{i}_{\mathrm{bat,np}} = \begin{pmatrix} i_{\mathrm{bat,U},1} \\ \vdots \\ i_{\mathrm{bat,U},n_{\mathrm{par,np,U}}} \\ i_{\mathrm{bat,V},1} \\ \vdots \\ i_{\mathrm{bat,V},n_{\mathrm{par,np,V}}} \\ i_{\mathrm{bat,W},1} \\ \vdots \\ i_{\mathrm{bat,W},n_{\mathrm{par,np,W}}} \end{pmatrix} \tag{8}$$

The matrix $\boldsymbol{A}_{\mathrm{bat,np}}$ consists of seven separate sub-matrices, which are explained in the following. Its total dimension is $(n_{\mathrm{par,np,U}} + n_{\mathrm{par,np,V}} + n_{\mathrm{par,np,W}} + 3) \times (n_{\mathrm{par,np,U}} + n_{\mathrm{par,np,V}} + n_{\mathrm{par,np,W}} + 3)$.

$$\boldsymbol{A}_{\mathrm{bat,np}} = \begin{pmatrix} \boldsymbol{A}_{\mathrm{bat,U,np}} & \underline{0} & \underline{0} \\ \underline{0} & \boldsymbol{A}_{\mathrm{bat,V,np}} & \underline{0} \\ \underline{0} & \underline{0} & \boldsymbol{A}_{\mathrm{bat,W,np}} \\ \underline{R}_{\mathrm{bat,U}} & -\underline{R}_{\mathrm{bat,V}} & \underline{0} \\ \underline{R}_{\mathrm{bat,U}} & \underline{0} & -\underline{R}_{\mathrm{bat,W}} \\ \underline{1}_{\mathrm{U}} & \underline{1}_{\mathrm{V}} & \underline{1}_{\mathrm{W}} \end{pmatrix} \tag{9}$$

In order to write the matrices more compactly, $X$ is used as a variable for U, V and W. The three sub-matrices $\boldsymbol{A}_{\mathrm{bat},X,\mathrm{np}}$ are created as follows:

- they are $n_{\mathrm{par,np},X} \times (n_{\mathrm{par,np},X} + 1)$ matrices
- all elements $a_{i,i}$ with $i \in 1 \dots n_{\mathrm{par,np},X}$ are $a_{i,i} = R_{\mathrm{bat}}$
- all elements $a_{i,j}$ with $j > i$ and $i, j \in 1 \dots n_{\mathrm{par,np},X}$ are $a_{i,j} = -R_{\mathrm{bat}} - 4R_{\mathrm{DS(on)}}$

The variable $n_{\mathrm{par,np},X}$ is the amount of parallel modules connected to the neutral point of the converter in phase $X$. The three sub-matrices $\underline{R}_{\mathrm{bat},X}$ are created as follows:

- they are $(n_{\mathrm{par,np},X} + 1) \times 1$ vectors
- the first element of the vector $r_1 = R_{\mathrm{bat}}$
- all other elements are zeros

The three sub-matrices $\underline{1}_X$ are created as follows:

- they are $1 \times (n_{\mathrm{par,np},X} + 1)$ vectors
- all elements are ones

All other elements of matrix $\boldsymbol{A}_{\mathrm{bat,np}}$ are zeros.

The vector $\underline{B}_{\mathrm{bat,np}}$, as defined in (10), contains the variables and the system states of the neutral point of the system which depend on the current situation (phase currents, battery voltages and switching state) of the MMSPC.

$$\underline{B}_{\mathrm{bat,np}} = \begin{pmatrix} U_{\mathrm{bat,U},1} - U_{\mathrm{bat,U},2} + 2\gamma_{\mathrm{U}} R_{\mathrm{DS(on)}} i_{\mathrm{ph,U}} \\ \vdots \\ U_{\mathrm{bat,U},n_{\mathrm{par,np,U}}-1} - U_{\mathrm{bat,U},n_{\mathrm{par,np,U}}} + 2\gamma_{\mathrm{U}} R_{\mathrm{DS(on)}} i_{\mathrm{ph,U}} \\ U_{\mathrm{bat,V},1} - U_{\mathrm{bat,V},2} + 2\gamma_{\mathrm{V}} R_{\mathrm{DS(on)}} i_{\mathrm{ph,V}} \\ \vdots \\ U_{\mathrm{bat,V},n_{\mathrm{par,np,V}}-1} - U_{\mathrm{bat,V},n_{\mathrm{par,np,V}}} + 2\gamma_{\mathrm{V}} R_{\mathrm{DS(on)}} i_{\mathrm{ph,V}} \\ U_{\mathrm{bat,W},1} - U_{\mathrm{bat,W},2} + 2\gamma_{\mathrm{W}} R_{\mathrm{DS(on)}} i_{\mathrm{ph,W}} \\ \vdots \\ U_{\mathrm{bat,W},n_{\mathrm{par,np,W}}-1} - U_{\mathrm{bat,W},n_{\mathrm{par,np,W}}} + 2\gamma_{\mathrm{W}} R_{\mathrm{DS(on)}} i_{\mathrm{ph,W}} \\ U_{\mathrm{bat,U},1} - U_{\mathrm{bat,V},1} \\ U_{\mathrm{bat,U},1} - U_{\mathrm{bat,W},1} \\ I_{\mathrm{sig}} \end{pmatrix} \tag{10}$$

The factor $\gamma_{\mathrm{X}}$ is used to generalize the equation and is defined as:

$$\gamma_{\mathrm{X}} = \begin{cases} +1, & \text{last module in } X \text{ is in series-negative} \\ -1, & \text{last module in } X \text{ is in series-positive.} \end{cases} \tag{11}$$

The significant phase current $I_{\mathrm{sig}}$, which is necessary to define the sum of all battery currents in the neutral point, is calculated according to (13). The factor $\beta_{\mathrm{X}}$ is defined as described in (12).

$$\beta_{\mathrm{X}} = \begin{cases} 0, & \text{last module in } X \text{ is series-negative} \\ 1, & \text{last module in } X \text{ is series-positive.} \end{cases} \tag{12}$$

$$\begin{aligned} I_{\mathrm{sig}} &= \beta_{\mathrm{U}} i_{\mathrm{ph,U}} + \beta_{\mathrm{V}} i_{\mathrm{ph,V}} + \beta_{\mathrm{W}} i_{\mathrm{ph,W}} \\ &= \sum_{c=1}^{n_{\mathrm{par,np,U}}} i_{\mathrm{bat,U},c} + \sum_{c=1}^{n_{\mathrm{par,np,V}}} i_{\mathrm{bat,V},c} + \sum_{c=1}^{n_{\mathrm{par,np,W}}} i_{\mathrm{bat,W},c} \end{aligned} \tag{13}$$

Analogous to (7), (14) has to be solved for each possible parallel group combination in the neutral point during each switching cycle to estimate the current distribution.

$$\underline{i}_{\mathrm{bat,np}} = \boldsymbol{A}_{\mathrm{bat,np}}^{-1} \underline{B}_{\mathrm{bat,np}} \tag{14}$$

### *B. Internal resistance*

The converter's internal resistance and therefore the converter's conduction losses $P_{\mathrm{cond}}$ can be calculated directly by using basic transformations according to Thévenin's theorem. In dependence of all valid switching states and combinations of the SMs, a resulting total internal resistance for each phase is calculated offline. Since there are symmetries in the MMSPC for each phase, they can be used to reduce memory required for data storage. A lookup table (LUT) in the field-programmable gate array (FPGA) stores the phase resistances $R_{\mathrm{ph},X}$ of each switching state.

The total conductive losses during operation are estimated according to (15). As simplification, the batteries are assumed to be balanced and therefore internal circulating currents are neglected.

$$P_{\mathrm{cond}} = R_{\mathrm{ph,U}} i_{\mathrm{ph,U}}^2 + R_{\mathrm{ph,V}} i_{\mathrm{ph,V}}^2 + R_{\mathrm{ph,W}} i_{\mathrm{ph,W}}^2 \quad (15)$$

### C. Switching losses

The switching losses $P_{\mathrm{sw}}$ are estimated according to the characteristics in the datasheet [14]. In dependence of the switching transition of a module, either eight transistors change their conduction state, when switching from series-positive to series-negative or vice versa, or only four during every other transition. Consequently, the switching losses within one module have to be scaled with both the phase current $i_{\mathrm{ph}}$ and the number of transistor transitions between the states. The voltage switched by one transistor is defined as the nominal battery voltage $U_{\mathrm{bat,nom}}$.

## IV. Control scheme

Based on the presented analysis, an MPC optimizes the output of the converter based on the possible switching states in two complementary ways. During operation, the motor current controller calculates and a subsequent delta-sigma modulator (DSM) [5] discretizes the demanded output levels of each phase of the converter, which serve as the input to the presented MPC.

As the motor's phases are connected in delta configuration and therefore no neutral point is existent, a zero-voltage component can be added by the MPC without affecting the current control. Starting from the current switching state and the difference of the DSM outputs of the last and the new control cycle, the control scheme additionally adds five different discrete zero-voltage levels (-2, -1, 0, 1, 2) to the calculated outputs of the three phases. As a result, up to five different feasible combinations of the three outputs are possible to fulfill the demanded phase-to-phase voltage.

Furthermore, each phase of the MMSPC has various options to realize a specific output level [6]. As mentioned before, the MMSPC has more than $10^{10}$ different feasible switching states. For obvious reasons it is not practicable to check every possibility to find the optimal state transition for the next control cycle. Some of the possibilities have lower probability to be useful than other states. Therefore some restrictions have to be implemented to be able to find a solution which is more likely to be better than most of the other possibilities in real-time. To limit the number of possible subsequent switching states, a pre-selected solution space is determined. Only serial states of the same polarity and no bypass-states within a phase are used, and a maximum of three modules within a phase are allowed to change their states. As a result of these limitations, the maximum voltage step at the output of each phase is limited, too. Furthermore, it is assumed that the differences in $U_{\mathrm{bat},}$ are small, i.e. the batteries are identical and balanced. This is valid because balancing of the batteries is one of the objectives of the used MPC. It has to be mentioned that due to simplifications throughout the design process of the MPC, it might be possible that the true optimal switching state is not considered in the calculation for the next switching state.

The main loss mechanisms of an MMSPC are the conductive losses due to the battery and transistor resistances as shown in Section III-B, and the switching losses $P_{\mathrm{sw}}(s_0, s_1, i_{\mathrm{ph}})$ of the semiconductors [7], as described in Section III-C. The total losses $J_{\mathrm{losses}}$ depend on the present switching state of the modules $s_0$, the possible new switching state $s_1$ of the solution space $\mathcal{L}_1(s_0)$ ($s_1 \in \mathcal{L}_1(s_0)$) and the phase currents $i_{\mathrm{ph}}$ according to following equation:

$$J_{\mathrm{losses}}(s_0, s_1, i_{\mathrm{ph}}) = P_{\mathrm{cond}}(s_1, i_{\mathrm{ph}}) + P_{\mathrm{sw}}(s_0, s_1, i_{\mathrm{ph}}) \quad (16)$$

The costs for the SoC-balancing in dependence of each possible new switching state $s_1$, the phase currents $i_{\mathrm{ph}}$ and therefore the battery current distribution according to Section III-A, are calculated with (17).

$$J_{\mathrm{SoC}}(s_1, i_{\mathrm{ph}}) = \sum_{c=1}^{3n_{\mathrm{ph}}} (i_{\mathrm{bat},c}(\overline{SoC} - SoC_{\mathrm{c}})^2 \cdot \mathrm{sgn}(\overline{SoC} - SoC_{\mathrm{c}})) \quad (17)$$

Where $\overline{SoC}$ denotes the mean of all SoCs. It is updated in each switching cycle. In simulations the calculation of the costs with squared difference of the SoC-deviation lead to good converging behavior of the SoCs. The square function is a trade-off between stronger consideration of higher deviations (in comparison to linear consideration) and simplicity in calculation (compared to higher powers). Since the square of a difference is always positive, it is necessary to add the signum function of the difference as a factor to the cost function to get equalizing behavior of the SoCs. The cost function considers not only a penalty (positive result of an addend), but also a reward (negative result of an addend) if low charge modules are charged or high charge modules are discharged.

The best state ${s_1}^*$ of the solution space with the lowest combined costs of the objective functions is evaluated using (18) and sent to the three phases.

$${s_1}^* = \underset{s_1 \in \mathcal{L}_1}{\arg\min} (\lambda_{\mathrm{losses}} J_{\mathrm{losses}}(s_0, s_1, i_{\mathrm{ph}}) + \lambda_{\mathrm{SoC}} J_{\mathrm{SoC}}(s_1, i_{\mathrm{ph}})) \quad (18)$$

The weighting factors $\lambda_{\mathrm{losses}}$ and $\lambda_{\mathrm{SoC}}$ can be chosen to enhance specific behavior of the control algorithm and they depend on different operational strategies of the converter (e.g. maximum efficiency, energy utilization). In this contribution, the weighting factors to minimize the total losses of the converter and to balance the batteries in every control step are used separately (one factor is 1 while the other factor is 0 and vice versa). In Section V it is shown that both extremes work and lead to an expected behavior. The combination of these weighting factors ($\lambda_{\mathrm{losses}} > 0$ and $\lambda_{\mathrm{SoC}} > 0$) during operation to achieve best utilization of the stored batteries' energy will be presented in further contributions.

Fig. 4 shows the flow diagram of the implemented MPC algorithm. In the calculation loop, highlighted in orange, $5 \cdot 5^3 = 625$ different switching combinations of the phases

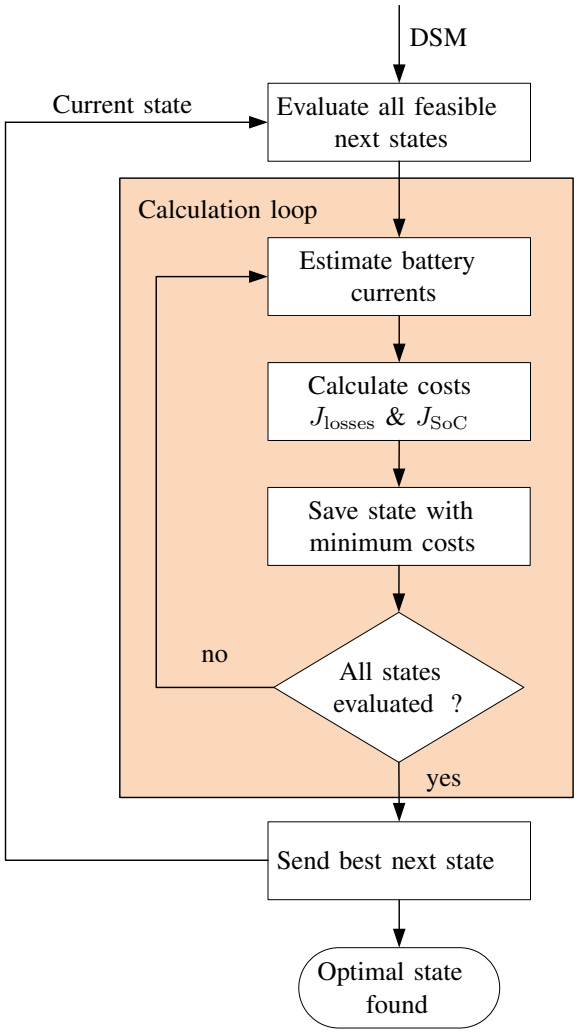



Fig. 4: Flow diagram of the MPC algorithm

are evaluated (estimate battery currents, calculate and compare costs). These 625 combinations result from five different voltage level combinations and five different switching states per phase according to the pre-selected solution space.

## V. Measurement Results

The MPC method was implemented and verified in a lab-scale prototype MMSPC and a test bench with an automotive permanent magnet synchronous machine (PMSM). The technical specifications of the converter and load machine are given in Table I. The control method, including the field-orientated motor current control is executed in real-time at $80\,\text{kHz}$ on a Cyclone IV EP4CE40F23C6 FPGA from Intel, CA. Both the reduction of the phase resistance using a CM voltage and the ability of the control scheme to balance the module battery SoCs is shown in this section.

The ability of the proposed control method to reduce the losses of the converter can be seen in Fig. 5a, which shows the measured current and the voltage of phase U as well as the injected CM voltage $U_{\text{inj}}$. Without taking SoC-balancing into account, the injected voltage reduces the overall conduction losses by decreasing the absolute output voltage of a phase when the output phase current is high, allowing more modules to be used in parallel and therefore reducing the internal resistance. However, the relative line-to-line voltage of the phases is not modified by the CM voltage. In Fig. 5b it can be seen that the batteries see only a small ripple current and no battery current is significantly higher than the current of another battery within the phase except for module 1. Since it is always in parallel to the first modules in every other phase, the optimizer distributes the current maximum phase current among them to reduce overall conduction losses.

TABLE I
System parameters

(a) Model parameters

| Parameter | Symbol | Value |
|---|---|---|
| Modules per phase | $n_{\text{ph}}$ | 5 |
| Modulation frequency per phase | $f_{\text{sw}}$ | $80\,\text{kHz}$ |
| MOSFET Drain-Source-resistance | $R_{\text{DS(on)}}$ | $4.4\,\text{m}\Omega$ |
| Battery nominal voltage | $U_{\text{bat,nom}}$ | $12\,\text{V}$ |
| Battery capacity | $C_{\text{bat}}$ | $18\,\text{Ah}$ |
| Battery resistance | $R_{\text{bat}}$ | $15\,\text{m}\Omega$ |

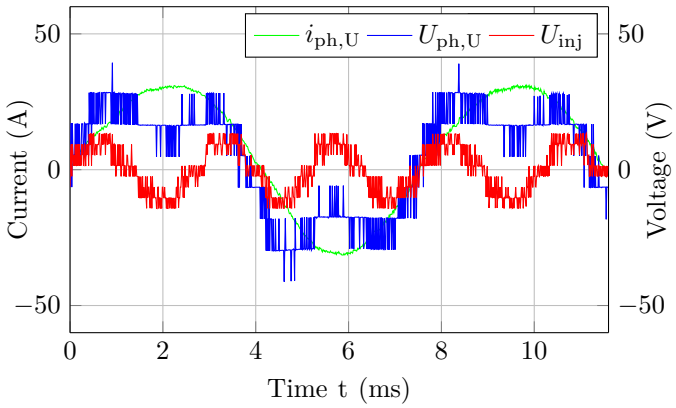
(b) Motor parameters

| Parameter | Symbol | Value |
|---|---|---|
| Pole pairs | $p$ | 16 |
| Permanent magnet flux linkage | $\psi$ | $37\,\text{mV s}$ |
| d-axis inductance | $L_{\text{d}}$ | $44\,\mu\text{H}$ |
| q-axis inductance | $L_{\text{q}}$ | $44\,\mu\text{H}$ |
| Stator winding resistance | $R_{\text{s}}$ | $49.5\,\text{m}\Omega$ |

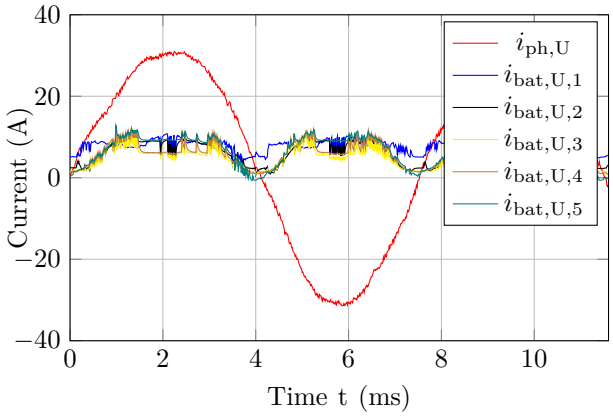
Fig. 6 shows the difference to $\overline{SoC}$ of the SoCs of all battery modules (6a) and the average values of the SoC of the phases (6b). At $t = 0\,\text{s}$ the module SoCs are initialized according to a relation between the open circuit voltage and the current SoC of the battery. During operation, the battery currents are measured with a sampling rate of $80\,\text{kS}$. The change in charge is calculated every cycle and an SoC-estimator adds up the change and estimates the new SoC. Until about $t = 380\,\text{s}$ (dashed black line), loss reduction of the MMSPC is the only objective of the controller, which leads to diverging SoCs ($\lambda_{\text{losses}} = 1$ and $\lambda_{\text{SoC}} = 0$). After $t = 380\,\text{s}$ the balancing of the SoCs is the only objective ($\lambda_{\text{losses}} = 0$ and $\lambda_{\text{SoC}} = 1$). It can be seen that all SoCs are driven towards $\overline{SoC}$. Simultaneously, the differences between phase SoCs are balanced over time. After about $t = 1750\,\text{s}$ all SoCs are within $0.1\,\%$ deviation which is the resolution of the implemented SoC-estimator.

## VI. Conclusion

We have presented and implemented a real-time MPC algorithm that allows the operation of the MMSPC to be optimized at each switching step. The algorithm uses a set of equations for precise current prediction together with the CM voltage as an additional degree of freedom to achieve both the reduction of the converter losses and active balancing of the modules' SoCs within and between the phases. In further research the exact design of the different weighting factors for the objective function will be examined.

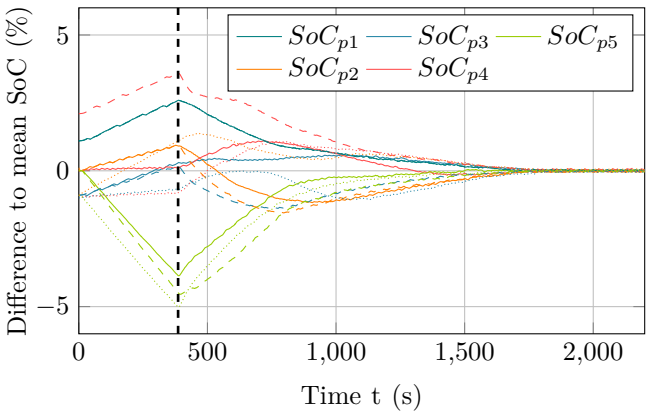



(a) Phase and common-mode voltage and current

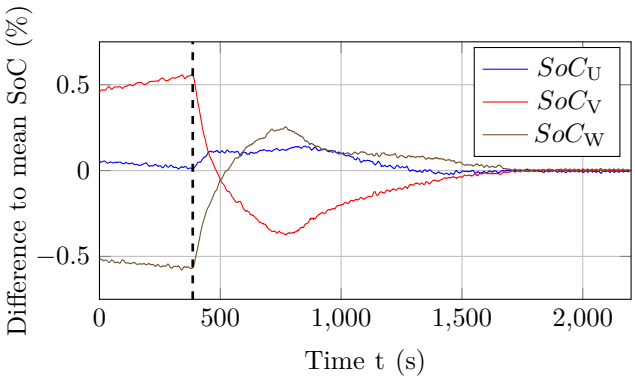



(b) Battery currents of all modules in phase U

Fig. 5: Output voltages and battery currents of the prototype, at $500\,\mathrm{min}^{-1}$ and $27\,\mathrm{Nm}$




(a) SoCs of all modules (solid: $p \mathrel{\widehat{=}}$ phase U, dashed: $p \mathrel{\widehat{=}}$ phase V and dotted: $p \mathrel{\widehat{=}}$ phase W.




(b) Average SoCs of the phases

Fig. 6: The capability of the algorithm to balance the modules and phases is shown by the SoCs converging during operation.

## References


[1] F. Helling, J. Gluck, A. Singer, and T. Weyh, "Modular multilevel battery (M2B) for electric vehicles," *2016 18th European Conference on Power Electronics and Applications, EPE 2016 ECCE Europe*, 2016. DOI: 10.1109/EPE.2016.7695480.

[2] C. Korte, E. Specht, M. Hiller, and S. Goetz, "Efficiency evaluation of MMSPC/CHB topologies for automotive applications," in *Proceedings of the International Conference on Power Electronics and Drive Systems*, vol. 2017-Decem, Institute of Electrical and Electronics Engineers Inc., Feb. 2018, pp. 324–330, ISBN: 9781509023646. DOI: 10.1109/PEDS.2017.8289145.

[3] A. Kersten, M. Kuder, E. Grunditz, Z. Geng, E. Wikner, T. Thiringer, T. Weyh, and R. Eckerle, "Inverter and battery drive cycle efficiency comparisons of CHB and MMSP traction inverters for electric vehicles," *2019 21st European Conference on Power Electronics and Applications, EPE 2019 ECCE Europe*, pp. 1–12, 2019. DOI: 10.23919/EPE.2019.8915147.

[4] J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, 2002, ISSN: 02780046. DOI: 10.1109/TIE.2002.801052.

[5] S. M. Goetz, A. V. Peterchev, and T. Weyh, "Modular multilevel converter with series and parallel module connectivity: Topology and control," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 203–215, 2015, ISSN: 08858993. DOI: 10.1109/TPEL.2014.2310225.

[6] E. Specht, C. Korte, and M. Hiller, "Reducing computation effort by parallel optimization for modular multilevel converters," in *Proceedings: IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, Institute of Electrical and Electronics Engineers Inc., Dec. 2018, pp. 3991–3996, ISBN: 9781509066841. DOI: 10.1109/IECON.2018.8591496.

[7] C. Korte, E. Specht, S. M. Goetz, and M. Hiller, "A Control Scheme to Reduce the Current Load of Integrated Batteries in Cascaded Multilevel Converters," *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, pp. 1–8, 2019.

[8] D. Kraus, E. Specht, T. Merz, and M. Hiller, *Optimized Real-Time Control for Modular Multilevel Converters using Adaptive Neural Networks*. 2019, ISBN: 9789075815313.

[9] S. M. Goetz, Z. Li, A. V. Peterchev, X. Liang, C. Zhang, and S. M. Lukic, "Sensorless scheduling of the modular multilevel series-parallel converter: Enabling a flexible, efficient, modular battery," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, vol. 2016-May, Institute of Electrical and Electronics Engineers Inc., May 2016, pp. 2349–2354, ISBN: 9781467383936. DOI: 10.1109/APEC.2016.7468193.

[10] S. M. Goetz, Z. Li, X. Liang, C. Zhang, S. M. Lukic, and A. V. Peterchev, "Control of Modular Multilevel Converter with Parallel Connectivity-Application to Battery Systems," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8381–8392, Nov. 2017, ISSN: 08858993. DOI: 10.1109/TPEL.2016.2645884.

[11] Z. Li, R. Lizana, A. V. Peterchev, and S. M. Goetz, "Distributed balancing control for modular multilevel series/parallel converter with capability of sensorless operation," *2017 IEEE Energy Conversion Congress and Exposition, ECCE 2017*, vol. 2017-Janua, no. 1608929, pp. 1787–1793, 2017. DOI: 10.1109/ECCE.2017.8096011.

[12] ——, "Predictive control of modular multilevel series/parallel converter for battery systems," in *2017 IEEE Energy Conversion Congress and Exposition, ECCE 2017*, vol. 2017-Janua, Institute of Electrical and Electronics Engineers Inc., Nov. 2017, pp. 5685–5691, ISBN: 9781509029983. DOI: 10.1109/ECCE.2017.8096945.

[13] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range - Power Tech Conference Proceedings, 2003 IEEE Bologna," *2003 IEEE Bologna PowerTech - Conference Proceedings*, vol. 3, pp. 1–6, 2003. DOI: 10.1109/PTC.2003.1304403.

[14] Infineon Technologies AG, "Datasheet: IPB044N15N5," 2016.