Channel Geometry Scaling Effect in Printed Inorganic Electrolyte-Gated Transistors

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***Abstract*— Unlike nanoscale silicon transistors, printed thin-film transistors usually rely on micrometer size channel lengths. The device dimensions, the morphology of the channel material, and the interface properties strongly influence important device parameters such as the threshold voltage (V_{th}) and the transconductance parameter (k). In this article, we analyze and model the dependence of critical electrical device properties of printed, electrolyte-gated transistors, based on crystalline indium oxide channel, for various device geometries. It is shown that the threshold voltage scales with the charge density at the electrolyte channel interface and is hence linearly dependent on the channel length (L). Furthermore, nonlinear scaling effects in the transconductance parameter and in the ON-current are studied, which turn out to be dependent on both, channel width and length. Finally, we present a scaling model capturing the width/length dependencies of the studied transistor technology which enables the correct simulation of logic gates.**

***Index Terms*— Channel geometry scaling, electrolyte-gated transistors (EGTs), oxide semiconductors, printed electronics (PEs).**

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I. Introduction

PRINTED electronics (PE) technologies offer a variety of attractive features such as on-demand printing and realization of circuits and systems on flexible and rigid substrates. All such features are crucial for sensors, Internet of Things (IoT), and soft robotics [1], [2]. Traditionally, organic materials are used to develop PE transistors [3]–[5]. However, due to various challenges including low carrier mobility and reliability issues associated with such printing technologies [6], there has been considerable research for processes based on inorganic materials [7]–[9]. One such technology is the inkjet-printed electrolyte-gated transistor (EGT) technology [10] (also referred to as EGFET). Inorganic channel materials (such as indium oxide) based EGTs have much higher mobility compared to transistors based on organic materials and can operate at a very low supply voltage (< 1 V) due to electrolyte-gating [11]–[14].

EGT technology has improved over time starting from the initial material based studies [15] to electronic design automation (EDA) flows [16]. Research on all such topics has helped to scale the technology from device to circuit level and to improve the design flow. However, the top-gate EGT geometry scaling effect on performance parameters has not been modeled and integrated into the design flow. The scaling of such parameters is mainly dependent on the device materials stack and printing process. Thus, the parameter scaling trend could be different for different technologies. The effects of geometrical scaling should be systematically studied and modeled to update the compact models in the design environment (also referred to as process design kit). Such predictive models provide a proper interface between technology and circuit design.

In this study, we perform a comprehensive empirical study by printing devices with different channel geometry to evaluate the key performance parameters of the EGT, i.e., threshold voltage (V_{th}), transconductance parameter (k), and ON-current (I_{ON}). We would like to point out, that we use geometric scaling of the channel area only to tune the electrical characteristics using the same fabrication process steps, which allows to be captured during the circuit design phase. This is in addition to other work where, e.g., the material stack, channel doping, and process steps were altered to change the device characteristics, which yields more fundamental changes in the electrical transport mechanisms [18], [19]. Usually, charge carrier mobility is discussed as an important performance parameter and is calculated by extracting transconductance and estimating

a constant gate-capacitance. As the gate-capacitance and the effective area of the gate are not straightforward to estimate in EGTs due to their rough interfaces and voltage-dependent gate-capacitance [20], instead of electron mobility we report and discuss transconductance as a performance parameter that can be extracted from measurement data directly. The transconductance parameter is the product of mobility (μ) and gate capacitance (C_g). It is observed that V_{th} scales with the channel length (L), which resembles in a short-channel effect observed in MOSFET for channel lengths less than 2 μm [21]–[23]. Interestingly, this effect is visible in EGT technology for $L \geq 10$ μm. On the other hand, k and I_{ON} scale with channel width (W) and length (L). The parameter k is limited in the long-channel devices due to the high surface roughness resulting in voids at the semiconductor–insulator interface and reduced mobility [24]. The scaling behavior of the performance parameters is reported, modeled, validated, and added into the design environment. It will help to provide more accurate device models to design and optimize circuits and systems within the optimal range of these parameters in the future.

This article is organized as follows. In Section II, we discuss the related work on channel geometry scaling for printed transistors. In Section III, experimental details and analysis of the performance parameters for EGT are discussed. Section IV addresses the modeling of performance parameters and extension of the EGT dc model. Finally, Section V concludes this work.

II. Related Work on Geometrical Scaling Effect

Multiple studies were reported in the past for the geometrical scaling effect in printed transistors. The performance parameters trends were analyzed for organic thin-film transistors (OTFTs) [25], indium-zinc-oxide (a-InZO) TFT [26] and in-plane EGTs [27]. In all aforementioned studies, the threshold voltage (V_{th}) and mobility (μ) trends are studied and reported. Liu *et al.* [25] claim that for small channel devices carrier mobility transport is limited by contact injection. Additionally, μ increases while V_{th} decreases with the increase in channel length (L). However, for $L > 40$ μm, both parameters saturate. Lee *et al.* [26] claim that μ is independent of channel length. However, V_{th} increases with L due to intrinsic voltage stress instabilities. The work by Mondal *et al.* [27] is the closest compared to our study, where the authors have analyzed the performance parameters scaling for in-plane EGTs. The authors claim that the mobility decreases with the increase in L due to high trap charge densities and nonuniform channel surface for long-channel devices. On the other hand, they also reported V_{th} scaling with L but there is no discussion on the trend.

It can be concluded from all studies that the trends of device parameters are dependent not only on channel geometries but also on the device fabrication process and materials stack. That is why a systematic study and modeling of such geometrical effects is required to account for them in the simulation environment.

III. Experimental Details

Different EGTs with various channel widths and lengths are evaluated to study the scaling behavior of performance parameters. The channel length is varied from 10 to 100 μm and the channel width is varied from 200 to 600 μm. From the characterization data we extract and report the threshold voltage (V_{th}), transconductance parameter (k) and ON-current (I_{ON}) in linear and saturation regimes. Finally, we analyze and discuss these parameters with their dependence on channel geometry scaling.

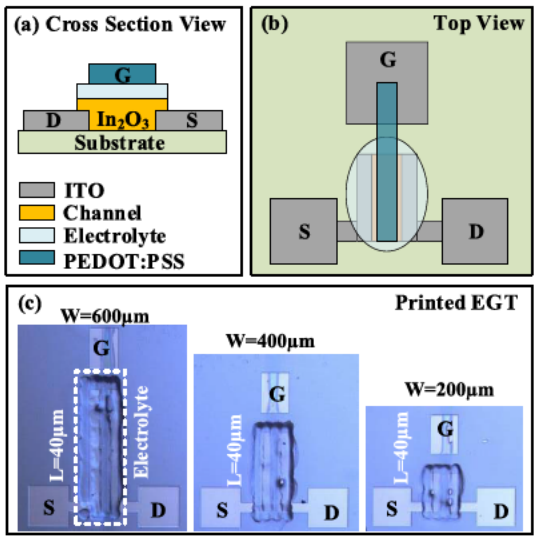

Fig. 1. (a) Cross section view, (b) top view, and (c) optical image of printed EGTs.

A. Device Fabrication and Characterization

The EGTs are printed on a glass substrate sputtered with indium tin oxide. First, drain-, source- and gate-electrodes are structured using electron-beam lithography. Next, the indium precursor is printed as a channel between drain- and source-electrodes. After that, the substrate is annealed at 400 °C for 2 h. Then, the composite solid polymer electrolyte (CSPE) is printed on top of the channel, and finally, the poly(3,4-ethylenedioxythiophene) (PEDOT):polystyrene sulfonate (PSS) based top-gate is printed. All materials are printed using a Dimatix DMP-2831 ink-jet printer. Detailed information about the EGT structure and materials is provided in [10]. Fig. 1 shows the side- and top-view of the EGT and optical pictures of the printed EGTs with different channel widths.

For this work, we printed top-gate EGTs with different channel geometries. The channel lengths (L) are 10, 20, 40, 60, 80 and 100 μm while channel widths (W) are 200, 400 and 600 μm for each channel length. In total, transistors with 18 unique channel geometries are printed. Ten EGTs are printed for each geometry making it 180 transistors in total. For all devices, the current–voltage (I–V) characteristics are measured using a Keysight 4156C precision semiconductor parameter analyzer. The results for a total of 90 devices (five transistors per geometry) are used in our analysis. The rest of the transistors were discarded due to unstable electrical characteristics, bad pin contacts and/or gate leakage paths. The small hysteresis does not have an impact on device characteristics (not shown). The measurements were performed at a relative humidity level of 50% and room temperature. The electrical

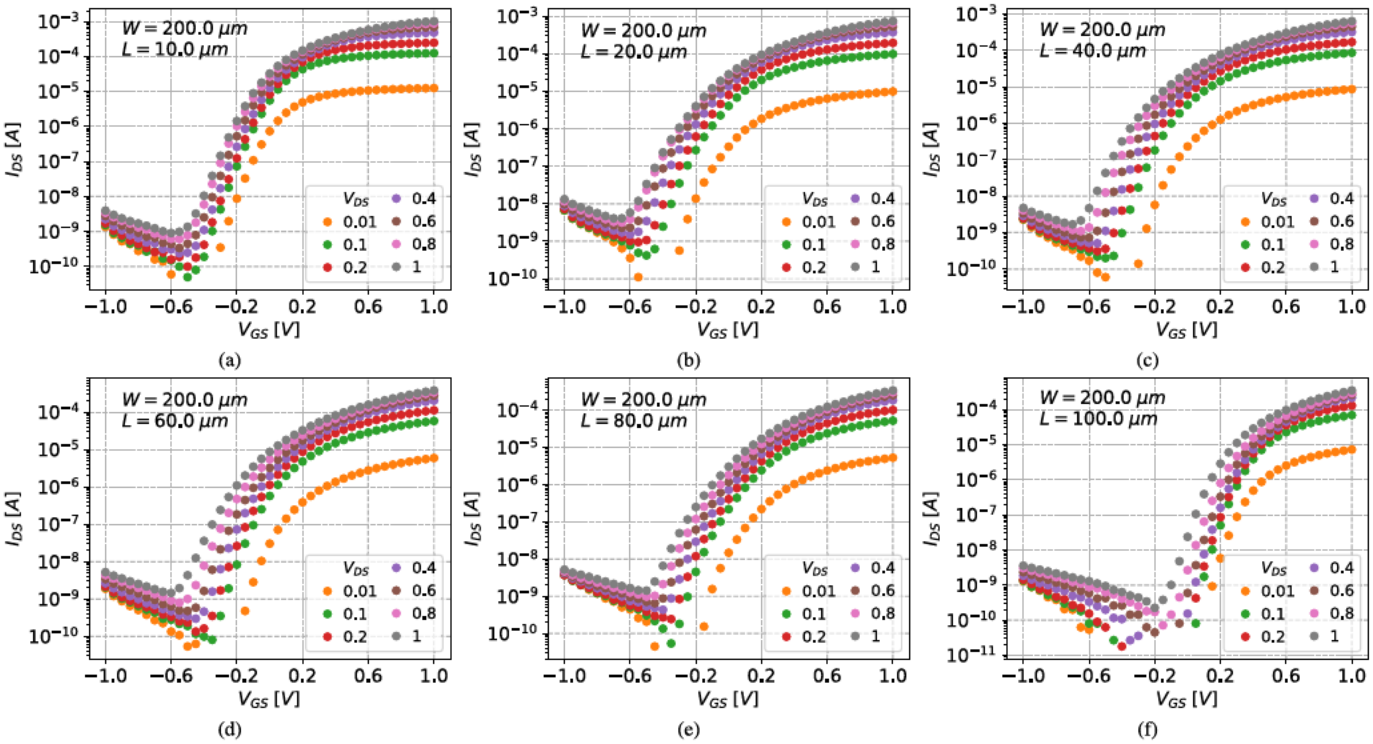

Fig. 2. Measured transfer characteristics of EGT with channel width (W) = 200 μm and channel length (L) = 10 to 100 μm. (V_{GS} = −1 to 1 V and V_{DS} = 0.01 to 1 V) [17].

measurements of the devices for $W = 200$ μm and $L = 10$ to 100 μm are shown in Fig. 2. The gate–source voltage (V_{GS}) is swept from −1 to 1 V for drain–source voltage (V_{DS}) of 0.01 to 1 V.

B. Parameters Extraction

The I–V characteristics of the transistors are used to extract the performance parameters The parameters are extracted in the linear ($V_{DS} = 0.2$ V) and saturation ($V_{DS} = 1.0$ V) regimes to observe their trend in both operating regimes of the EGT. The V_{th} is extracted using the H-integral function which is the typical method for TFTs [28]. The H-integral function is given by the following equation:

$$H(V_{GS}) = \frac{\int_0^{V_{GS}} I_{DS}(V_{GS})}{I_{DS}(V_{GS})} dV_{GS}. \quad (1)$$

The transconductance parameter ($k = \mu \times C_g$) is extracted by extending the slope of the linear part in the $\sqrt{I_{DS}}$ versus V_{GS} measurements. I_{ON} is extracted from the transfer characteristics at maximum applied gate–source voltage (i.e., $V_{GS} = 1.0$ V). The measured electrical characteristics of an EGT and extraction of the V_{th} is shown in Fig. 3.

C. Analysis and Discussion

The extracted threshold voltage (V_{th}), transconductance parameter (k) and ON-current (I_{ON}) for different channel geometries are shown in Fig. 4. It can be observed that all such parameters show a clear trend with respect to channel geometry. V_{th} is dependent on channel length (L) while there is no clear trend for V_{th} dependence on channel width (W). We attribute the V_{th} scaling to a low charge density at the electrolyte-channel interface for long-channel devices, in addition to, e.g., morphological arguments [29] which remain unaffected by the model presented here. On the other hand, k and

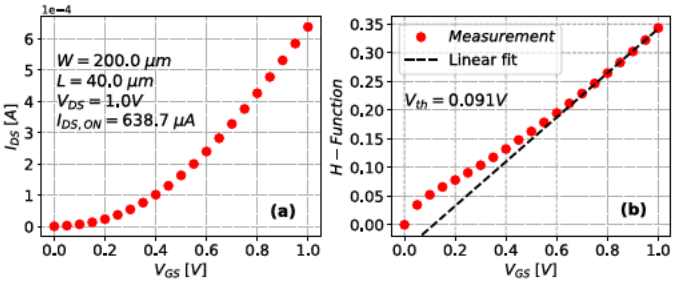

Fig. 3. (a) Measured transfer characteristics of an EGT and (b) extraction of threshold voltage (V_{th}) through H-integral function ((1)) from the measured current-voltage (I–V) characteristics in saturation regime (V_{DS} = 1.0 V).

I_{ON} scale with both W and L. Both parameters are influenced by the channel surface roughness and large crystallites in the channel material. Further discussion regarding the scaling behavior of each performance parameter is as follows.

1) Threshold Voltage Scaling: As V_{th} increases with an increasing channel length L up to 100 μm without saturation, we rule out conventional short-channel effects originating from the source/drain electrodes. Instead, we propose a model that takes the interface capacitances between the electrolyte and the other transistor materials (such as channel, top-gate, drain- and source-electrodes) into account. We assume the ions to be mobile throughout the whole electrolyte. Additionally, we assume a double layer build-up at its interfaces. Due to low voltage operation, we neglect redox reactions at the electrolyte interfaces, i.e., the charge is conserved in the electrolyte. For simplicity, we assume the drain–source voltage (V_{DS}) to be small compared to the gate–source voltage (V_{GS}), but note that this is not a limitation of the model presented.

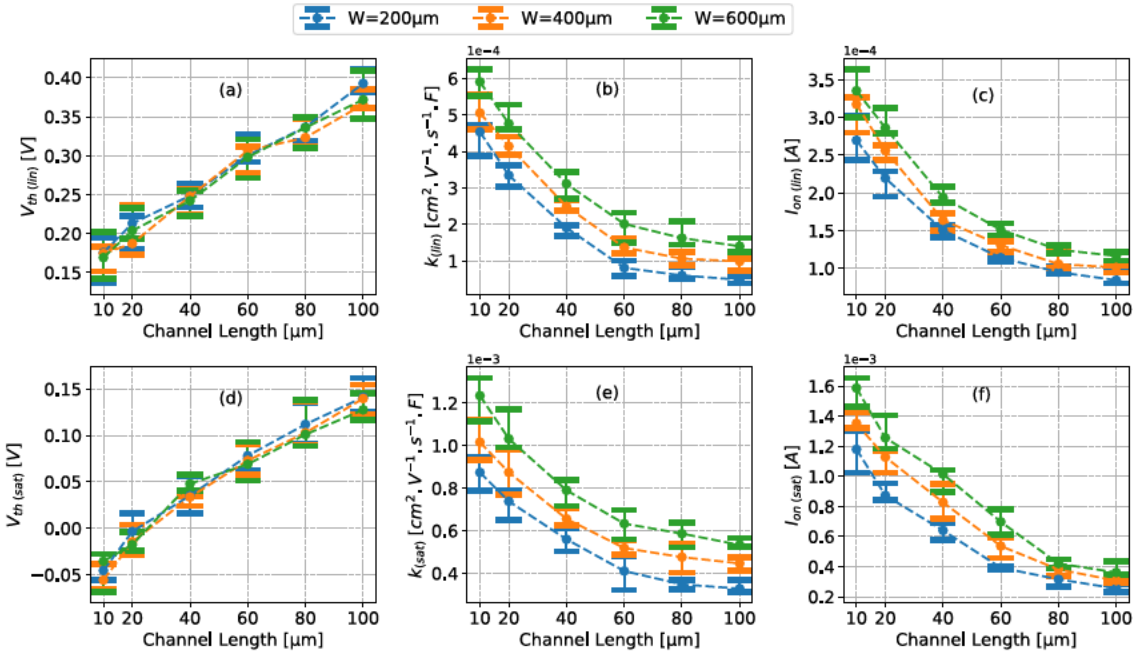

Fig. 4. Threshold voltage (V_{th}), transconductance parameter (k) and ON-current (I_{ON}) scaling trend with respect to channel length scaling for different channel widths in (a)–(c) linear ($V_{DS} = 0.2$ V) and (d)–(f) saturation ($V_{DS} = 1.0$ V) regime.

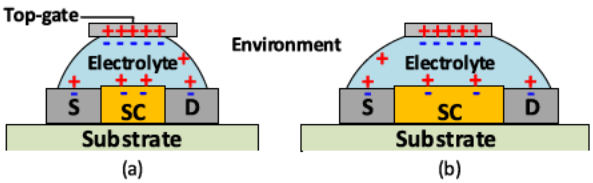

Fig. 5. Conceptual cross section view of the channel area (not to scale), including the charge carrier accumulation in the electrolyte and electrodes for a positive gate voltage. "SC" denotes the semiconductor channel. (a) shows the charge distribution for a smaller channel length compared to (b), this implies a smaller charge density at the electrolyte-channel-interface in the latter case (S = source, D = drain).

In Fig. 5(a), a conceptual cross section of the transistor and the net charge distribution in the electrolyte is shown. If the top-gate is, e.g., positively charged, negative ions accumulate in the electrolyte near the top-gate, i.e., that interface capacitance is charged. The accumulation of negative ions at the top-gate leads to an excess of positive ions in the rest of the electrolyte. As the bulk of any electric conductor in equilibrium has to be field free, there may be no field in the electrolyte and positive and negative charge has to compensate each other. The excess positive ions repelled by the top gate have to accumulate at the other interfaces.

The charge density at the electrolyte-channel interface changes if we increase the channel length and keep all other dimensions fixed, as depicted for a longer channel in Fig. 5(b). As the channel area increases with its length and the top gate size and gate voltage being fixed, the charge density at the electrolyte-semiconductor interface decreases. This implies that for the transistor in Fig. 5(b), a higher gate voltage is needed to induce the same charge carrier density in the semiconductor as in the transistor in Fig. 5(a). This immediately relates to a higher threshold voltage for a long channel device.

This model applies to the presented EGTs due to the limited resolution in printing the top gate. The top-gate is supposed to cover the whole channel and overlap with the source/drain-electrodes as little as possible (see Fig. 1). However, the width of the top-gate measures at least ≈ 40 μm, which is defined by the printer resolution and positioning position accuracy as well as the ink. This implies that the size of the top gate is constant for channel lengths from 10 to 40 μm and covers a larger area as desired. Top gate size increases for longer channels, but its accuracy remains limited since the channel length is in the same order of magnitude as the minimum possible printing size of the top gate. We, therefore, assume the top gate size increases sublinearly with the channel area. However, we may assume a linear correlation of the top gate width and the channel width, as the channel width is one order of magnitude larger than its length. This matches our observation that V_{th} does not depend on W.

2) Transconductance Parameter Scaling: As can be seen in Fig. 4, in both operating regions, the transconductance parameter value decreases with the increase in channel length. This can be attributed to channel surface roughness due to the formation of large crystallites when the printed oxides (such as In_2O_3) are heated at high temperatures. The surface roughness causes gaps/voids at the semiconductor–electrolyte interface leading to charge traps and reduced mobility values [24]. Mondal *et al.* [27] have confirmed this behavior by estimating the interfacial trap charge densities. The scanning electron microscope (SEM) image [1] of an EGT's cross section is shown in Fig. 6. where the crystalline structure formed in the channel material (indium oxide) are clearly visible.

3) ON-Current Scaling: ON-current (I_{ON}) is dependent on multiple physical parameters such as V_{th}, k, W and L. The trend for I_{ON} is also shown in Fig. 4 where it can be seen that, similar to transconductance, the I_{ON} decreases for long-channel devices. This is mainly due to the increased channel resistance

[1]The SEM images is adapted from Figure S9b in the supporting information of [9].

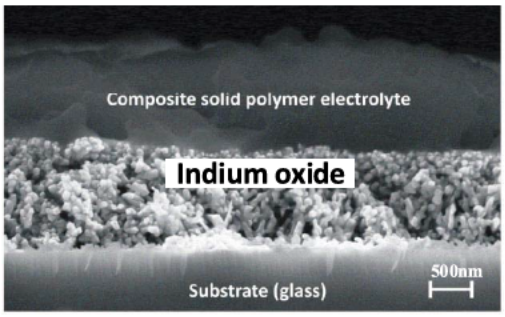

Fig. 6. Cross section SEM image of indium oxide-dielectric interface (annealing temperature = 400 °C). Reproduced with permission [9].

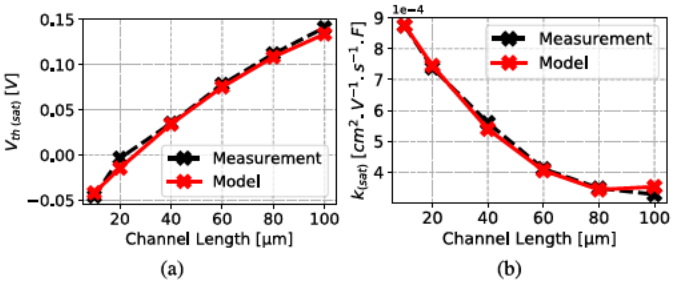

Fig. 7. (a) Threshold voltage (V_{th}) and (b) transconductance parameter (k) model comparison with the parameters extracted/estimated from the measurement data of EGTs (channel width = 200μm) in the saturation regime.

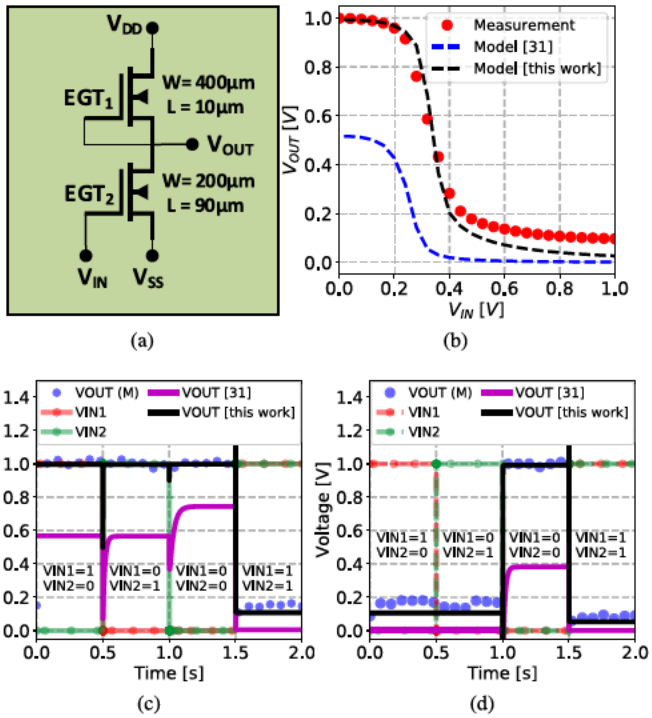

Fig. 8. (a) TT logic-based inverter circuit. The comparison of measured and simulation of (b) voltage transfer characteristic of an inverter, (c) transient behavior of NAND, and (d) NOR TT-based logic gates (VOUT (M) is the measured output voltage).

and reduced mobility in long-channel devices. Additionally, the disproportionate decrease in I_{ON} (with the increment in L) is attributed to the high probability of encountering defects in the channel for long-distance transport [27].

IV. Parameters Modeling

The channel geometry dependence for V_{th} and k, being the crucial performance parameters of the EGT, should be modeled to reflect their behavior in the simulation environment. It is important to optimize such parameters during the design cycle, for device/technology development as well as for circuit design. As I_{ON} is dependent on multiple parameters, the model for V_{th} and k can be added to the EGT dc model to capture the I_{ON} trend. Before discussing the modeling procedure, we give a short introduction of the EGT dc model in Section IV-A.

A. EGT DC Model

The EGT dc model was proposed in the past [30]. The drain current equation for the EGT dc model is given by

$$I_{DS} = I_0\left(\ln\left(f_3 + e^{\frac{v_p - v_s}{2}}\right)^{\gamma} - \ln\left(f_3 + e^{\frac{v_p - v_d}{2}}\right)^{\gamma}\right) \quad (2)$$

where

$$I_0 = 2nf_1\frac{W}{L}\phi_t^2 \quad v_p \approx \frac{V_{GS} - (V_{th} - f_4 V_{DS})}{\frac{n}{f_2}\phi_t}$$

and

$$n = \frac{1}{SS \cdot \phi_t \cdot \ln(10)}.$$

The channel geometry is represented by parameters W and L as channel width and length, respectively. The parameter n is the slope factor while v_p, v_d, and v_s present channel, drain, and source potentials, which are normalized by the thermal voltage ϕ_t. The threshold voltage (V_{th}), power-law parameter (γ), and subthreshold slope (SS) are extracted empirically by extrapolating the linear regions of the measured characteristics curve. The rest of them are fitting parameters (f_1, f_2, f_3 and f_4), which are extracted by minimizing the relative error between the measured and model generated transistor characteristics curve. Parameter f_1 is referred to a fitting parameter in the EGT dc model [30] as it was not extracted from the measurement data. However, it is the sum of multiple parameters and the transconductance parameter (k) is one such parameter. In this study, the k is extracted from the measurement data before calculating the fitting parameter f_1. Hence, k and f_1 are treated as two separate model parameters.

B. Channel Geometry Scaling Model

The EGT dc model is extended by accounting the channel geometry scaling effect on V_{th} and k. As discussed earlier in Section III-C, k is dependent on W and L both while V_{th} is dependent on L only. Least absolute shrinkage and selection operator (LASSO) regression [31] is used for the model parameter extraction. The model equations are updated as

$$I_0 = 2nf_1 k\phi_t^2, \quad k = g_1(W, L), \quad V_{th} = g_2(L) \quad (3)$$

where g_1 and g_2 are the polynomial functions obtained through LASSO regression. These functions are used to calculate the V_{th} and k based on the channel geometry. The model and measurement comparison for parameters in saturation regimes are shown in Fig. 7. The R^2 error for the V_{th} model is 0.96 while for k it is 0.97. For circuit level validation, we design the transistor-transistor (TT) based logic gates

[see Fig. 8(a)] and compare the measurements with simulation results. In the TT-logic design, the pull-up logic is realized through a normally-on EGT ($V_{\text{th}} \leq 0$ V) while pull-down logic is realized using a normally-off EGT ($V_{\text{th}} \gg 0$ V). The detailed information about the EGT-based TT-logic design is given in [29]. Fig. 8 shows the measurement and simulation results comparison for the TT-logic based inverter, NAND and NOR gates (pull-down logic: $W = 200$ μm, $L = 90$ μm, pull-up logic: $W = 400$ μm, $L = 10$ μm). It is shown that the proposed model matches very well with the measurement (output voltage) with negligible difference for the output voltage levels.

V. Conclusion

In this study, we have measured, analyzed, and modeled the critical performance parameters of thin-film, electrolyte gated indium oxide channel transistors (EGTs). In partic-ular, we have studied the effect of channel length scal-ing on transistor performance parameters. We observe an increase of the threshold voltage V_{th} with the channel length, which we attribute mainly to a lower ion density at the electrolyte-channel interface. The transconductance k decreases with channel length due to larger crystallites and therefore increased surface roughness and more voids. The ON-current I_{ON} decreases for longer channels due to the decrease of k and the higher resistance of long-channel devices. This enables us to tune the performance parameters of the devices. In addition, we have modeled the performance parameters trend and included it into EGT's dc model. The model is validated by comparing the simulation results with measurement data of devices and logic gates, which match very well.

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References

[1] S. Khan, L. Lorenzelli, and R. S. Dahiya, "Technologies for printing sensors and electronics over large flexible substrates: A review," *IEEE Sensors J.*, vol. 15, no. 6, pp. 3164–3185, Jun. 2015.

[2] Y. S. Rim, S.-H. Bae, H. Chen, N. De Marco, and Y. Yang, "Recent progress in materials and devices toward printable and flexible sensors," *Adv. Mater.*, vol. 28, no. 22, pp. 4415–4440, Jun. 2016.

[3] J. S. Chang, A. F. Facchetti, and R. Reuss, "A circuits and systems perspective of organic/printed electronics: Review, challenges, and contemporary and emerging design approaches," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 7, no. 1, pp. 7–26, Mar. 2017.

[4] S. H. Kim *et al.*, "Electrolyte-gated transistors for organic and printed electronics," *Adv. Mater.*, vol. 25, no. 13, pp. 1822–1846, Apr. 2013.

[5] H. Sirringhaus, "25th anniversary article: Organic field-effect transistors: The path beyond amorphous silicon," *Adv. Mater.*, vol. 26, no. 9, pp. 1319–1335, Mar. 2014.

[6] J. Noh, M. Jung, Y. Jung, C. Yeom, M. Pyo, and G. Cho, "Key issues with printed flexible thin film transistors and their application in disposable RF sensors," *Proc. IEEE*, vol. 103, no. 4, pp. 554–566, Apr. 2015.

[7] W. Wu, "Inorganic nanomaterials for printed electronics: A review," *Nanoscale*, vol. 9, no. 22, pp. 7342–7372, 2017.

[8] G. A. Torres Sevilla and M. M. Hussain, "Printed organic and inorganic electronics: Devices to systems," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 7, no. 1, pp. 147–160, Mar. 2017.

[9] S. K. Garlapati *et al.*, "Electrolyte-gated, high mobility inorganic oxide transistors from printed metal halides," *ACS Appl. Mater. Interface*, vol. 5, no. 22, pp. 11498–11502, Nov. 2013.

[10] G. Cadilha Marques, D. Weller, A. T. Erozan, X. Feng, M. Tahoori, and J. Aghassi-Hagmann, "Progress report on 'from printed electrolyte-gated metal-oxide devices to circuits,'" *Adv. Mater.*, vol. 31, no. 26, 2019, Art. no. 1806483.

[11] S. K. Garlapati, M. Divya, B. Breitung, R. Kruk, H. Hahn, and S. Dasgupta, "Printed electronics based on inorganic semiconductors: From processes and materials to devices," *Adv. Mater.*, vol. 30, no. 40, Oct. 2018, Art. no. 1707600.

[12] X. Yu, T. J. Marks, and A. Facchetti, "Metal oxides for optoelectronic applications," *Nature Mater.*, vol. 15, no. 4, pp. 383–396, Apr. 2016.

[13] A. Liu *et al.*, "Fully solution-processed low-voltage aqueous In_2O_3 thin-film transistors using an ultrathin ZrO_x dielectric," *ACS Appl. Mater. Interface.*, vol. 6, no. 20, pp. 17364–17369, 2014.

[14] X. Feng, C. Punckt, G. C. Marques, M. Hefenbrock, M. B. Tahoori, and J. Aghassi-Hagmann, "Impact of intrinsic capacitances on the dynamic performance of printed electrolyte-gated inorganic field effect transistors," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3365–3370, Aug. 2019.

[15] S. K. Garlapati *et al.*, "Ink-jet printed CMOS electronics from oxide semiconductors," *Small*, vol. 11, no. 29, pp. 3591–3596, Aug. 2015.

[16] F. Rasheed, M. Hefenbrock, R. Bishnoi, M. Beigl, J. Aghassi-Hagmann, and M. B. Tahoori, "Crossover-aware placement and routing for inkjet printed circuits," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 16, no. 2, pp. 1–22, Apr. 2020.

[17] G. C. Marques, "Circuit design and compact modeling in printed electronics based on inorganic materials," Ph.D. dissertation, Dept. Inform., Chair Dependable Nano Comput., Karlsruhe Inst. Technol., Karlsruhe, Germany, Apr. 2020.

[18] F. Neuper, A. Chandresh, S. A. Singaraju, J. Aghassi-Hagmann, H. Hahn, and B. Breitung, "Tailoring threshold voltages of printed electrolyte-gated field-effect transistors by chromium doping of indium oxide channels," *ACS Omega*, vol. 4, no. 24, pp. 20579–20585, Dec. 2019.

[19] R. Martins, P. Barquinha, I. Ferreira, L. Pereira, G. Gonçalves, and E. Fortunato, "Role of order and disorder on the electronic performances of oxide semiconductor thin film transistors," *J. Appl. Phys.*, vol. 101, no. 4, Feb. 2007, Art. no. 044505.

[20] X. Feng, G. C. Marques, F. Rasheed, M. B. Tahoori, and J. Aghassi-Hagmann, "Nonquasi-static capacitance modeling and characterization for printed inorganic electrolyte-gated transistors in logic gates," *IEEE Trans. Electron Devices*, vol. 66, no. 12, pp. 5272–5277, Dec. 2019.

[21] H. Liu, A. T. Neal, and P. D. Ye, "Channel length scaling of MoS_2 MOSFETs," *ACS Nano*, vol. 6, no. 10, pp. 8563–8569, Oct. 2012.

[22] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H. S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, no. 3, pp. 259–287, Mar. 2001.

[23] V. K. Khanna, *Short-Channel Effects MOSFETs*. New Delhi, India: Springer, 2016, pp. 73–93.

[24] K. Okamura and H. Hahn, "Carrier transport in nanocrystalline field-effect transistors: Impact of interface roughness and geometrical carrier trap," *Appl. Phys. Lett.*, vol. 97, no. 15, Oct. 2010, Art. no. 153114.

[25] X. Liu, M. Kanehara, C. Liu, and T. Minari, "Ultra-high-resolution printing of flexible organic thin-film transistors," *J. Inf. Display*, vol. 18, no. 2, pp. 93–99, Apr. 2017.

[26] S. Lee, Y. Song, H. Park, A. Zaslavsky, and D. C. Paine, "Channel scaling and field-effect mobility extraction in amorphous InZnO thin film transistors," *Solid-State Electron.*, vol. 135, pp. 94–99, Sep. 2017.

[27] S. K. Mondal, N. Devabharathi, and S. Dasgupta, "Effect of semiconductor surface homogeneity and interface quality on electrical performance of inkjet-printed oxide field-effect transistors," *Nanotechnology*, vol. 30, no. 43, Aug. 2019, Art. no. 435201.

[28] A. Ortiz-Conde, F. J. G. Sánchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," *Microelectron. Rel.*, vol. 42, nos. 4–5, pp. 583–596, Apr. 2002.

[29] G. C. Marques *et al.*, "Printed logic gates based on Enhancement- and depletion-mode electrolyte-gated transistors," *IEEE Trans. Electron Devices*, vol. 67, no. 8, pp. 3146–3151, Aug. 2020.

[30] F. Rasheed, M. S. Golanbari, G. Cadilha Marques, M. B. Tahoori, and J. Aghassi-Hagmann, "A smooth EKV-based DC model for accurate simulation of printed transistors and their process variations," *IEEE Trans. Electron Devices*, vol. 65, no. 2, pp. 667–673, Feb. 2018.

[31] T. Hastie, R. Tibshirani, and J. Friedman, *The Elements of Statistical Learning: Data Mining, Inference and Prediction*, 2nd ed. New York, NY, USA: Springer, 2009.