Development of Fully Printed Oxide Electronics for Flexible Substrates

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I declare that I have developed and written the enclosed thesis completely by myself, and have not used sources or means without declaration in the text.

Karlsruhe; April 28, 2021

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(Surya Abhishek Singaraju)

To Amma, Akka -
two awesome women in my life

Abstract

With the emergence of Internet of Things (IoT) and the desire to refashion everyday things into becoming smart and intelligent, there is high demand for new generation sensors that are flexible and even wearable. Billions of such sensors would need to be manufactured, thereby requiring low cost, easy processing and large area manufacturing on flexible substrates. Printing as a means of ink deposition is economically very viable method to manufacture flexible electronics and the quest to fully printing electronics is gathering more attention. Thereupon, digitally printed electronics has received increased interest in the past two and half decades, thanks to the ability to upscale easily and at low costs. In order to satisfy the complicated specifications of future flexible sensing devices, basic electronic components such as capacitors and transistors need to be developed in complex circuits on flexible substrates. While flexible organic semiconductors are quite developed in terms of printing process and circuit technologies, their predominant p-type nature, environmental instability and low mobility are points of concern. Therefore, there is a need to develop roadmaps for printing environmentally stable and high mobility metal-oxide semiconductors on flexible substrates such as PET/PEN. Another advantage is that oxide semiconductors are also widely available as n-type semiconductors. In this regard, fully printing electronic circuits on non-rigid substrates such as PET/PEN or paper requires attention towards many factors. These include adhesion on the substrate, compatibilty with other functional components as well as substrate-suitable processing temperature for each component. Performance identifying parameters such as device mobility, mechanical stability and reproducibility need to be paid attention to. The electronic components of the printed circuits include conductive parts (including electrodes and interconnects) that require metallic inks (such as silver, graphene), semiconducting active materials made of metal-oxides (such as ZnO, In_2O_3), and electronically insulating components for gate dielectrics such as high capacitance electrolytes. Therefore, printing and processing techniques of the above mentioned functional inks are to be designed such that they match the physical requirements of flexible substrates. At the same time, the chemical and electrical compatibility of all components with one another are to be ensured in order to maximize the performance of the printed circuit.

Subsequently, the work in this thesis focuses on the development of printed oxide transistors and logics on flexible substrates. A comprehensive study of layer wise development of fully printed electronic devices is attempted as part of this thesis. Electrolyte gated transistors (EGTs) are first fully printed on glass substrates, in which (In_2O_3) is the active semiconductor and conductive graphene ink formed the passive components such as, electrodes, resistors and interconnects. Different device architectures are investigated to minimize contact resistance and unwanted chemical reactions as well as to maximize the active area on the semiconductor. Special attention has been given to key parameters of the fully printed EGTs such as capacitance, switching speeds, current on-off ratio,

subthreshold swing and threhold voltage tested on a large number of devices. Electrolyte gating facilitated operating voltages less than 1 V which makes the devices compatible with printed batteries. The EGTs also have contact resistance of 33 Ωcm, which is several orders lower than other dielectric gated devices.
To test the transistors for potential utilization in complex circuits, logics such as transistor-resistor logic (TRL) are printed and tested as inverters. In order to print these on flexible polyimide substrate, careful attention is devoted to the preparation of the substrate for printing and parameters such as the signal gain, propagation delay and rise/fall times of the printed inverter determined. A signal gain of 3.5 is observed for the TRL structures, which is similar to the observed value for similar structures on rigid substrates. Furthermore, the mechanical stability of the oxide semiconductor on polyimide has been determined over a number of cycles. Finally, the processing temperature of the oxide is reduced to suit processing on a PEN substrate. Photonic curing method is utilized to make the processing of the In_2O_3 semiconductor suitable on the PEN substrate. By using photonic curing, furnace necessity is eliminated for the formation of oxide from precursor, which reduces the processing times in the order of 10^5, from 2 hours to 20 milliseconds. In short, this work therefore can be packaged into a successful quest for fully printing oxide electronics on cheap plastic substrates, thereby, paving way for digitized and roll-to-roll compatible electronic applications such as flexible large-area displays and wearable sensors.

Zusammenfassung

Mit dem Erscheinen des Internets der Dinge (IoT) und dem Wunsch Alltagsgegenstände intelligenter zu machen, steigt die Nachfrage an mechanisch flexiblen oder in Textilien integrierbare Sensoren dieser nächsten Generation. Schon jetzt werden unzählige dieser Sensoren benötigt, um den immer größer werdenden Bedarf zu decken. Aus diesem Grund, sind kostengünstige Herstellungsprozesse, die eine großflächige Herstellung auf einem flexiblen Substrat erlauben von Interesse. Das Drucken funktionaler Tinten erlaubt die Herstellung kostengünstiger elektronischer Bauteile auf flexiblen Substraten. Das vollständige Drucken von elektronischen Bauelementen in den letzten zwei Jahrzehnten immer mehr an Bedeutung gewonnen,dank einfacher und kostengünstiger Skalierung dieser gedruckten Bauelemente. Um den komplexen Anforderungen zukünftiger Sensoren gerecht zu werden müssen gedruckte elektronische Elemente wie beispielsweise Kondensatoren oder Transistoren auf flexiblen Substraten, integriert werden. Flexible, überwiegend p-leitende, organische Halbleiter sind bis zum jetzigen Zeitpunkt weit verbreitet, sind aber unter normalen Umgebungsbedingungen instabil und weisen eine geringe Ladungsträgerbeweglichkeit auf. Metalloxide, die ebenfalls n-leitende Halbleiter sind, können die Nachteile von organischen Materialien überwinden und zudem auf flexiblen Substraten, wie z.B. PET oder PEN aufgebracht werden. Nichtsdestotrotz wird die Herstellung von vollständig gedruckten Schaltungen auf flexiblen Substraten von vielen verschiedenen Faktoren beeinflusst. Insbesondere ist es wichtig, dass die Bauteile auf dem Substrat haften, kompatibel mit anderen elektronischen Bauelemente und die Prozesstemperaturen auf das Substrat abgestimmt sind. Auch der Einfluss von Leistungsparametern wie der Ladungsträgerbeweglichkeit, der mechanischen Stabilität oder der Reproduzierbarkeit sind nicht zu vernachlässigen. Die elektronischen Komponenten einer Schaltung beinhalten elektrisch leitende Elemente (Elektroden und elektrische Verbindungen), die leitende Tinten wie Silber oder Graphen), Halbleiter basierend auf Metalloxiden (ZnO, In_2O_3) und elektrische Isolatoren wie beispielsweise als Gate-Dielektrikum dienende Elektrolyte benötigen.. Daher müssen die zuvor aufgeführten Materialien unter Berücksichtigung der physikalischen Gegebenheiten des Substrates in einem Druckprozess integriert werden. Des Weiteren müssen die chemische und elektrische Kompatibilität aller Komponenten berücksichtigt werden, um die Leistung der gedruckten Schaltung zu maximieren. Daher liegt der Fokus der vorliegenden Arbeit auf der Entwicklung von gedruckten (Metall)Oxid-Transistoren und Logikgattern auf flexiblen Substraten. Insbesondere auf die Architektur der Transistoren wird hierbei eingegangen. Durch ein Elektrolyt isolierte Transistoren, mit Indiumoxid als aktiven Semikonduktor und den durch konduktive Graphentinte realisierten Elektroden und elektrischen Verbindungen als passive Komponenten, werden vollständig auf ein Glassubstrat gedruckt. Verschiedene Transistorarchitekturen werden analysiert, um Kontaktwiderstände und chemische Reaktionen zu minimieren und gleichzeitig die aktive Fläche im Halbleiter zu maximieren. Ein besonderes Augenmerk liegt dabei auf

den Schlüsselparametern der gedruckten Transistoren wie beispielsweise Kapazitäten, Schaltgeschwindigkeit, Ein-, Ausschaltströme und Schwellwertspannung, die für eine große Anzahl an Transistoren analysiert wird. Die Isolation der Transistoren mit einem Elektrolyten erlaubt es, die eingesetzten Versorgungsspannungen auf 1 V zu reduzierenund als gedruckte Batterien zur Spannungsversorgung einzusetzten. Diese Transistoren zeigen mit nur 0.33 Ωcm einen deutlich niedrigeren Kontaktwiederstand als Transistoren mit konventionellem Dielektrikum. Um die Transistoren für den potentiellen Einsatz in elektronische Schaltungen zu untersuchen, werden Logikgatter in Form von Invertern in der Widerstands-Transistor-Logik (TRL) gedruckt und analysiert. Um diese Gatter auf ein mechanisch flexibles Polyamid Substrat zu drucken, wird besondere Aufmerksamkeit auf die Vorbereitung des Substrats und die Ermittlung kritischer Parameter wie die Signalverstärkung und Signallaufzeiten gelegt. Die Signalverstärkung von 3.5 ist für diese Inverter identisch zu Invertern wellche auf unflexiblen Substrate gedruckt sind. Des Weiteren wird die mechanische Flexibilität von Indiumoxid auf dem Polyamidsubstrat über mehrere Zyklen hinweg untersucht. Abschließend, Für die Kompatibilität mit den PEN-Substratewird die Prozesstemperatur vom Indiumoxid reduziert . Das Formen eines Indiumoxid-Films wird dabei durch optische anstatt thermischen Methode erzielt, wodurch die Prozesszeit von 2 Stunden auf etwa 20 Millisekunden reduziert werden kann. Zusammenfassend beschäftigt sich die vorliegende Arbeit mit der Entwicklung von vollständig gedruckten elektronischen Bauelementen, die auf Metalloxiden basieren und die auf preisgünstigen Plastiksubstraten prozessiert werden., Diese Entwicklung ebnet den Weg für den zukünftigen Einsatz in digitalisierten und role-to-roll kompatiblen elektronischen Anwendungen wie Großraum Displays und tragbaren Sensoren.

Contents

Part I.

Introduction

1. Printed and Flexible Electronics

1.1. Motivation

The dawn of the age of reason occurred with a great invention of humankind: the printed word. Printing as a means of communication and discussion dates back to the ancient Central Asian civilization from where, Marco Polo brought the knowledge of the movable type printer to Europe[1]. Subsequently, during the renaissance period of mid 15^{th} century, the development of the printing press and typography by Johannes Gutenberg[2] in the German city of Mainz resulted in a revolution of mass communication among people. Ever since, many varieties of large area printing such as rotogravure, offset, screen printing etc, have been developed for communication and knowledge storage. Five hundred years later, the construction of the bipolar junction transistor by John Bardeen, Walter Brattain and William Shockley resulted in another revolution of ultrafast data processing and communication among people[3]. Thereafter, the world has witnessed a surge in electronics development such as the integrated circuit, microprocessor, memory storage devices etc. Presently, in the second millennium, a combination of printing and electronics is expected to once again revolutionize communication, not just among people but also between physical objects.

The concept of internet of things (IoT), in which, not just computers, tablets or smartphones, but all physical objects (things) would be connected to each other through internet is the basis for opening up a broad spectrum of new technologies[4]. These technologies include flexible displays, intelligent sensors, wearable health monitors, identification tags and energy harvesters that would be manufactured on cheap flexible substrates. It is projected that in the future, trillions of such sensors need to be fabricated[5]. In order to reduce manufacturing costs, the number of processes need to be inexpensive and minimal, unlike conventional manufacturing that requires expensive processing methods at every layer such as semiconductor growth, masking, lithography, etching etc. Printing as a deposition technique for all the layers eliminates the need for additional processes and cheap printable inks can easily be manufactured to be relevant even for flexible substrates. Other cost cutting avenues are reduction of the high vacuum and high temperature requirement for processing electronics, especially on flexible substrates. To print thin films on any given substrate, functional inks[6, 7, 8] developed either by dissolving or dispersing a powder solute in a liquid solvent should be deposited on any substrate. Solution coating methods such as spin coating or dip coating or doctor-blading are widely used to manufacture printed batteries, solar cells and conductive lines[9, 10, 11] but these processes require mask or subtracting process and are therefore limited in terms of directed deposition.

Electronic circuit manufacture on flexible substrates is easier with digital printing methods compared to other solution processed methods. Drop-on-demand printing techniques such as inkjet printing, microplotting or aerosol jet printing provide a comparative advantage since digitally structured designs can be printed with ease when using these technologies. Printing is now used to fabricate structures such as resistors, interconnects, p-n diodes and solar cells[12, 13]. However, electronic circuits, especially the ones using inorganic (oxide) materials are yet to be fully printed on flexible substrates. This research gap has been addressed in this thesis and the outcome could be potentially translated to mass manufacturing of flexible electronics using roll to roll technology[14].

Employment of printing for electronics fabrication implies printing of every element of the device without employing hybrid fabrication such as lithographically prepared electrodes. So far, most of printed electronics research has focused on physical vapour deposition or solution coating methods for the passive components, for example as source, drain and gate electrodes in a transistor. Through such methods, researchers were able to produce reproducible devices but such hybrid fabrication add up to the costs and thus, fully printed methods that display reliable and reproducible devices are sought after[15]. There has been considerable development in fully printed flexible organic materials, not just because of the inherent flexible nature of polymers, solution formation and the high tensile strength of thin film polymers[16]. However, organic materials seemingly exhibit high resistivity, low environmental stability, low semiconductor mobility and are typically hole (p-type) semiconductors. To build complex electronic circuits, the counterpart n-type semiconductors are sought after. Inorganic materials such as oxides exhibit high mobility, are very stable in air, can be found to be electron (n-type) semiconductors, and are therefore an attractive choice as materials for printed electronics. Added to this is the possibility of making inexpensive and environment friendly inks as precursors for oxides. The composition of the ink affects the processing temperature and therefore the precursor recipe can be tailored for processing temperature of choice. Apart from the semiconducting part, a fully printed electronic circuit consists of two other components, namely conducting and dielectric parts. Conductive inks are required to fabricate contacts for semiconductors, interconnects, resistors and can be made on flexible substrates from inks such as silver and graphene[17]. To perform the function of dielectrics, printable ion gels and polymer electrolytes are the most suitable for flexible substrates. Given such a variety of inks for electronic components and given the need for compatibility between individual components, a comprehensive study of a fully printed system of printed, flexible electronics is necessary. For example, metals are prone to chemical reactions in the presence of electrolytes[18], which is detrimental to the electrical performance of the printed devices. Therefore, the interface between various components of an electronic device, such as: metal-semiconductor, metal-insulator, semiconductor-insulator and also the substrate effects have to be precisely understood. Overall, an attempt has been made here, to develop fully printed electrolyte-gated transistors using n-type oxide semiconductor (In_2O_3) and graphene electrodes and resistors. Printed inverters using these transistors are demonstrated on flexible substrates as well. Detailed characterization of materials, device architecture and electrical characterization - static as well as transient are demonstrated.

1.2. Outline of Thesis

In this thesis, the development of fully printed transistors on plastic substrates will be discussed in three stages: first, the evolution and thorough investigation of every aspect of a fully printed transistor will be discussed, second, its mechanical strength and electrical characteristics when printed on flexible substrates will be evaluated. In the third, a reduction in processing temperature is shown, in order to suit PET/PEN. The second part includes chapters on the basic understanding of a transistors, the concept behind the work, the state of the art in fully printed electronics and the materials, methods.

The experimental results begin in chapter 5 of third part, with the buildup of a fully printed electrolyte-gated oxide transistor using graphene passive electrodes and printed by digitally controlled processes on glass substrates. The device architecture and the materials used are characterized comprehensively. A detailed understanding of the graphene-metal oxide semiconductor contacts that include the contact morphology and the electrical contact resistance is shown. Stable electrochemical windows for operation are investigated to identify unwanted chemical reactions. Capacitance is calculated using standard electrochemical characterization and the device mobility is calculated, thereafter giving a clear picture of the performance of the EGT. All in all, the most suitable material combination and device architecture for a fully printed EGT is demonstrated, which helps in designing electronic circuits.
Chapter 6 explains in detail, the applicability of the fully printed electrolyte-gated oxide transistors and inverters, on flexible substrates. The printability of the inks is studied on thermally stable flexible substrates, since the processing temperature is retained as on glass substrates. The effect of the surface modification of the polymer surface on the oxide film morphology is analysed and a flexible inverter developed. Complete electrical characterization of the inverter and mechanical stability are determined. The successful reproducibility of the inverter is as well shown.
Chapter 7 showcases photonic curing of precursor[19] ink as a suitable method for oxide film processing on plastic substrates with low glass transition temperatures, such as polyethylene naphthalate/terephthalate (PEN/PET). Printing electronics on PEN/PET films is sought after, since they are cheap, possess high mechanical strength, with well defined processing methodology and are most widely utilized in packaging, transparent displays. Thus, they are very attractive for transparent displays, photovoltaics, electrochromic windows as well as flexible and wearable applications. Photonic sintering[20] is quite appealing as the curing procedure for the precursor since it does not affect the polymer substrate and processes the oxide film in very short times. A comprehensive study of this includes material characterization of the photonic cured oxide film as well as electrical characterization of transistors prepared on transparent PET substrates.
The thesis is summarized in the fourth part and an outlook provided, while the fifth part consists of the appendix chapters.

Part II.

Fundamentals and Background

2. Printed Transistors and Inverters

The primary objective of the thesis is to find suitable solution based inorganic materials, device architectures for printing and processing methods to develop inorganic electronic devices on flexible substrates. In the process, an attempt to understand in detail, the physical and electrochemical compatibility between every element of the printed device is shown in this thesis. The studies include electrical characterization of printed transistors and inverters; surface profilometry and microscopy to observe the morphology of printed films; and electrochemical studies, to understand the chemistry at the interfaces. The present chapter introduces in order, the concept of printing techniques, the basic understanding of a transistor, the interaction between the anatomical components of the transistor, its electrical characteristics and the build up to an inverter. Since the goal is to print devices on flexible substrates, the surface energy and thermal limitations for flexible substrate are discussed.

2.1. Printing Techniques

Digital printing is attractive to fabricate electronics because of the possibility to deposit any given circuit design over flexible substrates with relative ease[21]. This is an advantage over state of the art thin film deposition techniques such as physical vapor deposition[22] or coating methods in which the use of high vacuum and photoresist/mask restricts circuit design on flexible substrates. Moreover, the deposition area of these techniques is lesser. Therefore, solution processed techniques that do not require vacuum find more traction as effective deposition techniques over large area[23]. Other advantages of solution processing include fast, cheap preparation and easy handling. A number of solution processing techniques have been developed such as rotogravure printing, screen printing, doctor blading and spin coating, which are already in commercial use[24]. For example, spin coating is used tremendously in flexible photovoltaic applications, organic light emitting diodes[10] and doctor blading used for printed batteries[9]. However, these still require mask and are considered to be 'subtractive' processes. With the heavy demand for billions of low cost printed electronics in recent times, digital printing technique is more relevant. In this regard, printing techniques such as ink-jet, aerosol-jet, microplotting - have been invented. Since the digital printing methods are additive in nature, there is also little scope for material wastage and hence is environment friendly. As part of this thesis, we discuss two of such digital printing methods, namely inkjet printing and microplotting.

2.1.1. Inkjet printing

As the name suggests, in this approach ink can be jetted by the application of a potential energy which is converted into mechanical energy. Inkjet printing is a classic example of a 'drop on demand' technique which means that ink can be dispensed in a controlled manner as and when required from a height, requiring no contact with the substrate. Seen in Figure 2.1a is a piezoelectric sheet attached to the nozzles which is activated by a tunable sinusoidal potential. The nozzle is movable longitudinal to the substrate at an adjustable height. The sinusoidal potential influences the size and volume of the emerging droplet controlling which, facilitates guided deposition of printed patterns. The droplet is also shaped by the nozzle diameter. Typical diameter is 20 μm and the emanating drop is 10 pL in volume, and hence, can offer printed resolutions as small as 20 μm. Droplet formation is very important because in inkjet printing, individual drops make up any desired pattern or shape after deposition. The distance between the center of two printed drops is known as drop spacing and is vital for the coalescence or separation of the drops. Therefore, the diameter of the drops need to comply with the acceptable range of drop spacing in the inkjet printer, to ensure the film is uniform during the drying process. Since the nozzle diameter is fixed, the drop size is generally controlled by the fluid properties of the ink. The printability of any liquid is illustrated by a plot of Weber number vs the Reynolds number in Figure 2.1b.

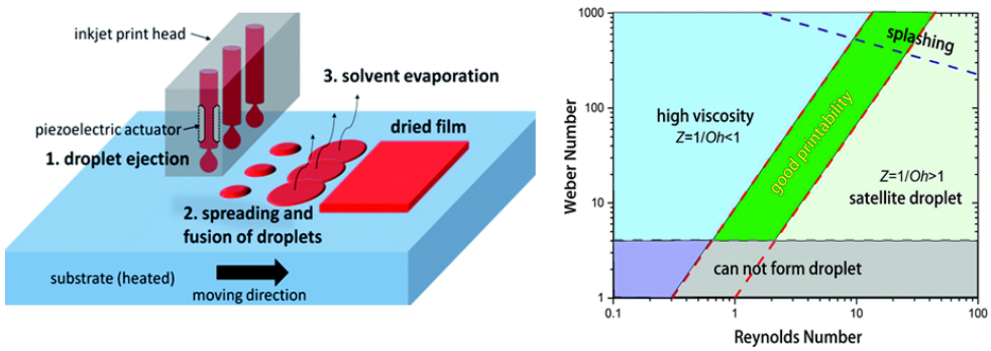

Figure 2.1.: Functioning of inkjet printer and viscosity requirement. a) Piezoelectric attached to the nozzles can be subjected to mechanical stress by applying a potential, to dispense the liquid. The inkjet nozzle moves in three dimensions, with respect to the substrate. The drop-spacing influences the proper formation of the dried film. b) The slope of square root of Weber number vs Reynolds number is the Ohnesorge number. The viscosity of the ink is defined by this slope. Reproduced with permission from RSC[25, 26]

The inverse of the Ohnesorge number (Z=1/Oh) is a function of Reynold's number (Re) and the Weber number (We) and is given by Equation (2.1). Drop formation and printability is most suited when 1<z<10. Below this range, drop formation is not feasible since the ink viscosity is too high. Above the range, the ink gets too dilute and this leads to abberations in printing.

$$Z = \frac{1}{Oh} = \frac{We^{1/2}}{Re} \tag{2.1}$$

Re is inversely proportional to the viscosity of the liquid[27]. Therefore liquids with high Re are unsuitable for inkjet printing due to their high viscosity and the ones with high Re culminate in the possibility of spewing unwanted smaller drops around the desired pattern called satellite drops. The acceptable range of Re is indicated by the green patch in the middle of the graph. This is typically within a viscosity range of 1-10 cPs. The very precise viscosity range accounts for high resolution of printed films in the range of 20-50 μm. The viscosity also determines the flow of the ink through the nozzles (free flow/clogging) as well as the film thickness. In addition to the viscosity of the ink, the surface tension and the particle 'loading' in case of dispersion become important parameters. We number is inversely proportional to the surface tension of the ink and therefore surface tension and viscosity are key parameters to have good inkjet printed inks. To ink-jet printable ink, a precursor, where in a metal salt is dissolved in a low viscous solvent. Therefore the probability of nozzle clogging is reduced significantly. While the frequency of the waveform of the potential applied to the piezoelectric plays a crucial role in the dispensing of the drop, another parameter that influences printing is the drop spacing. The wetting properties are dependent on the substrate chemical composition, surface roughness and contact angle with the drop and can be modified using suitable techniques. Since the amount of material required is about 2 mL, there is little scope for wastage. There have been numerous works that demonstrated inkjet printing as a viable option for electronics manufacture and many inks, especially conductive ones exist. Sekitani et al[28] printed silver nanoparticle inks and organic transistors on flexible substrates over a decade ago. They were able to print wireless power transmittors and demonstrated high power transmission and position sensing based on inkjet printed micro electro mechanical system (MEMS) switches and organic transistors respectively. The ability of inkjet printing to deposit inks based on high mobility single crystals was showcased by Minemawari et al[29]. They focused on controlled printing of the ink by fine-tuning the surface tension of the solvent and thereby controlling the evaporation process. Thus inkjet printing is a proven approach towards printing high frequency and high mobility electronics.

2.1.2. Microplotting

Microplotting is another drop-on-demand technique that as well employs a piezoelectric for printing. In this technique, a capillary is glued to a piece of piezoelectric material. The capillary being a hollow tube has a resonant frequency which changes as the ink fills the capillary. The capillary is vibrated at frequencies between 100 kHz and 700 kHz using the piezoelectric and the resonant frquency detected from the vibration amplitudes. This frequency ν that is used to dispense the ink on the substrate is given by Equation (2.2), where L is the length of the capillary and the velocity, v is dependent on the exerted pressure (P) and as well, on the mass density (ρ) of the capillary, which in turn depends on the ink present inside. The factor, γ is the laplace correction used to determine the

resonant frequency of a hollow tube.

$$\nu = \frac{nv}{2L} \tag{2.2}$$

where,

$$v = \sqrt{\frac{\gamma P}{\rho}}$$

The printing of patterns on a substrate by microplotting is akin to the functioning of a fountain pen, making contact with the substrate is necessity. The forces acting on the ink at the tip of the capillary during printing are schematized in Figure 2.2.

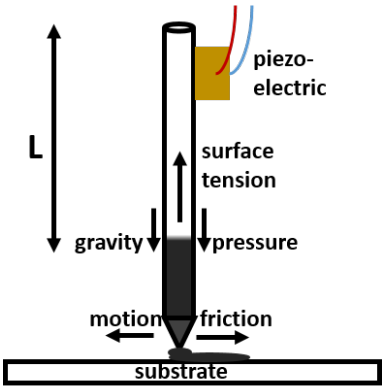

Figure 2.2.: Schematic of microplotter capillary. The ink is filled by capillary attraction. The various forces acting on the ink that assist in dispensing and pattern formation are denoted. It should be noted that the capillary is in contact with the substrate.

The surface tension of the liquid (with a concave meniscus) assists in the capillary rise. To counter this and dispense the ink, a potential is applied to the piezoelectric material. This, in addition to the weight of the liquid, pushes the ink downwards and the frictional forces assist in writing structures. Microplotting is well suited for inks with wider range of viscosities and surface tension as compared to inkjet printing while the resolution can be tuned simply by changing the diameter of the capillary tip. Glass capillaries can be heat pulled to achieve tip diameters that range just few microns. Even though microplotting is a type of contact printing, it profits by the fact that particle dispersion inks with any particle size can be easily printed with it. Being capillary-assisted, microplotting requires just about 100 μL of ink, making it very economical in terms of material usage. Different inks, varying from oxide and metallic nanoparticle dispersions to complicated carbon nanotube inks can be printed using the microplotting technique. Cai et al[30] have shown that dense $BaTiO_3$ films can be printed as gate dielectrics with high, precise resolutions of 150 μm. Robinson et al[31] successfully utilized microplotting for flexible electronics by printing silver nanodispersions and in further steps, Chen et al[32] printed every component of a carbon nanotube based transistor. For these reasons, both the above printing techniques

are very fascinating for manufacturing flexible electronics and can be used to fully print field-effect transistors.

2.2. Structure of Transistor

The electronic devices that are aimed to be printed as part of this thesis are metal oxide semiconductor field effect transistors (MOSFET) and inverters, since they serve as the basic units for most of the electronic circuits. In general, a transistor is an electrical switch that is made of three functional components:
1. Dielectric, which does not offer free space for electrons
2. Conductor, which offers free space for electrons and
3. Semiconductor, which allows space for electrons under some conditions.
The semiconductor is the tunable component whose resistance can be changed by the application of a potential on a conducting plate which is separated from the semiconductor by an insulator.

2.2.1. Insulators - dielectrics/electrolytes

Insulators generally have a dual role of minimising leakage currents and can be polarized by applying a potential. These are known as dielectrics and their dielectric properties influence their utility in MOSFETs. There exist many insulating metal oxides that have high dielectric constant and are hence known to polarize well[33]. These oxides are typically deposited as ultra thin films (0.5 nm) with atomic smooth surface using epitaxial (layer-by-layer deposition) techniques such as atomic layer deposition (ALD) or molecular beam epitaxy (MBE)[34]. Oxide dielectrics can also be solution deposited and thickness in tens of nanometers can be obtaining through coating. For example, in a metal-insulator-semiconductor (MIS) capacitor, "high-κ" dielectrics such as HfO_2 of about 30 nm are spin-coated as the gate components[35]. HfO_2 has very high permittivity/dielectric constant (κ) and hence leads to high capacitance indicating that the amount of charges induced to form a conducting channel in the semiconductor at a given potential are high. This can be mathematically seen in eq refeq:Capacitance, where capacitance (C) of a dielectric in between two parallel plates is proportional to the product of κ and permittivity of vacuum (ϵ_0), the cross sectional area (A) and to the inverse of the thickness, d. Thin films give rise to higher capacitance values.

$$C = \frac{\kappa \epsilon_0 A}{d} \tag{2.3}$$

In a transistor, the gate electrode acts as one plate whereas the semiconductor acts as the other parallel plate. At any given potential difference between the plates, the charge induced depends on the magnitude of the capacitance. The capacitance and the response frequency are further influenced by the intrinsic properties such as orientation and relaxation of ions in the dielectric material[36]. Therefore, very small distance between the

parallel plates is desired to ensure that the charge is influenced by the potential on the metal and not the space-charge limited field. In printed electronic circuits, to obtain such thin capacitors and highly smooth interface between dielectric and semiconductor (much like Si-SiO_2 interface), electrolytes such as composite solid polymer electrolyte (CSPE), which is known to be used in commercial capacitors and batteries can be printed as the gate dielectrics[37, 38]. Electrolytes have high ionic conductivity (10^{-2}-10^{-3} Scm^{-1}) and offer good switching frequencies at low potential[39, 40]. Electrolyte is basically a salt solution and is not just easily printable at room temperature but also highly conformal as in, it follows the surface corrogation on which it is printed. The backbone polymer forms a gel-matrix along the surface after the solvent evaporates and ions can migrate within this matrix. Thus, the polymer electrolyte is ionic conducting but is electronically insulating and makes up a good dielectric material. The capacitance of the electrolyte is fairly large because electric field penetrates only within few nanometers and thus form very thin capacitors at the interfaces[41]. Such a field penetration at the interface can be explained by the electrical double layer models proposed by Helmholtz and in later times, Gouy-Chapman and Stern[42].

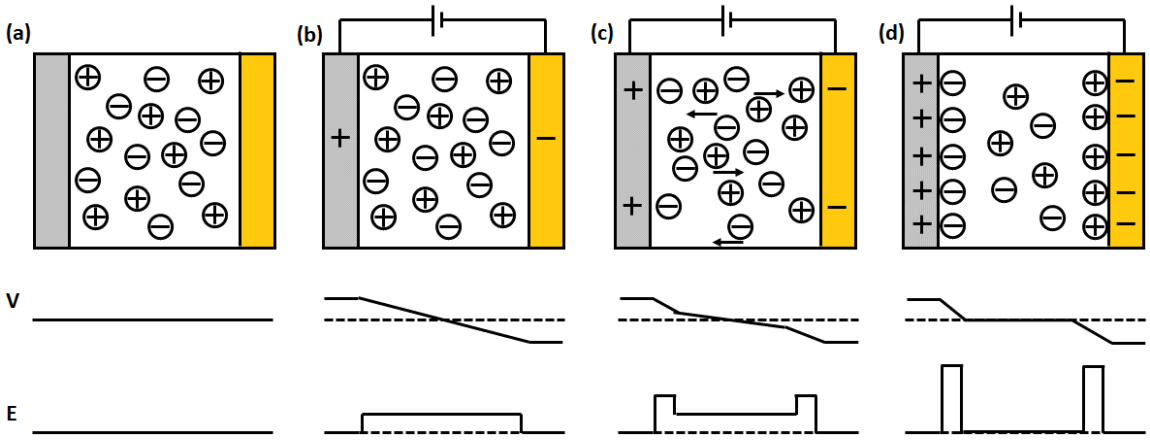

Figure 2.3.: Stepwise formation of electrical double layer. a) Charge inside unbiased electrolyte is neutral. b) Electrolyte in contact with electrodes is subjected to a bias and hence, an electric field. c) The bias leads to ionic migration in electrolyte, potential drop gets sharper at the interfaces. d) Once the double layer is formed, there is no field in the bulk of the electrolyte. Only at the interfaces.

The nature of the ultrathin double layer formation can be seen stepwise in Figure 2.3. Initially, the ions are equally distributed throughout the bulk of the electrolyte (Figure 2.3a) with no potential across. When two electrodes (ex. gate and semiconductor) are placed in electrolyte (Figure 2.3b), the resultant bias difference leads to the migration of ions towards oppositely polarized electrodes (Figure 2.3c). The potential drop and the resultant electric field then shift towards the interfaces and within the bulk of the electrolyte, the potential reduces, meaning that the charges inside the electrolyte tend to be neutral. In steady state (Figure 2.3d), the potential drop and the corresponding constant field is seen only across the double layer with the electrolyte bulk remaining neutral. The double layer

is basically a capacitor with few nanometers thickness which is important to estimate operation potentials. The nature of the potential drop across this layers in the steady state in Figure 2.3d can be understood using the models proposed in Figure 2.4.

The early model that proposes a linear potential drop across the double layer was proposed by Helmholtz (Figure 2.4a). However, since the ions migrate throughout the bulk of the electrolyte, the ion distribution and therefore the potential drop is spread into the bulk of the electrolyte. This was modeled as an exponential drop into the bulk of the electrolyte by Gouy-Chapman (figure 2.4 b). The limitation of the model is that the high density of charges at the interface is disregarded. This was corrected in the Stern model (figure 2.4c), which is a combination of the linear Helmholtz layer at the interface and a diffuse layer, into the electrolyte bulk. Therefore, this model accommodates the high density of charges at the interface and also the charge migration beyond the double layer. All the models depict that the field is present within few nanomaters from the interfaces. Thus, according to Equation 2.3, the capacitance of the electrolyte is fairly large (10-100 μFcm^{-2}). Since the charge accumulation is proportional to the capacitance and the input potential (Q = CV), such large capacitance would require low input potentials and is compatible with printed batteries.

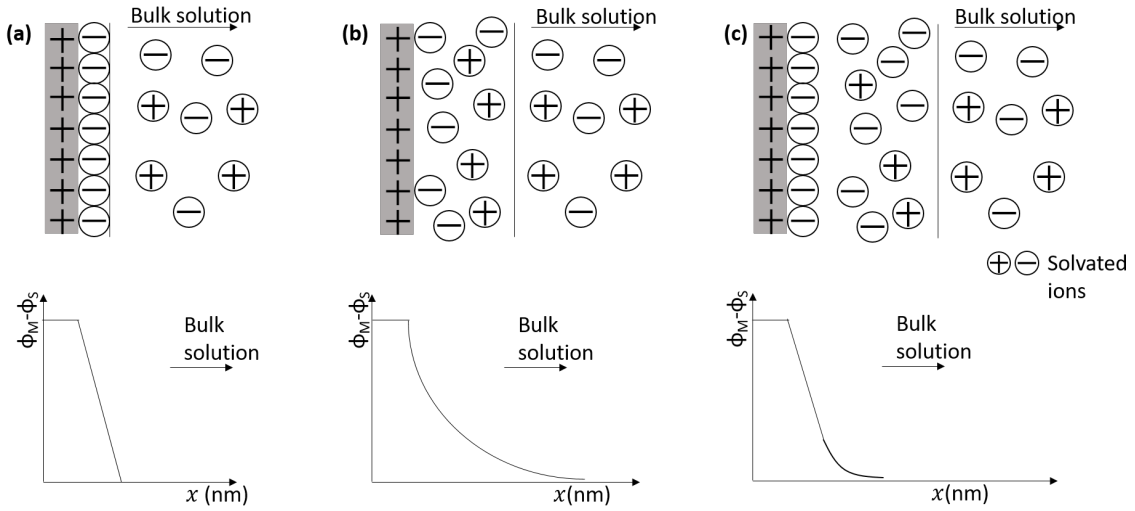

Figure 2.4.: Various models for electrical double layer formation. a) Helmholtz model proposes that the potential drops at the double layer within few nm and goes to zero. b) Gouy-Chapman model proposes an exponential decay of the potential into bulk of the electrolyte. c) Stern model is a mixture of both the above models.

Owing to the above mentioned double layer formation, electrolytes possess high capacitance values and therefore induce large amounts of charge at low voltages. Thus, the transistors can be operated at very low potentials and consume very low power. The following table 2.1 gives the capacitance values offered by various dielectrics and the thickness of the capacitors.

Dielectric	Capacitance (μFcm^{-2})	Thickness (nm)	Ref
SiO_2	0.175	100	[36]
Al_2O_3	0.20	33	[33]
Polymer electrolyte with $LiClO_4$	10-200	0.01	[43]

Table 2.1.: Capacitance offered by various dielectrics. Thickness of the dielectrics is also given.

2.2.2. Conductors - metals/non-metals

In conventional electronics, the electrodes (charge carrier emitters and collectors) comprise of heavily doped silicon and the contacts for them are prepared by evaporating metals like gold or aluminium onto them[44]. Metal band structure consists of overlapping valence and conduction bands (Figure 2.5a) and hence consist of a sea of electrons ready for participation in charge transport. The dense packing of the metal crystal structure serves as a passage for the wave-like electron conduction[45]. For thin film electronics, there are well known techniques of metal deposition such as magnetron sputtering, pulsed laser deposition, cluster ion deposition, etc[46, 47]. With regards to solution processing, metal inks are prepared in two ways: nanoparticle dispersion and precursor based solution. Nanoparticle dispersion is prepared by dispersing metal nanopowders of a fixed weight (in mg) in 100 mL of solvent along with a binder to keep the ink stable over longer periods[48]. Once deposited onto a substrate, the film is sintered/cured to eliminate the binder and the left over metal nanoparticles stick together, leading to highly conductive lines. The choice of the binder and the solvent influences the curing temperature while the particle size and the contact between each particle plays a key role in the conductivity of the films. The precursor route on the other hand follows a chemical method to obtain the metallic films. Silver is the most used metal ink[49, 50] due to its high conductivity. There are also materials that are cheaper, more stable and sufficiently conductive and suitable for the passive elements of the electronics such as conductive indium tin oxide (ITO), which is a degenerate n-type semiconductor[51, 52]. The high conductivity of ITO (Figure 2.5b) is due to the formation of degenerate bands in the conduction band due to high level of donor doping that shifts the fermi energy level upwards into the conduction band. In addition to its conductivity, its environmental stability and high transparency[53] due to a large band-gap, makes it an attractive choice for transparent electronics, such as displays.

On the other hand, carbon materials such as graphite and the one atom thick, two-dimensional (2D) crystal, graphene are well known for their application in printed batteries[54, 55] can be used to print the passive elements[56]. Graphene has carbon atoms arranged in a honeycomb lattice in which the carbon atoms have three neighbours each and forms alternating single and double bonds, like in benzene. Undoped graphene (Figure 2.5c is a zero bandgap semiconductor, which is characterised by six double cones with the Fermi level situated at these connection points, called Dirac points[57]. This gives graphene its very high electron mobility, including at room temperature. In spite of acous-

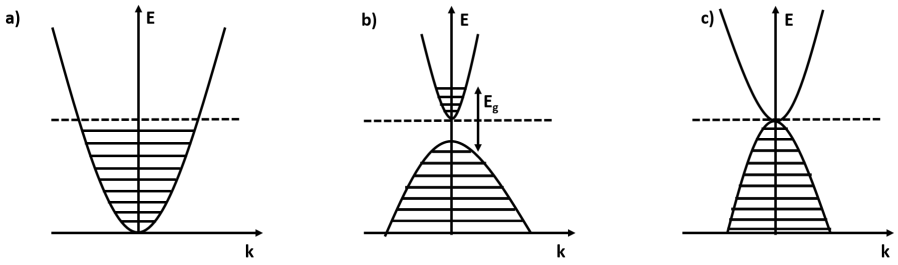

Figure 2.5.: Band Structures (energy vs momentum) of a) metal, b) ITO and c) Graphene. The dotted line represents the Fermi energy. The valence and the conduction band overlap for metals and in ITO, the Fermi level lies beyond the bandgap, E_g, in the conduction band due to doping. In Graphene, there exists six double cones at which the conduction and valence bands touch.

tic phonon scattering in graphene, the mobility values are as high as 200,000 $cm^2(Vs)^{-1}$. Table 2.2 gives a comparison of bulk conductivity of the above discussed conductors.

Conductor	Bandgap (eV)	Resistivity (Ωcm)
Ag	-	10^{-6} - 10^{-8}
ITO	3.5	$7.5x^{-4}$
Graphene	0	10^{-7}

Table 2.2.: Resistivity and Band Gap Values of Different Conductor Materials.

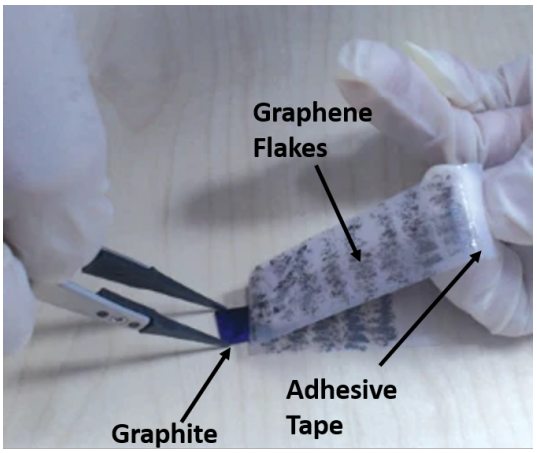

Figure 2.6.: Graphene flake removal using scotch tape method. Adhesive tape is stuck to a graphite piece and pulled repeatedly to obtain single layer graphene flakes. Reproduced from Nature[58]

The production of graphene is very interesting and discussion-worthy. For quite long, graphitic oxide was prepared using Hummer's method[59]. However, it was only after

AK Geim and KS Novoselov, in their Nobel prize winning attempt in 2004, isolated and characterized graphene using a 'scotch-tape method,' that the extraordinary electronic properties of graphene as mentioned above, were discovered[60]. In scotch-tape method, an adhesive tape is stuck to a piece of graphite and quickly removed (Figure 2.6. The adhesive tape is then self stuck and opened repeatedly, to obtain graphene flakes as thin as 5 A°. In order to mass produce graphene flakes, graphitic oxide made from Hummer's method is reduced using chemical or thermal means which are widely used now-a-days. One other method used to produce graphene from graphite is liquid exfoliation[61].

Layering and doping graphene accordingly could lead to ferromagnetic and superconductive properties, respectively. Graphene can be tuned to exhibit ohmic contact with oxide semiconductors[62, 63, 64], the importance of which will be discussed in further sections.

2.2.3. Semiconductors - n-type/p-type

The most important segment of electronic circuits for tunability, is the active component, made from semiconducting materials. In a MOSFET or specifically, EGT, the active material consists of a semiconductor whose resistance can be controlled via electrolyte gating. Semiconductors are defined in two categories: n-type in which, an intrinsic semiconductor is doped with an electron donor and p-type where an intrinsic semiconductor is doped with an electron acceptor. As discussed earlier, while printed organic semiconductors are mostly p-type, the pursuit of high performance n-type semiconductors is one reason for research on oxide materials. For a more fundamental understanding, a look at the band diagram of the intrinsic and n-type doped semiconductor is given in Figure 2.7. An intrinsic semiconductor consists of the same number of electrons in the conduction band (E_C) and holes in the valence band (E_V). The fermi level (E_F) or work function is the energy level at which the probability that states with energy E are occupied is 1/2[65]. For an intrinsic semiconductor, E_F lies almost in the middle of the bandgap, E_G= E_C-$E_V$as seen in Figure 2.7a. The carrier concentration of electrons and holes in the respective energy levels is symmetric. The product of electron and hole concentration is a constant and is given by the law of mass action in Equation 2.4.

$$np = {n_i}^2 \tag{2.4}$$

When the intrinsic semiconductor is doped with an electron donor, the energy level of the donor (E_D) usually lies within E_G, closer to E_C (Figure 2.7b). The fermi level changes and the majority charge carrier (electron) concentration is then calculated from E_F. The law of mass-action is still applicable and therefore, the minority charge carrier (hole) concentration is reduced. P-type doping of an intrinsic semiconductor is carried out in a similar way and the fermi level shifts towards the valence band (Appendix A.1).

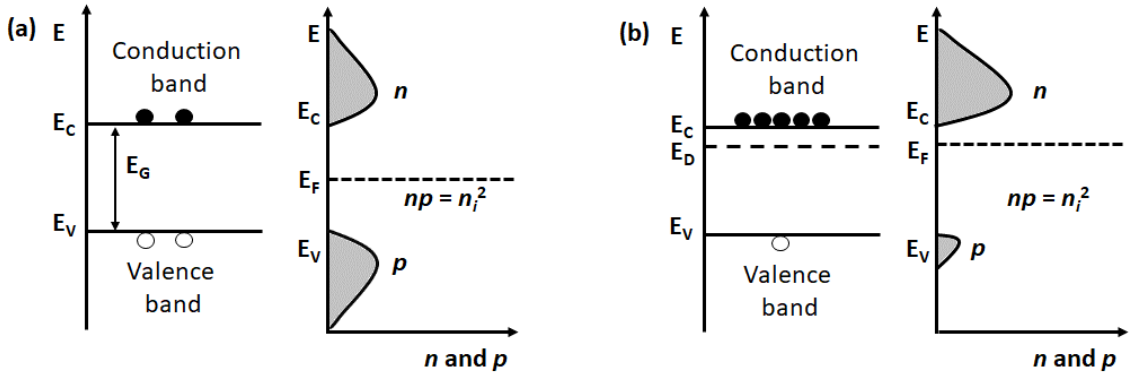

Figure 2.7.: N-type doping of a semiconductor. a) Intrinsic semiconductor has equal number of electrons and holes. The fermi level lies in the middle of the bandgap. b) Addition of electron donor increases the electron concentration and the fermi level shifts towards the conduction band.

The following table 2.3 gives a comparison of intrinsic mobilities offered by some of the n-type semiconductors. Polycrystalline indium oxide has a slight edge over ZnO because of the larger atomic radius for overlap.

Semiconductor	Bandgap (eV)	Electron mobility ($cm^2V^{-1}s^{-1}$)
a:Si	1.7	1
ZnO	3.2	5-50
In_2O_3	3.5	10-50

Table 2.3.: Optical and electrical properties of some n-type semiconductors. Ref [15]

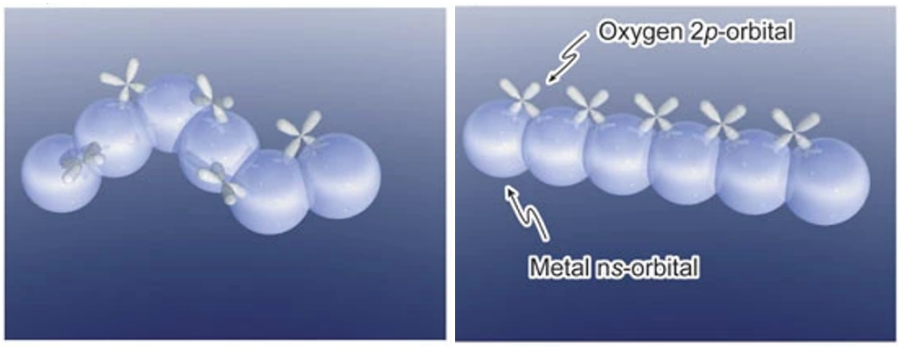

Figure 2.8.: Carrier transport paths in post transition metal oxide semiconductors with a) Amorphous and b) Crystalline structures. The fully occupied oxygen p-orbitals form the VBM and the metal s-orbitals form the CBM. Reproduced with permission from Nature[66]

In the present thesis, a post-transition metal oxide, namely indium oxide (In_2O_3), is chosen as the n-type semiconductor material[67]. The valence band maxima (VBM) is

comprised of the fully occupied $2s^2$ $2p^6$ orbital of the bonded oxygen and the conduction band minima (CBM) is comprised of the empty $5s^0$ orbital of the bonded indium[66]. ns orbitals lose electrons readily compared to (n-1)d orbitals in post-transition metals since fully filled (n-1)d orbitals are favoured. The electron donors in In_2O_3 are the oxygen vacancies that are always formed during the processing of the oxide. The molecular formula would then be In_2O_{3-x}, where x is the amount of oxygen vacancies. These energy level of the oxygen vacancies is situated close to the conduction band and hence, an n-type behaviour of indium oxide arises as seen in Figure 2.7. In the conduction band, since the indium 5s orbitals are large and spherical, they overlap with the adjacent indium 5s orbitals very comfortably (Figure 2.8). Among the post-transition metals, Indium has one of the largest ns orbitals. Metals with larger orbitals exist but however are carcinogenic in nature. The band structures of amorphous and crystalline band structures of metal oxide is illustrated in Figure 2.8a,b respectively. The disorder in the arrangement of the amorphous oxide reduces the charge carrier mobility due to high number of impurities and collision points[68]. In the crystalline oxide, on the other hand, a neatly ordered conduction pathway is formed, leading to high intrinsic mobility (160 $cm^2(Vs)^{-1}$) of the charge carriers[69].

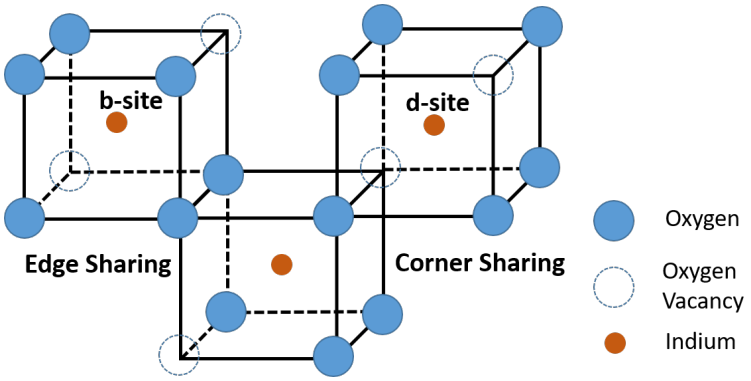

Figure 2.9.: Crystal Structure of indium oxide. Each indium atom is surrounded by six oxygen atoms and two oxygen vacancies, which give rise to electron conduction in the material. The b-sites at the edge shared cubes and d-sites at the corner shared cubes are shown.

Indium oxide crystallises in a cubic bixbyite structure as seen in Figure 2.9. Each indium atom is surrounded by six oxygen atoms and two oxygen vacancy points[70]. These are divided into two types of indium sites: d-site and b-site. Most of the indium atoms lie in the d-sites, which are distorted octahedral vacancy sites, where the edge is shared and the rest lie in the corner shared b-sites, which are triagonally compressed octahedral vacancy sites. Thus, the unit cell of indium oxide comprises of 32 indium atoms (24 in d-sites and 8 in b-sites), surrounded by a total of 48 oxygen atoms. The lattice parameter is about 10 A°. Each oxygen vacancy contributes two extra electrons and hence give rise to the n-type carrier concentration of indium oxide[71]. In solution processed indium oxide, apart from the crystallinity, the morphology of the printed films plays a crucial role in the electron mobility. Defects that arise due to the processing could mostly be negative

for the device characteristics. Notwithstanding, crystalline films of indium oxide can be formed at low temperature through solution processes and therefore can be printed on plastic substrates. During printing, phenomena like coffee-ring formation and crack propagation are most significant for the semiconductor oxide film and can be tackled by changing the ink composition or the surface energy of the substrate. Owing to its high device mobility[23], indium oxide is chosen as the semiconductor in this thesis.

2.3. Transistor Contacts and Architecture

For the smooth functioning of the transistor, interfaces such as the metal-semiconductor and metal-electrolyte are important since they influence the contact and architecture of the transistor. With regards to contacts, ohmic contacts are preferred at metal interface with the semiconductor since rectifying contacts (ex. schottky contacts) could lead to potential losses[72]. Contact resistance of various metals with an oxide semiconductor was found to be in the range of 10-20 kΩ in a thin film transistor[73]. As with electrolyte gating, it is additionally necessary that the metal contacts are chemically inert and maintain a minimal contact area, which could otherwise lead to parasitic capacitance[74]. This calls for a suitable architecture of the transistor, where the contact of the metal with electrolyte is minimal while at the same time maintaining an ohmic contact with the semiconductor. Given below is a glimpse of the interface between graphene passives - oxide semiconductor and graphene passives - electrolyte.

2.3.1. Metal - semiconductor contact

The contact between metal and semiconductor depends on their respective work functions. Metals typically have high work function (ϕ_m) and the conduction and valence bands overlap. χ is the ionisation potential of the semiconductor (conduction band to vacuum), E_{Fm} and E_{Fs} are the fermi levels of metal and semiconductor respectively, while E_C and E_V denote the conduction and valence bands of the semiconductor. When a metal comes in contact with an n-type oxide semiconductor (work function, ϕ_s), electrons are transferred between the semiconductor conduction band and the metal, fermi levels are aligned and the bands bend at the junction[75]. The energy levels of the electrons in the semiconductor either raise or lower, relative to that of the metal. When ϕ_m is greater than ϕ_s, electrons flow from E_C into the metal whereas electron injection from metal to the semiconductor conduction band is obstructed. Such contacts are referred to as 'rectifying contacts.' E_C and E_V lower with respect to the metal and a positive charge due to uncompensated ions develop within the depletion width, W at the junction. The potential barrier height (ϕ_B) for electron injection from ϕ_m to E_C is equal to the difference between the metal work function and the ionization potential of semiconductor, $\phi_m - \chi$ (Figure 2.10a-b).

For electron diffusion from semiconductor into the metal, the minimum potential that is to be applied is the difference between the work functions of metal and semiconductor ($V_0 = \phi_m - \phi_s$). In a printed transistor, electrons are injected from the source to the semiconductor and then eject at the drain. For the transport to be smooth, 'ohmic contacts'

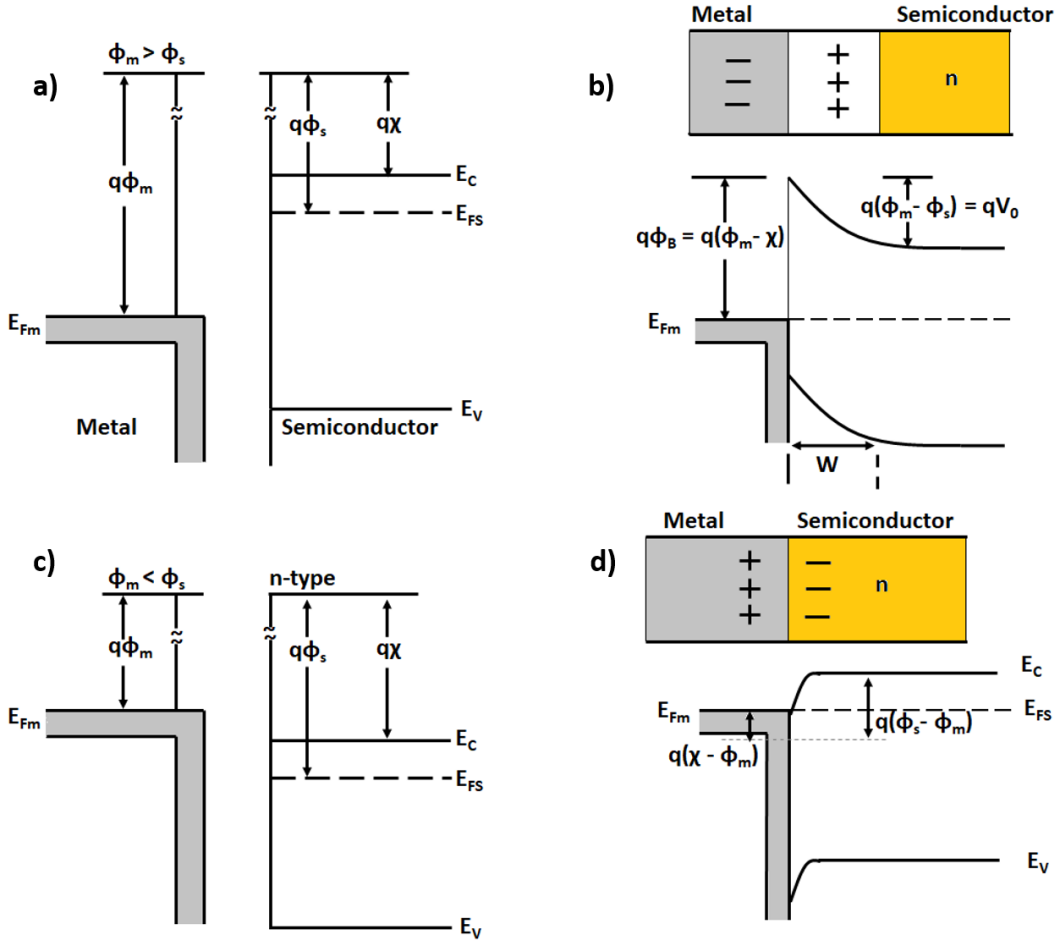

Figure 2.10.: Metal and n-type semiconductor contacts. a-b) Rectifying contact occurs when metal work function is greater than semiconductor. A depletion layer is formed at the junction. c-d) Ohmic contacts arise when the work functions match. No depletion layer would be formed at the junction χ is the semiconductor ionisation potential, ϕ_s its work function, E_C and E_V the conduction and valence bands.

are preferred which means that the work functions of the metal and semiconductor are as close as possible, the fulfillment of which has been the focus of many researchers[76]. In order to keep V_0 as low as possible, the metal work function should be similar or lower than that of the n-type oxide semiconductor. When ϕ_m is lower than ϕ_s (Figure 2.10c-d), ohmic contacts are formed at the metal-semiconductor junction and electrons (majority carriers) are transferred into the n-type semiconductor. There is no depletion layer that is formed. The electron band energies in the n-type semiconductor are raised and even the barrier height is negligible ($\chi - \phi_m$). A smooth injection of electrons from metal into semiconductor due to the negligible barrier height can be realized and a smooth diffusion of electrons from the semiconductor E_C to the metal due to matching work functions is feasible. It should be noted that the required potential can be controlled by the bias at the drain contact. Depending on the bias, the potential difference can be increased or reduced.

A similar situation can be seen in metal and p-type semiconductor contacts and can be seen in appendix A.1

2.3.2. Transistor architecture

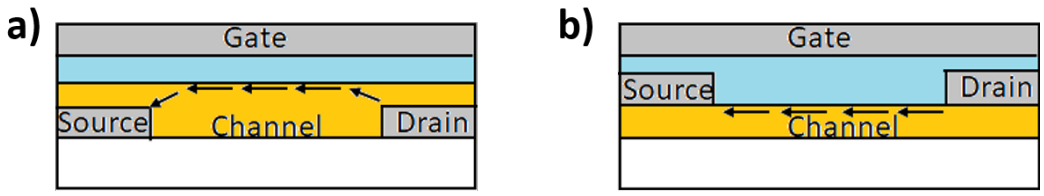

Figure 2.11.: Staggered and coplanar transistor configurations. a) Staggered top-gate. Source and drain have no contact with the electrolyte. b) Coplanar top-gate. Source and drain have contact with the electrolyte (blue). Current flow from drain to source in the semiconductor (yellow) is shown in both cases.

The device architecture and the arrangement of the three components has a big impact on the functioning of the EGT. When printing EGTs with a top-gate, two arrangements exist: staggered and coplanar[77]. Staggered means that the source and drain contacts are separated from the electrolyte by the semiconductor (Figure 2.11a). Coplanar on the other hand is one where the source and drain contacts are in between the semiconductor and electrolyte (Figure 2.11b). Each configuration has distinct advantages and disadvantages. Staggered configuration is used when electrodes are fabricated in the conventional lithography methods as the morphology of the electrodes is much smoother compared to the printed semiconductor. In this configuration, the source and drain have no contact with the electrolyte and therefore the parasitic capacitance (capacitance between electrodes due to electrolyte contact) is nullified. However, the space charge resistance between the source-drain contacts and the channel at the semiconductor-electrolyte interface contributes to the contact resistance. In coplanar configuration, the source-drain contacts are exposed to the electrolyte and therefore contribute towards parasitic capacitance. However, the contact resistance at the metal-semiconductor is greatly reduced since the source-drain contacts are in direct contact with the channel. It results in the contacts being 'gated,' which makes the contact resistances extremely negligible in an EGT that has coplanar configuration[78]. Hence, coplanar devices are the chosen option as far as this thesis is concerned.

2.4. Transistor Operation

An EGT is a replication of the metal oxide semiconductor field effect transistor (MOSFET). A brief introduction to a MOSFET and its application into further electronic components is explained in the following section. MOSFET is a three terminal device that consists of a semiconductor film, the conductivity of which is controlled by a gate electrode that is

separated by a gate insulator. The tuned resistance of the semiconductor can be mapped between the source and the drain electrodes separated by the length, L of the semiconductor (W being the width). A schematic of the thin film transistor is shown in Figure 2.12a. V_G (same notation as V_{GS} in this thesis) , V_D (V_{DS}) and V_S are the terminal potentials at the gate, drain and source respectively. The source terminal is typically grounded and is the charge (electron) injector whereas the drain is the charge extractor. I_D, I_G and I_S are the currents at each terminal and add up to zero, according to the Kirchoff's current law.

2.4.1. Current - voltage characteristics

The MOSFET (or EGT in this case) characteristics follow the assumptions that the metal-insulator-semiconductor (MIS) capacitor portion is ideal, with no interfacial charge traps whereas the semiconductor is uniformly doped and the electric field due to the double layer (transverse field) is much more prominent than the field in the plane of source and drain (longitudinal). This assumption is called gradual-channel approximation and the mobility of charge carriers in the channel is constant. Another condition to be followed is that only the drift currents are considered and diffusion currents neglected. With these set conditions, the current along the channel is continuous and constant and is valid after the applied gate potential has overcome the threshold voltage (V_{Th}). In the ideal scenario, no interfacial traps exist. However in reality, there do exist localized traps at the interface and residual deep traps in the bulk of the semiconductor. Work function difference at every interface plays a crucial role in increasing the threshold voltage. It is possible that the V_{Th} is subjected to unstable shifts with time and is very relevant to EGT functioning. The potential along the channel is a function of the distance x until the length, L. The corresponding charge density, Q(x) accumulated at a position x in the semiconductor surface due to a gate potential ($V_G > V_{Th}$) is given by Equation 2.5, where C_{DL} is the double layer capacitance at the semiconductor.

$$Q(x) = C_{DL}(V_G - V_{Th} - V(x)) \tag{2.5}$$

Knowing the drift velocity, $v_d = \mu.E(x)$ and the current density, $J(x) = Q(x).v_d$
Current along the length of the channel is,

$$I_D(x) = W\mu Q(x)E(x) \tag{2.6}$$

Substituting 2.5 in 2.6 and $E(x) = \frac{dV(x)}{dx}$, we get

$$I_D(x)dx = W\mu C_{DL}(V_G - V_{Th} - V(x)dV(x)) \tag{2.7}$$

Integrating from x=0 to x=L, the drain current in the gradual-channel scenario is,

$$I_D = \frac{W\mu C_{DL}}{L}[(V_G - V_{Th})V_D - \frac{{V_D}^2}{2}] \tag{2.8}$$

A close look at Equation 2.8 and the Figure 2.12 gives us the scenario at every step of V_D. A channel is formed in the semiconductor at $V_G > V_{Th}$ and the charge carrier concentration between source and drain is constant and uniform. At low drain potentials, ($V_D \ll V_G$), the

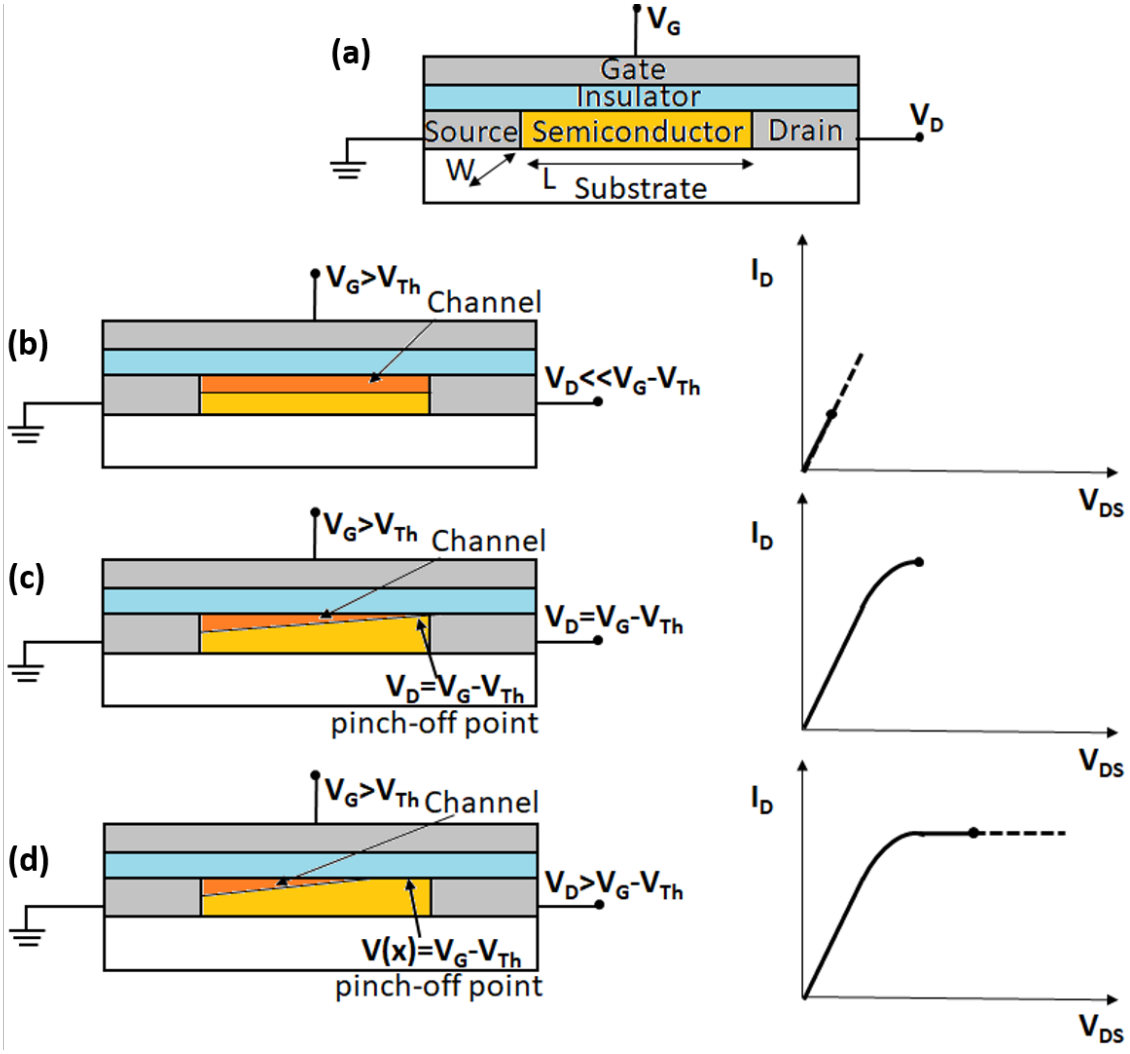

Figure 2.12.: Channel formation in MOSFET in a gradual-channel approximation. Channel is formed when V_G is greater than V_{Th}. a) When V_D is much lesser than V_G-V_{Th}, the channel acts as an ohmic resistor. b) When V_D is equal to V_G-V_{Th}, the channel gets pinched off at the drain due to opposing potential V_D. c) Channel shortens as a result of increasing V(x) and current saturates.

voltage increases linearly from source to the drain and as a result, the I_D also increases. Mathematically, one can see that $\frac{V_D{}^2}{2}$ in Equation 2.8 is negligible and the linear relation can be given by the Equation 2.9.

$$I_{D,lin} = \frac{W\mu C_{DL}}{L}[(V_G - V_{Th})V_D] \tag{2.9}$$

This known as the linear regime (Figure 2.12b). As V_D is increased to V_G-V_{Th}, the current no longer increases due to an obstruction arising as a result of the V(x) induced depletion layer. The channel is said to be "pinched-off" at this point (Figure 2.12c). Beyond this point (V_D>V_G-V_{Th}), as the obstructing V(x) increases, the only current that flows

through to the drain is the space-charge current offered by the semiconductor. It can be seen in Figure 2.12d that the channel length starts reducing as a result of widening of the depletion region in which no charge carriers exist. This is imaged in the i-v characteristics by a saturation in the drain current, I_D and the current here can be represented by the Equation 2.10.

$$I_{D,sat} = \frac{W\mu C_{DL}}{L}[\frac{(V_G - V_{Th})^2}{2}] \tag{2.10}$$

2.4.2. Transistor performance and key parameters

When a potential is applied to a transistor to turn it on, it is called an enhancement device and if the applied potential is to turn off the transistor, it is called a depletion device[65]. As an example, the characteristics of an n-type electrolyte gated transistor (NEGT) are shown are given in Figure 2.13. The characteristics for a p-type electrolyte gated transistor (PEGT) mirror the NEGT characteristics. While measuring the current-voltage characteristics of a transistor, certain key parameters need to be noted.

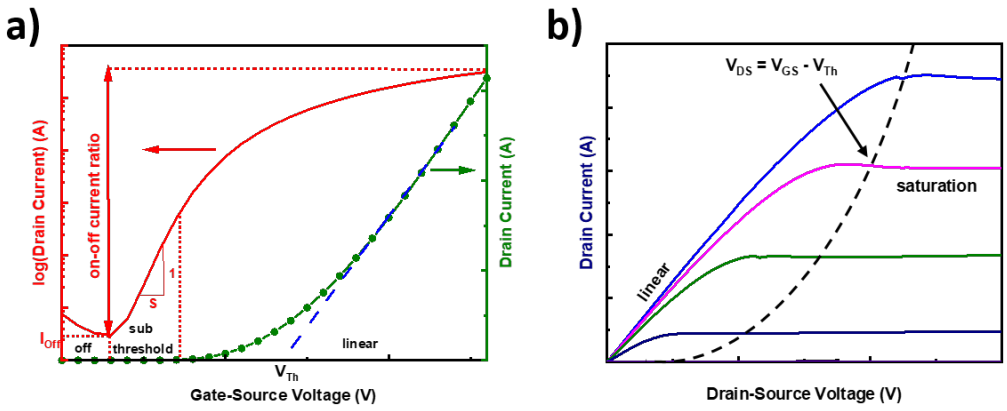

Figure 2.13.: Characteristics of EGT. a) Transfer curve in linear regime gives information about on-off ratio and subthreshold slope. b) I-V curve gives the locus of pinch-off points as seen.

On-off ratio

On-off ratio ($\frac{I_{on}}{I_{off}}$) for an n-type transistor is defined as the ratio of the current when the transistor is in 'on-state' beyond the threshold voltage and in 'off-state' below the threshold voltage and is important to build complicated circuits. Especially in digital circuits, high on-off current ratio is preferred for a clear distinction between the 0 and 1 states rendering it extremely useful for storage. It depends on the threshold voltage and the subthreshold swing, in that the value of the threshold voltage determines where the off-current occurs and the value of the subthreshold swing determines the rate at which the on-current is reached.

Threshold Voltage

The threshold voltage of a MOSFET depends on factors such as the charge carrier traps in the semiconductor, which can be found at the grain boundaries and other defect sites including the surface and interfaces[79]. For an n-type transistor, the position of threshold voltage determines whether the channel is formed or not at zero gate bias. Accurate tuning of threshold voltage is useful to construct electronic circuits. Generally, the threshold voltage is calculated in the linear regime (V_{DS}«V_{GS}-V_{Th}) by extrapolating to the x-axis as seen in Figure 2.13a.

Subthreshold Slope

The subthreshold slope indicates the steepness of the drain current rise with gate bias. This is important for low voltage applications such as switches for digital logic and memory applications. The region immediately after the off-current is the subthreshold region in which the diffusion currents in the semiconductor are greater than the drift currents. This of course occurs below the threshold voltage, when the drift currents begin to dominate and its value therefore depends on the density of interfacial charge traps. I_D in the subthreshold region varies exponentially with V_G and the slope of the curve is called subthreshold slope. The inverse of this slope is called the subthreshold swing and is given by the Equation 2.11. In other terms, in the logarithmic scale of the transfer curve, the subthreshold slope gives the information on the amount of potential required to increase the output current by one decade of drain current ($mVdec^{-1}$). The i-v curves as seen in the previous pages give the locus of the pinch-off points (Figure 2.13b) for different sets of gate voltages. The threshold voltage (V_{Th}) of the NEGT is positive, meaning that an application of gate voltage is necessary to overcome the impurities and deep charge traps and set up a channel for the conducting charges. In the transfer characteristics, it is measured as a direct extrapolation of the linear curve to the x-axis (Figure 2.13a), when V_D is much lower than V_G-V_{Th}.

In general, the subthreshold swing is designated by the following equation arising from the transconductance value.

$$S = \frac{\partial V_G}{\partial(log_{10} I_D)}$$

As mentioned earlier, the subthreshold swing is proportional to the capacitance offered by the interface-trap density (C_{IT}) for the electrolyte. This dependence is seen in the following equation.

$$S = (ln10)(\frac{K_B T}{q})\frac{C_{DL} + C_{IT}}{C_{DL}} \tag{2.11}$$

The subthreshold slope can also be used to estimate the interface charge trap density. Closer the S value is to the theoretical limit, lesser are the trapped charges.

Hysteresis

In a fully printed EGT system, variations that are more prominent than conventionally fabricated electronics are reflected in form of hysteresis between the forward and reverse

scan of gate-source voltage. Injection of charges into the traps at various interfaces and humidity affects are among the identified reasons for the advancing of hysteresis over time[80]. This reflects on the subthreshold swing as well.

In general, in thin film oxide transistors, hysteresis occurs in two ways: clockwise and counter clockwise that leads to rising and lowering of threshold voltage respectively[81]. Clockwise hysteresis is observed due to the trapping of electrons at the shallow energy defects at the semiconductor-electrolyte interface. Higher electrical field is required to overcome the charge trap occupancy and to obtain the same channel carrier density. This results in a larger threshold voltage in the reverse gate voltage scan. Counter clockwise hysteresis on the other hand, could be caused by the huge electric field due to the already present charges at the double-layer interface leading to a negative shift in the threshold voltage.

Mobility

A defining parameter for transistor performance is its mobility. Higher device mobility allows for faster device performance. This is the reason behind chosing a polycrystalline oxide semiconductor and especially indium oxide, which has large metal-ns orbitals in the conduction band exhibits high intrinsic mobility. Intrinsic mobility is the inherent mobility of a semiconductor consists which in turn defines the device mobility of the EGT, which in the best case scenario is equal to the intrinsic mobility. In general, the device mobility in fully printed EGT is influenced by a number of factors such as the printing, processing, morphology of semiconductor, contact resistance and parasitic capacitance. To calculate the mobility from the transistor characteristic curves, the transconductance, $\frac{\partial I_D}{\partial V_G}$ can be used in the linear region (Equation 2.9) or $\frac{\partial \sqrt{I_D}}{\partial V_G}$ can be utilized in the saturation regime (Equation 2.10).
Thus, the mobility in saturated regime ($V_D > V_G - V_{Th}$) can be calculated as,

$$\mu_{sat} = \frac{2L}{WC}\left(\frac{\partial \sqrt{I_D}}{\partial V_G}\right)^2$$

whereas in the linear regime ($V_D \ll V_G - V_{Th}$), the constant mobility can be obtained using the Equation 2.12 and is used in the thesis.

$$\mu_{lin} = \frac{L}{WCV_D}\left(\frac{\partial I_D}{\partial V_G}\right) \tag{2.12}$$

Notice that both μ_{sat} and μ_{linear} are independent of the gate voltage.

Switching Speed of EGT

A high value of mobility (μ) is a necessary but not sufficient condition to ensure high frequency performance of the fully printed EGT. For a fully printed EGT, the channel length, the contact resistance and the length (thickness) of the electrical insulator (printed electrolyte) are all defined and limited by the printing resolution[82]. While a low drive

voltage (V_{DS}) makes the EGT compatible with printed batteries and other avoids unwanted faradaic currents, this limits the operation frequency for a channel length L, as per Equation 2.13.

$$f_T = \frac{\mu V_{DS}}{2\pi L(L + \Delta L)} \tag{2.13}$$

F_T is the limiting frequency of a transistor, known as cut-off frequency. This equation is valid for contact resistance corrected mobility so as to obtain a frequency that results in an unity current gain.

Since fully printed EGT has another limiting factor arising from the ionic conductivity of the electrolyte, the thickness of the electrolyte becomes an important parameter. The resistance of the electrolyte is thickness dependent and the cut-off frequency ($f_{T,el}$) for such an RC circuit is therefore given by

$$f_{T,el} = \frac{1}{2\pi R_{el} C_{DL}} \tag{2.14}$$

where R_{el} and C_{DL} are the electrolyte resistance and the double-layer capacitance respectively.

2.4.3. Transistor - resistor logic

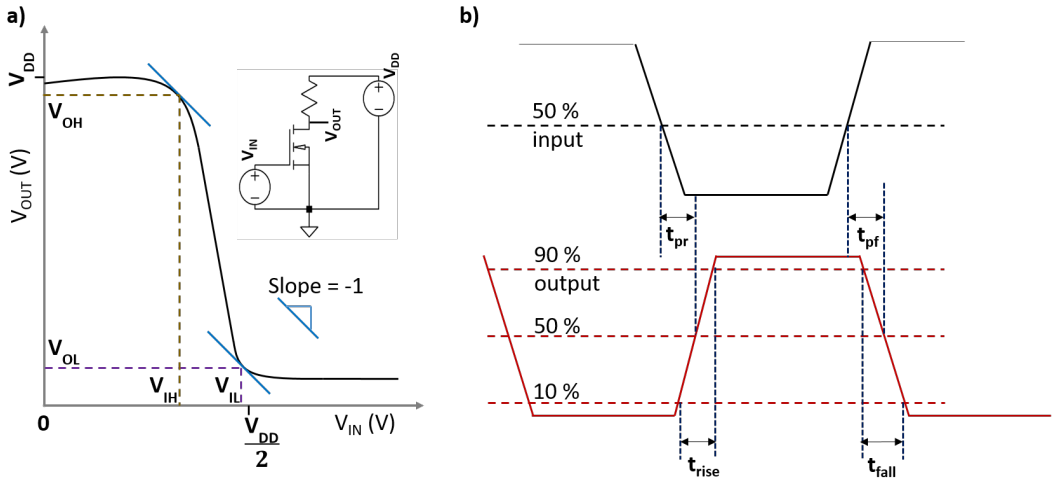

Figure 2.14.: Characteristics of a TRL inverter. a) DC characteristics. The output remains high until about the input of $\frac{V_{DD}}{2}$ after which it drops to zero. At a slope of -1, the noise margins can be calculated. b) Transient analysis. The propagation delay and the rise, fall times are marked

The transistor is a basic electronic component, which makes up logics such as a NOR, NAND, XOR gates, which further make up many complicated electronic circuits[83]. To make the first tests for the applicability of transistor in complex circuits, the next basic

building block, that is an inverter is relevant. This is because most logic gates can be accomplished with resistors, transistors and inverters as building blocks. Inverters can be fabricated using a transistor-transistor logic (TTL) in which, an n-type and a p-type transistor are connected to each other, to achieve high output potentials at low input potential and vice versa. Another route in which inverters can be manufactured, is by connecting an n-type transistor to a resistor to make a transistor-resistor logic (TRL), as shown in Figure 2.14a. The schematic in the inset shows a TRL, in which the input (V_{IN}) is given at the gate terminal of the transistor. The source is grounded and the drain is connected to a resistor load which is maintained at a constant drive voltage, V_{DD}. The output voltage (V_{OUT}) is measured at the drain terminal. Since the V_{Th} of the transistor is positive, the gate input voltage at low potentials is not enough to form the channel in the semiconductor. Therefore, the inverter output is dictated by the drive voltage at the load. Until the transistor fully switches on, the inverter output continues to be equal to V_{DD}. Once the transistor is switched on and the channel becomes fully conducting, the source and drain terminals are at the same potential and therefore, the output voltage drops to zero. This typically occurs around an input of $\frac{V_{DD}}{2}$.

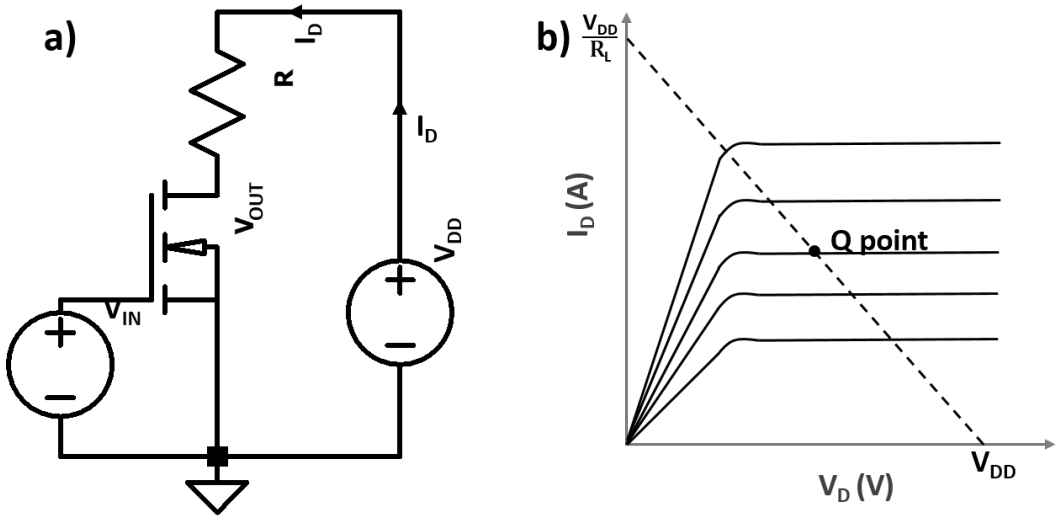

Figure 2.15.: Loadline analysis on EGT. a) Kirchoff voltage law is applied on the transistor-resistor loop to give a linear equation. b) The straight line is defined by R_L to identify the operation Q-point.

At negative 1 slope, the output and input voltages corresponding to the high values (V_{OH} and V_{IH}) and to the low values (V_{OL} and V_{IL}) become important in noise margin estimation. High noise margins are more immune to noise as compared to low margins. However, noise margins can sometimes be exchanged for higher switching speeds. Figure 2.14b shows the transient characteristics of the inverter. The curve on the top is the input and below is the output curve whose values are almost reversed with respect to the input. The time required for the reversal is known as the propagation delay (t_p) and is calculated as the average of the difference between 50% of the input and output during the rise and fall of the output, respectively. The rise (t_{rise}) and fall (t_{fall}) times are calculated as the

difference between the 90% and 10% of the output potential.

$$V_D = V_{DD} - I_D R_L \tag{2.15}$$

The inverter parameters *vis-a-vis*, the iv characteristics of the transistor and the load resistance (R) define the operating point of the TRL inverter. Applying the Kirchoff voltage law in clockwise direction on the transistor-resistor loop in Figure 2.15a, the loadline Equation 2.15 can be obtained. The straight line in Figure 2.15b is defined by the load resistance (R_L) and the middle of the straight line is denoted as the operation point. It is evident that lower the R_L, higher is the Q-point. The value of the R_L is carefully chosen after the loadline analysis.
To fully print the transistors and inverters on flexible substrates, just understanding the interfacial behaviour between different components of a transistor or the architecture would not suffice. The suitability of the substrate with regards to printing, thermal compatibility and mechanical flexibility needs to be understood as well. This is detailed in the following section.

2.5. Substrates

A valid question that arises in printed electronics is about the adhesion of the processed inks, especially the oxide film to the substrate. The answer lies in surface energies. Much like the conventional deposition techniques, oxide and metallic films attach well to most of the substrates, due to the van der waals forces acting at atomic distances between the film and the substrate. Naturally, the macroscopic properties such as roughness and the surface energy of the substrate plays a vital role during film deposition by printing[84]. Depending on the solvent used for the ink, the film formation varies on the surface of the substrate due to energy differences. During the drying of the film, the interfacial forces sometimes lead to the formation of a coffee-ring[85]. The coffee-ring forms when the printed film is pinned to the substrate and the solvent lost by evaporation at the edge of the film is replaced by solvent that is pulled from the center. The pulled solvent also carries the solute with it, which is deposited in a ring at the edge of the film. The wetting property of the substrate, along with the solvent used in ink preparation is relevant in this case.

2.5.1. Substrate - film interface

While most coating processes exhibit thicknesses as satisfied by the so-called Landau-Levich equation, the thickness of films by drop on demand (DOD) techniques typically are affected by the coffee-ring effect which is influenced by the contact angle. The surface energy of the substrate and the ensuing van der waal force based wetting properties affects the contact angle of the printed drops. A fixed contact angle, known as contact angle pinning generally leads to 'coffee-ring effect'[86] due to the flow of particles towards the film edges. On the other hand, a weak contact angle hysteresis which is the difference

between the advancing and receding contact angles, leads to a Marangoni flow, which counters the coffee-ring effect.

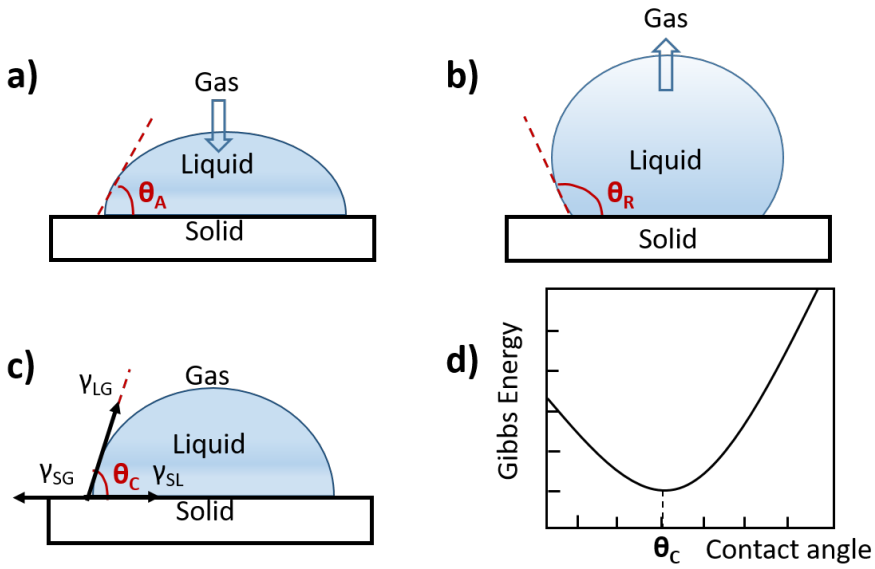

Figure 2.16.: Contact angle of printed drop on substrate. a) The contact angle is advancing as ink spreads on the substrate b) The contact angle is receding, if the drop coalesces c) The contact angle is pinned when the drop is stable on the substrate d) Gibbs free energy as a function of contact angle. An energy minimum is seen when contact angle is pinned.

Contact angle is derived from the simple young's equation. At the interface where solid, liquid and gas phases co-exist, called as the 'three phase contact line,' the forces acting are the interfacial tension of the substrate with the liquid (γ_{SL}) and gas (γ_{SG}), and the surface tension at the liquid-gas interface (γ_{LG})[87]. When a drop of liquid spreads on the solid, the contact angle (θ_A) is said to be advancing (Figure 2.16a), whereas for a drop that is coalescing, the contact angle (θ_R) is receding (Figure 2.16b). At the equilibrium point (Figure 2.16c), the contact angle ((θ_C)) is said to be pinned. The equilibrium forces at this pinned contact line are satisfied by Equation (2.16).

$$\gamma_{SG} = \gamma_{SL} + \gamma_{LG} cos\theta_C \tag{2.16}$$

Contact angle hysteresis is given by the difference between the advancing and receding contact angles, $\theta_A - \theta_R$ and the contact angle pinning occurs when the printed drop is stable and the gibbs energy is minimum. As seen in Figure 2.16d, the energy of the drop on the solid substrate initially reduces until the contact angle pinning. Depending on the surface energy of the substrate, the drop that exhibits weaker wetting has higher energy than the one that has strong wetting.

2.5.2. Coefficient of thermal expansion

In order that the printed solution forms oxide film, certain activation energy should be applied and typically this is provided in form of temperature. The physical and mechanical properties of the substrate are affected by changes in the surrounding temperature and this further influences the morphology of the oxide film. For example, when the coefficient of thermal expansion (α) of the substrate is higher than that of the film, the chances of crack formation in the film are high (α of indium oxide is 8 x 10^{-6} / °C)[88]. A table of α for different substrates is given in table 2.4.

Substrate	Coefficient of thermal expansion (α) (x 10^{-6} / °C)	Ref
Silicon	2.6	[89]
Glass	4	[90]
Polyimide	30-60	[91]
PET	20-80	[92]

Table 2.4.: Thermal Expansion Coefficients of Various Materials

Generally, polycrystalline oxide films form at temperatures greater than 100 °C. As seen in table 2.4, silicon and glass have low thermal expansion coefficient and are stable even at about 450 °C. However, silicon and glass are rigid and to achieve bendable/wearable electronics, it is necessary to use flexible substrates such as polyimide (PI), polyethylene terephthalate (PET) or polyethylene naphthalate (PEN). Therefore, processing of the printed films need to comply with the temperature requirements of even the substrates with the lowest temperature withstanding capability such as PET/PEN. Several other methods exist, in order to process the oxide films from precursors on PET/PEN, such as laser curing and photonic curing. For photonic curing, the absorption spectrum of the wavelength for the precursor is the key factor since transparent substrates do not absorb most of the visible spectrum.
PET/PEN are the most utilised in terms of packaging. So printing electronics on such substrates would go off well with practical applications such as transparent displays, smart packaging and labeling. This, along with the ease of printing and cheap availability are the reasons for extensive research towards making electronics on PET.

2.5.3. Mechanical Properties

The primary objective of printing on plastic substrates is the mechanical flexibility of plastic substrates. The bending of the substrate undeniably impacts the printed film as well. When a substrate is bent, three kinds of deformation zones arise on the substrate (Figure 2.17)[93].

Zone A is typically the undeformed zone and is therefore unaffected by the bending. Zone B is the fatigue damaged zone and is under an uneven strain during bending. The central zone C is under a constant strain and is also not subjected to any fatigue. Therefore zone B becomes the most critical one in terms of strain fatigue. Neutral axis is where the elongation forces are compensated by compression forces and lies near the interface

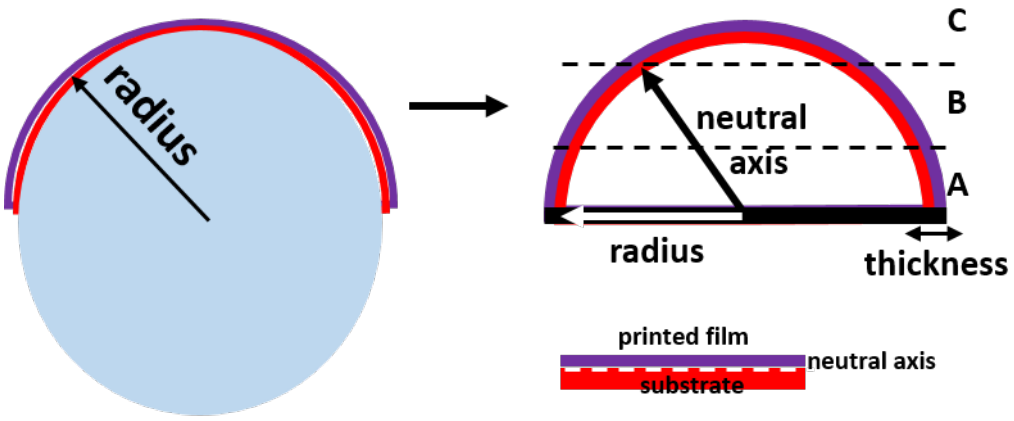

Figure 2.17.: Various strain zones on a bent substrate. Zone B is subjected to the maximum strain compared to C and A. The interface between the printed film and flexible substrate is the neutral axis.

of the printed film and substrate. Even though the thickness of the oxide film is few orders lesser than the substrate, the neutral axis is still dictated by the bending of the oxide film. The radius to the neutral axis is used to calculate the tensile strain that the oxide film can withstand. Naturally, the radius of bending has an inverse effect on the withstand-able strain. Smaller bending radius implies higher bending and hence higher tensile strength. Much akin to bending, tensile strength of the oxide layer can be studied in terms of stretching as well. By stretching, the possibility of the oxide layer not falling in a fatigue damaged zone is eliminated and the perfect adhesion of oxide to the substrate can be figured.

3. State of the Art

Using the above given understanding of the components and performance of a transistor, fully printed electrolyte gated transistors (EGTs) are prepared. High device mobility values are achieved using inkjet printed polycrystalline indium oxide[94, 95, 96]. However, the bigger challenge is to print the passive elements and replace the conventional epitaxial film deposition methods.
The emergence of graphene transistors[97, 98] spiked the research interest on inkjet printed graphene transistors[99, 100]. However, considering that the conductivity of graphene is high and the conductivity tuning is as well performed at high currents, it is possible to use graphene as printed resistors and conductors. Until a while ago, resistors based on graphene oxide ink were fabricated die to the unavailability of printable graphene inks. In this regard, Kim et al[101] demonstrated that graphene can be used as stretchable and transparent electrodes. The films have an average roughness of 15 nm along 100 μm width and controlled thickness (90 nm) are printed with highly reproducible resistance values. Ye et al constructed a graphene EGT and were able to assess more precisely, the high carrier density of single and multilayered graphene[102]. Later, Secor et al[61] were able to successfully synthesise printable inks as mentioned above, by dispersing graphene in ethylcellulose containing cyclohexanone. For the inkjet printed graphene, they obtained a resistance of 4 mΩ.cm following annealing temperatures as low as 250 °C. The average roughness of the printed graphene lines was much lower (2 nm). In later years, the mechanical and environmental robustness of the graphene inks have been improved by replacing EC with nitrocellulose[103]. Nitrocellulose residue offers better covalent bonding as compared to EC residue and hence provides higher conductivity (40,000 S/m). Cellulose being a plant derivative makes the graphene ink environmentally friendly.

As a comparison, a table with a list of individual printed components and the key identification parameters is given in 3.1.

3.1. Fully Printed Transistors

With regards to fully printed transistors or inverters, there are decent number of reports when it comes to organic semiconductors. For example, Song et al have printed graphene passive electrodes using a flexible cytop/Si mould to achieve resolutions as low as 30 μm. On these P3HT EGTs fabricated on PET, they were able to observe mobilities of 0.3 $cm^2V^{-1}s^{-1}$[108]. Hyun et al have also demonstrated the working of P3HT EGTs on PET using Cu-plated printed Ag films as source and drain, whereas graphene was printed as gate. They observed slightly higher mobility of 0.48 $cm^2V^{-1}s^{-1}$[109]. Seo et al were also able to demonstrate solution processed transistors on flexible polyethylene naphthalate

Printed Component	Ink Material	Printing Technique	Identification Parameter (units)	Value	Reference
Insulator	HfO_2	Spin Casting	Dielectric Constant	8.1	[33]
	$LiClO_4$ in DMSO, PVA	Ink-jet Printing	Ionic Conductivity	10^{-3}-10^{-4}	[104]
	Ion Gel in DMSO, PVA	Ink-jet Printing	(Scm^{-1})	10^{-2}-10^{-3}	[105]
Conductor	Ag nanoparticle	Aerosol-jet Printing	Resistivity	10^{-3}-10^{-4}	[48]
	ITO nanoparticle	Ink-jet Printing		10^{0}-10^{-1}	[106]
	P3-SWNT	Microplotting	(Ωm)	10^{1}-10^{0}	[30]
Semiconductor	ZnO		Intrinsic Mobility	200	
(inorganic n-type)	In_2O_3	Ink-jet Printing		160	[107]
	IZO		($cm^2V^{-1}s^{-1}$)	40	[69]

Table 3.1.: Examples of Printed Individual Electronic Components

(PEN) substrate[110]. However, to date, there are negligible reports that fully printed oxide EGTs on plastic substrates. Sharma et al have printed amorphous indium gallium zinc oxide (IGZO) EGTs[111]. In this work, conductive ITO films and semiconducting IGZO are processed using a precursor method. IGZO is printed across these ITO electrodes and a device mobility of 6 $cm^2V^{-1}s^{-1}$ is achieved and inverters with a signal gain of 2.5 are shown. The preparation however required high annealing temperatures of 500 °C. This is greater than the glass transition temperatures of most flexible polymers and is restricted to development on only Si wafers. Scheideler et al[112] have demonstrated low temperature (<300 °C) processed oxide transistors from aqueous precursors. Aluminium doped CdO is used as electrodes for InO_x semiconductor which showed contact resistance of 160 Ωcm and a device mobility of 19 $cm^2V^{-1}s^{-1}$. The devices are fabricated on Si wafer but these can potentially be transferred onto a flexible plastic substrate. Nonetheless, toxic cadmium (Cd) metal has been used to contrive the passive elements.
In order to fully print and characterize chemically stable and low temperature processed transistors, the functional inks used in this work are an aqueous precursor for indium oxide, graphene ink and a composite solid polymer electrolyte. The interfaces, surface morphologies, electrochemical and electrical characteristics are studied using techniques described in the following chapter.

4. Materials and Methods

Printable inks are prepared and the ensuing films are characterized for their optical, material, electrical and mechanical properties. The ink preparation, processing and instrumentation used for characterization are illustrated in this chapter.

4.1. Ink Preparation

4.1.1. Indium oxide precursor

In this thesis, precursor inks are prepared for the semiconducting indium oxide (In_2O_3). 0.05 M $In(NO_3)_3.xH_2O$ (99.99%, Sigma Aldrich) salt is dissolved in a solution of 4 parts milli-Q water (18.2 MΩ resistance) and 1 part glycerol. The glycerol addition facilitates better printing and drying of the printed precursor. The solution is translucent at this point. The solution is sonicated in an ultrasonic bath for 20 minutes and left on magnetic stirrer with 300 rpm at room temperature for about 30 minutes until the solution turns fully transparent. The transparent solution is filtered through 0.45 and 0.2 μm polyvinylidene flouride (PVDF, GE Healthcare) filters respectively, to eliminate any possible particulate matter and assist easy inkjet printing. The printed films are annealed at 300-400 °C depending on the substrate, to form indium oxide films. The chemical reactions in the process are possibly as follows.

$$In(NO_3)_3 + H_2O \longrightarrow In(OH)_3 + ... \xrightarrow{\Delta} In_2O_3 + ...$$

For a spin coated film, the substrate is spun at 300 rpm for 30 seconds and then 800 rpm for another 30 seconds.

4.1.2. Composite solid polymer electrolyte

The composite polymer solid electrolyte (CSPE) is prepared by dissolving 1 part lithium perchlorate ($LiClO_4$, 99.99% Sigma Aldrich GmbH) in 9 parts propylene carbonate (OC anhydrous 99.7% Sigma Alrdich GmbH) and stirring for one hour at room temperature. Concurrently, a 1:20 mixture of polyvinyl alcohol (PVA, hydrolyzed 98% Sigma Aldrich GmbH) and dimethyl sulfoxide (DMSO, anhydrous 99.9%, Sigma Aldrich GmbH) is mixed at 85 °C for one hour. Finally, both the solutions are mixed and stirred with 300 rpm overnight at room temperature. This solution is transparent and is filtered through a 0.2 μm polytetraflouroethylene (PTFE, Pall Inc.) filter. Figure 4.1 shows the chemical formula and structure of the ingredients used to make the CSPE.

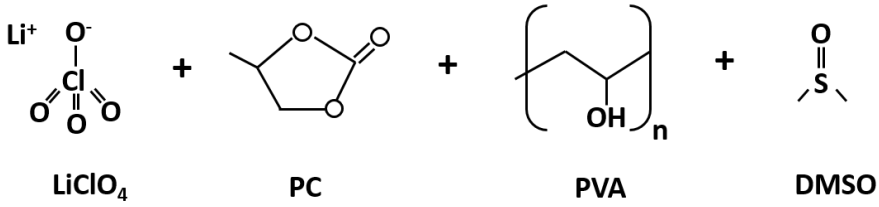

Figure 4.1.: Components of the CSPE. From left to right: lithium perchlorate, propylene carbonate, polyvinyl alcohol and dimethyl sulfoxide

4.1.3. Graphite slurry

Ethylcellulose (EC) and ethanol mixture is used to exfoliate and suspend graphene flakes (Figure 4.2a-d). EC matches with the surface energy of graphene and is suitable solvent for exfoliation. Since the resulting EC-stabilised graphene flakes are hydrophobic in nature, these are suspended first, in a 85/15 cyclohexanone/terpineol mixture, after being washed in a brine water-ethanol mixture. This also helps in controlling the viscosity of the ink, as well as to keep the flakes from coagulation. These inks are highly stable and show conductivity as high as some metal thin films and can be cured at much lower temperatures (250 °C) than ITO precursor inks. Graphene inks can be digitally printed and are very uniform.

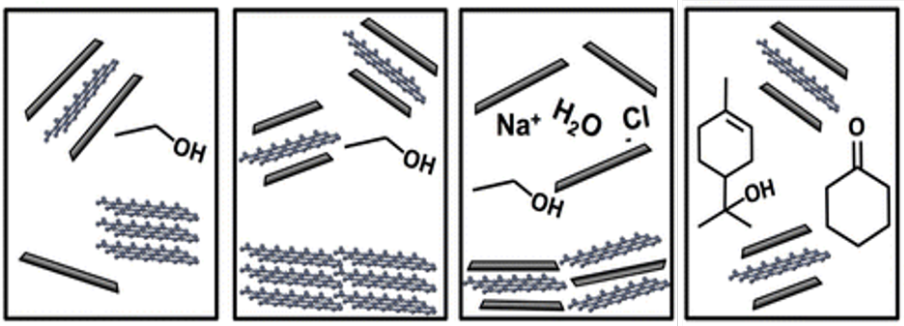

Figure 4.2.: Graphene ink prepared by liquid exfoliation. a) Graphite powder is ultrasonicated in ethanol/EC mixture b) Bulk and big graphite sheets are sedimented by centrifugation followed by c) flocculation of graphene/EC in brine solution d) Ink is prepared by dispersing the graphene-EC in 85/15 cyclohexanone/terpineol. Reprinted with permission from ACS[61], 2013.

Two kinds of graphite inks are prepared. One is a commercial ink with graphene flakes (Graphene ink, Merck) of size less than or equal to 3 μm. A 2.4 wt.% of solid graphene and ethyl cellulose is dispersed in cyclohexanone/terpineol solvent. The curing conditions for the ink is 250-350 °C for 20 to 30 minutes. Following this, the printed films are conductive. Similarly, a home made graphite slurry is prepared by dispersing a 94 wt.% of graphite in milliQ water and a separate dispersion of 6 wt.% PVA in milliQ water, stirred with 300 rpm at 80 °C for an hour. stirring overnight at . This ink is conductive at room temperature.

4.2. Material and Optical Characterization

4.2.1. X-ray diffractometry

In this work, x-ray diffraction (XRD) is used o identify the crystal structure of the printed oxide films. When monochromatic high energy electrons bombards copper atom, certain characteristic x-rays are emitted. The high energy electrons knock out electrons from K shell (the first shell in the atom with highest probability of finding an electron) such that the knocked out electron reaches higher shells (such as L). They then fall back from L to K shell and give rise to the characteristic x-rays[113]. These x-rays reflect when incident on the planes of a crystal. The reflected rays from the first two planes have a path difference which is an integral (n=1,2,3...) multiple of the incident wavelength and therefore the rays interfere constructively. This is given by the Bragg's equation, 4.1 where d_{hkl} is the interplanar distance, θ_{hkl} the incident angle and λ the characteristic wavelength (1.54 A°).

$$n\lambda = 2d_{hkl}sin\theta_{hkl} \tag{4.1}$$

Each reflecting plane is indexed by the miller indices *h,k,l* of the corresponding reciprocal lattice. This can be used to identify the crystal system of the sample. X-ray diffraction is a safe characterization method for the sample and does not destroy it. The crystal structure, grain size, interatomic distances and lattice parameters of the sample can be found from the technique. The utilized x-ray diffractometer is the model Philips Cu-xrd. Other material characterization include fourier transform infrared (FTIR) spectroscopy in which energies ranging from 4000 to 400 cm^{-1} are supplied to study the atomic bonds based on change in dipole moment.

4.2.2. Scanning electron microscopy

Scanning electron microscopy (SEM) is used for investigating the morphology and the interface between the printed films. As mentioned in the previous section, when a monochromatic high energy (5-20 kV) electron beam is incident on a material, the beam can be transmitted, reflected or absorbed. The reflected electrons can be characteristic or continuous x-rays, auger, cathodoluminescence. Other electrons that are reflected and very useful for imaging are secondary and back-scattered electrons (Figure4.3) which are generated as a result of inelastic (ionization) and elastic scattering respectively. The incident beam being made up of electrons, can be focused using electromagnetic lenses. The intensity of these secondary species is simultaneously mapped to generate a high spatial resolution image of the sample. Since the wavelength of the electron beam is atleast two orders lesser than light, this resolution is extremely high and can be as small as few nanometers.
SEM can be used to image all kinds of printed films. Since electron beam would charge an insulating material, insulating or sometimes semiconducting films are coated by a thin layer of gold or carbon, to avoid charging. Conducting films therefore do not require any further coatings. A Leo1530, Zeiss Jena model has been utilized.

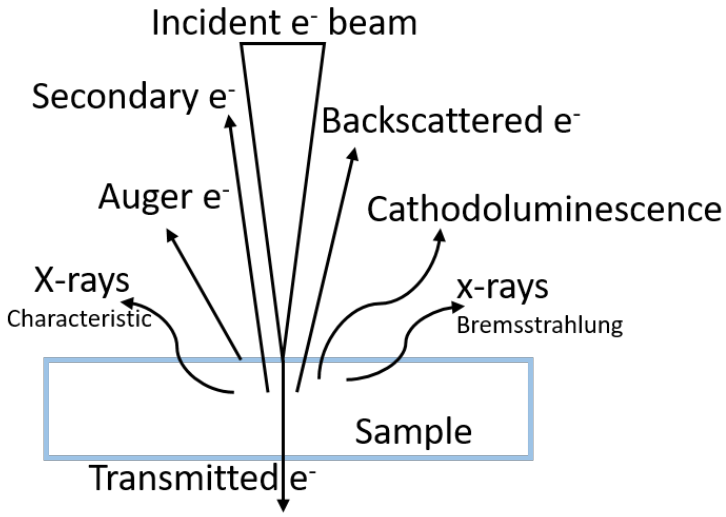

Figure 4.3.: Scenario on a sample on which an electron beam is incident. Electrons can be transmitted,absorbed or reflected. The different types of electron emission are shown

Optical microscope

A Leica M165 C microscope is used to capture optical images of the printed devices. The magnification is set to 10x and ImageJ software used to process the pictures.

Sessile Goniometer

A sessile-drop goniometer (DSA-30, KRÜSS) is used to measure the contact angle on substrates. A syringe places a drop of the ink on top of the substrate, which is studied with a transversely placed camera. The contact angle is calculated by applying young-laplace formulae.

4.2.3. Atomic force microscopy

Atomic force microscopy (AFM) maps the surface of printed films using a cantilever with a very sharp tip made of silicon or silicon nitride. There are three modes of measurement, contact, non-contact and tapping, out of which tapping mode is utilized in this thesis. Tapping mode utilizes the concept of resonant frequency changes as a result of cantilever deformation. The thickness and width of the tip of the cantilever are negligible compared to the length of the cantilever. The resonant frequency of the cantilever is determined and this changes as it interacts with the surface of the film. The capillary tip can be traversed along a desired area on the surface on the film and this is how the surface height is determined. The forces acting on the capillary tip are therefore in three dimensions mostly (normal and lateral) and are determined by the Hooke's law[114]. The interaction of the tip with the film surface leads to a deformation of the cantilever according to Hooke's law. This can be identified by the change in the resonant frequency and hence it is important

to know the deformation stiffness in different directions. AFM can be used to map the surface of any kind of film surface - conducting, insulating, soft and hard. A Bruker AFM has been used.

Surface profilometer

A Dektak 32 profilometer is used to probe the thickness of the printed films. It consists of a diamond tip of 12.5 μm radius for probing and has a resolution of 50 - 50,000 nm while probing the height of the films.

4.3. Electrical Characterization

4.3.1. Van der pauw method

In order to precisely measure the sheet resistance of a film, van der Pauw method is used[115]. This is a type of four-point resistance measurement suitable for thin films because of the high aspect ratio. Van der Pauw measurements are done on films that are dense and typically square shaped. Square shapes cancel out the length/width part of the resistance and the remainder is the sheet resistance of the film, which is only dependent on the film thickness. Therefore the units are given as $\Omega/\square$ for the sheet resistance. Van der Pauw method employs four probes at four corners of the film, in contrast to the linear four-point resistance measurement. Thus, the average resistivity of the film from four edges can be measured[116].

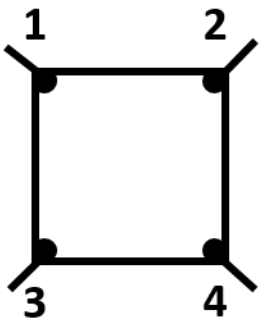

Figure 4.4.: Van der Pauw method to determine four-point resistance on a square shaped thin film

In Figure 4.4, the resistance at the edge where a potential, V_{34} is applied and a current in the opposite edge I_{12} is observed is,

$$R_{12,34} = \frac{V_{34}}{I_{12}}$$

Since the thin film is square shaped, the resistance is identical on all the edges and thus an average of resistance (R_{avg}) from each edge can be applied to the van der Pauw formula,

$$exp(-\frac{\pi R_{\text{avg}}}{R_{\text{vp}}}) = -\ln 2$$

which gives the van der pauw resistance, 4.2

$$R_{\text{vp}} = \frac{\pi R_{\text{avg}}}{\ln 2} \tag{4.2}$$

4.3.2. Cyclic voltammetry

Cyclic voltammetry (CV) as is evident from the name is an electrochemical analysis method in which a DC input potential is applied across the electrodes at a certain scan rate and the output current measured[117]. A three electrode system with a reference, counter and working electrodes can be used or a two electrode system with a working and reference/counter electrode can also be used in cyclic voltammetry. Multiple cycles of current vs voltage can be performed from which the thermodynamics and kinematics due to chemical response at the electrode-electrolyte interface can be interpreted. When diffusion kinematics due to electrochemical reactions occur at the electrode, bumps due to redox reactions are observed for the output current. In Figure 4.5a, for a given scan rate, as the input voltage is increased (forward scan), the initial capacitive flat current from A increases linearly due to the faradaic currents from the analyte until B, where the electrode potential is half ($E_{1/2}$). At this point, the kinetics of electron transfer are such that the concentration of reducing reactants and oxidizing products is in equilibrium and the Nernst equation[118] is satisfied. The anodic peak current ($i_{p,a}$) at C is the maximum oxidation current[119], where the current increased due to increasing potential is balanced by the decreasing flux of analyte from the electrode surface, where the electric double layer is formed (Figure 2.3). Beyond C, the concentration gradient of analyte between the bulk of solution and electrode interface limits the current, the Nernst equation is not followed and hence the current reduces until D. From D through G, the process that occurs at the cathode is a mirror image of the oxidation process with a cathodic peak current ($i_{p,c}$) at the peak cathodic potential.

$$Q = CV$$

for a constant C,

$$i = \frac{dQ}{dt} = C\frac{dV}{dt} \tag{4.3}$$

In the case of a linear capacitor with a constant capacitance C, the equation2.3 is satisfied. In this case, the redox reactions seen in Figure 4.5a arising as a result of electrochemistry are not seen. Instead, the current(charge flow per unit time) is proportional to the scan rate of the potential as seen in 4.3. Therefore, for a particular scan rate, even with an increase in applied potential, the output current stays constant. In the reverse direction the same scan rate is now negative and the current simply reverses polarity, but remains constant. Thus, the rectangular shape seen in Figure 4.5b fits well for the cyclic voltammetry of a

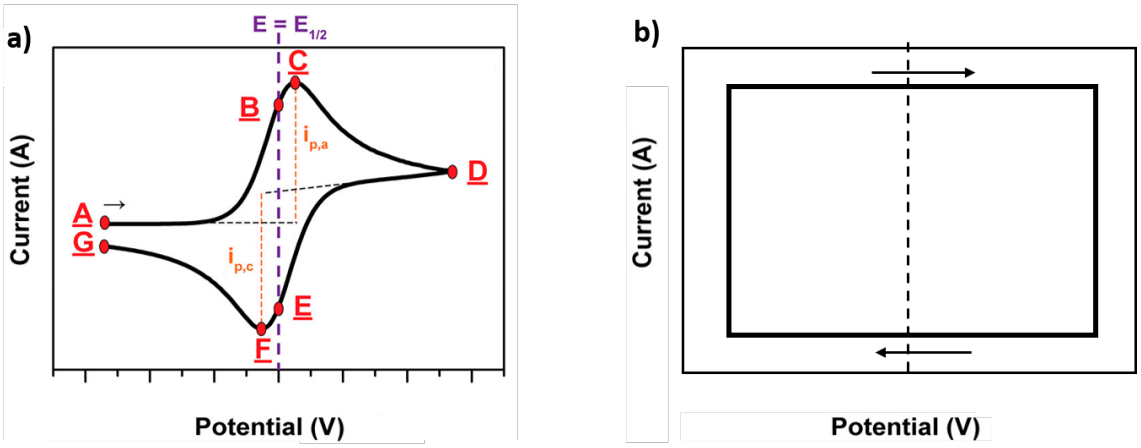

Figure 4.5.: a) Duck shaped CV curve. As potential is increased, after A , an onset potential leads to exponential increase in current until C ian oxidation peak is observed. From C to D, the neutral

parallel plate capacitor with two metallic plates. The conductivity of the plates would naturally play a role in the voltammetric scan and this is utilized in an electrolyte gated transistor.

4.3.3. Electrochemical impedance spectroscopy

Electrochemical Impedance Spectroscopy (EIS) is used to find the resistance offered by all the components of a circuit[120]. It is measured by applying a sinusoidal potential to the circuit system and measuring the observed output current. In the context of this thesis, two relevant electrical components are a resistor and capacitor. The impedance offered by a resistor is its resistance (R) which is a real value and the impedance offered by a capacitor is the imaginary $\frac{1}{jwC}$ where w is the signal frequency and C is the capacitance. In a circuit comprising of a resistor and a capacitor in parallel, which is the scenario at an electric double layer, the total impedance (Z) becomes 4.4, which means that only the imaginary part is frequency dependent.

$$\frac{1}{Z} = \frac{1}{R} + jwC$$

$$= \frac{1 + jwcR}{R}$$

which gives,

$$Z = \frac{R}{1 + w^2C^2R^2} - j\frac{wcR^2}{1 + w^2C^2R^2} \tag{4.4}$$

In an electrolyte-gated transistor, the simplest equivalent circuit consists of the electrolyte resistance in series with the double layer capacitance, with a parallel resistance to it, commonly referred to as a 'Randle circuit'[118]. The so called Nyquist plot, which is the map of the imaginary impedance (from capacitor) vs the real impedance (from resistor) at

a given frequency is a semicircle for this circuit (Figure 4.6). The semicircle begins from high frequency, when current flows through the capacitor to low frequency, when the current flows through the parallel resistor. This circuit is important since the capacitor and the parallel resistor are analogous to the double-layer capacitance that is seen in EGTs.

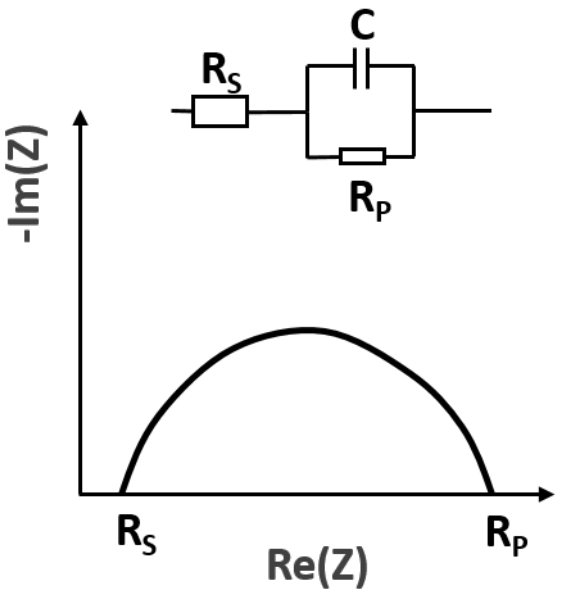

Figure 4.6.: Representation of a nyquist plot. x-axis is the real part of the circuit impedance and y-axis is the imaginary part. Inset shows a Randle circuit. The curve varies with the choice of the circuit.

Capacitance can be calculated from the real and imaginary parts of the impedance using the equation4.5[82],

$$C = \frac{-ImZ}{w|ReZ|^2} \tag{4.5}$$

The double-layer capacitance is not a perfect capacitor and acts as a constant phase element as in, kinematics arising from chemical ractions and the resulting diffusion kicks in and this phenomena is described with a 'Warburg element.' Even though the nyquist plot is a consequence of frequency dependence of the impedance, it is not explicitly seen in the plot. In this regard, a Bode plot is more relevant since the impedance magnitude and phase angles are plotted as a function of frequency. Thus, the frequency values are known in Bode plot. All this makes EIS a very useful tool to study the double-layer capacitance and the ensuing chemical reactions at the electrode-electrolyte interface. A Biologic SP-150 is utilized to make both cyclic voltammetry and electrical impedance spectroscopy studies.

4.3.4. Probe station

Electrical measurements such as two-point resistance, van der pauw resistance, transistor characteristics and electrochemical studies on the device are measured at ambient conditions and a 50% humidity using a precision probe station (SÜSS MicroTec MLC-150C),

and performed with a precision semiconductor analyzer (Agilent 4156C). The devices are contacted with a source measure unit (SMU) which, as the name suggests, can both source voltage and measure current at the same time. During measurement, the rise time, measure time and the wait time are changeable and are set in accordance to the speed of the active device.

4.4. Processing and Flexibility

4.4.1. Photonic curing

Methods other than heating the precursor exist, in order to produce the oxide films. One of them is photonic curing, in which high energy photonic pulses are flashed onto the printed film to attain the high temperatures required for curing of the oxide film. Photonic curing is an ultrafast transient process, requiring only milliseconds for curing oxide films with morphology and performance comparable to thermally annealed films. Since the process is based on surface heating due to photonic absorption, it is a safe method for oxide film formation on flexible substrates that appear in daily life, such as PET/PEN and even paper. Therefore it can be assumed that this method is ideal for utilization in roll-to-roll processes and the materials are invented accordingly.
Photonic curing, as the name suggests, consists of a set of capacitors that are charged to a high potential so as to discharge high energy pulses through a xenon lamp. This allows the lamp to illuminate the sample with high energy light flashes that have a spectral range of 200-1100 nm. The short processing time assists immediate curing and at speeds of about 1.6 ms^{-1} in a wide web format. In this work, a Novacentrix PulseForge1200 have been utilized for photonic curing[121]. The exposure level ranges from 0.01 Jcm^{-2} to 20 Jcm^{-2}. The broadcast nature of the light source allows uniform curing of area as large as 112 cm^2 in a single flash.

4.4.2. Mechanical flexibility

The influence of stretching on the oxide film is studied to evaluate the performance of the flexible devices printed on Dupont Kapton® and PET. The substrate is clamped on either edge of the long side and stretched to observe the mechanical strain that the oxide film can withstand. The setup is manufactured by CK Trading Co., South Korea (CK-770FET).

Part III.

Results

5. Fully Printed Electrolyte-Gated Transistors

Printing passive structures includes the printing of the source, drain, and the gate electrodes of a transistor. With regard to conductivity, metal electrodes would be the preferred choice. Recently, studies about a certain compatibility between silver and oxide semiconductor have been published. However, silver and other similar metals are not compatible with the electrolyte due to the ensuing undesirable chemical reactions during operation that facilitate metal migration. Therefore, instead of metals, chemically stable graphene ink is printed.

As discussed in section 5.2.1, the work function difference between the metal and semiconductor has a big impact on whether the contacts are ohmic or rectifying. In graphene, any residual organic compounds can drastically vary the work function or contribute to a rectifying contact by creating electrical traps and impurities at the interface. This will be focused in the present chapter, along with the device architecture. The design of the device architecture plays another important role in device functioning as seen in section 5.2.2. The choice of either a staggered or a coplanar structure can be decided by some factors such as printability of each component. For this, the roughness of the films and sometimes the drying phenomena play crucial role and find focus in this chapter. Once the material and the device architecture are set, the EGT characteristics, the calculation of key parameters and the subsequent improvement of the device performance are explained.

5.1. Fabrication and Basic Characterization

5.1.1. Printing procedure

Towards fabrication of electric circuits on flexible substrates, the first step is to develop a procedure for a fully printed transistor, including all its active and passive components. The precursor solution, the polymer electrolyte, and PEDOT:PSS are printed with a Dimatix 2831 inkjet printer. While printing the semiconductor, the drop spacing is set to 25 μm at a 3.5 in. water meniscus, and the stage is heated to 60 °C; the piezoelectric voltage is 40 V. The necessary steps to construct an all-printed EGT with graphene electrodes are illustrated in Figure 5.1. First, the indium oxide precursor ink is ink-jet printed on glass substrate and heated to 400 °C in 2 h and annealed at the same temperature for an additional 2 h. Afterwards, the graphene electrodes are printed partially on top of the semiconductor using a Sonoplot microplotter and processed

at 250 °C for 30 min. The capillaries required for microplotting the graphene ink are precision made to have the required tip diameter (3-5 μm). For the electrolyte, the drop spacing is fixed at 55 μm, and the stage is heated to 40 °C; the voltage given is 40 V. The electrolyte dried within few minutes of printing. As the top gate, several layers of electrolyte (thickness 5 μm) are printed and dried before printing PEDOT:PSS on top of it. The PEDOT:PSS was dried at room temperature. The gate-channel distance is limited to 50 μm in the in-plane devices, whereas in the top-gated geometry the gate-channel distance is determined by the thickness of the electrolyte.

High resolutions are enabled using ink-jet printing and precursor films are printed in tens of micrometers dimensions. Graphene on the other hand is microplotted since the graphene flakes coagulate the ink-jet printer nozzle. Microplotter as well enables resolutions of choice.

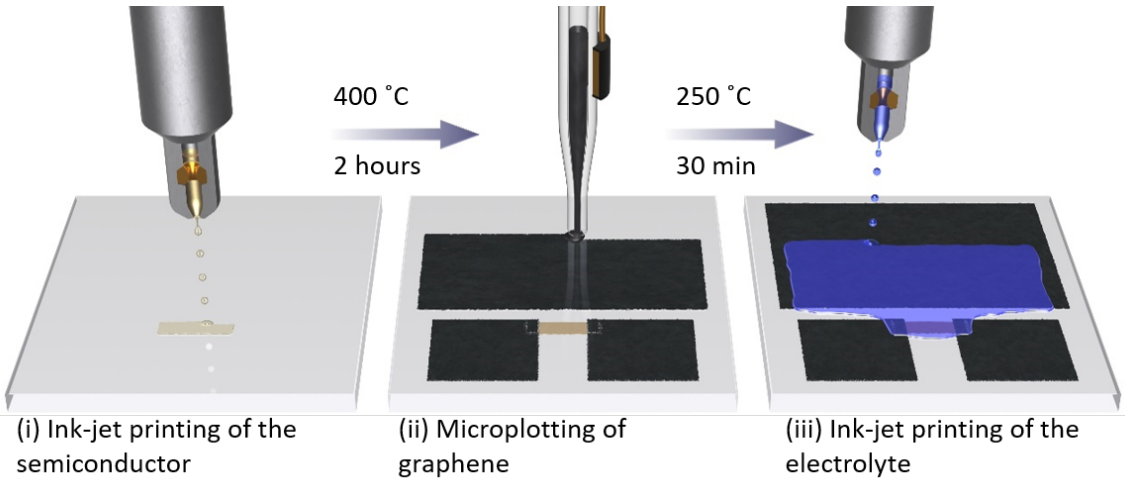

Figure 5.1.: Schematic of Fabrication of Fully Printed EGT. Semiconductor precursor is first ink-jet printed on a glass substrate. Graphene electrodes are then microplotted in a staggered setting. CSPE is ink-jet printed across the semiconductor and most of the gate electrode. The thickness of each layer is controlled by the number of printing steps.

A side view schematic of the printed device during operation is provided along with the electrical characterization in upcoming subsections 5.3.

5.1.2. Material characterization

Thickness of the printed layers influences the carrier mobility in them. Films that are very thin are not packed densely enough result in poor particle contacts and films that are very thick generally lead to interaction of layers that give rise to physical defects such as cracks in the film. In both cases, the mobility of charge carriers is adversely affected. Printing of two layers of the precursor, followed by the annealing step to form the oxide showed that the particles are packed close to each other as seen in the sem micrograph (Figure 5.2 a), with negligible roughness. While some pores are noticed, the negative contributions from

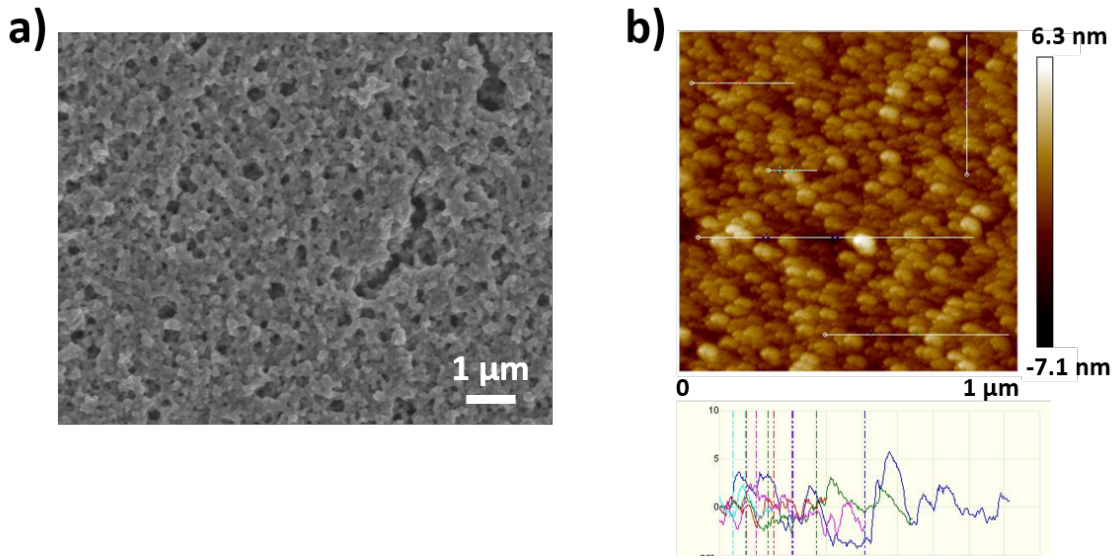

Figure 5.2.: SEM and AFM micrographs of printed indium oxide film. a) SEM micrograph shows an average particle size of about 100 nm. The close packing of the particles make up a dense oxide film. b) AFM micrograph averaged over many directions on the film show the dense packing of the oxide film, with a very smooth morphology. Roughness is only few nms. The graph below denotes the surface roughness profile.

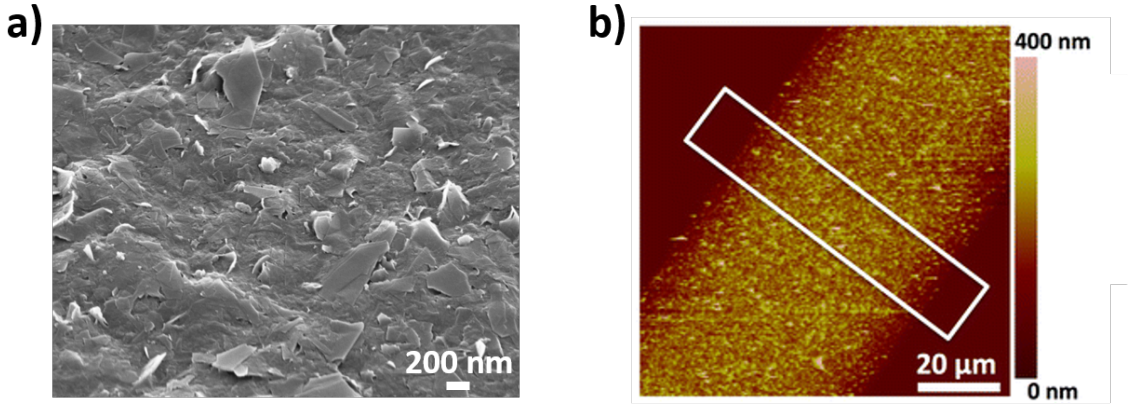

Figure 5.3.: a) SEM micrograph of graphene films show flake size variation from 200 nm to 2 μm. The dense packing assists in high conductivity of the films. b) AFM micrograph shows the typical roughness of the graphene film to be around 400 nm. The high roughness is from the flake size variation.

these pores are negligible. The conductivity of the oxide film measured by the van der pauw method is also in the expected range for a semiconductor. In the afm micrograph in Figure 5.2 b, the roughness range is from -7.1 nm to 6.3 nm, which is a result of few pores but mostly flat morphology. The average roughness is about 4 nm. The average thickness of the film is 150 nm. The film thickness and electrical conductivity measurements are shown in the appendix (A.2). Similarly, the graphene film morphology is observed. The graphene flakes are held together by bonding with the ethyl cellulose present in the ink. SEM micrograph studies reveal the flake size variation from 200 nm to 2 microns (Figure 5.3 a). As seen in Figure 5.3 b, AFM studies revealed the roughness to be few hundred nanometers. Typical thickness of the printed graphene films is about 300 nm and is shown in the appendix (A.3). The annealing conditions for indium oxide formation are based on the activation energy, crystallization temperature and solvent conditions[69]. For the graphene ink, the annealing conditions are motivated by the solvent conditions and the polymer binder present in the ink. To obtain significantly low resistance in order to make the electrodes, the polymer binder in graphene ink has to be burnt away.

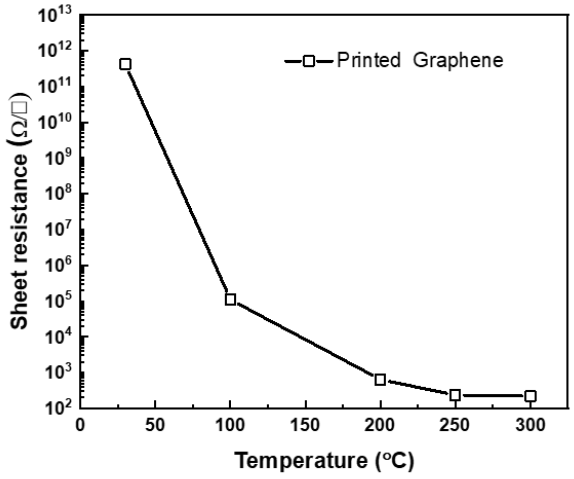

Figure 5.4.: Resistance of graphene films shows sharp fall from room temperature to 100 °C to 200 °C and saturates after 250 °C.

The variation of graphene resistance with annealing temperature is calculated using van der pauw method (section 4.3.1) and is illustrated in Figure 5.4. The resistance of the as-printed film is in the order of 10^{12} Ω/□, making it an insulator at room temperature. The resistance drops drastically by seven orders when the film is heated to 100 °C and a further two orders to 10^3 when heated to 200 °C. The resistance value when the film is heated to 200°C is 640 Ω/□ and the conductivity is 7,500 S/m. As discussed in 2.5, the choice of the substrate decides the processing temperature and hence films heated at 200 °C are considered despite this low conductivity. However, at this temperature, organic residues which are a consequence of the unburnt solvents and binders in graphene ink could lead to rectifying contacts with the indium oxide semiconductor. A further increase in temperature to 250 °C led to a reduction of resistance to 220 Ω/□ where the value

saturates even when heated to 300 °C, giving rise to a conductivity value of 22,000 S/m. The resistance reduced as the organic residues burnt away and at the same time, it is observed that ethyl cellulose binder at this temperature actually assists in conductivity by forming $\pi - \pi$ bonds with graphene flakes[61]. This adds to the mechanical stability of the film, when utilized on flexible substrates.

The removal of the binders with temperature are explained using fourier transform infra-red (FTIR) studies performed on graphene heated from room temperature until 250 °C (appendix A.5). The functional group presence in the film and the disappearance of the solvents with heating can be clearly seen. The elimination of solvents such as terpineol and cyclohexanone is observed with the reduction of signal at 3000 cm^{-1}. The signal at 1087 cm^{-1} also reduces significantly indicating a reduction of C-O functional groups. The FTIR spectrum for the film heated at 250 °C matches well with pristine graphene[122]. A peak appears at 3600 cm^{-1} and is an indication of the adsorption of -OH groups by ethyl cellulose which is susceptible to hydroxyl group adsorption. The ethyl cellulose as mentioned earlier assists in conduction by forming $\pi - \pi$ bonds with graphene flakes.

The composite solid polymer electrolyte (CSPE) is the third component and has been proved to possess an ionic conductivity of 10^{-2} Scm^{-1} in temperature ranging from -35 °C to 60 °C[104].

5.2. Interface Studies

The interfaces between graphene-indium oxide and graphene-CSPE are studied to check for a suitable device architecture and chemical stability. Since there is an outright difference in the roughness of indium oxide and graphene, the construction of the device relies on the order of printing each component.

5.2.1. Graphene - indium oxide

Conventional vapour deposited electrodes are smooth and it is easier to print the precursor on top of the electrodes. However, in the printed regime, the graphene film roughness as seen in section 5.1.2 is few orders more than the indium oxide film roughness. Indium oxide in this case cannot be printed on top of graphene film. As seen in Figure 5.5 a, when precursor is deposited and processed on top of printed graphene, the film peeled off as seen at the left electrode. This is clearly due to the difference in roughness of both the films in addition to some leftover organic residues in graphene film that evaporate in the process.

Also, the graphene electrodes 'moved away' from the indium oxide. This could arise from the fact that graphene has a negative coefficient of thermal expansion[123] and shrinks and forms wrinkles as a result. This causes a movement away and the consequence is a poor electrical contact between indium oxide and graphene. The extreme differences in the thermal expansion lead to cracks in indium oxide film. To solve this, indium oxide

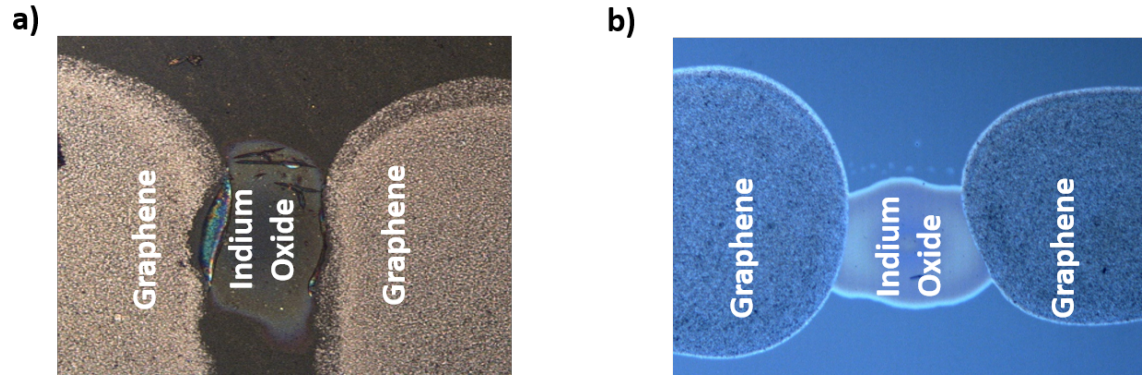

Figure 5.5.: Device architecture is dependent on processing conditions. a) Coplanar structure leads to peeling out of graphene flakes. b) Staggered structure shows a smooth interface between indium oxide and graphene printed on top. Graphene film is printed on the very smooth indium oxide films.

precursor is printed in the first step, as seen in Figure 5.1 and heated to obtain indium oxide film. When the graphene is later printed on top of indium oxide, the thermal expansion difference does not adversely effect the device structure as seen in Figure 5.5 b. Since this is a coplanar structure 2.3.1, it facilitates a much reduced contact resistance but could contribute towards unwanted parasitic capacitance when the transistor is built.

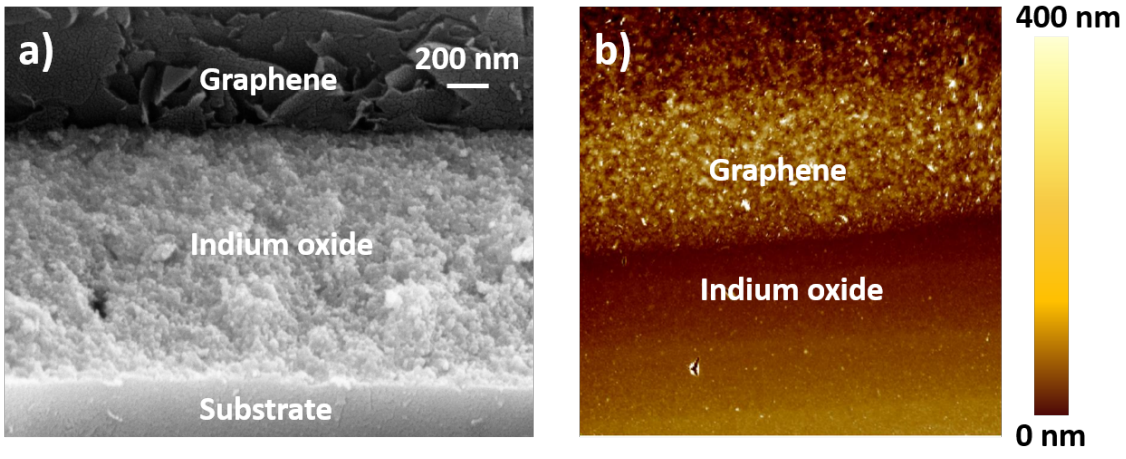

Figure 5.6.: SEM and AFM micrographs of the graphene-indium oxide interface. a) Cross-sectional SEM micrograph taken after the printing of graphene layer reveals a continuous interface between graphene on top of indium oxide. b) AFM micrograph reveals the stark difference between the roughness of graphene and indium oxide.

After the graphene is printed, the interface and the difference in the roughness are observed using SEM and AFM microscopy respectively. As seen in Figure 5.6 a, the interface between the indium oxide and the graphene on one side and glass substrate on the other side is realized using a cross-sectional sem micrograph. Especially the continuous interface

between graphene and indium oxide is very advantageous for the electrical behaviour. The afm micrograph in Figure 5.6 b shows the huge difference in the roughness. In fact, the indium oxide roughness is negligible as compared to the graphene at the interface. This aides easy deposition and processing of graphene on top of indium oxide. This justifies the idea for coplanar structure.

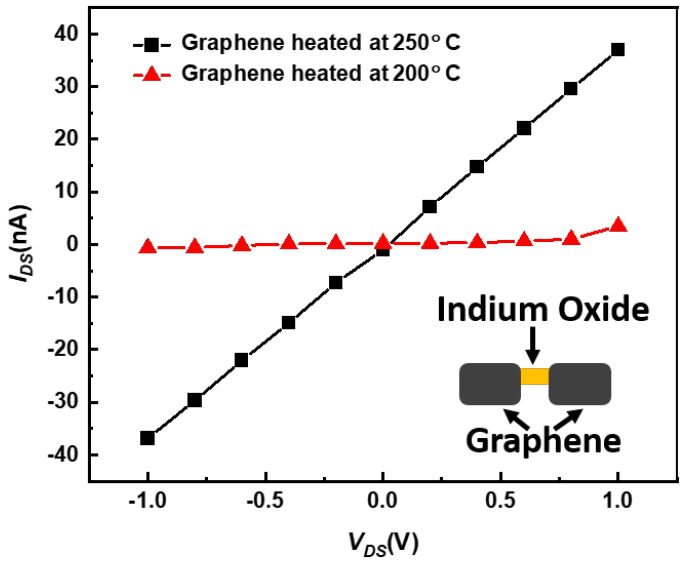

Figure 5.7.: Current-voltage characteristics of graphene-indium oxide contacts. Even though graphene sheet resistance is of the same order when heated to 200 °or 250 °C, residual organic components give rise to schottky contacts for 200 °C heated graphene. Ohmic contacts were achieved with 250 °C heated graphene.

That one may be able to print oxide devices on PET/PEN substrates in the future, both graphene and indium oxide should be processed at most at 200 °C. Graphene heated at 200 °C has resistance in the range of a conductor but as discussed earlier, unwanted organic residues are present in the film. The C-O functional groups are still significantly present in the film, even at the interface. This obstructs the charge carrier mobility between graphene and indium oxide and is reflected as negligible currents in Figure 5.7, indicating rectifying or schottky contacts in the two-point current-voltage characteristics. This hints at the role of organic residues in work function of the printed graphene or the cause for rectifying contacts. Therefore, either vacuum heating or further increase in processing temperature to 250 °C had to be applied to obtain ohmic contacts. The difference in the output currents in both the cases is quite evident in Figure 5.7 which shows occurrence of ohmic contact between indium oxide and graphene when graphene is heated 250 °C. It has to be noted that the indium oxide semiconductor is printed and processed before printing graphene in accordance to the roughness factor. Therefore, a coplanar architecture is chosen to suit roughness of indium oxide and graphene. The annealing

temperatures of indium oxide and graphene have been set to 400 °C and 250 °C, respectively.

5.2.2. Graphene - electrolyte

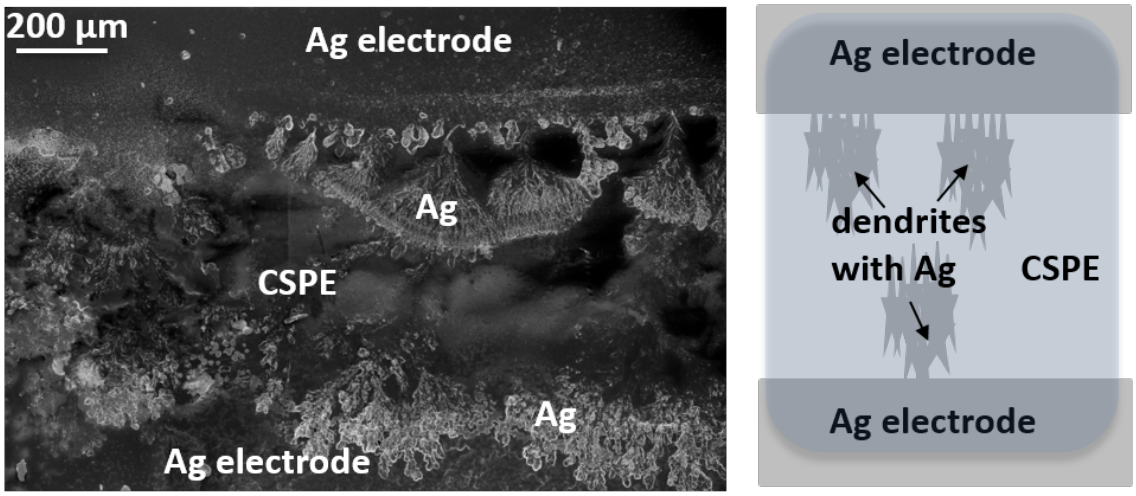

Figure 5.8.: SEM micrograph of silver electrodes in electrolyte system. Dendritic growth and ionic movement towards the cathode (from top towards bottom in the image) lead to an eventual short-circuiting.

Given that the conductivity of printed silver[48] is two orders higher than printed graphene, the suitability of silver as passive components in a fully printed EGT is investigated. The CSPE consists of lithium (Li^+) and perchlorate (ClO_4^-), which is a strong oxidising agent. With lithium, it is well known that dendritic structures arising as a result of metal nucleation are formed due to many factors including the ionic concentration and the structuring of the metallic film[124]. In presence of the perchlorate oxidising agent, silver is oxidised the result of which is the dendritic growth towards the cathode as the oxidised silver is reduced to silver metal. This eventually leads to shorting of the electrodes due to silver migration. To test for this, the CSPE is deposited across two silver electrodes and a cyclic voltammetry run from -1 V to 1 V. After three cycles of cyclic voltammetry, dendritic formation was observed at the anode (Figure 5.8 a) and these migrated to the cathode. A schematic of the experiment setup is shown in Figure 5.8 b. Dendritic structures formed, peeling out silver and leading to silver migration from one electrode to another. On the other hand, graphene is not just chemically stable, but also it has been proven in battery research that graphene stifles dendrite formation by lithium[125]. The electrical characteristics of the cyclic voltammetry form -1 V to 1 V are plotted in Figure 5.9 a for silver and graphene electrodes. The silver system was stable until 1.1 V after which the dendritic formation started. This continued with each cycle that eventually led to ionic migration and subsequent shorting of electrodes. This is clearly visible from the sudden appearance of a large ohmic current of 0.2 mA. Graphene on the other hand continued to show negligible currents even until 1.5 V. Figure 5.9 b shows that even after multiple

cycles, graphene behaves like a normal conductor which normally shows a rectangular curve. The deviation from rectangular curve into an elliptical curve is due to the parasitic capacitance and resistance.

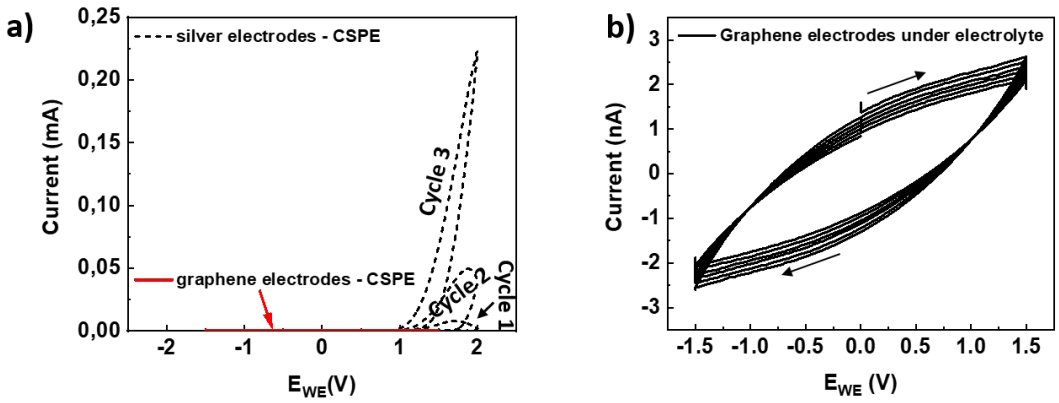

Figure 5.9.: Cyclic voltammetry of silver electrodes and graphene electrodes in presence of CSPE. a) By the third cycle, silver already showed high ohmic currents, indicating a short circuit. Graphene on the other hand continued to exhibit stable but negligible currents compared to the silver electrodes. b) More detailed view of graphene under electrolyte shows a capacitve behaviour, with some resistor component as well.

Therefore, in spite of silver superiority over graphene in terms of conductivity, graphene is chosen as the electrode to avoid undesirable electrochemical oxidation in the presence of perchlorate which is a very strong oxidizing agent.

5.3. Electrical Characterization of Printed Devices

The transistor characteristics of the as-prepared fully printed in-plane EGT are summarized in Figure 5.10. The transfer curve in Figure 5.10 a shows a clear switching behavior of the device at a threshold voltage (V_{Th}) of 0.23 V. Since a positive voltage is supplied to 'turn on' the device, it is rendered as a normally off device. The positive threshold voltage would render the transistor more suitable for usage in a lot of electronic circuits. A small clockwise hysteresis of around 0.05 V is observed, which infers the presence of few electron trap sites at the electrolyte-semiconductor interface. In the transfer curve, the drain current (I_{DS}) starts to increase linearly with the gate voltage (V_{GS}) from an off-value (I_{Off})of 10^{-9} A to an on-value (I_{On}) of about 10^{-4} A, which results in an on-off ratio of 10^5. The subthreshold slope is calculated from Equation 2.11 to be 120 mV dec^{-1} (theoretical limit around 60 mV dec^{-1}) which is also an indication of the capacitance due to charge trap density. It should be noted that in the present device the channel is 150 μm in length (L) and 60 μm in width (W). The low W/L ratio is chosen in order that the conductivity of the channel formed in indium oxide is lower than

the graphene electrodes. The negligible gate leakage current (-10^{-10} A) indicates good interfaces at every level, which makes the device very stable. The electrolyte gating promotes device operation even at low input voltages. The output I-V curve in Figure 5.10 b shows a linear increase in the drain current at low drain voltages, and it saturates at higher drain voltages, in currents in the range of 10^{-5}-10^{-4} A, for different gate-source potentials. To further characterize the printed devices, the mobility of the transistors was calculated and the contact resistance between the printed graphene and In_2O_3 is determined.

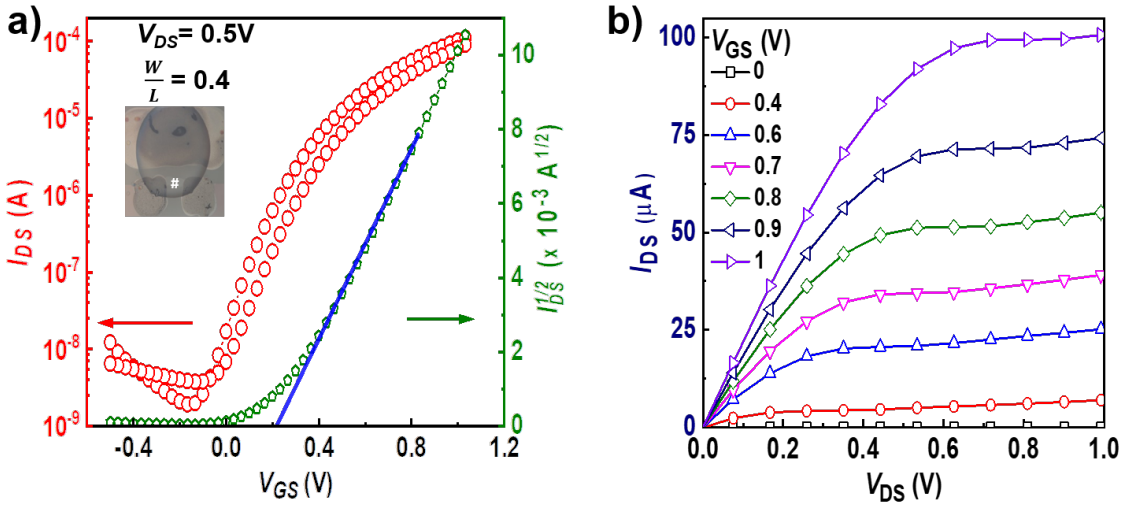

Figure 5.10.: Electrical characterization of fully printed EGT. a) Transfer characteristics give information about on-off ratio and threshold voltage. The inset shows an optical microscope image of the device; electrolyte (dark), graphene electrodes (light gray), and the semiconductor (#) connecting source and drain. (b) Output I_{DS} vs V_{DS} curves at different V_{GS} provide the drain conductance values.

Figure 5.11 depicts through a schematic, the functioning of the EGT. Indium oxide connected on either side with graphene source and drain is electrolyte-gated with graphene (Figure 5.11 a). After printing indium oxide, the electrodes are positioned at the edges, partially covering the semiconductor and leaving an area of 150 μm by 60 μm exposed. For an in-plane device, the gate is printed not on top but beside the electrodes, while the electrolyte covers the entire area of the exposed semiconductor and 80% of the graphene gate. The different viewing angles are labelled as 1 and 2. The electrical double layer is formed at the gate-electrolyte interface (Figure 5.11 b), which covers a large area. An equal double layer is formed on the other end, at the electrolyte-semiconductor interface (Figure 5.11 c), leading to a huge concentration of charge carriers on the semiconductor surface that form the conducting channel across source and drain. Unlike a dielectric gated device which requires thin film dielectric to account for electric field penetration, electrolyte gating is independent of film thickness as far as field effects are concerned.
Owing to its nanometer scale thickness, the so formed double layer capacitance contributes

to a large value of capacitance that supplies huge electric field at the interfaces. This capacitance is measured on the as prepared devices by cyclic voltammetry studies as seen in the next section 5.3.1.

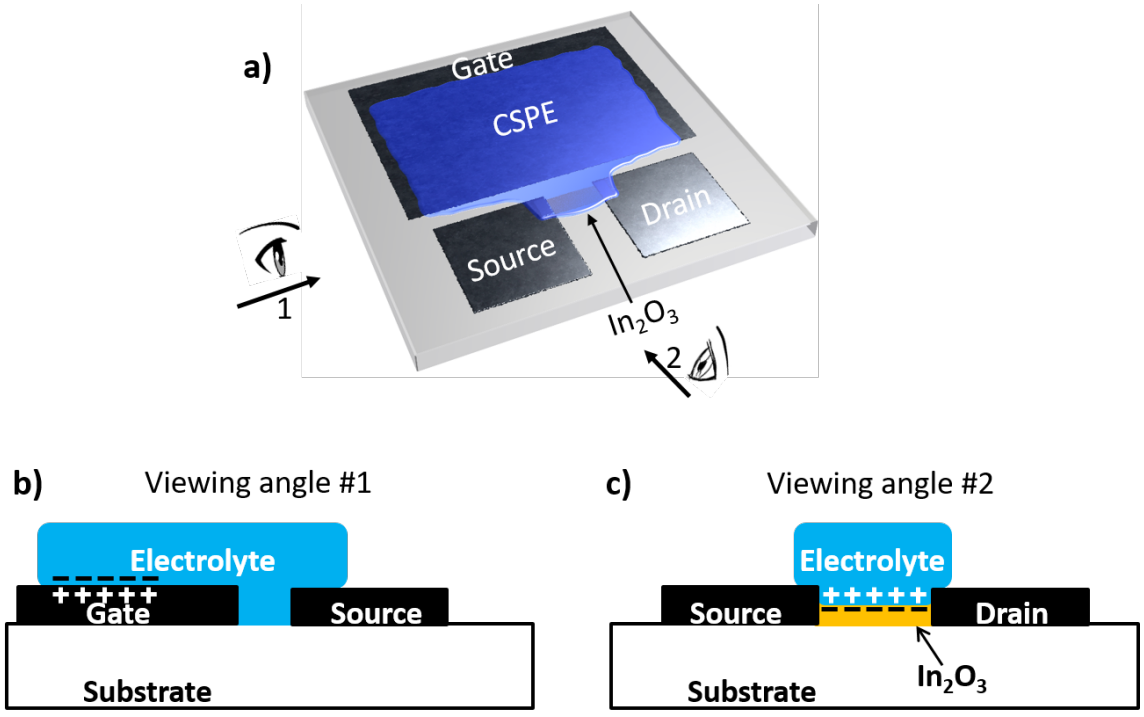

Figure 5.11.: a) Top-view of the fully printed transistor. The different viewing angles are labelled as 1 and 2. b) Viewing angle 1 during operation. After applying a gate potential, an electric double layer is formed at the electrolyte/gate interface. c) This leads to formation of an electric double layer at the electrolyte/semiconductor surface as well (viewing angle 2), despite the interfaces not being parallel.

5.3.1. Capacitance measurement

To compute μ_{lin}, the double-layer specific capacitance, at the channel-electrolyte interface (C_{SP}) is first determined. This is done by an in-situ cyclic voltammetry (CV) measurement on the EGT. These measurements are performed directly on the in-plane device structures, with shortened source and drain electrodes (Figure 5.12 a), by using different sweeping rates of the gate-source potential between -0.5 and 1 V. As the V_{GS} is swept from zero towards positive values, a conducting channel forms beyond the threshold voltage leading to higher currents in CV characteristics. As the input voltage is swept back, a reversal of the curves is seen (inset, Figure 5.12 a). This is half of the rectangular curve that is typically observed for a conductor as seen in Figure 4.5 b and can be explained by the fact that a conducting channel appears after the threshold voltage unlike a constant conductor. In reality, since the channel formation is gradual and there exists a resistive component

in addition to capacitance, there is some deviation from the ideal curve. This is observed on the EGT as well, as seen in Figure 5.12 b. Current density (J_{GS}) at different sweeping rates ($\frac{\partial V_{GS}}{\partial t}$) has been plotted against the input V_{GS}. Until the threshold voltage of 0.23 V, there is no conducting channel that is formed on the surface of the semiconductor. Beyond the threshold voltage, a gradual formation of the channel due to accumulation of charge carriers (electrons in this case) and a near saturation is seen, indicating the conductor-like CV graph. In the reverse sweep, an exponential characteristic at the corner is observed, which is an indication of parasitic capacitance and other resistive components.

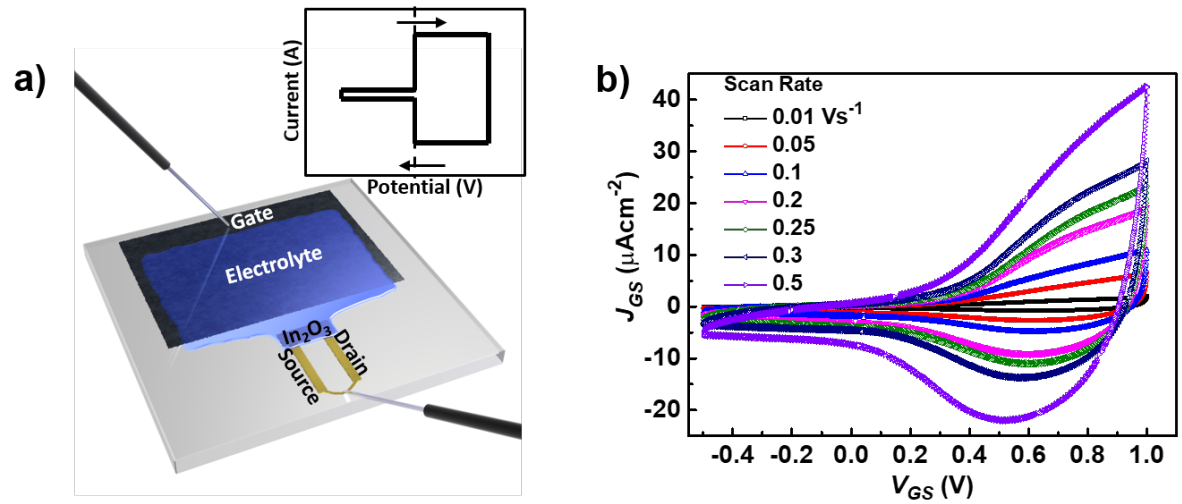

Figure 5.12.: Double layer capacitance measurement in the EGT. a) Experiment setup. The source and drain are shorted to make indium oxide as the working electrode. Inset shows an ideal double layer capacitance at the electrolyte-gated semiconductor. b) Current density vs gate voltage plot reveals the half dog-bone shaped curve. The deviation from the ideal curve is due to the additional resistances. Current density measurements are performed for different scan rates.

The average current density at every V_{GS} is plotted against the scan rate as seen in Figure 5.13 a. This is a family of linear curves and the slope of the curves ($J_{GS} = C_{SP}(\frac{\partial V_{GS}}{\partial t})$, given by the Equation 4.3) is calculated to be C_{SP}. The linear increase in the current density before the threshold voltage is slightly flat and beyond the threshold voltage the linear curves steepened and then saturated. The C_{SP} at this saturated slope is considered. This trend is similar to the capacitance that has been observed in an ideal metal insulator semiconductor (MIS) capacitor structure.

Figure 5.13 b shows C_{SP} as a function of V_{GS}. The capacitance increases almost linearly from 10 μ Fcm-2 at 0.1 V to 35 μFcm^{-2} at 0.5 V, and it appears to saturate after 0.7 V at 42 μFcm^{-2}. The capacitance of 40 μFcm^{-2} at a gate voltage of 0.6 V is used for the mobility extraction. The value of the specific capacitance is higher than what is generally expected for a semiconductor[107]. This could arise from the underestimation

of the semiconductor surface area, since the porosity of indium oxide as seen in Figure 5.2 a is neglected in area calculation.

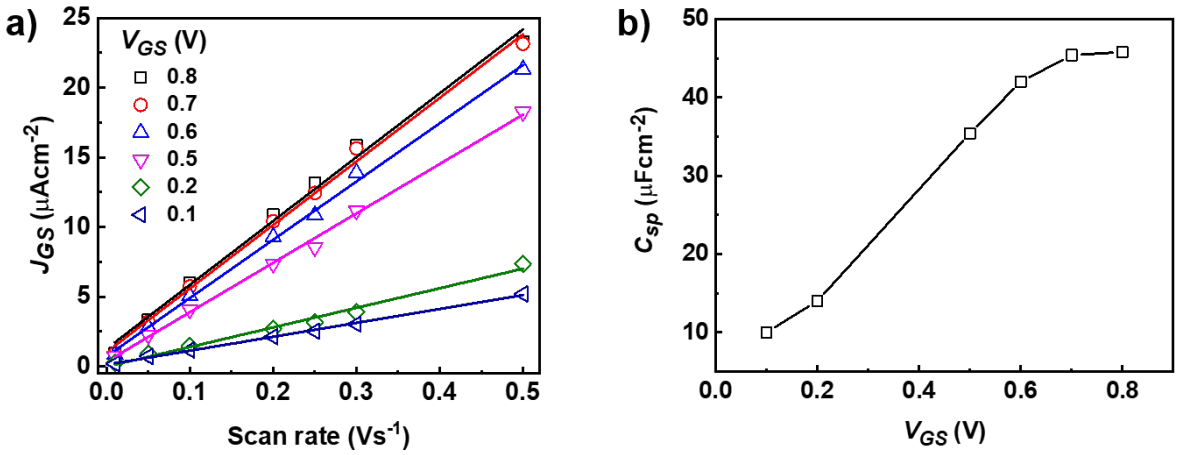

Figure 5.13.: EDL capacitance calculation from CV measurement. a) The slope of current density vs scan rate gives the value of the capacitance at different gate voltage. b) Capacitance value saturates when the channel is fully formed in indium oxide.

The specific capacitance value obtained from cyclic voltammetry is corroborated with the value obtained using impedance studies on the fully printed EGT. The nyquist plot with the imaginary part of impedance on the y-axis and the real part on the x-axis is shown in Figure 5.14. The chosen frequency range is 100 Hz to 0.1 Hz and the capacitance is calculated at a gate voltage of 0.6 V for 1 Hz using the Equation 4.5. Since the EGT is limited by the ionic conductivity and double-layer formation in the electrolyte, a the capacitance is calculated at 1 Hz frequency. It is known that electrical double layer polarization contributes to low frequency response, with cutoff frequencies of KHz or lesser[33]. A Randle cell is used as the equivalent circuit and a double-layer capacitance value of 35 μFcm^{-2} is calculated.

Parasitic capacitance

From Figure5.9 b, the estimated capacitance for graphene with the electrolyte is 12 μFcm^{-2}. Considering this high capacitance value, in the coplanar structure, parasitic capacitance (capacitance between source/drain and the gate due to overlap of electrodes by the electrolyte) is high. This could affect the speed of device operation. Assuming a negligible overlap of electrodes by the electrolyte, the transistor cut-off frequency (f_T) Equation 2.13 for a channel length of 150 μm with a device mobility of 20 cm^{2}V^{-1}s^{-1} results in f_T equal to 15 kHz. Considering a non-negligible overlap of about 25 μm on the electrodes owing to printing variability, the f_T reduces to 12 kHz. Even without considering the parasitic capacitance, this is a significant reduction. For an in-plane structure, when the resistance

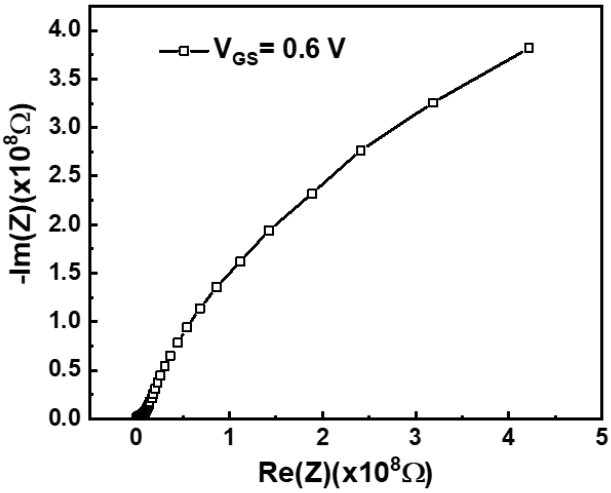

Figure 5.14.: Capacitance measurement using impedance spectroscopy

of the electrolyte due to the large gate to channel distance is considered, a reduction is seen in the frequency that is introduced in Equation 2.14.

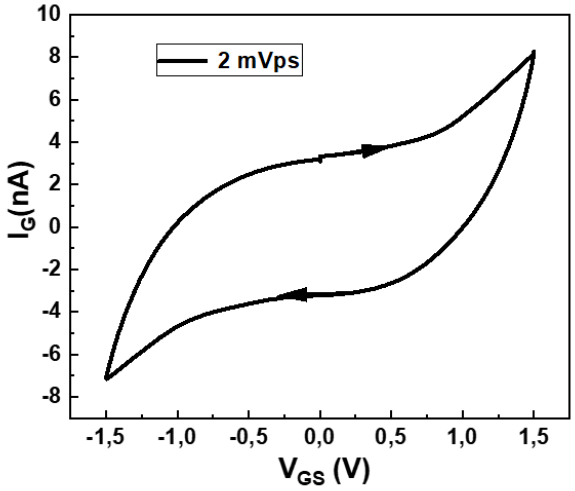

Figure 5.15.: Gate current vs gate voltage in EGT

Therefore it is very important to ensure negligible overlap of electrodes as well as low gate to channel distance, in fully printed EGTs meaning that the printing process should be well defined and controlled. Given the undefined area of the overlap of the electrodes, the parasitic capacitance can only be estimated from the gate current, I_G seen in Figure 5.15. A very low gate current is observed until 1 V leading to an estimated parasitic capacitance of about 5 μFcm^{-2}. An increase in gate current is noticed only after about 1.2 V, which

is an indication of faradaic currents in the electrolyte. Therefore the device operation is restricted to less than or equal to 1V.

It has been established that electrolyte gating reduces the contact resistance as compared to dielectric gating[126] and in a coplanar structure, due to the presence of electrical double layer in the electrolyte even at the electrode/semiconductor interface, excess ions give additional electric field and drive injection of charges from the contact[78]. The reduced contact resistance is calculated in the following section.

5.3.2. Contact resistance correction

An important device parameter, which significantly affects the transistor performance, especially at low input voltages, is the contact resistance between graphene and semiconductor. To analyze the performance of the transistor, the contact resistance between graphene and the In_2O_3 channel, while using electrolyte gating, needs to be accounted for. Therefore, the specific contact resistance is measured in the EGT by using the so-called transmission line method (TLM), proposed by Reeves and Harrison[127]. To eliminate or correct for the contact resistance in the mobility estimation, the conditions set are that the channel width, W is kept constant while varying the length, L.

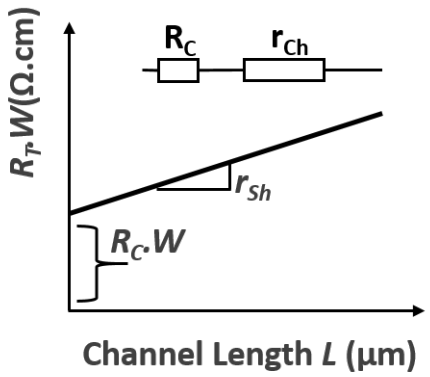

Figure 5.16.: TLM to measure specific contact resistance. Total resistance is plotted as a function of length. Slope gives the sheet resistance of channel and y-intercept the contact resistance.

As can be seen in the inset circuit of Figure 5.16, the contact resistance (R_C) is in series to the channel resistance, r_{Ch}. Together, these constitute the total resistance, R_T.

$$R_C + r_{Ch} = R_T$$

The channel resistance can be written in terms of its sheet resistance, r_{Sh} as

$$R_C + r_{Sh}\frac{L}{W} = R_T$$

Multiplying the entire equation with W, we get

$$R_{\mathrm{C}}.W + r_{\mathrm{Sh}}L = R_{\mathrm{T}}.W \tag{5.1}$$

This is a linear relation between R_T.W and L (figure 5.16), the slope of which gives r_{Sh} and the y-intercept gives the R_C.W. As per the Equation 2.9, the drain current in the linear regime is given by,

$$I_{\mathrm{D,lin}} = \frac{W\mu C_{\mathrm{SP}}}{L}[(V_{\mathrm{G}} - V_{\mathrm{Th}})V_{\mathrm{D}}]$$

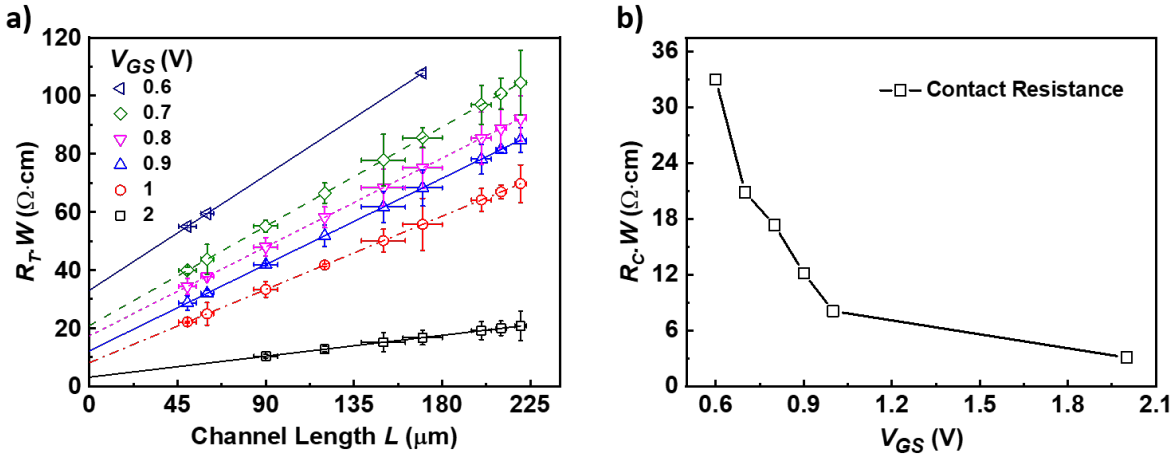

Figure 5.17.: Contact resistance extracted using transmission line method. a) Resistance from the drain conductance in the linear regime is plotted as a function of channel length. Y-intercept gives the contact resistance. Slope gives channel resistance.

When the contact resistance correction is introduced, only the influence by the channel resistance has to be considered and the contact resistance part eliminated. Therefore, the current looks like the Equation 5.2

$$I_{\mathrm{D,lin}} = \frac{W\mu C_{\mathrm{SP}}}{L}[(V_{\mathrm{G}} - V_{\mathrm{Th}})(V_{\mathrm{D}} - I_{\mathrm{D}}R_{\mathrm{C}})] \tag{5.2}$$

The inverse of the drain conductance ($\frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{D}}}$) is the total resistance, R_T. Reorganising the Equation 5.2 and differentiating, the following equations are obtained.

$$(1 + \frac{W\mu C_{\mathrm{DL}}}{L}(V_{\mathrm{G}} - V_{\mathrm{Th}})R_{\mathrm{C}})I_{\mathrm{D,lin}} = \frac{W\mu C_{\mathrm{SP}}}{L}(V_{\mathrm{G}} - V_{\mathrm{Th}})V_{\mathrm{D}}$$

Differentiating the above equation and rewriting total resistance, R_T in terms of the drain conductance we get,

$$R_{\mathrm{T}} = \left.\frac{\partial V_{\mathrm{D}}}{\partial I_{\mathrm{D}}}\right|_{lin} = \frac{L}{W\mu_{\mathrm{lin}}C_{\mathrm{SP}}(V_{\mathrm{G}} - V_{\mathrm{T}})} + R_{\mathrm{C}} \tag{5.3}$$

To calculate the contact resistance, devices, with varied channel lengths, but of fixed width (W), were prepared, and the inverse of the slope, in the linear region of the output curve ($R_T = \frac{\partial V_{DS}}{\partial I_{DS}}$) is plotted against the channel length (R_T.W vs L) and presented in figure 5.17 a. The y-intercept of the linear curves, R_C is plotted against V_{GS} in Figure 5.17 b and amounts to 33 Ω·cm for a gate-source potential of 0.6 V, which cannot be neglected in the mobility estimation (the channel resistance in comparison is about 70 Ω·cm for the channel length of 150 μm). The device mobility is therefore calculated after correcting for the contact resistance according to Equation 5.3. It is of note that this contact resistance value is significantly lower than the contact resistances typically obtained by using dielectric gating[17] The channel sheet resistance (Figure 4c), which is obtained from the slope of the individual linear fits in Figure 4a, marginally decreases with gate voltage, and it has a value around 4 kΩ between 0.6 and 1 V. Additionally, the device parameters, with varied channel dimensions, are presented in Table 1. Further device details, including the measurement reliability factor[128], can be found in the Supporting Information.

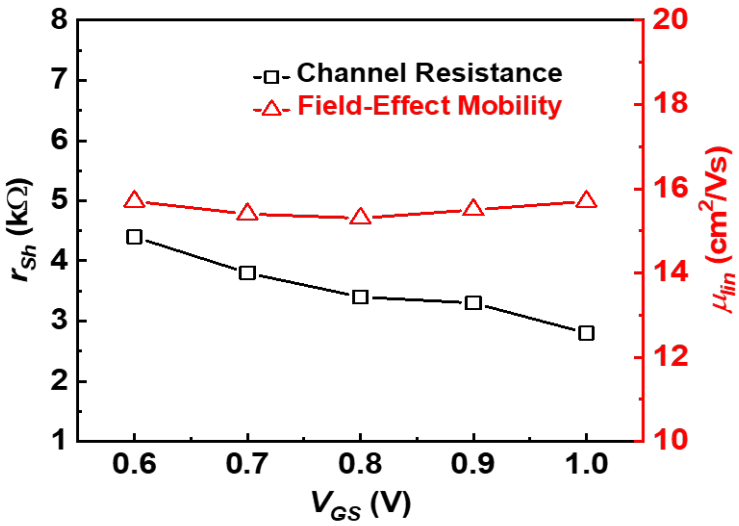

Figure 5.18.: Contact resistance corrected mobility show constant value with gate voltage. The channel resistance is plotted on the left y-axis as a function of gate voltage beyond the threshold voltage.

From the above given equations, the channel sheet resistance can be written as Equation 5.4.

$$r_{Sh} = \frac{1}{\mu_{lin} C_{SP} (V_G - V_T)} \tag{5.4}$$

r_{Sh} is independent on the dimensions of the channel. This is plotted in Figure 5.18. Beyond the threshold voltage, once the channel is fully formed, the channel sheet resistance is almost constant at 3500 Ω. The mobility extracted from the linear region using Equation 2.12 is now corrected for the contact resistance. This is naturally reflected in the mobility values which is calculated as 16 $cm^2V^{-1}s^{-1}$ and reflects a constant mobility situation. This

contact resistance corrected mobility value can now be used in the determination of the transistor switching speed. The device mobility is comparable to that obtained in devices with printed ITO electrodes, and it outperforms the value that has been reported for all-printed devices with amorphous oxide semiconductors[111, 129]. The device parameters with varying channel dimensions are presented in Table 5.1.

channel dimension W/L	on-off ratio $\log(I_{on}/I_{off})$	subthreshold slope mV/dec	threshold voltage V	mobility, μ_{lin} $cm^2V^{-1}s^{-1}$
1	2.7	70	-0.11	2.7
0.8	4	140	-0.07	2.6
0.6	5.25	130	0.15	10.8
0.4	5.75	120	0.23	16
0.2	5.5	86	0.32	17.6

Table 5.1.: Fully printed EGT performance at different W/L values.

5.3.3. Top-gated devices

To examine the impact that changed transistor geometry has on the performance, the architecture of the devices was changed from in-plane to top-gated configuration. As top-gated electrode, room temperature processed poly(3,4-ethylene dioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS) was utilized, being that the temperature necessary for the processing of graphene would render the electrolyte unusable. Additional layers of electrolyte are printed to ensure that the top gate does not short with the semiconductor and PEDOT:PSS is ink-jet printed in such a way that it is above the entire semiconductor (Figure 5.19).

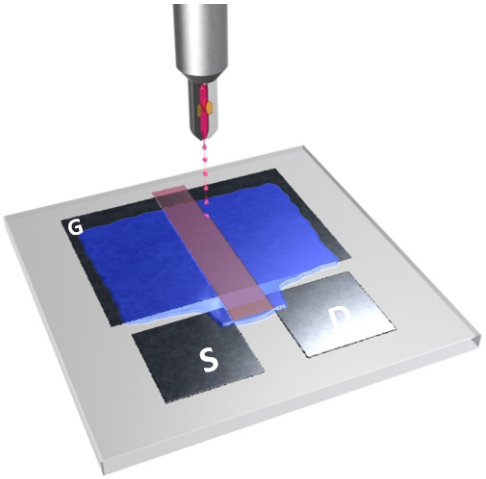

Figure 5.19.: Printing top gate structure instead of in-plane structure. Room temperature conducting PEDOT:PSS is printed as top gate to improve device performance.

The threshold voltage is considerably lowered for a top-gated device (0.08 V) as compared to an in-plane device. This occurred despite the semiconductor being the same as before. Therefore, it can be assumed that higher electric field arising from the top-gate lead to a reduction in threshold voltage. The addition of ethylene glycol to PEDOT:PSS led to an increase in conductivity resulting from the straightening of the polymer chains in PEDOT:PSS[130], because of the addition of ethylene glycol and water. As a result, the on-off ratio for the top-gated device improved by one order to 10^6 as can be seen in Figure 5.20 a. This is one order higher in magnitude compared to the in-plane device. Additionally, a reduced hysteresis is also observed, plausibly due to the reduced charge traps at the electrode-semiconductor interface which is now influenced by electrolyte gating. This is clearly indicated by a reduction in the subthreshold slope (SS) to 70 $mVdec^{-1}$, which is closer to the theoretical limit. The electrolyte thickness is bound to influence the subthreshold slope as well[131]. In addition, the top-gated devices demonstrate high output current (Figure 5.20 b) of 115 μA at a gate-source voltage of 1 V. The reduction from 50 μm to 5 μm for in-plane and top-gated architectures, respectively, reduces the formation time of the electrical double-layer, resulting in a higher switching frequency. The switching speed is inversely dependent on the resistance, which is in turn dependent on the length between the gate and the semiconductor.

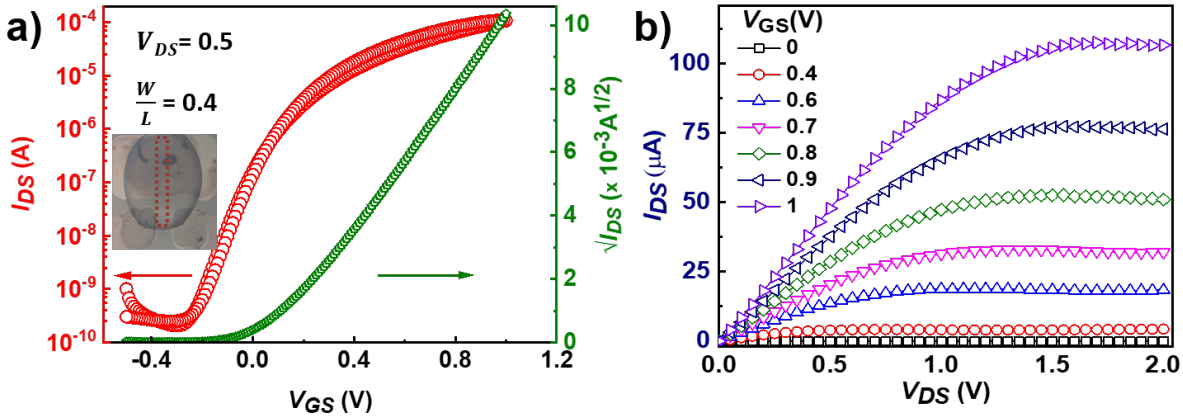

Figure 5.20.: Electrical characterization of fully printed top gated EGT. a) Transfer characteristics show higher on-off ratio and lower threshold voltage compared to in-plane structure. Hysteresis is also reduced. Inset shows an optical microscope image of the device with the red dotted rectangle denoting the top gate. (b) Output I_{DS} vs V_{DS} curves at different V_{GS} follow the Shockley trend.

To estimate the switching speed difference between the two geometries, pulsed potential measurements have been performed and the time needed for the formation of the electrical double layer (τ_{RC}) is obtained. Figure 5.21 shows the comparison of the current increase during pulsing. It is identified that the top-gated devices display much higher sensitivity against the potential change than that of in-plane devices. The device

performance is tested when the gate voltage is pulsed from -1 V to 1 V (blue curve) at a frequency of 1 Hz. The current in the top-gated device (black curve) rises to 10^{-4} A between 0.3 and 0.4 s and saturates, whereas in the in-plane device, the current (green curve) rises to 10^{-5} A from 0.3 to 0.6 s and is yet to saturate after 0.8 s. Overall, the current in the top-gated device rises to 1 order higher I_{DS} as compared to the in-plane device within a time period of 0.5 s. By fitting the measured curves to an exponential function in Equation 5.5, the $R_{el}C_{DL}$ time constant for top-gated devices is calculated as 80 ms and 220 ms for in-plane devices.

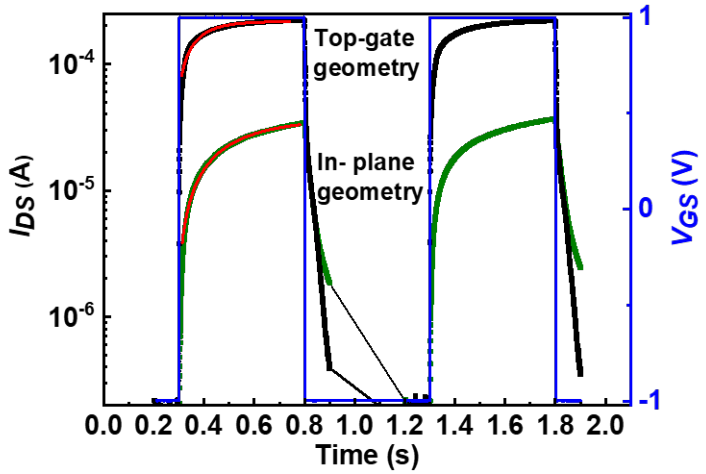

Figure 5.21.: Switching speed comparison of top-gated and in-plane devices. A voltage pulse from -1 to 1 V is applied with a frequency of 1 s. It can be seen that top-gated devices reaches one order higher current within 0.5 s compared to the in-plane devices.

The fitting equation is denoted as

$$I_{DS} = I_{DS,max}.(1 - exp(\frac{-t}{\tau_{RC}})) \tag{5.5}$$

For top-gate devices, the curve fit gives rise to

$$I_{DS,top} = (2.16x10^{-4}).(1 - exp(\frac{-t + 0.28}{0.08}))$$

And for in-plane devices, the fitted curve is

$$I_{DS,in\text{-}plane} = (3.7x10^{-5}).(1 - exp(\frac{-t + 0.28}{0.22}))$$

Therefore, as per the equation, the extracted τ_{RC} is 0.08s for top-gate geometry and 0.22s for in-plane geometry.

A comprehensive comparison of the in-plane and top-gate geometries are shown in the table 5.2 and the resultant device is completely characterized to be used in a fully printed circuit on flexible substrate.

Parameters		In-plane device	Top-gate device
Channel width/length	$\frac{W}{L}$	0.4	0.4
Threshold voltage, V_{Th}	V	0.23	0.08
Current on-off ratio	$\frac{I_{On}}{I_{Off}}$	10^5	10^6
Hysteresis	V	0.05	negligible
Subthreshold Swing	$mVdec^{-1}$	120	70
Switching speed	ms	220	80

Table 5.2.: Comparison of Device Parameters for In-Plane and Top-Gate Geometries

6. Printed and Flexible Inverters

Having developed a fully printed transistor that is characterized and corrected for the contact resistance and switching speed, EGTs and inverters can next be developed on flexible substrates. Since the annealing of the indium oxide requires high temperature when polymer substrates are concerned, a temperature stable polyimide kapton® (PI) is used. Since the surface energy of the PI is different compared to glass substrate, the contact angle hysteresis during the printing process are studied is overcome in order to avoid the coffee-ring effect on the film. Macroscopic effects are also influenced by the thicknesses, the elastic moduli and the thermal expansion coefficients of the oxide film and the substrate. While plastic substrates require that the oxide film is processed at lower temperatures, their surface properties influence the wettability and morphology of the. During the processing, the thermal expansion coefficients and the substrate surface effects are tuned to obtain indium oxide films identical to the ones prepared on glass. In order to design the inverter with a NEGT, a transistor-resistor logic (TRL) is used and graphene is printed as the resistor as well. The hence obtained fully printed inverters are characterized for their electrical behaviour over time and with subject to mechanical strain. Details of the studies are presented in this chapter.

On the relatively smooth surface of glass, printing aqueous precursors of indium oxide is well defined. The printed contact angle can be modified to one's wish by making the substrate hydrophilic using surface treatments such as plasma cleaning, piranha treatment or by making the substrate hydrophobic using thin layers of coating. During the curing process of the precursor into indium oxide, glass remains rigid because of its lower coefficient of thermal expansion compared to indium oxide. However, with regards to flexible kapton® (PI), the surface roughness, energy and the thermal expansion coefficient are different and the printing process is not well defined. For example, the surface roughness is about five times as compared to the float glass and the thermal expansion coefficient is about ten times as that of indium oxide (refer to table 2.4). Therefore there is a higher probability of crack formation during the annealing of indium oxide and hence this needs to be well controlled. The Kapton is physically tough with a tensile strength of 165 MPa at a thickness of 125 μm. However, the PI film begins to decompose and pyrolyse beyond 400 °C and 800 °C respectively. PI film elongates by more than 10% at room temperature post annealing at 400 °C[91], which is the temperature used to cure the semiconductor precursor into indium oxide. This is sufficient for crack formation in the oxide film, to counter which, the precursor ink formulation is changed to reduce the processing temperature. Ethylene glycol (EG) is used as the co-solvent to water instead of glycerol as the boiling point of ethylene glycol is 197 °C as compared to 290 °C for glycerol. Since aqueous nitrates decompose into oxides at fairly low temperature (about 170 °C)[132], the curing temperature of the oxide precursor could hence be limited to 300

°C, which is below the softening temperature of PI. The xrd diffraction patterns of indium nitrate precursor heated at 300 °C and 400 °C as seen in Figure 6.1 shows that pure indium oxide peaks are obtained at 300 °C as well. Thus it is possible to print electrolyte-gated transistors using semiconductor precursors on PI film.

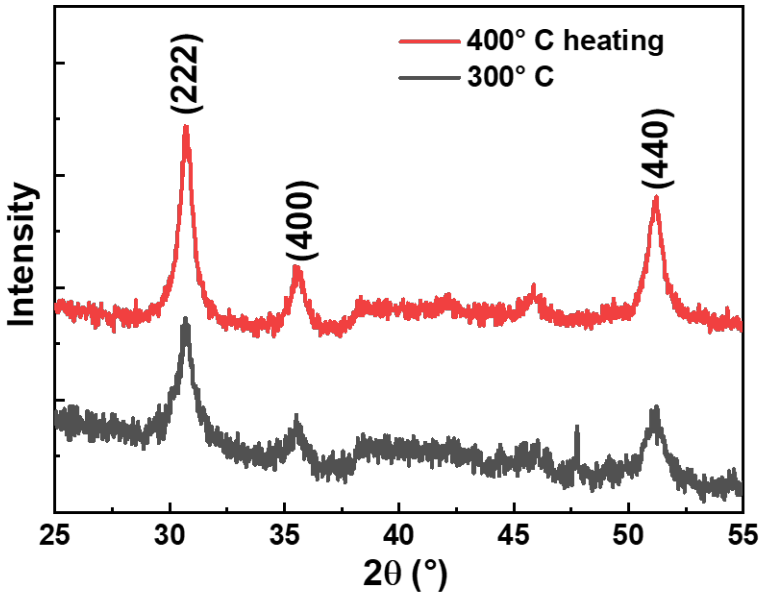

Figure 6.1.: XRD patterns of indium oxide precursor with ethylene glycol heated at 300 °and 400 °C. Pure indium oxide peaks are indexed.

6.1. Surface Modification of Polyimide

The PI substrate is initially aged by heating for 2 hours at 400 °C, to avoid abrupt expansion effects during the processing of the precursor ink printed on the substrate. This leads to a change in the contact angle of the printed aqueous drop which is observed using a sessile goniometer as shown in Figure 6.2. The contact angle of the untreated PI substrate is 64.4 °and falls in the range of most stable contact angle[133]. The increase in the surface energy after thermal treatment resulted in a reduction of contact angle to 37.6 °. Therefore, after pre-heating, the PI substrate is rinsed with a solution of 4:1 isopropanol and acetone mixture to reduce the surface energy[134] and counter the contact angle pinning. This leads to an increase of the contact angle to 71.4 °(Figure 6.2 c)) and precursor films with controlled dimensions and sharper edges could be printed.

The pinning of the contact angle on the treated substrate resulted in a coffee-ring formation. Since the contact is pinned at low angles, an outward flow of particles resulted in a ring formation as seen in Figure 6.3 a. Apart from the addition of ethylene glycol to counter the coffee-ring effect through the Marangoni flow, the treatment with isopropanol-acetone

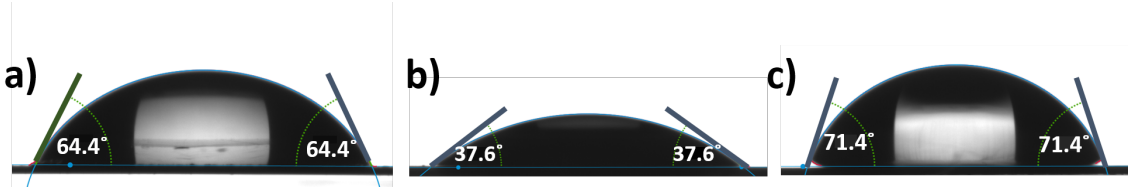

Figure 6.2.: Contact angle on surface modified PI substrate. a) Untreated PI b) Annealed c) Solvent treated post annealing.

mixture assisted in countering the contact angle pinning on the PI surface, thereafter giving rise to a concentrated film as seen in Figure 6.3 b.

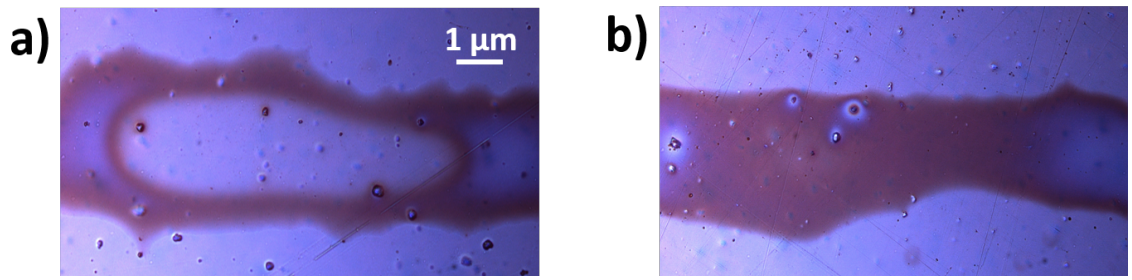

Figure 6.3.: Printing and processing of precursor ink on a) Polyimide substrate without the cleaning step. The high surface energy of the polyimide to the formation of the so called 'coffee-ring' immediately after printing. b) Substrate treated with 4:1 isopropanol and acetone mixture after pre-heating. Dense films can be seen after printing and continues even after heating to 300 °C. Reproduced with permission from Wiley[135]

6.2. Printed Inverters

As discussed in the previous chapter, indium oxide is printed first in accordance to roughness difference with graphene and to minimize the contact resistance.

6.2.1. Indium oxide on polyimide

To obtain high-performance electronics, a dense and continuous oxide film is necessary. However, when the aqueous precursor of the In_2O_3 is printed on the PI after the substrate treatments. The precursor is then dried at 100 °C before annealing at 300 °C. Thus water is already evaporated giving a concentrated film that is to be cured into indium oxide. Oxide films prepared in this way on the PI substrate have homogeneous morphology and can be seen clearly in an optical micrograph (Figure 6.4 a). The dried film exhibited dense morphology even after annealing at 300 °C (Figure 6.4 b). The surface profile of the oxide film is mapped using an atomic force micrograph and the roughness of the film is measured to be less than 5 nm. The precursor ink for the channel, which is printed first,

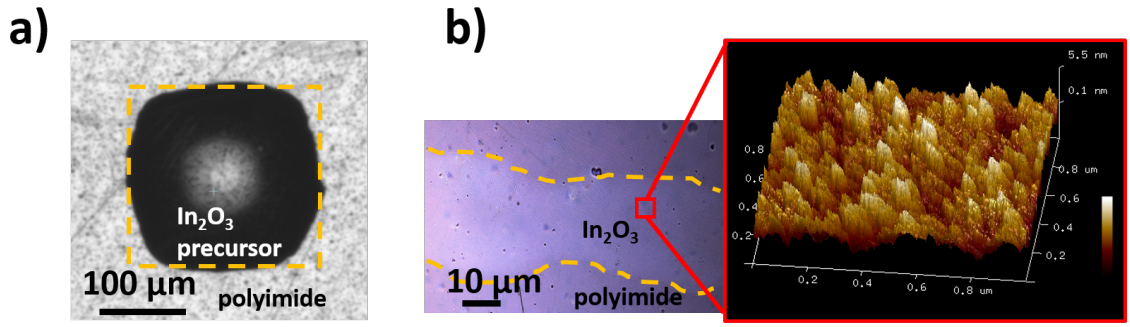

Figure 6.4.: a) Printed patterns that fit perfectly with the desired ones (as seen in yellow dashed lines) could be achieved. b) Optical image of the smooth and homogenous In_2O_3 formed after the annealing step. In the inset, atomic force micrograph of 1 μm^2 area on the oxide film shows minimal roughness.Reproduced with permission from Wiley[135]

is dried at 100 °C. The passive electrodes are printed using graphene ink such that the channel has a width-to-length ratio (W/L) of 60/150. The precursor and all the graphene passive structures are heated together to 300 °C for two hours after which electrolyte and top gate are printed.

6.2.2. Printed graphene resistors

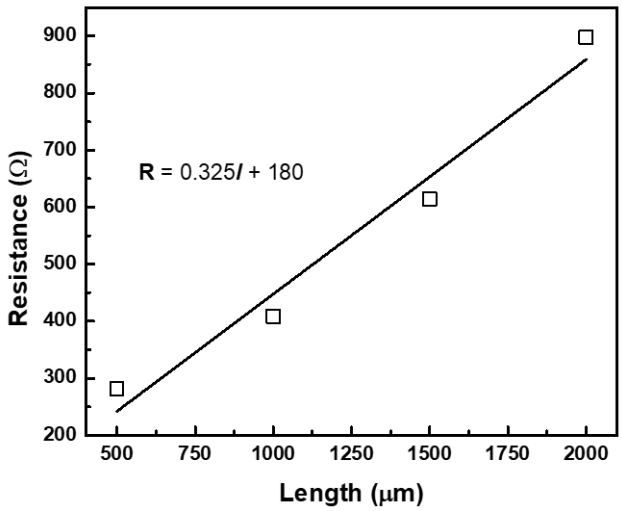

Figure 6.5.: Resistance variation of printed graphene lines with a constant cross-sectional area, processed at 250 °C. The meander structures of graphene give rise to a resistance of 400 kΩ. Reproduced with permission from Wiley[135]

The graphene passive structures mentioned above consist of the source/drain/gate electrodes as well as the resistor in the TRL inverter. In general, for a body of intrinsic resistivity ρ, length l and cross sectional area A, the resistance R is given by the Equation 6.1. For a printed graphene film as well, the resistance is found to be linearly proportional to the length of the film for a fixed cross sectional area. The typical thickness of the printed graphene is 300 nm.

$$R = \frac{\rho l}{A} \tag{6.1}$$

The plot of resistance vs length can be seen in Figure 6.5 for graphene heated at 250 °C for 2 hours. A linear increase in the resistance against the length is observed in the trend and hence it is possible to print resistors of choice with graphene ink. The linear dependence is given in the inset of the graph and the conductivity of the graphene film is calculated from the slope which is equal to 0.325 Ωm^{-1}. Knowing a thickness of 300 nm and width of 300 μm which make up the cross-sectional area A, the resistivity is calculated as 4 x 10^{-5} Ωm. Thus, the conductivity of the printed graphene film is 25,000 S/m. The linear dependence of the resistance with length implies that the resistance of the printed graphene ink can be controlled by changing the length of the printed film and thus, meander structures of the graphene ink are printed at the drain electrode and processed at 250 °C to obtain a resistance of 250 – 400 kΩ. For example, to achieve resistance of 250 kΩ, a graphene film of about 3 cm in length is printed. In contrast, if silver is used, a length of 10^4 m has to be printed.

6.2.3. Fully printed inverters

The details of the printing process are shown in Figure 6.6 a-e. The substrate is first aged at 400 °C and rinsed with isopropanol-acetone mixture. Then the aqueous nitrate precursor is printed and dried at 100 °C, after which the graphene passive structures are printed. The substrate is annealed at 300 °C for two hours, followed by CSPE and PEDOT:PSS top gate printing. This is the design for a fully printed transistor-resistor logic based inverter. Transistors are printed separately to assess the required resistance and frequency of operation for the inverters.

Figure 6.7 shows a microscope image of the fully printed inverters prepared using a TRL. The inset shows an image of a single inverter with the source (S), drain (D) electrodes, pull-up resistor to the right, the CSPE and top-gate between the dashed lines. Source is grounded. The input voltage (V_{IN}) is given at the gate of the transistor and the output, V_{OUT} is measured at the drain of the transistor. The inverter is 'pulled up' to the applied drive voltage, V_{DD}. The CSPE and the PEDOT:PSS are also marked in the image.

6.3. Electrical Characterization of Flexible Devices

First, the fully printed transistors on flexible PI are evaluated for their characteristics. Subsequently, inverters are evaluated for the DC characterization, signal gain, transient

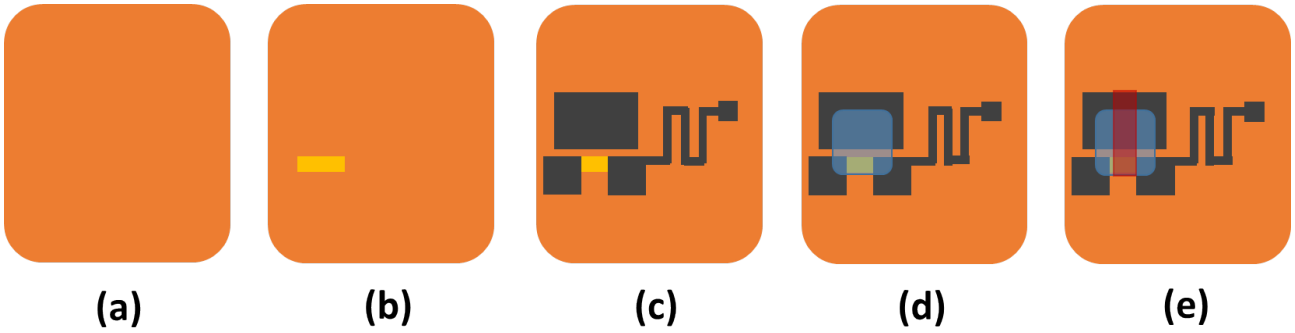

Figure 6.6.: Steps followed in the fabrication of fully printed inverters on polyimide. a) Polyimide substrate pre-heated to 400 °C and rinsed with 4:1 isopropanol and acetone mixture. b) Precursor of In_2O_3 printed and dried at 100 °C. c) Printing of graphene passive structures (source-, drain-, gate- and resistance). d) CSPE printed across semiconductor and gate. e) Printing of PEDOT:PSS top gate.Reproduced with permission from Wiley[135]

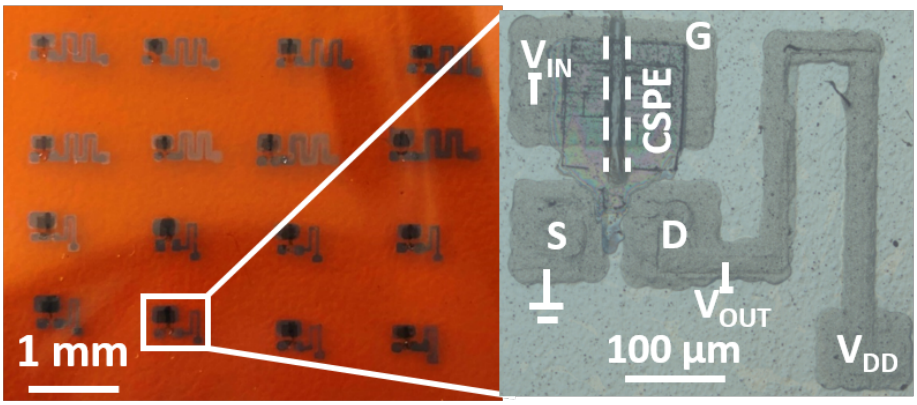

Figure 6.7.: Optical micrograph sample of the printed inverters and a zoomed in image of a single inverter. In the inset, the input and output voltages, the drive voltage and the components are labeled. Reproduced with permission from Wiley[135]

properties and noise margin calculation. Mechanical strength of the printed devices and temporal stability are also comprehensively studied.

6.3.1. Flexible transistors

The fully printed transistors (Figure 6.8) exhibit an off-current of about $4x10^{-11}$ and an on-current of $2x10^{-5}$ therefore displaying an on/off ratio of about 10^6. The high on-off ratio is useful for digital circuits. Considerably negligible gate currents (10^{-9}) indicate that the channel is well isolated from the gate and parasitic capacitance is low since the overlap of electrodes is negligible. The subthreshold slope in the linear region is 100 $mVdec^{-1}$, which is an increase over the devices prepared on glass in earlier chapter (section 5.3.3). This is an indication of increase in charge trap density, as the PI substrate

due to its high dielectric strength can probably trap more charge compared to glass. The threshold voltage, obtained through the extrapolation of the linear region of the I_{DS} vs V_{GS} plot at low drain-source voltage, is calculated to be 0.2 V, which is expected. However, the hysteresis of the transistor threshold voltages in the forward and reverse sweeps of the transfer curve ($V_{th,forward}$-$V_{th,backward}$) carries a value of 0.15 V. This is because of the low ionic mobility in the electrolyte, that leads to high resistance and slow response of ions in the electrolyte at the given input voltages and charge traps at the electrolyte-substrate interface. The device mobility is extracted from the linear region of the transfer curve using the drain conductance (Equation 2.12). The $\mu_{lin}C_{DL}$ is 250μF $V^{-1}s^{-1}$ for the printed transistor. Considering the capacitance value of 35 μFcm^{-2} as calculated using cyclic voltammetry,[136] the device mobility (μ_{lin}) is 12 $cm^2V^{-1}s^{-1}$. This value is similar to the fully printed transistors that are printed on rigid substrates such as glass.

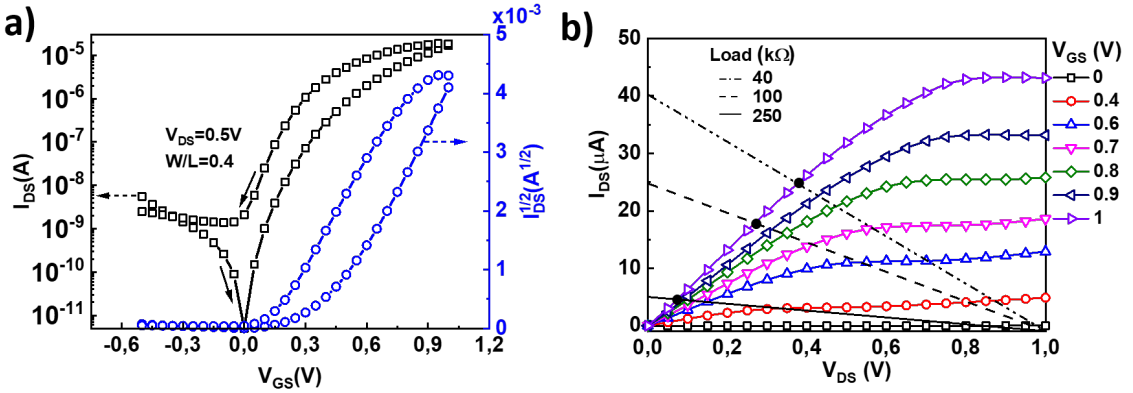

Figure 6.8.: Fully printed electrolyte-gated transistor and inverter on flexible PI substrate. a) Transfer characteristics of a typical fully printed electrolyte-gated oxide transistor on a flexible substrate. The applied drain voltage is 0.5 V. The squares represent I_{DS} vs V_{GS}, whereas the circles represent $I_{DS}^{1/2}$ vs V_{GS}. The threshold voltage is calculated to be 0.2 V. b) I_{DS}-V_{DS} output characteristics of the transistor with V_{GS} varied from 0 V to 1 V.

The loadline analysis can be seen in the output characteristics of the flexible transistor, Figure 6.8 b. Load resistances of 40, 100 and 250 kΩ are plotted using the loadline Equation 2.15. A look at the output curve for V_{GS} of 1 V shows the output drain voltage swing for the 40 kΩ resistance to be between 0.4 and 1 V whereas for the load resistance of 250 kΩ, the output range is between 0.06 and 1 V. For 100 kΩ load resistance, the output swing is between 0.25 and 1 V. It can be therefore inferred that high load resistance is to be printed for a larger output swing in inverters based on transistor-resistor logic.

6.3.2. Flexible inverters

In the printed inverter, since the n-type electrolyte-gated transistor is off-state at low input voltages, the output voltage can be 'pulled-up' to the supply voltage, V_{DD}. To facilitate this,

a graphene resistor load of 250 kΩ is printed in series with the transistor (TRL inverter). Since the graphene ink offers higher resistance compared to other metallic inks like silver, resistors can beprovides the advantage of printing. Since the resistance of the printed graphene increases linearly with the length of the structure, lines with a length of 1000 μm, a constant width of 75 μm and a thickness of 300 nm are printed to obtain the 250 kΩ resistance load in the inverter. The DC characteristics of the printed inverter for a supply voltage (V_{DD}) of 1 V and an input voltage (V_{IN}) swept from -1 to 1 V are shown in Figure 6.9. Output voltages (V_{OUT}) of 0.99 V and 0.03 V at low and higher V_{IN}, respectively, are observed. This is in agreement with the loadline analysis on the printed transistor. The V_{OUT} did not reach the ideal minimum of 0 V since the transistor carries some resistance even when the channel has been fully formed.

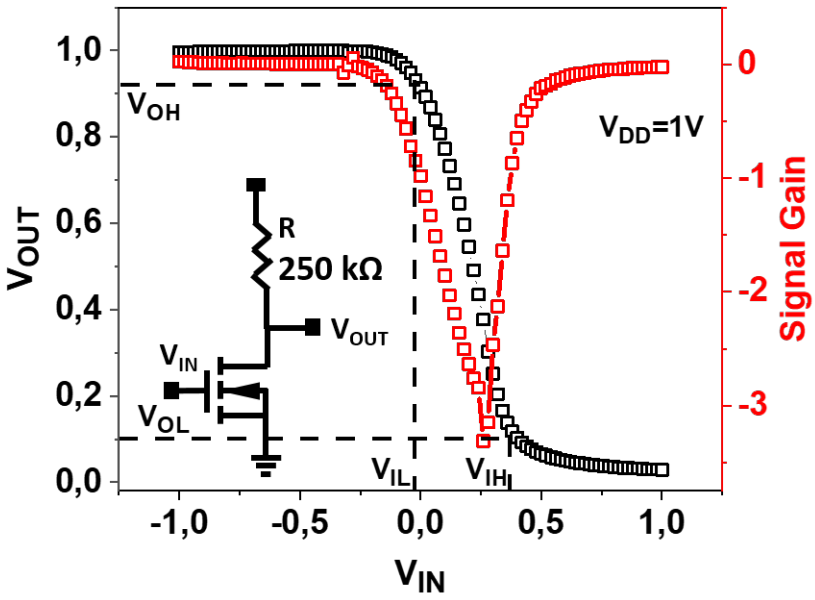

Figure 6.9.: The DC characteristics of the printed inverter. The schematic of the inverter circuit can be seen in the inset. The calculated peak signal gain is 3.5. Reproduced with permission from Wiley[135]

The maximum signal gain, dV_{OUT}/dV_{IN} is a major determining factor for an inverter and demonstrates the sharpness of the transition between the high and low output voltage regions. Therefore a gain higher than 1 is preferred. For the fully printed inverter, the gain is calculated to be 3.5 at a switching threshold potential (V_{IN}=V_{OUT}) of 0.25 V. The device performance in this study is similar to the reported values that use lithography processes to fabricate circuits in TRL[137].

The noise margins are calculated from the inverter output characteristics using the following Equation 6.3

$$NM_H = V_{OH} - V_{IH}$$

where V_{OH} is the minimum high output voltage and V_{IH} is the minimum high input voltage. The high noise margin, NM_H is calculated as 140 mV

$$NM_H = V_{OH} - V_{IH} \tag{6.2}$$

$$NM_L = V_{IL} - V_{OL} \tag{6.3}$$

where V_{IL} is the maximum low input voltage and V_{OL} is the maximum low output voltage. The low noise margin, NM_L is calculated as 50 mV. The noise margins are plotted later in the transient analysis for understanding of the device performance.

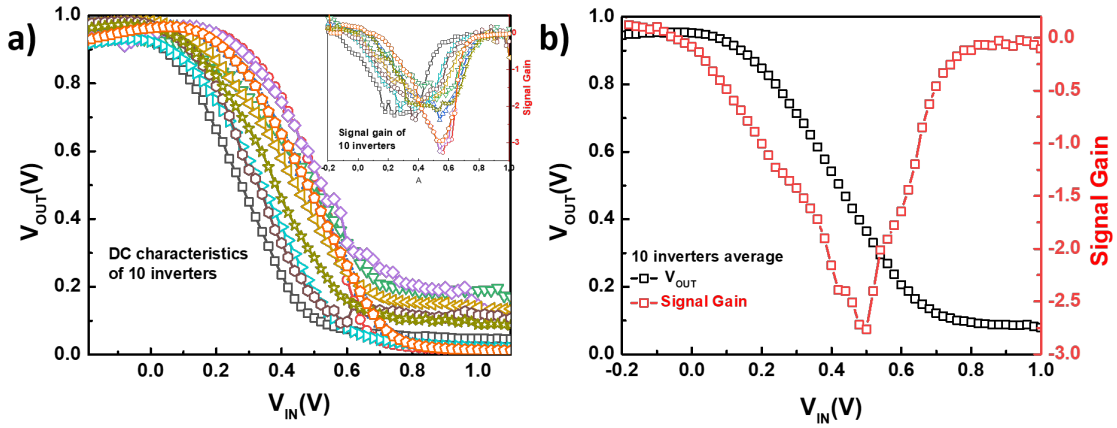

Figure 6.10.: Statistics of the DC characteristics of ten fully printed inverters. Reproduced with permission from Wiley[135]

As every component of the inverter is printed, certain non uniformities need to be accounted for. The variations arise mainly from the printing. The semiconductor dimensions, semiconductor overlap by electrodes and electrode overlap by the electrolyte play a role in the variations. Other variations that arise are from the lower switching speeds offered by the fully printed devices, especially with graphene offering higher parasitic capacitances. These variations however can be capped within a range and the reproducibility demonstrated by fully printing ten inverters of matching dimensions. Figure 6.10 a depicts the output characteristics of ten fully printed inverters and the inset shows the calculated signal gain for them. The inverters function at switching thresholds between 250 and 400 mV and exhibit a signal gain between 2.5 and 3.5.

The transient properties of the inverter at a frequency of 1 Hz are measured for 10 s as seen in Figure 6.11 a. Between 1 s and 2 s, the fall time (t_{fall}) is calculated as the time difference between 90% to 10% of the output voltage values and the rise time (t_{rise}) calculated between 10% to 90% of second half of the output value. The rise and fall times are denoted by the vertical dotted lines in the Figure 6.11 b and are estimated as 100 ms and 120 ms respectively.
The noise margins measured from a -1 slope in the DC characteristics are calculated to

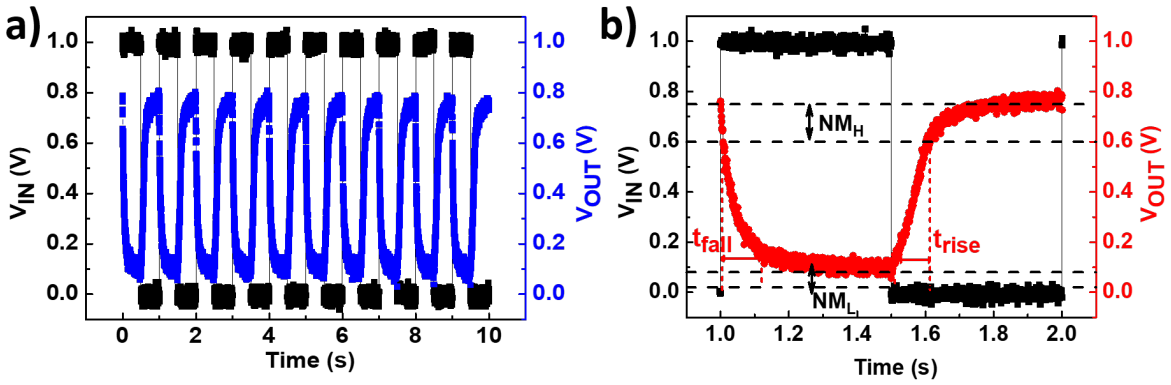

Figure 6.11.: Printed, flexible Inverter Transient Characteristics. a) Extended transient characteristics for 10 s b) The transient properties of the printed inverter on flexible substrate at 1 Hz. Fall (t_{fall}) and Rise (t_{rise}) in a time period of 1s are denoted by vertical red dotted lines. The V_{IN} is pulsed from 0 to 1 V and V_{DD} is 1 V (black rectangular pulses). The noise margins for the high and low levels are depicted by the horizontal black dotted lines. Reproduced with permission from Wiley[135]

be 140 mV in the high level (NM_H) and 50 mV in the low level (NM_L) region. Ideally, equal NM_H and NM_L are desired but NM_H is larger. However, the noise margin is big enough, meaning that the inverter is immune to noise and stable with respect to signal interference.
The propagation delay calculated as a difference between 50% of input and output curves amounts to 30 ms for the fully printed inverters. The inverter is potentially suitable for fully printed circuit applications.

6.4. Mechanical and Temporal Characterization

The mechanical stability of the devices was determined by performing bending and stretching tests to measure the tensile strain on the devices. This is performed over a period of more than four weeks and the stability over time is exhibited.

6.4.1. Mechanical stability

The substrate thickness (ε_{sub}) is 125 μm, the oxide film thickness (t_{ox}) is 200 nm and the bending radius (r) is 4.5 mm resulting in a tensile strain of 1.5% which is consistent with state of the art developments. As shown in Figure 2.17, the bending is divided into zones A, B and C where A and C zones are not subjected to fatigue but zone B is subjected to fatigue. Elongation or stretching on the other hand acts on every area of the substrate. Hence, complementary to the bending tests, stretching tests on the oxide film were conducted as well.

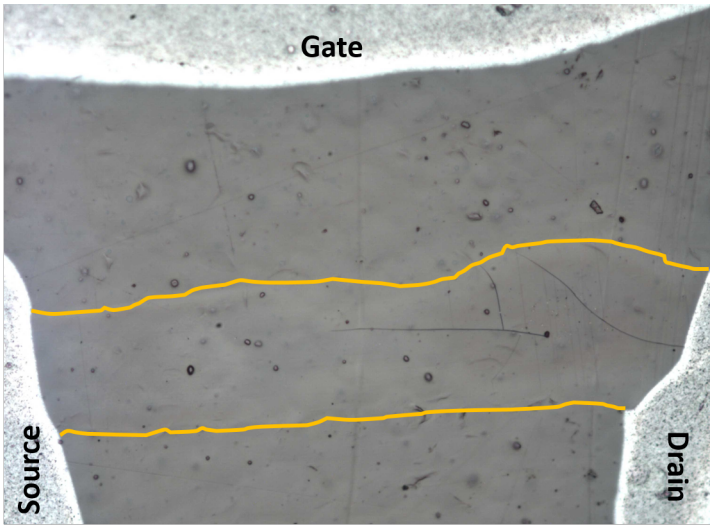

Figure 6.12.: Tensile strength test of the oxide film before printing electrolyte. The applied strain is 1.5% and crack formationcan be seen in the right top corner of the oxide film, whereas the graphene electrodes are intact.

Since the oxide film is highly adhesive to the substrate owing to van der waals and interfacial forces, it is certain that the oxide film is as well subjected to stretching. This is evident since the oxide film begins to crack slightly upon an applied strain of greater than 1.5% (Figure 6.12). However, it should be noted that the graphene electrodes and resistors show no sign of cracks and remain intact.

$$strain = \frac{\varepsilon_{\text{sub}} + t_{\text{ox}}}{2r} \tag{6.4}$$

The bending tests are performed for over 200 cycles at a radius of 4.5 mm and the threshold voltage, the mobility of the transistor are measured (Figure 6.13). A constant inverter signal gain is observed throughout the bending cycles indicating that the inverter performance is stable as long as the polycrystalline oxide film is intact. The slight lowering and rise of the gain could be due to the contact resistances arising from the placement of the source measure unit (SMU) needles of the probe station. The inset figure shows printed inverters on a PI film.

6.4.2. Temporal stability

Temporal stability tests are conducted as well, to determine the lifetime of the inverters. The output characteristics over four weeks are plotted in Figure 6.14 and indicate a shift of the slope but with no significant trend. This can be attributed to the variations in contact resistance that differ with each new measurement. The threshold voltage is shifted, meaning that charges are trapped at various interfaces. This could also be due to the inconsistent shift in the threshold voltage of the printed transistors[138] with time as the ion mobility in the electrolyte gets affected with drying.

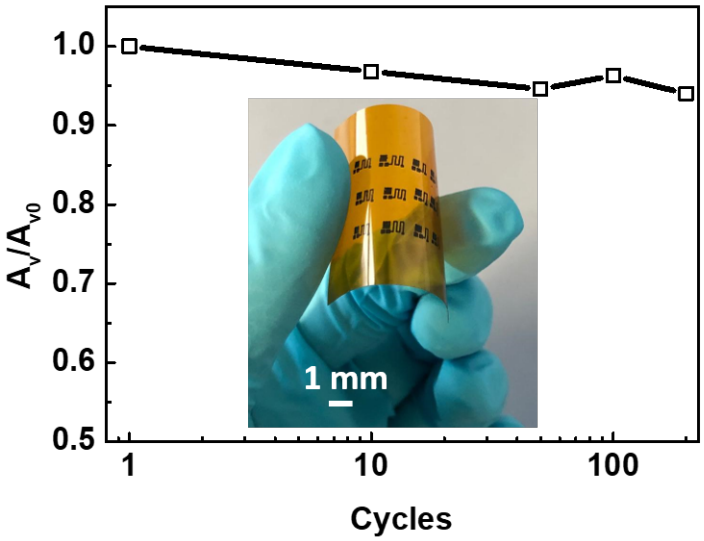

Figure 6.13.: The mechanical and temporal stability of the printed oxide transistors. a) The signal gain of the inverters normalised with the initial value remained constant over 200 bending cycles. In the inset, is an image of the devices on the flexible substrate before printing the electrolyte. Reproduced with permission from Wiley[135].

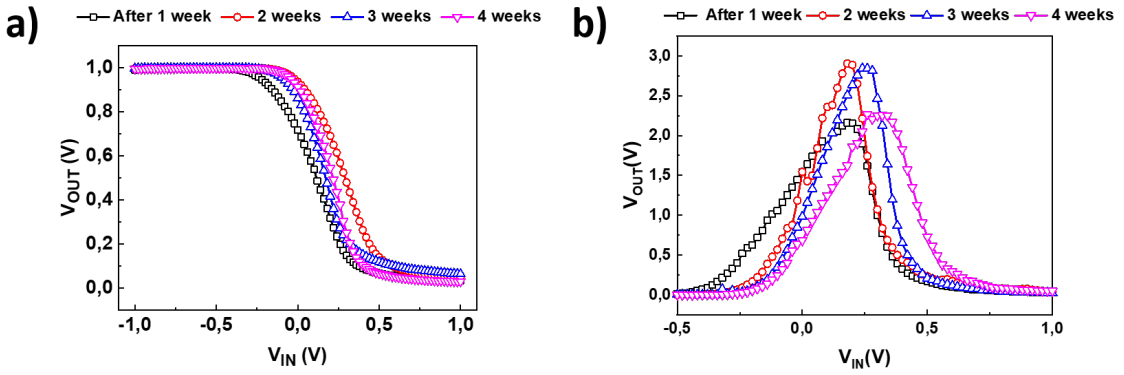

Figure 6.14.: Stability of the printed inverters as a function of time, measured over 4 weeks throughout which, a) Output voltage remained largely similar. b) Signal gain remained constant.

The propagation delay remains constant throughout, as observed in the transient properties in Figure 6.15. However, the inverters reach to lower maximum output voltage through second and third weeks and reach the initial maximum. This is probably due to the variations in ambient conditions, namely humidity during storage.

In summary, fully printed oxide-based inverters in transistor-resistor logic have been fabricated on flexible polyimide substrate. The lithography process used in the state of

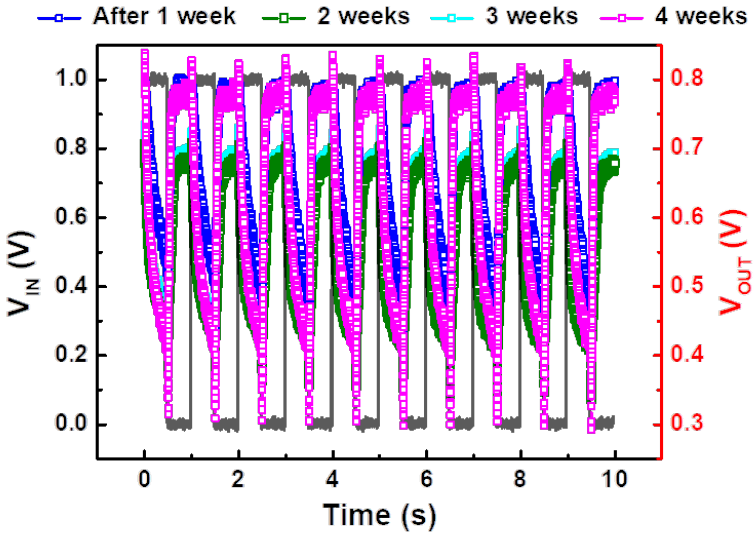

Figure 6.15.: Temporal Consistency of Inverter Transient Characteristics.

Material	Substrate	Fabrication	Logic	Signal Gain	Delay (ms)	Ref
TIPS-PEN	Arylite^{TM}	Ink-jet Printing	TTL	5.5	0.44	[139]
sc-SWCNT	PET	ALD, Lithography, Inkjet Printing	TTL	33	0.06	[140]
TIPS-Pentacene	Polycarbonate	Screen Printing, Slot Casting	TTL	9	-NA-	[141]
In_2O_3	Glass	Lithography, Ink-jet Printing	TTL	21	-NA-	[23]
ZnO	Flexible SiO_2	Lithography, Doctor Blading	TTL	21	0.06	[142]
In_2O_3	Glass	Lithography	TRL	4	2.3	[143]
In_2O_3	Kapton^{HN}	Ink-jet Printing Microplotting	TRL	3.5	30	This work

Table 6.1.: Comparison of results of the present work with state-of-the-art

the art methods is replaced by direct printing, which simplifies the fabrication of passive structures on polymer substrates. The printed flexible transistors exhibited a threshold voltage of 0.2 V and I_{on}/I_{off} value of 10^6. A resistor load of 250 - 400 kΩ is printed to fabricate the transistor-resistor logic gate in form of an inverter. Multiple inverters are

printed and the output characteristics lie well in the printed variation proving that the devices are reproducible. A signal gain upto 3.5 is observed and the average signal gain of the ten inverters is 3. Propagation delay of 30 ms is observed for the printed flexible inverters while exhibiting decent mechanical endurance and temporal stability. The propagation delay can be further improved by more controlled device dimensions and architecture and increasing the conductivity of the printed graphene passive electrodes. Considering the drop-on-demand printing techniques used in this study, this can be advanced into high-throughput digital fabrication of printed and flexible electronics. For better understanding the performance of the printed and flexible inverters in this work, a comparison with state-of-the-art printed inverter logics is shown in table 6.1.

7. Room Temperature Processing of Transistors

The development of fully printed metal-oxide inverters on flexible substrates paves the way for the fabrication of electronics on plastics that are used in daily life such as polyethylene terphthalate (PET) or polyethylene naphthalate (PEN). Even though polyimides are very flexible and has high thermal tolerance, developing electronics on PET/PEN is preferred since they are cheaper, transparent, find usage in daily life such as packaging/bottling and also have a possibility to be derived from plants. Printing on PET/PEN is similar to printing on PI substrate since their roughness (0.02 - 0.04 μm) is similar to the roughness of Kapton® HN, which has a roughness of 0.042 μm. Untreated PEN, like PI, has a contact angle of 75 °[84] and falls in the stable contact angle range[133]. However, unlike PI, PEN has low glass transition temperature (about 200 °C[20]) which is lower than the processing temperature of the indium oxide precursor. As a result, various studies that use nanoparticulate inks of indium oxide have resulted in the development of EGTs on PEN[144, 23]. Stable inks are developed by using a polymer binder which is eliminated using chemical or physical separation after printing. Notwithstanding the high temperature required, development of oxides from precursors would be cheaper and results in denser films, aiding high mobility in the metal-oxides. To ensure plausibility on PET/PEN, the processing temperature for indium oxide formation should be reduced. In this regard, few reports focused on self-combustion solution[19], far-UV annealing[145] and rapid photonic curing[146] among other methods.

7.1. Ink Development for Photonic Curing

7.1.1. Self combustion mixture

In the self-combustion method, a fuel and oxidizer are added to the precursor. After a threshold temperature is applied to the solution, the oxidizer activates the fuel inside the solution, leading to an internal combustion and provides the energy required for the formation of metal-oxide bonds. The internal energy would mean that the applied temperature is lower and therefore can be used on a PEN substrate. The internal energy is released through an exothermic process thanks to the reduction of activation energy of the reactants as seen in Figure 7.1. As seen in the figure, the activation energy of the solution with fuel (E_a) is lower than the activation energy of the reactants without fuel (E_{a1}). This leads to a negative ΔG (Gibbs free energy difference of products and reactants) which is indication of an exothermic reaction. The addition of fuel takes the initial free energy to higher levels. Without the fuel, the reaction is endothermic and

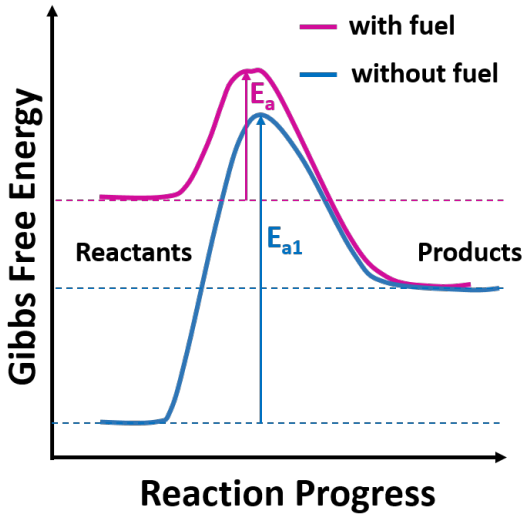

Figure 7.1.: Gibbs free energy of reactants comprised of indium nitrate precursor increases with the addition of acetylacetone fuel. The activation energy reduces and products form with the supply of lesser external energy.

higher temperatures need to be applied for the reaction to happen. The combustion films still require externally applied temperatures of 250 - 350 °C[147] and hence, combustion solution alone is insufficient to synthesise metal-oxide electronics on PET/PEN. In this regard, UV assisted or rapid photonic curing can be employed.

7.1.2. Photonic sintered indium oxide

UV assisted curing uses energy from a UV source (10 nm - 300 nm) in order to reduce the thermal energy required to form metal-oxide. The UV light is absorbed by the oxide precursors to decompose into metal-oxide which is assisted by the heating of the substrate to about 150 °C. The UV absorption by the precursors is selective and requires long times ranging from 30 minutes to 3 hours for decomposition to take place. To reduce the processing time further, rapid photonic annealing is engaged. This processing can be easily transferred to roll-to-roll processing. A comprehensive comparison of processing times and possible temperatures reached is given in table 7.1. Among all the curing methods, rapid photonic annealing is very fast and also very suitable for PEN substrate since the substrate will only be heated to 75 °C.

In rapid photonic curing, high energy pulses of light generated by a flash lamp or laser are absorbed by a thin metallic layer which absorbs the photons and converts the light energy into vibrational energy. These lattice phonons are excited as thermal energy, which is transferred to the precursor deposited on top of the metallic layer. Thus the precursor decomposes into metal-oxide. The temperature rise occurs within a very short time, as seen in Figure 7.2. The metal layer absorbs the photons, translates the energy into thermal energy, which is transferred to the oxide precursor. In this process, the PEN substrate is

Curing method	Material	Processing time (min)	Temperature (°C)
Thermal	precursor	120 - 200	300 - 500
Chemical	nanoparticles	10	RT - 100
Photonic	aqueous precursor	1.5	not measured
UV-Vis/UV-Laser	nanoparticles	0.15	not measured
Thermal	self-combustion precursor	30 - 120	150 - 350
Rapid photonic	precursor	< 0.0015	200 (precursor) 75 (substrate)

Table 7.1.: Processing Time and Temperature for Curing Methods of Metal-Oxides

unaffected and at the same time, the precursor is subjected to temperatures as high as 600 °C within less than 5 ms. The substrate does not heat to more than 150 °C.

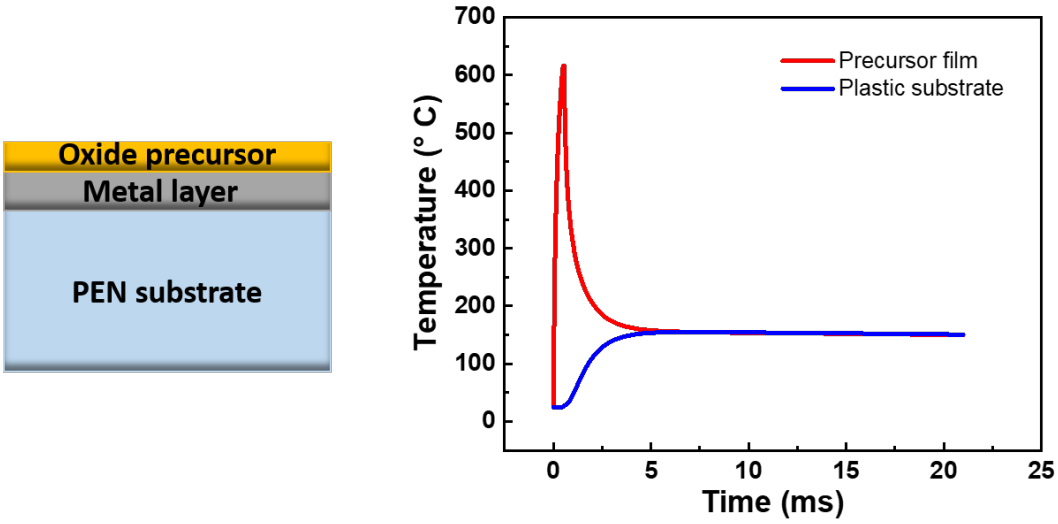

Figure 7.2.: Temperature profile of oxide precursor on PEN. On the left is the cross sectional schematic of oxide precursor on PEN with metal layer in between. Right is the temperature graph. Precursor reaches 600 °C and substrate reaches only 150 °C

In this context, since the temperature rise is only for few milliseconds, a combustion mixture would lead to better distribution of temperature in the precursor film. The fuel gets activated by the sudden rise in the temperature and this could trigger the combustion, thereby crossing the activation energy barrier. An x-ray diffraction (XRD) pattern on a self-combustion solution photonically cured for 20 ms can be seen in Figure 7.3. The peaks are indexed and match very well with the peaks observed for indium oxide. This is a qualitative proof for the decomposition of nitrate precursors into metal-oxides in the proposed curing method. Thus, pure indium oxide can be fabricated within no time from combustion precursors using rapid photonic curing. In contrast, photonically sintered precursor solution without the presence of a combustion fuel requires 90 s to obtain a

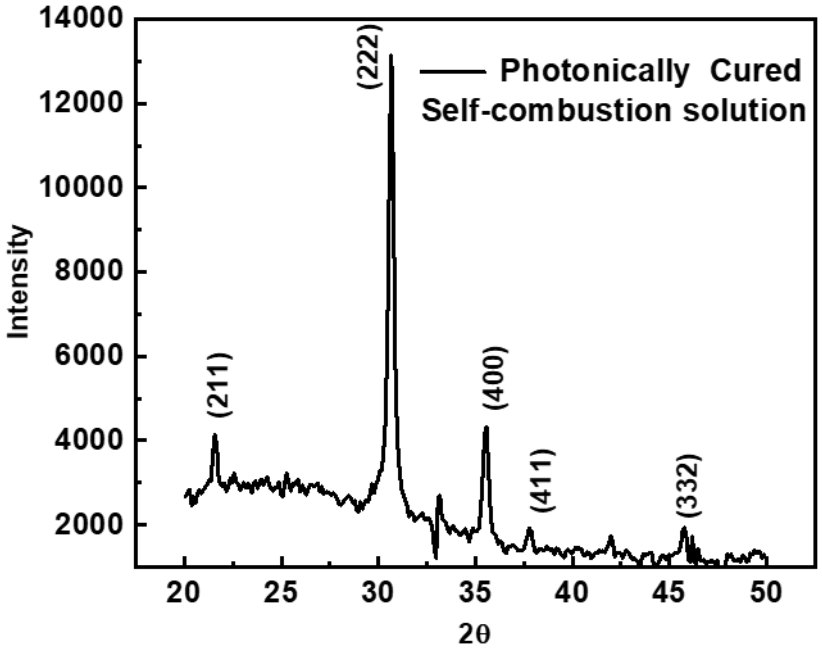

Figure 7.3.: XRD performed on the photonically cured self-combustion based precursor confirms the presence of indium oxide pure phase. Indium oxide peaks are indexed in the graph.

pure indium oxide phase[23]. The longer exposure to the high energy pulses leads to the melting of the PEN substrate whereas the 20 ms exposure in this work heats up the PEN substrate to a maximum of about 150 °C, and below the glass transition temperature of the substrates. The short heat burst ignites the fuel and the nitrate oxidizer assists in the self combustion of the precursor, thereby leading to the decomposition into oxide very rapidly.

7.2. Electrolyte-Gated Transistors

The processed indium oxide is tested for its applicability in electrolyte gated transistors fabricated on a PEN substrate. The self combustion precursor solution is deposited across metal electrodes to first study the semiconductor functionality. The idea can then be easily transferred into a fully printed scenario.

7.2.1. Fabrication

Since the absorption of photons and the reflection of the energy pulses is high at the surface of metals like chromium and aluminium, the passive elements such as the source, drain and gate electrodes are fabricated by thermally evaporating chromium onto a PEN substrate. The self combustion precursor is prepared by dissolving 0.05 M $In(NO_3)_3$ in 5

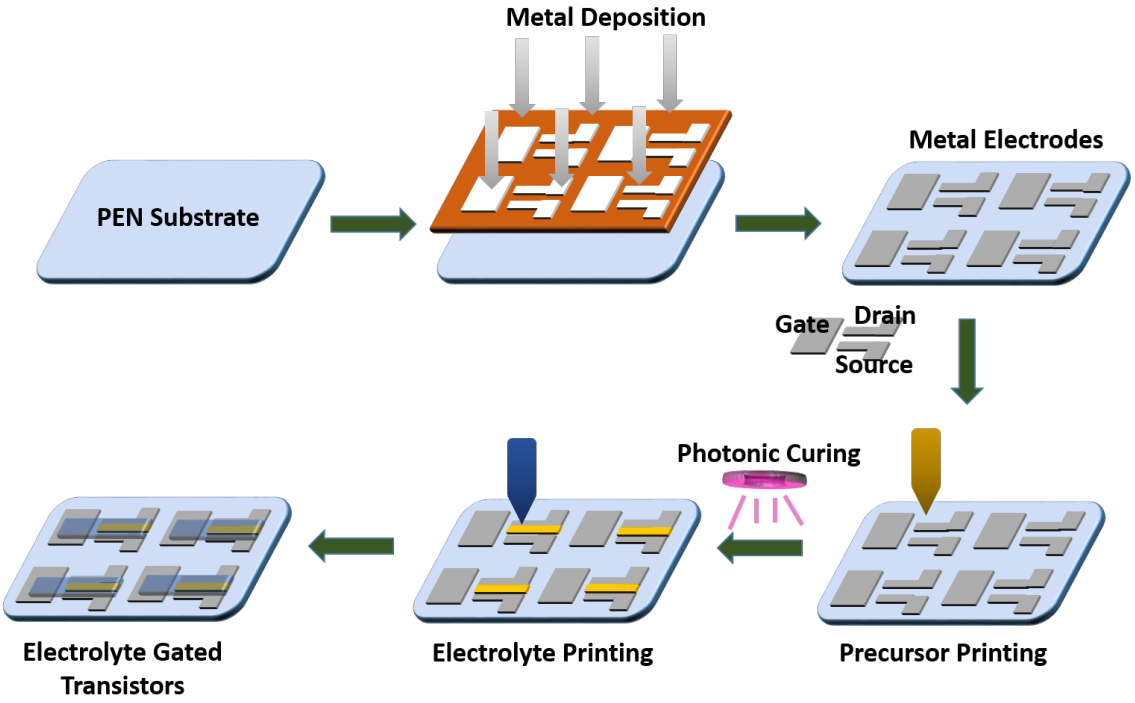

Figure 7.4.: Fabrication of Self Combustion Precursor based EGTs on PEN Substrate. Starting from the left - Transparent PEN substrate is covered with a mask through which metal electrodes are deposited. Self combustion precursor is printed across source and drain, followed by subjection to photonic curing. CSPE is later printed across the gate and the processed oxide to achieve EGTs.

mL of the solvent in which 0.2 mL is acetylacetone, the combustion fuel. The precursor is deposited across the source and drain using an Optomec aerosol-jet printer. The width and length of the printed precursors are 1000 μm and 100 μm respectively (W/L = 10). The printed precursor is then photonically cured using a single pulse of 20 ms width. CSPE is printed as the electrolyte across the semiconductor and the gate to fabricate EGTs. A pictograph depicting the detailed fabrication process can be seen in Figure 7.4. The cross section of the printed device is observed using an SEM micrograph. Continuous interfaces are clearly seen between the electrode-semiconductor-electrolyte.

7.2.2. Electrical performance

Transfer characteristics of the transistors fabricated on PEN assisted by rapid photonic curing can be seen in Figure 7.5 a and the output characteristics in Figure 7.5 b. The on-off ratio is 10^5 and is similar to the printed devices in which the oxide was formed by temperature annealing. The threshold voltage is calculated by extrapolating I_{DS} in linear region to the x-axis and the subthreshold swing is calculated near the threshold voltage in the log-scale of I_{DS}. The threshold voltage value is 0.07 V, which places the device in enhancement mode. Subthreshold swing is 150 $mVdec^{-1}$, which is larger than the transistors printed on glass and polyimide. This could be a result of charge trap density at

the electrolyte-ambient/substrate interface and requires further investigation. The very negligible hysteresis (clockwise) is an indication of the low electron traps at the defects occurring in the semiconductor-electrolyte interface. The mobility is calculated from the drain conductance and the defining parameter $\mu_{\text{lin}}C_{\text{DL}}$ is calculated as 870 μFV^{-1}s^{-1}. Considering the capacitance value of 35 μFcm^{-2} as calculated using cyclic voltammetry[136], the device mobility is 25 cm^{2}V^{1}s^1. This value exceeds the one obtained on glass or polyimide because of the high conductivity of the lithographically patterned chromium electrodes.

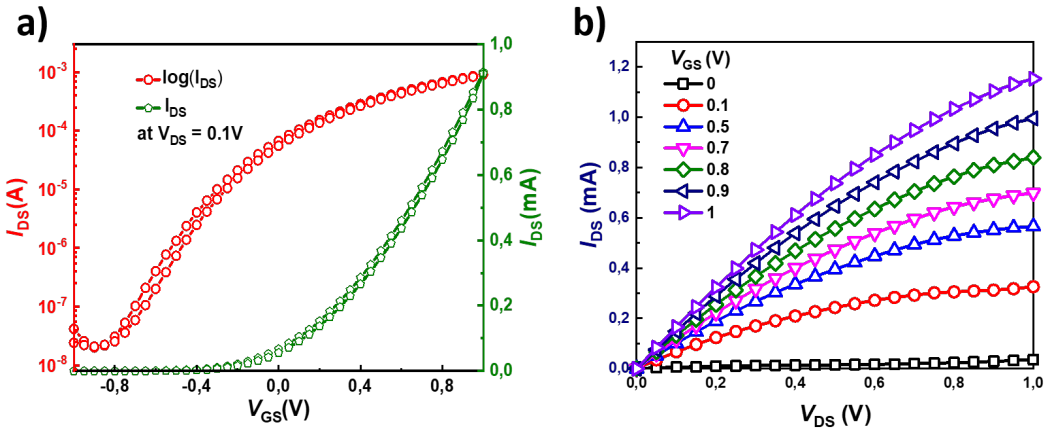

Figure 7.5.: Electrical Characterization of Self Combustion Precursor based EGTs on PEN Substrate. a) Transfer characteristics in linear regime. b) Output I_{DS} vs V_{DS} curves at different V_{GS}.

Therefore, rapid photonic curing can be used to fabricate EGTs and since photonic curing is harmless to the PEN substrate because of the metal layer protection, transistor fabrication on PEN is feasible using this method.

Part IV.

Summary and Outlook

8. Summary

Printed electronics is a young field being developed in complementary to conventional silicon electronics. The approach of printed electronics can be utilized to fabricate electronics where high performance is not required but is desired on flexible or transparent substrates such as on a PET substrate (Figure 8.1). Printing is attractive because of the ease of circuit design with digital drop-on-demand techniques which allows the fabrication of a variety of electronic devices through just one click, instead of physically changing a multitude of components such as photoresists and masks. Therefore to develop flexible electronics where ultrahigh performance is not an defining parameter, it makes sense that each and every component of an electronic circuit is printed.

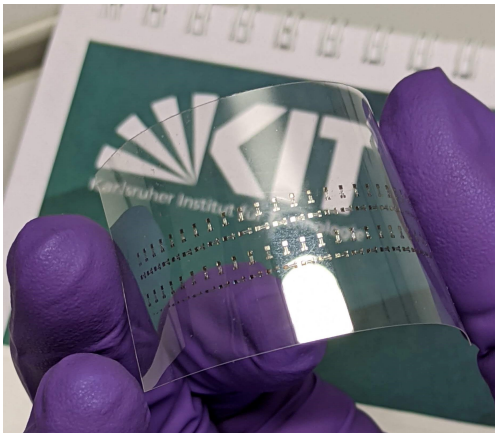

Figure 8.1.: Electrolyte gated transistors printed on transparent PET substrate.

So far, the field of printed electronics has seen significant development in the printability of many materials, namely semiconductors, conductors and insulators. Also, their applicability in diodes, solar cells, resistors, antennae, capacitors and transistors has been proved. In the search for a good n-type inorganic semiconductor, inkjet printed polycrystalline indium oxide has intrinsic mobility values that exceed 100 $cm^2V^{-1}s^{-1}$. Using a composite solid polymer electrolyte (CSPE) as gate insulator facilitated device operations lower than 2 V, which is compatible with printed batteries and energy harvesters. Electrolyte gated transistors (EGTs) fabricated using indium oxide and CSPE exhibited a device mobility of 126 $cm^2V^{-1}s^{-1}$. Lithographically patterned ITO electrodes are typically utilized in such works.
In this thesis, the patterned ITO electrodes are replaced with printed conductive graphene ink. The electrical performance of the EGT is optimized by ensuring physical and chemical compatibility through morphological and electrochemical studies. The device architec-

ture is designed based on the difference between printed graphene and indium oxide in parameters such as roughness, work function and annealing temperature. Graphene is also observed to be chemically stable in presence of the CSPE and resulted in very low gate leakage currents. With a channel length of 150 μm and width of 60 μm, the fully printed EGT on glass substrate exhibits high on-off ratio of 10^5, a subthreshold swing of 120 mVdec^{-1} and a threshold voltage of 0.23 V, which indicates that the device is an 'enhancement-mode' device. This especially makes it interesting for building inverters and other logic gates. The switching time for the planar devices is calculated to be 220 ms. When PEDOT:PSS is printed as the top-gate, significant improvement is observed in the switching time, which reduced to 80 ms. Additionally, the on-off ratio increased to 10^6 and the subthreshold swing reduced to 80 mVdec^{-1}, which is very close to the theoretical limit of 60 mVdec^{-1}.
The device mobility is a defining parameter for the fully printed EGT and is calculated in the linear region of the device transfer characteristics after correcting for the contact resistance between indium oxide and graphene. The calculated contact resistance in the EGT is 33 Ωcm, which is orders lower compared to dielectric gated transistors. A required parameter is the double-layer capacitance, which is calculated on the EGT by making the three terminal device into a two terminal device (source and drain are shorted). The capacitance is measured as 35 μFcm^{-2} using cyclic voltammetry and corroborated by impedance measurements. The device showed mobility values upto 16 cm^{2}V^{-1}s^{-1}, which is much higher than state-of-the-art fully printed transistors and similar to the ones fabricated on rigid substrates.
The fully optimized printed EGT is then printed on a polyimide (PI) Kapton substrate. PI is chosen primarily for its thermal stability, since the oxide precursor is heated to 350 °C. Since the PI substrate is different from the glass substrate in terms of surface energy and roughness, it is treated accordingly and contact angle measurements of the indium oxide precursor are performed. The contact angle is about 65 °and lies in the most stable region for drop formation and crack-free oxide films are formed on the PI substrate. The subsequent flexible EGTs on the PI exhibited current on-off ratio of 10^5, subthreshold swing of 100 mV dec^{-1}, threshold voltage of 0.2 V and device mobility of 12 cm^{2}V^{-1}s^{-1}. These values are similar to the ones observed for the fully printed EGTs on glass.
Inverters are made using a transistor resistor logic (TRL) because of the lack of p-type oxide semiconductor that has performance similar to n-type indium oxide. Graphene is printed as the resistor in the TRL inverter after executing a loadline analysis on the device i-v characteristics. A load of 250 kΩ is chosen and interestingly, graphene with its 20,000 S/m conductivity is best suited for this. To achieve similar resistance values with silver ink, a line of 10 meters needs to be printed. The TRL inverters exhibit a signal gain of 3.5, which is similar to the inverters prepared on rigid substrates using the same logic. The propagation delay amounts to 30 ms and rise and fall times are estimated to be 100 ms and 120 ms respectively. The noise margins at the high and low level are significantly large, ensuring a comfortable functioning of the inverter. Overall, the TRL based fully printed inverter can certainly find applications in complex circuits.
There is limited state-of-the-art on the flexibility of the printed oxide films which were so far printed on rigid substrates. The mechanical flexibility and the tensile strength of the EGTs printed on PI is therefore studied using bending and stretching studies. The oxide

films can withstand a tensile strain upto 2% which is high for oxide films but can still be improved. Additionally, these inverters are found to be highly reproducible and function stably over many weeks.
The printed and flexible devices are then prepared on cheaper substrates such as PET/PEN. Since PET/PEN have lower glass transition temperatures compared to glass and PI, they are not subjected to thermal curing but are subjected to photonic curing instead. Formation of the indium oxide precursor is feasible at the same time unaffecting the polymer substrate because the metallic electrodes absorb the photons and heated the precursor on top and thermally protected the substrate at the bottom. The formation of the indium oxide is proved using x-ray diffraction and the fabricated EGTs exhibited a mobility of 25 $cm^2V^{-1}s^{-1}$, which is significantly higher than the devices obtained using thermally annealed oxide.
In conclusion, fully printed EGTs being compatible with printed batteries usher in new interesting flexible electronic applications with requirements of low to medium performance. With the low power consumption of the TRL logic, printed and flexible oxide electronics potentially break ground for new applications such as flexible displays, electronic skin and bio-mimicking.

9. Outlook

In future, it would be interesting to fully print circuits on PET/PEN substrates. The development of a TRL inverter on flexible substrate can be translated into a ring oscillator, which is a signature for the application of the EGT in circuit technology. Ring oscillators consist of an odd number of inverters connected in series and output of the last inverter is connected to the input of the first. With application of a 'supply voltage,' the ring oscillator begins to oscillate with the frequency that is defined by the delay at each inverter stage. The propagation delay, τ_P is given by the following Equation 9.1 in which f is the measured frequency of the ring oscillator that consists of 2α+1 number of stages and α is a constant.

$$\tau_P = \frac{1}{2(2\alpha + 1)f} \tag{9.1}$$

The following Figure 9.1 shows a three stage ring oscillator. Three stages indicates three inverters out of which the first inverter is part of a NAND-gate. This allows the switching off the oscillations into on and off. By turning on V_{Enable}, the ring oscillations start, which is called the active state. Otherwise, the ring oscillator is in a constant state. The inverters are constructed using a TRL as can be seen, which makes the fully printed version possible.

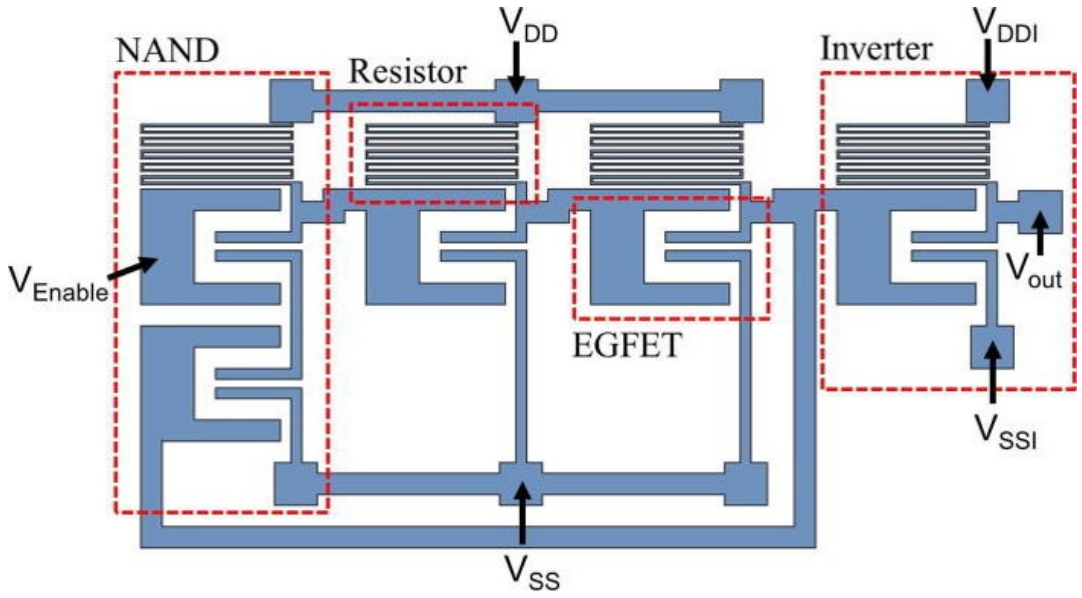

Figure 9.1.: Layout of a Three Stage Ring Oscillator. Reproduced with permission from AIP[143]

The challenge, however, would be the interconnects. Silver cannot be used as all the passive structure, including the electrodes and the interconnects, since it could react with

the electrolyte. Moreover, silver cannot be used as the resistor component, since it is highly conductive. Therefore a hybrid between silver and graphene, or a different printable ink for example, made of semi metal such as graphite could be used. If silver and graphene combination is used, then again, the physical, chemical and electrical interface between silver and graphene requires attention. Given the 30 ms propagation delay observed in the flexible inverters, ring oscillators that function at few kHz can be expected, which paves the way to printing of more complex electronic circuits on flexible plastic substrates.

Part V.

Appendix

A. Supplementary Material

A.1. Understanding p-type Semiconductor

In contrast to the n-type semiconductor in which the majority charge carriers (electrons) are situated in the conduction band, the majority charge carriers in a p-type semiconductor are holes and are situated in the valence band. The acceptor level (E_A) is situated closer to the valence band since the effective mass of the valence band (E_V) is way more than that of the conduction band (E_C). Therefore, the fermi level (E_F), that is the energy level through which the charge carriers conduct is situated close to E_V.

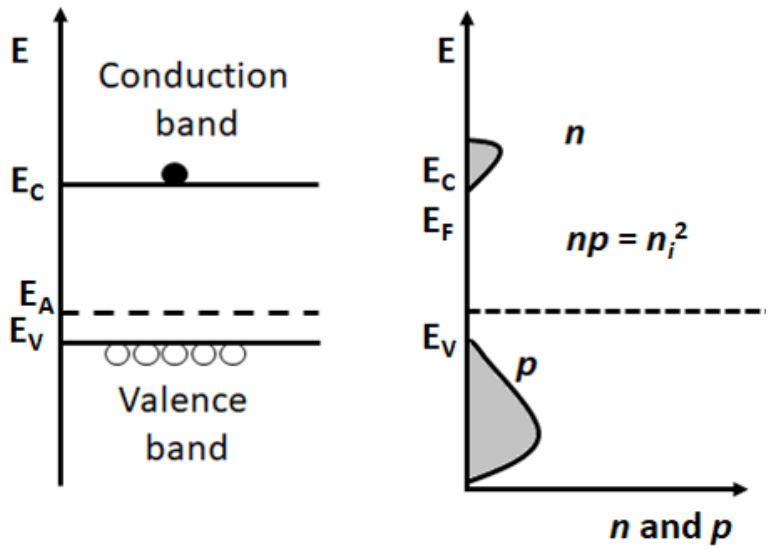

Figure A.1.: P-type doping of a semiconductor. Intrinsic semiconductor has equal number of electrons and holes. The fermi level lies in the middle of the bandgap. Addition of electron acceptor increases the hole concentration and the fermi level shifts towards the valence band.

A.1.1. Rectifying contacts with p-type semiconductor

As seen in section 2.3.1, the difference in the work functions lead to rectifying contact between the semiconductor and the connected metal. For a n-type semiconductor rectifying contacts arise when the metal work function is greater than the semiconductor. In p-type semiconductors, the opposite is true. Therefore, as shown in figure A.2 when (E_{FS}) is

greater than (E_{Fm}), for hole diffusion from semiconductor into metal, a potential (V_0 = $q(\phi_m$-$\phi_s)$) needs to be applied. This makes the contact a rectifying p-type contact.

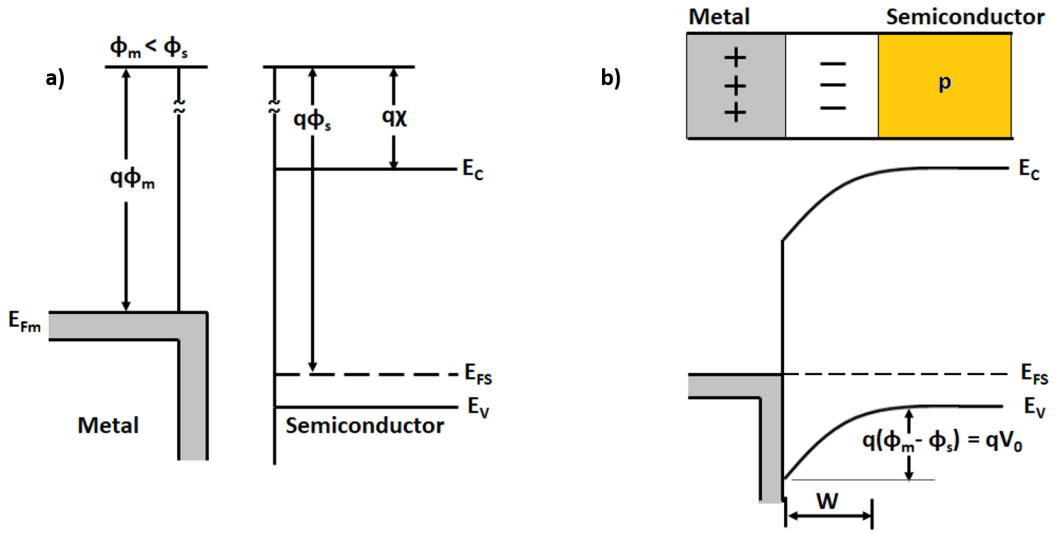

Figure A.2.: Rectifying contact occurs when metal work function is lesser than semiconductor. A depletion layer with minority charge carriers is formed at the junction.

A.2. Indium Oxide Thickness and Conductivity

The thickness of the indium oxide is measured using a surface profilometer (Dektak 32) and is observed to be 175 nm for the two printed layers. The thickness of the inkjet printed indium oxide based on precursor can be seen in figure A.3. Within a length of 100 μm, the thickness rises upto 175 nm.

For a square shaped oxide film, the resistance value is calculated in the range of MΩ to GΩ, using van der Pauw method.

A.3. Graphene Thickness

The thickness of the microplotted graphene is measured to be 300 nm for a width of 150 μm as seen in figure A.4. This cross-section (A) is consistently used to calculate microplotted graphene resistance (R = $\rho\frac{l}{A}$), where l is the length of the printed line and ρ is the resistivity.

A.4. FTIR Studies

The fourier transform infrared spectroscopy (FTIR) studies performed on the graphene ink as the printed film is heated from RT to 300°C is shown in figure A.5.

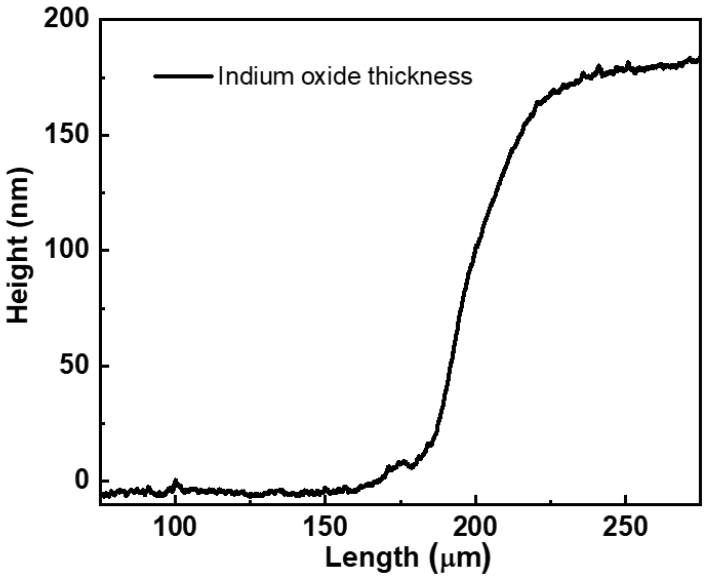

Figure A.3.: Thickness of Precursor based Indium Oxide Annealed at 400°C

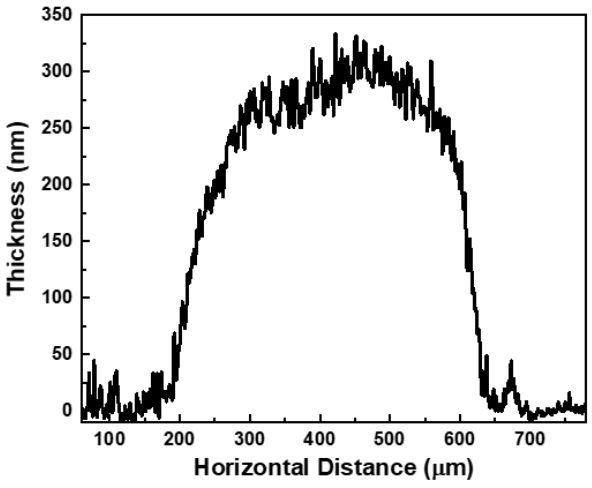

Figure A.4.: Printed graphene thickness

A.5. Measurement Reliability Factor

To assess the behavior of the increase of conductivity with carrier density under constant mobility, a recently proposed parameter, the experimental reliability factor[128], is calculated for the fully printed transistors. This factor specifies the ability of the printed device to deliver current in accordance to the applied voltages, with a value

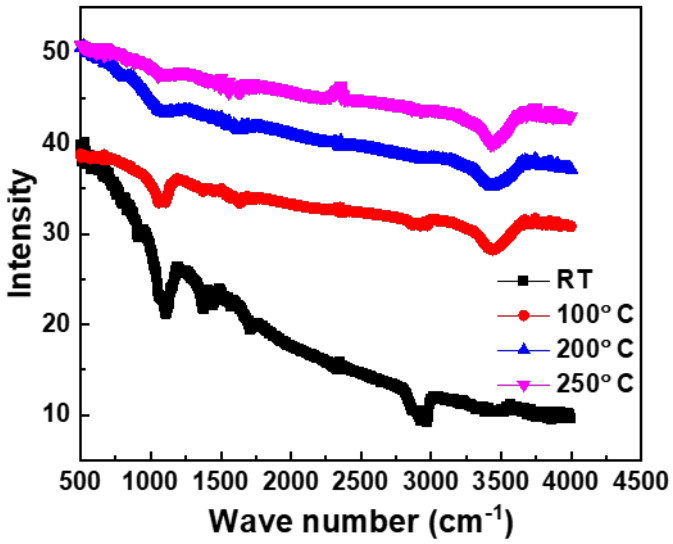

Figure A.5.: FTIR spectra of graphene films heated from room temperature to 250°C (bottom to top). Signal near 3000 cm^{-1} vanishes with temperature and peak at 1100 cm^{-1} reduces significantly with temperature.

of 1 for the ideal transistor. In the linear regime, the experimental reliability factor (r_{lin}) is calculated to be 0.66 using the difference between the drain current, $|I_{DS}|^{max}$ at $|V_{GS}|^{max}$, 1 V and the drain current, $|I_{DS}|^{0}$ 0 V. The formula used to calculate r_{lin} is given in equation A.1. The results can be seen in table A.1.

$$r_{\text{lin}} = \left(\frac{|I_{\text{DS}}|^{\text{max}} - |I_{\text{DS}}|^{0}}{|V_{\text{GS}}|^{\text{max}}}\right)/\left(\left|\frac{\partial I_{\text{DS}}}{\partial V_{\text{GS}}}\right|\right)_{\text{claimed}} \tag{A.1}$$

Channel dimension, W/L	Mobility, μ_{lin} ($cm^2V^{-1}s^{-1}$)	Reliability factor (r_{lin})
1	2.7	0.73
0.8	2.6	0.86
0.6	10.8	0.67
0.4	16	0.66
0.2	17.6	0.66

Table A.1.: Reliability of Device Performance in Accordance with [128]

Part VI.

Index and References

List of Figures

List of Tables

List of Abbreviations

IoT Internet of Things

RFID Radio Frequency Identification

PET Polyethylene Terphthalate

PEN Polyethylene Naphthalate

EGT Electrolyte-Gated Transistor

FET Field-Effect Transistor

TRL Transistor-Resistor Logic

TTL Transistor-Transistor Logic

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MBE Molecular Beam Epitaxy

ALD Atomic Layer Deposition

MIS Metal Insulator Semiconductor

2D Two Dimensional

VBM Valence Band Maximum

CBM Conduction Band Minimum

NEGT n-type Electrolyte-Gated Transistor

PEGT p-type Electrolyte-Gated Transistor

SS Subthreshold Swing

RT Room Temperature

DOD Drop On Demand

SEM Scanning Electron Microscope

AFM Atomic Force Microscope

FTIR Fourier Transform Infra Red

CV Cyclic Voltammetry

EIS Electrochemical Impedance Spectroscopy

TLM transmission Line Method

PI Polyimide

EG Ethylene Glycol

DC Direct Current

SMU Source Measure Unit

UV Ultra Violet

XRD X-Ray Diffraction

PVDF Polyvinylidene Flouride

PTFE Polytetrafluoroethylene

EC Ethyl Cellulose

rpm Rotations per Minute

CSPE Composite Solid Polymer Electrolyte

ITO Indium Tin Oxide

Ag Silver

DMSO Dimethyl Sulfoxide

PVA Polyvinyl Alcohol

ZnO Zinc Oxide

IZO Indium Zinc Oxide

IGZO Indium Gallium Zinc Oxide

Si Silicon

Cd Cadmium

PEDOT:PSS Poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate)

Li Lithium

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Part VII.

Personal Details

Personal Data

Education

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Feb. 2017 - present	Graduate researcher, Hahn group Institute of Nanotechnology, KIT, Germany
Jan. 2016 - May. 2016	Masters Thesis, SEST University of Hyderabad, India
Apr. - Jun. 2013,14	Summer research scholar, Indian Academy of Science

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Fellowships and Grants

MERAGEM Graduate School *Feb 2017 - present*
Graduate Fellowship

Fellowship from the Ministry of Science, Research and Arts of Baden Württemberg for the fellowship of the graduate school for research in printed electronics

Karlsruhe Institute of Technology/DAAD *Nov 2019*
DAAD Grant

Grant to extraordinarily committed doctoral researchers for academic and social commitment

Karlsruhe House of Young Scientists *Oct 2019 - Dec 2019*
Research Travel grant

KIT grant to travel abroad to conduct research in the University of Minnesota for three months.

Optical Society of America *Jul 2019*
Conference Travel grant

Received travel grant from the Optical Society of America to attend IONS'19 conference in Barcelona

Indian Academy of Sciences *May 2013 & May 2014*
Student Fellowship

Received fellowship consecutively for two years to travel to and conduct research in any laboratory across India during summer

Conferences and Workshops

Oral Presentations

- **Singaraju, S.A.**; Siddhartha.; Bhattacharya, S.S.; Hahn, H.; Breitung, B. Inkjet Printing of Cu_2ZnSnS_4 Absorber Layer for Application in Thin Film Photovoltaics and Other Electronic Devices, *OSA - IONS'19, Barcelona*, Jul 2019.
- **Singaraju, S.A.**; Aghassi-Hagmann, J.; Hahn, H.; Breitung, B. Fully Printed Electrolyte-Gated Field-Effect Transistors and Logics, *EMRS Spring Meeting, Nice*, May 2019.
- **Singaraju, S.A.**; Aghassi-Hagmann, J.; Hahn, H.; Breitung, B. Fully Printed Electrolyte-Gated Field-Effect Transistors, *NanoVision, Zurich*, Feb 2019.
- **Singaraju, S.A.**; Baby, T.T.; Kruk, R.; Aghassi-Hagmann, J.; Hahn, H.; Breitung, B. Graphene Electrodes for Fully-Printed Electrolyte-Gated Field-Effect Transistors, *LOPE-C, Munich*, Mar 2018.
- Singaraju, S.A.; **Baby, T.T.**; Kruk, R.; Aghassi-Hagmann, J.; Hahn, H.; Breitung, B. Solution processed hybrid field effect transistors based on graphene electrodes, *Deutsche Physikalische Gesellschaft, Berlin*, Mar 2018.

Poster Presentations

- Baby, T.T.; Chandresh, A.; **Singaraju, S.A.**; Breitung, B.; Hahn, H. Printed Electronics, *POF, Karlsruhe*, Sep 2018.
- Baby, T.T.; Chandresh, A.; **Singaraju, S.A.**; Breitung, B.; Hahn, H. Synthesis and characterization of graphite oxide based ink for printed transistors, *Deutsche Physikalische Gesellschaft, Berlin*, Mar 2018.

- **Singaraju, S.A**.; Krishna, M.G. Characterization of Cu_2ZnSnS_4 Thin Films for Solar Cell Applications, *FIP, Hyderabad*, Mar 2016.

- **Singaraju, S.A**.; Paidi, V.K.; Ramamoorthy, R.K.; Bhatnagar, A.K. Investigation of Structural Variation and Physical Properties of Heavy Metal Oxide Tellurite Glasses, *ISGFM, Guntur*, Dec 2015.

Invited Talks and Publications

Invited Talks

University of Duisburg, Germany *July 2020*
Printed electronics on plastic substrates using low temperature processed metal oxides

Leibniz Institute for New Materials, Germany *July 2019*
Towards Low Temperature Processed Printed Electronics

University of Hyderabad, India *April 2019*
Printed Electronics: Made in Garage

Select Peer-reviewed Publications

Google Scholar Surya Abhishek Singaraju

Feng, X.; **Singaraju, S.A**.;.....;Aghassi-Hagmann, J. (**2021**). Low-frequency Noise characteristics of Inkjet-Printed electrolyte-gated thin-film transistors incorporating indium oxide semiconductor, *IEEE EDL*.

Singaraju, S.A.; Marques, G.C.; Gruber, P.; Kruk, R.; Hahn, H.; Breitung, B.; Aghassi-Hagmann, J. (**2020**). Fully Printed Inverters using Metal-Oxide Semiconductor and Graphene Passives on Flexible Substrates, *PSS Rapid Research Letters*.

Singaraju, S.A.; Baby, T.T.; Neuper, F.; Kruk, R.; Hahn, H.; Aghassi-Hagmann, J.; Breitung, B. (**2019**). Development of Fully Printed Electrolyte-Gated Oxide Transistors using Graphene Passive Structures, *ACS Appl. Electron. Mater*.

Jeong, J.; Marques, G.C.; Feng, X.; Boll, D.; **Singaraju, S.A**.; Aghassi-Hagmann, J.; Hahn, H.; Breitung, B. (**2019**). Ink-jet Printable, Self-assembled, and Chemically Crosslinked Ion-gel as Electrolyte for Thin Film, Printable Transistors, *Adv Mat. Int.*

Neuper, F.; Chandresh, A.; **Singaraju, S.A**.; Aghassi-Hagmann, J.; Hahn, H.; Breitung, B. (**2019**). Tailoring Threshold Voltages of Printed Electrolyte-Gated Field-Effect Transistors by Chromium Doping of Indium Oxide Channels, *ACS Omega*.

Marques, G.C.;...; **Singaraju, S.A**.....; Aghassi-Hagmann, J. (**2019**). Fabrication and Modeling of pn-Diodes Based on Inkjet Printed Oxide Semiconductors, *IEEE EDL*

Book Chapters

Printing Technologies for Integration of Electronic Devices and Sensors, *2020*
Functional Nanostructures and Sensors for CBRN Defence and Environmental Safety and Security
Functional Nanostructures and Sensors for CBRN Defence and Environmental Safety and Security, Springer

Active Materials for Printed Inorganic Electronic Devices, *post processing*
Handbook of Printed Electronics, Springer

Others

Reviewed several scientific publications for IoP, ACS, RSC, Wiley and IEEE journals

Two publications selected as cover page articles by ACS and Wiley

Under Preparation

Singaraju, S.A.; Lemmer, U.; Hahn, H.; Breitung, B.; Aghassi-Hagmann, J. (**2020**). Room Temperature Processing of Oxide Transistors on Polyethylene Terephthalate Substrates using Rapid Photonic Curing.

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