Mirror Source based Overcurrent and Short Circuit Protection Method for High Power SiC MOSFETs

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Abstract

This paper presents a fast overcurrent and short circuit protection based on the mirror source detection method for 1200 V/1200 A Silicon Carbide (SiC) MOSFETs used in a high power Dual Active Bridge (DAB). It will be shown that this protection method is feasible for a low inductive short circuit caused by a half bridge shoot through, a high inductive short circuit based on a failure inside the load as well as short circuits of Type 1 or hard switching fault. Additionally, the short circuit behaviour is analyzed for different junction temperatures of the MOSFETs. Experimental results proof that using the investigated method always ensures the operation in the Short Circuit Safe Operating Area (SCSOA) of the MOSFET after triggering short circuits.

1 Introduction

Silicon Carbide (SiC) power semiconductors provide several advantages in comparison to conventional silicon devices. Among others, SiC has a 10-times higher breakdown field strength and thereby allows thinner chips which results in lower conduction losses [1]. Furthermore, switching speeds of SiC MOSFETs are faster and switching losses are reduced accordingly. Consequently, SiC power modules allow more efficient and compact power-electronic converters [2].
Due to the low chip thickness and the absence of a desaturation effect, the short circuit of SiC MOSFETs is more difficult to handle compared to IGBTs. Whereas silicon IGBTs usually allow short circuit withstand times of a few 10 µs, the withstand time in SiC power devices is only a few microseconds [3]. Additionally the turn off current slope of the short circuit current is much higher than for normal operation. For this reason a soft turn off might be considered to reduce the overvoltage spike and to ensure operation in Short Circuit Safe Operation Area (SCSOA). The soft turn off, however, further increases the turn off losses. At the same time, different short circuit scenarios have to be handled: the low- and high-inductive short circuit of the load as well as the hard switching fault (HSF) also called Type 1 short circuit. For HSF the MOSFET is turned on directly into the short circuit [4]. To overcome this hurdle, the investigated SiC MOSFET module by Mitsubishi Electric provides the so-called Real Time Current Control (RTC), a mirror source based overcurrent detection and current limiting circuit which can be combined with a short circuit protection.

2 Mirror Source Based Overcurrent Detection and RTC

To detect the overcurrent and short circuit event, a current mirror is integrated in the MOSFET chip and conducts a certain fraction of the total source current. This scaled-down current is used to detect the short circuit. This mirror source or mirror emitter concept for short circuit detection has already been applied to silicon and SiC devices before [5] [6] [7]. Compared to state of the art detection methods, like desaturation techniques [8] [9], this solution can detect both Type 1 and Type 2 short circuits while being significantly faster. To reduce the turn off time and stress on the device the mirror source detection can be combined with the RTC. As soon as a short circuit is detected the RTC reduces the gate voltage inside the power module immediately to limit the

current rise and therefore simplifies the short circuit turn-off.

The simplified schematic of the RTC and the driver circuit is shown in Fig. 1. The simplified waveforms in case of a short circuit are depicted in Fig. 2. At $t = t_0$ the short circuit occurs and the current is increasing with a much higher steepness than usual. The short circuit threshold for $i_\mathrm{D} = i_\mathrm{D,th}$ is reached at $t = t_1$. During $t_1 < t < t_2$ the detection circuit (SC Detect) is reacting to the short circuit. During $t_2 < t < t_3$ the bipolar transistor Q1 is turned on by the detection circuit and reduces the gate voltage V_GS according to the voltage divider consisting of R_G, R_RTC and the diode D_RTC. The resulting gate voltage is given in Eq. (1) and is typically in the range from 3 V to 6 V.

$$V_\mathrm{GS} = \frac{R_\mathrm{RTC}}{R_\mathrm{RTC} + R_\mathrm{G}} \cdot (V_\mathrm{Driver} - V_\mathrm{f,Drtc} - V_\mathrm{Q1}) + V_\mathrm{f,Drtc} + V_\mathrm{Q1} \tag{1}$$

The reduction of the gate voltage brings the MOSFET into the active region and limits the current. This is shown between $t_2 < t < t_4$. Additionally the turn on of the transistor Q1 reduces the voltage at the feedback pin SC of the MOSFET to V_Q1 and the error feedback circuit can detect that signal to react to the fault. The reaction time from t_3 to t_4 should be below 3 µs and represents the reaction time of the gate driver.

At $t = t_4$ the gate driver output is switched to open circuit and the gate capacitance C_iss is discharged by the passive discharging resistors and R_RTC which finally results in $V_\mathrm{GS} = 0\,\mathrm{V}$. At this point the MOSFET is turned off and the current ceases to $i_\mathrm{D} = 0\,\mathrm{A}$. An error feedback to the superordinate control system turns off the whole converter at $t = t_5$ to achieve a safe state.

In the following, practical results are presented using a 1200 V, 1200 A Full-SiC power module FMF1200DX1-24A with built-in RTC by Mitsubishi Electric.

3 Gate Driver Circuit

The gate driver is divided into three main functional groups, which can be seen in Fig. 1, the power

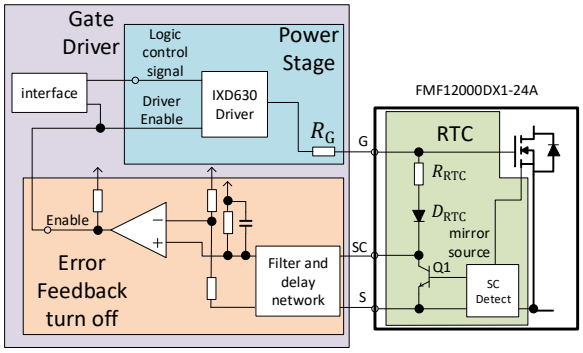

Fig. 1: Simplified Gatedriver and RTC circuit

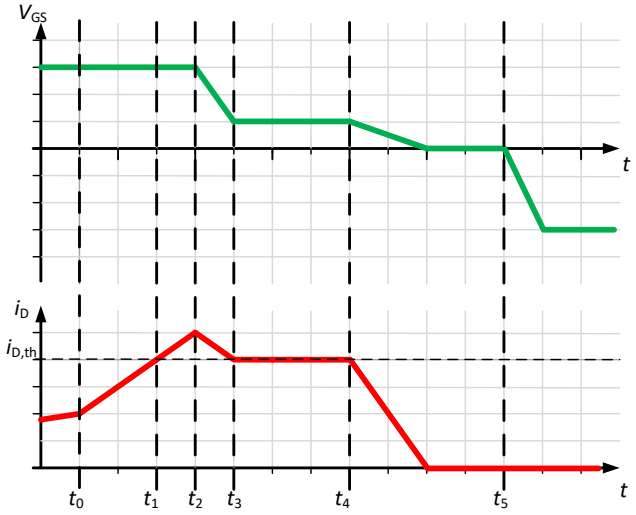

Fig. 2: Simplified waveforms for RTC short circuit protection

stage, the error feedback and error turn off and the communication interface with the superordinate control. The power stage consists of a push-pull power amplifier MOSFET driver and the gate resistor R_G which has to be designed according to Eq. (1) and the switching behaviour of the MOSFET in normal operation. The communication interface of the gate driver is implemented using fiber optics to reduce electromagnetic interference (EMI) in converter applications and consists of the control signal and the error feedback signal. A simplified circuit diagram of the error feedback and error turn off circuit is shown in Fig. 1. As discussed in the previous chapter, the SC pin is high level for normal operations and zero in case of an error. This signal is detected, filtered to prevent false error detection due to EMI, as well as delayed to increase the turn off time for

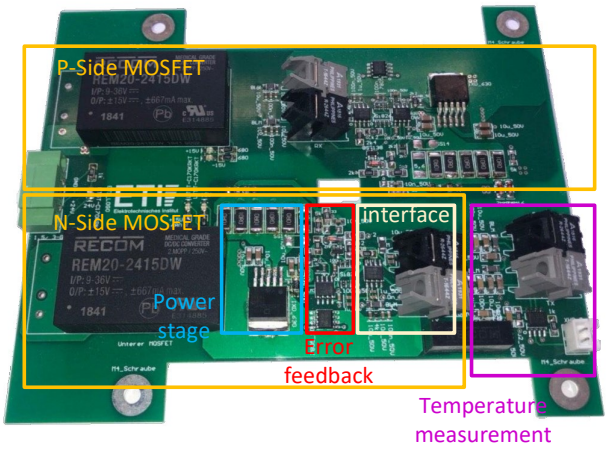

Fig. 3: Gate Driver for FMF1200DX1-24A half bridge with error feedback and soft turn off

reduced component stress if necessary. The filtered signal is compared to a defined reference level by using a comparator circuit. The output of the comparator enables or disables the power stage to achieve a high resistance output for the power stage. This enables the discharging process of the gate capacitance C_{iss}, with help the of the RTC resistor R_{RTC} and a high ohmic passive discharging resistor, as mentioned in the previous chapter. At the same time a feedback signal is sent to the superordinate control to disable the converter. All signals are implemented as logic low in case of an error to prevent critical failures. The resulting printed circuit board (PCB) is shown in Fig. 3.

4 Converter Turn Off in Case of High Inductive Load Short Circuit

After triggering a short circuit turn off at one MOSFET the converter has to be turned into a safe state to prevent further damage. The easiest way to do so is by turning off all MOSFETs of the full bridge as shown in Fig. 4 on the left-hand side for a high inductive load short circuit. This results in a free wheeling current through the DC-Link and the remaining inductance in series to the short circuit. After zero current crossing of the short circuit current i_{sc} the energy of the inductance is reduced until there is no energy remaining in the magnetic field of the inductance and the MOSFET body diodes are no longer conducting. Because of that the MOSFET capacitances C_{oss} are charged, which is shown in Fig. 4 and results in oscillations between the load inductance and the capacitances with the resonance frequency f_{res} calculated in Eq. (2). Figure 5 shows measurements with the simple converter turn off method. At the zero current crossing the voltage V_{DS}, V_{GS} and the current i_{D} at the observed MOSFET are oscillating. In the worst case, these oscillations have an EMI related impact on the corresponding gate voltages and can lead to failure or unexpected turn on of the MOSFETs.

$$f_{\mathrm{res}} = \frac{1}{2\pi\sqrt{C_{\mathrm{oss}} \cdot L_{\sigma}}} \tag{2}$$

To avoid this problem, it is possible to turn on one unaffected MOSFET having no error signal to provide a defined free wheeling path and to avoid the occuring oscillations between the output capacitances C_{oss} of the MOSFETs and the load inductance. This is shown in Fig. 4 on the right-hand side. In this case MOSFET T2 detects the short circuit and is turned off. All other MOSFETs are also turned off to prevent additional failure. After 2 µs MOSFET T1 is turned on again and provides the free wheeling path. This delay time is necessary to prevent additional short circuit detection and component stress. The results are shown in Fig. 6 for the same operation point. It can be observed that there are no oscillations after cut off of the current resulting in a safe state of the converter.

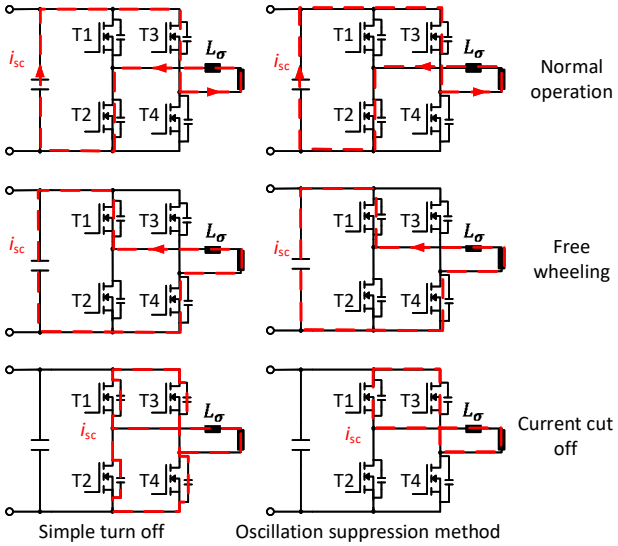

Fig. 4: Current Paths for the Converter turn off. left: simple turn off right: oscillation suppression method

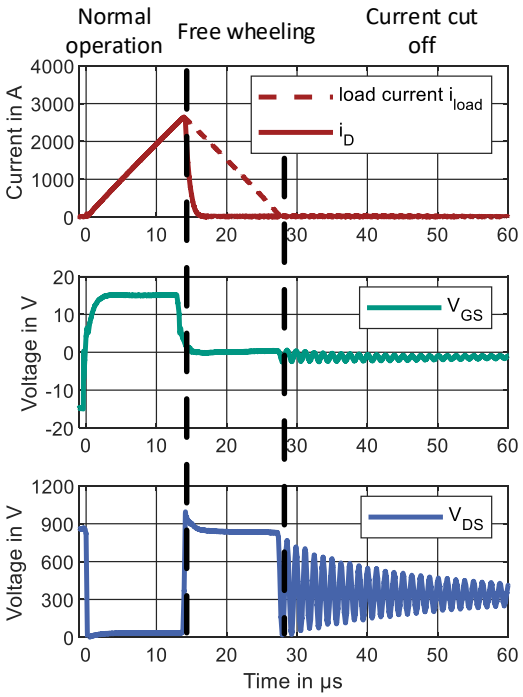

Fig. 5: Simple turn off strategy for $V_{\mathrm{DC}} = 850\,\mathrm{V}$

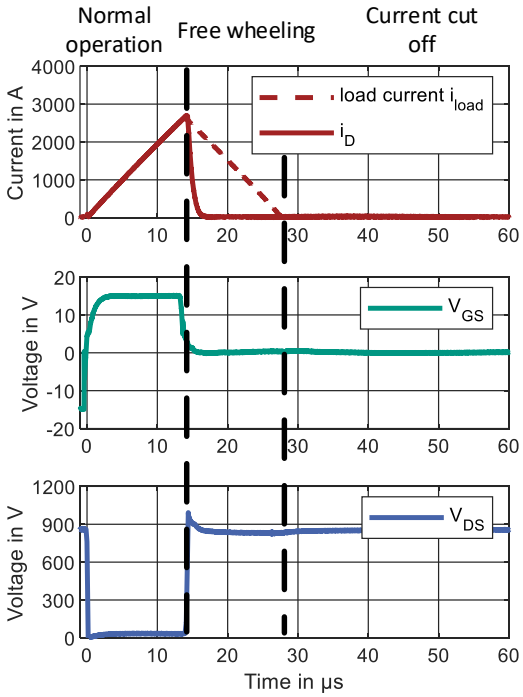

Fig. 6: Oscillation suppression method for $V_{\mathrm{DC}} = 850\,\mathrm{V}$

5 Experimental Setup

To measure both a high- and low inductive short circuit in a typical application, a full bridge configuration shown in Fig. 8 is used. This is a common setup for all kind of galvanic isolated DC/DC converter like the DAB or resonant LLC converter. The load consists of a Medium-Frequency-Transformer (MFT), which is shorted on the secondary side. The resulting stray inductance, consisting of the connection busbar and the MFT itself, is measured as $L_\sigma = 4.5\,\mu\mathrm{H}$. In order to measure at different junction temperatures, an oil tempered cooling plate is used. With this setup DC-Link voltages up to $V_{\mathrm{DC}} = 850\,\mathrm{V}$, short circuit currents of 5 kA and junction temperatures of up to 150 °C have been measured. The parameters of this measurement setup are adapted according to the requirements of a 500 kW DAB for which this study was made. The setup of the DAB is shown in Fig. 7.

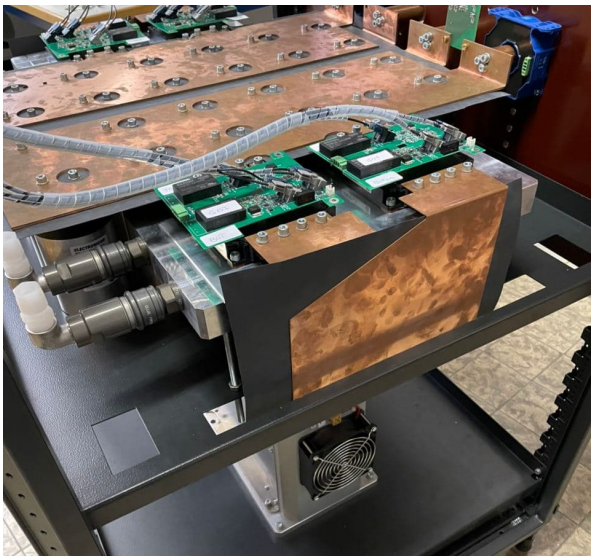

Fig. 7: Setup of the 500 kW DAB

Two basic short circuit situations, which differ in their inductive load, are tested. The first one is a high inductive short circuit which is caused by isolation faults on the load side of the system. An example for this short circuit is an isolation fault within the windings of the MFT and therefore is separated from the power electronics. This results in a high inductance between the DC-Link and the short circuit. Therefore, the resulting current

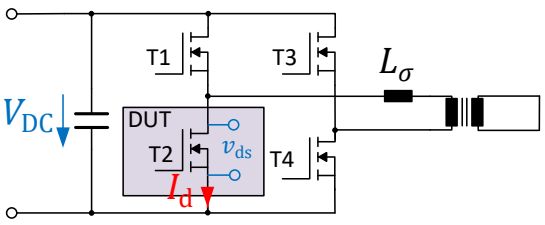

Fig. 8: equivalent circuit diagram of measurement setup

steepness is comparably low. Typical values of the inductances for such an short circuit are between $L_{\mathrm{sc,high}} = 1..5\,\mu\mathrm{H}$ in high power DAB applications. The second short circuit is the low inductive short circuit caused by a half bridge shoot through. This may result from controller malfunction or power module failure. In this case the inductance is in the range of few nH which results in a very high current steepness. Both scenarios can be emulated by using the MFT stray inductance with a short-circuited secondary winding and turning on both MOSFETs half bridge respectively.

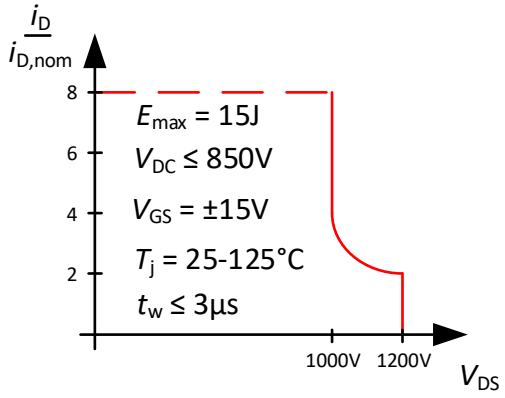

Fig. 9: Short circuit SOA curve defined for FMF1200DX1-24A

6 Experimental Results

To evaluate the performance of the short circuit detection and protection method proposed, the setup descriped in the previous chapter is used. The results are compared to the specified SCSOA shown in Fig. 9. The most important factors are the maximum short circuit drain current which is

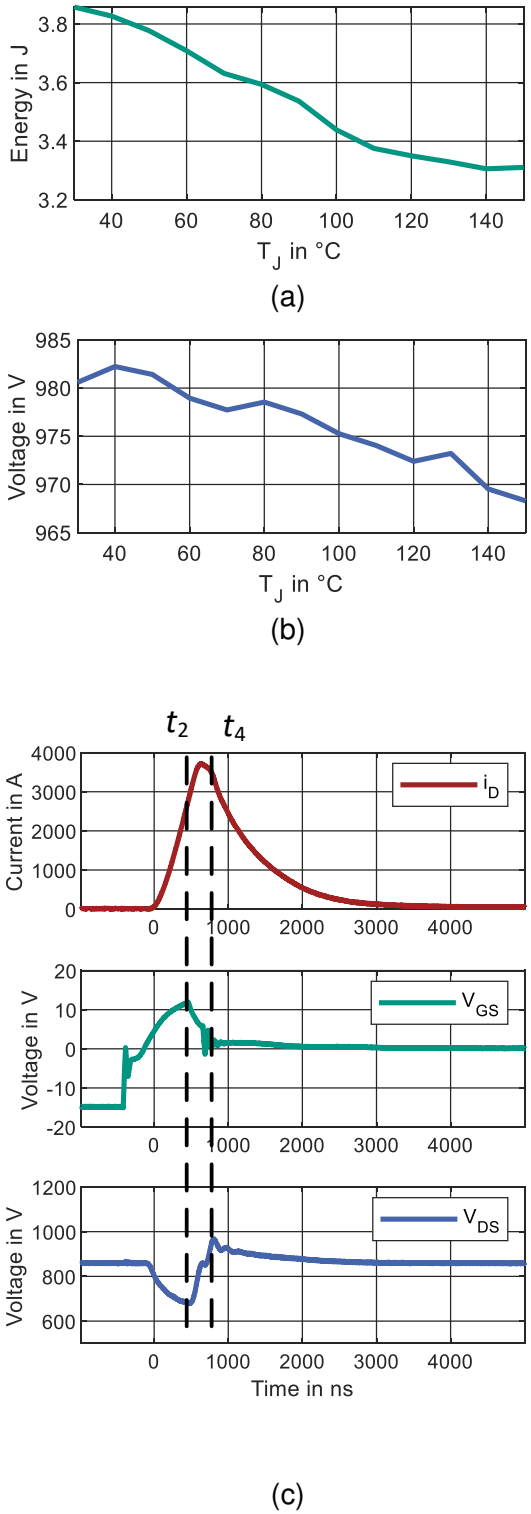

Fig. 10: (a) Measured pulse energy for 850 V low inductive short circuit (b) peak voltage $\hat{V}_{\mathrm{DS}}$ (c) waveforms at $T_{\mathrm{J}} = 150\,^{\circ}\mathrm{C}$

$i_{\mathrm{D}} < 8 \cdot i_{\mathrm{D,nom}} = 9.6\,\mathrm{kA}$ according to the used module. Another limitation is the short circuit withstand time t_{w} which has to be below $3\,\mu\mathrm{s}$. The

last important factor is the maximum loss energy for the turn off process which should not exceed $E_{\max} = 15\,\mathrm{J}$.

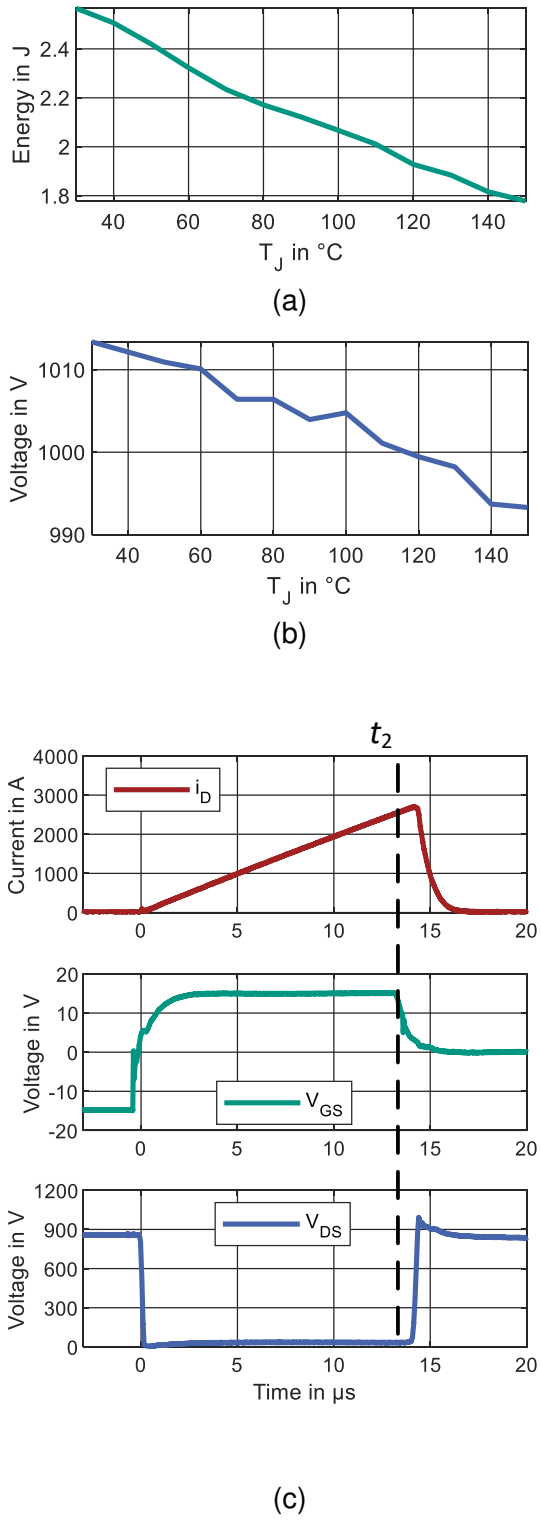

Fig. 11: (a) Measured turn off energy for 850 V high inductive short circuit (b) peak voltage $\hat{V}_{\mathrm{DS}}$ (c) waveforms $T_{\mathrm{J}} = 150\,^{\circ}\mathrm{C}$

Figure 10 (a) and (b) is showing the measurement results for the low inductive short circuit for $V_{\mathrm{DC}} = 850\,\mathrm{V}$ and Fig. 10 (c) for $T_{\mathrm{J}} = 150\,^{\circ}\mathrm{C}$. In Fig. 10 (a) the energy loss for the short circuit pulse is shown. The measured energy loss $E_{\mathrm{pulse}} \approx 1/4 E_{\max}$ is significantly lower than the maximum energy loss defined by the SCSOA. Moreover, the peak voltage $\hat{V}_{\mathrm{DS}}$ shown in Fig. 10 (b) is below 1 kV and therefore does not violate the SCSOA. In Fig. 10 (c) the experimental waveforms at $T_{\mathrm{J}} = 150\,^{\circ}\mathrm{C}$ are shown. The marked points are corresponding with the theoretical waveforms from Fig. 2. The reaction time of the gate driver is less than 250 ns after the detection of the short circuit and the short circuit is safely turned off after 2 µs and therefore does not violate the SCSOA. Since the reaction time is really low, the theoretical plateau of the gate voltage shown in Fig. 2 between t_3 and t_3 does not occur. The peak current is lower than the maximum current defined by the SCSOA.

Figure 11 shows the measurement results for the high inductive short circuit for $V_{\mathrm{DC}} = 850\,\mathrm{V}$ and Fig. 11 (c) for $T_{\mathrm{J}} = 150\,^{\circ}\mathrm{C}$. It can be observed that for the high inductive short circuit every parameter is inside the SCSOA in Fig. 9. Therefore both high and low inductive short circuit can be handled without damaging the module or violating the SCSOA.

7 Conclusion

In this paper, a fast overcurrent and short circuit detection and protection method based on a mirror source was described. The short circuit turn off was measured on a experimental setup for a 500 kW Dual Active Bridge (DAB) with a 1200 V/1200 A SiC MOSFET module. Two short circuit types are investigated, the low- and high inductive short circuit that can occur in DAB applications. Both measurements have shown that the short circuit safe operating area is not violated and the module is not damaged by the short circuit. Additionally, a converter turn off strategy was presented to prevent oscillations between the MOSFETs' output capacitances C_{oss} and the load inductance in case of a load short circuit.

8 References

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