Characterization and compact modeling of printed electrolyte-gated thin film transistors and circuits

Zur Erlangung des akademischen Grades eines

Doktors der Ingenieurwissenschaften (Dr.-Ing.)

von der KIT-Fakultät für Elektrotechnik und Informationstechnik
des Karlsruher Instituts für Technologie (KIT)

genehmigte

Dissertation

von

M.Sc. Xiaowei Feng

aus Shanghai, China

Tag der mündlichen Prüfung:	30.07.2021
Hauptreferent:	Prof. Dr. rer. nat. Ulrich Lemmer
1. Korreferentin:	Prof. Dr. rer. nat. Jasmin Aghassi-Hagmann
2. Korreferent:	Prof. Dr. Mehdi Baradaran Tahoori

Acknowledgments

I would like to sincerely thank my advisers, Prof. Jasmin Aghassi-Hagmann and Prof. Mehdi Tahoori, who continuously supported and encouraged me during my doctoral studies. I would also like to thank Prof. Ulrich Lemmer for acting as my first supervisor.

My biggest thank goes to Prof. Jasmin Aghassi-Hagmann for introducing me to the world of research. From her, I acquired most of the hard and soft skills during these four years of my Ph.D., which will be guiding me through life. Also, I am very thankful to Prof. Horst Hahn for the wonderful collaboration with his group.

I wish to show my appreciation to all my colleagues at the Karlsruhe Institute of Technology and the University of Applied Sciences Offenburg for their support. I wish to extend my special thanks to Dr. Christian Punckt for teaching me how to write and think scientifically. To Dr. Gabriel Cadilha Marques, I would like to thank him for inspiring new ideas and giving me guidance in the Lab. My thanks go also to Alexander Scholz, Dennis Weller, Surya Singaraju, Palak Gupta, Ahmet Turan Erozan and Farhan Rasheed for fruitful discussions.

Furthermore, I appreciate the assistance provided by undergraduate students Esha Jindal, Tongtong Fu and Hongrong Hu. I am also thankful to Ms. Siri Weiße and Ms. Iris Schröder-Piepka for their friendly support.

Words cannot express my gratitude to my family. Especially, I would like to my wife, Chang Zhang, for the endless support and encouragement. I owe so much thanks to my mother, Jie Ni, who is continuously supporting me throughout my life.

Finally, I would like to thank the Ministry of Science, Research, and Arts of the state of Baden Württemberg, Germany for their financial support to my research activities in the form of the MERAGEM scholarship as well as the German Federal Ministry of Education and Research (BMBF) through the project 2HORISONS.

Publication list

Journals

- **Feng, X.**, Singaraju, S. A., Hu, H., Marques, G. C., Fu, T., Baumgartner, P., Secker, D., Tahoori, M. B., and Aghassi-Hagmann, J. (2021). Low-frequency Noise Characteristics of Inkjet-Printed Electrolyte-gated Thin-Film Transistors. *IEEE Electron Device Letters, 42(6), 843-846.*
- **Feng, X.**, Scholz, A., Tahoori, M. B., and Aghassi-Hagmann, J. (2020). An Inkjet-Printed Full-Wave Rectifier for Low-Voltage Operation Using Electrolyte-Gated Indium-Oxide Thin-Film Transistors. *IEEE Transactions on Electron Devices, 67(11), 4918-4923.*
- **Feng, X.**, Marques, G. C., Rasheed, F., Tahoori, M. B., and Aghassi-Hagmann, J. (2019). Nonquasi-Static Capacitance Modeling and Characterization for Printed Inorganic Electrolyte-Gated Transistors in Logic Gates. *IEEE Transactions on Electron Devices, 66(12), 5272-5277.*
- **Feng, X.**, Punckt, C., Marques, G. C., Hefenbrock, M., Tahoori, M. B., and Aghassi-Hagmann, J. (2019). Impact of intrinsic capacitances on the dynamic performance of printed electrolyte-gated inorganic field effect transistors. *IEEE Transactions on Electron Devices, 66(8), 3365-3370.*
- Wang, Z., Cui, H., Li, S., **Feng, X.**, ... and Levkin, P. (2021). A Facile Approach to Conductive Polymer Micro-electrodes for Flexible Electronics. *ACS Applied Materials & Interfaces Manuscript, 13(18), 21661-21668.*

- Ulianova, V., Rasheed, F., Bolat, S., Sevilla, G. T., Didenko, Y., **Feng, X.**, ... and Aghassi-Hagmann, J. (2020). Fabrication, Characterization and Simulation of Sputtered Pt/In-Ga-Zn-O Schottky Diodes for Low-Frequency Half-Wave Rectifier Circuits. *IEEE Access, 8, 111783-111790.*
- Marques, G. C., Sukuramsyah, A. M., Rus, A. A., Bolat, S., Aribia, A., **Feng, X.**, ... and Aghassi-Hagmann, J. (2019). Fabrication and Modeling of pn-Diodes Based on Inkjet Printed Oxide Semiconductors. *IEEE Electron Device Letters, 41(1), 187-190.*
- Cadilha Marques, G., Weller, D., Erozan, A. T., **Feng, X.**, Tahoori, M., and Aghassi-Hagmann, J. (2019). Progress Report on "From Printed Electrolyte-Gated Metal-Oxide Devices to Circuits". *Advanced Materials, 31(26), 1806483.*
- Jeong, J., Marques, G. C., **Feng, X.**, Boll, D., Singaraju, S. A., Aghassi-Hagmann, J., ... and Breitung, B. (2019). Ink-Jet Printable, Self-Assembled, and Chemically Crosslinked Ion-Gel as Electrolyte for Thin Film, Printable Transistors. *Advanced Materials Interfaces, 6(21), 1901074.*

Workshops

- **Feng, X.**, Marques, G. C., Rasheed, F., Tahoori, M. B., and Aghassi-Hagmann, J. (2018). Analog Properties of Printed Electrolyte-Gated FETs based on Metal Oxide Semiconductors. *59. MPC Workshop, IEEE German Section Solid-State Circuit Society.* ***Best Paper Award***.

Conference contributions

Posters

- **Feng, X.**, Tahoori, M. B., and Aghassi-Hagmann, J. (2019). An Extended Meyer Capacitance Model of Inkjet-Printed Electrolyte-gated Inorganic Transistors. *Trade fair and conference for printed electronics (LOPEC).*

Presentations

- **Feng, X.**, Scholz, A., Tahoori, M. B., and Aghassi-Hagmann, J. (2020). A printed rectifier based on inkjet-printed electrolyte-gated inorganic transistors. *Trade fair and conference for printed electronics (LOPEC).*
- **Feng, X.**, Lukosiunas, J., Strunk, K., ... and Aghassi-Hagmann, J. (2021). Process Design Kit for Printed Organic Electronics within an Integrated Sensor Platform. *Trade fair and conference for printed electronics (LOPEC).*

Abstract

The manufacturing of conventional electronics has become a highly complicated process, which requires intensive investment. In this context, printed electronics keeps attracting attention from both academia and industry. The primary reason is the simplification of the manufacturing process via additive printing technology such as ink-jet printing. Consequently, advantages are realized such as on-demand fabrication, minimal material waste and versatile choice of substrate materials. Central to the development of printed electronic circuits are printed transistors. Recently, metal oxide semiconductors such as indium oxide have become promising materials for the fabrication of printed transistors due to their high charge mobility. Furthermore, electrolyte-gating also provides benefits such as the low-voltage operation in sub-1 V regime due to the large gate capacitance provided by electrical double layers. This opens new possibilities to fabricate printed devices and circuits for niche applications.

To facilitate the design and fabrication of printed circuits, the development of compact models is necessary. However, most of the current works have focused on the study of the static behavior of transistors, while the in-depth understanding of other characteristics such as the dynamic or noise behavior is missing. To this end, the purpose of this work is the comprehensive study on capacitance and noise properties of inkjet-printed electrolyte-gated thin-film transistors (EGT) based on indium oxide semiconductors. Proper modeling approaches are also proposed to capture accurately the electrical behaviour, which can be further utilized to enable advanced analysis of digital, analog and mixed-signal circuits.

In this work, the capacitance of EGTs is characterized using voltage-dependent impedance spectroscopy. Intrinsic and extrinsic effects are

carefully separated by using de-embedding test structures. Also, a dedicated equivalent circuit model is established to offer accurate simulations of the measured frequency response of the gate impedance. Based on that, it is revealed that top-gated EGTs have the potential to reach operation frequency in the kHz regime with proper optimizations of materials and printing process. Furthermore, a Meyer-like model is proposed to accurately capture the capacitance-voltage characteristics of the lumped terminal capacitance. Both parasitic and nonquasi-static effects are considered. This further enables the AC and transient analysis of complex circuits in circuit simulators.

Following, the study of noise properties in the field of printed electronics is conducted. Low-frequency noise of EGTs is characterized using a reliable experimental setup. By examining measured noise spectra of the drain current at various gate voltages, the number fluctuation with correlated mobility fluctuation has been determined as the primary noise mechanism. Based on that, normalized flat-band voltage noise can be determined as the key performance metrics, which is only $1.08 \times 10^{-7}\,\mathrm{V^2\,\mu m^2}$, significantly lower in comparison with other thin-film technologies, which are based on dielectric gating and semiconductors such as IZO and IGZO. A Plausible reason could be the large gate capacitance offered by the electrical double layers. This renders EGT technology useful for low-noise and sensitive applications such as sensor periphery circuits.

Last but not least, various circuit designs based on EGT technology are proposed, including basic digital circuits such as inverters and ring oscillators. Their performance metrics such as the propagation delay and power consumption are extensively characterized. Also, the first design of a printed full-wave rectifier is presented by using diode-connected EGTs, which features near-zero threshold voltage. As a consequence, the presented rectifier can effectively process input voltage with a small amplitude of 100 mV and a cut-off frequency of 300 Hz, which is particularly attractive for the application domain of energy harvesting. Additionally, the previously established capacitance models are verified on those circuits, which provide a satisfactory agreement between the simulation and measurement data.

Zusammenfassung

Die Herstellung konventioneller Elektronik ist ein hochkomplexer Prozess, der hohe Kosten erfordert. In diesem Zusammenhang gewinne die gedruckte Elektronik sowohl in der Wissenschaft als auch in der Industrie eine erhöhte Aufmerksamkeit. Der Hauptgrund dafür ist die Vereinfachung des Herstellungsprozesses durch additive Drucktechnologien wie Inkjet-Druck. Dies hat Vorteile wie die bedarfsgerechte Herstellung und minimaler Materialverbrauch. Außerdem wird eine vielfältige Auswahl verschiedener Substratmaterialien ermöglicht. Im Zentrum der Entwicklung von Schaltungen auf Basis gedruckter Elektronik stehen gedruckte Transistoren. In letzter Zeit sind Metalloxidhalbleiter wie Indiumoxid aufgrund ihrer hohen Ladungsbeweglichkeit zu vielversprechenden Materialien für die Herstellung gedruckter elektronischer Bauelemente geworden. Darüber hinaus bietet der Elektrolyt-Gate-Ansatz aufgrund der großen Gate-Kapazität, die durch die elektrischen Doppelschichten bereitgestellt wird, auch die Vorteile, einen Niederspannungsbetrieb im Sub-1 V-Bereich zu erreichen. Dies eröffnet neue Möglichkeiten für die Herstellung gedruckter Bauteile und Schaltungen in Nischenanwendungen.

Um das Design und die Herstellung von gedruckten Schaltungen zu erleichtern, ist die Entwicklung kompakter Modelle erforderlich. Die meisten existierenden Arbeiten haben sich bisher auf die Untersuchung des statischen Verhaltens von Transistoren konzentriert. Hierbei wird das dynamische und das Rauschverhalten der Bauteile häufig vernachlässigt. Ziel dieser Arbeit ist es daher, die umfassende Untersuchung der Kapazitäts sowie Rauscheigenschaften Tintenstrahl-gedruckter Dünnschichttransistoren mit einem flüssig-prozessierbaren Feststoffelektrolyten als Isolator

(EGT) und einem Indiumoxid-Halbleiter als Kanalmaterial durchzuführen.. Es werden geeignete Modellierungsansätze vorgeschlagen, um das elektrische Verhalten genau zu erfassen. Dies ermöglicht eine erweiterte Analyse analoger, digitaler sowie gemischter analog-digitaler Schaltungen.

In dieser Arbeit wird die Kapazität von EGTs mittels spannungsabhängiger Impedanzspektroskopie charakterisiert. Intrinsische und extrinsische Effekte werden durch Verwendung von De-Embedding-Teststrukturen getrennt. Des Weiteren wird ein Ersatzschaltbild erstellt, um genaue Simulationen des gemessenen Frequenzgangs der Gate-Impedanz zu ermöglichen. Auf dieser Grundlage zeigt sich, dass Top-Gate EGTs das Potenzial haben, eine Schaltfrequenz im kHz-Bereich zu erreichen, wenn die Materialien und der Druckprozess weiter optimiert werden. Darüber hinaus wird ein Meyer-ähnliches Modell vorgeschlagen, um die Kapazitäts-Spannungs-Eigenschaften der Anschlusskapazität genau zu erfassen. Es werden sowohl parasitäre Kapazitäten als auch nicht-quasistatische Effekte berücksichtigt. Die resultierenden Modelle ermöglichen weitere AC- und transiente Simulationen komplexer Schaltungen in der EGT-Technologie.

Im Folgenden werden Untersuchungen zu den Rauscheigenschaften gedruckter EGTs durchgeführt. Das Niederfrequenzrauschen wird anhand eines eigens dafür optimierten Versuchsaufbaus charakterisiert. Durch Untersuchung der gemessenen Rauschspektren im Transistor-Drainstrom bei verschiedenen Gate-Spannungen wurde die Ladungsträgerschwankung mit korrelierter Mobilitätsschwankung als primärer Rauschmechanismus bestimmt. Auf dieser Grundlage kann das normalisierte Flachband-Spannungsrauschen als Hauptleistungsmetrik berechnet werden, was im Vergleich zu anderen Dünnschichttechnologien, die auf Dielektrika und Halbleitern wie IZO und IGZO basieren, einen erheblich niedrigeren Wert aufweist.. Ein plausibler Grund könnte die große Gate-Kapazität sein, die durch die elektrische Doppelschicht erzeugt wird. Daher eigenen sich gedruckte EGTs für beispielsweise rauscharme Anwendungen in der Sensorik.

Abschließend werden verschiedene Schaltungsdesigns vorgeschlagen, die auf EGT-Technologie basieren. Dies beinhaltet grundlegende digitale Schaltungen wie Inverter Strukturen und Ringoszillatoren. Ihre Leistungsmetriken, einschließlich der Gatterlaufzeit und dem Stromverbrauch, werden ausführlich charakterisiert. Des Weiteren wird das erste Design eines gedruckten Brückengleichrichters unter Verwendung von EGTs mit eine nahe-null-Volt-Schwellspannung in einer Dioden-Konfiguration vorgestellt. Der vorgestellte Gleichrichter ist in der Lage, Eingangsspannungen mit kleiner Amplitude von circa 100 mV effektiv zu verarbeiten. Dies ist besonders im Anwendungsbereich des Energy-Harvestings von Interesse. Zusätzlich werden die zuvor etablierten Kapazitätsmodelle auf diesen Schaltungen verifiziert. Ein Vergleich der Simulations- und Messdaten zeigt deren sehr gute Übereinstimmung und verifiziert die entwickelten Kapazitätsmodelle.

Contents

List of Figures

List of Tables

1. Introduction

1.1. Overview of Printed electronics

1.1.1. History

The history of humanity has already experienced three industrial revolutions. Central to the third revolution is the invention and widespread use of solid-state electronics. The deriving technologies such as integrated circuits, computers and the internet has changed almost every aspect of daily life since the latter half of the 20th century. At the same time, the semiconductor industry have undergone rapid growth, while the miniaturization of transistor devices is the key driving force. As predicted by "Moores Law", the number of transistors in integrated circuits increases by a factor of two in every two years (Fig. 1.1 [1]). This has been guiding the research and development of the semiconductor industry. In 1971, the world's first commercial microprocessor Intel 4004 integrates only 2300 transistors based on the 10 µm technology [2], while in 2019, the AMD's Zen 2 microprocessor contains 39.54 billion transistors using TSMC's 7 nm technology [3]. However, the manufacturing of conventional electronics has evolved into a highly complicated process, including multiple subtractive steps such as photo-lithography, etching, doping, cleaning. It has become an investment intensive business. Nowadays, the cost of building a new semiconductor fabrication plant, also called foundry, can easily exceed one billion U.S. dollars [4].

On the contrary, printed electronics (PE) offers a complementary solution to conventional electronics by simplifying the manufacturing process via

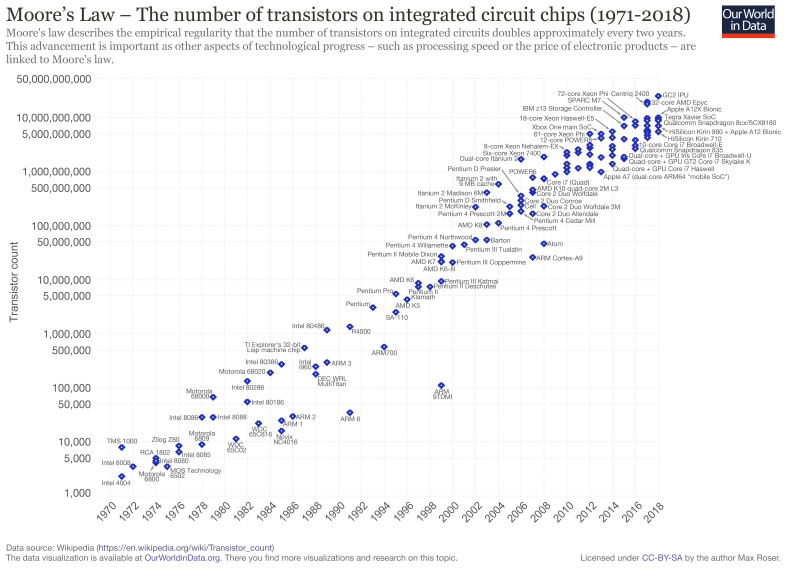

Figure 1.1.: The Moore's law predicts that the number of transistors in an integrated circuit doubles every 24 months. Reprint from [1] under license CC-BY-4.0.

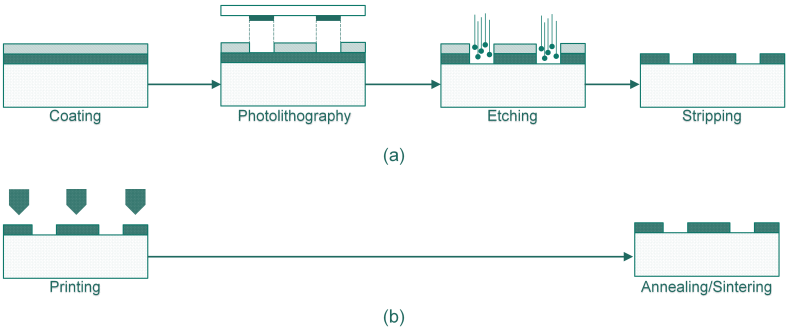

Figure 1.2.: (a) The manufacturing of conventional electronics is based on the subtractive process with complex fabrication steps involved. (b) The manufacturing of printed electronics is based on the additive process with much less fabrication steps involved.

additive printing technology. Fig. 1.2 illustrates the fundamental difference of the fabrication process between conventional and printed electronics. The functional materials such as metals and semiconductors are directly deposited and patterned on the substrate. Therefore, as compared with conventional electronics, printed electronics has the unique advantage of low-cost fabrication, which mainly originates from two factors: minimal material wastes and fewer fabrication steps during the process. Furthermore, it possesses more features such as the on-demand fabrication, which can hardly be accomplished by conventional electronics and thus keep attracting the attention from both research and industry.

1.1.2. Material aspect

The history of printed electronics begins with organic electronics. It can be traced back to the discovery of conductive polymers in 1977 [5], followed by the development of organic semiconductors in 1983 [6] and organic field-effect transistors (OFETs) in 1986 [7]. Since organic materials can be naturally formed into inks, the idea of printed OFETs becomes reality in 1997 [8]. However, organic electronics suffer from the low charge mobility, which is an essential property to determine the speed and driving ability of transistors. Despite the research efforts in the past three decades, the charge mobility of printed organic semiconductor materials can barely exceed $5\,cm^2\,V^{-1}\,s^{-1}$ [9], which is almost three orders of magnitude lower than the single-crystalline silicon [10]. This has significantly limited the practical applications of printed organic electronics. Furthermore, some organic materials have the stability issue, including the sensitivity to the oxygen and water in the environment.

The limit of printed electronics is again pushed by the development of inorganic semiconductor materials, including metal oxide, carbon nanotube and graphene. These kinds of materials possess high charge carrier mobility even if printed, which can easily exceed $10\,cm^2\,V^{-1}\,s^{-1}$ [11]. Recently, there have been even reports showing high charge mobility approaching $100\,cm^2\,V^{-1}\,s^{-1}$ [12]. The road map published by Organic Electronics

Association (OE-A) predicts that the long term development of printed semiconductors relies on the innovation of inorganic and nano-materials [13].

However, there are also several disadvantages to those materials. One of them is the high post-processing temperature which hinders the realization of flexible electronics, because most flexible substrates cannot endure high temperature, such as polyethylene naphthalate (PEN) < 155 °C, and polyethylene terephthalate (PET) < 250 °C. Nevertheless, inorganic and nano-materials are still very promising candidates for printed electronics applications in the near future.

1.1.3. Application domains

Printed electronics has been gifted with lots of attractive features, such as mechanical flexibility, low-cost and on-demand fabrication. Therefore, it is exciting to imaging, how many kinds of new applications can be enabled by this emerging technology. Notably, printed electronics targets applications that can be hardly covered by conventional electronics.

Generally, printed electronics is increasingly recognized as a key enabler for various fields of application. For example, in the automobile industry, the utilization of organic light emitting diodes (OLEDs) can potentially reduce the weight and production costs, while the form-factor provided by flexible displays and printed sensors realize new designs of interaction and entertainment systems [14]. Also, medical applications are the potential market. The stretch-ability and mechanical flexibility of printed electronics can be fully utilized to make bio-compatible and wearable devices to monitor vital signs of human invasively [15, 16]. In another example, novel medical devices using disposable printed sensors are invented to measure the pressure distribution on occlusal surfaces, which facilitates the diagnosis of diverse symptoms [17]. Last but not the least, in the area of Internet of Things (IoT), printed electronics can play an important role to realize niche applications. There have already been demonstrations of

radio-frequency identification (RFID) tags consisting of organic transistors [18]. Additionally, due to the large number of sensors required by IoT, printed sensors are advantageous and competitive in the aspect of fabrication cost [19, 20].

As of 2018, the printed electronics has already its total market of 31.7 USD billion, where the categories of printed/flexible displays and sensors are the primary driving forces, with the shares of 26 USD billion and 3.6 USD billion, respectively. On the other hand, printed logic circuits, memories and batteries possess also strong growth potential [21]. It is forecasted by IDTechEx Research that, in 2029, the market of printed electronics can reach the total market of 74 USD billion [22].

1.2. Motivation

In conventional electronics, proper tools are essential to design circuits and applications. In the semiconductor industry, this tool package is called process design kit (PDK), comprising design rules and model libraries for a certain technology. The former defines constrains and criteria of standardized physical and electrical manufacturability, whereas the latter accurately reproduces the electrical characteristics of electron devices using a set of mathematical equations in the circuit simulator. To assure the simulation speed, compact modeling is preferred where expensive math functions are often avoided. A standard transistor model library covers various aspects of the electrical characteristics of devices. For instance, the famous industry-standard Berkeley Short-channel IGFET Model (BSIM) consists of drain-current model, threshold voltage model, capacitance model, flicker noise model, just to name a few [23]. With the help of an accurate PDK, the design process can be largely facilitated.

Although PDK techniques have been widely introduced in the conventional silicon industry, PDK developed for printed electronics has been scarcely reported. For instance, the VLSI Group and Organic Electronics Group of University of Minnesota have developed an open-source

Organic PDK based on their Gel-Electrolyte-Gated Polymer Transistors in 2011 [24], which supports the layout design and basic circuit simulation. Another example is the PDK presented by the group of Nanyang Technological University based on their fully additive printing technology [25] with similar functionality as the aforementioned one. They have successfully demonstrated the design and fabrication of basic digital and analog circuits using the PDK.

In those early demonstrations of PDKs for printed electronics, one can conclude that most works regarding the compact modeling have only focused on the modeling of static current-voltage (I-V) characteristics. This enables direct current (DC) analysis of circuit simulation, while other models such as capacitance-voltage (C-V) and noise models are missing to support e.g. transient, alternating current (AC) and noise analysis. In the recent publication of M. Fattori, et al. in 2019 [26], capacitance and noise models are included in the PDK to enable a comprehensive analysis of the transimpedance amplifier. However, the modeling approaches and outcomes are still in a preliminary stage as presented in PDKs, lacking deep understanding of the device physics and careful validation of models with experimental data.

Indeed, the development of reliable models for printed transistors is a challenging task due to the large variety of devices in terms of materials and fabrication process. However, the everlasting evolution of compact modeling in design tools is essential for the development of circuits/applications/systems in printed electronics.

Apart from the PDK development, there have also been research works concentrating on compact modeling of printed electronics. However, the focus of most studies has been still on I-V modeling and the static performance of devices and circuits. On contrary, other kinds of characteristics have received less attention, which hinders more advanced circuit analysis.

In this context, the purpose of this thesis is to comprehensively characterize the electrical behavior of printed transistors to gain a deep understanding of the device physics, including the capacitance and noise. Based

on that, compact models are developed for accurate circuit simulation as a part of the standard PDK. Also, both basic and novel printed circuits are developed and characterized.

1.3. Structure of this thesis

The rest of the thesis into five chapters are organized as listed below:

- Chapter 2 gives an introduction to field-effect transistors and the technical background of printed electronics. Also, the basic structure of printed transistors and their functionality will be extensively evaluated.
- Chapter 3 deals with characterization and modeling of capacitance in EGTs. Measurements Voltage-dependent impedance spectroscopy of transistors will analyzed, and the frequency response will be modelled by the equivalent circuit method. This reveals important information of the dynamic behavior in EGTs. Additionally, a Meyer-like nonquasi-static model is established to enable advanced circuit simulations.
- Chapter 4 presents the study on the low-frequency noise in printed electronics. The noise generation mechanism of EGTs will be comprehensively explained by comparing with the existing theories and experimental data. Figure of merit will be calculated to provide the benchmark of noise level with state-of-the-art thin-film technologies.
- Chapter 5 proposes various circuits based on the printed electronics, including printed inverter, ring oscillator and full-wave rectifier. Also, the compact modeling of the transistor capacitance is validated through the comparison between measurement and experimental data in the circuit level.
- Chapter 6 summarizes the whole thesis and gives an outlook for future works.

2. Background

Transistors are the basic building blocks of integrated circuits, the rapid development of which triggers the revolution in modern electronics since their first invention at Bell Labs in 1947. In the history of transistors, various types of transistors have been invented, such as bipolar junction transistors (BJTs), junction field-effect transistorss (JFETs) and metal-oxide-semiconductor field-effect transistors (MOSFETs). The last ones have become the most dominant semiconductor devices due to a set of advantages over the others, including the easy manufacturability, the high gate impedance and the low leakage current.

To effectively understand the principle of MOSFETs, in this chapter, a comprehensive introduction on metal-oxide-semiconductor (MOS) capacitors is firstly presented. Based on that, the device physics of MOSFETs will be explained in detail. Then, fundamentals in printed electronics will be focused on, including material properties and printed technologies. The final section gives the technical background of the the main subject of study, namely EGTs.

2.1. MOS capacitor

2.1.1. Operation modes

In Fig. 2.1, the cross-section view of an n-type MOS capacitor base on the p-type substrate is illustrated as an example. For p-type MOS capacitors, the polarization of the semiconductors is inverted. It has a sandwich structure

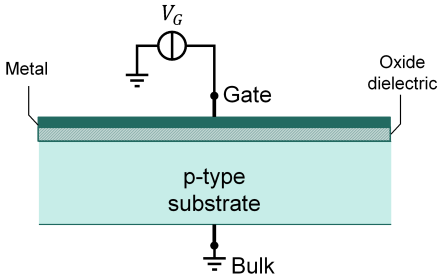

Figure 2.1.: Cross-section view of a planar n-type MOS capacitor.

formed by the gate contact on the top, the body contact at the bottom and the oxide dielectric in between. Upon the application of the bias potential between gate and body, the operation of the MOS capacitor can be divided into four modes, namely the flat-band, accumulation, depletion and inversion mode. Here, the corresponding energy band diagrams as presented in Fig. 2.2 (a)-(d) are often used to help the understanding of the working modes.

(a) Flat-band condition: The analysis starts with a special condition called the flat-band condition, as shown in Fig. 2.2(a), which is realized by applying a certain flat-band voltage V_{FB} to the gate voltage V_G. Here, the free electron level E_0 is continuous since the electron can freely move between the crystal field of different materials. In the metal, the Fermi level E_F lies inside the conduction band E_C, while in the p-type semiconductor, E_F lies between the E_C and valence band E_V, which is closer to the E_V due to the doping. In the flat-band condition, the electric field in the three materials is zero.

(b) Accumulation condition: If a gate voltage less than the flat-band voltage is applied as depicted in Fig. 2.2(b), the energy band of the gate metal shifts upwards. At the same time, the energy band of the semiconductor substrate bends upward. Due to bending, the Fermi level on the surface of the semiconductor is more closer to the valence band than

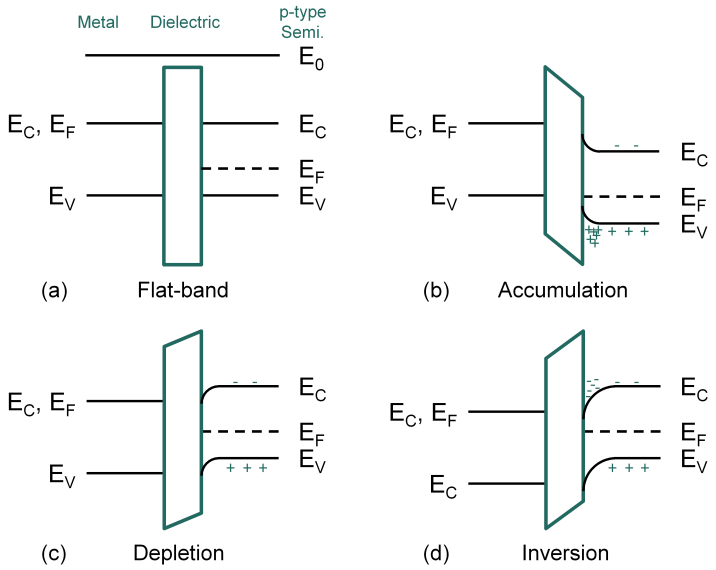

Figure 2.2.: Energy band diagram of MOS capacitor base on p-type substrate under different conditions: (a) flat-band, (b) accumulation, (c) depletion, (d) accumulation.

the Fermi level in the bulk, resulting in an excess of holes on the surface. Therefore, this is referred to as surface accumulation.

(c) Depletion condition: On the contrary, if the applied gate voltage is higher than the flat-band voltage as shown in Fig. 2.2(c), the band bends downwards. When the Fermi level on the surface of the semiconductor is neither close to the conductance band nor the valence band, both electron and hole charge densities are significantly small. Now, a depletion region has been established, and this condition is called the depletion mode.

(d) Inversion condition: Finally, when the gate voltage is increased more positively, the energy band bends further downwards. When the Fermi level is closer to the conduction band than the valence band, holes are

depleted from the surface, resulting in the electron concentration at the surface exceeding the hole concentration. At this point, the applied gate voltage is termed as threshold voltage V_{th}. After that, the operation of the MOS capacitor enters the inversion region, where the p-type substrate surface has been inverted to another polarity, not due to the doping but the applied electric field.

2.1.2. C-V characteristics

The capacitance-voltage (C-V) characteristics of the MOS capacitor reveal important information such as the doping concentration, gate oxide thickness, flat-band voltage and threshold voltage. Furthermore, the C-V characteristics are also strongly related to the working principle of the MOSFET and its current-voltage (I-V) characteristics.

In the C-V analysis of the MOS capacitor, the capacitance is always referred as the small-signal capacitance, which is defined as:

$$C = \frac{dQ}{dV}, \tag{2.1}$$

where the Q is the charge that the capacitor holds, and V is the voltage applied to it. Since the derivative of the charge with respect to the time, dQ/dt, is the current $i(t)$, one can also measure the small-signal capacitance by applying an alternating voltage $v(t)$ and measuring the resulting current $i(t)$:

$$C = \frac{dQ}{dV} = \frac{dQ/dt}{dV/dt} = \frac{i(t)}{dv(t)/dt}. \tag{2.2}$$

Often, the small-signal capacitance is measured by the LCR meter. More details about the measurement techniques will be discussed later in chapter 3.

A simplified illustration of the C-V characteristics is presented in Fig. 2.3, where the four aforementioned bias conditions are reflected, namely accumulation, flat-band, depletion and inversion.

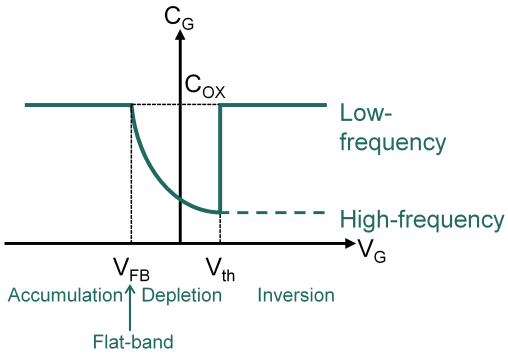

Figure 2.3.: C-V characteristics of the MOS capacitor.

(a) Accumulation region: In the accumulation mode when $V_G < V_{FB}$, only the accumulation charge Q_{ACC} is present on the surface of the substrate. Therefore, the MOS capacitor behaves like a normal parallel plate capacitor. Consequently, in C-V characteristics, one can only see the gate oxide capacitor C_{OX} in the measurement in this region.

(b) Depletion region: When the V_G exceeds V_{FB} and therefore the MOS capacitor enters the depletion region, one additional depletion capacitor C_{DEP} is introduced due to the creation of the depletion layer with the thickness of W_{DEP} as a function of the gate voltage. Therefore, the value of C_{DEP} can be calculated as:

$$C_{DEP} = \frac{\epsilon_{SUB}\epsilon_0}{W_{DEP}}, \tag{2.3}$$

where ϵ_{SUB} is the dielectric constant of the substrate material and ϵ_0 is the vacuum permittivity,.

As V_G increases, the depletion layer expands, and C_{DEP} becomes smaller. Electrically, C_{DEP} is in series connection with C_{OX}. Thus, the total capacitance can be calculate as:

$$\frac{1}{C_G} = \frac{1}{C_{OX}} + \frac{1}{C_{DEP}}. \tag{2.4}$$

As shown in Fig. 2.3, its value decreases as the V_G increases in the depletion region.

(c) Inversion region: As V_G further increases and reaches the threshold voltage V_{th}, the inversion layer is formed. Now, the inversion charge Q_{INV} is present between the substrate and oxide dielectric interface, resulting in the inversion capacitance C_{INV}. Electrically, C_{INV} is in parallel connection with the depletion capacitance. Therefore, the calculation of the total gate capacitance C_{DEP} becomes:

$$\frac{1}{C_G} = \frac{1}{C_{OX}} + \frac{1}{C_{DEP} + C_{INV}}. \tag{2.5}$$

In the inversion region, the value of C_G increases aggressively due to the presence of C_{INV} until it approaches again the C_{OX}. However, since the inversion capacitance is originated from the minority charge carrier, it has a large time-scale and fails to respond to the high-frequency signal. Therefore, at high frequencies (for silicon MOSFET it is typically above 100 Hz), less C_G can be measured in C-V characteristics.

2.2. MOSFET

The MOSFET has a more complex three-terminal structure than the MOS capacitor. As shown in Fig. 2.4 (a), two additional source and drain electrodes are introduced as compared to the MOS capacitor. Upon the application of the gate voltage, the surface state of the channel is modified accordingly similar to the MOS capacitor. With the channel in the accumulation/depletion mode, the transistor is in OFF state, while it is turned

ON when the channel is in the inversion mode. This section explains the working principle of the MOSFET, its current-voltage characteristics in the on-state are studied.

2.2.1. I-V characteristics

When the bias between gate and source V_{GS} exceeds the threshold voltage V_{th}, an inversion layer is induced at the channel-oxide interface. Supposing that a small drain-source bias V_{DS} is applied, the local voltage $V(x)$ is distributed along the channel, yielding a local channel charge density:

$$Q_{INV} = -WC_{OX}(V_{GS} - V_{th} - V(x)), \tag{2.6}$$

where W is the channel width.

As discussed in the analysis of MOS capacitor, Q_{INV} is only present when:

$$V_{GS} - V_{th} - V(x) > 0, \tag{2.7}$$

Consequently, the local current per unit length can be calculated using the field-effect mobility μ_{FET} and local electric field $E(x)$:

$$\begin{aligned} I_{DS} &= \mu_{FET} Q_{INV} E(x) \\ &= -\mu_{FET} WC_{OX}(V_{GS} - V_{th} - V(x))E(x). \end{aligned} \tag{2.8}$$

Noting that $E(x) = -\frac{dV(x)}{dx}$, the total current in the channel can be obtained by performing the integration on both sides of Eq. 2.8:

$$\begin{aligned} \int_0^L I_{DS} dx &= \int_0^L \mu_{FET} WC_{OX}(V_{GS} - V_{th} - V(x)) \frac{dV(x)}{dx} dx \\ &= \int_0^{V_{DS}} \mu_{FET} WC_{OX}(V_{GS} - V_{th} - V(x)) dV \\ &= \mu_{FET} WC_{OX}((V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2), \end{aligned} \tag{2.9}$$

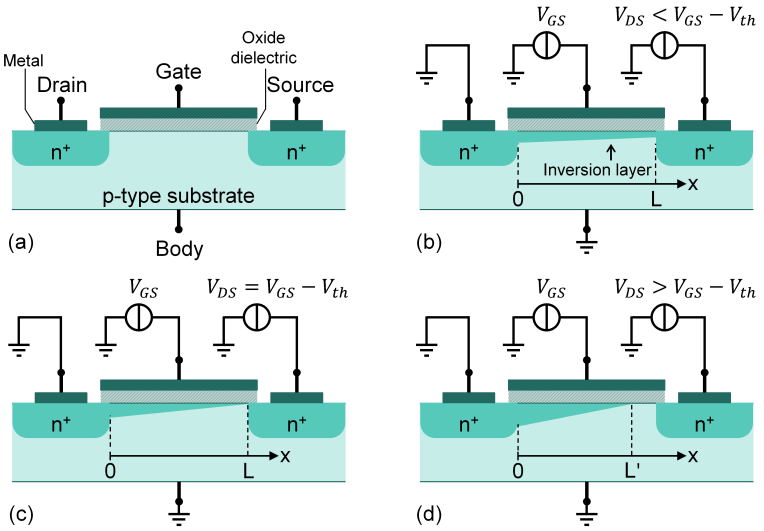

Figure 2.4.: (a) Cross-section view of a planar n-type metal oxide field-effect transistor. MOSFET in different bias conditions: (b) Triode region, (b) Channel pinch-off and (c) Saturation region.

$$I_{DS} = \frac{W}{L}\mu_{FET}C_{OX}((V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2), \tag{2.10}$$

where V_{DS} is the drain-source bias and L is the channel length. The Eq. 2.10 holds true for a small V_{DS}. This is the so-called triode region of the MOSFET operation as shown in Fig. 2.4 (b).

When the drain-source bias V_{DS} further increases to $V_{GS} - V_{th}$, the potential difference between oxide-channel interface becomes zero. It fails to support the depletion layer at the drain side. Thus, Eq. 2.7 cannot be satisfied any more. At this moment, the so-called channel "pinch-off" occurs as shown in Fig. 2.4(c). Now, the integration in Eq. 2.8 becomes:

$$\int_0^L I_{DS}dx = \int_0^{V_{GS}-V_{th}} \mu_{FET}WC_{OX}(V_{GS} - V_{th})dV \tag{2.11}$$

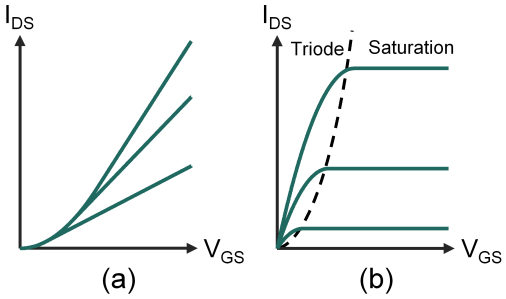

Figure 2.5.: Typical I-V characteristics of the n-type MOSFET. (a) Transfer characteristics. (b) Output characteristics.

$$I_{DS} = \frac{1}{2}\frac{W}{L}\mu_{FET}C_{OX}(V_{GS} - V_{th})^2. \tag{2.12}$$

Starting from the "pinch-off" point, the MOSFET is in its saturation region as shown in Fig. 2.4 (d). To calculate the I_{DS} after this point, Eq. 2.11 can still be used, where the length in the left side becomes shorter, $L' = L - \Delta L$. Based on the first order assumption, $\frac{\Delta L}{L} = \lambda V_{DS}$ [27]. Consequently, I_{DS} can be calculated as:

$$I_{DS} = \frac{1}{2}\frac{W}{L}\mu_{FET}C_{OX}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \tag{2.13}$$

This is called the channel-length modulation, where λ is the modulation coefficient. To this end, the whole regions when the MOSFET is turned on have been described with their I-V characteristics exemplified in Fig. 2.5.

2.2.2. C-V characteristics

In the previous section, the static I-V characteristics of the MOSFET have been described. To understand the dynamic behavior of the MOSFET, one needs knowledge of the transistor capacitance.

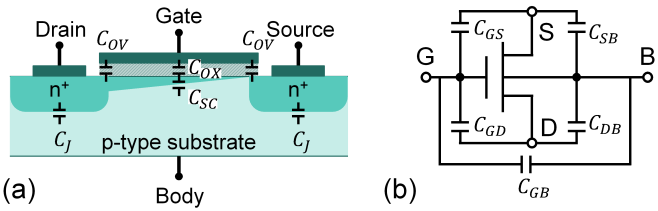

Figure 2.6.: (a) Physical structure of capacitance components in the MOSFET. (b) Representation of lumped terminal capacitance model in schematic level.

As shown in Fig. 2.6 (a), different capacitance components in the MOSFET are present at various material interfaces. Firstly, as discussed previously, the oxide capacitance C_{OX} is present between the gate and channel. Also, in the MOSFET device, it unavoidable to have the overlap region between the gate and source/drain electrodes. yielding the overlap capacitance C_{OV}. Additionally, considering the MOSFET in an ON-state, the depletion layer and the inversion layer are formed on the surface of the semiconductor, corresponding to the depletion capacitance and inversion capacitance. Since they are electrically in parallel connection as explained earlier, the semiconductor capacitance C_{SC} is used to represent their summation. Furthermore, since the n-type doped source and drain area creates a p-n junction at the interface with the p-type substrate, the junction capacitance C_J is formed there.

The aforementioned capacitance components can be categorized into two groups, namely intrinsic and extrinsic capacitance. Both C_{OX} and C_{SC} are considered as the intrinsic effects since they are associated with the state of the channel, while die others are extrinsic effects.

During the operation of the MOSFET, a non-zero V_{DS} is applied to the device. Often, this results in a non-uniform distribution of the inversion layer thickness on the semiconductor surface along the channel direction. Therefore, the C_{SC} is not always constant, but a function of the channel position, which also changes concerning the applied external bias voltage.

From the perspective of compact modeling, a practical approach is to treat the transistor capacitance as a lumped capacitance between terminals, which are described as voltage-dependent capacitors. Each of them contains both intrinsic and extrinsic effects. This idea is illustrated in Fig. 2.6 (b), among which the gate-source capacitance C_{GS} and gate-drain capacitance C_{GD} are the ones of highest interest. Here, a comprehensive investigation will be given to determine their values in different operation regions of the MOSFET. For simplicity, only intrinsic components are considered.

In principle, the terminal capacitance is the partial derivative of gate charge Q_G with respect to the terminal voltage:

$$C_{GS} = \frac{\partial Q_G}{\partial V_{GS}}, \tag{2.14}$$

$$C_{GD} = \frac{\partial Q_G}{\partial V_{GD}}. \tag{2.15}$$

The investigation starts by applying gate bias V_{GS} above the threshold voltage, while source-drain bias V_{DS} is zero. In this case, the inversion charge on the semiconductor surface is uniformly distributed along the channel length, and the total gate capacitance is $C_{GG}= WLC_{OX}$. Therefore, the MOSFET is now symmetric with respect to the source and drain. The terminal capacitance C_{GS} and C_{GD} shares equally the total gate capacitance:

$$C_{GS} = C_{GD} = \frac{1}{2} WLC_{OX}. \tag{2.16}$$

When the V_{DS} increases, in the channel, the charge density at the source side becomes more, while it drops to at the drain side, as illustrated in Fig. 2.4 (c). This leads to an increase of the C_{GS} and decrease of the C_{GD}. When V_{DS} equals the overdrive voltage $V_{GS} - V_{th}$, there are no inversion charges at drain side. At this point, the C_{GD} is zero and C_{GS} reaches the maximum.

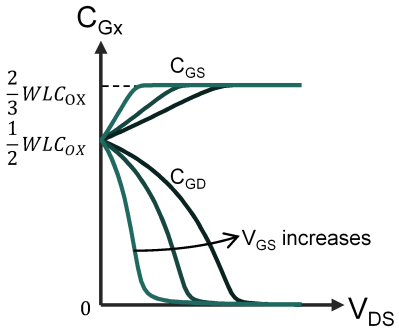

Figure 2.7.: Typical C-V characteristics of MOSFET as a function of drain-source voltage V_{DS} at various gate-source voltage V_{GS}.

To determine the values of C_{GD} and C_{GS} , the total gate charge needs to be studied. It can be proved that the local gate charge per channel length $Q_i(x)$ can be expressed as a function of channel position x [28]:

$$Q_i(x) = WC_{OX}(V_{GS} - V_{th})\sqrt{1 - \frac{x}{L}} \tag{2.17}$$

The total charge at the gate can be then obtained by integrating the expression from channel position $x = 0$ to $x = L$:

$$Q_G = WC_{OX}(V_{GS} - V_{th}) \int_0^L \sqrt{1 - \frac{x}{L}} dx = \frac{2}{3} WLC_{OX}(V_{GS} - V_{th}). \tag{2.18}$$

Then, using the definition in Eq. 2.14, one can obtain $C_{GS} = \frac{2}{3}WLC_{OX}$ and $C_{GD} = 0$. Fig. 2.7 shows both terminal capacitances as a function of and V_{DS}, when V_{GS} is changing.

2.2.3. Noise characteristics

Apart from the I-V and C-V characteristics, noise characteristics is also an important aspect. On one hand, it is a powerful non-destructive tool to

study surface defects, surface roughness and interface properties of the MOSFET device. It also helps to understand the charge carrier transport mechanism. On the other hand, it is unwanted and degrades the signal quality, especially for analog and radio-frequency (RF) circuits. Accurate modeling is required to correctly predict the performance of MOSFET circuits such as signal-to-noise ratio.

Electrical noise is a statistical random process. As the value of a noise signal changes randomly, it is impossible to predict its value in the time domain. Therefore, a more practical way to quantify a noise signal is to inspect its power spectral density (PSD), which gives more versatile information in the frequency domain. For a noise voltage signal in the time domain $v(t)$, the PSD is defined using the Fourier transformation as:

$$S(f) = |\int_{\infty}^{-\infty} e^{-2\pi i f t} v(t) dt|^2, \tag{2.19}$$

which has the unit of V^2/Hz. It implies that the energy or power of a noise signal that is normalized to 1 Hz bandwidth at various frequency points.

For MOSFET devices, there are two sources of noise, namely the thermal noise and the flicker noise. The thermal noise originates from the random motion of charge carriers inside conductors, which is independent of the external electric field. For resistors, the thermal noise can be described either by a voltage source v_n or a current source i_n in series connection with a noiseless resistor R, as depicted in Fig. 2.8. The power spectral density, namely S_V and S_i can be calculated as:

$$S_V = 4k_B T R \Delta f, \tag{2.20}$$

$$S_I = \frac{4k_B T}{R} \Delta f, \tag{2.21}$$

where k_B is the Boltzmann constant, T is the temperature, R is the resistance and Δf is the frequency bandwidth. As can be seen from Eq. 2.20 and 2.21, the thermal noise is independent of the frequency. It shows a

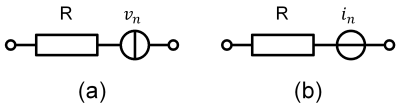

Figure 2.8.: Thermal noise model in (a) voltage source and (b) current source representation.

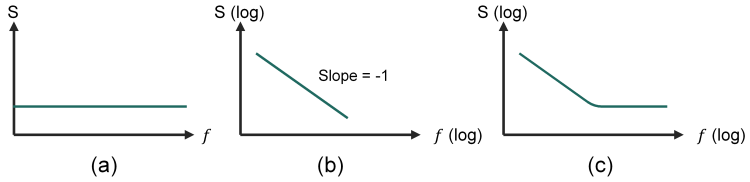

Figure 2.9.: Noise power density of (a) thermal noise and (b) flicker noise. In MOSFETs, both types of noise co-exist, resulting a noise behavior as shown in (c).

constant flat line in its PSD spectrum, as shown in Fig. 2.9 (a). For this reason, it is also called white noise.

The flicker noise has a power spectral density which is proportional to f^{-1}:

$$S(f) \propto \frac{1}{f}, \tag{2.22}$$

Therefore, in the logarithmic plot of the PSD spectrum, it has a constant slope of -1 as displayed in Fig. 2.9 (b). In most MOSFET devices, both thermal and flicker noise co-exist. At low frequency, the flicker noise often dominates, while in high frequencies the thermal noise is more pronounced. A typical noise spectral density of MOSFET is shown in Fig. 2.9 (c).

The generation mechanism of flicker noise in MOSFETs is a complex topic. Until now, there is still an on-going discussion on its physical origin. In principle, two kinds of theories are popular in this field, namely carrier number fluctuation theory and mobility fluctuation theory. The first one was firstly proposed by McWhorter [29], who claims that the fluctuation

behavior originates from the random trapping and de-trapping events of charge carriers on the surface traps of oxide, which is a purely surface effect. On the other hand, an opposite opinion considers the origin of flicker noise as a bulk effect. The representative one is Hooge's model [30] proposed based on the observation that the normalized current power density is inversely proportional to the total number of charge carrier. A more detailed discussion will be introduced in Chapter 5.

2.3. Printed thin-film transistor

Currently, the microelectronics market is dominated by the silicon-based bulk technology. However, in the future generation of electronics, new types of materials and fabrication processes are required to meet the needs of niche applications such as Internet-of-Things (IoT), smart sensors and wearable/implantable devices. As compared with the conventional bulk technology, thin-film transistors (TFTs) offer a set of attractive features such as the possibility to realize flexible electronics. Especially, the deployment of additive printing process during the fabrication of TFTs further adds more contributes, including cost-effective manufacturing, on-demand design, large-area and environmentally friendly processability. Therefore, printed TFTs are considered as promising candidates to meet the new requirements of emerging applications, which are largely complementary to their silicon counterparts.

Thin-film transistors are multi-layer structural electronic devices, comprising the dielectric layer, semiconductor layer and source/drain/gate electrodes According to the relative position of electrodes, TFTs can be categorized into two four configurations [31], including bottom-gate/bottom-contact, bottom-gate/top-contact, top-gate/top-contact and top-gate/bottom-contact as shown in Fig. 2.10 from (a) to (d). Due to the better transferring path of charge carriers, the configurations of bottom-gate/top-contact and top-gate/bottom-contact often exhibit better performance [32].

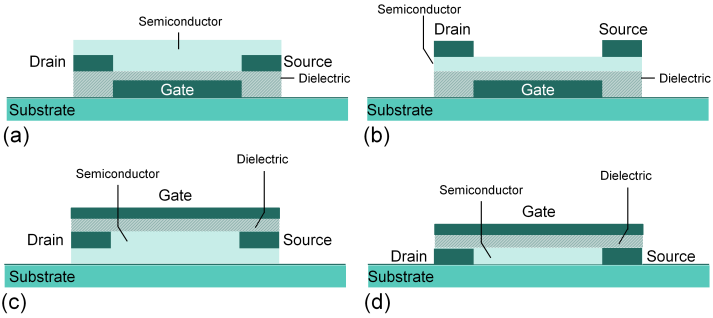

Figure 2.10.: Various configurations of thin-film transistors regarding the relative position of source, drain and gate electrode: (a) bottom-gate/bottom-contact, (b) bottom-gate/top-contact, (c) top-gate/top-contact and (d) top-gate/bottom-contact.

2.3.1. Printing technology

In printed thin-film technology, materials such as metals, dielectrics and semiconductors can be directly deposited on the substrate. The deposition process can be accomplished by various additive printing techniques using solution-processable materials, as illustrated in Fig.2.11.

Generally, printing techniques can be classified into two groups [33]. One is the inkjet digital printing that utilizes the nozzle to deposit solutions on the substrate. It produces patterned thin-film on-demand in a non-contacting way without additional masks. Therefore, it is a convenient technique, especially for rapid prototyping. As shown in Fig. 2.11(a), the inkjet printing system comprises the jetting control system, the vision system, and a motion platform. The printing nozzle heads are connected to the ink cartridge or reservoir. The electrical pulse applied to the piezo transducer triggers the ejection of the droplets from nozzles. Their positions relative to the substrate are observed by the vision system and controlled by the motion system which moves the substrate. Then, well-defined ink patterns are obtained on the substrate.

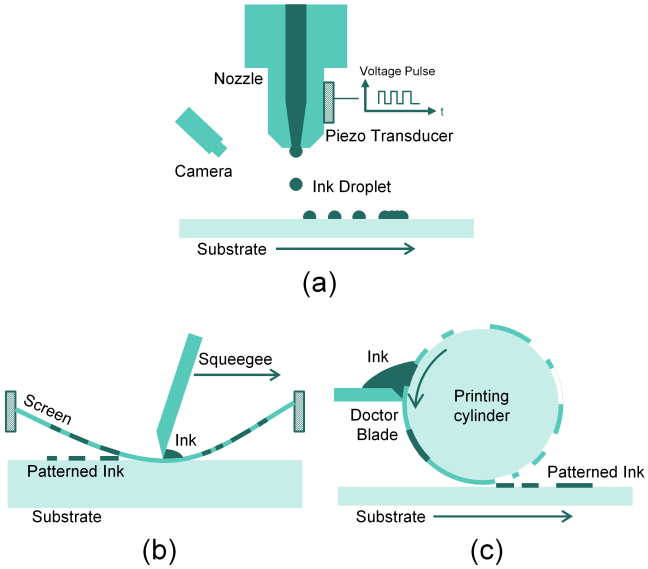

Figure 2.11.: Illustration of various printing techniques: (a) inkjet printing, (b) screen printing and (c) gravure printing.

Another class is non-digital printing including e.g. screen, gravure and transfer printing, which is suitable for mass production. In screen printing as shown in Fig. 2.11(b), a screen mask with pre-defined patterns are required. Using the squeegee, ink materials are squeezed through the mask, resulting in patterned large-area thin-film on the substrate surface. In gravure printing as shown in Fig. 2.11 (c), ink materials are contained in the gravure cylinder with pre-patterned cavities, while excess ink materials are removed by a doctor blade. Then, ink patterns are transferred onto the substrate through the rolling of the gravure cylinder.

Each printing technique features different printing resolutions and printing speed, while their requirements for the solution viscosity also differs.

The specifications of various printing techniques are summarized [31, 34] in Tab. 2.1.

Table 2.1.: Specification of various printing techniques

Technique	Resolution (μm)	Printing speed (m/min)	Film thickness (μm)	Viscosity (mPa s)
Inkjet	30 – 50	1 – 100	0.3 – 20	1 – 40
Screen	50 – 100	10 – 100	3 – 100	500 – 5000
Gravure	20 – 75	20 – 1000	0.1 – 5	2 – 200

2.3.2. Metal oxide semiconductors

In printed thin-film technology, a wide variety of materials can be chosen for the fabrication of semiconductor, dielectric and electrode materials. Among them, the semiconductor materials are the most important one which determine the performance of the transistors. Potential printable semiconductors can be organic, inorganic metal oxide and 1-D/2-D materials. As introduced in chapter 1.1.1, organic semiconductors have been the leading force in the field of printable semiconductors, which feature low-temperature processability and good compatibility with flexible substrates. However, they suffer from low intrinsic mobility which limits the device performance and applications. As predicted by the OE-A roadmap [35], the upper limit of mobility of organic semiconductors in commercially available quantities lays merely around $10\,cm^2\,V^{-1}\,s^{-1}$, while the further development to achieve higher mobility ($>10\,cm^2\,V^{-1}\,s^{-1}$), comparable with silicon-based semiconductor, needs to rely on inorganic and nanomaterials.

Alternatively, metal oxide semiconductors have been considered as promising materials due to their superior charge carrier mobility. Examples are crystalline oxide semiconductors such as CuO, Cu_2O, ZnO and In_2O_3, and amorphous oxide semiconductors such as ZTO, IZO and IGZO. Oxygen

vacancies and metal interstitials in metal oxides cause their semiconducting n-type and p-type behavior, respectively. In the energy band structure, the overlap of oxygen 2p and metal ns orbitals forms a localized valence band and a high dispersive valence band. Consequently, electrons have a low effective mass as compared with holes, leading to a high charge carrier mobility in n-type oxides than in p-type. I.e., in metal oxide semiconductor transistors, the p-type devices are still much inferior in performance in comparison to their n-type counterparts, which hinders the development of complementary metal-oxide-semiconductor (CMOS) logic. In Tab. 2.2, key electrical properties of printed TFTs with various metal oxide semiconductors are listed based on the literature research.

Table 2.2.: Key electrical properties of printed TFTs with various metal oxide semiconductors

Semiconductor	Printing techniques	Mobility ($cm^2\,V^{-1}\,s^{-1}$)	I_{on}/I_{off}	V_{th} (V)	Ref.
IGZO	Inkjet	10.2	2×10^8	2	[36]
IZO	Inkjet	8	1×10^5	2	[37]
Zn_2GeO_4	Transfer	25	2.5×10^3	1	[38]
In_2O_3	Inkjet	13.7	3.5×10^6	−4	[39]
ZnO	Gravure	90	1×10^5	0.25	[40]
Zn_3As_2	Transfer	305	1×10^5	−16	[41]
WSe_2	Inkjet	1	3×10^5	0	[42]

Traditional fabrication methods of metal oxide semiconductors include atomic layer deposition and sputtering, which require a vacuum process. Alternatively, solution-processable precursors have also been widely investigated, which are suitable for printed electronics. However, they often require a high annealing temperature between 300 °C and 400 °C to achieve the complete conversion from precursors to stable metal-oxide-metal bonds. This significantly restricts the usage of flexible substrates that barely withstand high temperature over 300 °C [43, 44]. Recently, efforts have been made to allow the low-temperature process of the metal oxide

thin-film. Alternative strategies are the usage of aqueous solution[45], combustion chemistry [46] and photo-activation annealing [47].

2.3.3. Electrolyte-gating approach

In MOSFETs or TFTs, the gate is separated from the channel by the insulation layer, where dielectric materials are often used. As discussed in section 2.2, the unit gate capacitance C_{OX} per unit area generated by the dielectrics layer is an essential parameter for the functionality of MOSFET. From Eq. 2.13, one can deduce that the current driving ability scales linearly with the value of C_{OX}. I.e., with a higher C_{OX}, sufficient source-drain current can already be induced by the low bias voltage, which is important to realize the low-voltage operation of devices.

By assuming the parallel plate capacitor, the value of C_{OX} can be calculated as below:

$$C_{OX} = \frac{\epsilon_{DEL}\epsilon_0}{t_{OX}}, \tag{2.23}$$

where ϵ_{DEL} is the relative dielectric constant of the dielectric material and t_{OX} is the layer thickness. To increase C_{OX}, one can either increase ϵ_r by utilizing so-call "high-k" dielectrics or reduces the effective thickness of the resulting layer. However, both approaches are difficult in the domain of printed electronics, since stable and solution-processable "high-k" dielectrics are rare, and the printing process limits the thickness of printed materials (normally between several hundreds of nm). Until now, TFTs with both dielectric and semiconductor materials printed are often operated at high voltages (> 10 V) [48, 49, 50]. This largely hinders the realization of printed low-voltage devices to satisfy the requirements of potential applications in e.g. IoT and wearable devices, where batteries that can supply high voltages are often not available.

Alternatively, solid electrolytes can be utilized to replace conventional dielectric materials. The so-called electrolyte-gating approach is especially beneficial for the development of printed electronics from various aspects.

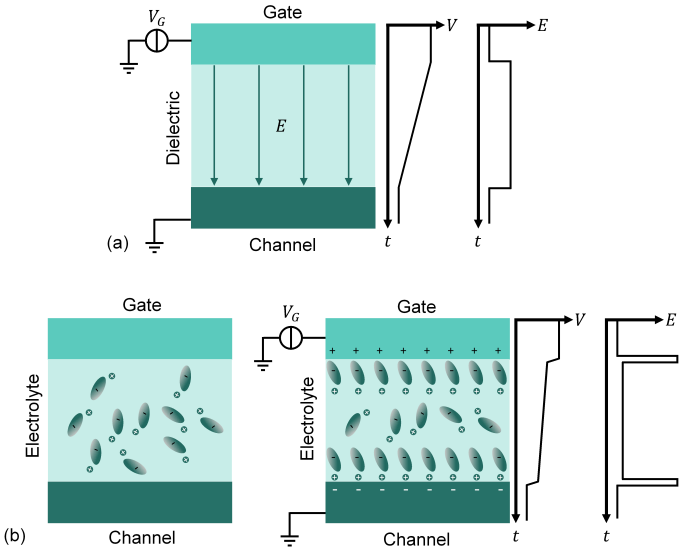

Figure 2.12.: Schematics of charge mechanism of (a) dielectric-gating and (b) electrolyte-gating approach.

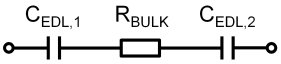

Figure 2.13.: Basic equivalent circuit model of electric double layers consisting of two double layer capacitance $C_{EDL,1}$ and $C_{EDL,2}$, and the R_{BULK} representing the ionic resistance of the bulk electrolyte.

The primary motivation to deploy electrolytes as gating materials is the large gate capacitance produced by electric double layers (EDLs), effectively inducing a strong electric field at the channel surface already at low voltage. The advantage of electrolyte-gating can be seen by comparing with the distribution of electric field in conventional dielectric-gating.

As illustrated in Fig. 2.12(a), in conventional dielectric-gating, upon the application of the gate voltage V_G, the potential drops across the bulk of the dielectric layer, and a constant electric field is generated. In the electrolyte-gating system as shown in Fig. 2.12(b), as the positive gate voltage is applied, anions are attracted to the gate-electrolyte interface, while cations are repelled to the electrolyte-channel interface causing the charge carrier accumulation on the semiconductor surface. At the steady-state, almost all of the applied potential is dropped across those two interfaces, whereas the potential drop across the electrolyte bulk is small. Consequently, so-called EDLs are formed at the interfaces that possess a high electric field.

Furthermore, the electric double layer capacitor C_{EDL} can be considered as two parallel plate capacitors in series connection. In Fig. 2.13, the basic equivalent circuit model of EDLs is presented, where $C_{EDL,1}$ and $C_{EDL,2}$ are the two EDLs at each interface and R_{BULK} represents the ionic resistance of the bulk electrolyte. Since $C_{EDL,1}$ and $C_{EDL,2}$ are in series connection, the total capacitance in a double layer structure is:

$$\frac{1}{C_{EDL,total}} = \frac{1}{C_{EDL,1}} + \frac{1}{C_{EDL,2}}. \tag{2.24}$$

In each capacitor, the thickness between two plates is in the nanometer range, defined as the Debye screening length λ_D. Based on the capacitance equation:

$$C_{EDL} = \frac{\epsilon_r \epsilon_0}{\lambda_D}, \tag{2.25}$$

the double layer capacitance can easily exceed $1\,\mu F\,cm^{-2}$ by assuming $\lambda_D = 1\,nm$ and $\epsilon_r = 10$, which is at least one order of magnitude higher than the value that is attainable in conventional dielectric systems. More importantly, the high capacitance value is independent of the thickness of the resulting electrolyte layer. In Tab. 2.3, a comparison of the attainable unity capacitance and layer thickness is given between the dielectric and electrolyte materials used as gate insulators.

Table 2.3.: Comparison of the areal capacitance and layer thickness between the dielectric and electrolyte materials

Material	Areal capacitance ($\mu F\,cm^{-2}$)	Layer thickness (nm)	Ref.
	Dielectric		
TiO_2	0.373	97	[51]
Al_2O_3	0.7	6.5	[52]
Ta_2O_5	0.136	160	[53]
	Electrolyte		
$PEO/LiCLO_4$	5	400	[54]
Ionic Liquid	6	$5{\cdot}10^4$	[55]
Ionic Gel	12	$2{\cdot}10^3$	[56]

Additionally, electrolyte-gating possesses more advantages. For example, many solid electrolytes are inherently printable [57, 58]. Also, it helps to realize unique material stacks to achieve new device architecture, such as the in-plane devices [59, 60]. In particular cases, electrolytes are conformable and can wet porous and rough structures effectively, which are the surface property often possessed by printed materials [61]. All those features make this technique a viable approach to fabricate printed TFT devices, which is suitable for low-voltage operation.

2.4. EGT technology

In this thesis, the key device under study is the electrolyte-gated field-effect transistors (EGT) incorporating indium oxide semiconductors. It utilizes precursor-derived inorganic semiconducting material which assures a high effective charge carrier mobility. Also, the deployment of electrolytes as the gate insulator provides a high gate capacitance to induce sufficient drain-source current already at low voltages. As a result, the advantages

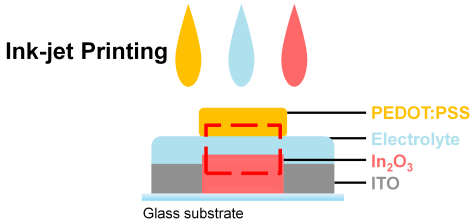

Figure 2.14.: Material stack of EGT.

of high performance and low-voltage operation are combined in inkjet-printed transistors. Here, the technical background of EGT is explained, including its fabrication process and the I-V modeling approach.

2.4.1. Fabrication

Fig. 2.14 illustrates the material stack of EGT. To fabricate the device, passive patterns for source, drain and gate electrodes are structured on ITO sputtered glass using e-beam lithography. Then, the precursor $In(NO_3)_3 \cdot \times$ H2O ink is inkjet-printed between source and drain electrode. Through a subsequent annealing process at 400 °C, the In_2O_3 channel is formed. Next, the lithium-ion based composite solid polymer electrolyte (CSPE) is prepared by mixing two solutions: 0.05 g of $LiCLO_4$ dissolved in 0.45 g propylene carbonate (PC), and 0.213 g of Polyvinyl alcohol (PVA) dissolved in 4.29 g of dimethyl sulfoxide (DMSO). The mixture solution is printed on top of the channel, fully covering the channel region and partially overlapping with source and drain electrodes. Until now, the EGT with in-plane architecture has been realized if CSPE also connects with the gate electrode. To fabricate the top-gate architecture, the additional conductive polymer poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) is printed on the top of CSPE while connecting to the gate electrode.

2.4.2. I-V modeling

To enable the circuit simulation, the static I-V characteristics of EGTs have to be modelled. Here, the extended Enz–Krummenacher–Vittoz (EKV) model has been used [62, 63]. The drain-source current equation is defined as below:

$$I_{DS} = I_0 \cdot (ln(f_3 + e^{\frac{v_p - v_s}{2}})^\gamma - ln(f_3 + e^{\frac{v_p - v_d}{2}})^\gamma), \tag{2.26}$$

$$I_0 = 2nf_1 \frac{W}{L} \phi_t^2, \tag{2.27}$$

$$n = \frac{1}{S \cdot \phi_t \cdot ln(10)}, \tag{2.28}$$

where n is the slope factor and S is the sub-threshold slope; v_p, v_s and v_d represent channel, source and drain voltage normalized by the thermal voltage ϕ_t, which are expressed as below:

$$\phi_t = \frac{k_B T}{q} = \frac{V_D}{v_d} == \frac{V_S}{v_s}, \tag{2.29}$$

$$v_p \approx \frac{V_{GS} - (V_{th} - f_4 V_{DS})}{\frac{n}{f_2}\phi_t}, \tag{2.30}$$

with k_B as the Boltzmann constant, T the temperature, q the elementary charge and V_{th} the threshold voltage; f_{1-4} are fitting parameters which tune the modelled I-V characteristics in different regions.

3. Capacitance in EGTs

3.1. Background

As an emerging technology, printed electronics finds its niche applications due to its unique features such as on-demand fabrication and realization of flexible electronics. Especially, to realize low-voltage operation (<1 V), the electrolyte-gating approach has received increasing interest in the field of printed electronics. As already explained in section 2.3.3, this feature is enabled by the large gate capacitance provided by electric double layers.

To facilitate the development of sophisticated circuits in a large scale using printed electrolyte-gated transistors, a proper PDK dedicated to the printed electronics is required. As mentioned in section 1.2, compact capacitance modeling is the essential part in PDKs. In this chapter, the EGT capacitance is systematically characterized. Then, a study is performed, how the intrinsic capacitance affects the dynamic performance of EGT devices and circuit. Finally, a simulation program with integrated circuit emphasis (SPICE)-compatible Meyer-like model is developed based on experimental data of capacitance-voltage characteristics, which can enable accurate transient and AC circuit simulations.

3.2. Characterization method

3.2.1. Impedance Spectroscopy

Impedance spectroscopy is a powerful tool to characterize various electrochemical systems, such as batteries, fuel cells and electric double layers [64]. It is performed by applying sinusoidal AC voltage signal to the device under test (DUT), which is can be expressed by:

$$V(t) = |V_0|e^{j2\pi ft}, \tag{3.1}$$

where $|V_0|$ is the signal amplitude and f is the signal frequency. In most cases, the applied AC signal has a small amplitude that produces a linear response. Then, based on the assumption of a linear system, the current response $I(t)$ can be measured upon the application of $V(t)$ and expressed as a complex quantity:

$$I(t) = |I_0|e^{j(2\pi ft+\varphi)}, \tag{3.2}$$

where φ is the phase shift between $V(t)$ and $I(t)$.

Therefore, the impedance of DUT can be calculated as:

$$Z = \frac{V(t)}{I(t)} = \frac{|V_0|e^{j2\pi ft}}{|I_0|e^{j(2\pi ft+\varphi)}} = |Z|e^{-j\varphi}, \tag{3.3}$$

where $|Z|$ is the magnitude and φ is the phase. Furthermore, as a complex number, $|Z|$ can be also expressed as:

$$Z = R + jX, \tag{3.4}$$

where $R = |Z|\cos(-\varphi)$ is the real part and $X = |Z|\sin(-\varphi)$ is the imaginary part of the impedance.

One effective way to examine the impedance is the Nyquist plot [64], where the real part as the x-axis is plotted against the imaginary part as the y-axis in Cartesian coordinates. There, the frequency information is implicit.

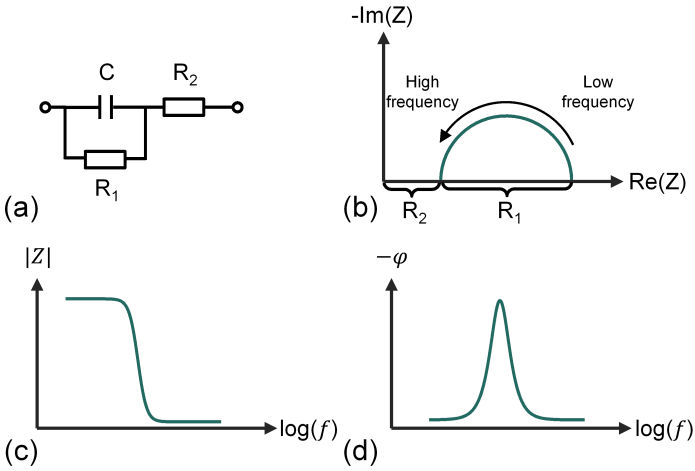

Figure 3.1.: (a) Complex network comprising resistor and capacitor. (b) Nyquist plot of the impedance of the complex R-C network in (a). (c) and (d) Bode plot including the magnitude and phase of the frequency response of the complex R-C network.

Practically, the y-axis is often plotted as the negative imaginary part, since many electrochemical systems show a capacitive behavior. From the Nyquist plot, one can easily examine the types of DUTs. For instance, for resistor devices, the phase information $\varphi = 0$, and the magnitude equals their resistance value:

$$Z_R = R. \tag{3.5}$$

In case DUTs are ideal loss-less capacitors or inductors, their impedance is purely imaginary that can be expressed by:

$$Z_C = \frac{1}{j2\pi fC}, \tag{3.6}$$

and

$$Z_L = j2\pi fL. \tag{3.7}$$

For more complex networks comprising basic electronic components (R, L and C), they can produce certain impedance patterns in the Nyquist plot, which are the basics of the equivalent circuit model. As an example, in Fig. 3.1(a), the resistor-capacitor (R-C) network is considered, which consists of the resistor R_1 and C in parallel connection and the resistor R_2 in series connection. In the quasi-static state, where $f \approx 0$, capacitor C produces a infinitely large impedance. Therefore, it can be treated as an open-circuit, and the total impedance of the network is $Z = R_1 + R_2$. When the frequency is sufficiently high, capacitor C behaves like a short-circuit, and the network impedance becomes $Z = R_2$. In the transition between these two extremes, the total impedance forms a semi-circle above the real part axis, the diameter of which is determined by the value of R_1. The overall impedance response is shown in Fig. 3.1(b).

Another practical method to examine the impedance is the Bode plot. There, the magnitude and phase values are plotted against the frequency respectively, so that the frequency response is presented clearly. The Bode plots of the example circuit are shown in Fig. 3.1(c) and (d). Both plots are used in this chapter to illustrate the complex impedance of the DUT.

3.2.2. Measurement Setup

Following the previous discussion, proper impedance measurement methods are required for the capacitance characterization. Various techniques have been developed [65], including auto-balancing bridge method, radio-frequency current-voltage (RF-IV) method and network analysis method. In Tab. 3.1, their specifications on the impedance and frequency ranges are compared. As can be seen, the auto-balancing bridge method provides the widest impedance and frequency range. As the low-frequency measurement below 1 kHz is required in this work, the auto-balancing bridge method is preferred for the study.

Fig. 3.2 shows the circuit schematic of the auto-balancing bridge method. To perform accurate impedance measurements, the oscillation voltage V_{osc} is applied on the DUT through the high current (H_c) terminal, while

Table 3.1.: Specification of various impedance measurement techniques

Measurement technique	Frequency range	Impedance range
Auto-balancing bridge	20 Hz-110 MHz	1 mΩ-100 MΩ
RF-IV	1 MHz-3 GHz	0.2 Ω-20 kΩ
Network analysis	>300 kHz	$\approx Z_0$*

*Z_0 is the characteristic impedance of the measurement instrument.

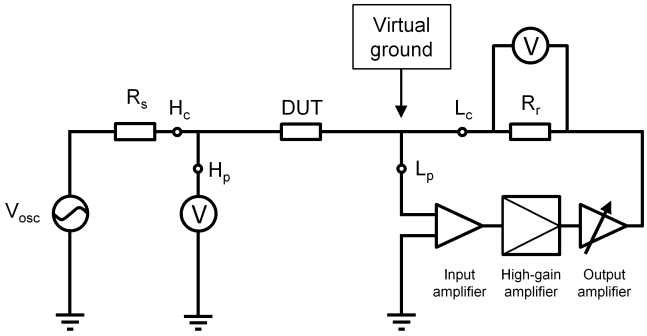

Figure 3.2.: Circuit schematic of the auto-balancing bridge method for low frequency impedance measurement.

the applied voltage is measured by a voltmeter at the high potential (H_p) terminal. The resulting current flows through the DUT to the low current (L_c) terminal. The current signal is measured through the shunt resistors R_r and measured by the voltmeter. At the L_c terminal, if potential exists, an additional current will be generated through the stray capacitance between the terminal and ground. Therefore, it is necessary to create virtual null potential at the L_c terminal. This is accomplished by introducing the low potential (L_p) terminal, which is connected to the L_c terminal in a feedback loop through the null amplifier consisting of an input amplifier, high-gain amplifier and output amplifier. Eventually, the so-call "four-terminal pair" configuration is used to assure a high accuracy and minimal error factor in the measurement path.

3.3. Dynamic performance

Despite the recent progress in modeling the static behavior of EGTs [62, 66, 67], the understanding of their dynamic performance has received less attention. Therefore, the study of intrinsic capacitance is essential, which influences the dynamic performance of EGTs significantly. As an approximation for the basic analysis, test structures such as metal-electrolyte-metal or metal-electrolyte-semiconductor have been often used to investigate the charging behavior of EDLs [68, 61, 69, 70], similar to the MOS analysis for MOSFETs. However, such approaches fail to reproduce the impact of the overall capacitance on the dynamic performance of real transistor devices, due to the difference in device dimensions, material stacks, and fabrication processes. Furthermore, the strong bias-dependency of EDL capacitance is often neglected, which has a significant influence on the AC characteristics of EGTs in circuits.

In this regard, a direct in-depth experimental analysis of EGT capacitance is required. Proper test structures are necessary to differentiate the intrinsic and extrinsic effects of transistor capacitance. Using impedance spectroscopy, the bias-dependent frequency response of the gate capacitance is characterized. Based on the equivalent circuit and parameter extraction, frequency characteristics are accurately modelled. Consequently, important information about the impact of intrinsic capacitance on the device dynamic behavior is revealed, which also sheds light on the material optimization to improve the performance of EGTs.

3.3.1. Experiment configuration

In this study, two types of the EGT architecture are of interest, namely the in-plane and top-gate structures. The first one, often also called the displaced-gate configuration, is a unique type that can be realized by the electrolyte-gating technology. The three-dimensional electric field within the CSPE allows the position of the gate electrode at the same plane as the source and drain electrodes. To realize the top-gate architecture based on

the in-plane one, the additional PEDOT:PSS is printed on top of the electrolyte, that vertically covers the channel region. In this way, a stronger electric field is induced by the top-gate as compared to the in-plane gate counterpart, enhancing the DC performance. Since the ions need to migrate less distance within the electrolyte, the top-gate architecture is also predicted to possess a superior AC performance. However, the in-plane gate architecture is sometimes advantageous since less printing steps are involved.

During the printing process, overlap areas can occur e.g. between the source and drain electrodes and electrolyte. Since the ITO electrodes behaves as metals, electric double layers are also formed there. This resulting capacitance is an unwanted extrinsic effect, often referred to as the overlap capacitance. In inkjet technologies, the printing resolution is typically low. This leads to significant overlap capacitance, even comparable with the intrinsic capacitance from the EDLs at the channel/electrolyte interface. Therefore, the overlap capacitance needs to be treated carefully during the capacitance characterization of EGTs.

To this end, so-called de-embedding devices are prepared in the experiment for both architectures, where the printing of the channel material is skipped, while the remaining fabrication parameters and dimensions are kept the same as in normal EGTs. This enables the independent characterization of the overlap capacitance. Furthermore, the comparison between the normal EGTs and de-embedding devices allows a clear observation of the intrinsic effect from the channel capacitance. In Fig. 3.3, material stacks and 3-D top view schemes of both architectures are presented with the illustration of their de-embedding devices without channel. Channel width W and length L of all devices are 200 µm and 50 µm, respectively, while overlap width t on the source and drain electrodes is 50 µm.

In EGTs, one of the EDL capacitors, namely $C_{G/E}$, is at the gate/electrolyte interface, while the another, $C_{E/CH}$, is at the electrolyte/semiconductor interface. Notably, a large $C_{G/E}$ is necessary to produce a small impedance. Consequently, $C_{E/CH}$ is charged more effectively. To realize this, in the test structure of in-plane devices, the contact area between the gate electrode

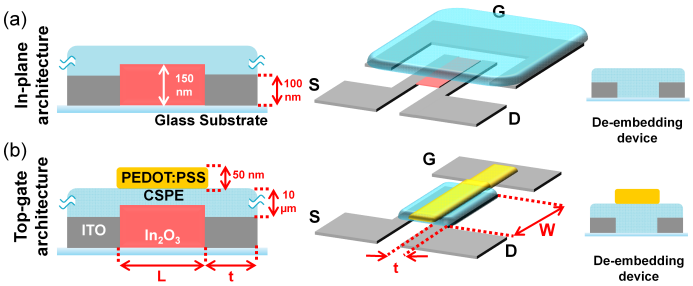

Figure 3.3.: Material stacks and 3-D top view schemes of (a) in-plane and (b) top-gate architectures. L and W are the device channel length and width, while t is the width of the overlap region between source/drain electrodes and electrolyte. For each architecture, their de-embedding test structure without channel materials are also fabricated. Reprint with permission from [71] ©2019 IEEE.

and electrolyte is designed as an area 10 times larger than that between electrolyte and channel, as shown in Fig. 3.3(a). For top-gate architecture, it is observed that top-gate material PEDOT:PSS penetrates the electrolyte, creating a 3-D contact there. Consequently, large $C_{G/E}$ is produced without the design of the large top-gate area.

3.3.2. Static I-V characteristics

Prior to the capacitance measurements on the aforementioned test structures, the static I-V characterization is performed to correlate the AC and DC behaviors of EGTs. The Agilent 4156C semiconductor parameter analyzer is used to apply terminal bias voltages on the DUTs through Cascade EPS150 probe station. As revealed by related studies, the electrolyte is sensitive to the environmental humidity [72]. Therefore, experiments are conducted under a controlled environment with a relative humidity of around 50 % and room temperature of 298 K.

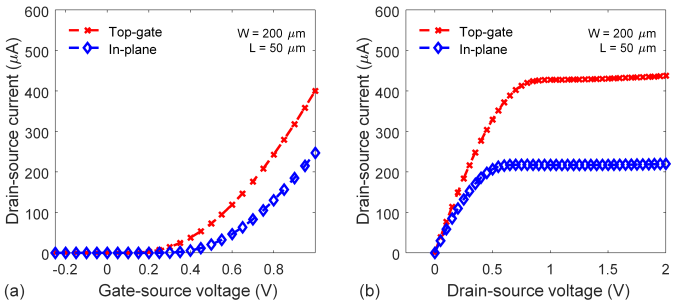

Figure 3.4.: Comparison of the typical steady state I-V characteristics of EGTs with top-gate and in-plane architecture: (a) transfer curves and (b) output curves. Reprint with permission from [71] ©2019 IEEE.

Fig. 3.4 shows the difference of the static I-V characteristics of EGTs with top-gate and in-plane architectures. One can note that the drain current of the top-gate device is nearly two times higher than that of the in-plane device. Also, the extracted threshold voltage V_{th} of the top-gate device is 0.07 V, significantly lower than the extracted in-plane device at 0.26 V. This difference in I-V characteristics can be already attributed to the higher gate electric field in top-gate devices, resulting in a strong charge accumulation and reduced channel resistance, as discussed in [73].

3.3.3. Capacitance characteristics

The intrinsic capacitance of EGTs is characterized using the auto-balancing bridge method as discussed earlier. The environmental parameters are controlled similarly as in the I-V characteristics. To characterize the gate capacitance C_{GG}, source and drain terminals are short-circuited. Then, the bias voltage V_{GG} ranging from −0.3 V to 0.9 V is applied at the gate terminal, which is superimposed by a sinusoidal signal V_{osc}. During experiments, the amplitude of V_{osc} is set to a small value of 20 mV to satisfy the condition of the linear response. For top-gate devices, the frequency of

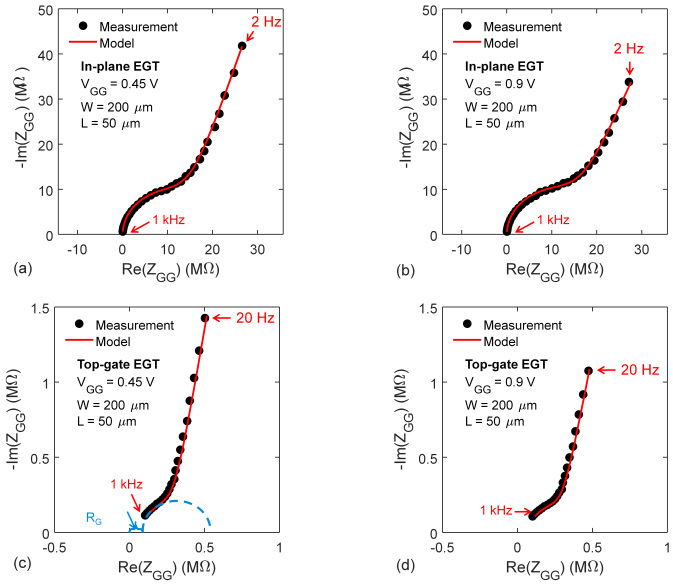

Figure 3.5.: Measured and modelled gate impedance Z_{GG} in Nyquist plots at gate voltage V_{GG} of 0.45 V and 0.9 V. (a) and (b) are data of the in-plane EGT, while (c) and (d) are of the top-gate EGT. Using the auxiliary line, a gate resistance $R_G \approx 50\,\text{k}\Omega$ at the bias voltage of 0.45 V in the equivalent circuit can already be graphically determined in (c). Reprint with permission from [71] ©2019 IEEE.

V_{osc} is swept from 20 Hz to 1 kHz using Keysight LCR Meter 4980A. Since in-plane devices are generally slower, the frequency is adjusted to from 2 Hz to 1 kHz, and the characterization of those devices are accomplished by Biologic SP150 Potentiostat.

Fig. 3.5(a)-(d) show measured gate impedance Z_{GG} of two device architectures at gate voltage V_{GG} of 0.45 V and 0.9 V, respectively. Although the impedance spectra differ between device architectures and gate voltages in values, a general form can be observed in the Nyquist plot, which can be divided into three regions. At low frequencies, a tilted line represents

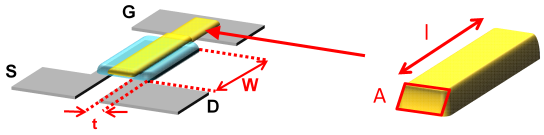

Figure 3.6.: The printed top-gate material can be assumed as a long, cuboid structure with the cross section area A of 50 µm × 50 nm, and the length l of 400 µm.

the frequency response of EDL capacitance. As the gate voltage changes, the position of the tilted line is also changing, indicating the voltage dependency of the EDL capacitance. Then, at the intermediate frequency, gradually, the measured impedance spectra form a part of a circle. Here, because ions within electrolytes fail to follow the applied oscillation signal at the gate, the effect of ionic conductivity starts to dominate. Finally, at sufficiently high frequency, the impedance spectra approach the real axis, as illustrated in Fig. 3.5(c) with the help of extrapolation of the circle. The resulting value on the real-axis is attributed to the effect of gate resistance.

For EGTs with the top-gate architecture, low conductive material PEDOT:PSS is employed as the top-gate material. Therefore, the value of the gate resistance is significant. It can be roughly estimated by considering the top-gate as a long, cuboid structure as shown in Fig. 3.6 with the cross-section area A of 50 µm × 50 nm, and the length l of 400 µm. By using the specific resistivity σ of 30 S cm^{-1}, which is commonly obtained by printed PEDOT:PSS materials, the gate resistance can be calculated using:

$$R = \frac{l}{\sigma A}. \tag{3.8}$$

Then, the top-gate resistance R_{TG} value of 53 kΩ can be estimated, which is consistent with the graphical readout in Fig. 3.5(c).

Based on the discussion of the general form of measured impedance spectra, an equivalent circuit model can now be built to accurately reproduce the overall frequency response at various gate voltage.

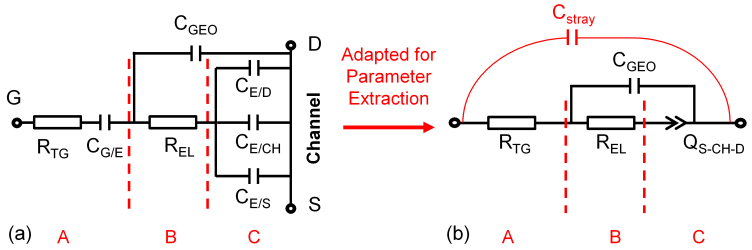

Figure 3.7.: Schematics of (a) overall equivalent circuit model for in-plane and top-gate EGTs in the accumulation region, and (b) adapted model for the parameter extraction. Both models can be divided into three parts, corresponding to the (A) electrolyte-gate interface, (B) electrolyte bulk and (C) electrolyte-channel interface including the overlap regions on the source/drain electrodes. Reprint with permission from [71] ©2019 IEEE.

3.3.4. Equivalent circuit models

The equivalent circuit models have been widely used to characterize electrochemical systems such as EDLs. Opposed to simple sandwiched structures [74, 75], EGTs contains more intrinsic components that need to be captured by the equivalent circuit model.

The analysis begins with the channel/electrolyte interface at accumulation region, where one of the EDL capacitors $C_{E/CH}$ occurs. The resulting impedance is designated as $Z_{E/CH}$. Following the transmission line approach [76], the impedance at the electrolyte/channel interface $Z_{E/CH}$ can be expressed by

$$Z_{E/CH} = \frac{1}{j2\pi f C_{E/CH}} + \frac{R_{CH}}{12}, \tag{3.9}$$

where f is the frequency and R_{CH} is the channel resistance. In the above threshold region, $R_{CH}/12$ has the impedance value in hundred Ω range, which is considerably lower than the contribution of $C_{E/CH}$ in Eq. 3.9. Consequently, R_{CH} is negligible, and $Z_{E/CH}$ can be simply expressed by:

$$Z_{E/CH} = \frac{1}{j2\pi f C_{E/CH}}. \tag{3.10}$$

In the depletion region, $C_{E/CH}$ is zero since the EDL capacitance is not established, and R_{CH} is also zero short-circuited by the external connection.

Next, the counter EDL capacitor is formed at the gate electrode side of the EGTs, named here as $C_{G/E}$. Considering the finite resistance of the gate material, the top-gate resistance R_{TG} is connected with $C_{G/E}$ in series. Also, the two double-layer capacitors, namely $C_{G/E}$ and $C_{E/CH}$, are electrically connected to the electrolyte bulk resistance R_{EL}, representing the mobility of ions in the electrolyte. Additionally, the geometric capacitance C_{GEO} is located between the gate and the short-circuited source/drain terminal, accounting for the dielectric bulk effect due to the permittivity of the electrolyte.

Furthermore, apart from the channel region, EDL capacitor also arise due to overlap regions between the electrolyte and source/drain electrodes, namely $C_{E/S}$/$C_{E/D}$, . Electrically, they are in parallel connection to the channel capacitance $C_{E/CH}$. Finally, the overall equivalent circuit model has been developed for EGTs as presented in Fig. 3.7(a), applicable for both in-plane and top-gate architectures as well as their de-embedding structures.

It is laborious to analytically determine the values of all components in the equivalent circuit model due to the complex electric field and structures within EGTs. However, they can be extracted by parameter fitting using experimental data as obtained in Fig. 3.5.

Before that, the model in Fig. 3.7(a) can be further adapted to reduce the number of components. First, as explained before, $C_{G/E}$ is sufficiently large in both architectures to produce negligible impedance . Therefore, $C_{G/E}$ can be eliminated from the circuit. Second, $C_{E/CH}$, $C_{E/S}$ and $C_{E/D}$ can be treated as a single component, C_{S-CH-D}, due to their parallel connection. As shown in Fig. 3.5(a)-(b), the effect of C_{S-CH-D} generates the titled line in the low frequency regime. However, it deviates from the behavior of an ideal capacitor that produces straight lines perpendicular to the real axis. This indicates the frequency dispersion behavior that can be attributed to the surface roughness and adsorption effects [61, 77, 78, 79]. For this

reason, it is appropriate to model the C_{S-CH-D} as a constant phase element (CPE) Z_{S-CH-D} that can be expressed as

$$Z_{S-CH-D} = \frac{1}{Q_{S-CH-D} j\omega^{\alpha_{CPE}}}, \tag{3.11}$$

where Q_{S-CH-D} represents the frequency-dependent capacitance with the unit of $\mathrm{F} \cdot \mathrm{s}^{\alpha_{CPE}-1}$, $\alpha_{CPE} \leq 1$ is the non-ideal factor of CPE. When $\alpha_{CPE} = 1$, the CPE element describes an ideal capacitor. In the following analysis, the value Q is used to present the charge capacity. Third, an additional C_{stray} is placed in parallel to the whole equivalent circuit to account for the stray capacitance from the cabling and instrumentation. It has a constant value in the range of 10^{-10}F that is obtained by the open circuit measurement. Finally, the Fig. 3.7(b) shows the adapted equivalent circuit with a reduced number of components. To demonstrate the physical interpretation, the adapted equivalent circuit can be divided into three parts, namely the electrolyte-gate interface (A), electrolyte bulk (B), and electrolyte-channel/source/drain interface (C).

3.3.5. Parameter extraction

The extraction of parameters in the adapted equivalent circuit in Fig. 3.7(b) is essentially an optimization problem of the multi-variable function. Additionally, all parameters have constrained boundaries, e.g. they need to be positive and $\alpha_{CPE} > 1$. Therefore, an extraction routine is developed based on interior point method. The Broyden–Fletcher–Goldfarb– Shanno (BFGS) approximation [80] is chosen to determine the Hessian, while gradients are evaluated using forward finite differences. To achieve the best fitting, the sum of squares error function is minimized, which is defined as below:

$$SSE = \sum_{n=1}^{N} \sqrt{\mathrm{Re}(\epsilon_n)^2 + \mathrm{Im}(\epsilon_n)^2} \tag{3.12}$$

with $\epsilon_n = \hat{Z}_{GG,n} - Z_{GG,n}$, where $\hat{Z}_{GG,n}$ and $Z_{GG,n}$ are the nth measured and simulated impedance value. N is the total number of frequency points at

each gate voltage V_{GG}. Measurement data are grouped by the individual EGT device. In each group, $P = 7$ curves are measured at various V_{GG}.

To design an effective parameter extraction routine, two factors are considered: the algorithm is highly sensitive to the initial conditions; physical parameters in Fig. 3.7 either are constant or change continuously with the increase of the V_{GG}. To this end, a "warm-start" strategy has been implemented. For the impedance spectrum with index variable $P = 1$ that is measured at the lowest V_{GG}, the extraction is performed using the following initial points based on the rough estimation of physical quantities, which can be expressed in the vector:

$$\vec{F}_0 = [R_{G,0} = 1k\Omega, R_{EL,0} = 1k\Omega, Q_{DL,0} = 1nF, \alpha_{CPE,0} = 1, C_{geo,0} = 1nF] \quad (3.13)$$

The extraction ends when the step tolerance is less than 10^{-6}. After the first extracted result is obtained, it is used as the initial points for the next impedance spectrum with index variable $P = 2$. The same process is repeated until the last spectrum $P = 7$ in the group. To assure an equal quality, the extraction routine runs backwards from $P = 7$ to $P = 1$. Finally, the parameter extraction routine can be visualized in Fig. 3.8.

The parameter extraction routine is applied to the measurement data of both in-plane and top-gate architectures, and the extraction results are listed in Tab. 3.2. Also, through the comparison between normal and de-embedding devices, it is possible to observe the pure channel capacitance based on the subtraction:

$$Q_{E/CH} = Q_{S-CH-D} - (C_{E/S} + C_{E/D}), \quad (3.14)$$

which has values only in the accumulation region. Using the $Q_{E/CH}$ data from Tab. 3.2 and the channel area $A = W \times L = 200\,\mu m \times 50\,\mu m$, the specific capacitance per unit area ranging from $23\,\mu F\,cm^{-2}$ to $48\,\mu F\,cm^{-2}$ can be obtained from top-gate EGT. This high value can be attributed to the rough and perhaps slightly porous surface possessed by the printed precursor-derived In_2O_3, which effectively increases the interface areas accessed by electrolyte and, therefore, the capacitance value.

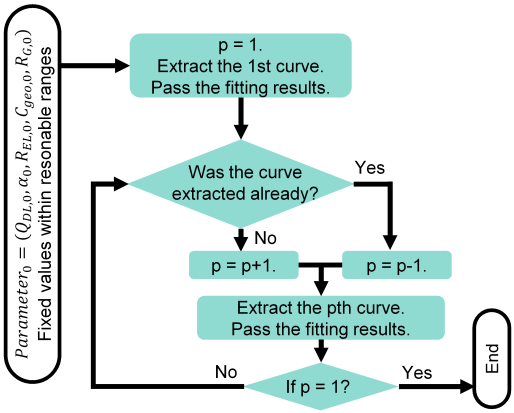

Figure 3.8.: Flow chart of the parameter extraction with the "warm-up" strategy.

The voltage dependency of Q_{S-CH-D} as shown in the Tab. 3.2 has also been frequently observed, which is related to the size, shape and chemical structure of electrolyte ions and electrode materials [70, 81]. Also, the extracted values of $Q_{E/CH}$ in the top-gate EGT are nearly two times that in in-plane ones. This ratio well corresponds to the ratio of the drain-source current between the two device architectures as shown in Fig. 2.5:

$$\frac{Q_{ch,in-plane}}{Q_{ch,top-gate}} \approx \frac{I_{sat,in-plane}}{I_{sat,top-gate}} \approx \frac{1}{2}, \tag{3.15}$$

This can be explained by considering the basic I-V characteristic in the saturation region:

$$I_{DS,sat} = \mu_{FET} C_{E/CH} \frac{W}{L} \frac{(V_{GS} - V_{th})^2}{2}, \tag{3.16}$$

where μ_{FET} is the charge carrier mobility, and $C_{E/CH}$ is represented by $Q_{E/CH}$ here. Furthermore, the ideal factor α_{CPE} is improved through the additional top-gate, indicating a better effectiveness of this device architecture.

Table 3.2.: Parameter extraction results

In-plane EGT					
V_{GG} (V)	$R_G + R_{EL}$ $(M\Omega)$	C_{GEO} (pF)	Q_{S-CH-D} $(nF \cdot s^{\alpha_{CPE}-1})$	$Q_{E/CH}(C_{E/S} + C_{E/D})^{a}$ $(nF \cdot s^{\alpha_{CPE}-1})$	α_{CPE}
−0.30	16.9	26	1.86	− (1.76)	0.85
−0.15	17.5	36	2.11	− (2.23)	0.84
−0.00	17.3	49	2.40	− (2.53)	0.83
0.45	17.1	44	3.87	1.10 (2.77)	0.79
0.60	17.6	52	4.27	1.35 (2.92)	0.78
0.75	17.4	19	4.95	1.94 (3.01)	0.76
0.90	17.6	44	5.32	2.30 (3.02)	0.74

Top-gate EGT						
V_{GG} (V)	R_G $(k\Omega)$	R_{EL} $(k\Omega)$	C_{GEO} (nF)	Q_{S-CH-D} $(nF \cdot s^{\alpha_{CPE}-1})$	$Q_{E/CH}(C_{E/S} + C_{E/D})^{a}$ $(nF \cdot s^{\alpha_{CPE}-1})$	α_{CPE}
−0.30	59.7	178.9	0.43	5.20	− (4.49)	0.75
−0.15	63.2	188.6	0.44	4.52	− (4.52)	0.78
0.00	54.3	191.2	0.47	4.72	− (4.80)	0.79
0.45	53.8	200.1	1.12	7.84	2.31 (5.53)	0.88
0.60	55.2	196.6	1.21	8.82	3.01 (5.81)	0.89
0.75	55.2	193.6	1.26	9.90	3.85 (6.05)	0.90
0.90	54.1	194.2	1.28	11.1	4.80 (6.30)	0.88

[a] $Q_{E/CH} = Q_{S-CH-D} - (C_{E/S} + C_{E/D})$ has values only in the accumulation region.

The extracted value of the geometric capacitance C_{GEO} is only tens of pF for in-plane EGTs, while it is significantly increased in top-gate architecture. This is due to the deployment of the top-gate material, which builds effectively a parallel plate capacitor and enhances the bulk effect.

Due to the small contribution of C_{GEO} in the in-plane EGT, it is hard for the parameter extraction routine to differentiate the R_G and R_{EL}. Therefore, $R_G + R_{EL}$ is presented as a single parameter, which is a constant value about $\sim$ 17 MΩ. Since the electrolyte is directly connected to the gate electrode, R_G has only a small contribution. For top-gate EGTs, the R_G can be extracted independently and has a mean value of 56 kΩ, which is due to the deployment of low conductive PEDOT:PSS as the top-gate material. Moreover, due to the shortened path from the gate to channel, the value of R_{EL} is largely reduced to $\sim$ 200 kΩ.

Conclusively, the deployment of the top-gate architecture brings benefits to the device performance from various aspects: it largely reduces the resistive bulk effect of the electrolyte, leading to a stronger electric field from the gate to channel; The channel capacitance is almost doubled in comparison with the in-plane architecture, resulting in a stronger charge accumulation; The charging process of the channel capacitance is more effective, as indicated by the ideal factor in the CPE element.

As shown in Fig. 3.5, the proposed equivalent circuit model accurately reproduces the measured impedance. Also, an accurate fit of the frequency response is provided as shown in Fig. 3.9, where the dynamic performance of EGTs can be further analyzed.

3.3.6. Frequency response

The measured and modelled frequency characteristics of gate capacitance $C_{GG} = 1/(2\pi f Im(Z))$ and loss $G = Re(1/Z)$ are shown in Fig. 3.9. Using the parameter extraction routine proposed before, a satisfactory agreement between the measurement and model is achieved.

Also, the frequency response reveals important information about the dynamic performance. In both architectures, the gate capacitance C_{GG} decreases monotonically with increased frequency. This is due to the reduced number of ions that cannot follow the high frequency signal to effectively form the EDLs. On the other hand, the loss-frequency plot can

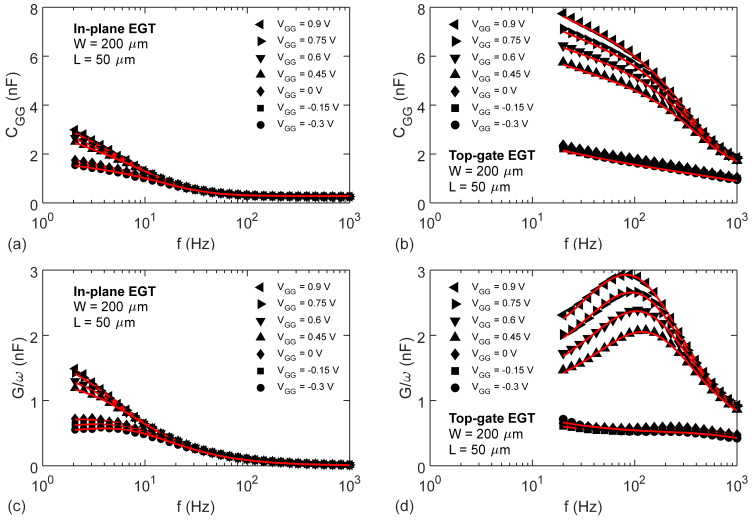

Figure 3.9.: Measured and modelled frequency response of gate capacitance $C_{GG} = 1/(2\pi f Im(z))$ and loss G/ω, $G = Re(1/Z)$, of EGTs with in-plane and top-gate architecture. Reprint with permission from [71] ©2019 IEEE.

reach a maximum for the top-gate EGT operating in the accumulation. This indicates the maximum speed of EGT's operation, which is often referred to as the electrolyte cut-off frequency f_C [82]. For example, at the gate voltage of 0.9 V, the f_C reaches 91.7 Hz, consistent with the measurement result of fabricated ring oscillator in related work [83]. On the contrary, for the loss characteristics of in-plane EGT, the peak is not clearly shown within the frequency range of the measurement. This indicates the cut-off frequency f_C smaller than 2 Hz, which is nearly two orders of magnitude lower than top-gate devices. As discussed, the superior dynamic performance of top-gate EGT is due to the largely reduced electrolyte bulk resistance.

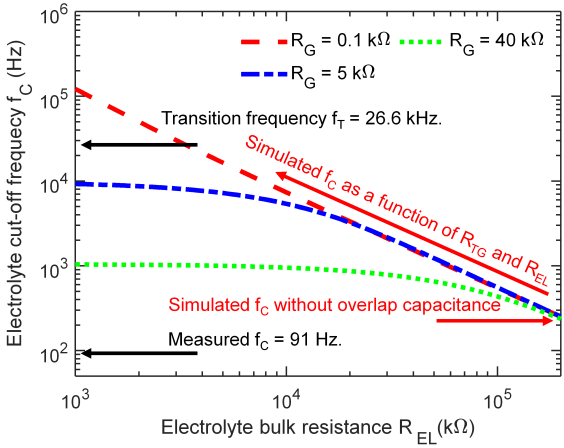

Figure 3.10.: Simulation of the electrolyte cutoff frequency f_C as a function of top-gate resistance R_{TG} and electrolyte resistance R_{EL} evaluated by the frequency characteristics of the loss G/ω, $G = Re(1/Z)$. The calculation of the transition frequency f_T is described in the text. Reprint with permission from [71] ©2019 IEEE.

To this end, simulation results are generated in MATLAB to show quantitatively, how the electrolyte cut-off frequency f_C can be increased. Here, the equivalent circuit model developed in Fig. 2.13 is used. To simplify the analysis, extraction results in Tab. 3.2 of the top-gate EGT at 0.9 V are utilized. Based on the equivalent circuit, Fig. 3.10 presents the simulated electrolyte cut-off frequency as a function of top-gate resistance R_{TG} and electrolyte resistance R_{EL} evaluated by the frequency at the peak loss G/ω. As can be seen, upon the removal of the overlap capacitance, the f_C can be increased to 226 Hz. Additionally, reductions in R_{TG} and R_{EL} can significantly improve the f_C. Through the reduction of the R_{EL} by two orders of magnitude unilaterally, the cut-off frequency approaches 1 kHz. With the low R_G of 0.1 kΩ, even f_C up to 10 kHz can be obtained.

Practically, the reduction of R_{EL} and R_{TG} is feasible by using printable materials with a higher electric or ionic conductivity. Also, a smaller R_{EL} can be achieved by printing a thinner electrolyte layer, given that the top-gate material does not penetrate into the electrolyte. Furthermore, overlap capacitance can be reduced via a more precise printing process to improve the overall dynamic performance.

Besides the electrolyte cut-off frequency, the maximal attainable frequency of EGT is also limited by the transition frequency f_T. Above the f_T, the current gain becomes less than unity. It can be calculated as below:

$$f_T = \frac{\mu_{FET} \cdot (V_{GS} - V_{th})}{2\pi L^2}. \tag{3.17}$$

Using the μ_{FET} evaluated in the previous related work [61], printed In_2O_3 has the $f_T = 26.6\,\text{kHz}$ with the channel length $L = 50\,\mu\text{m}$ at the $V_{GS} = 0.9\,\text{V}$.

Conclusively, as can be seen in Fig. 3.10, the measured cut-off frequency is still more than two orders of magnitude lower than the transition frequency. This indicates a huge space for the optimization of the attainable maximal frequency of the EGT, including new printable top-gate materials with less resistivity, a thinner electrolyte layer with higher ionic conductivity, and a more precise printing process to reduce the overlap capacitance.

3.4. Compact capacitance modeling

In the previous section, the limitations of the maximal frequency have been systematically studied with the help of the equivalent circuit model. In this section, a compact capacitance model for EGT will be developed to enable accurate circuit simulations. To this end, the characterization of lumped terminal capacitance as a function of the bias voltage is necessary. For dielectric-based silicon and organic field-effect transistors [84, 82, 85], analytical compact models have been developed. Novel modeling

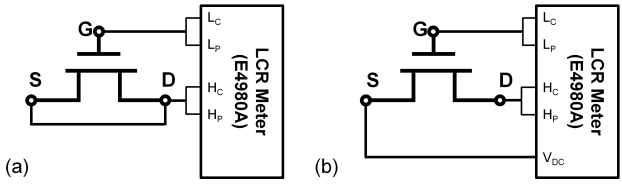

Figure 3.11.: Measurement setup of (a) gate-terminal capacitance and (b) source and drain terminal capacitances. Reprint with permission from [87] ©2019 IEEE.

techniques such as neural networks [86] have been studied but not yet applied to electrolyte-gated transistors. To develop the proper model for inkjet-printed EGTs, one needs to consider the dependency of EDL capacitance on the bias voltage [71, 70, 81]. Additionally, extrinsic parasitic capacitance is often claimed as a major factor, which limits the dynamic performance of printed circuits due to the low printing resolution of existing techniques.

3.4.1. Experiment configuration

In this section, printed EGTs with the top-gate architecture is focused on, because they offer superior electrical performance as revealed in the previous section. Similar to the previous study, to properly separate the extrinsic and intrinsic effects, both normal transistor devices and de-embedding structures without channel materials are prepared as illustrated in Fig.3.3(b). Here, the characterized EGTs have the channel geometry of length $L = 60\,\mu m$ and width $W = 100\,\mu m$. The overlap region between the electrolyte and source/drain electrodes has a width of $t = 100\,\mu m$.

To establish an accurate compact capacitance model that can be used in circuit simulators, lumped terminal capacitance are of interest, the values of which depend on bias voltage V_{GS} and V_{DS}. In Fig. 3.11, the measurement setup is illustrated. All terminal capacitances are experimentally characterized by voltage-dependent impedance measurement using

a Keysight E4980A LCR meter. Measurements are performed through a Cascade EPS150 probe station at the room temperature of 298 K.

In Fig. 3.11(a), the gate terminal capacitance C_{GG} is firstly characterized. Here, the gate of EGT is connected to the L_c and L_p terminals of the LCR meter, whereas the source and drain are electrically short-circuited and then connected to the H_c and H_p terminals. A step-wise DC voltage V_{GG} sweeps at the gate terminal from 0 V to 1 V, which is superimposed by the AC small-signal with the frequency of 40 Hz and amplitude of 10 mV. Secondly, as presented in Fig. 3.11(b), the drain and source terminal capacitances C_{GD} and C_{GS} are characterized. Here, one of the source and drain is connected to the H_c and H_p terminals of the LCR meter, while another one is connected to a DC voltage source. In this way, V_{GS} and V_{DS} are biased independently. To calculate the capacitances, Eq. 3.6 is utilized. In this work, the effect of C_{DS} is considered as a negligible effect, since the source and drain electrodes are separated by a long distance as compared with the thickness of the electrolyte. Both kinds of characterization have been performed on normal EGTs and their de-embedding devices.

3.4.2. Extrinsic capacitance

De-embedding test structures allow the independent characterization of extrinsic effects of terminal capacitances. As the positive gate voltage is applied, negative ions in the electrolyte are attracted to the interface between top-gate and electrolyte to form an EDL capacitor. Due to the reasons explained before, this capacitance has a large value and generates negligible impedance during the measurement, which can be neglected in the following analysis. Positive ions are opposed to the interface between source/drain electrodes and electrolyte, generating two overlap capacitances, which are termed here as $C_{GS,ext}$ and $C_{GD,ext}$. Their summation is the extrinsic gate capacitance $C_{GG,ext}$:

$$C_{GG,ext} = C_{GS,ext} + C_{GD,ext}. \tag{3.18}$$

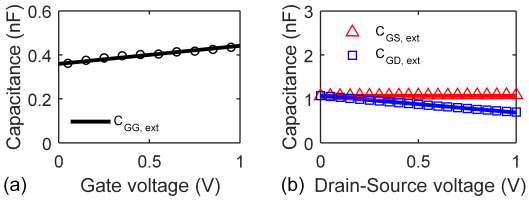

Figure 3.12.: The extrinsic overlap capacitance is characterized independently on the de-embedding test structure with the device geometry of channel length $L = 60\,\mu m$, width $W = 100\,\mu m$ and width of the overlap region $t = 50\,\mu m$. (a) Measured (points) and modelled (lines) extrinsic gate capacitance $C_{GG,ext}$ as a function of V_{GG}. (b) Measured (points) and modelled (lines) extrinsic gate-source capacitance $C_{GS,ext}$ and gate-drain capacitance $C_{GD,ext}$ as a function of V_{DS} at $V_{GS} = 0\,V$. Reprint with permission from [87] ©2019 IEEE.

In Fig. 3.12(a), $C_{GG,ext}$ as a function of V_{GG} is characterized using the measurement setup in Fig. 3.11(a). An almost linear voltage dependency is demonstrated. For EDL systems, this behavior has been frequently observed [81, 88], and fits to the description given by the theory of interfacial tension in EDLs [88]. Using the first-order linear algebraic formula, the experimental data can be well approximated as shown in Fig. 3.12(a):

$$C_{GG,ext} = c_{GS,ext0} + c_{GD,ext1} \cdot V_{GG}, \tag{3.19}$$

where $c_{GS,ext0} = 0.36\,nF$ and $c_{GS,ext0} = 0.11\,nF\,V^{-1}$ as extracted using the linear-mean-square (LMS) method.

Fig. 3.12(b) shows the measured extrinsic overlap capacitance at source and drain, namely $C_{GS,ext}$ and $C_{GD,ext}$, as a function of V_{DS}, while V_{GS} is set to 0 V. One can note that the value of $C_{GD,ext}$ decreases almost linearly when V_{DS} increases, while the value of $C_{GS,ext}$ is almost constant. This can be explained by viewing $C_{GS,ext}$ and $C_{GD,ext}$ as two single EDL capacitors, the capacitance of which has a linear dependency on the applied voltage, i.e. V_{GS} and V_{DS}, respectively. Similarly, based on the linear algebraic formula, their values can be expressed as below:

$$C_{GS,ext} = c_{GS,ext0} + c_{GS,ext1} \cdot V_{GS}, \tag{3.20}$$

$$\begin{aligned} C_{GD,ext} &= c_{GD,ext0} + c_{GD,ext1} \cdot V_{GD} \\ &= c_{GD,ext0} + c_{GD,ext1} \cdot (V_{GS} - V_{DS}). \end{aligned} \tag{3.21}$$

By using the extracted $c_{GS,ext0} = 0.22$ nF, $c_{GS,ext1} = 0.048$ nF V^{-1}, $c_{GD,ext0} = 0.20$ nF and $c_{GD,ext1} = 0.035$ nF V^{-1}, a good fitting has been achieved as shown in Fig. 3.12(b). Notably, coefficients in Eq. 3.20 and 3.21 are close to the half of the corresponding values in Eq. 3.19. This indicates that the overlap capacitance scales with the area of the overlap region.

Although the proposed approach can lead to an asymmetric device behavior, no convergence problem has been encountered so far. Conclusively, the proposed model offers a good approximation to the measurement data of extrinsic overlap capacitance.

3.4.3. Intrinsic capacitance

Here, the capacitance of normal EGT devices is characterized and modelled, including both intrinsic and extrinsic effects.

Fig. 3.13(a) shows the measurement results of the gate capacitance C_{GG} as a function of gate voltage V_{GG}. When a sub-threshold gate voltage is applied, the channel is in the OFF-state, and no EDL capacitance is formed at the interface between the electrolyte and semiconductor. Therefore, merely extrinsic overlap capacitance is characterized, which shows a linear dependency on the gate voltage as shown in the characteristics of de-embedding devices. When V_{GG} exceeds the onset-voltage around 0.15 V, a strong increase in the capacitance is observed, which is followed by a higher plateau. This is due to the increase of the intrinsic gate capacitance $C_{GG,int}$ that is associated with the charge accumulation in the channel in the ON state.

The development of $C_{GG,int}$ can be explained by a two-component model, as illustrated by 3.14. One is the EDL capacitance C_{EDL}, which can be viewed as a constant value that depends on the shape, size and chemical structure of ions in the electrolyte [70, 89]. In the semiconductor, another

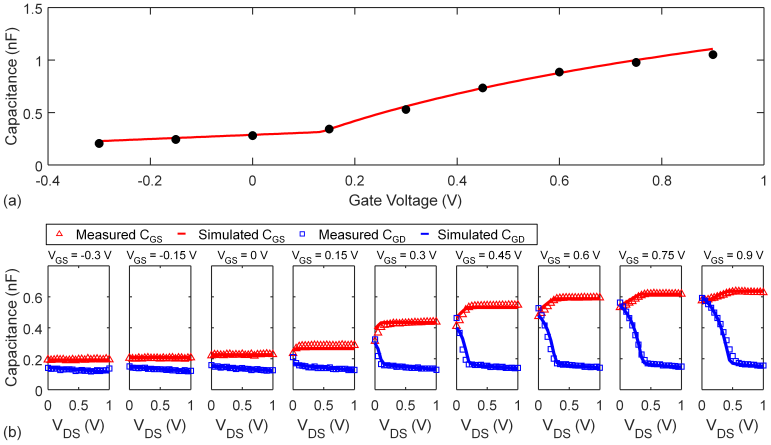

Figure 3.13.: Terminal capacitance of EGT with channel length $L = 60\,\mu m$ and $W = 100\,\mu m$ is characterized, including both intrinsic and extrinsic effects. (a) Measured and modelled gate terminal capacitance C_{GG} as a function of V_{GG}. (b) Measured and modelled drain and source terminal capacitance, C_{GD} and C_{GS}, as a function of V_{DS} at various V_{GS}. Reprint with permission from [87] ©2019 IEEE.

space-charge capacitance C_{SC} exists. Its value strongly depends on the applied voltage [64]. Consequently, the overall gate capacitance can be expressed by:

$$C_{GG} = \begin{array}{l} C_{GG,ext} + C_{GG,int} \\ C_{GG,ext} + \frac{C_{EDL} \cdot C_{SC}}{C_{EDL} + C_{SC}} \end{array} \tag{3.22}$$

Empirically, C_{SC} can be described as a capacitance with a linear dependency on V_{GG}, once V_{GG} exceeds the on-set voltage V_{ON}, i.e.:

$$C_{SC} = \begin{cases} 0 & V_{GG} < V_{on} \\ c_{sc}(V_{GG} - V_{on}) & V_{GG} \geq V_{on} \end{cases} \tag{3.23}$$

It is necessary to point out that the linear dependency of C_{SC} described here deviates from the exponential behavior predicted by Mott-Schottky analysis that is often applied for electrolyte-semiconductor interfaces.

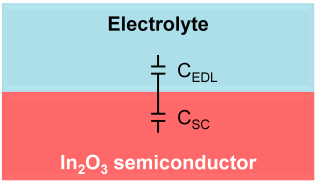

Figure 3.14.: Two-component-model to explain the intrinsic gate capacitance.

This deviation can be attributed to the potential-dependent charging of surface states [64]. As shown by Fig. 3.13(a), a satisfactory agreement between the measured and modelled data can be achieved using the voltage-dependency coefficient $c_{SC} = 3.0\ \mathrm{nF\,V^{-1}}$, on-set voltage $V_{on} = 0.118\ \mathrm{V}$, and EDL capacitance $C_{EDL} = 3.2\ \mathrm{nF}$.

Subsequently, the lumped terminal capacitance including C_{GS} and C_{GD} is characterized and modelled using the corresponding measurement setup as described in Fig. 3.11(b).

Experimental results are presented in Fig. 3.13(b), where C_{GS} and C_{GD} are measured with increasing V_{DS} and constant V_{GS} in each subplot, while V_{GS} increases between subplots in a step-wise manner from $-0.3\ \mathrm{V}$ to $-0.9\ \mathrm{V}$. In subplots when $V_{GS} < V_{th}$ (V_{GS} from $-0.3\ \mathrm{V}$ to $0\ \mathrm{V}$), since the channel is still in depletion mode, only extrinsic parasitic capacitance has been measured. Once V_{GS} exceeds the V_{th} (V_{GS} from $0.15\ \mathrm{V}$ to $0.9\ \mathrm{V}$), intrinsic capacitance from the channel can be measured. At $V_{DS} = 0\ \mathrm{V}$, the charge distribution along the channel can be assumed to be uniform. Therefore, $C_{GG,int}$ is equally shared by the intrinsic terminal capacitance $C_{GS,int}$ and $C_{GD,int}$. As V_{DS} further increases, the channel part at the drain side is again depleted while more charges accumulate at the source side. The resulting non-uniform distribution leads to an increase in the measured value of $C_{GS,int}$ and a decrease in $C_{GD,int}$. Finally, $C_{GD,int}$ becomes almost zero and $C_{GS,int}$ reaches the maximum. Similar behavior of the charge partitioning has been frequently observed in various kinds of dielectric-gated transistors [84, 90]. There, the Meyer-capacitance model has been widely accepted.

Although this model fails to obey the charge conservation [91, 80, 27], it has a simple mathematical expression and is SPICE-compatible, usually resulting in acceptable errors in circuit simulations [82].

Through the examination of experimental results in this work, it is found that the factor of partitioning deviates from 2/3 as described by the conventional Meyer model. The reason is the overall voltage-dependency of EDL capacitance. Therefore, the classical Meyer model is extended by introducing the voltage-dependent $C_{GG,int}$ and fitting parameter K_S and K_D:

$$C_{GS,int} = \frac{2}{3} C_{GG,int} K_S \left[1 - \left(\frac{V_{GTe} - V_{DSe}}{2V_{GTe} - V_{DSe}} \right)^2 \right] \tag{3.24}$$

$$C_{GD,int} = \frac{2}{3} C_{GG,int} K_D \left[1 - \left(\frac{V_{GTe}}{2V_{GTe} - V_{DSe}} \right)^2 \right] \tag{3.25}$$

Especially, the fitting parameter K_S has been described as a function of V_{GS} using the second-order linear algebraic formula:

$$K_S = q_0 + q_1 V_{GS} + q_2 V_{GS}^2, \tag{3.26}$$

where $q_0 = 2$, $q_1 = 2.5$ and $q_2 = -1.79$ are extracted from the measurement. Also, $K_D = 0.92$ is used. The effective over-drive voltage V_{GTe} and effective gate drain-source voltage V_{DSe} are expressed as:

$$V_{GTe} = \frac{1}{2} \left[V_{DS} + V_{GT} - \sqrt{V_\delta + (V_{DS} - V_{GT})^2} \right], \tag{3.27}$$

$$V_{DSe} = \delta V_{DS}, \tag{3.28}$$

which provide the smooth transition to the saturation region. Here, $V_{GT} = V_{GS} - V_{th}$ is the gate over-drive voltage, and V_δ and δ are constant parameters determining the transition width and shape.

The total terminal capacitance, namely C_{GS} and C_{GD}, is then sum of their extrinsic and intrinsic components. For the EGT device characterized here, the corresponding extrinsic parameters are extracted in Tab. 3.3.

Table 3.3.: Extrinsic parameters in capacitance model

Parameter	Value
$c_{GG,ext0}$	0.28 nF
$c_{GG,ext1}$	0.15 nF V^{-1}
$c_{GS,ext0}$	0.23 nF
$c_{GS,ext1}$	0.08 nF V^{-1}
$c_{GD,ext0}$	0.16 nF
$c_{GD,ext1}$	0.04 nF V^{-1}

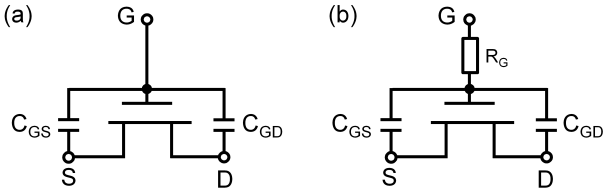

Figure 3.15.: Illustration of the quasi-static (a) and nonquasi-static capacitance model. Reprint with permission from [87] ©2019 IEEE.

Finally, using the proposed models, a satisfactory agreement has been achieved between the measurement and modeling results as shown in Fig. 3.13(b).

3.4.4. Nonquasi-static effect

Until now, a quasi-static (QS) capacitance model for EGTs has been developed by considering the capacitance-voltage characteristics of lumped terminal capacitors, namely C_{GS} and C_{GD}. In the schematic level, the QS capacitance model can be illustrated in Fig. 3.15(a). Here, the charging of gate capacitance and the transition of the channel state are assumed as instantaneous processes. However, as revealed before [71], at least two

resistor components co-exist on the charging path at the gate terminal of the EGT. One is the electrolyte bulk resistance, which originates from the ionic mobility of the electrolyte. Another one is the resistance due to the finite conductivity of the top-gate material PEDOT:PSS. Due to their existence, the channel transition in EGTs fails to respond immediately to the application of the gate voltage. Consequently, the switching speed is limited.

To reflect the charging process and simulate the behavior of circuits correctly, the nonquasi-static (NQS) is required for EGTs, where an additional resistor, namely the effective gate resistor R_G, is inserted on the gate path. Fig. 3.15(b) illustrates the schematic of the NQS capacitance model. R_G includes both the contributions from top-gate resistance and electrolyte bulk resistance. As has been investigated previously [71], their values can be determined using the parameter extraction based on the equivalent circuit model.

3.5. Conclusion

In this chapter, the characterization and modeling of capacitance in EGTs have been extensively studied. Voltage-dependent impedance spectroscopy has been performed, and the frequency response of the gate capacitance is analyzed using the equivalent circuit method. With the help of de-embedding test structures, extrinsic parasitic capacitance has also been carefully treated. The extracted physical parameters in the equivalent circuit reveal important information to explain the dynamic performance of EGTs. Furthermore, the simulation results shed light on the possibility to optimize the device operating frequency. Consequently, a Meyer-like compact model has been proposed to accurately describe the capacitance-voltage characteristics of the lumped terminal capacitance. This has laid a sound foundation to enable accurate transient and AC circuit simulations, which will be elaborated in detail in the following chapter.

4. Noise in EGTs

4.1. Background

As briefly introduced in Chapter 2.2.3, noise is important for electronic devices. On one hand, it is an asset, serving as a useful tool to study surface properties. On the other hand, it is a hindrance, particularly degrading the signal quality of analog and RF circuits. There have been interesting results regarding the study of the noise properties for silicon-based MOSFETs, which provides tools for the circuit simulation [92, 93, 94].

Recently, metal oxide semiconductors have become popular in the fabrication of printed electronic devices, which feature many attractive properties such as high intrinsic charge carrier mobility, optical transparency and non-toxicity [95]. There have been many reports on the noise properties of such devices, especially in the low-frequency region which is rich in flicker noise. In [96, 97], low-frequency noise of amorphous IGZO TFTs has been studied and the origin of the flicker noise has been discussed. The noise behavior of IZO TFTs has been modelled based on industry-standard BSIM model [98]. However, little is known about the noise characteristics of indium-oxide TFTs, especially the ones fabricated using solution-processable materials via printing technologies. Also, the electrolyte-gating approach provides the possibility to fabricate transistors with low-voltage operation. Its influence on the noise properties needs to be studied.

In this context, this chapter focuses on the characterization of the low-frequency noise characteristics of ink-jet printed EGTs incorporating indium-oxide semiconductors. Firstly, well-established theories on noise

are introduced. Then, the characterization method for the low-frequency noise is presented. Next, the noise measurement of EGTs based on the dedicated test structures is conducted. This chapter aims to determine the origin of the flicker noise in EGTs and quantify the noise level to provide a fair comparison with other printing technologies.

4.2. Flicker noise theory

As briefly introduced in section 2.2.3, in field-effect transistors, the flicker noise dominates the noise spectrum in the low-frequency range, the power spectral density of which is almost proportional to $1/f$. The major theories in the modeling of flicker noise in MOSFETs can be categorized into two groups. The One is the carrier number fluctuation introduced by McWhorter [29], which claims that the flicker noise is fundamentally a surface effect. The other theory is the carrier number fluctuation theory developed by Hooge [99]. It considers the flicker noise as a bulk effect based on the observations that the normalized noise is inversely proportional to the total number of charge carriers in the bulk. Usually, it is challenging to predict, which theory can be applied to a certain type of technology. Therefore, experimental works need are necessary, based on which the conclusion can be drawn by examining the important figure of merits.

4.2.1. Carrier number fluctuation

In the scheme of carrier number fluctuation, it is proposed that the $1/f$ spectrum can be treated as the superposition of relaxation processes with a wide spread of time constant. This is originated from dynamic trapping/detrapping events of charge carriers due to traps allocated at the channel-insulator interface. This leads to the fluctuation in the chan-

nel/insulator interface charge Q_{IT}, which can be represented by the fluctuation in the flat-band voltage:

$$\delta V_{FB} = -\frac{\delta Q_{IT}}{WLC_i}, \tag{4.1}$$

where C_i is the gate capacitance per unit area, and the W and L are the channel width and length. Therefore, assuming that the effective charge carrier mobility μ_{eff} is independent on the insulator charge δQ_i, the drain current fluctuation δI_D can be directly expressed by the flat-band voltage fluctuation:

$$\delta I_D = \delta V_{FB} \frac{\partial I_D}{\partial V_{FB}}. \tag{4.2}$$

Considering that the fluctuation in flat-band voltage is equivalent to the gate voltage fluctuation, $\delta V_{FB} = \delta V_G$,the fluctuation in the drain current can be further converted to:

$$\delta I_D = \delta V_{FB} g_m, \tag{4.3}$$

where $g_m = \partial I_D / \partial V_G$ is the transconductance. Therefore, the power density of the drain current S_{I_D} normalized by the drain current I_D has the following expression:

$$\frac{S_{I_D}}{I_D^2} = \frac{g_m^2}{I_D^2} S_{V_{FB}}, \tag{4.4}$$

which is called the carrier number fluctuation without correlated mobility fluctuation (ΔN) [92]. Based on this concept, it can be observed that the normalized S_{I_D} is directly proportional to the squared transconductance to drain current ratio g_m^2/I_D^2 with a factor of flat-band voltage noise $S_{V_{FB}}$. Following [94, 100, 101], $S_{V_{FB}}$ can be either expressed by:

$$S_{V_{FB}} = \frac{q^2 k_B T N_T}{WLC_i^2 a_t f}, \tag{4.5}$$

where N_T is the trap density per volume in the semiconductor material and a_t is the tunnel attenuation distance, or

$$S_{V_{FB}} = \frac{q^2 k_B T N_{IT}}{WLC_i^2 f}, \tag{4.6}$$

where N_{IT} is the trap density per area at the channel-insulator interface.

In a more detailed approach, it needs to be considered that the effective charge carrier mobility μ_{eff} exhibits the dependency on the insulator/channel interface charge Q_{IT}. As a consequence, δQ_{IT} induces additional fluctuation in drain current. Thus, Eq. 4.2 needs to be rewritten:

$$\delta I_D = \delta V_{FB} \frac{\partial I_D}{\partial V_{FB}}\bigg|_{\mu_{eff}=const.} + \delta\mu_{eff} \frac{\partial I_D}{\partial \mu_{eff}}\bigg|_{V_{FB}=const.}. \tag{4.7}$$

Considering the general form of the effective mobility correlated with the insulator charge:

$$\frac{1}{\mu_{eff}} = \alpha_{SC} Q_{IT} + \frac{1}{\mu_{eff0}}, \tag{4.8}$$

where α_{SC} is the scattering coefficient and μ_{eff0} is a constant value, the fluctuation in the drain current in the linear region can be evaluated:

$$\delta I_D = -g_m \delta V_{FB} \mp \alpha I_D \mu_{eff} \delta Q_{IT}. \tag{4.9}$$

Also, the normalized power density of S_{I_D} can be expressed by:

$$\frac{S_{I_D}}{I_D^2} = (1 \pm \alpha_{SC}\mu_{eff} C_i \frac{I_D}{g_m})^2 \frac{g_m^2}{I_D^2} S_{V_{FB}}, \tag{4.10}$$

which is called the carrier number fluctuation with correlated mobility fluctuation ($\Delta N - \Delta\mu$). As can been seen from Eq. 4.10, excessive noise arises from the correlated mobility fluctuation. Consequently, the correlation between the normalized S_{I_D} and squared transconductance to drain current ratio becomes less as compared to the classical carrier number fluctuation model in Eq. 4.4.

Furthermore, in the $\Delta N - \Delta\mu$ model, the gate voltage noise spectral density S_{V_G} is expressed by:

$$S_{V_G} = (1 \pm \alpha_{SC}\mu_{eff} C_i \frac{I_D}{g_m})^2 S_{V_{FB}}. \tag{4.11}$$

In the above-threshold region, I_D/g_m is replaced by the gate over-drive voltage, resulting in

$$S_{V_G} = (1 \pm \alpha_{SC}\mu_{eff}C_i(V_{GS} - V_{th}))^2 S_{V_{FB}}, \tag{4.12}$$

Therefore, in the model of $\Delta N - \Delta\mu$, S_{V_G} exhibits a parabolic dependency on the gate over-drive voltage.

4.2.2. Carrier mobility fluctuation

Contrary to the surface effect claimed by the carrier number fluctuation theory, there have been reports showing that the intensity of flicker noise is inversely proportional to the total number of charge carriers in the bulk of homogeneous samples [99]. To explain these observations, the carrier mobility fluctuation ($\Delta\mu$) is developed. It considers that the fluctuation of the carrier mobility is the primary cause of the drain current fluctuation. Consequently, S_{I_D}/I_D^2 is described as:

$$\frac{S_{I_D}}{I_D^2} = \frac{\alpha_H}{fN_{tot}} = \frac{q\alpha_H}{fWLQ_i} = \frac{q\alpha_H}{fWLC_i(V_{GS} - V_{th})}, \tag{4.13}$$

where N_{tot} is the total number of charge carrier, q is the elementary charge, α_H is the Hooges parameter which is related to the process, and Q_i is the charge carrier per unit area in the bulk channel. Therefore, the gate voltage noise PSD S_{V_G} is given by:

$$S_{V_G} = \frac{S_{I_D}}{I_D^2}\frac{I_D^2}{g_m^2} = \frac{q\alpha_H}{fWLQ_i}\frac{I_D^2}{g_m^2}. \tag{4.14}$$

In the above-threshold region, the drain current to transconductance ratio is expressed by [102]:

$$\frac{I_D}{g_m} = (V_{GS} - V_{th})(1 + \theta(V_{GS} - V_{th})), \tag{4.15}$$

where θ is the mobility attenuation factor. Thus, by considering $Q_i = C_i(V_{GS} - V_{th})$, Eq. 4.14 is further reduced to:

$$S_{V_G} = \frac{q\alpha_H}{fWLC_i}(V_{GS} - V_{th})(1 + \theta(V_{GS} - V_{th}))^2. \tag{4.16}$$

As a consequence, in carrier mobility fluctuation theory, the gate voltage noise S_{V_G} has either a linear ($\theta \approx 0$) or super-linear (θ is sufficiently large) dependency on the gate over-drive voltage in the linear operation region, which is often considered as an important evidence for the diagnosis of noise origin.

4.3. Characterization method

To meaningfully interpret noise data, accurate and robust experimental setup for the measurement of the low-frequency noise spectrum is critical. Due to the complex nature of the noise measurement system, all possible parasitic and environmental effects need to be carefully considered. In this section, the characterization method dedicated to reliable low-frequency noise measurement is introduced. The measurement setup and principles are elaborated, which is verified by thermal noise measurement in resistors. Also, the test structure used in the noise measurement of EGTs is introduced.

4.3.1. Measurement setup

The measurement setup for the characterization of low-frequency noise in the device under test (DUT) is illustrated in Fig. 4.1. The measurement principle can be generally applied to DUTs such as transistors. Here, the key instrument is the battery-powered Standford Research SR570 low noise current amplifier. It amplifies the drain current signal of the transistor through the feedback resistance R_f and operational amplifier and converts it to the voltage output signal. To avoid the saturation of

the output, the DC component of the input current signal needs to be cancelled out by the built-in offset current source I_{offset}. Also, the current amplifier provides a programmable drain bias upon the application of V_{DS} to the non-inverting input terminal of the operational amplifier. The same potential appears at the inverting input terminal and is then applied to the drain terminal of the transistor. To properly bias the gate terminal of the DUT, the Keithley 2602 SMU is utilized. A low-pass RC filter is inserted here to filter out the noise from the gate supply, which possesses the cut-off frequency of only 0.01 Hz, lower than the frequency range of interest.

The output of the current amplifier is further connected to the spectrum analyzer SR770, which performs the FFT to convert the time domain signal waveform to the power spectral density (PSD). All instruments are automated by a Python-based program, which connects to the SMU and spectrum analyzer through GPIB and to the current amplifier via series port RS232. It is important to point out that the power of instruments needs to be connected in the star topology to avoid possible ground loop, which gives rise to the noise level. Also, the power measurement setup is isolated using an isolation transformer to avoid interference from the power grid. Last but not the least, it is necessary to place the DUT in Faraday cage, which shares the ground of other measurement instruments, and all signals are transferred between instrument through coaxial cables. In this way, the coupling noise from external sources can be largely eliminated.

Similar to the measurement setup designed for transistors as DUTs, the measurement principle for resistors are also introduced in Fig. 4.1. This measurement setup is mainly prepared for verification purpose as will be discussed in the next section. Since resistors are two-terminal devices, the additional gate biasing is not required.

Fig. 4.3 shows the photo of the experimental setup designed for the reliable noise measurement, where DUTs are placed in a Faraday cage to assure the good shielding from the background noise.

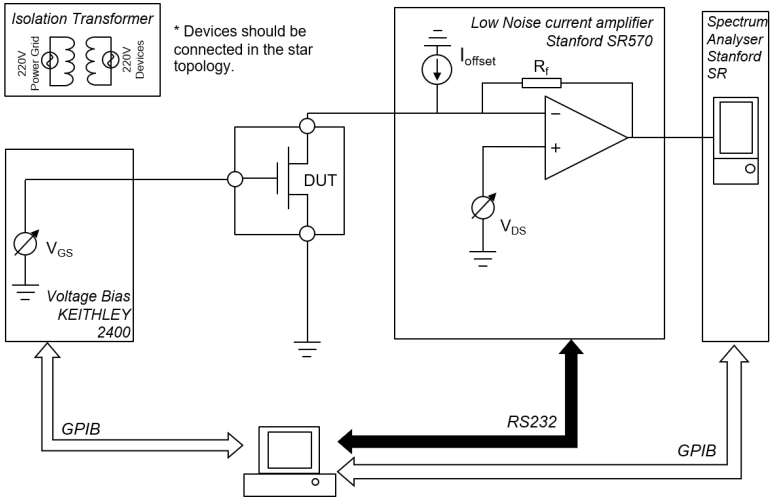

Figure 4.1.: Measurement setup for the characterization of low-frequency noise in EGTs.

4.3.2. System validation

The aforementioned measurement setup is verified by measuring the thermal noise of resistors. Here, thin-film resistors are chosen, which are typically free from flicker noise due to their homogeneous structures. Therefore, pure thermal noise can be observed from this type of resistor. According to Johnson–Nyquist equation described in section 2.2.3, the current thermal noise PSD of resistors, or S_{I_R}, can be calculated using their resistance values. Using the measurement setup in Fig. 4.2, resistors ranging from 5 kΩ to 100 kΩ are tested.

Fig. 4.4 shows the measured values (dots) of the current PSD using various resistors. Also, the calculations (lines) based on Johnson–Nyquist equation are plotted, which are reasonably close to the experimental data. This indicates that the present measurement setup is suitable for the reliable and accurate measurement of the low-frequency noise.

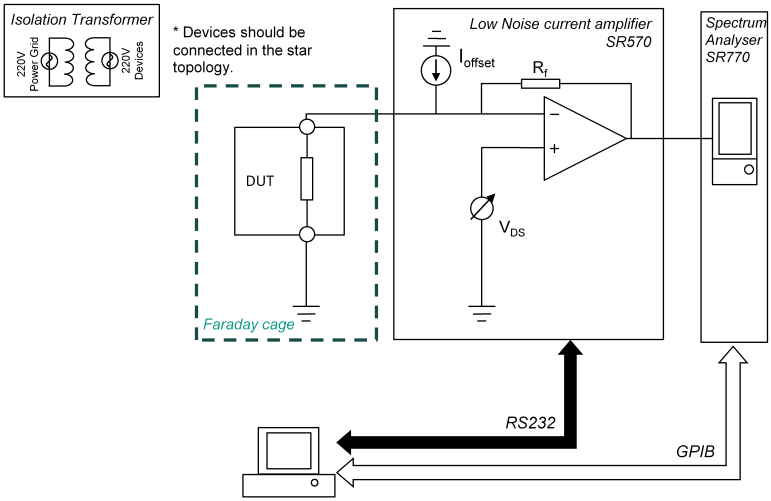

Figure 4.2.: Measurement setup for the characterization of thermal noise in thin-film resistors.

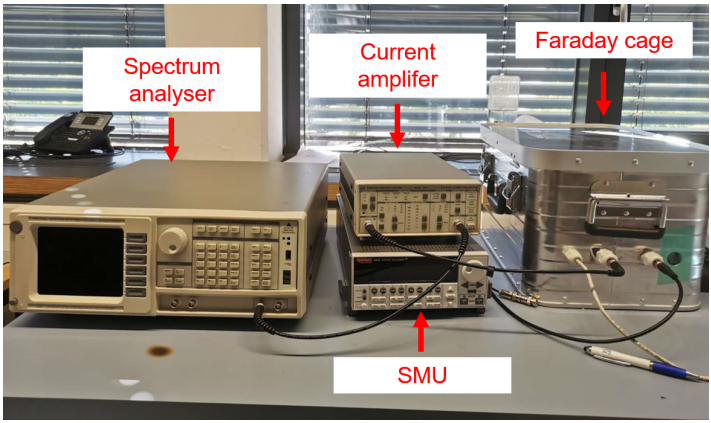

Figure 4.3.: Photo of the experimental setup designed for the reliable noise measurement. DUTs are placed in the Faraday to assure a good measurement quality.

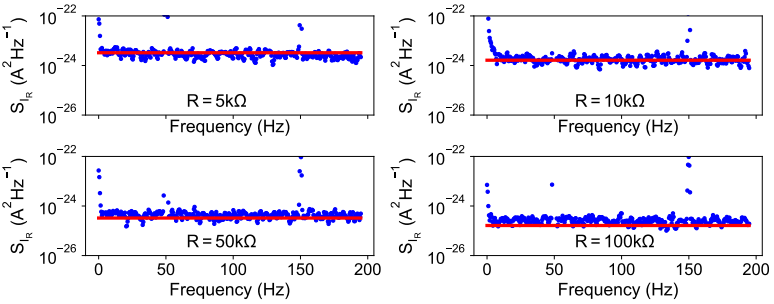

Figure 4.4.: Measured current power spectral density of thermal noise in thin-film resistors (dots), and calculated values using Johnson–Nyquist equation (lines). The measured values are close to the calculation.

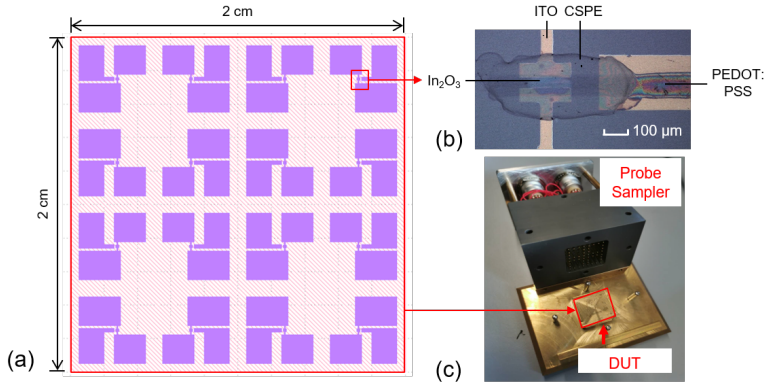

Figure 4.5.: (a) Layout of the test structure used for the low-frequency noise characterization. (b) Microscopic photo of the EGT embedded on the test structure, which has the channel length $L = 40\,\mu m$ and width $W = 200\,\mu m$. (c) Test structure seamlessly integrated in the probe sampler.

4.3.3. Experiment configuration

In this section, EGTs used for the characterization of their low-frequency noise has a channel geometry of $W = 200\,\mu m$ and $L = 40\,\mu m$. The test structure dedicated for the noise measurement is shown in Fig. 4.5(a), where 16 devices are fabricated. The microscopic photo of a single EGT is shown in Fig. 4.5(b). To measure the signal, a probe sampler as shown in Fig. 4.5(c) is used instead of the probe station to automate the measurement procedure, and experiments can be conducted in a Faraday cage to assure the reliable noise measurement. Therefore, large contacts as source, drain and gate terminals are designed for the needle contact in the sampler. The layout of the test structure is fabricated on the $2\,cm \times 2\,cm$ glass substrate, which can be seamlessly integrated into the probe sampler to conduct the noise measurement.

4.4. Results and discussions

4.4.1. Low-frequency noise characteristics

The low-frequency noise is characterized using the measurement setup based on the dedicated test structure as described before. To perform the necessary analysis, the I-V characteristics of EGTs with the channel geometry of $W = 200\,\mu m$ and $L = 40\,\mu m$ are firstly measured using Kiethley 2602B SMU. In Fig. 4.6(a), the transfer curve in the linear region is plotted with $V_{DS} = 0.1\,V$ and V_{GS} ranging from $-0.5\,V$ to $1\,V$ on the linear scale. To properly extract the threshold voltage V_{th}, the linear extrapolation technique is utilized [103]. The auxiliary line is extrapolated around the V_{GS} point at maximum transconductance g_m in the transfer curve. Its intersection point with the V_{GS} axis determines the V_{th}. Also, in the logarithmic plot in Fig. 4.6(b), the ON/OFF ratio of $\sim 10^6$ can be observed.

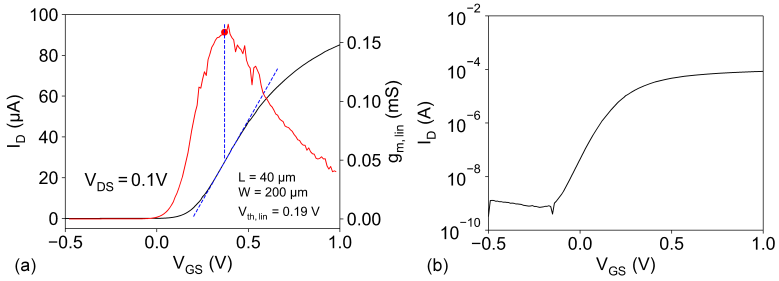

Figure 4.6.: I-V characteristics of the EGT with the channel geometry of $W = 200\,\mu m$ and $L = 40\,\mu m$. (a) Drain-source current (I_D) and linear transconductance $g_{m,lin}$ against gate-source voltage (V_{GS}) on the linear scale. The extracted value of threshold voltage $V_{th} = 0.19\,V$ using the linear extrapolation technique. (b) I_D - V_{GS} on the logarithmic scale.

Next, the drain current noise PSD is measured. The noise measurement is also performed in the linear region with $V_{DS} = 0.1\,V$, while V_{GS} is swept step-wise from 0.2 V to 1 V. The frequency of each spectrum ranges from 0.3 Hz to 10 kHz. Measured noise spectra are presented in Fig. 4.7(a). Additionally, the background noise floor generated by instruments is characterized, which is measured without the connection to DUTs under the open-circuit condition.

As one can see, the noise floor is orders of magnitude lower than the measured S_{I_D}, indicating a reliable characterization. Furthermore, the flicker noise dominates all the measured S_{I_D} in the low frequency range, which also shows dependence on the gate bias V_{GS}. The extracted exponent parameter γ according to $S_{I_D} \propto 1/f^{\gamma}$ is plotted in Fig. 4.7(b) as a function of V_{GS}. Except for the first point of $V_{GS} = 0.2\,V$, where the EGT is in the weak above-threshold state, the extracted γ has values between 1 and 1.25, which is the typical reasonable range for the flicker noise in field-effect transistors [104].

For S_{I_D} measured at high $V_{GS} > 0.8\,V$, the thermal noise component starts to dominate at high frequency. The increased thermal is considered to be related to the increase in channel conductance at high gate voltage, as

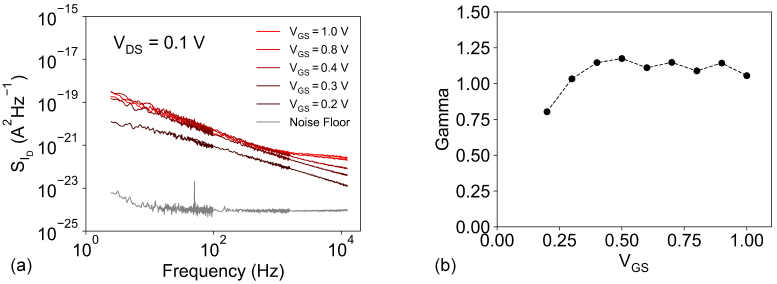

Figure 4.7.: (a) low-frequency noise characteristics of the EGT measured in the linear region. $V_{DS} = 0.1\,\mathrm{V}$, and various V_{GS} from 0.2 V to 1 V is applied. Also, the noise floor measured at the open circuit is plotted. (b) The extracted the exponent of the flicker noise plotted as a function of V_{GS}.

predicted by the Johnson–Nyquist equation. Additionally, the gate leakage current through the electrolyte insulator might have a contribution, which also increases at high V_{GS} and is often considerably high in electrolyte-gated transistors.

4.4.2. Noise generation mechanism

To investigate the noise generation mechanism in EGTs, one widely used technique is to plot the measured normalized drain current noise S_{I_D}/I_D^2 against the gate-overdrive voltage $V_{GS} - V_{th}$ [105, 98, 106]. Often, several frequency points are chosen. Then, the slop in the S_{I_D}/I_D^2 (log.) and $V_{GS} - V_{th}$ (log.) plot serves as an indicator of the applicable noise model:

- In the ΔN model, one can rewrite Eq. 4.4 using the substitution $I_D/g_m = V_{GS} - V_{th}$, resulting in the following form:

$$\frac{S_{I_D}}{I_D^2} = \frac{1}{(V_{GS} - V_{th})^2} S_{V_{FB}}. \tag{4.17}$$

  Consequently, the slop in the S_{I_D}/I_D^2 (log.) and $V_{GS} - V_{th}$ (log.) plot shows the value of -2.

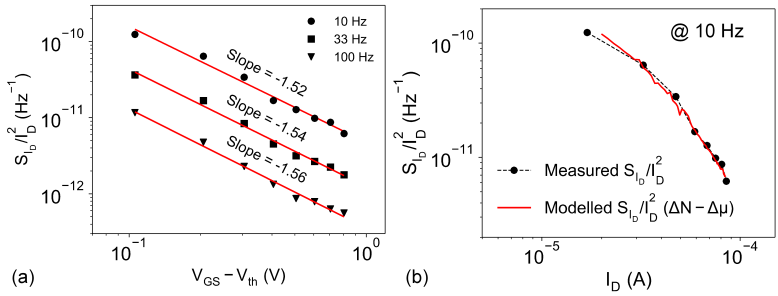

Figure 4.8.: (a) Measured normalized drain current noise S_{I_D}/I_D^2 as a function of gate over-drive voltage $V_{GS} - V_{th}$ at the frequency of 10 Hz, 33 Hz and 100 Hz, where slopes of ~ -1.5 can be extracted. (b) Measured normalized drain current noise S_{I_D}/I_D^2 as a function of gate over-drive voltage $V_{GS} - V_{th}$ (dots), which can be accurately modelled by the $\Delta N - \Delta\mu$ theory (line).

- Similarly, in the $\Delta N - \Delta\mu$ model, the drain current noise equation in Eq. 4.10 can be rewritten to:

$$\frac{S_{I_D}}{I_D^2} = (1 \pm \alpha_{SC}\mu_{eff}C_i(V_{GS} - V_{th}))^2 \frac{1}{(V_{GS} - V_{th})^2} S_{V_{FB}}. \qquad (4.18)$$

  Depending on the value of α_{SC}, the slop in the S_{I_D}/I_D^2 (log.) and $V_{GS} - V_{th}$ (log.) plot can exhibit values ranging between -1 and -2.

- In the $\Delta\mu$ model, the slope is approximately -1 as can be directly deduced from Eq. 4.13.

In Fig. 4.8(a), the noise measurement data of EGTs at the frequency of 10 Hz, 33 Hz and 100 Hz are shown. Notably, the extracted slops have the consistent values of ~ -1.5. Using the aforementioned criteria, the number fluctuation model with correlated mobility fluctuation ($\Delta N - \Delta\mu$) can be suggested as the primary noise generation mechanism in EGT technology.

Furthermore, the noise equation of ($\Delta N - \Delta\mu$) model in Eq. 4.10 is verified by modelling the measurement data of S_{I_D}/I_D^2, where $C_i = 4\,\mu\text{F}\,\text{cm}^{-2}$

and $\mu_{eff} = 5\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ as reported in earlier works [61]. Using $\alpha_{SC} = 7.9 \times 10^4\,\mathrm{V\,s\,C^{-1}}$ and flat-band voltage noise $S_{V_{FB}} = 1.28 \times 10^{-12}\,\mathrm{V^2\,Hz^{-1}}$, measured S_{I_D}/I_D^2 can be accurately modelled in Fig. 4.8(a). This further proves the validation of the $\Delta N - \Delta\mu$ model.

4.4.3. Benchmark of noise level

Finally, benchmarking of the noise performance between the presented work and reported thin-film technology is of high interest.

Generally, both α_{SC} and $S_{V_{FB}}$ are important parameters that determine the noise level in the $\Delta N - \Delta\mu$ model. Additionally, as can be seen from Eq. 4.6, $S_{V_{FB}}$ can be normalized by the areal gate capacitance C_i to obtain N_{IT}, which represents the quality of the semiconductor thin-film and insulator-semiconductor interface. Therefore, it is reasonable to include N_{IT} in the benchmark. However, to present a fair and comprehensive comparison between substantially different technologies, it is necessary to consider α_{SC}, $S_{V_{FB}}$ and N_{IT} simultaneously. Therefore, S_{I_D}/I_D^2 is the appropriate parameter for the comparison, since it contains both α_{SC} and $S_{V_{FB}}$ according to Eq. 4.10, while N_{IT} is contained in $S_{V_{FB}}$ regarding Eq. 4.6. As suggested by [107], S_{I_D}/I_D^2 can be further normalized by $W \times L$ to allow the comparison between different channel geometries. Conclusively, WLS_{I_D}/I_D^2 is considered as the generalized figure of merit to represent the overall noise level.

In the following Tab. 4.1, the noise performance between this work and state-of-the-art thin-film technologies is compared, where the differences in the material stack and fabrication process are also presented.

Table 4.1.: Comparison of the noise level in various TFT technologies

Source	Fabrication	Semicon.	Insulator	α_{sc} ($V\,s\,C^{-1}$)	$WLfS_{vfb}$ ($V^2\,\mu m^2$)	N_{it} ($cm^{-2}\,eV^{-1}$)	WLS_{id}/I_D^2 ($\mu m^2\,Hz^{-1}$)
This work	Solution-based, inkjet printing	In_2O_3	$LiCLO_4$-based electrolyte	7.9×10^4	1.28×10^{-7}	3.1×10^{13}	$10^{-7} - 10^{-8}$ (@10 Hz)
[108]	Sputtering	ZnO	SiO_2	9.53×10^5	1.1×10^{-5}	8.8×10^{10}	$10^{-4} - 10^{-7}$ (@10 Hz)
[97]	Sputtering	a-IGZO	SiO_2	8.7×10^5	5.2×10^{-6}	1.88×10^{10}	$10^{-7} - 10^{-8}$ (@20 Hz)
[101, 106]	Sputtering	a-IGZO	SiO_2	0	8×10^{-6}	1×10^{11}	$10^{-7} - 10^{-8}$ (@10 Hz)
[109]	Sputtering	a-IGZO	SiO_2-based electrolyte	N/A	N/A	N/A	$10^{-4} - 10^{-6}$ (@10 Hz)
[107]	Solution-based	C_8–DNBDT-NW	SiO_2	N/A	N/A	3.49×10^{12}	$10^{-4} - 10^{-6}$ (@10 Hz)
	Solution-based	PBTTT-C_{14}	SiO_2	N/A	N/A	N/A	$10^{-3} - 10^{-5}$ (@10 Hz)
	Solution-based	IZO	SiO_2	N/A	N/A	N/A	$10^{-4} - 10^{-5}$ (@10 Hz)

Firstly, α_{sc} and $WLfS_{vfb}$ are compared. The reported value of α_{sc} in this work is much lower than in ZnO TFTs [108] and a-IGZO TFTs [97], but higher than $\alpha_{sc} = 0$ of a-IGZO TFTs in [101, 106], where correlated mobility fluctuation is not present. Furthermore, $WLfS_{vfb}$ of this work is significantly lower than reported values in [108, 97, 101, 106]. The large areal gate capacitance provided by electrolyte-gating helps to effectively reduce the S_{vfb}, which can be deduced from Eq. 4.6.

Secondly, N_{it} calculated from S_{vfb} is focused, where a large value in the order of $10^{13}\text{cm}^{-2}\,\text{eV}^{-1}$ is found. This is significantly higher than the data reported in non-printed TFTs in [108, 97, 101, 106, 107], indicating an inferior quality of the printed semiconductor and semiconductor-insulator interface in the presented work, caused by the necessary solution process and inkjet-printing in fabrication.

Finally, WLS_{id}/I_D^2 is compared in Tab. 4.1 that represents the generalized noise level. One can find the values in the presented work are comparable to TFTs with sputtered high-quality semiconductors in [108, 97, 101, 106]. Also, the noise in the presented work is lower than non-printed electrolyte-gated TFTs in [109], where there are essential differences in the fabrication method and noise mechanism. Notably, as compared to non-printed but solution-based TFTs gated by conventional dielectric materials in [107], the WLS_{id}/I_D^2 in the presented work is still superior.

As a conclusion, in this study, despite the fact that printed EGTs possess a high N_{it}, its negative effect on the noise is largely compensated by the large C_i provided by electrolyte-gating, where S_{vfb} is effectively reduced. Eventually, this leads to a low S_{id}/I_D^2. Thus, it is shown that the electrolyte-gating approach largely improves the noise performance for printed TFTs, which could originally suffer from low material qualities with high trap density at the channel interface.

4.5. Conclusion

In this section, the noise aspect of EGT technology is discussed with the focus on the flicker noise in low frequency.

Firstly, two major theories are introduced, namely the carrier number fluctuation without and with correlated mobility fluctuation (ΔN and $\Delta N - \Delta\mu$), and carrier mobility fluctuation ($\Delta\mu$). Noise equations are derived based on the study of the device physics.

In addition, the measurement setup is presented, which is dedicated for the accurate characterization of low-frequency noise. The noise of both transistor and resistor devices can be measured. Also, the presented setup is carefully validated by measuring the thermal noise from thin-film resistors. Experimental data are compared with the calculated based on Johnson–Nyquist equation.

Next, the noise of EGTs is characterized. The linear operation region of EGTs is focused on, which gives sufficient information about the noise origin and performance. From experimental data, the carrier number fluctuation with correlated mobility fluctuation is confirmed ($\Delta N - \Delta\mu$).

Finally, the comparison of noise level in various thin-film technologies based on measurement data is performed. It is found that despite the high interface trap density in printed EGTs, the noise performance is large improved by the high areal gate capacitance, comparable with sputtered high-quality TFTs and superior than solution-processed TFTs with conventional dielectric gating. This conclusion emphasizes the usefulness of electrolyte in improving the noise performance, especially of printed TFTs, making them favourable for low noise applications.

5. Circuits and applications

5.1. Background

In this chapter, various basic circuit designs based on the aformentioned printed EGT technology are proposed. Unlike in modern very large-scale integration (VLSI) technology, usually, merely mono-type transistors are available for most printed electronics technologies, primarily due to the mismatch between the electrical performance of n- and p-type transistors. For instance, for technologies based on metal oxide semiconductors, the n-type transistors are more dominating. Therefore, a lot of circuit designs in the field of printed electronics are based on resistor-transistor logic (RTL).

In this work, proposed circuit designs include digital and analog circuits such as inverters, ring oscillators [87] and full-wave rectifiers [110], which are systematically characterized regarding their output waveform, delay, operating frequency and power consumption/efficiency. Also, the NQS capacitance model presented before needs to be verified by comprehensively comparing the measurement and simulation results to perform the hardware-simulation correlation.

5.2. Printed inverter

The inverter is the most basic block for logic circuits. It converts the input signal from HIGH (LOW) to the output of LOW (HIGH). Depending on the availability of transistor types, three kinds of the inverter can

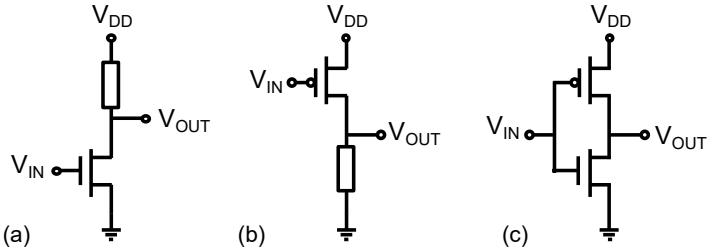

Figure 5.1.: Different kinds of inverter circuit: (a) NMOS inverter, (b) PMOS inverter and (c) CMOS inverter.

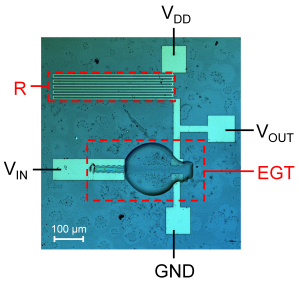

Figure 5.2.: Microscopic photo of the fabricated inverter based on the printed EGT with the channel geometry of $L = 60\,\mu m$ and $W = 100\,\mu m$. Reprint with permission from [87] ©2019 IEEE.

be designed, namely n-type metal-oxide-semiconductor (NMOS), p-type metal-oxide-semiconductor (PMOS)- and CMOS-inverter, which are illustrated in Fig.5.1. As discussed, for printed EGT technology, since only n-type transistors are available, the RTL logic in Fig.5.1(a) is chosen as the main subject of study in this work.

The RTL inverter is fabricated using the same process as of EGTs described previously, and the microscopic photo is presented in Fig. 5.2. Particularly, the EGT in the inverter has a channel geometry of $L = 60\,\mu m$ and $W = 100\,\mu m$. Also, the pull-up resistor R is realized by structuring meander ITO

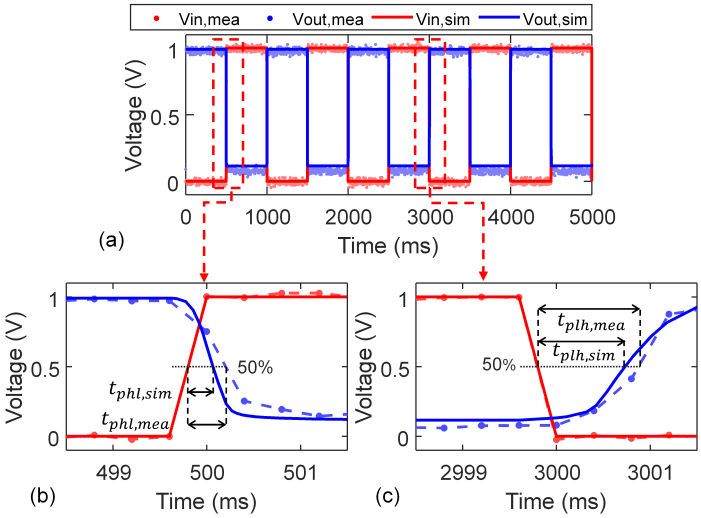

Figure 5.3.: (a) Measured and simulated waveform of the inverter input and output signal. (b) Falling edge of the output signal. (c) Rising edge of the output signal. Measured and simulated propagation delay HIGH-LOW/LOW-HIGH are termed as $t_{phl,mea}/t_{plh,mea}$ and $t_{phl,sim}/t_{plh,sim}$, respectively. Reprint with permission from [87] ©2019 IEEE.

patterns on the glass substrate using e-beam lithography. Here, the sheet resistance of sputtered ITO 670 Ω/□ has been considered. This results in the pull-up resistor $R = 50\,\text{k}\Omega$, which ensures a sufficient output signal swing between the HIHG and LOW.

The fabricated inverter is measured by applying a 1 Hz square wave at the input using Keithley 3390 function generator, while the output is connected to the Yokogawa DLM3022 oscilloscope. Therefore, the inverter output is loaded with instrument's internal resistance of 1 MΩ and capacitance of 20 pF. V_{DD}= 1 V is supplied by the Kiethley 2602B SMU. In Fig. 5.3(a), the input and output waveform are recorded. One can see that the printed inverter correctly toggles the input signal at the output, where the output high-level reaches almost 1 V and low-level is about 100 mV.

To realize the transient simulation in the environment of Cadence Virtuoso, the NQS capacitance model proposed in section 3.4 is implemented in Verilog-A code in combination with the EKV I-V model as described in section 2.4.2. Parameters required in the I-V model are extracted as V_{th} = 0.13 V, S = 16.45, γ = 1.57, f_1 = 7.6e-4 F V^{-1} s^{-1}, f_2 = 0.78, f_3 = 1.46 and f_4 = 0.02. Also, parameters in the capacitance model are adjusted according to the channel geometry used here.

The simulation results in the period of 5 s are presented in Fig. 5.3(a), where (b) and (c) show the falling and rising edge of the output signal in a smaller scale. One can observe that the simulation successfully captured the asymmetric behavior of the rising and falling edges due to the RTL logic. Also, the measured and simulated propagation delay of HIGH-LOW/LOW-HIGH, termed as $t_{phl,mea}/t_{plh,mea}$ and $t_{phl,sim}/t_{plh,sim}$, respectively. These parameters can determined by the delay time between the input and output at 50 % of the full swing. Tab. 5.1 lists the comparison between the measurement and simulation.

Table 5.1.: Evaluation of measured and simulated propagation delay

Delay	Measurement	Simulation
t_{phl}	0.272 ms	0.410 ms
t_{plh}	1.086 ms	0.943 ms

t_{phl}/t_{plh}:propagation delay from HIGH (LOW) to LOW (HIGH).
Reprint with permission from [87] ©2019 IEEE.

Conclusively, the proposed inverter design based on printed EGT works properly regarding its input and output relationship. Also, the presented nonquasi-static models provide a good empirical prediction of the inverter circuit in the time domain, whereas the accuracy can still be improved.

5.3. Printed ring oscillator

The ring oscillator circuit is considered as the key component for the technology characterization for microelectronic technologies. It comprises an odd number of inverter stages connected in a ring, with the output of the final stage fed to the input of the first stage. It serves as the prototype circuit to test a new semiconductor process, from which key technology parameters are revealed, such as delay (frequency) and power consumption.

The ring oscillator design presented here using printed EGTs is also based on resistor-transistor logic. Its schematic is presented in Fig.5.4. Three single-stage inverters are connected in the ring, while the first stage is implemented as a NAND gate so that the ring oscillator can be switched between quiescent and active mode via the enabling signal V_{ENABLE}. In this way, one can independently characterize the circuit in both active and quiescent modes. The output of the last inverter stage is also connected to an extra output inverter stage to improve the signal quality of the final output. Notably, the output stage is powered independently using the constant $V_{DDI} = 2\,\text{V}$. To measure the ring oscillator circuit, Agilent 4156C precision semiconductor parameter analyzer and Yokogawa DLM3022 oscilloscope are utilized. The comprehensive characterization results have been reported in the related work [83].

A variety of figure of merit represents the overall electrical characteristics and performance of the ring oscillator [111]. This includes the dependency of oscillation frequency on the supply voltage V_{DD}, which is obtained by applying Fast Fourier transformation (FFT) on the output waveform at various V_{DD}. Consequently, the propagation delay τ_p is determined as

$$\tau_p = \frac{1}{2(2\alpha + 1)f}, \tag{5.1}$$

where 2α+1 is the number of stages in the ring oscillator and f is oscillation frequency. Also, the quiescent and active current, namely I_{DDQ} and I_{DDA}, can be measured from the power supply. From them, the switching current

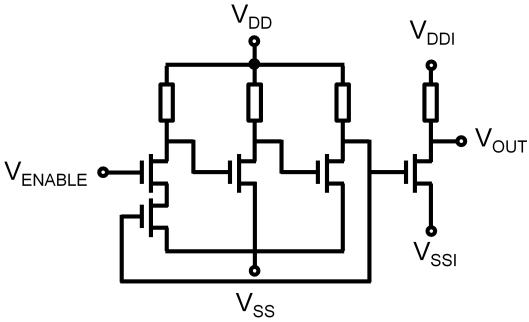

Figure 5.4.: Schematic of the printed 3-stage ring oscillator based on resistor-transistor logic.

I_{SW}, switching capacitance C_{SW} and switching resistance R_{SW} can be calculated as below:

$$I_{SW} = I_{DDA} - I_{DDQ}\frac{2\alpha}{2\alpha + 1} \tag{5.2}$$

$$C_{SW} = \frac{I_{SW}}{V_{DD}} 2\tau_p, \tag{5.3}$$

$$R_{SW} = \frac{V_{DD}}{2I_{SW}}, \tag{5.4}$$

Additionally, the quiescent power consumption P_Q and active power consumption P_A can be calculated as:

$$P_Q = I_{DDQ} V_{DD} \tag{5.5}$$

$$P_A = I_{SW} V_{DD} = C_{SW} V_{DD}^2 (2\alpha + 1) \tag{5.6}$$

Consequently, the total power P_{total} is calculated by:

$$P_{total} = P_Q + P_A. \tag{5.7}$$

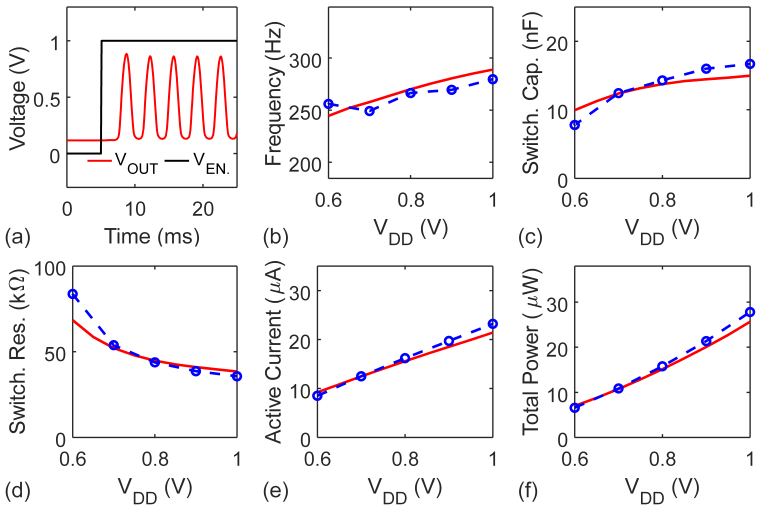

Figure 5.5.: (a) The simulated output waveform once V_{ENABLE} is set to high. (b)-(f) Comparison of measured (lines) and simulated (dots) figure of merit of the ring oscillator circuit including oscillation frequency, switching capacitance, switching resistance, active current and total power consumption on the supply voltage V_{DD}. Reprint with permission from [87] ©2019 IEEE.

In this work, the EGTs utilized in the ring oscillator design have a channel geometry of $W = 400\,\mu m$ and $L = 40\,\mu m$. Accordingly, their nominal behaviors regarding AC and DC characteristics have been modelled, and model parameters have been adjusted. E.g. f_1 in the extended EKV model becomes $1.74 \times 10^{-4}\,F\,V^{-1}\,s^{-1}$ which is commonly obtained for such devices and the threshold voltage $V_{th} = 0.33\,V$.

In Fig. 5.5(a), the transient simulation results is shown. Once V_{ENABLE} is raised to HIGH, the ring oscillator generates a stable oscillation frequency. From Fig. 5.5(b)-(f), various figure of merits and their dependencies on supply voltage V_{DD} have been simulated, including output frequency f, switching capacitance C_{SW}, switching resistance R_{SW}, active current

I_{DDA} and total power consumption P_{total}. As one can note, when V_{DD} sweeps from 0.6 V to 1 V, the oscillation frequency also increases. This also leads to the increased switching capacitance, which fits well to the capacitance-voltage profiling as investigated before, and the decreased switching resistance because EGT becomes more conductive under high gate voltage. However, the higher operating frequency also leads to higher power consumption, as has been demonstrated by the trend in active current and total power.

Notably, the comparison between the measurement and simulation have also been given. The simulation of aforementioned characteristics is reasonably close to the measurement data from the fabricated circuit.

Conclusively, the ring oscillator design based on print EGT has been demonstrated with an in-depth analysis of its electrical characteristics. Also, it is shown that the proposed nonquasi-static capacitance model for EGTs can provide a reasonable prediction for the designed circuit, which largely facilities the circuit design process.

5.4. Printed full-wave rectifier

Rectifiers are the essential electronic circuit, which can convert alternating current to direct current and thus realizes the voltage regulation. It can find applications in various fields such as energy harvesting and RFID. In printed electronics, the manufacturing of rectifiers has also been studied [112, 50]. Additionally, designs have been reported which utilize solution-processable semiconductors [113, 114, 115, 116, 117].

On one hand, by viewing the literature, one can note that the majority of reports have focused on e.g. radio-frequency applications in the MHz range or even higher. On the other hand, most of the presented circuits require the high operation voltage for the proper operation, often > 10 V. Reasons are the low electron mobility of the printed semiconductor materials, insufficient current ON/OFF ratio and the inevitable built-in potential

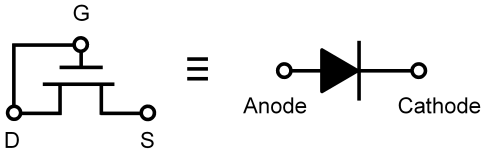

Figure 5.6.: Schematic Diode-connected EGT. Reprint with permission from [110] ©2020 IEEE.

originating from the diode p-n junction that the forward voltage needs to overcome. In consequence, most existing designs fail to process low input voltage level efficiently. This is, however, a vital but challenging feature to empower self-contained systems for smart sensor or Internet-of-things applications. There, many devices merely generate signals with a small amplitude and operate at low frequencies (typical values under 1 kHz).

To address these problems, in this section, the first inkjet-printed full-wave rectifier circuit is demonstrated [110]. The design is based on diode-connected EGTs as shown in Fig. 5.6, which possesses a set of benefits: EGTs technology can operate in the sub-1 V low-voltage regime due to the deployment of the electrolyte-gating approach as investigated in the earlier section; Also, in EGT technology, the transistor threshold voltage can be tuned via various approaches, including channel geometry scaling [118]. With the proper W/L setting, the near-zero threshold voltage can be achieved; Furthermore, in EGTs, the indium oxide semiconductor channel has a similar work function as the ITO source and drain electrodes, theoretically assuring a low ohmic contact. As a result, the printed rectifier design based on EGT technology features the attractive ability to efficiently process low input voltage, which can be useful for niche applications in the domain of energy harvesting.

In this work, diode-connected EGTs are fabricated and characterized, which have a channel geometry of $W = 200\,\mu m$ and $L = 90\,\mu m$. The measured I-V characteristics are shown in Fig. 5.7 on a logarithmic scale. The extracted V_{th} from the measurement is merely $-50\,mV$, while the

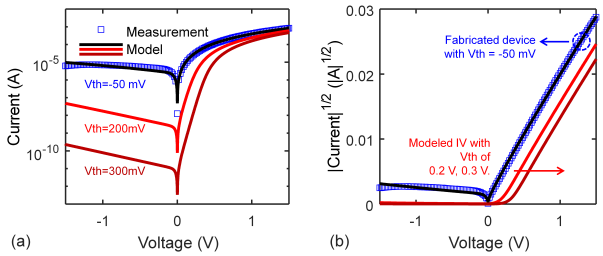

Figure 5.7.: Measured I–V characteristics of the diode-connected EGT. The channel geometry is $W = 200\,\mu m$ and $L = 90\,\mu m$. Also, modeling resulting by shifting the voltage to various values have been presented. (a) I-V characteristics on the logarithmic scale. (b) Square root of drain current versus applied voltage. Reprint with permission from [110] ©2020 IEEE.

current reaches about 800 µA at the applied voltage of 1.5 V. The ON/OFF ratio has reached 10^2 for ±1.5 V. However, it is comparable with reported diode performance based on other inkjet-printing technologies [119].

To demonstrate later, how the rectifier can benefit from devices with near-zero threshold voltage, the I-V characteristics are modeled using the extended EKV model [62, 63]. The model parameters extracted are as $\gamma = 1.8883$, $S = 29.5252$, $f_1 = 0.0009$, $f_2 = 0.5346$, $f_3 = 1$ and $f_4 = 0$. Then, parameter V_{th} is shifted unilaterally from −50 mV to 0.2 V and 0.3 V, and additional virtual I-V characteristics are generated, as shown in Fig. 5.7.

Combined with the modeling of the I-V characteristics, the well-established nonquasi-static capacitance model has also been applied to the devices under investigation to enable more comprehensive simulations. For diode-connected EGTs, gate and drain terminals have been electrically short-circuited. Therefore, the capacitance model is adapted from its original form in Fig. 5.8(a) to Fig. 5.8(b). Here, the model parameters have been adjusted according to the device geometry used in the circuit.

Based on the diode-connected EGTs, the inkjet-printed full-wave rectifier is fabricated and shown in Fig. 5.9. To characterize the rectifier, the sinusoidal signal with 1 V amplitude generated by Keithley 3390 function

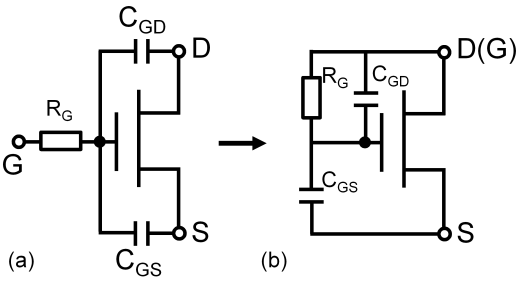

Figure 5.8.: (a) Nonquasi-static capacitance model of EGT. (b) Nonquasi-static capacitance model of diode-connected EGT. Reprint with permission from [110] ©2020 IEEE.

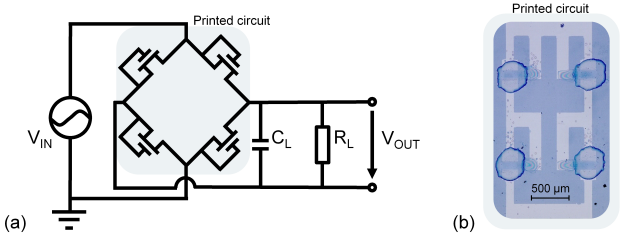

Figure 5.9.: (a) Schematic of full-wave rectifier schematic with the highlighted area marking the printed part of the circuit. (b) Microscopic photo of the fabricated full-wave rectifier. Reprint with permission from [110] ©2020 IEEE.

generator is applied to the input of the circuit, while the output waveform is measured by Yokogawa DLM3022 oscilloscope. During the measurement, the input frequency is swept from 10 Hz to 20 kHz. Also, different load resistors R_L ranging from 5 kΩ to 1 MΩ are tested, whereas the load capacitance R_C is fixed to 20 pF to observe the ripple output waveform.

Prior to the comprehensive characterization of the full-wave rectifier, the simulation has been performed to show quantitatively, how the threshold voltage of EGTs can affect the output performance. The transient output waveform is simulated with the input frequency of 10 Hz, the load

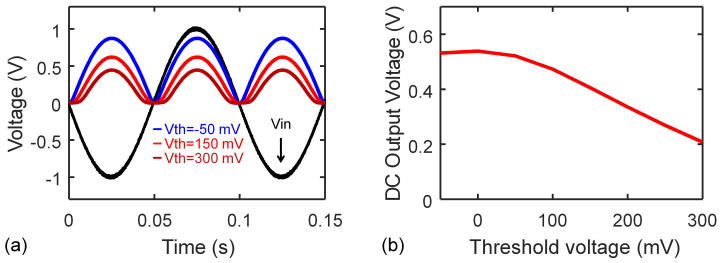

Figure 5.10.: Rectifier circuit simulation with the input frequency of 10 Hz, load capacitance of 20 pF and load resistor of 1 MΩ. (a) Simulated output waveform V_{OUT} based on EGTs with V_{th} from −50 mV to 300 mV. (b) DC output voltage as a function of EGT threshold voltage V_{th}. Reprint with permission from [110] ©2020 IEEE.

capacitor of 20 pF and load resistor of 1 MΩ. Various threshold voltage of EGTs are implemented from −50 mV to 300 mV. As shown in Fig.5.10(a), using $V_{th} = -50$ mV as extracted from the measurement, the maximal voltage drop between peak positions of input and output is 140 mV, which is significantly lower than reported values realized by e.g. organic diodes [112] and beneficial to a high effectiveness for the voltage regulation. Furthermore, as the V_{th} increases, the amplitude of the output waveform decreases. In Fig. 5.10(b), the DC output voltage V_{DC} is evaluated using

$$V_{DC} = \frac{1}{T}\int_0^T v_{out}(t)\, dt, \tag{5.8}$$

and plotted as a function of V_{th}. As can be seen, the maximum V_{DC} can be obtained with $V_{th} = 0$ V, while a deviation of ±50 mV results in a slight decrease in V_{DC}. However, the further increasing V_{th} leads to the significant reduction of V_{DC}. Therefore, conclusively, the V_{th} is an essential parameter in the design of rectifier using diode-connected transistors, which is expected to be near-zero and can be achieved via the selection of the channel geometry in EGT technology.

To experimentally characterize the printed full-wave rectifier, $R_L = 1$ MΩ is chosen, while the input frequency is swept from 10 Hz to 10 kHz. Re-

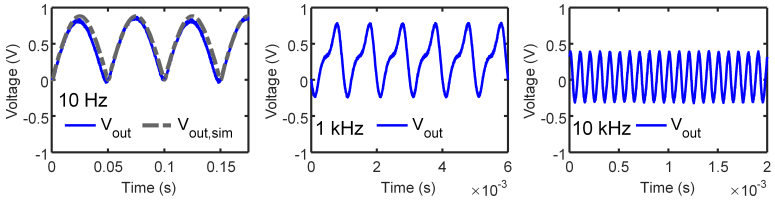

Figure 5.11.: Measured output waveform using the load capacitance of 20 pF and 1 MΩ load resistor at various input frequency: (a) 10 Hz, (b) 1 kHz and (c) 10 kHz. Also, output waveform at 10 Hz is simulated using the proposed EGT models. Reprint with permission from [110] ©2020 IEEE.

sults are presented in Fig. 5.11. At low frequency of 1 kHz in Fig. 5.11(a), the rectifier works properly with a small voltage loss. Also, the simulations show a good agreement with the measurement. As the frequency increases to 10 Hz in Fig. 5.11(b), the decrease in the output amplitude is observed since EGTs starts to work in the nonquasi-static state due to the infinite gate resistance. Consequently, EGTs cannot be turned on and off effectively. Furthermore, when the input frequency approaches 10 kHz, the capacitive shunting through the electrolyte insulator dominates the operation of EGTs. Finally, no more rectification effect can be seen in the output waveform in Fig. 5.11(c).

Next, different load resistors are tested to provide a more comprehensive study on the frequency responses, which are presented in Fig. 5.12(a). Under various R_L, the presented rectifier provides almost a constant V_{DC} at frequency below 300 Hz. Above that, V_{DC} starts to drop fast. Thus, the cut-off frequency of 300 Hz can be determined. Notably, within this region, in particular, some vibrational energy harvesters are functional [120]. At $R_L = 1\,\mathrm{M\Omega}$, the measured V_{DC} is very close to the theoretical maximal value obtained from an ideal, lossless full-wave rectifier, which can be calculated as [121]:

$$V_{DC,max} = \frac{2V_{AC}}{\pi} = 0.637\,\mathrm{V}, V_{AC} = 1\,\mathrm{V}. \tag{5.9}$$

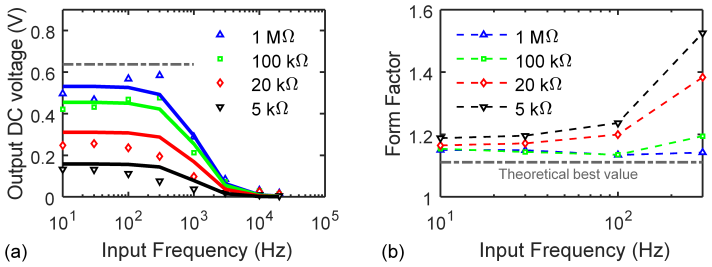

Figure 5.12.: (a) Measured and simulated DC output voltage V_{DC} as a function of the input frequency with various load resistors R_L. (b) Form factor of the inkjet-printed full-wave rectifier in the region below the cutoff frequency. Reprint with permission from [110] ©2020 IEEE.

With a smaller load resistance, the voltage drop over the channel resistance is higher due to the increased output current. Consequently, the decrease in V_{DC} is more pronounced.

As shown in Fig. 5.12(a), using the proposed I-V and nonquasi-static capacitance, a satisfactory agreement has been reached between the measurement and simulation data. The proposed models enhance the understanding of the dynamic behavior of printed full-wave rectifier. Also, it sheds light on the possibilities to increase the speed of the circuit, where the most effective way is to reduce R_G in Fig. 5.8 via the deployment of electrolytes with higher ion mobility.

Additionally, the efficiency of the rectification process has been addressed by calculating the form factor (FF) according to [121, 122] (the lower FF means better):

$$FF = V_{RMS}/V_{DC}, \tag{5.10}$$

$$\text{with } V_{RMS} = \sqrt{\int_0^T \frac{1}{T} v_{out}^2(t)\, dt}, \tag{5.11}$$

where V_{RMS} is the root-mean-square voltage cross R_L. This metric calculated for measurements below the cutoff frequency is shown in Fig. 5.12(b). In general, the form factor below 1.2 is achieved at low frequency with the large R_L, which is close to the theoretical best value for the ideal full-wave rectifier, namely $FF = 1.1$ [121, 122]. This indicates a high efficiency in this region.

Next, the power characteristics as a function of load resistance is calculated, including the DC output power P_{DC} and power conversion efficiency (PCE) according to:

$$P_{DC} = V_{DC}^2/R_L, \tag{5.12}$$

$$PCE = \frac{P_{out}}{P_{in}} = \frac{V_{DC}^2/R_L}{\frac{1}{T}\int_0^T v_{AC}(t) i_{AC}(t)\, dt}, \tag{5.13}$$

where $v_{AC}(t)(t)$ and $i_{AC}(t)(t)$ are the voltage and current waveform from the power supply, respectively. Since $i_{AC}(t)$ is not available during the measurement, it is estimated by:

$$i_{AC} = i_{load} + i_{leak}, \tag{5.14}$$

where i_{load} is the current through R_L, and i_{leak} is the summation of the leakage current when two EGTs are reverse biased. In worst case, $i_{leak} = 2 \times 10\,\mu A$ can be estimated as read from the I-V characteristics in Fig. 5.7(a). The characterization results of P_{DC} and PCE are presented in Fig. 5.13. As one can see, the rectifier generated $P_{DC} > 2.8\,\mu W$ using R_L over the range from $5\,k\Omega$ to $20\,k\Omega$ with the estimated PCE close to 15 %. However, as the R_L increases, both P_{DC} and estimated PCE decreases. The primary reason of the low power efficiency is due to the high gate leakage current of EGTs. The less careful printing of the top-gate materials can contribute to this issue, which needs to be addressed properly in the future development.

Finally, the possibility has been explored that the presented rectifier can work even with $< 1\,V$ input amplitude, which is an attractive feature for many energy harvester applications [123, 124]. The input signal with the frequency of 10 Hz and amplitude ranging from 1.5 V down to 0.5 V is tested, while the load resistance R_L is $1\,M\Omega$. Fig. 5.14(a) shows that the

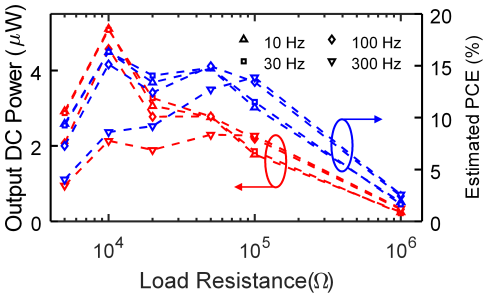

Figure 5.13.: Measurement of DC output power P_{DC} (red) and estimated power conversion efficiency (blue) (under the worst case consideration) as a function of load resistance R_L with various input frequency. Reprint with permission from [110] ©2020 IEEE.

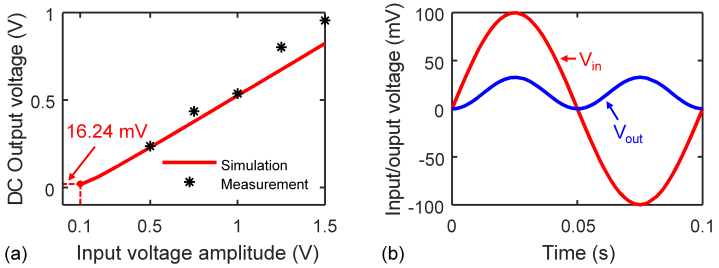

Figure 5.14.: (a) DC output voltage of the full-wave rectifier as a function of the input voltage amplitude. (b) Simulated waveform of the output voltage (blue curve) with an input voltage amplitude of 100 mV (red curve). In both plots, the input frequency is 10 Hz, and the load resistance is 1 MΩ. Reprint with permission from [110] ©2020 IEEE.

measured DC output voltage has a linear dependency on the input amplitude. Also, the rectifier is still functional with the low input amplitude of 0.5 V. Furthermore, the simulation result confirms that the rectifier even works until the input amplitude of 0.1 V, and the simulated transient output wave is displayed in Fig. 5.14(b). Due to a much inferior ON/OFF ratio in this region, the output amplitude becomes as low as 16.24 mV.

Nevertheless, the ability to process such low-voltage input can still be useful to some energy harvesting applications and has not yet been reported in other printed rectifier designs.

5.5. Conclusion

In this chapter, circuit designs have been presented based on inkjet-printed EGTs incorporating inorganic metal oxide semiconductors. Presented basic circuit blocks include the inverter, ring oscillator and full-wave rectifier, which are the foundation to develop more complex electronics circuits. Additionally, the proposed capacitance models in the earlier chapter enable advanced circuit analysis such as transient and AC simulations. Reasonable agreement between the simulation and measurement has been demonstrate. This further facilitates the circuit design process in the field of printed electronics.

6. Summary and outlook

6.1. Summary

Printed electronics is an emerging technology with a set of novel features, which are complementary to conventional silicon technology. Among different types of printed devices, printed transistors are important, which can be used to fabricate various electronic applications. Despite recent progress in improving the electrical performance of printed transistors, the fundamental understanding of their electrical performance is still missing, including AC and noise behavior. However, these are essential in the development of an accurate design flow tool such as a process design kit for printed electronics, which enables advanced circuit simulations such as the analysis of frequency response and signal-to-noise ratio for complex circuits and systems.

In this thesis, printed transistors using solution-processable indium oxide as the channel semiconductor featuring high effective mobility are extensively studied. Also, the electrolyte-gating approach is deployed to enable low-voltage operation ($< 2\,\mathrm{V}$) due to the large gate capacitance ($1\,\mu\mathrm{F\,cm^{-2}}$-$10\,\mu\mathrm{F\,cm^{-2}}$) offered by the electrical double layers. These EGTs open new possibilities to design and fabricate novel low-voltage printed circuits.

This thesis has several contributions to the understanding and advancement of printed electronics including the following aspects:

Chapter 2 introduces briefly the device physics of conventional MOS capacitors and MOSFETs, and the technical background of printed electronics including the fabrication process and material properties.

Chapter 3 presents a systematic study of the capacitance characteristics of EGTs. Using a dedicated equivalent circuit model, an accurate agreement has been achieved between measured and simulated spectra of gate impedance. This reveals important information about the charging mechanism of EGTs. Also, by simulating loss-frequency characteristics, the electrolyte cut-off frequency of $\sim 100\,\mathrm{Hz}$ can be evaluated for EGTs with channel width of $200\,\mu\mathrm{m}$ and length of $50\,\mu\mathrm{m}$. It is also shown that EGTs have the potential to achieve the operating frequency in the kHz regime, which can be feasibly improved by reducing the top-gate resistance and increasing the ionic conductivity of the electrolyte. Furthermore, a Meyer-like compact capacitance model of EGTs has been developed, which provides reasonable fit to the measured lumped voltage-dependent terminal capacitance. Both the parasitic and nonquasi-static effects have been considered. This lays a sound foundation for accurate AC and transient circuit simulations within a process design kit for complex EGTs circuits.

Chapter 4 investigates the low-frequency noise characteristics of EGTs. A dedicated experimental setup is established to provide an accurate noise measurement. The setup is also verified by the measurement of thermal noise from thin-film resistors and comparison with the Johnson-Nyquist theory. Next, the flicker noise of EGT is measured and analyzed. It is proved from the experimental data that the carrier number fluctuation with correlated mobility fluctuation is the dominant noise generation mechanism in EGT technology. Furthermore, to represent the overall noise level, the normalized flat-band voltage noise is extracted from measurement data. In comparison with other thin-film technologies with dielectric gating, the extracted value of $1.08 \times 10^{-7}\,\mathrm{V}^2\,\mu\mathrm{m}^2$ is considerably lower than reported values in literature. The deployment of electrolyte-gating can be a plausible reason. This conclusion renders the EGT technology very useful in the design of circuits for low noise applications.

Chapter 5 presents circuit designs of circuits based on EGT technology, including basic digital building blocks such as inverters and ring oscillators. The fabricated single-stage inverter works properly regarding its input and output relationship, while the three-stage ring oscillator generates the stable oscillation output between 250 Hz to 300 Hz under the supply voltage of 0.6 V to 1 V. Besides, the first design of printed full-wave rectifier using EGT technology has been proposed. It utilizes diode-connected EGTs as the equivalent for diodes, which feature near-zero threshold voltage that is achieved by proper channel geometry scaling. Consequently, the rectifier can effectively process input voltage with small amplitude down to 100 mV below the cut-off frequency of 300 Hz. These features can be beneficial for the application domain of energy harvesting. Furthermore, the nonquasi-static capacitance model developed in Chapter 3 is verified on the proposed circuits, showing satisfactory simulation results for the proposed circuits as compared to the experimental data.

6.2. Outlook

Despite results in the capacitance characterization and modeling for EGTs, most of the modeling approaches used in this thesis are empirical, which lacks physical *ab initio* calculations. Other shortcomings are that the Meyer-like model can produce unrealistic simulation results under certain circumstances, simply because it fails to preserve the charge conservation law. Although the physical models are challenging for printed electronics due to the large process variation, they are still necessary in future development to deliver more accurate simulation results. Additionally, the emphasis of future work can be laid on the variation modeling of the transistor capacitance, which requires a large amount of experimental data, but can enable accurate Monte-Carlo simulation of circuits.

It is of high interest to develop more building blocks for digital and analog circuits, such as flip-flops and operational amplifiers. This will enable the development of more complex circuits and systems to expand the application domain of printed electronics.

In this thesis, the primary noise generation mechanism in EGT technology has been clarified, where the low-frequency noise measurement is only conducted in the linear region of the transistor. In the next step, it is necessary to characterize EGTs in the whole operation region including the saturation region. Based on that, a comprehensive noise model can be developed, which can be utilized in circuit simulations.

Bibliography

[1] *Moore's law - Wikipedia*. https://en.wikipedia.org/wiki/Moore's_law. (Accessed on 01/13/2021).

[2] *The Story of the Intel® 4004*. https://www.intel.com/content/www/us/en/history/museum-story-of-intel-4004.html. (Accessed on 01/07/2021).

[3] *AMD's 64-Core EPYC CPU Stripped: A Detailed Inside Look | Tom's Hardware*. https://www.tomshardware.com/news/amd-64-core-epyc-cpu-die-design-architecture-ryzen-3000. (Accessed on 01/07/2021).

[4] *TSMC says 3nm plant could cost it more than $20bn*. https://web.archive.org/web/20171012043608/https://www.theinquirer.net/inquirer/news/3018890/tsmc-says-3nm-plant-could-cost-it-more-than-usd20bn. (Accessed on 01/07/2021).

[5] Hideki Shirakawa et al. "Synthesis of electrically conducting organic polymers: halogen derivatives of polyacetylene,$(CH)_x$". In: *Journal of the Chemical Society, Chemical Communications* 16 (1977), pp. 578–580.

[6] F Ebisawa, T Kurokawa, and S Nara. "Electrical properties of polyacetylene/polysiloxane interface". In: *Journal of applied physics* 54.6 (1983), pp. 3255–3259.

[7] A Tsumura, H Koezuka, and TJAPL Ando. "Macromolecular electronic device: Field-effect transistor with a polythiophene thin film". In: *Applied Physics Letters* 49.18 (1986), pp. 1210–1212.

[8] Zhenan Bao et al. “High-performance plastic transistors fabricated by printing techniques”. In: *Chemistry of Materials* 9.6 (1997), pp. 1299–1301.

[9] Francesco Segatta, Gianluca Lattanzi, and Pietro Faccioli. “Predicting Charge Mobility of Organic Semiconductors with Complex Morphology”. In: *Macromolecules* 51.21 (2018), pp. 9060–9068.

[10] Zheng Cui. *Printed electronics: Materials, technologies and applications*. John Wiley & Sons, 2016.

[11] Suresh Kumar Garlapati et al. “Printed electronics based on inorganic semiconductors: from processes and materials to devices”. In: *Advanced Materials* 30.40 (2018), p. 1707600.

[12] Jaakko Leppaeniemi et al. “Far-UV annealed inkjet-printed In_2O_3 semiconductor layers for thin-film transistors on a flexible polyethylene naphthalate substrate”. In: *ACS applied materials & interfaces* 9.10 (2017), pp. 8774–8782.

[13] Donald Lupo et al. “OE-A roadmap for organic and printed electronics”. In: *Applications of Organic and Printed Electronics*. Springer, 2013, pp. 1–26.

[14] *Transparent OLEDs for Subway Train Windows | Printed Electronics World*. https://www.printedelectronicsworld.com/articles/21523/transparent-oleds-for-subway-train-windows. (Accessed on 09/13/2020).

[15] Yinji Ma et al. “Flexible hybrid electronics for digital healthcare”. In: *Advanced Materials* 32.15 (2020), p. 1902062.

[16] *Stick-On Electronic Tattoos | MIT Technology Review*. https://www.technologyreview.com/2011/08/11/192404/stick-on-electronic-tattoos/. (Accessed on 09/13/2020).

[17] *Dental Care*. https://www.innovationlab.de/en/services/showcases-printed-electronics/dental-care/. (Accessed on 09/13/2020).

[18] Vivek Subramanian et al. “Printed organic transistors for ultra-low-cost RFID applications”. In: *IEEE transactions on components and packaging technologies* 28.4 (2005), pp. 742–747.

[19] Tamaki Soga et al. “Inkjet-printed paper-based colorimetric sensor array for the discrimination of volatile primary amines”. In: *Analytical chemistry* 85.19 (2013), pp. 8973–8978.

[20] Devi D Liana et al. “Recent advances in paper-based sensors”. In: *sensors* 12.9 (2012), pp. 11505–11526.

[21] R Das, X He, and K Ghaffarzadeh. “Flexible, printed and organic electronics 2019–2029: forecasts, players & opportunities”. In: *IDTechEx Research* (2018).

[22] *Flexible, gedruckte und organische Elektronik 2020-2030: Prognosen, Technologien, Märkte: IDTechEx*. `https://www.idtechex.com/de/research-report/flexible-printed-and-organic-electronics-2020-2030-forecasts-technologies-markets/687`. (Accessed on 01/22/2021).

[23] Bing J Sheu et al. “BSIM: Berkeley short-channel IGFET model for MOS transistors”. In: *IEEE Journal of Solid-State Circuits* 22.4 (1987), pp. 558–566.

[24] *Organic Process Design Kit*. `http://opdk.umn.edu/index.html`. (Accessed on 09/14/2020).

[25] Jia Zhou, Tong Ge, and Joseph S Chang. “Fully-additive printed electronics: Process development kit”. In: *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE. 2016, pp. 862–865.

[26] Marco Fattori et al. “Circuit design and design automation for printed electronics”. In: *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE. 2019, pp. 42–47.

[27] Behzad Razavi. *Design of analog CMOS integrated circuits*. Tata McGraw-Hill Education, 2002.

[28] Yuan Taur and Tak H Ning. *Fundamentals of modern VLSI devices*. Cambridge university press, 2013.

[29] AL McWhorter and RH Kingston. "Semiconductor surface physics". In: *Univerisity of Pennsylvania Press, Philadelphia, PA* 207 (1957).

[30] Friits N Hooge. "1/f noise sources". In: *IEEE Transactions on electron devices* 41.11 (1994), pp. 1926–1935.

[31] Sichao Tong, Jia Sun, and Junliang Yang. "Printed thin-film transistors: research from China". In: *ACS applied materials & interfaces* 10.31 (2018), pp. 25902–25924.

[32] DJ Gundlach et al. "An experimental study of contact effects in organic thin film transistors". In: *Journal of Applied Physics* 100.2 (2006), p. 024509.

[33] Seungjun Chung, Kyungjune Cho, and Takhee Lee. "Recent progress in inkjet-printed thin-film transistors". In: *Advanced science* 6.6 (2019), p. 1801445.

[34] Katsuaki Suganuma. *Introduction to printed electronics*. Vol. 74. Springer Science & Business Media, 2014.

[35] Organic, Printed Electronics Association, et al. *Organic and Printed Electronics: Applications, Technologies and Suppliers*. 2013.

[36] Xiaosong Du et al. "Amorphous In-Ga-Zn-O thin-film transistors fabricated by microcontact printing". In: *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* 33.5 (2015), p. 052208.

[37] Yan Wu et al. "Ultraviolet light sensitive In-doped ZnO thin film field effect transistor printed by inkjet technique". In: *physica status solidi (a)* 208.1 (2011), pp. 206–209.

[38] Zhe Liu et al. "Contact printing of horizontally aligned Zn_2GeO_4 and $In_2Ge_2O_7$ nanowire arrays for multi-channel field-effect transistors and their photoresponse performances". In: *Journal of Materials Chemistry C* 1.1 (2013), pp. 131–137.

[39] Dawei Sun et al. "High performance inkjet-printed metal oxide thin film transistors via addition of insulating polymer with proper molecular weight". In: *Applied Physics Letters* 112.1 (2018), p. 012102.

[40] Yi-Kuei Chang and Franklin Chau-Nan Hong. “The fabrication of ZnO nanowire field-effect transistors by roll-transfer printing”. In: *Nanotechnology* 20.19 (2009), p. 195302.

[41] Gui Chen et al. “Single-crystalline p-type Zn_3As_2 nanowires for field-effect transistors and visible-light photodetectors on rigid and flexible substrates”. In: *Advanced Functional Materials* 23.21 (2013), pp. 2681–2690.

[42] Xinzhou Wu et al. “A new nanocomposite dielectric ink and its application in printed thin-film transistors”. In: *Composites Science and Technology* 94 (2014), pp. 117–122.

[43] Bongjun Kim et al. “High-speed, inkjet-printed carbon nanotube/zinc tin oxide hybrid complementary ring oscillators”. In: *Nano letters* 14.6 (2014), pp. 3683–3687.

[44] Seong Hun Yu et al. “In/Ga-free, inkjet-printed charge transfer doping for solution-processed ZnO”. In: *ACS applied materials & interfaces* 5.19 (2013), pp. 9765–9769.

[45] Athavan Nadarajah et al. “Amorphous In–Ga–Zn oxide semiconducting thin films with high mobility from electrochemically generated aqueous nanocluster inks”. In: *Chemistry of Materials* 27.16 (2015), pp. 5587–5596.

[46] Subho Dasgupta et al. “Inkjet printed, high mobility inorganic-oxide field effect transistors processed at room temperature”. In: *ACS nano* 5.12 (2011), pp. 9628–9638.

[47] Yong-Hoon Kim et al. “Flexible metal-oxide devices made by room-temperature photochemical activation of sol–gel films”. In: *Nature* 489.7414 (2012), pp. 128–132.

[48] Yasunori Takeda et al. “Fabrication of ultra-thin printed organic TFT CMOS logic circuits optimized for low-voltage wearable sensor applications”. In: *Scientific reports* 6.1 (2016), pp. 1–9.

[49] E Gili, M Caironi, and H Sirringhaus. “Organic integrated complementary inverters with ink-jet printed source/drain electrodes and sub-micron channels”. In: *Applied Physics Letters* 100.12 (2012), p. 77.

[50] Minhun Jung et al. “All-printed and roll-to-roll-printable 13.56-MHz-operated 1-bit RF tag on plastic foils”. In: *IEEE Transactions on Electron Devices* 57.3 (2010), pp. 571–580.

[51] Guangming Wang et al. “Poly (3-hexylthiophene) field-effect transistors with high dielectric constant gate insulator”. In: *Journal of applied physics* 95.1 (2004), pp. 316–322.

[52] Leszek Artur Majewski, Raoul Schroeder, and Martin Grell. “Flexible high capacitance gate insulators for organic field effect transistors”. In: *Journal of Physics D: Applied Physics* 37.1 (2003), p. 21.

[53] Sung Wook Park and Ho Bin Im. “Effects of oxidation conditions on the properties of tantalum oxide films on silicon substrates”. In: *Thin Solid Films* 207.1-2 (1992), pp. 258–264.

[54] Matthew J Panzer, Christopher R Newman, and C Daniel Frisbie. “Low-voltage operation of a pentacene field-effect transistor with a polymer electrolyte gate dielectric”. In: *Applied Physics Letters* 86.10 (2005), p. 103503.

[55] S Ono et al. “High-mobility, low-power, and fast-switching organic field-effect transistors with ionic liquids”. In: *Applied Physics Letters* 92.10 (2008), p. 93.

[56] Keun Hyung Lee et al. “Electrical impedance of spin-coatable ion gel films”. In: *The Journal of Physical Chemistry B* 115.13 (2011), pp. 3315–3321.

[57] Yiyong He et al. “Ion gels by self-assembly of a triblock copolymer in an ionic liquid”. In: *The Journal of Physical Chemistry B* 111.18 (2007), pp. 4645–4652.

[58] Atsushi Noro, Mikihiro Hayashi, and Yushu Matsushita. “Design and properties of supramolecular polymer gels”. In: *Soft Matter* 8.24 (2012), pp. 6416–6429.

[59] Suresh Kumar Garlapati et al. “Electrolyte-gated, high mobility inorganic oxide transistors from printed metal halides”. In: *ACS applied materials & interfaces* 5.22 (2013), pp. 11498–11502.

[60] Yu Xia et al. “Correlation of on-state conductance with referenced electrochemical potential in ion gel gated polymer transistors”. In: *Applied Physics Letters* 94.1 (2009), p. 4.

[61] Subho Dasgupta et al. “Printed and Electrochemically Gated, High-Mobility, Inorganic Oxide Nanoparticle FETs and Their Suitability for High-Frequency Applications”. In: *Advanced Functional Materials* 22.23 (2012), pp. 4909–4919.

[62] Farhan Rasheed et al. “A smooth EKV-based DC model for accurate simulation of printed transistors and their process variations”. In: *IEEE Transactions on Electron Devices* 65.2 (2018), pp. 667–673.

[63] Farhan Rasheed et al. “Variability modeling for printed inorganic electrolyte-gated transistors and circuits”. In: *IEEE Transactions on Electron Devices* 66.1 (2018), pp. 146–152.

[64] Mark E Orazem and Bernard Tribollet. “Electrochemical impedance spectroscopy”. In: *New Jersey* (2008).

[65] A Wadsworth. “The parametric measurement handbook”. In: *Agilent Technologies Inc., USA* (2012).

[66] Deyu Tu et al. “A static model for electrolyte-gated organic field-effect transistors”. In: *IEEE transactions on electron devices* 58.10 (2011), pp. 3574–3582.

[67] Katharina Melzer et al. “Characterization and simulation of electrolyte-gated organic field-effect transistors”. In: *Faraday discussions* 174 (2014), pp. 399–411.

[68] Jiyoul Lee et al. “Ion gel-gated polymer thin-film transistors: Operating mechanism and characterization of gate dielectric capacitance, switching speed, and stability”. In: *The Journal of Physical Chemistry C* 113.20 (2009), pp. 8972–8981.

[69] Lars Herlogsson et al. “Polyelectrolyte-gated organic complementary circuits operating at low power and voltage”. In: *Advanced Materials* 23.40 (2011), pp. 4684–4689.

[70] M Singh et al. “The double layer capacitance of ionic liquids for electrolyte gating of ZnO thin film transistors and effect of gate electrodes”. In: *Journal of Materials Chemistry C* 5.14 (2017), pp. 3509–3518.

[71] Xiaowei Feng et al. “Impact of intrinsic capacitances on the dynamic performance of printed electrolyte-gated inorganic field effect transistors”. In: *IEEE Transactions on Electron Devices* 66.8 (2019), pp. 3365–3370.

[72] Gabriel Cadilha Marques et al. “Influence of humidity on the performance of composite polymer electrolyte-gated field-effect transistors and circuits”. In: *IEEE Transactions on Electron Devices* 66.5 (2019), pp. 2202–2207.

[73] Gabriel Cadilha Marques et al. “Electrolyte-gated FETs based on oxide semiconductors: Fabrication and modeling”. In: *IEEE Transactions on Electron Devices* 64.1 (2016), pp. 279–285.

[74] Jinhee Kang et al. “Development of an equivalent circuit model for electrochemical double layer capacitors (EDLCs) with distinct electrolytes”. In: *Electrochimica Acta* 115 (2014), pp. 587–598.

[75] Elliot Schmidt et al. “Characterization of the electric double layer formation dynamics of a metal/ionic liquid/metal structure”. In: *ACS applied materials & interfaces* 8.23 (2016), pp. 14879–14884.

[76] Feilong Liu et al. “Coupling of channel conductance and gate-to-channel capacitance in electric double layer transistors”. In: *Applied Physics Letters* 103.19 (2013), 209_1.

[77] Vera Lockett et al. “Differential capacitance of the electrical double layer in imidazolium-based ionic liquids: influence of potential, cation size, and temperature”. In: *The Journal of Physical Chemistry C* 112.19 (2008), pp. 7486–7495.

[78] Tamás Pajkossy. “Impedance spectroscopy at interfaces of metals and aqueous solutions—Surface roughness, CPE and related issues”. In: *Solid State Ionics* 176.25-28 (2005), pp. 1997–2003.

[79] Thomas C Halsey. “Frequency dependence of the double-layer impedance at a rough surface”. In: *Physical Review A* 35.8 (1987), p. 3512.

[80] Mordecai Avriel. *Nonlinear programming: analysis and methods*. Courier Corporation, 2003.

[81] Tsusyoshi Funaki and Takashi Hikihara. “Characterization and modeling of the voltage dependency of capacitance and impedance frequency characteristics of packed EDLCs”. In: *IEEE transactions on power electronics* 23.3 (2008), pp. 1518–1525.

[82] Tarek Zaki et al. “Accurate capacitance modeling and characterization of organic thin-film transistors”. In: *IEEE Transactions on Electron Devices* 61.1 (2013), pp. 98–104.

[83] Gabriel Cadilha Marques et al. “Digital power and performance analysis of inkjet printed ring oscillators based on electrolyte-gated oxide electronics”. In: *Applied Physics Letters* 111.10 (2017), p. 102103.

[84] Kangmin Kim and Youngmin Kim. “Intrinsic capacitance characteristics of top-contact organic thin-film transistors”. In: *IEEE transactions on electron devices* 57.9 (2010), pp. 2344–2347.

[85] Antonio Valletta et al. “Modeling of capacitance characteristics of printed p-type organic thin-film transistors”. In: *IEEE Transactions on Electron Devices* 61.12 (2014), pp. 4120–4127.

[86] Imad Benacer and Zohir Dibi. “Modeling and simulation of organic field effect transistor (OFET) using artificial neural networks”. In: *International Journal of Advanced Science and Technology* 66 (2014), pp. 79–88.

[87] Xiaowei Feng et al. “Nonquasi-Static Capacitance Modeling and Characterization for Printed Inorganic Electrolyte-Gated Transistors in Logic Gates”. In: *IEEE Transactions on Electron Devices* 66.12 (2019), pp. 5272–5277.

[88] Luis Zubieta and Richard Bonert. “Characterization of double-layer capacitors for power electronics applications”. In: *IEEE Transactions on industry applications* 36.1 (2000), pp. 199–205.

[89] S Thiemann et al. “Ionic liquids for electrolyte-gating of ZnO field-effect transistors”. In: *The Journal of Physical Chemistry C* 116.25 (2012), pp. 13536–13544.

[90] Tarek Zaki et al. “AC characterization of organic thin-film transistors with asymmetric gate-to-source and gate-to-drain overlaps”. In: *Organic Electronics* 14.5 (2013), pp. 1318–1322.

[91] Mehmet A Cirit. “The Meyer model revisited: Why is charge not conserved?(MOS transistor)”. In: *IEEE transactions on computer-aided design of integrated circuits and systems* 8.10 (1989), pp. 1033–1037.

[92] Gerard Ghibaudo et al. “Improved analysis of low frequency noise in field-effect MOS transistors”. In: *physica status solidi (a)* 124.2 (1991), pp. 571–581.

[93] Kwok K Hung et al. “A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors”. In: *IEEE Transactions on Electron Devices* 37.3 (1990), pp. 654–665.

[94] Gérard Ghibaudo and T Boutchacha. “Electrical noise and RTS fluctuations in advanced CMOS devices”. In: *Microelectronics Reliability* 42.4-5 (2002), pp. 573–582.

[95] Pedro Barquinha et al. *Transparent oxide electronics: from materials to devices*. John Wiley & Sons, 2012.

[96] Christoforos G Theodorou et al. “Origin of low-frequency noise in the low drain current range of bottom-gate amorphous IGZO thin-film transistors”. In: *IEEE electron device letters* 32.7 (2011), pp. 898–900.

[97] Hyun-Sik Choi et al. “Verification of interface state properties of a-InGaZnO thin-Film transistors with SiN_x and SiO_2 gate dielectrics by low-frequency noise measurements”. In: *IEEE electron device letters* 32.8 (2011), pp. 1083–1085.

[98] Yuan Liu et al. “Analysis and simulation of low-frequency noise in indium-zinc-oxide thin-film transistors”. In: *IEEE Journal of the Electron Devices Society* 6 (2018), pp. 271–279.

[99] FN Hooge. “1/f noise”. In: *Physica B+ C* 83.1 (1976), pp. 14–23.

[100] D Rigaud, M Valenza, and J Rhayem. “Low frequency noise in thin film transistors”. In: *IEE Proceedings-Circuits, Devices and Systems* 149.1 (2002), pp. 75–82.

[101] Hongyu He, Xueren Zheng, and Shengdong Zhang. “$1/f$ Noise Expressions for Amorphous InGaZnO TFTs Considering Mobility Power-Law Parameter in Above-Threshold Regime”. In: *IEEE Electron Device Letters* 36.2 (2014), pp. 156–158.

[102] Gérard Ghibaudo. “Analytical modelling of the MOS transistor”. In: *physica status solidi (a)* 113.1 (1989), pp. 223–240.

[103] Yashu Swami and Sanjeev Rai. “Comparative methodical assessment of established MOSFET threshold voltage extraction methods at 10-nm technology node”. In: *Circuits and Systems* 7.13 (2016), pp. 4248–4279.

[104] Michael J Buckingham. *Noise in electronic devices and systems*. Horwood, 1983.

[105] F Crupi et al. “Impact of the interfacial layer on the low-frequency noise (1/f) behavior of MOSFETs with advanced gate stacks”. In: *IEEE Electron Device Letters* 27.8 (2006), pp. 688–691.

[106] Jae Chul Park et al. “Low-frequency noise in amorphous indium-gallium-zinc oxide thin-film transistors from subthreshold to saturation”. In: *Applied Physics Letters* 97.12 (2010), p. 122104.

[107] Shun Watanabe et al. “Remarkably low flicker noise in solution-processed organic single crystal transistors”. In: *Communications Physics* 1.1 (2018), pp. 1–8.

[108] Yuan Liu et al. “Low-frequency noise in hybrid-phase-microstructure ITO-stabilized ZnO thin-film transistors”. In: *IEEE Electron Device Letters* 39.2 (2017), pp. 200–203.

[109] Xiaochen Ma et al. “Low-Frequency Noise in Electric Double Layer InGaZnO Thin-Film Transistors Gated with Sputtered SiO2-Based Electrolyte”. In: *ACS Applied Electronic Materials* 1.6 (2019), pp. 972–976.

[110] Xiaowei Feng et al. “An Inkjet-Printed Full-Wave Rectifier for Low-Voltage Operation Using Electrolyte-Gated Indium-Oxide Thin-Film Transistors”. In: *IEEE Transactions on Electron Devices* 67.11 (2020), pp. 4918–4923.

[111] Manjul Bhushan and Mark B Ketchen. *Microelectronic test structures for CMOS technology*. Springer Science & Business Media, 2011.

[112] Petri S Heljo et al. “Printed half-wave and full-wave rectifier circuits based on organic diodes”. In: *IEEE transactions on electron devices* 60.2 (2013), pp. 870–874.

[113] Kris Myny et al. “An integrated double half-wave organic Schottky diode rectifier on foil operating at 13.56 MHz”. In: *Applied physics letters* 93.9 (2008), p. 324.

[114] Chang-Yu Lin et al. “High-frequency polymer diode rectifiers for flexible wireless power-transmission sheets”. In: *Organic Electronics* 12.11 (2011), pp. 1777–1782.

[115] Soeren Steudel et al. “50 MHz rectifier based on an organic diode”. In: *Nature materials* 4.8 (2005), pp. 597–600.

[116] Miao Li et al. “0.7-GHz Solution-Processed Indium Oxide Rectifying Diodes”. In: *IEEE Transactions on Electron Devices* 67.1 (2019), pp. 360–364.

[117] Stuart G Higgins et al. “Organic Diode Rectifiers Based on a High-Performance Conjugated Polymer for a Near-Field Energy-Harvesting Circuit”. In: *Advanced Materials* 29.46 (2017), p. 1703782.

[118] Gabriel Cadilha Marques et al. “Printed logic gates based on enhancement-and depletion-mode electrolyte-gated transistors”. In: *IEEE Transactions on Electron Devices* 67.8 (2020), pp. 3146–3151.

[119] AG Martinez-Lopez et al. “Electrical Characterization of Schottky Diodes Based on Inkjet-Printed TiO_2 Films”. In: *IEEE Electron Device Letters* 39.12 (2018), pp. 1940–1943.

[120] CB Williams and Rob B Yates. “Analysis of a micro-electric generator for microsystems”. In: *sensors and actuators A: Physical* 52.1-3 (1996), pp. 8–11.

[121] Cheruku Dharma Raj et al. *Electronic devices and circuits*. Pearson Education India, 2008.

[122] Roberto Visintini. “Rectifiers”. In: *CAS CERN Accelerator School Specialized Course on Power Converters* (2006), pp. 133–183.

[123] Marcel Gueltig et al. “High-Performance thermomagnetic generators based on heusler alloy films”. In: *Advanced energy materials* 7.5 (2017), p. 1601879.

[124] Christian Peters et al. “An ultra-low-voltage active rectifier for energy harvesting applications”. In: *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*. IEEE. 2010, pp. 889–892.

A. Glossary

Abbreviation

AC Alternating Current

BFGS Broyden–Fletcher–Goldfarb– Shanno

BJT Bipolar Junction Transistor

BSIM Berkeley Short-channel IGFET Model

C-V Capacitance-voltage

CMOS Complementary Metal-oxide-semiconductor

CSPE Composite Solid Polymer Electrolyte

DC Direct Current

DUT Device Under Test

EDL Electric Double Layer

EGT Electrolyte-gated Field-effect Transistor

EKV Enz–Krummenacher–Vittoz

FF Form Factor

FFT Fast Fourier Transformation

I-V Current-voltage

IoT Internet of Things

JFET Junction Field-effect Transistors

MOS Metal-oxide-semiconductor

MOSFET Metal-oxide-semiconductor Field-effect Transistor

NMOS N-type Metal-oxide-semiconductor

NQS Nonquasi-static

OE-A Organic Electronics Association

OFETs Organic Field-effect Transistors

OLEDs Organic Light Emitting Diodes

PCE Power Conversion Efficiency

PDK Process Design Kit

PE Printed Electronics

PMOS P-type Metal-oxide-semiconductor

PSD Power Spectral Density

QS Quasi-static

R-C Resistor-capacitor

RF-IV Radio-frequency Current-voltage

RFID Radio-frequency Identification

RTL Resistor-transistor Logic

SPICE Simulation Program with Integrated Circuit Emphasis

TFT Thin-film Transistor

VLSI Very Large-scale Integration

Nomenclature

α_H Hooges Parameter

a_t Tunnel Attenuation Distance

C_{DEP} Depletion Capacitor

$C_{E/CH}$ Capacitor at the Electrolyte/channel Interface

$C_{E/D}$ Overlap Double Layer Capacitance at the Drain Side

C_{EDL} Electric Double Layer Capacitor

$C_{E/S}$ Overlap Double Layer Capacitance at the Source Side

$C_{G/E}$ Electric Double Layer Capacitor at the Gate/electrolyte Interface

C_{GD} Gate-drain Capacitance

$C_{GD,ext}$ Extrinsic Gate-drain Capacitance

$C_{GD,int}$ Intrinsic Gate-drain Capacitance

C_{GEO} Geometric Capacitance

C_{GG} Total Gate Capacitance in MOSFET

$C_{GG,ext}$ Extinsic Total Gate Capacitance in MOSFET

$C_{GG,int}$ Intinsic Total Gate Capacitance in MOSFET

C_{GS} Gate-source Capacitance

$C_{GS,ext}$ Extrinsic Gate-source Capacitance

$C_{GS,int}$ Intrinsic Gate-source Capacitance

C_i Gate Capacitance Per Unit Area

C_{INV} Inversion Capacitance

C_J Junction Capacitance

C_{OV} Overlap Capacitance

C_{OX} Gate Oxide Capacitor

C_{SC} Semiconductor Capacitance

C_{stray} Stray Capacitance

C_{SW} Switching Capacitance

$\Delta\mu$ Carrier Mobility Fluctuation

ΔN Carrier Number Fluctuation without Correlated Mobility Fluctuation

$\Delta N - \Delta\mu$ Carrier Number Fluctuation with Correlated Mobility Fluctuation

E_0 Free Electron Level

E_C Conduction Band

E_F Fermi Level

ϵ_0 Vacuum Permittivity (=$8.8 \times 10^{-12}\,\mathrm{F\,m^{-1}}$)

ϵ_{DEL} Relative Dielectric Constant of Dielectric Materials

ϵ_{SUB} Dielectric Constant of the Substrate Materia

E_V Valence Band

f_C Electrolyte Cut-off Frequency

f_T Transition Frequency

g_m Transconductance

H_c High Current

H_p High Potential

$i_{AC}(t)$ Transient Current Waveform

I_D Drain Current

I_{DDA} Active Current

I_{DDQ} Quiescent Current

i_{leak} Transient Leakage Current Waveform

i_{load} Transient Load Current Waveform

I_{offset} Offset Current Source

I_{SW} Switching Current

k_B Boltzmann Constant (=$1.38 \times 10^{-23}\,\mathrm{J\,K^{-1}}$)

L Channel Length

λ Modulation Coefficient

λ_D Debye Screening Length

L_c Low Current

L_p Low Potential

μ_{FET} Field-effect Mobility

n Slope Factor

N_{IT} Trap Density at the Channel-insulator Interface

N_T Trap Density in the Semiconductor Material

N_{tot} Total Number of Charge Carrier

P_A Active Power

P_{DC} DC Output Power

ϕ_t Thermal Voltage

P_Q Quiescent Power

P_{total} Total Power

q Elementary Charge (= 1.6×10^{-19} C)

Q_{ACC} Accumulation Charge

Q_G Gate Charge

Q_i Charge Carrier Per Unit Area in the Bulk Channel

Q_{INV} Inversion Charge

Q_{IT} Channel/insulator Interface Charge

$Q_i(x)$ Local Gate Charge

R_{BULK} Ionic Resistance of the Bulk Electrolyte

R_C Load Capacitance

R_{EL} Electrolyte Bulk Resistance

R_f Feedback Resistance

R_G Effective Gate Resistor

R_L Load Resistance

R_{SW} Switching Resistance

S Sub-threshold Slope

S_i Power Spectral Density of Current Noise

S_{I_D} Drain Current Noise Power Spectral Density

σ Specific Resistivity

S_{I_R} Current Power Spectral Density of Resistor

S_V Power Spectral Density of Voltage Noise

$S_{V_{FB}}$ Flat-band Voltage Noise Power Spectral Density

S_{V_G} Gate Voltage Noise Power Spectral Density

T Temperature

τ_p Propagation Delay

θ Mobility Attenuation Factor

t_{phl} Propagation Delay of HIGH-LOW

t_{plh} Propagation Delay of LOW-HIGH

v_d Normalized Drain Voltage

v_p Normalized Channel Voltage

v_s Normalized Source Voltage

$v_{AC}(t)$ Transient Voltage

V_{DC} DC Output Voltage

V_{DD} Supply Voltage

V_{DS} Drain-source Bias

V_{DSe} Effective Gate Drain-source Voltage

V_{ENABLE} Enabling Signal

V_{FB} Flat-band Voltage

V_G Gate Voltage of MOS Capacitor

V_{GG} Gate Voltage of Transistor

V_{GS} Gate-source Bias

V_{GTe} Effective Over-drive Voltage

V_{th} Threshold Voltage

W Channel Width

W_{DEP} Depletion Layer Thickness

$Z_{E/CH}$ Impedance at the Electrolyte/channel Interface

Z_{GG} Gate Impedance

Chemical elements and compounds

Cu_2O Copper(II)-oxide

CuO Copper(I)-oxide

DMSO Dimethyl Sulfoxide

IGZO Indium-gallium-zinc-oxide

In_2O_3 Indium(III)-oxid

$In(NO_3)_3 \cdot \times H2O$ Indium(III)-nitrate-hydrate

ITO Indium-tin-oxide

IZO Indium-zinc-oxide

$LiCLO_4$ Lithium Perchlorate

PC Propylene Carbonate

PEDOT:PSS Poly(3,4-ethylenedioxythiophene) Polystyrene Sulfonate

PEN Polyethylene Naphthalate

PET Polyethylene Terephthalate

PVA Polyvinyl Alcohol

ZnO Zinc-oxide

ZTO Zinc-tin-oxide