# A 50 kW Power Hardware-in-the-Loop Test Bench for Permanent Magnet Synchronous Machines based on a Modular Multilevel Converter

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## Keywords

≪Modular Multilevel Converter≫, ≪Power Hardware-in-the-Loop≫, ≪Testing≫, ≪Permanent Magnet Synchronous Machine≫

## Abstract

This paper presents a power hardware-in-the-loop (PHIL) test bench for the emulation of highly utilized permanent magnet synchronous machines based on a square-wave powered Modular Multilevel Converter (SPMMC). Comparisons of the measurement results between an automotive machine and the PHIL during steady state operation and high dynamic current steps are done to show the performance of the PHIL test bench.

## Introduction

In recent times, the rapid development of electric drive trains has become increasingly important. In the first development phase various tools are used to simulate and verify the control algorithms of the inverter (device under test (DUT)). During the next phase a real-time hardware-in-the-loop (HIL) test is conducted to ensure proper function of the software and signal processing system [1]. The next step is the validation on a machine test bench. In many cases, however, the electric machine is yet unavailable because of the fast development process. A power hardware-in-the-loop (PHIL) test bench can be used to test the inverter without the electrical machine [2].

Compared to a HIL system, electrical power is exchanged when using a PHIL system. An additional benefit of a PHIL test bench is that several machines can be emulated without the need for more space and investment. The time consuming installation of various different machines is not needed anymore. In addition electrical and mechanical faults like a blocking rotor, sudden change of moment of inertia or winding short circuits, can be investigated without any damage.

Figure 1 shows the possibilities of testing the DUT with either a PHIL test bench or with a machine test bench. The PHIL test bench emulates an electrical machine by using an inverter, a coupling network and a real-time simulation system. The interface of the electrical machine and the PHIL is identical to ensure that no modified software on the DUT is needed.

This paper presents a PHIL test bench for the emulation of a highly utilized permanent magnet synchronous machine based on a square-wave powered Modular Multilevel Converter (SPMMC) [3, 4, 5]. The theory of the PHIL real-time simulation system was already introduced in [6, 7] and a brief introduction including the time-discrete model will be given in Section 1. Some practical implementation

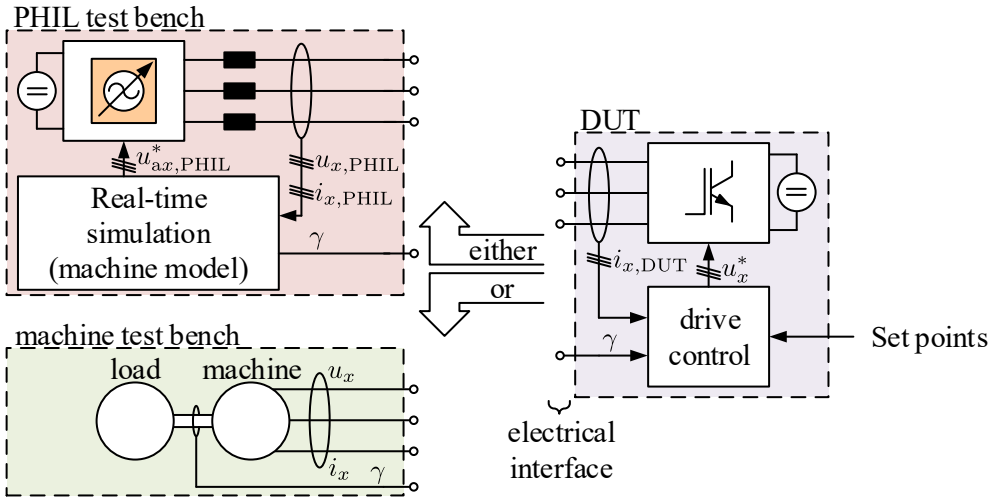



Fig. 1: Overview of testing the device under test either with a PHIL test bench or with a machine test bench

considerations are given for a successful operation of the derived time discrete model in conjunction with a PHIL inverter in Section 2. The used PHIL inverter, the DUT and the machine are introducted in Section 3. The PHIL test bench is verified and compared against the machine in Section 4. In this Section also the energy and balancing control of the SPMMC will be investigated. The conclusion is stated in Section 5.

# 1 Principle of Operation

A PHIL test bench consists of an inverter, a coupling network and a real-time simulation system, see Figure 1. To emulate an electrical machine, a PHIL test bench should have the identical behavior as the real electrical machine at the interface including the current ripple induced by the DUT. Therefore, a machine model describing the non-linear reaction of the electrical machine depending on the output voltage of the DUT $u_{x,\mathrm{PHIL}}$ is needed. Additionally, a PHIL model must also take care of the coupling network and the PHIL inverter to achieve correct operation. Both models are implemented on the real-time simulation system. The calculated output voltages from the real-time simulation system $u^*_{\mathrm{ax,PHIL}}$ are transferred to the PHIL inverter which is applying the voltage across the coupling network and the DUT.

The PHIL inverter has several requirements to fulfill: To prevent unwanted current flow from the DUT to the PHIL and vice versa, the PHIL inverter supply should be galvanically isolated from the DUT. The induced current ripple from the DUT has also to be emulated. Therefore, it is crucial that the overall PHIL system including the PHIL inverter, the measurement system and the real-time-simulation-system has a low dead time. This is particularly important at the switching instants of the DUT because at that moment also the PHIL has to react and this depends on the dead time in the PHIL system. This requirement leads to a high modulation frequency of the PHIL inverter to be able to update the output voltage $u^*_{\mathrm{ax,PHIL}}$ with low latency. Due to the fact, that an electrical machine does not produce an inherent current ripple, the PHIL inverter should also try to avoid producing additional current ripple. On the one side, this is achieved by a high switching frequency of the PHIL inverter and on the other side by a multilevel output voltage. The current ripple is also reduced for larger inductances in the coupling network, but the disadvantage of a large coupling network is a reduction in current dynamics at a limited output voltage of the PHIL inverter.

The following sections are deriving the needed equations for emulating a permanent magnet synchronous machine (PMSM) in conjunction with the PHIL inverter and the coupling network.

## 1.1 Machine Model

This section shows a derivation of the machine model for the emulated PMSM with saturation and cross-coupling effects [6, 8]. Dielectric currents, spatial air-gap harmonics and temperature effects of the

machine are neglected. The equivalent circuit of a PMSM is shown in Figure 2a and consists of the stator resistances $R_S$ and the stator inductances with their induced voltage ${}^{d\Psi_{Sx}}/_{dt}$ and the stator flux linkages $\Psi_{Sx}$ with phase number $x \in 1,2,3$. $i_x = i_x(\Psi_{S1}, \Psi_{S2}, \Psi_{S3}, \gamma)$ are describing the stator currents depending on the stator flux linkages with $\gamma$ as the electrical angle between the rotor flux-axis and the winding of the first phase. To simplify calculations an identical resistance in all three phases is assumed.

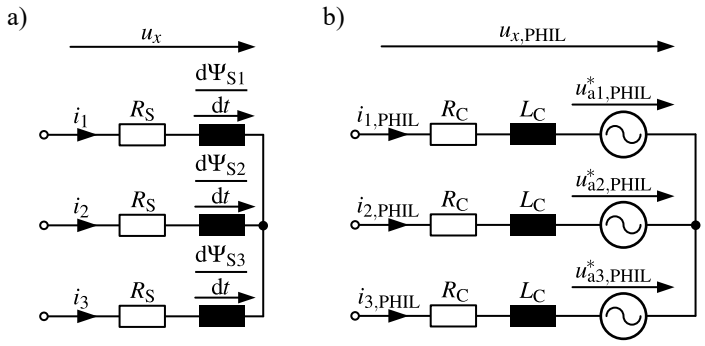



Fig. 2: Equivalent circuits of
a) permanent magnet synchronous machine (PMSM)
b) PHIL inverter with coupling network

The circuit in Figure 2a can then be written down for all three phases:

$$u_x = R_S \cdot i_x + \frac{d\Psi_{Sx}}{dt} \tag{1}$$

Equation (1) is transformed into the dq-system by eq. (2) with the rotor flux-axis $\gamma$ as transformation angle to reduce the amount of stator current function parameters. This results in eqs. (4) and (5) with the use of eq. (3). The dq-stator currents are now described as $i_d = i_d(\Psi_d, \Psi_q)$ and $i_q = i_q(\Psi_d, \Psi_q)$. The functions $i_x(\Psi_d, \Psi_q)$ are obtained by inverting the flux linkage functions $\Psi_x = \Psi_x(i_d, i_q)$. The required stator flux linkages can either be obtained by measurements of a real machine on a test bench or by the use of finite element method (FEM) if the design and used materials are known. The proof that the stator flux linkage functions for a three phase machine are invertible is shown in [8]. The inverse stator flux linkages are shown in fig. 3 and were obtained by measurements of the emulated machine [9]. The saturation and cross-coupling effects of the machine are clearly visible. The electrical angular velocity of the machine is denoted as $\omega = \frac{d\gamma}{dt}$.

$$\underline{x} = \frac{2}{3} \cdot (x_1 + \underline{a} \cdot x_2 + \underline{a}^2 \cdot x_3) \cdot e^{-j\gamma} \qquad \text{with} \qquad \underline{a} = e^{j\frac{2\pi}{3}} \tag{2}$$

$$\underline{x} = x_d + j \cdot x_q \tag{3}$$

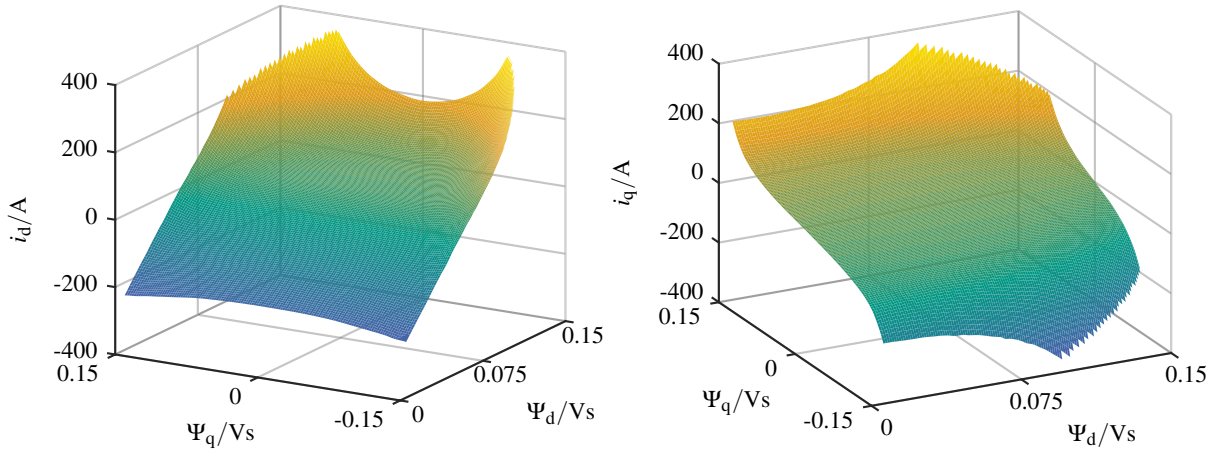
$$u_d = R_S \cdot i_d + \frac{d\Psi_d}{dt} - \omega\Psi_q \tag{4}$$

$$u_q = R_S \cdot i_q + \frac{d\Psi_q}{dt} + \omega\Psi_d \tag{5}$$

The eqs. (4) and (5) are describing the complete machine. The model is only fed by the output voltage of DUT $u_d$ and $u_q$. The stator resistance $R_S$ is constant over time and $i_d = i_d(\Psi_d, \Psi_q)$ and $i_q = i_q(\Psi_d, \Psi_q)$ are depending only on the stator flux linkages. The stator flux linkages $\Psi_d$ and $\Psi_q$ are obtained by integration after rearranging eqs. (4) and (5) to the derivatives ${}^{d\Psi_x}/_{dt}$.

## 1.2 PHIL Model

In this section the transformed model of the PHIL inverter including the coupling network is presented. The equivalent circuit of the PHIL test bench is shown in Figure 2b) with the resistance $R_C$ and inductance $L_C$ of the coupling network and the output voltage of the PHIL inverter $u^*_{ax,PHIL}$. The circuit for all three




(a) current $i_d$ depending on the stator flux linkages

(b) current $i_q$ depending on the stator flux linkages

Fig. 3: stator currents depending on the stator flux linkages $\Psi_d$ and $\Psi_q$

phases can be written down:

$$u_{x,\mathrm{PHIL}} = R_C \cdot i_{x,\mathrm{PHIL}} + L_C \frac{\mathrm{d}i_{x,\mathrm{PHIL}}}{\mathrm{d}t} + u^*_{\mathrm{a}x,\mathrm{PHIL}} \tag{6}$$

The transformation in eq. (2) is also used to transform the PHIL model into the dq-system with the rotor flux-axis $\gamma$ as transformation angle. The resulting PHIL model in the dq-system is shown in eqs. (7) and (8) and the equation is rearranged to the output voltage of the PHIL inverter $u^*_{\mathrm{ad,PHIL}}$ and $u^*_{\mathrm{aq,PHIL}}$.

$$u^*_{\mathrm{ad,PHIL}} = u_{\mathrm{d,PHIL}} - R_C \cdot i_{\mathrm{d,PHIL}} - L_C \cdot \frac{\mathrm{d}i_{\mathrm{d,PHIL}}}{\mathrm{d}t} + L_C \cdot \omega i_{\mathrm{q,PHIL}} \tag{7}$$

$$u^*_{\mathrm{aq,PHIL}} = u_{\mathrm{q,PHIL}} - R_C \cdot i_{\mathrm{q,PHIL}} - L_C \cdot \frac{\mathrm{d}i_{\mathrm{q,PHIL}}}{\mathrm{d}t} - L_C \cdot \omega i_{\mathrm{d,PHIL}} \tag{8}$$

According to Figure 2 the eqs. (9) and (10) are derived. Equation (9) states that the voltage across the machine model and the PHIL inverter is equal since both are controlled from the DUT. Equation (10) demands that the currents from the PHIL inverter are the same than in the real machine which is the main focus of a PHIL test bench.

$$u_{x,\mathrm{PHIL}} = u_x \tag{9}$$

$$i_{x,\mathrm{PHIL}} \stackrel{!}{=} i_x \tag{10}$$

This information is used to calculate the output voltage of the PHIL inverter $u^*_{\mathrm{ad,PHIL}}$ respectively $u^*_{\mathrm{aq,PHIL}}$. The voltages $u_{\mathrm{d,PHIL}}$ and $u_{\mathrm{q,PHIL}}$ are measured at the terminal of the DUT and are equal to the machine model voltages $u_d$ and $u_q$ from the eqs. (4) and (5).

### 1.3 Time Discretization

In the former sections the needed model equations were derived in the time continuous domain. For an implementation on a field-programmable gate array (FPGA) they have to be transformed in the Laplace domain and afterwards into the time discrete Z-domain. The results for the eqs. (4), (5), (7) and (8) in the Z-domain by using the forward euler rule in eq. (11) are shown in eqs. (12) to (15). The forward euler rule was chosen due to achieve a stable time discrete implementation. The sampling time of the discrete system is denoted as $T_s$:

$$s = \frac{z-1}{T_s} \tag{11}$$

$$\Psi_d = \Psi_d \cdot z^{-1} + T_s \cdot (u_d - R_S \cdot i_d + \omega \Psi_q) \tag{12}$$

$$\Psi_q = \Psi_q \cdot z^{-1} + T_s \cdot (u_q - R_S \cdot i_q - \omega \Psi_d) \tag{13}$$

$$u^*_{\mathrm{ad,PHIL}} = u_{\mathrm{d,PHIL}} - R_\mathrm{C} \cdot i_{\mathrm{d,PHIL}} - L_\mathrm{C} \cdot i_{\mathrm{d,PHIL}} \cdot \frac{(1-z^{-1})}{T_\mathrm{s}} + L_\mathrm{C} \cdot \omega i_{\mathrm{q,PHIL}} \tag{14}$$

$$u^*_{\mathrm{aq,PHIL}} = u_{\mathrm{q,PHIL}} - R_\mathrm{C} \cdot i_{\mathrm{q,PHIL}} - L_\mathrm{C} \cdot i_{\mathrm{q,PHIL}} \cdot \frac{(1-z^{-1})}{T_\mathrm{s}} - L_\mathrm{C} \cdot \omega i_{\mathrm{d,PHIL}} \tag{15}$$

# 2 Considerations for Practical Implementation

In this section practical hints for the implementation on a test bench are given.

## 2.1 Lookup-Tables

The emulated machine has a non-linear behavior and the inverse stator flux-linkages must be stored in lookup-tables (LUT). If an analytic formula for the inverse flux linkage exists this can be used instead of a LUT. Due to memory restrictions the size and resolution of the LUT is limited. The LUTs are used to obtain the actual currents in the machine and are fed into the PHIL model to inject the currents into the DUT. To achieve a smooth transition between the breakpoints of the LUTs an interpolation, e. g. bilinear interpolation, is needed. Otherwise, there will be steps in the obtained values leading to problems because of the derivations in eqs. (14) and (15).

## 2.2 Overlayed Current Controller

The current $i_{x,\mathrm{PHIL}}$ is open loop controlled from the machine model by the PHIL inverter. Due to offset error, linearity errors, model, parameter and measurement errors the emulated current $i_{x,\mathrm{PHIL}}$ will vary from the machine model current $i_x$. This will lead to inaccurate emulation results since the DUT measures another current than the machine model has calculated. The solution is to use a proportional controller [7] to control the current $i_{x,\mathrm{PHIL}}$ according to the machine model currents $i_x$, see eqs. (16) and (17). The calculated output voltage from eqs. (14) and (15) is corrected by the proportional factor $K_\mathrm{P}$ and the difference between the machine model current and the real current.

$$u^*_{\mathrm{ad,PHIL,corr}} = u^*_{\mathrm{ad,PHIL}} + K_\mathrm{P} \cdot (i_\mathrm{d} - i_{\mathrm{d,PHIL}}) \tag{16}$$

$$u^*_{\mathrm{aq,PHIL,corr}} = u^*_{\mathrm{aq,PHIL}} + K_\mathrm{P} \cdot (i_\mathrm{q} - i_{\mathrm{q,PHIL}}) \tag{17}$$

The proportional factor $K_\mathrm{P}$ heavily depends on the quality of the used measurement equipment and PHIL inverter and, therefore, no specific values can be given.

## 2.3 Downsampling of the Output Voltage

The sampling time $T_\mathrm{s}$ of the model should be as low as possible to achieve a good measurement of the output voltage of the DUT, especially during switching instants. The modulation period $T_\mathrm{m}$ of the PHIL inverter is usually higher than the sampling time $T_\mathrm{s}$. This means that the model is updating its output voltage $F = {}^{T_\mathrm{m}}/_{T_\mathrm{s}}$-times during one modulation period of the PHIL inverter. Best results were obtained with a moving average filter over $\lfloor F + 0.5 \rfloor$ samples of the model outputs. This calculates the average output voltage of the PHIL model during one modulation period and is then applied across the PHIL coupling network and the DUT which leads to the correct average voltage at the coupling network.

# 3 Laboratory Setup

## 3.1 PHIL Test Bench

In this section the PHIL test bench is explained. As real-time simulation processing system a PicoZed™ System-On-Module (SOM) based on a Xilinx Zynq®-7030 is used. For this SOM a carrier card [10] was designed with additional I/Os for emulating an incremental encoder for the DUT, communicating with the human machine interface (HMI) and for transferring the output voltages $u^*_{\mathrm{ax,PHIL}}$ to the PHIL inverter. For measuring the output voltage of the DUT $u_{x,\mathrm{PHIL}}$ and the phase currents $i_{x,\mathrm{PHIL}}$ LTC2323-14 analog-digital-converters with a sample rate of $4.878\,\mathrm{MS\,s^{-1}}$ are used. Analog frontends for voltage and current scaling are used. The Zynq®-7030 is a Kintex-7 FPGA including about 1.2 MiB block RAM supported by two ARM Cortex-A9 cores. The Zynq-FPGA is used for the real-time simulation of the

machine model and the LUTs for the non-linear model are stored in the block RAM. The machine model calculations are performed in fixed-point math and are running at a calculation frequency of 2.439 MHz. Because the calculation for the machine model takes longer than the time for ADC sampling every second ADC sample is used. On one ARM core additional services are managed like changing parameters online for the machine model and on the other arm core an operating system is running for logging, variable observation and communication with the HMI.

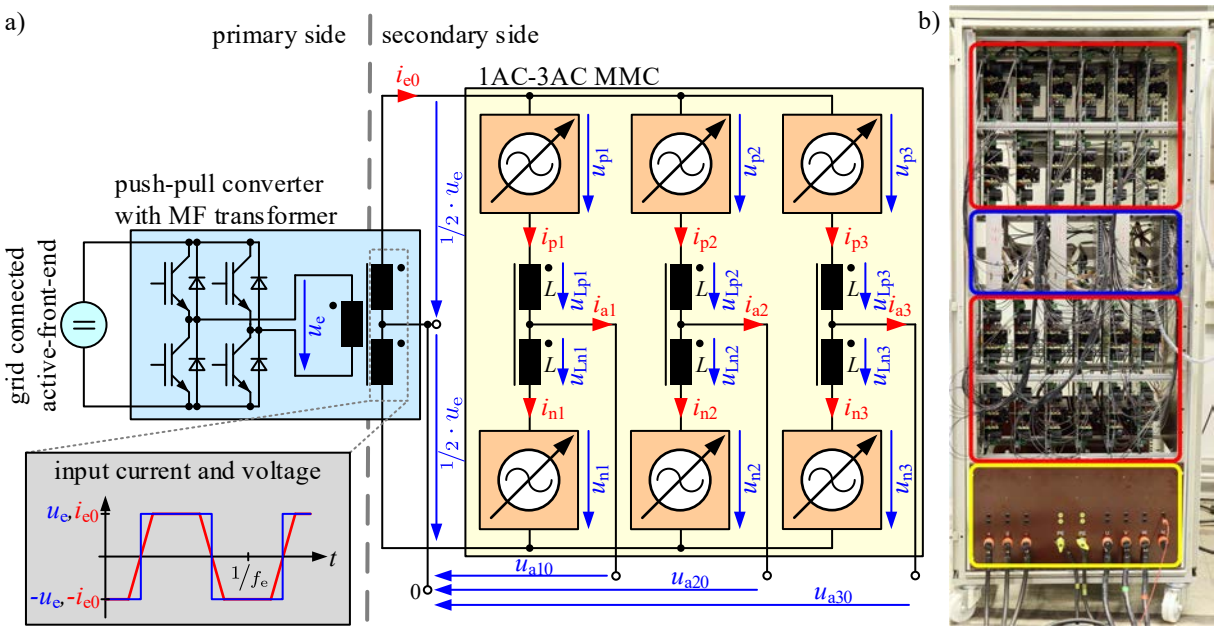



Fig. 4: Overview of the PHIL test bench
a) Schematic diagramm of the PHIL inverter
b) Constructed PHIL inverter with the terminal box (yellow area), the cell boards (red areas) and the signal processing (blue area)

Figure 4a shows the schematic diagram of the used PHIL inverter, introduced in [3] as a square-wave powered 1AC-3AC MMC (SPMMC). The inverter is based on the MMC technology and consists of two arms for each of the three phases. Every arm is built by eight series connected full-bridge low voltage cells described in [4] which leads up to 17 voltage levels at the output. The resulting modulation frequency of the inverter is 100 kHz by utilizing the hybrid control concept presented in [5]. With the hybrid control concept the MMC control is separated in the energy and balancing closed loop control calculated on a digital signal processor (DSP) with a lower control frequency than the modulation frequency and the control of the output voltage on an FPGA with the modulation frequency. The inverter is supplied by a one phase square-wave input voltage $u_e$ which is additionally electrically isolated by a medium frequency (MF) transformer. The input voltage $u_e$ is generated with a push-pull converter which is supplied by an industrial SIEMENS SIMATICS S120 55 kW active-front-end. The coupling network consists of three uncoupled inductors with an inductance of $L_C = 350\,\mu H$.

Figure 4b presents the constructed SPMMC as described above. In the lower part of the inverter is the terminal box (yellow area). The terminals for the input voltage are on the left side and for the output voltage are on the right side. The power connection of the cell boards (red areas) is created via a backplane in the inverter. The communication between the cells and the signal processing (blue area) is done by fibre optic cables. Therefore, each cell has a dedicated Intel®MAX10®-FPGA for measuring the cell capacitor voltage and generating the gate signals for the full-bridge inverter. All cells per phase are connected to one phase-FPGA which does the cell balancing and the measurement of the arm currents. Each phase-FPGA is connected via fibre optic cables to the Cyclone®IV central-FPGA where the DSP TMS320C6748 from TI [11] is connected to. The SPMMC control algorithm is calculated on the DSP. The central-FPGA has also an interface for receiving the SPMMC setpoint voltage from the Zynq-FPGA calculated by the PHIL model. The setpoints for the arms respectively for the cells are then

sent backwards through this chain of FPGAs to the cells.

The DSP additionally controls the industrial active-front-end for the DC supply of the inverter and the push-pull converter of the MF transformer for the electrical isolation.

### 3.2 Machine Test Bench

The used motor test bench consists of the automotive machine HSM1-6.1712-C01 manufactured by Brusa which is an interior permanent magnet synchronous machine with strong saturation and cross-coupling effects, see Figure 3. The machine has three pole pairs with a maximum shaft power of 97 kW, maximum speed of 12 000 $\mathrm{min}^{-1}$ and maximum torque of 220 N m. The recommended DC link voltage is from 300 V to 450 V and the maximum phase current is 300 A.

The power inverter of the DUT is based on the six-pulse bridge Semikron SkiiP 513GD122-3DUL and is working at 300 V DC-link voltage. The control algorithm of the DUT is a predictive current controller for saturated cross-coupled permanent magnet synchronous machines described in [8, 9] and is working at a control and modulation frequency of 8 kHz. The DUT can either be connected to the real machine test bench or to the PHIL test bench to compare the real machine and the PHIL test bench.

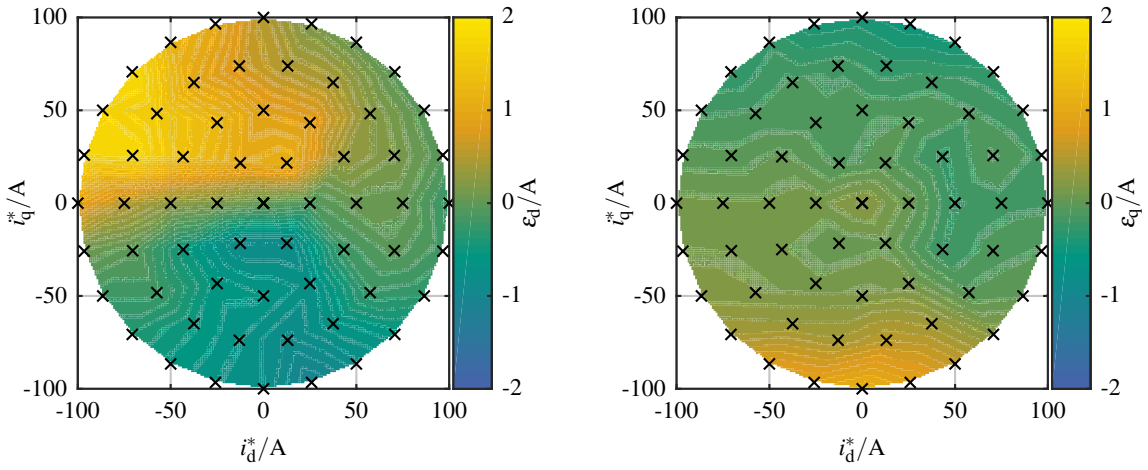
## 4 Experimental Results

This section shows experimental results of stationary and dynamic measurements operated by the DUT. Therefore, the DUT was either connected to the real machine test bench or to the PHIL test bench.

### 4.1 Stationary Measurements

To compare the PHIL test bench against the machine, stationary measurements in the dq-current-plane were conducted. For this measurement the integral term of the DUT controller was disabled and this results in a pure feed-forward control of the machine. This prevents that inaccuracies of the PHIL inverter are compensated by the DUT controller. The difference between the PHIL test bench and machine currents are shown in Figure 5 for the error $\varepsilon_x$ in d- and q-currents. The crosses are depicting the measured values, all other values are interpolated. The error is calculated according eq. (18).

$$\varepsilon_x = i_{x,\mathrm{PHIL}} - i_x \tag{18}$$




(a) Error d-current

(b) Error q-current

Fig. 5: Difference between the currents of the PHIL inverter test bench and the machine measured in the dq-current-plane with $i_\mathrm{d}^*$ and $i_\mathrm{q}^*$ as setpoint values at 1000 $\mathrm{min}^{-1}$

The maximum amplitude of the phase current is limited to 100 A due to the current limitation of the PHIL inverter. The stationary error between the machine and the PHIL inverter is very good since the absolute maximum error is smaller than 2 A in the complete operating area of the PHIL inverter. The occurring errors result due to the PHIL measurement, the PHIL inverter and inaccuracies of the LUTs.

The next measurement shows a comparison of the machine current $i_1$ and the PHIL current $i_{1,\mathrm{PHIL}}$ in phase 1, see Figure 6. The line-to-line voltage of the DUT $u_{12,\mathrm{DUT}}$ and the line-to-line voltage of the PHIL inverter $u_{12,\mathrm{PHIL}}$ is also shown. Both voltages were recorded during the PHIL operation. To reduce ringing from the switching instants all channels have been filtered by a moving-average-filter over 3 samples. The measurement was done with a Keysight MSOX3024T scope and was conducted in the same operating point of the machine and PHIL inverter. For the voltage measurements Keysight N2790A differential probes were used and for the current measurement a Tektronix A6303 current measuring clamp with the measuring amplifier Tektronix AM 503 was used. The scope was triggered by a falling edge of the phase current at 100 A for the machine and the PHIL test bench. The slope of both currents is matched very well but in the switching instants of the DUT deviations between both currents can be seen. This occurs due to the dead time in the PHIL inverter whereby the modulation period is the largest part of the dead time. It also depends if the DUT switching occurs at the begin or the end of a modulation period. The PHIL output voltage $u_{12,\mathrm{PHIL}}$ shows the demand for a PHIL inverter with high dynamics in the output voltage because it must be able to generate fast and short pulses to emulate the current ripple accordingly. Due to the multilevel output voltage of the PHIL inverter a small additional induced current ripple can be identified in $i_{1,\mathrm{PHIL}}$.

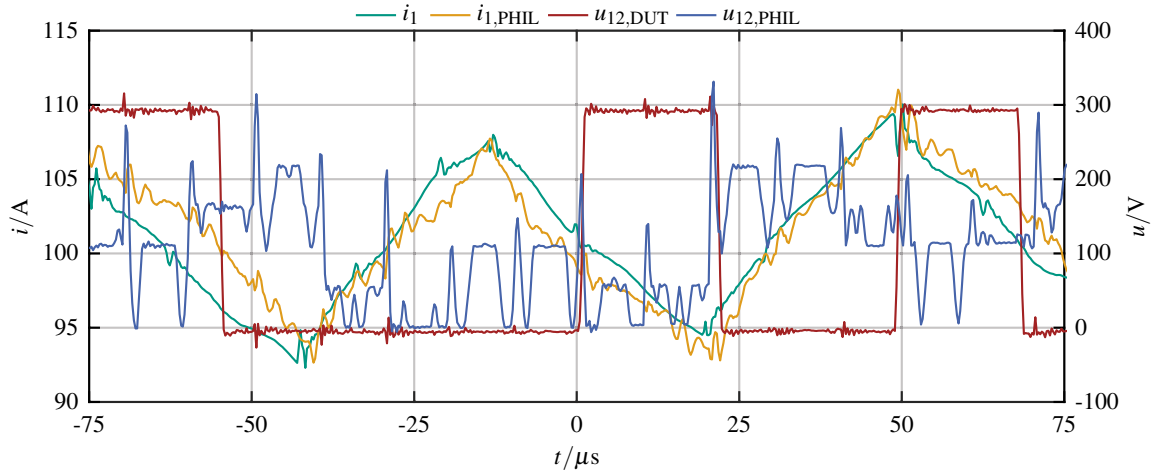


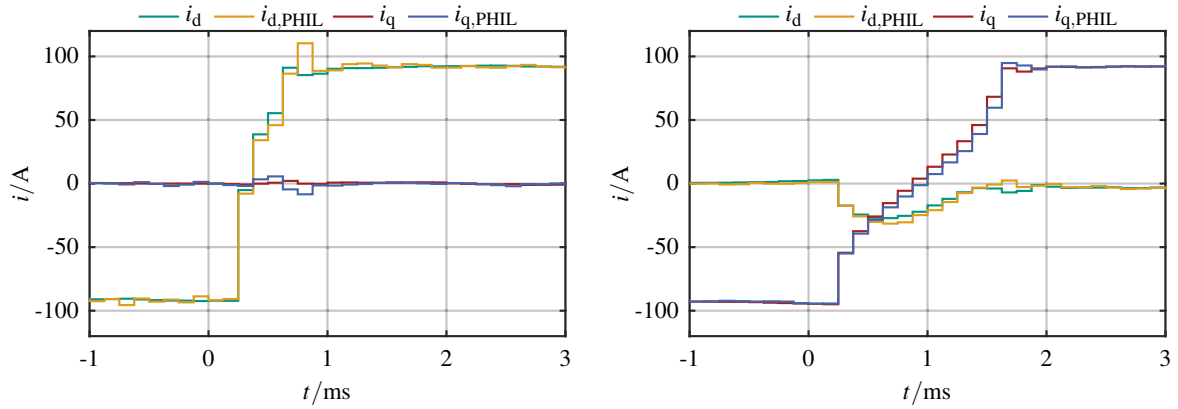

Fig. 6: Scope measurement of machine current $i_1$ and emulated current of the PHIL $i_{1,\mathrm{PHIL}}$ in the same operating point

## 4.2 Dynamic Measurements

Figure 7 shows current reversal steps for either the d- or q-currents with the machine and PHIL test bench at 1000 $\mathrm{min}^{-1}$. The measurements have always been conducted at the same rotor angle $\gamma_{\mathrm{Step}} = \pi$ to ensure same voltage limit conditions for the measurements. The values are sampled with the DUT at its control frequency of 8 kHz. Despite a current setpoint of $\pm 100$ A it is observed that the DUT does not reach the exact setpoints for both machine and PHIL test bench. There are two reasons for this behaviour: The integral term of the DUT controller is disabled and the LUTs for the DUT controller were characterized using only machine quantities. This means that the non-linearity of the DUT is not taken into account and this results in the current deviation. For the measurements this has no negative impact because the machine and the PHIL test bench are showing the same behavior.

Figure 7a shows the current step in the d-axis. Before and after the step the values of the machine and the PHIL test bench are identical. The jitter in the current $i_{\mathrm{d,PHIL}}$ is slightly higher than in $i_{\mathrm{d}}$. The reason for that is the small differential inductance in the d-axis in this operating point. During the step the deviations are, despite the high dynamics, with $\approx 20$ A in the d-current low.

Figure 7b shows the current step in the q-axis. As in Figure 7a the currents before and after the step are identical between the machine and the PHIL test bench. The jitter in $i_{\mathrm{d,PHIL}}$ disappeared because at 0 A the differential inductance of the machine is larger and, therefore, easier to emulate. During the step the deviations are, despite the high dynamics, with $\approx 10$ A in the q-current low. In $i_{\mathrm{d}}$ the cross-coupling effects of the used machine can be seen. The PHIL test bench is also able to emulate this behaviour.




(a) d-current step from $-100\,A$ to $+100\,A$ (b) q-current step from $-100\,A$ to $+100\,A$

Fig. 7: Current reversal step in either d- or q-current in comparison with the machine and PHIL test bench at $1000\,min^{-1}$

Figure 8 shows a torque reversal step from $-70\,Nm$ to $+70\,Nm$ at $+4000\,min^{-1}$. Figure 8a shows the sampled d- and q-currents of the DUT. Figure 8b shows the six arm capacitor voltages of the SPMMC. The setpoint of the arm capacitor voltage is 880 V and is perfectly controlled and balanced. Only during the torque reversal step the arm capacitor voltage slightly rises because of the changing power flow from $\approx +29\,kW$ to $\approx -29\,kW$ (a positive sign denotes a power flow from the PHIL inverter to the DUT). This demonstrates that the MMC energy and balancing control also works very well in PHIL operation mode.

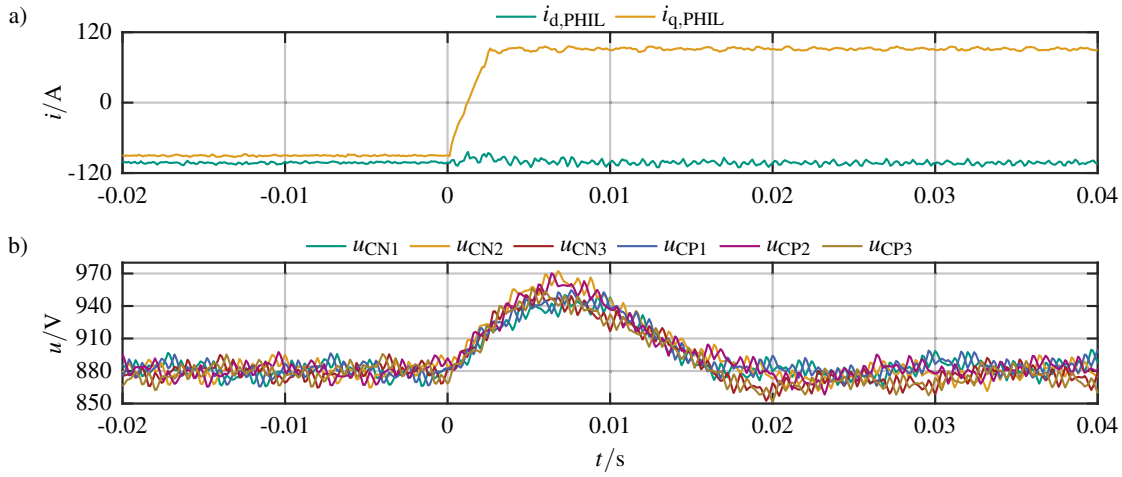



Fig. 8: Arm capacitor voltages of the SPMMC during torque reversal step from $-70\,Nm$ to $+70\,Nm$ at $+4000\,min^{-1}$

## 5 Conclusion

This paper presents a power hardware-in-the-loop (PHIL) test bench for emulation of highly utilized permanent magnet synchronous machines (PMSM) based on a square-wave powered Modular Multilevel Converter (SPMMC). First, the different abstraction levels of simulations like hardware-in-the-loop and power hardware-in-the-loop (PHIL) are described. Then an introduction and derivation of the machine and PHIL model is given. The result for a time discrete implementation of a non-linear and cross-coupled synchronous machine is shown by using lookup-tables for the inverse stator flux linkages. Additionally, practical implementation hints are given for a successful operation of the derived time discrete model in conjunction with a PHIL inverter. Afterwards, the device under test (DUT) and the PHIL test bench have been explained in detail, especially the PHIL inverter and the real-time simulation system. The PHIL test bench has been verified and compared against a highliy utilized PMSM both operated with the DUT. Static and dynamic measurements have been conducted to show the excellent emulation quality of the

PHIL inverter. The successful energy and balancing control of the arm capacitor voltages of the SPMMC has been demonstrated during a reversal torque step. The SPMMC as a PHIL test bench can be used for a wide field of applications like medium and high voltage power grid emulation and testing of electrical components.

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